gri-909

pulse input detector

GRI-909

PULSE INPUT DETECTOR

MANUAL

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PULSE INPUT DETECTOR MANUAL

1.0 <u>Specifications</u>:

1.1 <u>Function</u>:

The Pulse Input Detector provides the ability to detect the occurrence of pulse events external to the computer via the interrupt system of the GRI-909.

1.2 <u>Input</u>:

a) The inputs from external devices to the PID are signals which indicate that certain events have occurred. These signals must conform to either TTL or DTL positive logic specification or to the following:

1) $+2.4v \leq logic\ 1 \leq +12v$ from a source resistor greater than 1,000 ohms.

2) $0v \leq logic\ 0 \leq +0.4v$ with a source resistor less than 220 ohms, capable of sinking at least 1.6 milliamperes.

b) Control signals from the computer are shown in Figure 1-1, the block diagram of the PID.

c) The power required is 0.5 amperes of +5v (average).

Application Note:

THE INPUT CIRCUITS ON THE PULSE INPUT DETECTOR ARE HIGH SPEED
DEVICES WHICH ARE, THEREFORE, SUSCEPTIBLE TO NOISE. TO PREVENT
READ-IN ERRORS, INPUTS MUST BE PROPERLY GROUNDED AND CABLES MAY
REQUIRE SHIELDING, TERMINATORS, AND/OR NOISE SUPPRESSORS.

    d)   The time between interrupts on any one line must be greater
than two machine cycles (3.52 microseconds).

1.3 Output:

The output from the PID is one of eight predetermined memory
addresses loaded into the computer's Memory Address Register to
transfer program control to a new sequence of programmed machine
instructions. Only one of these eight addresses can occur at a time.

1.4 Sequence:

The PID registers are cleared when power is turned on or the
START key is depressed.

In use, the operator is enabled by setting its ISR bit, which
sets all eight interrupt signals at the same priority level within
the processor. However, there are eight priority levels on the op-
erator itself. When the interrupt occurs, PID first generates address
104_8 in which the beginning of the subroutine used for that particular
interrupt is stored. These addresses are as follows:

Input	Second Address (Octal)
1	105
2	107
3	111
4	113
5	115
6	117
7	121
8	123

Thus, when an interrupt occurs on input 4, for example, the contents of the sequence counter will be stored in location 104_8, and the program will continue in location 113_8. Since a jump instruction requires two words, location 114_8 contains a starting address of the subroutine.

1.5 Physical Description:

The PID is contained on one 9" X 4" printed circuit board.

2.0 Installation and Testing:

2.1 Installation:

The PID is installed in any location on the I/O bus at the rear of the chassis. Since the unit uses the interrupt system, it is necessary to add jumpers between PINL and POUTL (source bus pin 5 and E) in vacant slots to the left of the PID board viewing the bus from the rear of the machine.

2.2 External Connectors:

The external signals are connected to the PID by wiring the

appropriate pins on the 48-pin Amphenol connector (Part No. S40-203)

using pins made for the purpose (Part No. S40-204). The external

signals are wired as follows:

Input Signal	Pin Designation
1	J
2	K
3	L
4	M
5	N
6	P
7	R
8	S
Ground	A or the two connector mounting screws

Unshielded cable or twisted pair cable is sufficient for most

applications. When co-ax is necessary, ground connections may be

made to pin A or to the two connector mounting screws on the I/O

connector plate.

2.3 Testing:

Testing of the PID is complicated because it requires inputs

from an external device.

In use, the PID could generate program interrupts in random

order and possibly at high speed. GRI has prepared a diagnostic

(DPID) to accomplish this using the BOM operator, which sends eight

of its output signals to the PID in a pre-selected sequence. One

of these sequences uses a random number to test the operator under

almost real conditions. See the program description for more detail.

An alternative to using this test program is to build the test jig whose schematic is shown in Figure 2-1. This will allow testing the PID under low speed conditions. In use, various inputs are switched on, and the initiate switch is depressed. The machine should halt in the highest priority address. Depress CONTINUE and the machine should halt in the next highest location, depending on the switch positions. A routine to accomplish this is as follows:

Location	Instruction
1	06 0010 04
2	400
3	02 0010 04
4	00 0100 03
5	4
104	0
105	02 0100 00
106	00 0000 07
107	02 0100 00
110	00 0000 07
111	etc.
.	.
.	.
.	.
124	

3.0 <u>Programming Example</u>:

     Assume that PID is being used in a counting application that
requires incrementing a memory location and going to a subroutine
on an overflow. Then the program is as follows:

```
          BEGIN:  MR1       CNTKS-1,AX
                  RM        AX, .+5
                  MR1       -10,AY
                  ZMID      0
                  RS        AY,P1
                  JC        AY,NEZ,.-3
                  MR1       400,1SR
                  FO1       ICO

                              .
                              .
                              .

                  continue program


                  CNTRS   = .
                  CNTR1:  WRD Ø
                              .
                              .
                              .

                  CNTR8:  WRD Ø
          LOC 104
          WRD Ø
          MR1       INP1-1, SC
          MR1       INP2-1, SC
          MR1       INP3-1, SC
          MR1       INP4-1, SC
          MR1       INP5-1, SC
          MR1       INP6-1, SC
          MR1       INP7-1, SC
          MR1       INP8-1, SC
```

```
INP1:     RM1      MSR,∅              ;SAVE MSR

          RM1      TRP,∅              ;SAVE TRP

          MS       CNTR1,P1

          JC       MSR,LTZ,SUB 1      ;GO TO SUB 1 IF BOV

          MR       INP1+1,MSR         ;SUB 1 RETURNS HERE

          FO1      ICO

          MR       104,SC             ;GO BACK TO INTERRUPTED
                                       PROGRAM

INP2:     ETC
```

4.0 Theory of Operation:

This brief description of the operation of PID is based on
system timing, operation, and interfacing information given in
Appendix B of the System Reference Manual. The Logic Block Diagram
of the PID is available (D1747009A) which shows the operation in
detail. The information given here is meant to show the sequence
of operation which will assist in understanding the detailed LBDs.

Refer to the Block Diagram (Fig. A-1) and the Timing Diagram
(Fig. 4-2). At the beginning of any machine cycle, the processor
generates an interrupt synchronize (ISYNH) signal which transfers
interrupt signals stored in Register A into Register B. If ISR bit 8
is set and the conditions specified in Section 2.8 of the Reference
Manual hold, an interrupt occurs. If more than one interrupt request
is stored in Register A at the time of the synchronizing signal, the
Priority Decode Gates select the highest priority interrupt request
for processing.

When the processor starts an interrupt, the Interrupt Address Generator produces address 104_8 on the Destination Data Bus, which is used as the address to store the SC. Then the second address from the Interrupt Address Generator is gated onto the Destination Data Bus and program operation begins from there.

After the interrupt is serviced, the flip flop in Register A corresponding to the interrupt that was just processed is cleared. Thus, it is ready to cause another interrupt in the processor.
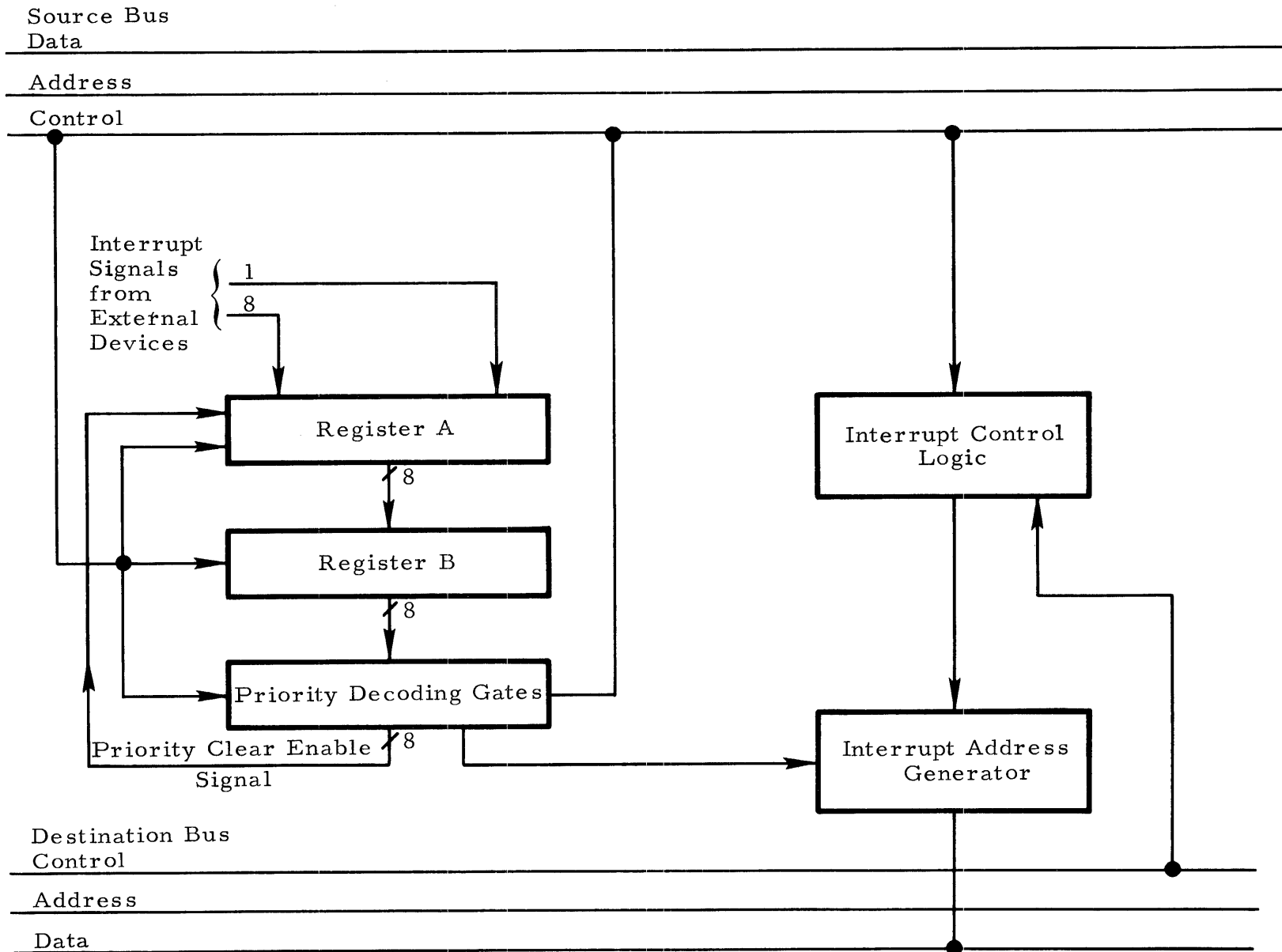
Source Bus
Data

Address

Control

Interrupt
Signals
from
External
Devices

1

8

Register A

8

Register B

8

Priority Decoding Gates

Priority Clear Enable
Signal

8

Interrupt Control
Logic

Interrupt Address
Generator

Destination Bus
Control

Address

Data

Figure 1-1

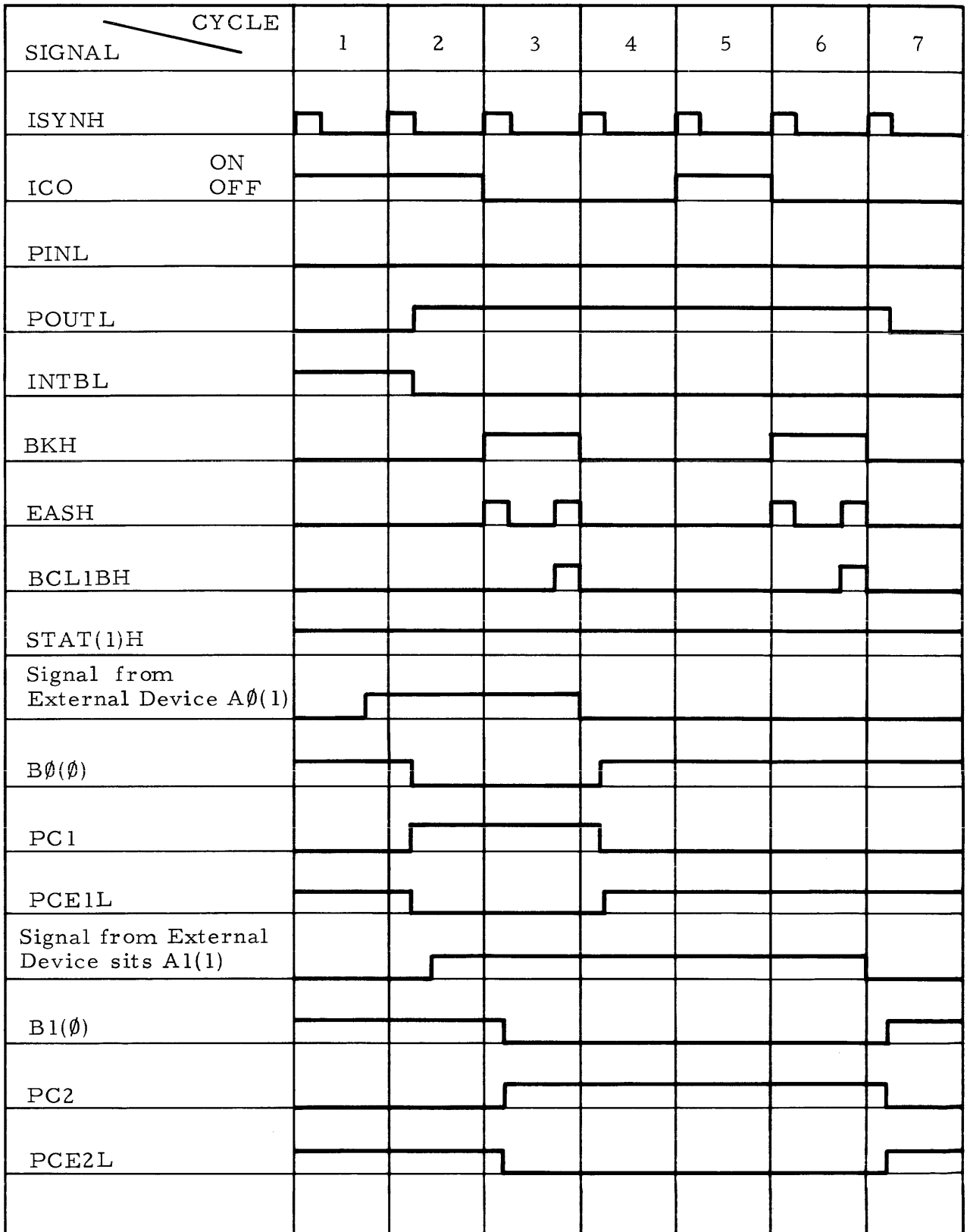| SIGNAL ╲ CYCLE	1	2	3	4	5	6	7
ISYNH							
ICO ON / OFF							
PINL							
POUTL							
INTBL							
BKH							
EASH							
BCL1BH							
STAT(1)H							
Signal from External Device A∅(1)							
B∅(∅)							
PC1							
PCE1L							
Signal from External Device sits A1(1)							
B1(∅)							
PC2							
PCE2L							

Figure 1-2

gri **GRI Computer Corporation**

320 NEEDHAM STREET, NEWTON, MASSACHUSETTS 02164

TEL: (617) 969-0800