gri-909

bim/bom manual

GRI Computer Corporation
320 NEEDHAM STREET, NEWTON, MASSACHUSETTS 02164

Price $3.75

GRI-909

BINARY INPUT MULTIPLEXER

BINARY OUTPUT MULTIPLEXER

MANUAL

GRI Computer Corporation, 320 Needham Street, Newton, Massachusetts 02164

Printed in U.S.A. Supercedes December 1970

10-40-003-A
1270-200

TABLE OF CONTENTS

CHAPTER ONE

BINARY INPUT MULTIPLEXER

1.0 Introduction:

Many transducers are switches or other on-off devices which indicate process states, valve positions, or alarm states. The BIM provides up to 32 cut-off inputs providing a simple means of interfacing such information. The function of the Binary Input Multiplexer is to assemble these discrete digital inputs into two 16 bit words for entry into and processing by the computer.

1.1 Specifications:

Input:

The inputs to the BIM are:

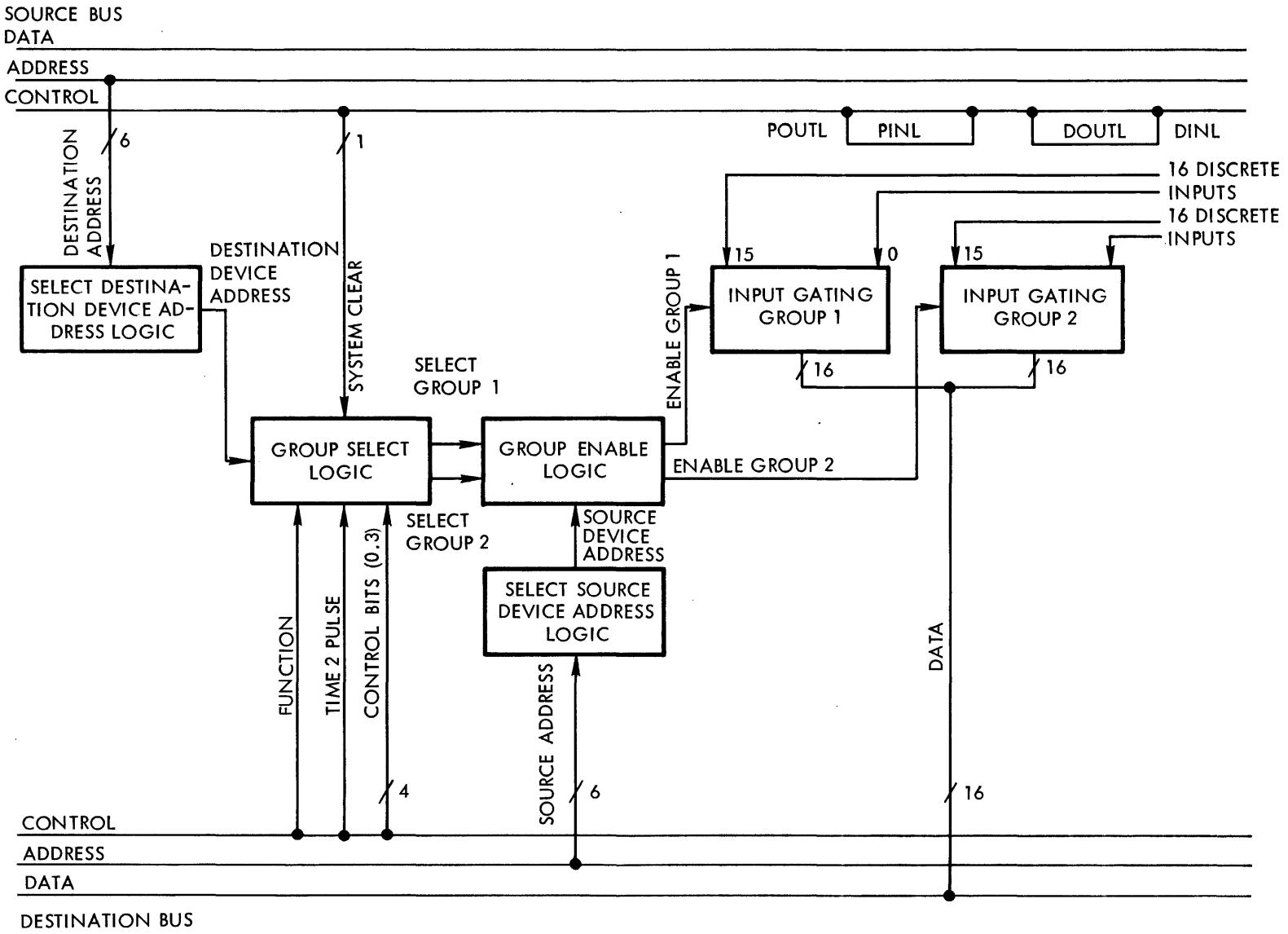
a. The on-off signals from external devices which conform to either TTL or DTL positive logic specifications or to the following:

   +2.4 volts $\leq$ logic 1 $\leq$ +12 volts from a source resistance greater than 1000 ohms.

   0 volts $\leq$ logic 0 $\leq$ 0.4 volts with a source resistance less than 220 ohms, capable of sinking at least 1.6 milliamperes.

b. Control signals from the computer as shown in Figure 1-1, which is a block diagram of the BIM system.

c. Power: 0.2 amp of +5v (average).



GRI BIM OPERATOR BLOCK DIAGRAM

FIGURE 1-1

Application Note:

THE INPUT CIRCUITS ON THE BINARY INPUT MULTIPLEXER ARE HIGH SPEED DEVICES WHICH ARE, THEREFORE, SUSCEPTIBLE TO NOISE. TO PREVENT READ-IN ERRORS, INPUTS MUST BE PROPERLY GROUNDED AND CABLES MAY REQUIRE SHIELDING, TERMINATORS, AND/OR NOISE SUPPRESSORS.

Output:

The outputs from the BIM are two 16-bit words that represent the status of the discrete digital signals. These words are fed to the destination bus of the processor.

Sequence:

In use, the 32 discrete digital signals are assembled into a register or memory by first selecting one of the 16-bit groups and then performing a register-to-register, register-to-memory transfer, or a data test operation. The group selection remains valid, once selected, until changed by another selection command, or until power is turned off, or the START key depressed.

1.2 Installation and Testing:

Installation:

The BIM is installed in any location in the IO bus at the rear of the chassis. Since neither direct memory access nor priority interrupt is used on BIM, it is not necessary to add jumpers between PINL and POUTL (source bus pins 5 and E) and DINL and DOUTL (source bus pins 6 and F) in vacant slots to the left of the BIM board. These jumpers will only be required if there are Interrupt or DMA devices to the right of BIM (viewing the IO bus from the rear of the

machine).

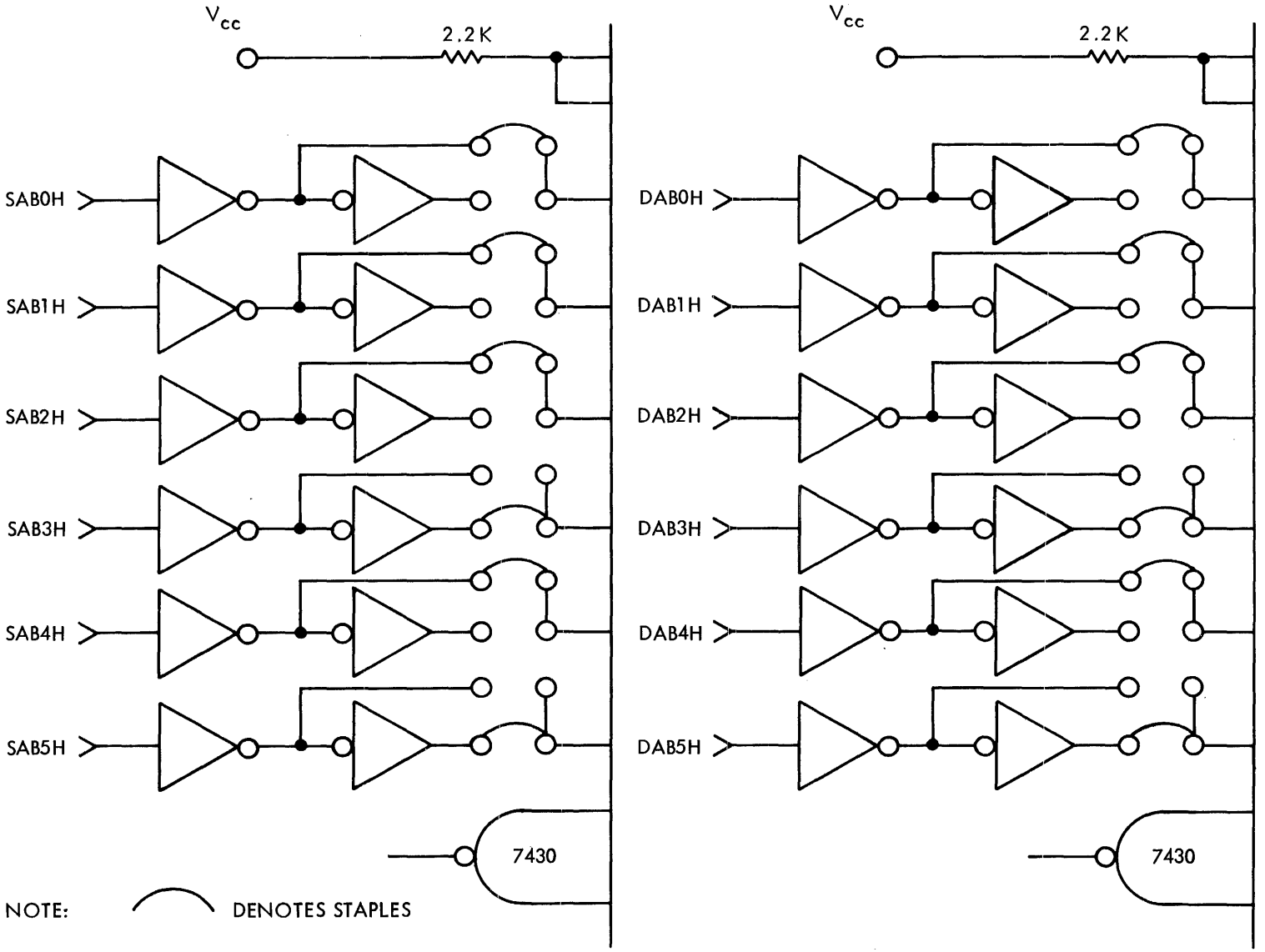
Any unused source or destination address may be specified, and the address is selected by clipping staples from an address selector on the printed circuit board. Figure 1-2 shows the BIM operator set up for source and destination address 50.

FO control bits are used to select one of the 16-bit groups; therefore, staples on the printed circuit board must be clipped to implement the selection. Note that two BIMs can be installed with the same source and destination address but with different Control Bits selected, i.e. BIM1 uses CB0 and CB1 and BIM2 uses CB2 and CB3.

External Connections:

The external signals are connected to BIM by wiring to the appropriate pins on the 48-pin Amphenol connector (Part No. S40-203) using pins made for the purpose (Part S40-204). The external signals are wired as follows:

Input Signals	PIN NUMBER Group 1	Group 2
1	4	1
2	D	B
3	F	A
4	6	2
5	12	K
6	M	8
7	N	J
8	11	9
9	15	14



BIM SET FOR SDA,DDA = 50_8

Figure 1-2

Input Signals	PIN NUMBER Group 1	Group 2
10	S	R
11	17	18
12	U	V
13	24	X
14	b	20
15	a	Y
16	23	21
GROUND	7, H, P, 13, 19, W, 25, C	c, 3, 10, L, 16, T, 22, Z

Unshielded ribbon or twisted pair cable is sufficient for most applications. When Co-ax is necessary, ground connections may be made to the unused connector pins or to the two connector mounting screws.

Testing:

A simple key-in loop to display BIM in 27 is coded as follows:

```
BEG:    RR SWR,AX          10  0000 11
        RRC 06,AY          06  0010  12
        FO 0,BIM           02  0000  50
        RM AO, .+2         13  0000  06
        FO 0,BIM           02  0000  50
        RR BIM,27          50  0000  27
        JU BEG             00  0100  03
```

1.3 Programming:

Coding:

Assume the following address and control definitions have been selected:

GP1 = 1
GP2 = 2
BIM = 50

Programming this operator is quite simple, since all that is required is to select a group and then to transfer the data from BIM to hardware register or memory location. As long as the same group is to be read by the program, it need not be selected by an FO command again. Turning power off and on or depressing START results in clearing the group selection (i.e. no group selected). For instance, to transmit Group 1 to the AX, code as follows:

```
FO GP1,BIM     02  0001  50
RR BIM,AX      50  0000  11
```

To transmit Group 2 to a memory location

```
FO GP2,BIM     02  0010  50
RM BIM,06      50  0000  06
   XXXX            XXXX
```

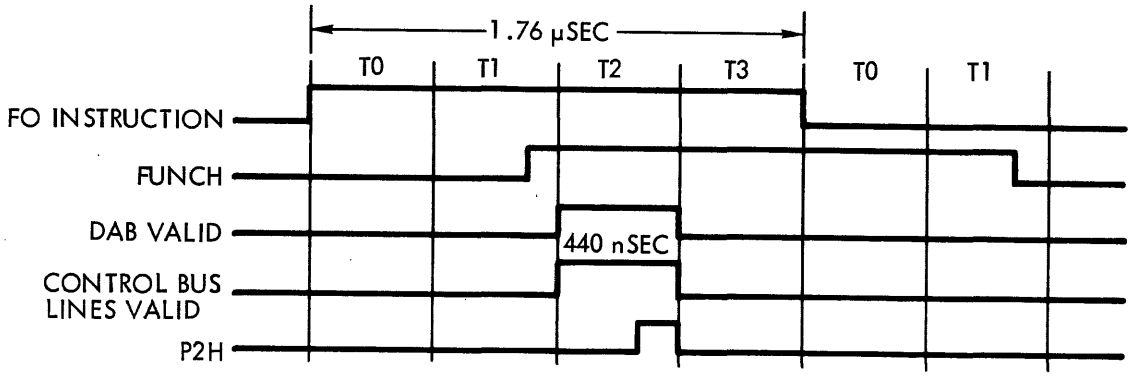
The inclusive OR of the two groups can be formed by selecting both groups and is often useful for determining if any one or more of 32 inputs are "1's".

```
FO GP1,GP2,BIM     02  0011  50
JC BIM,NEZ,100     50  0100  03
                       100
```

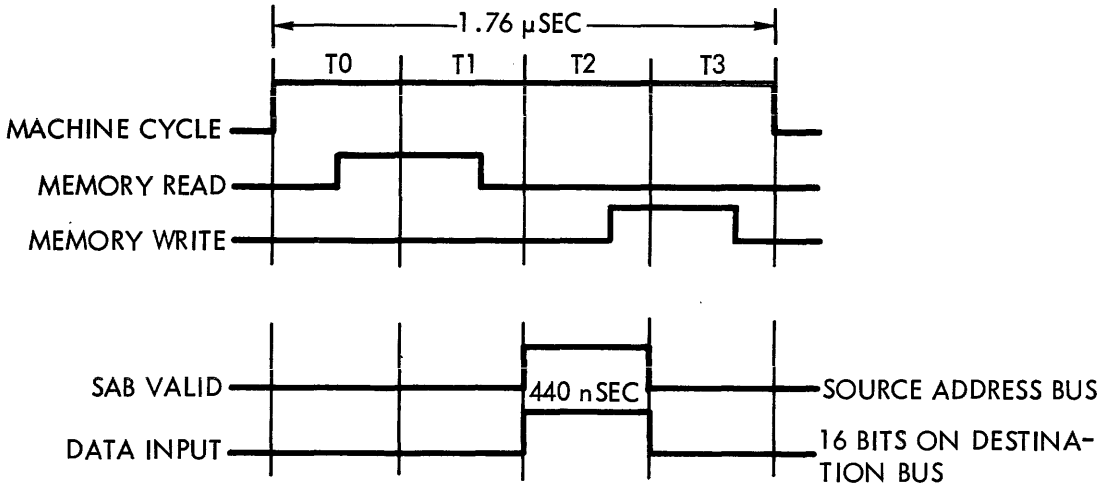
1.4 Theory of Operation:

In the discussion that follows, it will be assumed that the reader understands digital techniques; thus, only highlights of the operation will be mentioned. Logic Block Diagram D 17 47 003 should be referred to for troubleshooting or similar use.

Recall from Section 1.3 (Programming) that the first line of code selects the group of discrete signals to be assembled onto the destination bus for transfer to some specified register or memory location. This selection is made by an FO instruction, which delivers four pulses to operators for setting or clearing flip flops. The block "SELECT DDA LOGIC" consists of a six input gate which decodes the destination address lines DAB0H to DAB5H, so only this device responds when it is specified as a destination. Thus, when the BIM address is selected as a destination, the block "GROUP SELECT LOGIC" is enabled and depending on the combination of control bits, CB0H to CB3H selects either Group 1, Group 2, or both. The timing is shown in Figure 1-3.



The next line of code transfers the state of the external discrete signals into the processor. This is accomplished by decoding the source address lines in block "SELECT SDA LOGIC". When the address on the source bus is valid, either or both of the "GROUP ENABLE" lines cause the information at the input of the "INPUT GATING" block to be transferred to the destination bus data lines. Timing is shown in Figure 1-4.



BIM TIMING

Figure 1-4

CHAPTER TWO

BINARY OUTPUT MULTIPLEXER

2.0 Introduction:

The Binary Output Multiplexer is the interface connecting the GRI-909 Computer to various on-off devices. Thus, the function of the BOM is to provide the capability to control the state of such devices as solenoid valves, electric motor starters, lamps, and latching relays. There are two versions of BOM, one for logic outputs, one for drive relays; up to 32 binary outputs can be interfaced with the BOM.

2.1 Specifications:

Input:

The inputs to the BOM are

a) Control signals as shown on Figure 2-1, which is a block diagram of the BOM.

b) The 16-bit data word that represents the state of the output devices.

c) Power: 0.5 amps of +5 volts (average).

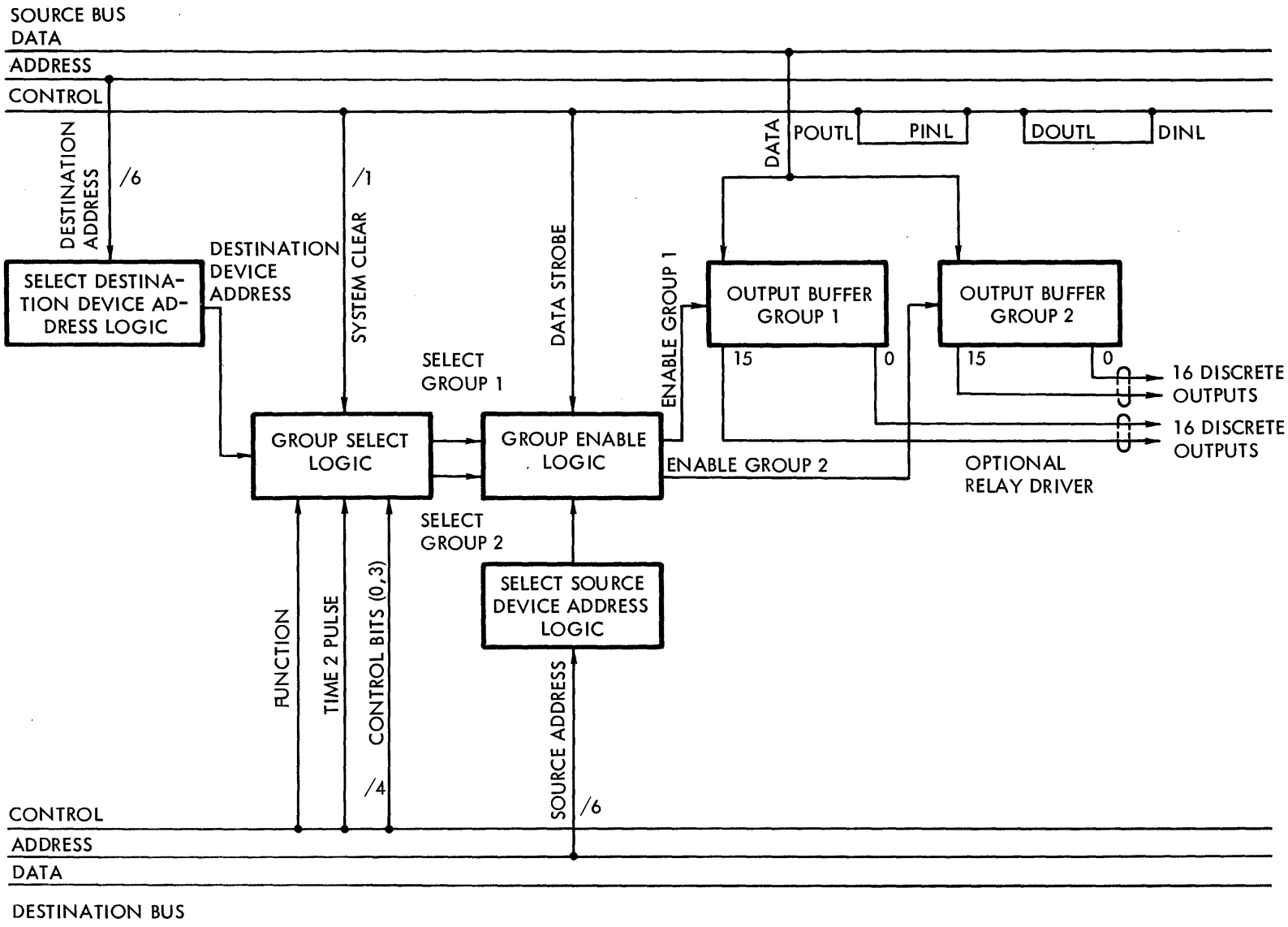
Outputs:

a) Two 16-bit words that represent the desired state of on-off devices to be controlled. The standard output is:

   1) In the logical zero state, the output is 0.4V and will sink 16 ma.

   2) In the logical one state, the output is between 2.4V and 5.0V and will drive 400 microamps.

b) The optional relay drive buffers will drive relays which require up to 30V to the coil. Since the power dissipation is limited, refer to the section on Operation for a detailed discussion of this option.



GRI BOM OPERATOR BLOCK DIAGRAM

Figure 2-1

Sequence:

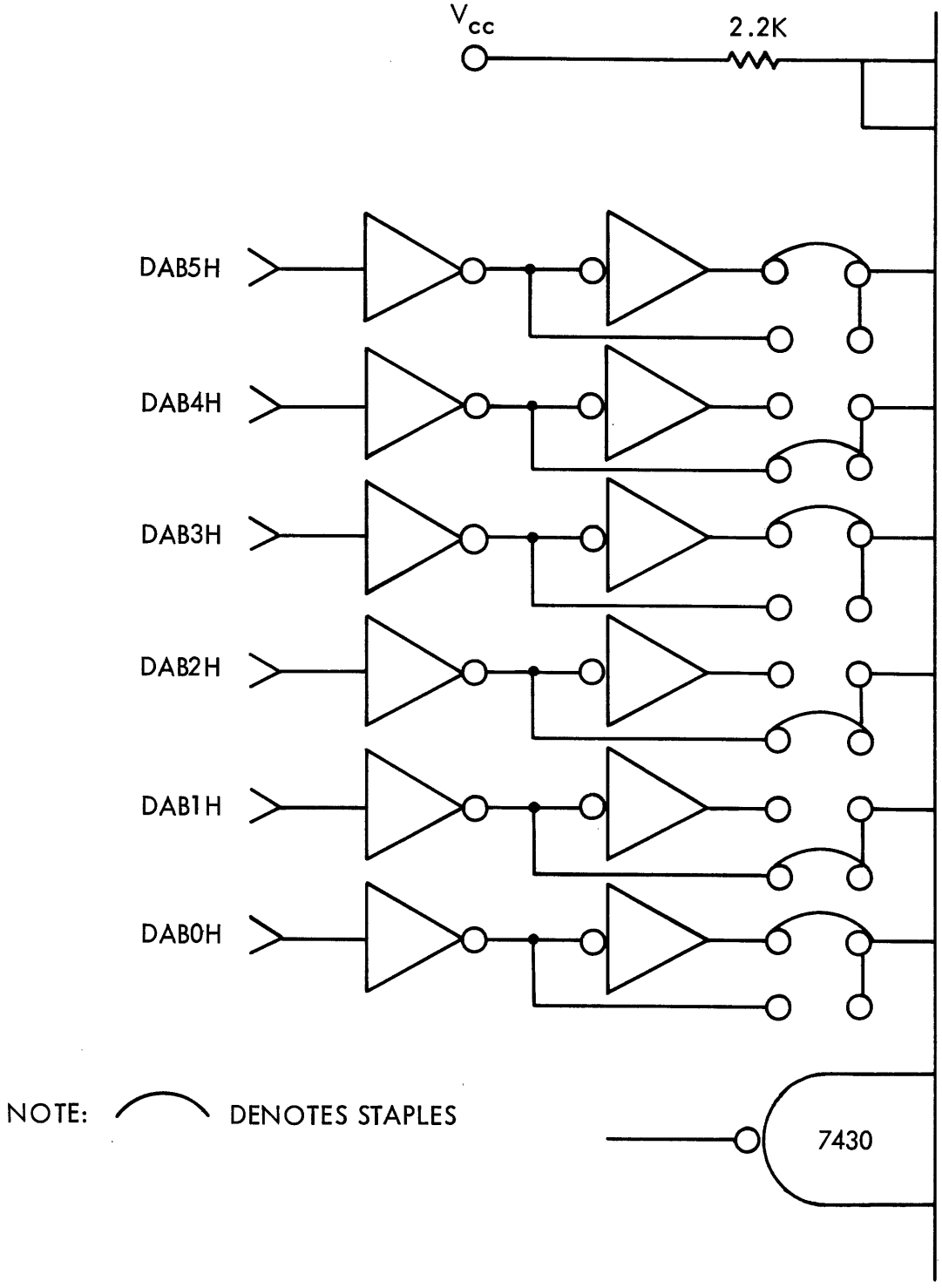
In use, the 32 discrete outputs are transferred to the external output device by first selecting one of the 16-bit groups and then performing a register-to-register or memory-to-register transfer.

2.2 Installation and Testing:

Installation:

The BOM is installed in any location in the IO bus at the rear of the chassis. Since neither direct memory access nor priority interrupt is used on BOM, it is not necessary to add jumpers between PINL and POUTL (source bus pins 5 and E) and DINL and DOUTL (source bus pins 6 and F) in vacant slots to the left of the BOM board. These jumpers will only be required if there are interrupt or DMA devices to the right of BOM (viewing the IO bus from the rear of the machine).

Any unused destination address may be specified, and the address is selected by clipping staples from an address selector on the printed circuit board. Figure 2-2 shows the operator set up for a destination address 51.



BOM SET FOR DDA = 51_8

Figure 2-2

FO control bits are used to select one of the 16-bit groups; therefore, staples on the printed circuit board must be clipped to implement the selection. Note that two BOMs can be installed with the same source and destination address but with different Control Bits selected, i.e. BOM1 uses CB0 and CB1 and BOM2 uses CB2 and CB3.

External Connections:

The BOM is connected to the external device by wiring to the appropriate pins on the 48-pin Amphenol connector (Part No. S40-203) using pins made for the purpose, (Part. No. S40-204). The external signals are wired as follows:

Output Signal	PIN NUMBER Group 1	Group 2
1	F	2
2	D	1
3	B	4
4	A	6
5	N	8
6	M	12
7	K	11
8	J	9
9	V	17
10	U	18
11	S	15
12	R	14
13	b	21

Output Signal	PIN NUMBER Group 1	Group 2
14	a	23
15	y	24
16	x	20
GROUND	C, H, L, P, T, W, Z, C	3, 7, 10, 13, 16, 19, 22, 25

Unshielded ribbon or twisted pair cable is sufficient for most applications. When Co-ax is necessary, ground connections may be made to the unused connector pins or to the two connector mounting screws.

Testing:

A simple key in loop will suffice for simple go-no go testing of all outputs. The problem will be to determine whether each output is actually functioning. The logic level output registers (8H90 buffers) will drive a 6.3v, 20ma bulb returned to +5v. The following loop can be used to activate each output from the console switches for Group 1 or Group 2.

```
0  FO GP1,BOM     02  0001  51
1  RR SWR,BOM     10  0000  51
2  JU .-1               1
```

The instruction in loc 0 may be changed to select either group.

If a BIM, BOM, and special interconnecting cable is available, a complete, high speed exercise and diagnostic called DBIO, 79-43-013 is available. Note that this configuration is intended for use with

logic level BOMs only.

2.3 Programming:

Coding:

Assume the following address and control definitions have been selected and made in the assembler:

BOM = 51

GP1 = 1

GP2 = 2

Programming this operator is quite simple, since all that is required is selecting a group and then transferring the data from a hardware register or memory location to BOM. As long as the same group is being used by the program, it need not be selected by an FO command again. Turning power on and off or depressing START clears the group select logic; thus, no group is selected. For instance, to transmit from the AX to group 1, code as follows:

```
FO GP1,BOM    02  0001  51
RR AX,BOM     11  0000  51
```

To transmit from a memory location

```
FO GP2,BOM    02  0010  51
MR DATA,BOM   06  0000  51
                  XXXX
```

The inclusive OR of the two groups can be formed by selecting both groups and then transmitting the result. This feature is useful for setting all 32 outputs to either zeros or ones.

For example:

```
FO GRP1,GRP2,BOM    02  0011  51
ZR BOM              00  0000  51
```

Relay Driver Option:

The 32 bits are stored in 7475 DC flip flops with Signetics 7406 interface drivers to the external device connector. The 7406 couples low level logic information out of the processor to a higher level and provides the protection of buffer isolation and the advantage of power amplification. The information can now be transmitted through a high noise or power environment to external devices such as relays and lamps.

When using the 8T90, the maximum dissipation rating of 167 milliwatts at 125C must not be exceeded. The following discussion will provide guidelines to insure that this rating will not be exceeded, but if the user is in doubt, refer to the Signetics Corporation Application Notes.

The maximum steady state voltage that can be applied to the device in the "off" state is 30v DC. The maximum transient voltage must not exceed 40v. The maximum output current in an "on" state, i.e. output low, is 30ma per circuit. The maximum dissipation per driver is 30mw with 1v saturation drop across the output transistor. Determining the permissible total output current for the module is made complicated by the fact that some drivers may be off while others are on. The important consideration is that the maximum dissipation of 167mw must not be exceeded.

As an example, suppose it is necessary to drive a 24v, 50ma relay coil. Then, since each driver can only supply 30ma, two drivers in parallel are required, but this is marginal, so three would be better. When driving the three drivers in parallel, the device dissipation is:

$$3 \times 20 + 1 \times 50 = 110mw$$

The factors in the above expression are:

3 = number of drivers in parallel

20 = dissipation per driver in the module when turned on with zero output collector current

1 = saturated collector voltage drop across the output transistor

50 = load from the relay coil

If another driver was required to drive a separate 30ma load, the dissipation would be:

$$4 \times 20 + 1X (50 + 30) = 160mw$$

which would be all right. However, if a third separate load had to be driven, a separate module would have to be used, because

$$5 \times 20 + 1X (50 + 30 + 30) = 210mw$$

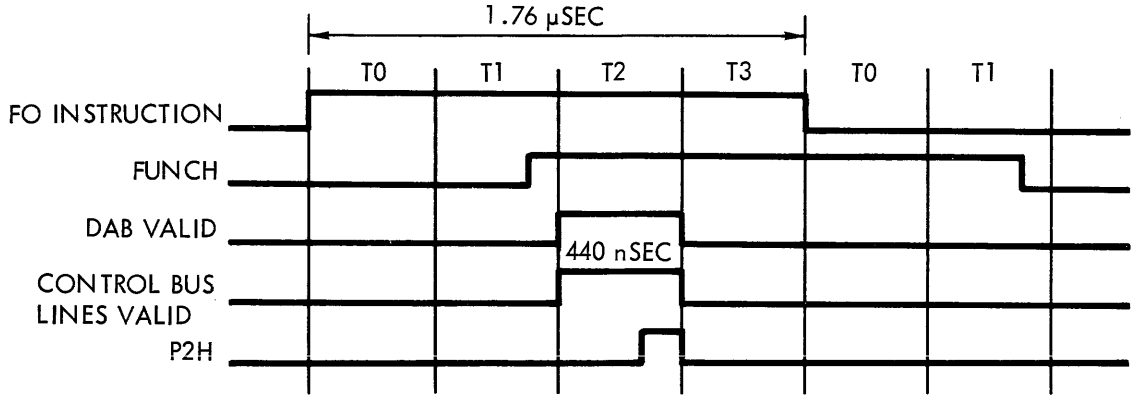
which exceeds the 167mw limitation. Note, though, that if only two of the three loads can be on simultaneously, then the one module could be used.

2.4 Theory of Operation:

In the discussion that follows, it will be assumed that the reader understands digital techniques. Thus, only highlights of the operation will be mentioned. Logic Block Diagram 17 47 002 should

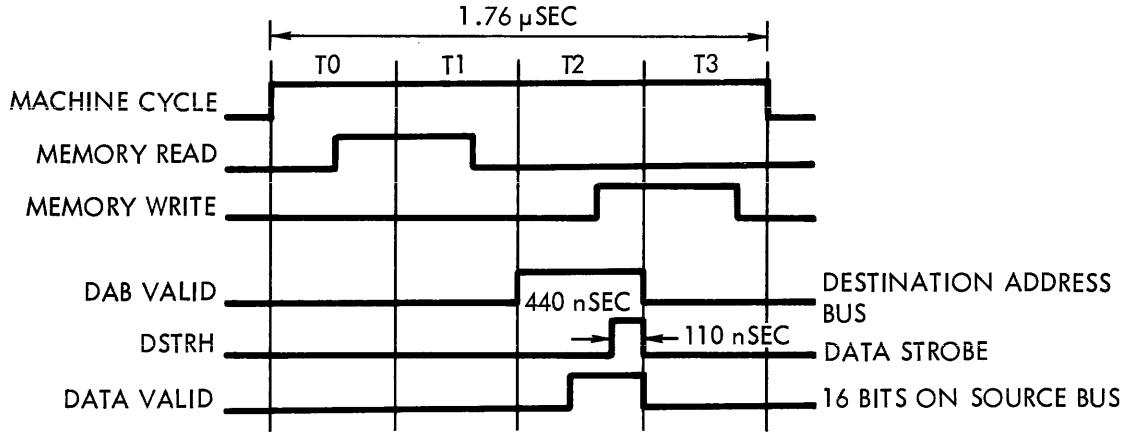
be referred to for troubleshooting or similar use. Recall from Section 2.3 (Programming) that the first line of code selects the group of discrete outputs to be sent to the external device. This selection is made by an FO instruction, which delivers four pulses to operators for setting or clearing flip flops. The block "SELECT DDA LOGIC" consists of 6 input gate, which decodes the destination address lines DABOH to DAB5H, so only this device responds when it is specified as a destination. Thus, when the BOM address (51) is selected as a destination, the block "GROUP SELECT LOGIC" is enabled, and depending on the combination of control bits, CBOH to CB3H selects either Group 1, Group 2, or both. The timing is shown in Figure 2-3.

The next line of code transfers the contents of either a hardware register or a memory location to the selected group. This is accomplished by decoding the source address lines in the block "SELECT SDA LOGIC". When the address on the source bus is valid, either or both of the "GROUP ENABLE" lines cause the information in the register to be transferred to the output buffer through the data lines of the source bus. Timing is shown in Figure 2-4.



BOM GROUP SELECTION

Figure 2-3



BOM TIMING

Figure 2-4

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REVISED PER ECO # 235	1/22/70	
		REVISED PER DWG # 283	3-27-70	
08-40 193	AA	7406'S WAS 8T90'S, ADDED R RESISTORS & ADDED LOCATION VIEW	GTB 10/4/71	

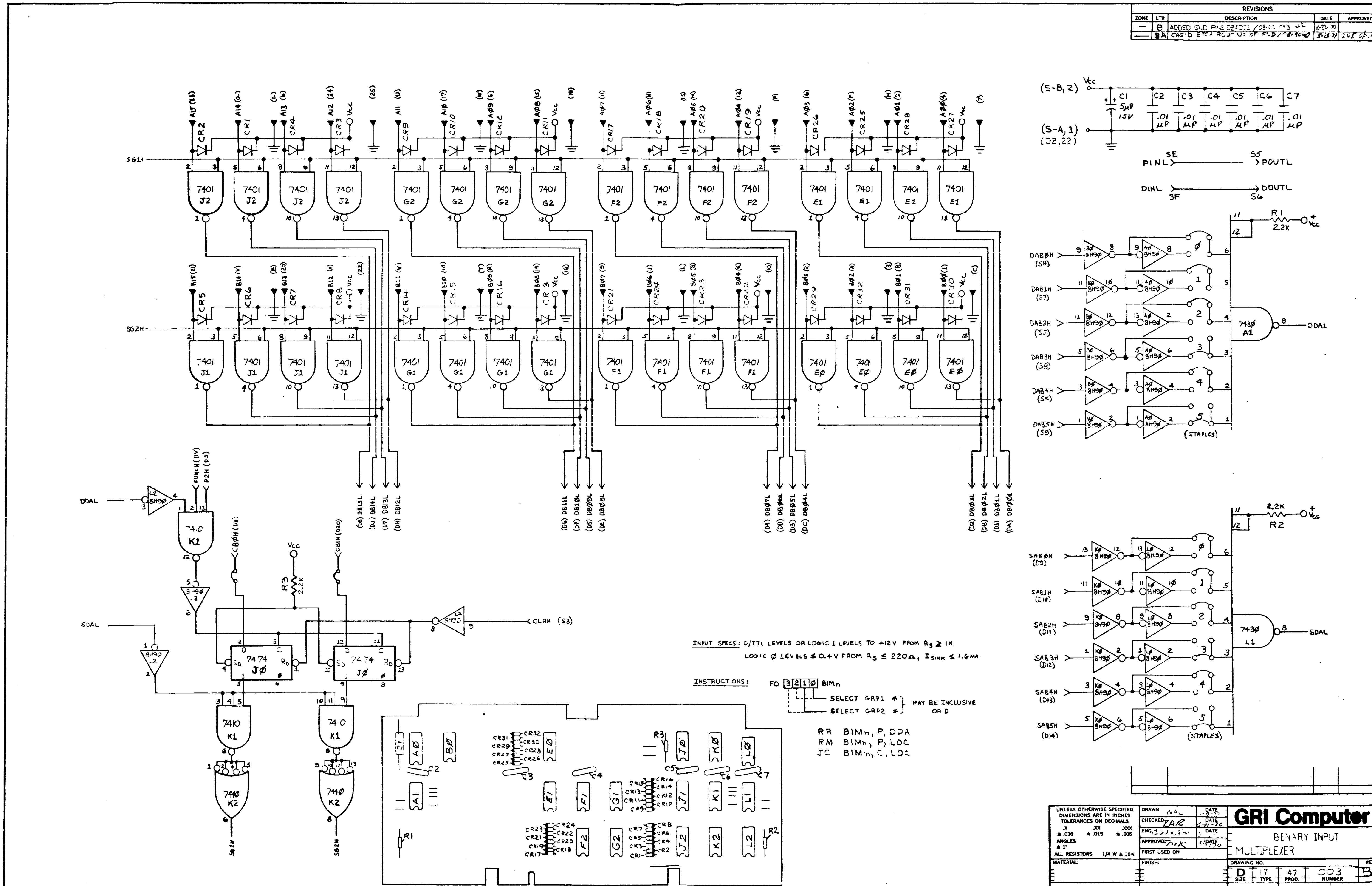
PART-1-8H90
PART-2-7406

PART-1-8H90
PART-2-7406

NOTES
1. INDICATES PROCESSOR I/O BUS CONNECTION
2. INDICATES INTERFACE CABLE CONNECTION
3. *PART-1 BOM - 8H90'S
PART-2 BORD-7406 WITH PULL-UPS R2,3,4

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .X ± .030 .XX ± .015 .XXX ± .005 ANGLES ± 1° ALL RESISTORS 1/4 W ± 10%	DRAWN	DATE	GRI Computer
	CHECKED	DATE	
	ENG. [illegible]	DATE 4-6-70	BINARY OUTPUT MULTIPLEXER
	APPROVED JAR	DATE 4/8/70	
	FIRST USED ON		
MATERIAL:	FINISH:		DRAWING NO. D 17 47 032 AA
REMOVE ALL SHARP EDGES			SIZE TYPE PROD NUMBER REV.
			SCALE: WEIGHT: SHEET

DIETZGEN Boston 1968 10296


REVISIONS
INPUT SPECS: D/TTL LEVELS OR LOGIC 1 LEVELS TO +12V FROM Rs ≥ 1K
LOGIC Ø LEVELS ≤ 0.4V FROM Rs ≤ 220Ω, ISINK ≤ 1.6MA.
INSTRUCTIONS:
FO 3 2 1 Ø BIMn
SELECT GRP1 *
SELECT GRP2 *
MAY BE INCLUSIVE OR D
RR BIMn, P, DDA
RM BIMn, P, LOC
JC BIMn, C, LOC
(STAPLES)
DDAL
SDAL
CLRH (S3)
PINL
POUTL
DINL
DOUTL
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS
.X ± .030
.XX ± .015
.XXX ± .005
ANGLES ± 1°
ALL RESISTORS 1/4 W ± 10%
MATERIAL:
REMOVE ALL SHARP EDGES
DRAWN
CHECKED
ENG.
APPROVED
DATE
FIRST USED ON
FINISH:
GRI Computer
BINARY INPUT MULTIPLEXER
DRAWING NO.
D SIZE
17 TYPE
47 PROD.
003 NUMBER
REV. BA
SCALE:
WEIGHT:
SHEET 1 OF 1

GRI Computer Corporation

320 NEEDHAM STREET, NEWTON, MASSACHUSETTS 02164

TEL: (617) 969-0800