HEWLETT PACKARD

# HP 12821A
# ICD DISC INTERFACE DIAGNOSTIC
## reference manual

ABSOLUTE BINARY PROGRAM NO. 12821-16001
DATE CODE 1928

**HEWLETT-PACKARD COMPANY**
**Roseville Division**
**8000 Foothills Boulevard**
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# PRINTING HISTORY

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# LIST OF EFFECTIVE PAGES

The List of Effective Pages gives the most recent update number on which the technical material on any given page was altered. If a page is simply re-arranged due to a technical change on a previous page, it is not listed as a updated page. Within the manual, changes are marked with a vertical bar in the margin. When a update is incorporated in a reprinted manual, the update number and vertical bar in the margin is removed but the update number will remain on this List of Effective Pages page.

| Pages | Update No. | Pages | Update No. |
|---|---|---|---|
| 1-2 thru 1-3 | 1 | | |
| 3-3 | 1 | | |

Table of Contents

| INTRODUCTION | SECTION I |
|---|---|

## 1.1 GENERAL

The Hewlett-Packard 12821A ICD Disc Interface Diagnostic will test any combination of hardware from one 12821A Disc Interface Card (DI), with or without cabling, to two 12821A Disc Interface Cards (DIs) with a mandatory bus interconnection.

NOTE! The DI cannot be connected to the discs when running the diagnostic. The recommended bus address of the DI is switches S1 thru S7 "closed" and S8 "open", resulting in a bus address of 0 and the DI being the System Controller.

The diagnostic has the ability to run with or without a console, to delay one second between tests, to loop on individual tests (console mode only), or loop on the entire diagnostic.

## 1.2 REQUIRED HARDWARE

The following hardware is required to test the 12821A Disc Interface Card:

a. HP 1000 M/E/F-Series Computer with a minimum 8k words (16K bytes) of memory.

b. HP 12897B Dual Channel Port Controller (Direct Memory Access).

c. Console device (optional but highly recommended).

d. Absolute binary loading device (used to load the Diagnostic Configurator and the 12821A Disc Interface Diagnostic).

e. Any of the following hardware configurations:
   (1) One 12821A Disc Interface Card with or without cabling.
   (2) Two 12821A Disc Interface Cards connected directly by two HP-IB bus cables (HP 59310-60005 Bus Input/Output Cables).

f. Switch S8 of the DIP rocker switches on the Disc Interface Card must be "open" on any DI under test. This establishes the DI as the System Controller.

## 1.3 REQUIRED SOFTWARE

The following software is required to test the Disc Interface Card:

a. The Diagnostic Configurator is used for equipment configuration and as a console device driver.

| | | |
|---|---|---|
| Binary Object Tape | Part No. | 24296-60001 |
| Manual | Part No. | 02100-90157 |

b. HP 12821A Disc Interface Diagnostic.

| | | |
|---|---|---|
| Binary Object Tape | Part No. | 12821-16001 |
| Manual | Part No. | 12821-90002 |

The HP 12821A Disc Interface Installation and Reference Manual, part no. 12821-90006, is not required but highly recommended.

The Diagnostic Serial Number (DSN) for this diagnostic resides in memory location 126 octal. The DSN is 103024 octal.

## 1.4 DIAGNOSTIC TEST LIMITATIONS

The diagnostic will not test the following:

a. The ability of the DI to propagate or generate priority-low signal (PRL).

b. The ability of the DI to transmit data over the bus at a specific rate of one megabyte per second.

c. The DI under actual subsystem conditions involving complex protocols and handshaking.

d. The DI with software controlled handshakes (only DCPC controlled handshakes are used by the diagnostic).

e. The two most significant bits of the bus address assigned to the DI (switches S4 and S5 on the DI). The diagnostic uses only the three least significant bits of the bus address (switches S1, S2, and S3).

f. The ability of the DI to interpret commands received over the bus such as UNTALK, UNLISTEN, TALK, LISTEN, etc.

## 1.5 DIAGNOSTIC EXECUTION LIMITATIONS

a. Select code 77 octal is reserved for use by the diagnostic. A DI in this select code will not be recognized by the diagnostic.

b. In the console mode, a DI in select codes 70 to 76 octal will not be found automatically by the diagnostic. The select code must be input by the operator.

c. The priority chain in the backplane must not be broken to any DI under test.

d. Switches S1, S2, and S3 determine the bus address of the DI. The position of these switches must be known when running the diagnostic. S1 is the least significant bit (LSB), and a switch setting of "open" corresponds to a logic "1".

e. Switch S8 determines if the DI is the System Controller. If S8 is "open", the DI is the System Controller. All DIs to be tested by the diagnostic must be designated as the System Controller.

f. In the single test loop mode, the only failure indications will be in S-Register bits 0-5.

g. In the non-console mode, a failure during a data transfer will not indicate the "good" and "bad" data, only that a failure occurred.

h. In the non-console mode, Preset Test T10 will be skipped.

i. For the Bus Test T15, two DIs must be connected directly by two HP **59310-60005** Bus Input/Out Cables with all discs disconnected.

## 1.6 GLOSSARY OF TERMS

A glossary of terms is contained in Table 1-1.

Table 1-1. Glossary of Terms

| | |
|---|---|
| DI | 12821A Disc Interface Card |
| SC | Select Code |
| SR | S-Register |
| DSN | Diagnostic Serial Number |
| T0 | Test 0 |
| T2 | Test 2 |
| T1 | Test 1 |
| T3 | Test 3 |
| T4 | Test 4 |
| T5 | Test 5 |
| T6 | Test 6 |
| T7 | Test 7 |
| T8 | Test 8 |
| T9 | Test 9 |
| T10 | Test 10 |
| T11 | Test 11 |
| T12 | Test 12 |
| T13 | Test 13 |
| T14 | Test 14 |
| T15 | Test 15 |
| IEN | Interrupt Enable |
| PP | Parallel Poll |
| CLC SC | Clear Control Flip Flop on the specified select code. |
| STC SC | Set Control Flip Flop on the specified select code. |
| STF SC | Set Flag Flip Flop on the specified select code. |
| CLC SC,C | Clear Control Flip Flop, Clear Flag Flip Flop on the specified select code. |
| HALT XXB | Halt code displayed in the T-register of the computer. T-register contents are actually 1020XX octal. |
| FF | Flip Flop |
| FIFO | Hardware Buffer (First in, First out) |
| DI #1 | 12821A #1, DI in the lower select code |
| DI #2 | 12821A #2, DI in the higher select code |

| PROGRAM STRUCTURE | SECTION II |
|---|---|

## 2.1 PROGRAM ORGANIZATION

The diagnostic is separated into four main sections, the Configuration Section, 12821A #1 Main Test Section, 12821A #2 Main Test Section, and the Bus Test Section.

### Configuration Section

The configuration section allows the operator to enter the select code and bus address of the DI or DIs under test. The priority chain in the backplane up to the DI must not be broken. The bus address is determined by switches S1 to S3 located on the DI.

### 12821A #1 Main Test Section

This section performs tests T0 through T14 on the DI that was specified first in the Configuration Section (DI in the lower select code).

### 12821A #2 Main Test Section

This section is executed only if a second DI was specified in the Configuration Section. If a second DI was specified, the diagnostic will enter this section and perform tests T0 through T14 on the second DI (DI in the higher select code).

### Bus Test Section

This section is executed only if two DIs were specified in the Configuration Section. If both DIs pass tests T0 through T14, the diagnostic enters this section and performs Bus Test T15. This test verifies that the two DIs successfully communicate and parallel poll each other over the bus.

## 2.2 PROGRAM CONTROL

Control of the diagnostic program is dependent upon whether the diagnostic is being run with or without a console device.

### Console Mode

The console mode of operation is extremely friendly and all messages and questions displayed should be self explanatory. The initial heading output to the terminal will give a brief explanation of the interactive operator commands. A detailed description of the operator commands can be found in Section 3-1. The configuration is performed interactively on the console. The diagnostic operation is controlled via interactive operator commands on the console, and execution options which are specified by the S-Register settings. The S-Register settings for diagnostic execution are listed in Table 3-1. Error reporting is performed via error messages output on the console. The messages should be self explanatory, but Table 5-1 contains a listing of all possible test failures.

### Non-Console Mode

In the non-console mode, configuration is performed by inputting configuration data in the S-Register after specific halts as described in Section 3-2 and Table 3-3. Diagnostic execution is controlled by the S-Register execution options which are listed in Table 3-2. Error reporting is performed via HALT codes and S-Register bits as listed in Table 5-1.

A flow chart of the diagnostic operating procedure is provided in Figure 3-1. Refer to the Diagnostic Configurator Manual for the procedure to load the Diagnostic Configurator and the 12821A Disc Interface Diagnostic.

NOTE! a. The DI must not be connected to any discs during diagnostic execution.
b. Switch S8 on the DI must be "open" to run the diagnostic (the DI must be the System Controller).
c. The bus address, determined by switches S1, S2, and S3. must be known to run the diagnostic.
d. If the DI is in a 12979A/B I/O Extender, which is being used in a dual CPU configuration, the I/O Extender must be locked to the port that the diagnostic is operating from.

## 3.1 CONSOLE MODE DIAGNOSTIC EXECUTION

If a console was specified during configuration of the Diagnostic Configurator, the diagnostic will automatically execute in the console mode. After loading the diagnostic, pressing PRESET, RUN will start the diagnostic. The console will output an opening message identifying this diagnostic and giving some guidelines for operation. If S-Register bit 13 is off, the diagnostic will list the console input options, automatically enter the Configuration Section, and output the first configuration question on the console.

### Configuration Section

The Configuration Section of the diagnostic will allow the operator to enter the select codes and bus addresses of the DIs under test. The configuration is interactive, and all messages and questions output to the console should be self explanatory.

The diagnostic checks the I/O backplane to find the select codes of the DIs. The diagnostic will find the DIs that have the lowest select codes. If, for example, the system has three DIs in select codes 12, 14, and 16 octal. The diagnostic will find the DIs in select codes 12 and 14. To test the DIs in select codes 14 and 16, the operator must input the select codes of the test DIs. The diagnostic will still find the first two DIs, but when it finds the first DI, the operator will override the diagnostic and input a select code of 14. When the diagnostic informs the operator that it found the second DI in select code 14, the operator will override it and input a select code of 16. The diagnostic will then execute on the DIs in select codes 14 and 16.

If DIs are located in select codes 70 to 76 octal, they will not be found by the diagnostic and their select code must be entered by the operator. The diagnostic requires the opertor to input the bus address of the DI under test. The bus address is determined by switches S1, S2, and S3 on the DI. Switch S1 is the least significant bit and an "open" setting corresponds to a logic one. Switches S4 to S7 are not applicable. The recommended switch settings are S1 to S7 all "closed" and S8 "open", which results in a bus address of zero and the DI being the System Controller.

## 12821A #1 Main Test Section

After the Configuration Section, the diagnostic enters the 12821A #1 Main Test Section. At this point the diagnostic is initialized for execution on DI #1 (lower select code), prompts the operator with a "?", and waits for a command. The operator commands are described in the following paragraphs. The diagnostic execution options are listed in Table 3-1. Test descriptions are listed in Section 4.

## 12821A #2 Main Test Section

If a second DI (higher select code) was specified during configuration, and DI #1 passed tests T0 through T14, the diagnostic is automatically initialized for DI #2 and executes tests T0 through T14 on DI #2. If DI #1 fails any of the tests T0 through T14, the diagnostic is left initialized for DI #1. To test DI #2, the F<cr> command must be used to force the diagnostic to be initialized for DI #2.

Bus Test Section

If two DIs were specified during configuration and the Main Test Section was completed successfully on both DIs, Bus Test T15 will be executed automatically. Test 15 is a check of the DI's ability to communicate over the bus. For Test 15, the DIs must be connected together by the bus cables (HP P/N 59310-60005) and the discs must not be connected to the bus. The two DIs alternately talk and listen over the bus. A test buffer is transferred, parallel polls are executed, and status is checked.

Console Mode Operator Commands

If a console device was specified during configuration of the Diagnostic Configurator, the diagnostic will automatically enter the console mode. Listed below are the valid operator commands.

NOTE! a. Execution of the commands <cr>, [n]<cr>, L[n]<cr>, E<cr>, and R<cr> begin immediately after the command is entered.

b. The commands F<cr> and G<cr> do not begin execution; they initialize the diagnostic for a particular DI and return with a "?" prompt. The operator can then input any of the commands listed under (a) above.

<cr>.....Carriage return, specifies default execution from Test 0 on DI #1 (card in the lower select code). If bit 14 of the S-Register is not set, the diagnostic will prompt operator intervention for Test 10, otherwise Test 10 will be skipped. If all tests complete successfully on DI #1, the message "TESTING COMPLETED ON S.C. XX" is output to the console. If a second DI was specified during configuration, the diagnostic will automatically initialize itself with the select code of the second DI and begin execution from Test 0 on the second DI. If all tests complete successfully on DI #2, the message "TESTING CONPLETED ON S.C. XX" is output to the console. If the diagnostic is configured for two DIs and both DIs have successfully completed tests T0 through T14, Bus Test T15 will automatically be executed. Upon successful completion of Test 15, the diagnostic will output a successful completion message to the console, initialize the diagnostic for the first DI (lower select code), prompt with a "?", and wait for the next input.

[n]<cr>....Begin execution from Test n (0 to 14) on the DI that the diagnostic is initialized for. If no faults are encountered, the diagnostic will progress automatically as described for the <cr> command. See the F<cr> and G<cr> commands for controlling which DI the diagnostic is initialized for. This command is useful for bypassing a failing test and execute the remaining tests on a particular DI.

L[n]<cr>...Loop on Test n, where n is a valid test number (0 through 14 if only one DI is installed, and 0 through 15 if two DIs are installed and connected by a bus), on the DI that the diagnostic is initialized for. The default value for n is 0. If n is omitted, the diagnostic will loop on Test 0. See F<cr> and G<cr> commands for controlling which DI is initialized for diagnostic execution. As an example, if the diagnostic is initialized for DI #1, L3 will cause Test 3 to loop on DI #1. To break out of the loop, toggle bit 15 of the S-Register ON and then OFF. The diagnostic will respond with a "?" prompt. If looping on Test 10, bit 15 may have to remain ON for nearly 10 seconds for the diagnostic to recognize it. During a test loop, the only error indications will be in S-Register bits 0-5

G<cr>.....Initialize the diagnostic for DI #1 (DI in the lower select code). The diagnostic is re-initialized using the select code of DI #1, but execution is not begun. The diagnostic will prompt with a "?" and wait for an execution command.

F<cr>.....Initialize the diagnostic for DI #2 (DI in the higher select code). The diagnostic is re-initialized using the select code of DI #2, but execution is not begun. The diagnostic will prompt with a "?" and wait for an execution command.

R<cr>.....Reconfigure the diagnostic. Identical to starting the diagnostic at P = 100B. The diagnostic will output all opening messages and enter the configuration section.

E<cr>.....Exit the diagnostic. This command causes an orderly termination of the diagnostic with a HALT 77 octal. Pressing PRESET, RUN after the halt will re-enter the program in an orderly manner and the operator will be issued a "?" prompt. If a reconfiguration is desired, re-enter at P = 100 octal, or input the R<cr> command.

?<cr>.....This command will result in a listing of the operator commands and a brief description of their function. The diagnostic will then prompt with a "?" and wait for a command.

## 3.2 NON-CONSOLE MODE DIAGNOSTIC EXECUTION

If a console was not specified during the configuration of the Diagnostic Configurator, the diagnostic will automatically execute in the non-console mode. After entering the DSN of the diagnostic, the configurator loads in the diagnostic program and terminates with a HALT 77B. Pressing PRESET, RUN starts the diagnostic.

### Configuration Section

The diagnostic halts the computer with specific halts, after which the operator must input the select code or bus address of the DI. The following are the configuration halts. Refer to flowchart Figure 3-1 and configuration Table 3-3.

HALT 1B...Occurs after pressing PRESET, RUN to start the diagnostic. Input the select code of DI #1 (lowest select code, highest priority) in S-Register bits 0-5. S-Register bits 6-15 are not applicable.
Press PRESET, RUN.

HALT 2B...Input the bus address (determined by DIP rocker switches S1 to S3 on the DI, "open" corresponds to a logic 1 and S1 is the least significant bit of the bus address) of DI #1 in S-Register bits 0-2. S-Register bits 3-15 are not applicable. Switch S8 must be "open" to run the diagnostic.
Press PRESET, RUN.

HALT 3B...If a second DI is installed, input the select code of DI #2 (higher select code, lower priority) in S-Register bits 0-5. If no second DI is installed, input a "0" in S-Register bits 0-5. S-Register bits 6-15 are not applicable.
Press PRESET, RUN.

HALT 4B...This halt will occur only if a non-zero number was input as the select code of the second DI after HALT 3B. If this HALT occurs, input the bus address (switches S1 to S3) of the second DI in R-Register bits 0-2. S-Register bits 3-15 are not applicable. Switch S8 on the second card must also be set to "open" to run the diagnostic. Press PRESET, RUN.

HALT 5B...Select the desired diagnostic execution option from Table 3-2. and input the corresponding bits in S-Register bits 12-15. S-Register bits 0-11 are not applicable for diagnostic execution options, they are used to report the failing test and subtest number (see table 5-1).
Press PRESET, RUN.

## 12821A #1 Main Test Section

The Main Test Section is automatically entered when PRESET, RUN is pressed following a HALT 5B. The diagnostic will automatically execute tests T0 through T14 (except for test T10) on DI #1. If all tests pass, the computer will halt with a HALT 77B. If the DI does not pass a particular test, the computer will halt with a HALT 7B. S-Register bits 0-11 will specify the failing test and subtest. Failure descriptions are listed in Table 5-1. Pressing RUN after HALT 77B or HALT 7B will result in a HALT 5B. The diagnostic is then initialized for DI #1. The operator can run the diagnostic again, selecting whatever diagnostic options he wishes from Table 3-2. In the non-console mode it is not possible to bypass failing tests. To reconfigure the diagnostic, enter the diagnostic at P = 100B. Test descriptions are listed in Section 4.

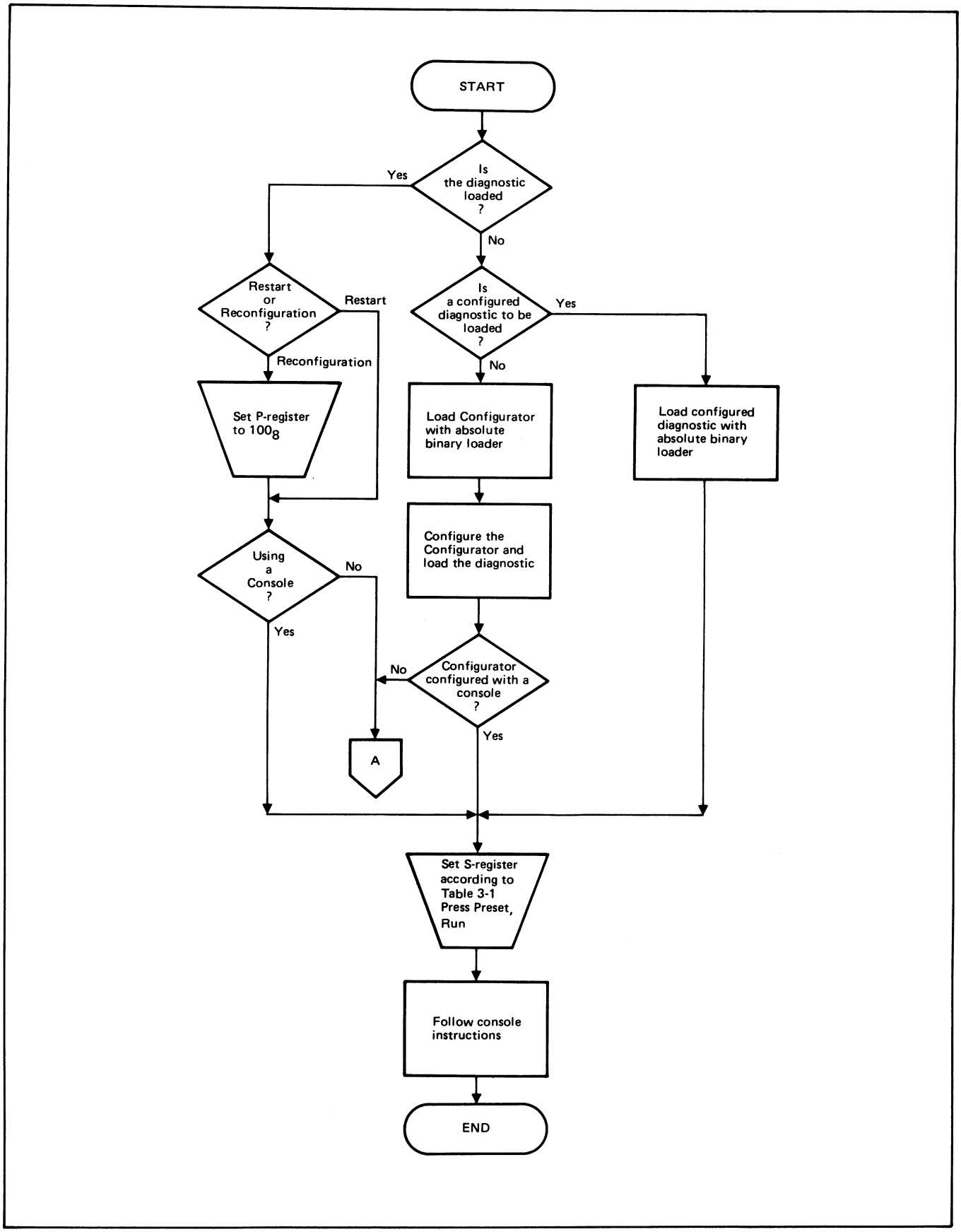
## 12821A #2 Main Test Section

If two DIs were specified during configuration, and tests T0 through T14 (except for test T10) pass on the first DI, the diagnostic will automatically initialize itself for the second DI. Execution of tests T0 through T14 (except for test T10) will begin automatically on the second DI. In the non-console mode, if the first DI fails one of the tests, it is possible to force testing of the second DI (see note on next page). Failure reporting is performed through a HALT 7B, with S-Register bits 0-11 specifying the failing test and subtest as listed in Table 5-1.

Bus Test Section

If two DIs were specified during configuration, and both DIs pass tests T0 through T14 (except for test T10), the diagnostic will automatically execute Bus Test T15. Test 15 tests the DIs ability to communicate over the bus. After a successful completion of Test 15 the computer will halt with a HALT 77B. At this point, the diagnostic is initialized for the first DI and the operator can run the diagnostic again, changing the execution option if desired. The execution options are listed in Table 3-2.

NOTE! a. HALT 77B indicates successful completion of all tests.
b. HALT 7B indicates a failure, refer to Table 5-1.
c. Memory location 135B contains the select code of the interface currently under test.
d. After a HALT 7B occurs in the T-register, S-register bits 6-11 specify the failing test, and S-register bits 0-5 specify the failing subtest. Table 5-1 contains test failure information.
e. If there are two DIs and DI #1 fails, to test DI #2 enter the diagnostic at P = 100B and reconfigure the diagnostic with the select code of DI #2 input as the response to the HALT 1B. This will cause tests T0 through T14 to be executed on DI #2.




7700-434

Figure 3-1. Operating Procedure Flowchart (Sheet 1 of 2)

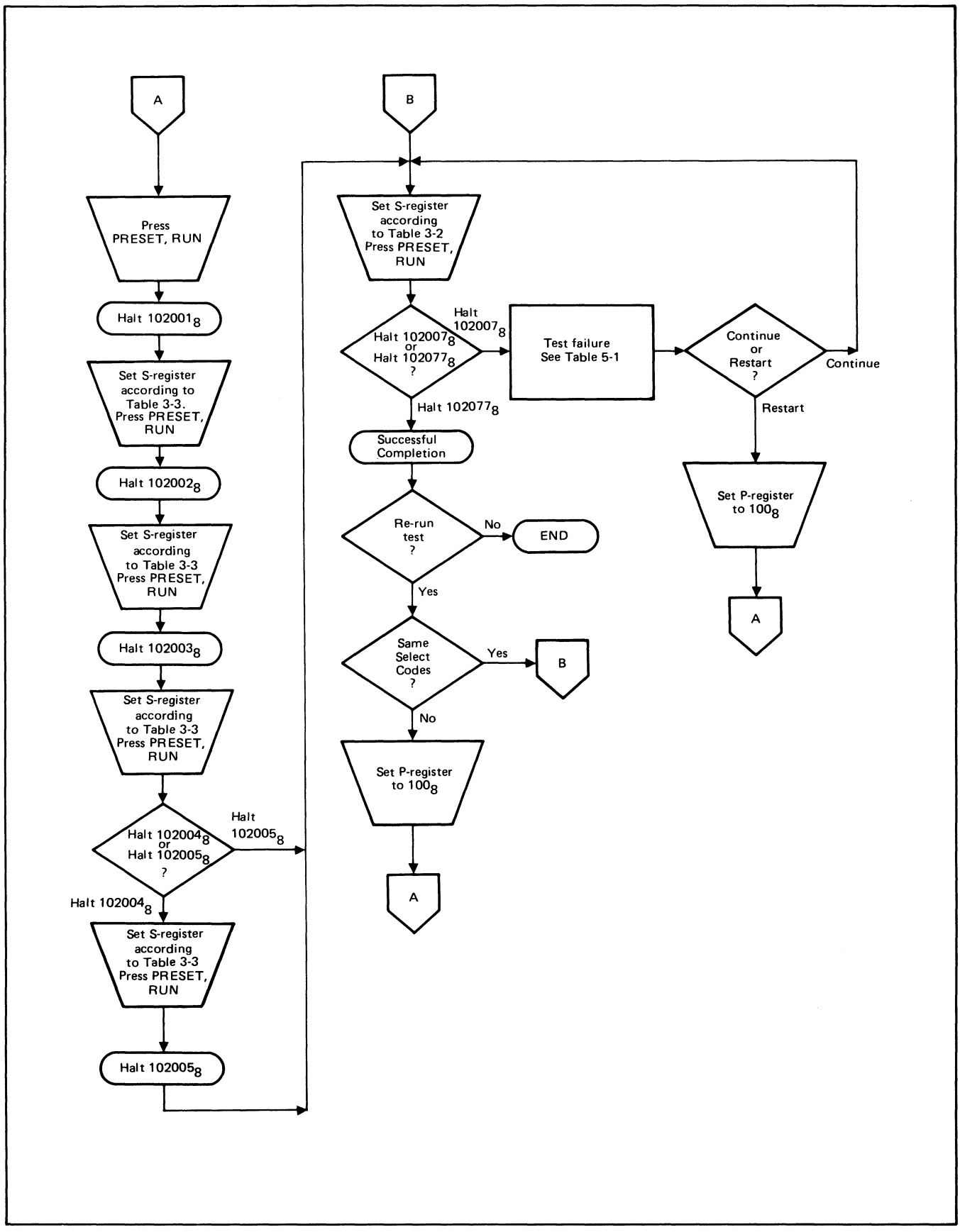



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Figure 3-1. Operating Procedure Flowchart (Sheet 2 of 2)

Table 3-1. Console Mode S-Register Execution Options

| SR bit | Execution Option |
|---|---|
| 15 | Set to logic 1 to loop on entire diagnostic.<br>-OR-<br>Toggle ON then OFF to break out of a looping test (see note (C) below). |
| 14 | Set to logic 1 to suppress operator intervention for Test 10 (i.e. Preset Test T10 is omitted). |
| 13 | Set to logic 1 to suppress non-error messages. |
| 12 | Set to logic 1 to provide 1 second delay between tests. |
| 11-0 | Not applicable. |

Table 3-2. Non-Console Mode S-Register Execution Options

| SR bit | Execution Option |
|---|---|
| 15 | Set to logic 1 to loop on entire diagnostic. |
| 14 | Not applicable. |
| 13 | Not applicable. |
| 12 | Set to logic 1 to provide 1 second delay between tests. |
| 11-0 | Not applicable. |

a. The above S-Register bits associated with the execution options are different than those used on most of the HP 1000 System diagnostics.
b. In the console mode, SR bit 15 has two functions. One is to force looping on the entire diagnostic and the other is to break out of looping on an individual test.
c. If looping on Test 10, it may be necessary to have SR bit 15 set ON for nearly 10 seconds before the diagnostic will recognize it. Be sure to toggle bit 15 OFF since if bit 15 remains on, looping on the entire diagnostic is enabled.

Table 3-3. Non-Console Mode Configuration Inputs

| Halt Code | S-Register Inputs | |
|---|---|---|
| 1B | SR bits 0-5 | Input the select code of DI #1 (DI in lower select code). |
| | SR bits 6-15 | Not applicable. |
| 2B | SR bits 0-2 | Input the bus address of DI #1 (switches S1 to S3 on the DI. The setting "open" corresponds to a logic "1" and S1 is the least significant bit). |
| | SR bits 3-15 | Not applicable. |
| 3B | SR bits 0-5 | Input the select code of DI #2 (DI in higher select code if installed). If there is no second DI, input a 0. |
| | SR bits 6-15 | Not applicable. |
| 4B | This halt code occurs only if a non-zero value was input in response to the HALT 3B. | |
| | SR bits 0-2 | Input the bus address of DI #2 (switches S1 to S3 on the DI). |
| | SR bits 3-15 | Not applicable. |
| 5B | SR bits 12-15 | Input the desired test execution option from Table 3-2. |
| | SR bits 0-11 | Not applicable. |

| TEST DESCRIPTIONS | SECTION IV |
|---|---|

The following describes each of the T0 through T15 tests performed by the disc interface diagnostic.

TEST 00 - Test 0 checks if CLC SC, C will clear the flag on the DI.

TEST 01 - Test 1 checks if STF SC will set the Flag FF on the DI.

TEST 02 - Test 2 checks if CLF SC will clear the Flag FF on the DI.

TEST 03 - Test 3 checks if the DI can successfully hold off interrupts with its Flag FF cleared.

TEST 04 - Test 4 checks to see if IEN low will successfully hold off interrupts.

TEST 05 - Test 5 checks if CLC SC, C to a select code other than the select code of the DI under test will accidently clear the Flag FF on the DI.

TEST 06 - Test 6 checks to see if the DI can successfully hold off interrupts with its Control FF cleared.

TEST 07 - Test 7 checks to see if the DI can successfully interrupt.

TEST 08 - Test 8 checks to see if data can be sent into the DI, through the FIFO buffer, and out of the DI.

TEST 09 - Test 9 checks to see if data can pass successfully around the CPU - FIFO buffer - CPU loop without loosing or picking up bits.

TEST 10 - Test 10 checks to see if "PRESET" will successfully clear the Control FF and set the Flag FF. This test is only executed in the console mode if switch S-register bit 14 is 0.

TEST 11 - Test 11 checks to see that an expected status word is returned from the DI after a known control word has been sent to it.

TEST 12 - Test 12 checks to see if the DI will perform a simple DMA output.

TEST 13 - Test 13 checks to see if the DI will perform a simple DMA input.

TEST 14 - Test 14 employs a special hardware diagnostic test mode to check the data path from the FIFO buffer to the bus tranceivers and back to the FIFO buffer.

TEST 15 - Test 15 uses two DIs (connected by a bus cable) to talk, listen, and parallel poll. A 36 word buffer (ASCII 0-9, A-Z) is transferred from a buffer through the two DIs over the bus and back into a test buffer using two-channel DMA. The transfer is attempted first in packed mode and then in unpacked mode.

# ERROR INFORMATION AND HALT CODES — SECTION V

Error information and halt codes are contained in Table 5-1. In the console mode, all error information and messages are output to the console and should be complete and self explanatory. In the non-console mode, the halts are the only means of communication with the operator and they must be interpreted using Table 5-1.

Table 5-1. Error Information and Halt Codes

| Halt Code (octal) | Meaning |
|---|---|
| 102001 | Input the SC of DI #1 in SR bits 0-5. Press PRESET, RUN |
| 102002 | Input the bus address of DI #1 in SR bits 0-2 (switches S1-S3 on DI) Press PRESET, RUN |
| 102003 | Input the SC of DI #2 in SR bits 0-5. If none input 0 in SR bits 0-5. Press PRESET, RUN |
| 102004 | Input the bus address of DI #2 in SR bits 0-2 (switches S1-S3 on DI) Press PRESET, RUN |
| 102005 | Input execution control option from Table 3-2. Press PRESET, RUN |
| 102077 | Successful completion. To re-test the same SC's, Press PRESET, RUN. Otherwise set P=100B and Press PRESET, RUN. |

CONTINUED

Table 5-1. Error Information and Halt Codes (continued)

| Halt Code (octal) | S-Register Bits 6-11 Test number in decimal | S-Register Bits 0-5 Sub-test number in decimal | Description of Failure |
|---|---|---|---|
| 102007 | 0 | 1 | T0 CLC SC, C did not clear Flag FF. |
| 102007 | 1 | 1 | T1 STF SC, C did not set Flag FF. |
| 102007 | 2 | 1 | T2 CLF SC did not clear Flag FF. |
| 102007 | 3 | 1 | T3 cleared Flag FF did not hold off interrupts. |
| 102007 | 4 | 1 | T4 IEN low did not hold off interrupts. |
| 102007 | 5 | 1 | T5 Instruction referencing a SC other than the DI's SC cleared the DI's Flag FF. |
| 102007 | 6 | 1 | T6 Control FF low did not hold off interrupt. |
| 102007 | 7 | 1 | T7 DI cannot interrupt. |
| 102007 | 7 | 2 | T7 DI interrupts through trap cell 0. |
| 102007 | 8 | 1 | T8 flag did not set when switched to listen mode with data in FIFO buffer. |
| 102007 | 8 | 2 | T8 FIFO buffer data error. |
| 102007 | 9 | 1 | T9 CPU-FIFO-CPU data path has a bit tied high. |

Table 5-1. Error Information and Halt Codes (continued)

| Halt Code (octal) | S-Register Bits 6-11 Test number in decimal | S-Register Bits 0-5 Sub-test number in decimal | Description of Failure |
|---|---|---|---|
| 102007 | 9 | 2 | T9 CPU-FIFO-CPU data path has a bit tied low. |
| 102007 | 9 | 3 | T9 CPU-FIFO-CPU data path has two bits tied together. |
| 102007 | 10 | 1 | T10 PRESET did not clear the FIFO buffer. |
| 102007 | 10 | 2 | T10 PRESET did not set the DI's Flag FF. |
| 102007 | 10 | 3 | T10 PRESET did not clear the FF. |
| 102007 | 11 | 1 | T11 for a known control word, the returned status was incorrect. |
| 102007 | 12 | 1 | T12 DMA output transfer failed, ending word count incorrect. |
| 102007 | 12 | 2 | T12 DMA output transfer failed, bad data. |
| 102007 | 13 | 1 | T13 DMA input transfer failed, ending word count incorrect. |
| 102007 | 13 | 2 | T13 DMA input transfer failed, bad data. |
| 102007 | 14 | 1 | T14 fault in transmit handshake logic. |

CONTINUED

Table 5-1. Error Information and Halt Codes (continued)

| Halt Code (octal) | S-Register Bits 6-11 Test number in decimal | S-Register Bits 0-5 Sub-test number in decimal | Description of Failure |
|---|---|---|---|
| 102007 | 14 | 2 | T14 fault in receive handshake logic. |
| 102007 | 14 | 3 | T14 transmit-bus-receive path has a bit tied high. |
| 102007 | 14 | 4 | T14 transmit-bus-receive path has a bit tied low. |
| 102007 | 14 | 5 | T14 transmit-bus-receive path has two bits tied together. |
| 102007 | 15 | 1 | T15 bad status returned from listener after talker sent IFC, REN. |
| 102007 | 15 | 2 | T15 listeners SRQ did not set talkers Flag FF. |
| 102007 | 15 | 3 | T15 timeout waiting for parallel poll response from listener. |
| 102007 | 15 | 4 | T15 incorrect parallel poll response. |
| 102007 | 15 | 5 | T15 timeout waiting for DMA to complete (HP-IB transfer). |
| 102007 | 15 | 6 | T15 data error (HP-IB transfer). |

Table 5-1. Error Information and Halt Codes (continued)

| Halt Code (octal) | S-Register Bits 6-11 Test number in decimal | S-Register Bits 0-5 Sub-test number in decimal | Description of Failure |
|---|---|---|---|
| 102007 | 15 | 7 | T15 timeout waiting for DMA to complete (HP-IB transfer, packed mode). |
| 102007 | 15 | 8 | T15 data error (HP-IB transfer, packed mode). |