



**HEWLETT  
PACKARD**

# Real-Time Emulator Intel® 80186/80188

**MODEL 64224S  
MODEL 64225S**

TECHNICAL DATA 1 JUN 1984

## Description

Models 64224S and 64225S Emulators provide real-time, transparent emulation for 80186 and 80188 microprocessor-systems. As an integrated subsystem of the HP 64000 Logic Development System, either model adds the power of emulation to all phases of 80186/80188 product design, development, and maintenance.

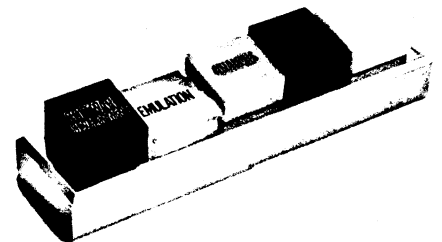
Model 64224S/64225S consists of an emulation control card, emulation pod, and operating system software. Connection to the target system is made with a 305 mm (12 in.) cable that terminates in a 68-contact leadless, chip-carrier probe. A typical 80186/80188 emulation system includes Model 64224S/64225S Emulation subsystem, Model 64156S Emulation Memory system, and Model 64302A Emulation Bus Analyzer. With this configuration, the HP 64000 system's extensive set of development aids can be readily applied to 80186/80188-based designs.

Directed syntax softkeys and an easy-to-use editor streamline software development and documentation. Logic State/Software Analysis and/or Logic Timing/Hardware Analysis can be combined with emulation for a variety of interactive, cross-triggered measurements. Model 64310A Software Performance Analyzer is effective in optimizing 80186/80188 programs, resulting in more efficient end products. With Model 64224S/64225S emulator and the many compatible HP 64000 analysis and development tools, you can produce a better 80186/80188-based product in less time, to gain a competitive edge.



## Features

- Real-time execution up to 8 MHz independent of emulator/target system memory assignment
- Instruction dequeuing in either normal or queue status operating mode
- Disassembly of 80186/8087 and 80188/8087 or 8089 instruction sets
- Nonintrusive, real-time tracing of all 80186/80188 cycles, including: Memory, DMA, I/O, Coprocessor
- Comprehensive display and modify functions for Internal registers, Peripheral Control registers, memory, and I/O ports
- Expanded measurement systems through interactive operation with other HP 64000 subsystems
  - Another 80186/80188 emulator or any other HP 64000 emulator
  - HP 64620S Logic State/Software Analyzer
  - HP 64600S Logic Timing/Hardware Analyzer
  - HP 64310A Software Performance Analyzer



## Getting Started

Even before target system hardware is ready, you can begin analyzing and debugging software as soon as the first code is written. The 8 MHz internal clock and emulation memory provide a base for exercising software with or without functional hardware. Real-time execution is fully maintained to assure correspondence between the emulated system and the final product.

Flexible mapping allows you to assign memory to the emulation system or target system in 256-byte blocks. Blocks are assigned as emulation ROM/RAM, target system ROM/RAM, or guarded, across the full address range of the 80186/80188 microprocessor. The 256-byte blocks are a convenient size for efficiently transferring newly developed resources from the emulator to the target system.

### Nonintrusive Analysis: A Must for Real-time Systems

Many designs based on the 80186/80188 processor are used to control or monitor real-time critical processes. Model 64224S/64225S emulator performs a wide variety of real-time measurements at full operating speeds, without intruding on 80186/80188 resources or execution. The emulator monitors all address, data, and status buses; you may display all bus cycles or a dequeued trace.

Information monitored by the emulator is passed to the HP 64302A Emulation Bus Analyzer where trigger and storage directives are applied. Triggers are defined for any event and set for the start, center, or end of the trace measurement. Storage qualifiers let you specify which kinds of events are captured and stored in analyzer memory. Commands are entered with softkeys, and trigger and store specifications may include address, data, status, ranges, don't-care bits, and occurrence counts.

As well as tracing the activity of the 80186/80188 system, the emulator/analyzer combination supports coprocessor functions. Instructions and memory cycles of the 8087 Numeric coprocessor or the 8089 I/O coprocessor may be traced and displayed in mnemonics. Figure 1 is an example of a real-time trace of processor activity.

### Controlling Your 80186/80188 System

Development and analysis tasks are simplified when the emulator provides complete control over the target system. HP 64224S/64225S emulator controls program execution with run-from, single-stepping, and run-until directives. You can display and modify any register, memory

```

Trace: execution data          break: none          count:
-----
line#  address  opc  data  i/o  data:hex  mnemonic  opcode or status  time, rel.
-----
-011   92400   2875         read mem. wd 8087          1.    uS
-010   92402   6BA1         read mem. wd 8087          1.    uS
-009   92404   20FF         read mem. wd 8087          1.    uS
-008   01294    25          AND AX, #000FFH          1.    uS
-006   01297    86          XCHG AH, AL              1.    uS
-004   01299   D08B         MOV DX, AX               1.    uS
-003   0129B    83          ADD DX, #000020H         1.    uS
-001   0129E    6D          INSB                      1.    uS
about  0FF20   FF20         read i/o wd              1.    uS
+001   02066   0000         write mem. wd            1.    uS
+002   0129F   C283         ADD DX, #00002H         1.    uS
+004   012A2    6D          INSB                      1.    uS
+005   0FF22   FF22         read i/o wd              1.    uS
+006   02068   80FF         write mem. wd            1.    uS
+007   012A3   C283         ADD DX, #00004H         1.    uS
+009   012A6   C783         ADD DI, #00002H         1.    uS

STATUS: 180186--Running          Trace complete          4:35

trace about NEW.TASK  data 0XX20H  status read..io

-----
run  trace  step  display  modify  break  end  ---ETC---

```

**Figure 1.** The logic analysis capabilities of Model 64224S/64225S trace executed 80186/80188 instructions. In addition, all coprocessor instructions and memory cycles are identified to assist in debugging. Model 64224S/64225S traces are based on data collected nonintrusively and in real time.

```

180186 Registers :repetitively
-----
Next IP 0000  SP 201E  SI 2614  DI 5C38  BP 201E
CS FFFF  SS 0000  DS 0000  ES 0000  FL [oditsz a p c]
AX 0000  BX 0026  CX 0000  DX 0000  000000000000
Relocation register: RR 20FF
DMA 1: CNT1 73A7  DP1 0B748  SP1 0C96B  CTL1 0000 0000 0000 0000
DMA 0: CNT0 D56E  DP0 03EFF  SP0 07DFD  CTL0 0000 0000 0000 0000
Chip select: MPCS B778  NMCS EBF8  PACS FFB8  LMCS 3DF8  UMCS FFFB
Timer 2: MC2 A021  MA2 FFFF  CR2 BAE7
Timer 1: MC1 A03F  MA1 FFFF  CR1 FFFF
Timer 0: MC0 A03F  MA0 FFFF  CR0 FFFF
Interrupt Control: IN3 000F  IN2 000F  IN1 000F  IN0 000F
DMA0 000F  DMA0 000F  TC 000F  IST 0004  IRR 0001
ISR 0000  PM 0007  MSK 00FD  PSR 0000

STATUS: 180186--Running in monitor          Trace complete          4:42

modify register SP0 to SERIAL_BUFF

-----
run  trace  step  display  modify  break  end  ---ETC---

```

**Figure 2.** The comprehensive register display of Model 64224S/64225S shows all the 80186/80188 internal registers. Sets of pertinent Peripheral Control Registers can be selected by the operator to achieve the most appropriate display.

location, I/O port, or Peripheral Control register. These functions are especially valuable in initial design stages, as they allow you to thoroughly investigate the details of target system operation.

Register displays, as shown in figure 2, are comprehensive, yet easily understood. The operator can display all or a subset of the Peripheral Control registers.

Memory displays show you any location or range of locations. Select a display in bytes, words, and ASCII equivalents, or the memory locations translated into the processor mnemonics. Modifications are by bytes or words, either singly or by ranges.

### Advanced Analysis Power — from Micro to Macro Measurements

As your 80186/80188 system grows, it becomes more complex and sophisticated. You can add correspondingly more sophisticated HP 64000 measurement systems as they are needed to serve new levels of measurement applications. Analyzers are available for the whole spectrum of logic measurements — from a micro level for a bit-by-bit analysis to a total system performance analysis for the macro view.

As the target system hardware evolves, Model 64600S Logic Timing/Hardware Analyzer may be added to check timing relationships at speeds up to 400 MHz. Postprocessing capabilities capture and hold timing measurements to store timing traces, compare measurements, mark significant signal combinations, and compute means and variances of specified intervals. HP 64600S hardware analyzer lets you take a close look at the detail of the operating system.

At the next level of measurements, Model 64620S Logic State/Software Analyzer has the functions to support intricate analysis modes: up to 120 input channels, 15 levels of sequential triggering, broad definitions for storage qualifiers, and measurement window specifications. The HP 64620S analyzer can be connected to the emulation subsystem through the HP 64304A Emulation Bus Preprocessor, to enhance or replace the HP 64302A emulation bus analyzer.

When programming in high-level languages, it is far more convenient to use the same language for analysis. With the HP 64620S software analyzer, you can generate a mixed display of high-level statements and the assembly level code associated with each statement (figure 3).

For optimizing and characterizing software performance, Model 64310A Software Performance Analyzer provides macro views of total system performance, by activity, interaction, or duration (figure 4). The performance analyzer becomes an integral part of the emulation system, so you can begin optimizing the program flow as soon as code exists. Module names are loaded into the HP 64310A performance analyzer automatically.

For multiprocessor applications, the HP 64224S/64225S emulator may be used interactively with any other HP 64000 system emulator with the Intermodule Bus (Model 64964A). The Intermodule Bus (IMB) also supports cross-triggering modes between analysis systems and emulators. The larger measurement system possible with the IMB is not restricted to analysis and emulation

subsystems in a single development station; HP 64303A IMB Extender board gives you access to measurement systems resident in other development stations.

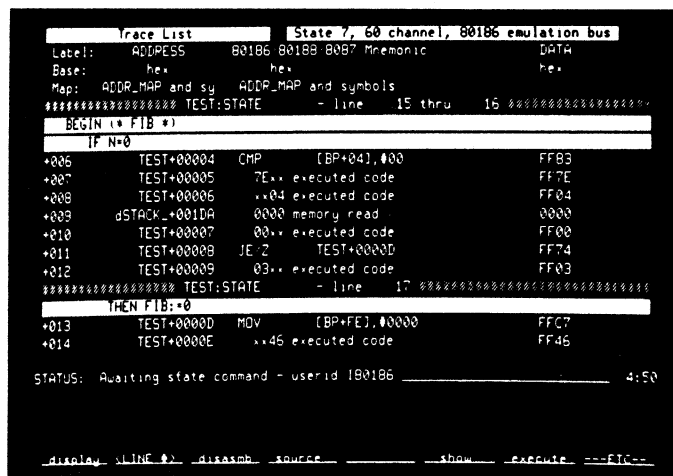


Figure 3. Model 64224S/64225S supports high-level language debugging by adding Model 64620S. One display mode of the HP 64620S traces high-level statements together with the assembly-level microprocessor instructions. Traces are based on system activity monitored nonintrusively in real time.

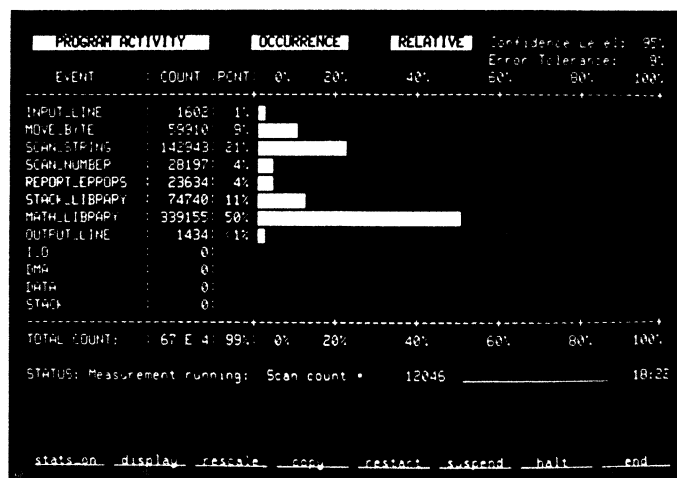


Figure 4. Total system performance can be monitored by adding Model 64310A Software Performance Analyzer to Model 64224S/64225S. A wide range of activity and duration measurements are available for a macro view of 80186/80188 system interactions, identifying where optimization efforts will yield the greatest performance improvement.

## Making a Difference

As an 80186/80188 hardware or software designer, the HP 64000 system design aids and development tools make you more efficient. You can focus your skills on the design and troubleshooting tasks because many of the time-consuming, repetitive chores inherent in creating new products are executed automatically by the HP 64000 system.

## Specifications

**Processor compatibility:** compatible with Intel 80186/80188 and any other microprocessors that comply with the specifications of either one of these processors.

**Note:** To properly connect and operate either emulator, the target 80186/80188 system must have an AMP® 55162-X socket and AMP® 55478-2 lid, an IDT 3M® Textool 68-pin JEDEC socket (part no. 268-5400-52), or equivalent socket assembly.

® Registered, AMP, Incorporated

® Registered, Minnesota Mining and Manufacturing Company

## Ordering Information

**Model 64224S 80186 Emulation Subsystem**

**Model 64225S 80188 Emulation Subsystem**

**Model 64156S Emulation Memory System** with memory control board and 32k-byte memory board

**Model 64156S Option 011:** expand to 64k-byte

**Model 64156S Option 012:** expand to 128k-byte

**Model 64156S Option 013:** expand to 256k-byte

**Model 64156S Option 014:** expand to 512k-byte

**Model 64156S Option 015:** expand to 1024k-byte

**Model 64302A 48-channel Emulation Bus Analyzer**

**Model 64853A 8086/88/186/188 Assembler/Linker**

**Model 64814A 8086/88/186/188 Pascal Compiler**

**Model 64818A 8086/88/186/188 C Compiler**

## COMPONENTS

**Model 64223A 80186/80188 Emulation Control Board**

**Model 64224A 80186 Emulation Pod** (includes software)

**Model 64225A 80188 Emulation Pod** (includes software)

## ELECTRICAL

**Maximum clock speeds:** 8 MHz (CLKOUT) with no wait states required for emulation or target system memory; 16 MHz max crystal frequency.

**Data inputs:** one LS TTL load plus approx 40 pF capacitance.

**Power:** 25 mA drawn from target system; all other power supplied by development station.

## PHYSICAL

**Cable length:** development station to emulation pod, approx 1.5 m (5 ft); emulation pod to target system interface, approx 305 mm (1 ft).

## ENVIRONMENTAL

**Temperature:** operating, 0° to +40° C (+32° to +104° F); nonoperating, -40° to +75° C (-40° to +167° F).

**Altitude:** operating, 4600 m (15 000 ft); nonoperating, 15 300 m (50 000 ft).

**Relative humidity:** 5% to 80%.

## ACCESSORIES SUPPLIED

Model 64224S 80186 Emulator and Model 64225S Emulator each include an emulation control board (Model 64223A) and an emulation pod (Model 64224A 80186 pod and Model 64225A 80188 pod); appropriate cables for connections from the board to the pod and from the pod to the target system; operating software supplied on flexible disc; and operators manual.