HEWLETT PACKARD

High Speed Timing/State Analyzer

MODEL 64610S

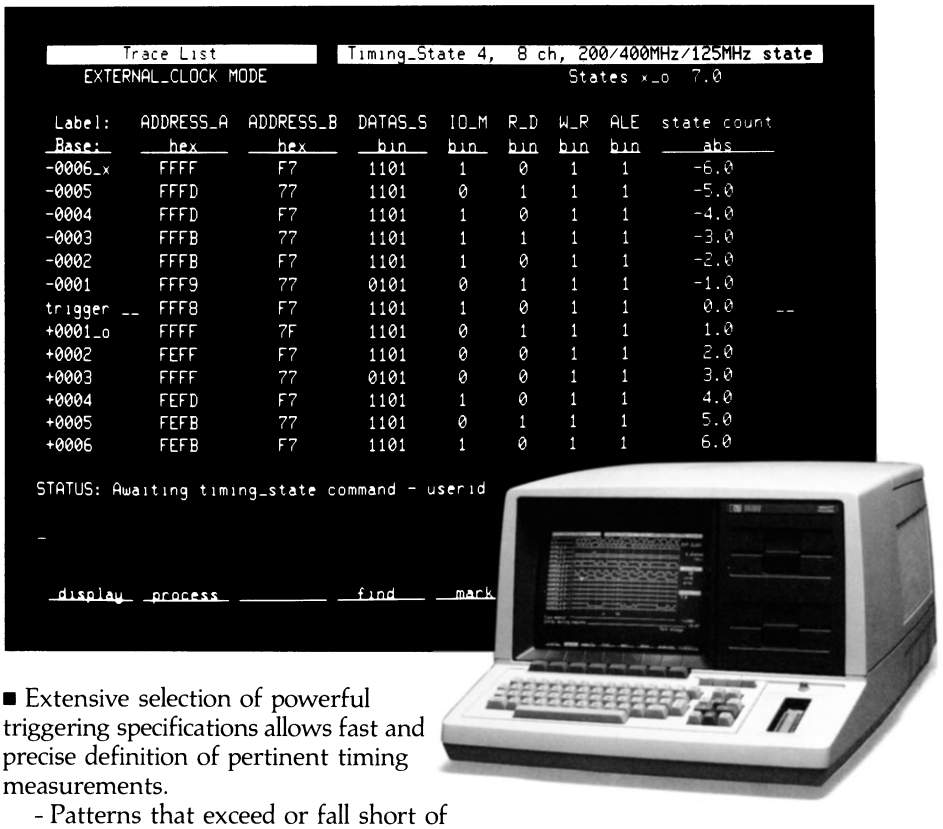
TECHNICAL DATA 1 OCT 84

Description

Model 64610S High Speed Timing/State Analyzer subsystem offers powerful high resolution, asynchronous and synchronous analysis with extensive postprocessing capabilities in the HP 64000 Logic Development System. The model 64610S, consisting of a control card (HP 64601B) and acquisition card (HP 64602A) with timing and clock probes, provides eight input channels expandable to 32 channels for timing or state analysis. Many triggering modes allow precise positioning of the display window to locate timing margin, state execution, and interaction problems. The analyzer's resources can be allocated to provide wide, fast, glitch, dual-threshold, and externally clocked measurements. Postprocessing adds another dimension to timing/state analysis with the ability to perform operations on acquired data, such as automated compare and statistical analysis of raw data.

Features

- Modular architecture allows optimum system configuration for each application environment.
- Asynchronous sampling from 2 Hz to 400 MHz for excellent resolution.
- Synchronous sampling to 125 MHz.
- 32 channel timing or state display and trigger capability.
- Compare level, range, and fault qualifications for state and timing listings.
- Memory depth of 4060 samples in wide sample mode and 8140 samples in fast sample mode for long, time measurement windows.
- Glitch capture and trigger for glitches as narrow as 3 ns to quickly locate problem-causing transients.
- Dual-threshold mode provides three-state analysis for checking transition times, loading problems, and noise margins.
- Low interchannel skew, less than 1.5 ns within an 8-channel pod and less than 3.0 ns between pods, minimizing errors in timing measurements.



- Extensive selection of powerful triggering specifications allows fast and precise definition of pertinent timing measurements.
  - Patterns that exceed or fall short of specified time duration
  - Transition into, or out of, specified states
  - Glitch
  - Boolean NOT condition
  - Intermediate signals between logic 1 and logic 0 voltages
  - Combined level and transition, or sequence triggering with the 16,24, or 32 channel analyzer options
  - Friendly user interface and symbolic triggering decrease learning time and increase convenience and simplicity of use
  - Powerful interactive analysis when multiple analyzer/emulation subsystems are installed, speeds integration of hardware and software
- Postprocessing of collected data for correlation and off-line analysis frees analyzer for use in other measurements
- Compensated probing with convenient connection alternatives for quicker set-up and reliable measurements.

Architecture

A model 64000 development station can be configured, with 8 to 32 channels of timing/state analysis if the necessary card slots are available. Depending on the measurement needs, and available card slots, additional timing/state analysis subsystems can be added to create multiple analysis systems in a single development station.

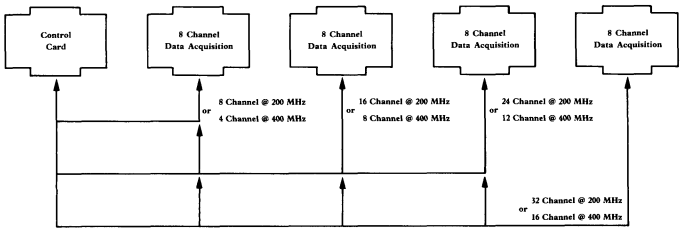


Figure 1. Timing Analysis subsystem combines a control card and a single data acquisition card for 8-channel input or a control card and two data acquisition cards for 16-channel input, three data acquisition cards for 24-channel input and four data acquisition cards for 32-channel input.

Measurement Modes

Measurements with the Timing Analyzer are made in four different modes: wide sample, fast sample, glitch capture, or dual threshold. Each mode offers a different view into the system under test. Selection of the desired mode is under software control and is made using the softkeys.

Wide Sample Mode (figure 2) is used to gather 4060 bits of data from each of eight inputs on each probe pod at sample rates from 2Hz to 200 MHz (0.5 s to 5 ns periods). Depending on the analyzer configuration, there can be one to four probe pods with the ability to monitor 8 to 32 test points. Measurement resolution is 6.5 ns including 1.5 ns of skew and memory depth is 4060 samples.

Fast Sample Mode (figure 3) increases the time resolution by using a 2.5 ns sample period (400 MHz). This increase in resolution is accomplished by allocating two samplers to each input with a 2.5 ns time separation between the samplers. Memory depth is increased to 8140 samples. The number of inputs to each probe that can be sampled is reduced by half. Measurement resolution between channels within a single pod (one clock period plus skew) is 4 ns.

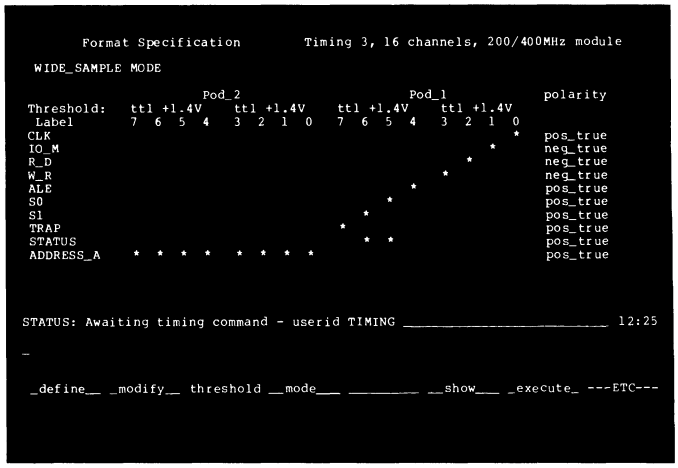


Figure 2. Wide Sample mode measurements are used for sampling rates from 2 Hz to 200 MHz.

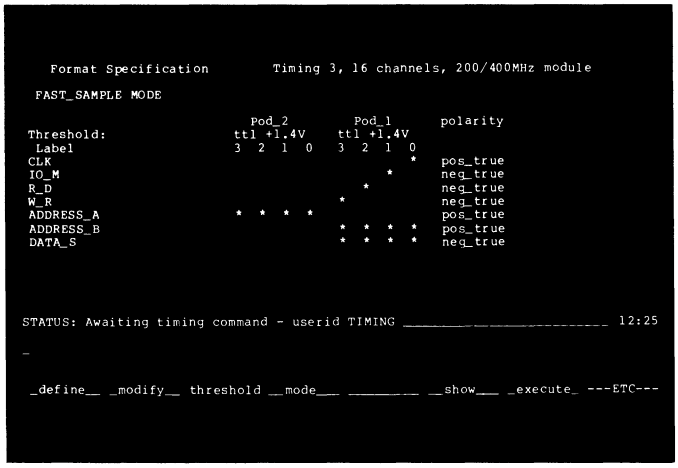


Figure 3. Fast Sample mode is used for sampling rates up to 400 MHz. Memory depth is 8140 samples.

Glitch Capture Mode (figure 4) captures and displays glitches as narrow as 3 ns on 4, 8, 12, or 16 channels, depending on the system configuration. The glitch capture mode monitors edges on incoming data while sampling data over a 2 Hz to 100 MHz range. When more than one edge occurs between two adjacent sample times, the event is recorded in a separate memory as a glitch. Since separate circuits and memory are used for detection and recording, glitches do not distort normal edge locations and glitches that are close to or on edges are captured and displayed separately.

Dual Threshold Mode (figure 5) offers more voltage resolution than is available with a basic timing analyzer measurement. This mode allows the specification of upper and lower thresholds for the signals being tested. Signals are displayed as the transition across the defined thresholds in three-level waveforms. By setting thresholds at a minimum acceptable high and maximum acceptable low, you can isolate marginal signal levels caused by excessive fan-out, defective components, weak pulldowns, etc.

In the dual threshold mode, marginal conditions are detected at sample rates from 2 Hz to 200 MHz. As with the preceding two modes, one-half of the available channels can be monitored because twice the information is stored in memory for each input channel.

Format Specification

Softkeys and symbolic triggering greatly simplify timing analysis by allowing the definition of measurement commands, specifications, displays, and recorded data in terms of signal names. Basic set-up is accomplished in the Format Specification where labels and names are assigned individual bits, input channels, or groups of channels. These assigned names are stored in a table and become part of the softkey command structure for building trace specifications.

The desired format display is called using softkeys (figures 2 through 5) which list the current data acquisition modes and the number of channels available. For example, the format specification in figure 3 is for a fast sample mode with a 16-channel system. Because system resources may be assigned as needed, the sampling rate is doubled to 400 MHz by halving the number of input channels. Therefore, the display shows eight channels, four for each of the two pods. Thresholds are defined on sets of four channels and displayed above the related channels. Logic polarity can be set for individual channels or labels. Labels, up to nine characters long, may be assigned to channels or group of channels (figure 5). In the Format Specification, labels may overlap: i.e., two or more labels may be assigned to the same input channel, allowing you to define labels for several different measurements.

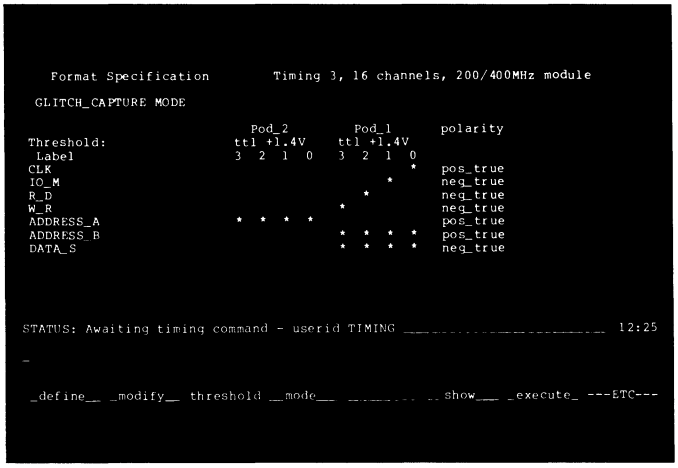


Figure 4. Glitches as narrow as 3 ns are detected and displayed with the Glitch Capture measurment mode.

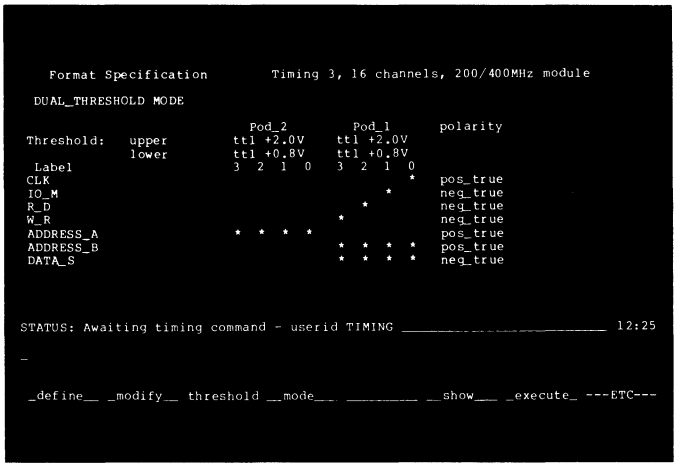


Figure 5. For Dual Threshold measurements, upper and lower thresholds are specified. This mode is valuable in analyzing tristating and rise and fall times.

Trace Specification

Sophisticated triggering allows you to take full advantage of the hardware analyzer's powerful measurement modes. These advanced triggering functions let you position the measurement window exactly where it is needed to solve difficult timing margin and system interaction problems. Complex measurements are set up easily using the softkeys with directed syntax.

There are five types of pattern triggering to qualify data capture in ways not possible with a simple occurrence trigger.

- Trigger upon entering a pattern
- Trigger upon leaving a pattern
- Trigger on greater than a specified duration of a pattern (including a middle level in the dual threshold mode)
- Trigger on less than a specified duration of a pattern (including a middle level in a dual threshold mode)
- Trigger on combinations of patterns and glitches.

Pattern Triggering is used in all measurement modes; an example trace specification of a wide sample mode is shown in figure 6. A trigger pattern (which may be entered in binary, octal, decimal or hexadecimal) is specified for the selected label and the occurrence of that pattern triggers the analyzer to collect a trace. The pattern may also include "don't care" entries where information on that line is captured in relation to selected points on other input lines. The Boolean NOT condition of a pattern may also be used as a trigger.

Transition Triggering sets a trigger on the condition of a set of signals (or single signal) "entering" or "leaving" a defined pattern (figure 7).

Time Interval Triggering (figure 8) can be used in two ways: a trigger can be specified for a pattern that persists too long or a pattern that does not persist long enough to meet a specification.

Glitch Triggering on one or more channels can be specified as trigger points. The occurrence of a glitch may be ANDed with a pattern, transition, or time duration specification to allow isolation of a glitch in proximity to a critical operation.

Additional cross-pod triggering in a 16, 24, or 32 channel subsystem allows conditional OR triggering, conditional duration triggering(except in external clock mode), or sequential triggering.

For example, it is possible to trigger on a pattern detected on one probe pod with its associated time duration specification followed by the pattern and a second time specification on the second probe. Another example is to set the first pod in a level-trigger mode (pattern plus duration), and the second pod in a transition-trigger mode where the trigger occurs when both conditions are met.

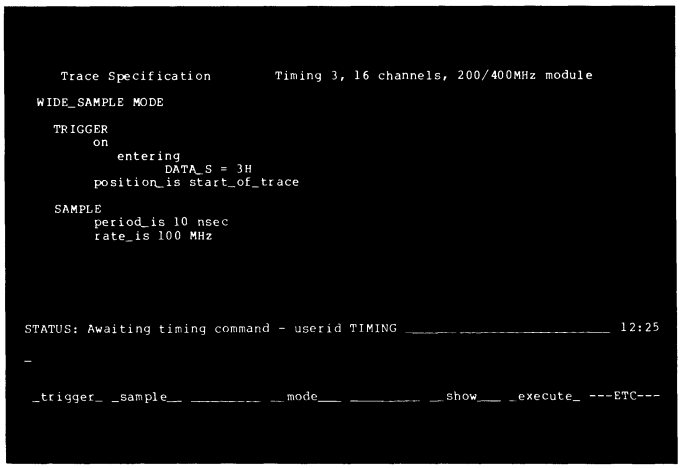


Figure 6. Pattern triggers may be defined in binary, octal, decimal, or hexadecimal, and assigned to input lines or to a label.

Figure 7. Trigger conditions may be set for one or more signals entering or leaving a defined state in transition triggering.

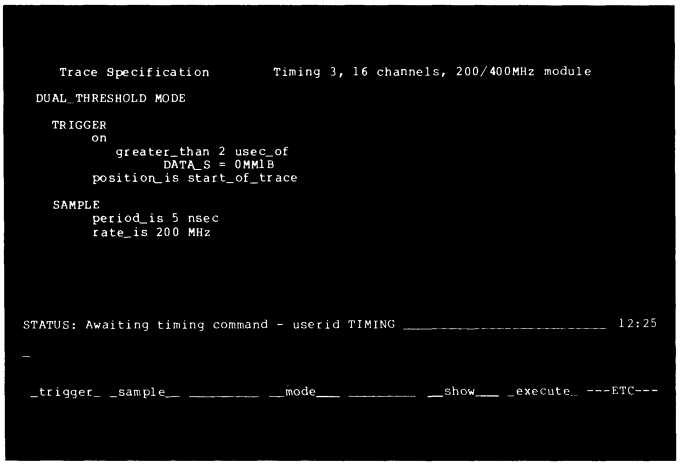


Figure 8. Time Interval trigger may be specified for a defined pattern that persists too long, or too short a time to meet specification.

Measurement data can be displayed in the form of either a timing diagram or a trace list. The timing diagram display can present up to sixteen channels of measurement data at a time while 32 channels of data can be present. The other 16 channels can be displayed by scrolling the display up or down. Channel ordering and spacing can be set by entering labels or default channel numbers. By selecting appropriate labels, data can be presented in a form that gives a clear display of what has been measured (figure 9).

Magnification, time cursors, and memory indicators are important features for study of the timing diagram. Magnification along the time axis allows the fine detail of a portion of the timing diagram to be expanded. Expansion ranges are X1, X2, X4, X10, X20, X40, and X100. An intensified region that can be positioned over areas of interest defines the expansion window for the next higher magnification factor.

Multiple time cursors (x, o in figures 9 and 10) are available to measure durations of events or intervals between events. Graticules and time-per-division information provide another reference to the amount of time being displayed.

For easy identification, glitches are displayed as dashed vertical lines (figure 9). Note that glitches are also displayed when they occur on transitions. Measurements in the dual threshold mode are displayed as three-level waveforms where the midlevel is for the sample periods during which the signal level is between the defined maximum and minimum threshold levels (figure 10).

Captured timing information can be displayed in trace list form (figure 11). You can scroll through the 4060 word memory, or by using the "find" softkey, go directly to areas of interest. When the Glitch Capture mode is used, the state listing indicates where a glitch occured with a "g" adjacent to the line. An "m" in the state listing defines the middle threshold condition when using the dual threshold mode. The x and o indicate where the time measurement markers are positioned.

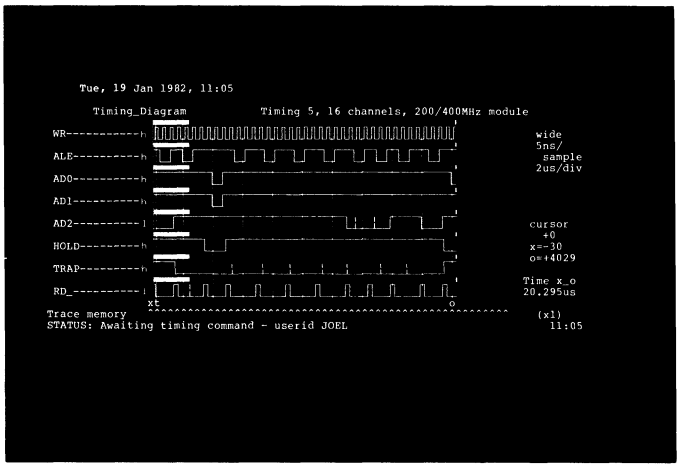


Figure 9. Displayed channels are arranged in order of interest for easy interpretation with glitches clearly displayed as dashed vertical lines.

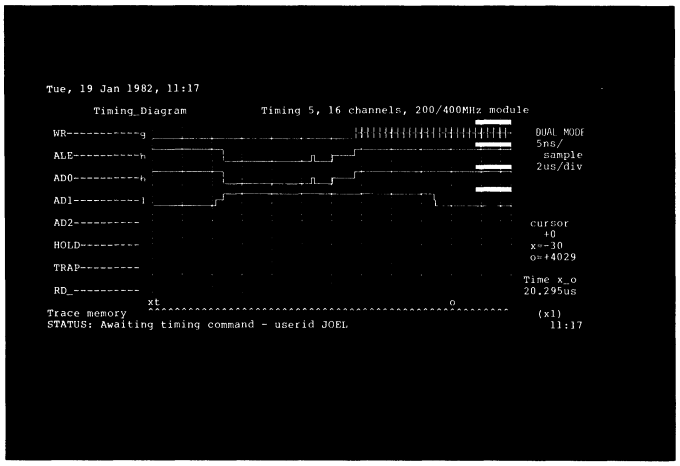


Figure 10. Three-level display in the Dual Threshold mode adds the capability for analyzing problems such as contention, loading, and transition time.

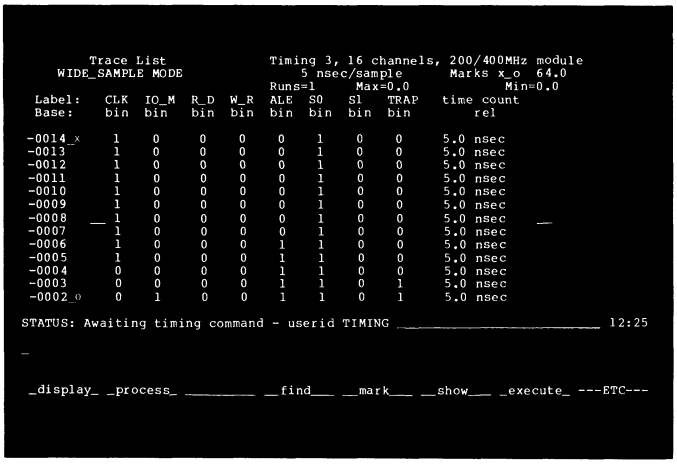


Figure 11. The x and o on the word listing of a timing trace indicate the start and stop points, respectively, for time measurement markers.

Interactive Measurements

Simultaneous, interactive timing and state measurements are powerful techniques for logic analysis in a microprocessor system. These measurements are made with an HP 64000 station configured with both a Timing/State Analyzer (Model 64610S) and Logic State/Software Analyzer (Model 64620S) connected by an Intermodule Bus (IMB). Either subsystem can enable or trigger the other subsystem in several functional combinations:

- State triggers state and timing.
- Timing triggers state and timing.
- State enables timing, timing triggers both.
- Timing enables state, state enables timing.
- State triggers state, state enables timing.
- Timing triggers timing, timing enables state.
- Feedback-restart loops, where state trigger enables state trace and simultaneously enables timing:
  Timing then:
  finds timing trigger and runs.
  State then:
  finds another condition, causing either
  (1) timing to retain data, or,
  (2) timing to reset and rerun, initiating a new trigger search.

Figure 12 is an example of enabling the timing analyzer by another subsystem in the station; i.e., "enable received" is the first condition for the trigger specification.

The IMB is not restricted to software analyzer/timing analyzer interfaces. It can be used to connect two or more timing analyzers, or two or more software analyzers, or analyzer and emulator analyzer subsystems. The emulator/analyzer combination is of particular value for developing multiprocessor-based systems.

One line of the IMB is a delay clock that can be used to define triggering and arming conditions in combination with delays. The display in figure 13 shows an "enable received" from another module; the timing module drives the trigger line 40 delay clocks after the specified trigger is satisfied.

Other forms of interactive measurements with external instruments are driven by the timing analyzer through a BNC connector on the rear panel of an HP 64000 station. Commonly, this mode can be used to trigger an oscilloscope, trigger a serial data analyzer, or provide a stimulus to user system hardware.

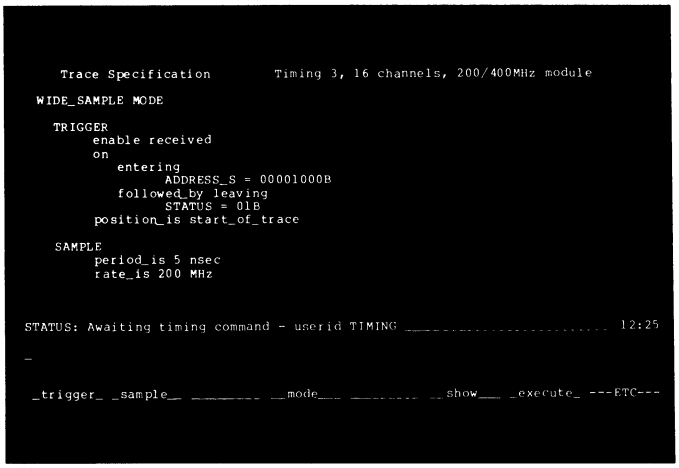


Figure 12. The statement "enable received" shows that this trace is to be initiated after receiving a signal from the Intermodule Bus (IMB).

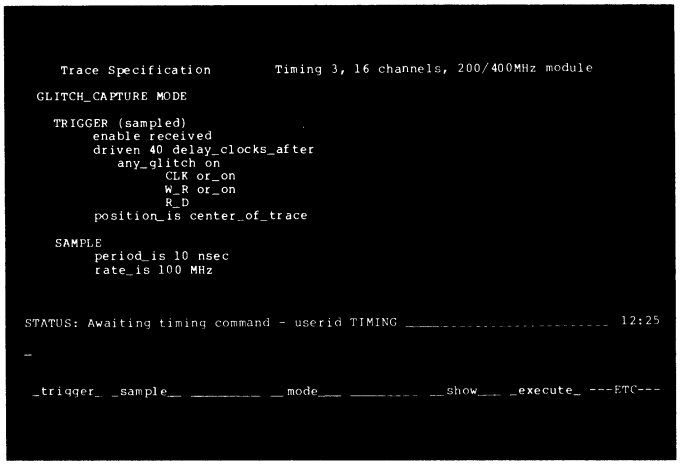


Figure 13. After a signal from another subsystem in the station is received via IMB, delay is added to the trace specifications of the Timing Analyzer.

Postprocessing

An extensive software package offers sophisticated, on-board, postprocessing capabilities of timing information. Postprocessing offers detailed analytical manipulation and statistical analysis of captured data without using external computers. There are seven major postprocessing functions:
- Storing and retrieving measurements
- Finding specific timing conditions
- Marking timing events
- Statistics on marked timing events
- Extended triggering conditions
- Processing asynchronous input as state listings
- Comparing stored and current measurements

Storing and Retrieving Measurements

Measurement results can be stored on disc and recalled for display and analysis at a later, more convenient time. Recalled data can be operated on as though it were just acquired, which allows sequential measurements to be acquired and detailed analysis accomplished with the analyzer off-line of the target system. The ability to store measurements on flexible disc means that analysis can be accomplished on other HP 64000 stations that did not initially acquire the data. An example of a recalled measurement displayed in trace list form is in figure 14.

Finding Specified Timing/State Conditions

Timing analyzers store data asynchronously without storage qualification, which means that a deep memory is important. With a memory depth of 4k bits, or 8k bits in fast sample mode, searching for a particular bit pattern 32-lines wide is not a trivial task. The postprocessing capability will automatically locate a particular machine state, each time that state occurred. The analyzer can also be directed to collect the occurrences of a bit pattern only when it exists longer or shorter than defined or, on entering or leaving a specified pattern. For example, figure 15 contains a trace list that was defined to locate a bit pattern upon entering CLK=1, IOM=0, etc. A cursor is placed at the desired location in either the trace list or timing diagram.

Marking Timing Events

Timing events can be marked using x and o markers along with four other markers labeled a, b, c, and d. The x and o markers are used to set start and end points of interest. In all cases, the markers can be set using specifications rather than manual positioning (figure 16).

One example of the a, b, c, and d markers could be to indicate the bit pattern that identifies service interrupts. By marking the interrupt with an "a", it is much easier to locate the interrupts in a trace than searching for the handshake that defines the interrupt.

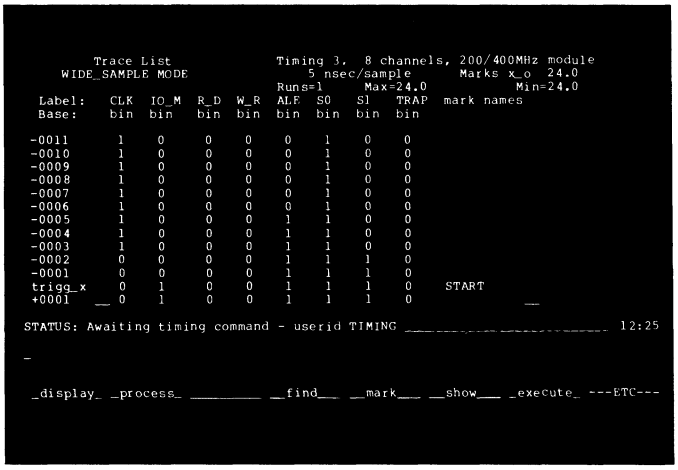


Figure 14. Recalled data from a file named "Test 1" reformatted and displayed in trace list form can be analyzed at your convenience.

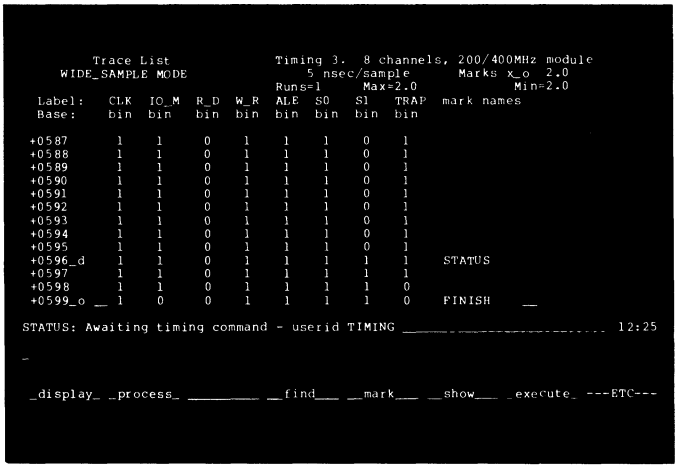


Figure 15. Automatic search through deep memory for a bit pattern simplifies analysis. The cursor "o" identifies the location of the desired bit pattern.

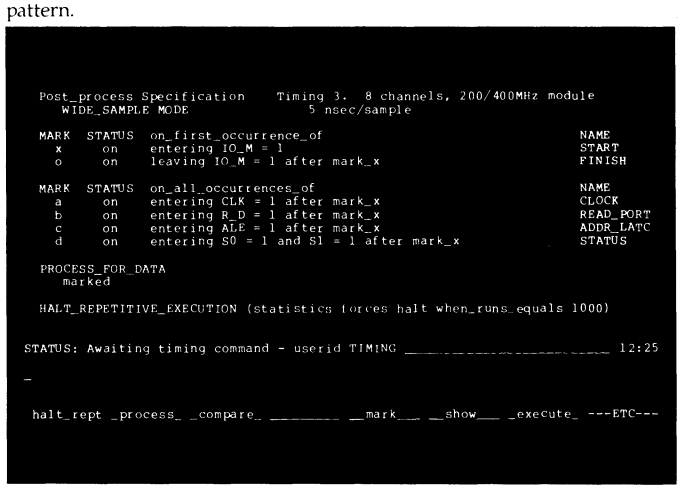


Figure 16. The postprocess specification displays the conditions that have been identified and marked along with other processing specifications, and are displayed even when the conditions were setup in other specifications.

Statistics on Marked Timing Events

The ability to define specific boundaries and parameters allows statistical measurements on those conditions. Statistical measurements can be run on time intervals or event counts by setting the analyzer for repetitive runs with the measurement made and accumulated on each run. A display of the maximum time, minimum time, mean time, standard deviation, and number of runs is updated with each run (figure 17). This measurement can be executed up to 1000 times to get a time interval measurement population for a circuit under test.

In addition to the time interval statistical measurements, the occurrences of other marked conditions within a defined time interval (x and o) can be counted. For example, to determine the number of times an I/O port is read, that condition can be identified as mark "b" (figure 16). The specification is then set to display the number of times mark "b" occurred between the time interval (x and o) on each run, including the maximum and minimum port accesses (figure 18). In addition to the maximum and minimum occurrences, the mean and standard deviation of the marks for the defined number of runs can also be displayed (figure 19).

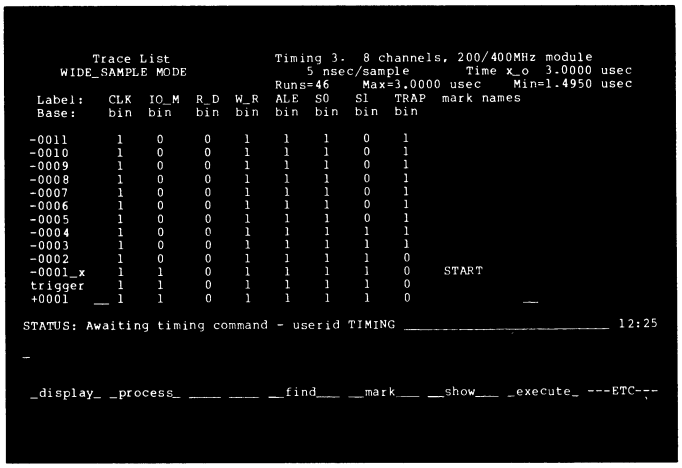


Figure 17. Status information for statistical measurements, number of runs, maximum and miminum times, etc., is displayed in the upper right.

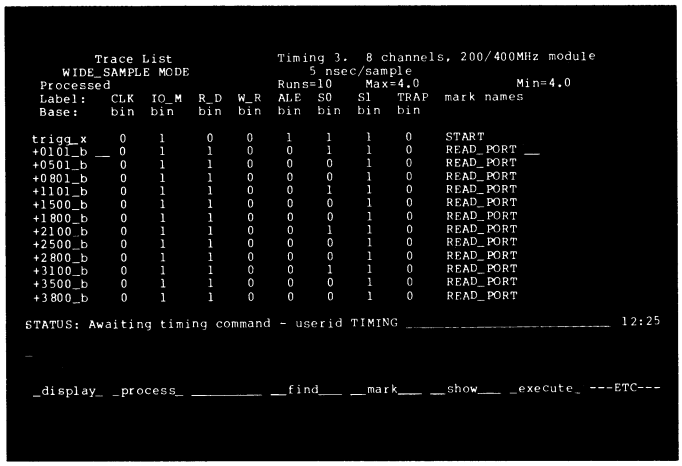


Figure 18. Then number of times a particular bit pattern occurred, mark b, between the marks x_o can be selected for display.

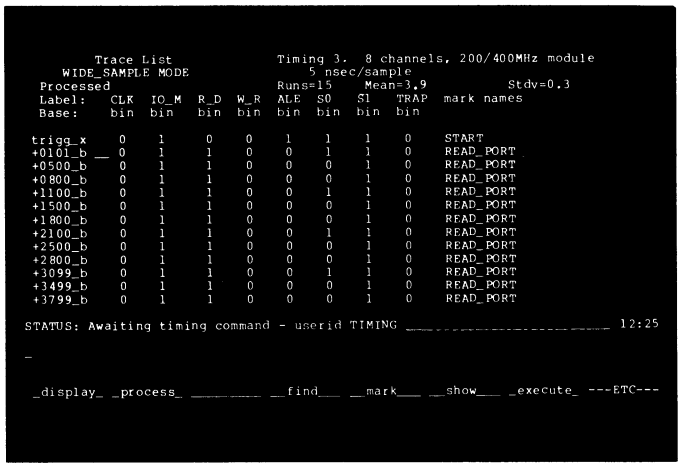


Figure 19. The mean and standard deviation can be automatically calculated and displayed to aid in system characterization.

Extended Triggering

Extended triggering adds another capability to the analyzer. The analyzer can be directed to make repetitive measurements until the number of marks exceed a given amount and then stop the measurement (figure 20). This capability allows the analyzer to capture the data present when there are more mark conditions than expected.

The analyzer can also be directed to trigger when the time interval from point x to point o exceeds a specified time duration (figure 21). This makes it very easy to monitor system operation over many runs and capture any timing violations.

Another powerful aspect of extended triggering is the ability to define sequences as part of a trigger. Up to five marks can be used in a trigger sequence. The mark sequence is set up in the Postprocess Specification (figure 22) and when the sequence is detected during a run, it triggers the analyzer to hold the captured information.

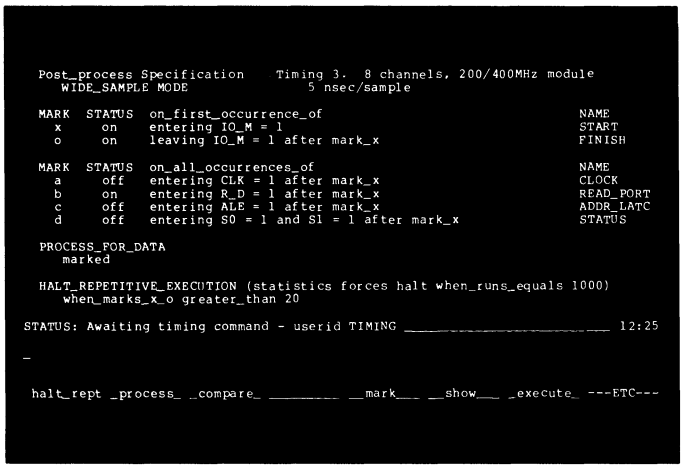


Figure 20. A postprocessing specification can be set up to identify conditions that occur more times than expected with repetitive measurements.

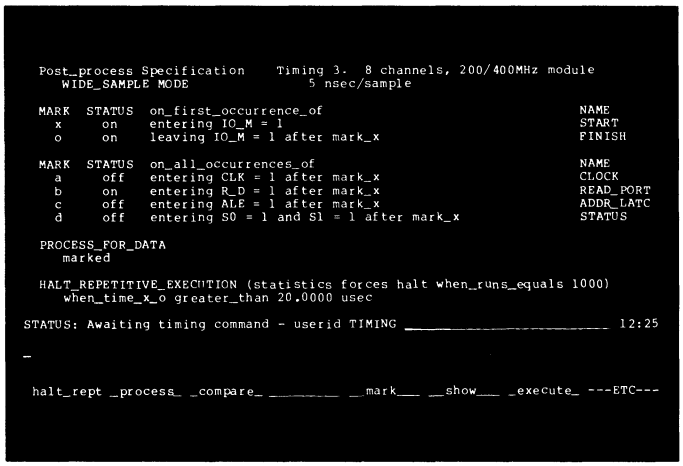


Figure 21. A repetitive measurement may be directed to halt execution when the time between two particular patterns in a program is too long.

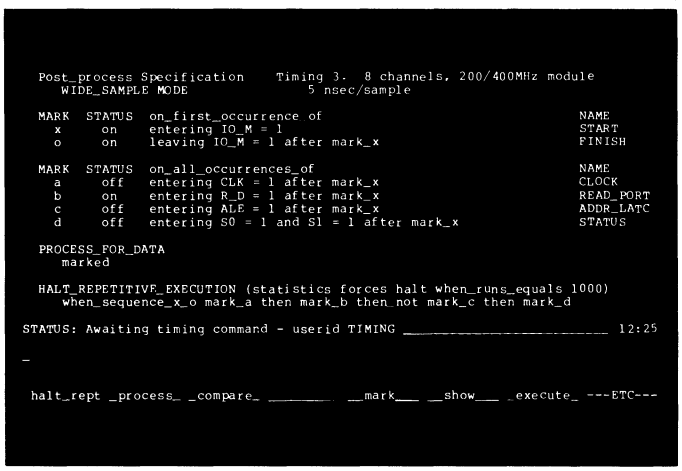


Figure 22. A repetitive measurement may be directed to halt repetitive execution when a defined sequence does not occur. The data acquired can then be analyzed to determine what caused the program to change its sequence.

Processing Timing Display for State Listing

The ability to translate a timing display to a state listing allows additional measurements to be performed on stored information. Data may be processed for conditions or patterns lasting longer than a specified time, removing transition or duplicate states not needed for analysis (figure 23). Additionally, stored data can be processed in relation to a sampled signal that can be defined as a clock with the data synchronized and displayed in relation to the clock as shown in figure 24 (not available in external clock mode). At a 200 MHz sample rate, this effectively gives you 66 MHz synchronous analysis.

Data can also be processed for all marked conditions. This allows the study of only the areas of interest without extraneous information (figure 25).

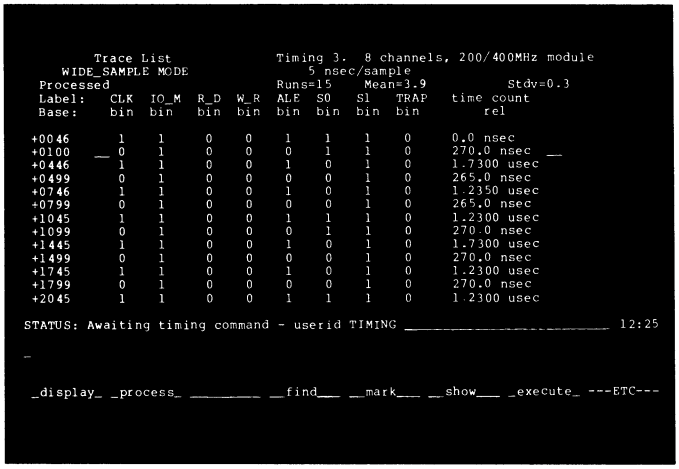


Figure 23. Stored information can be postprocessed to display only the data that existed longer than a defined time period.

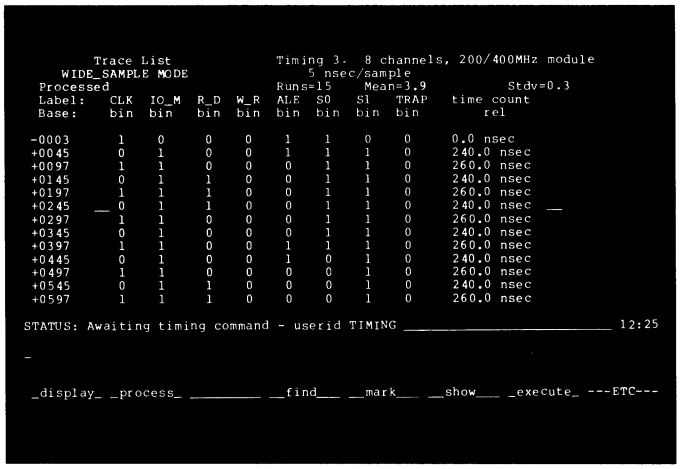


Figure 24. Data can be processed relative to another signal which provides information synchronous to that signal.

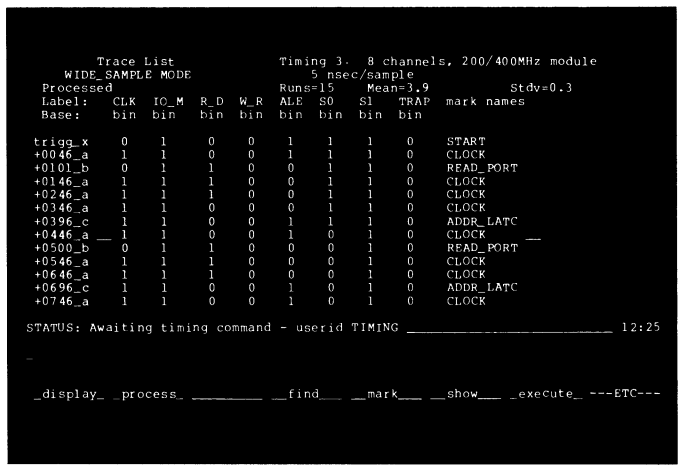


Figure 25. Data in memory can be processed so that only the marked conditions (a,b,c) are displayed to eliminate long searches through memory.

External Clock Mode

The External Clock Mode provides state analysis capabilities at clock speeds to 125 MHz with up to 32 input channels. This allows you to analyze the operation of high speed logic in bit slice and state machines in real time.

Format Specification

When the external clock mode is selected (figure 26), two commands are added that are not available in other operating modes. One, you can select the edge of the external clock that is used to clock in the data present on the data probes. Clock pod status information, such as the clock edge to be recognized and threshold level, is displayed in the upper section of the display.The selection of clock qualify allows clock to be valid only when the qualify input is true. (figure 27). Two, the threshold levels on the clock pod may also be selected.

Trace Specification

The trace specification allows you to set up the trigger parameters necessary to position the measurement window where it is needed for complex state analysis. The triggering functions available for capturing data include:

- Trigger on entering a pattern
- Trigger on leaving a pattern
- Trigger on a state (duration triggering is not available in external clock mode)

State Triggering

State triggering is set up in the External Clock Mode Trace Specification and is used to define a trigger condition on one to 32 channels depending on the analyzer configuration. The trigger specification (figure 28) may be entered in binary, octal, hexadecimal, or decimal. The Boolean NOT condition of a pattern may also be defined as a trigger.

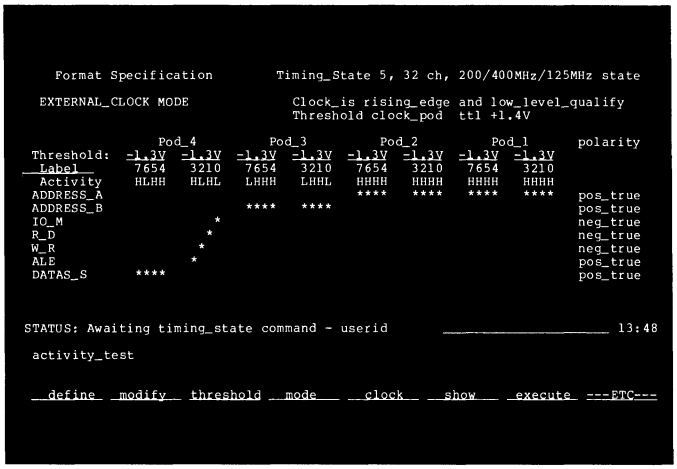


Figure 26. External clock mode can be selected in either the format or trace specification.

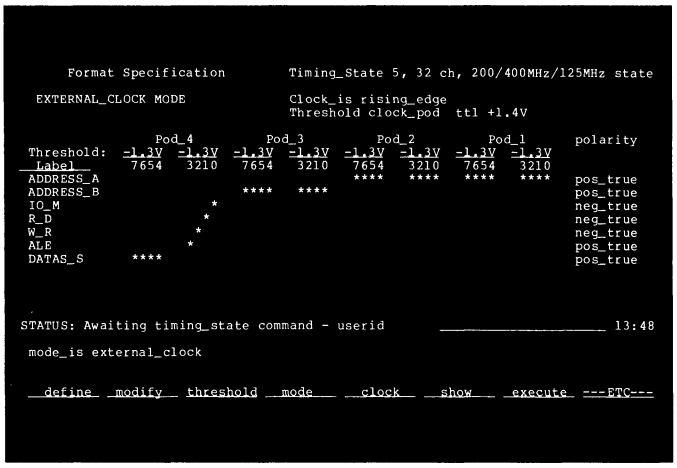


Figure 27. In the Format Specification, an activity test is available to dynamically display the activity on each channel.

Figure 28. In the Trace Specification, state triggering may be specified on a set of channels or on individual channels in hexadecimal, octal, decimal, or binary formats.

State Trace Listing

A state trace list resulting from the trace specification in figure 28 is shown in figure 29. Note that the sequential trigger point was located as directed (address_A=FFFF followed by Address_B=F6H and R_d=1 and IO_M=0). The displayed trigger point is the last condition of the trace specification. The captured data may then be displayed in the desired format by using the softkey selections.

Post Process Specification

An automated comparison of stored versus newly acquired data can be performed in the post process mode. In the post process specification, you can define the compare file to be stored and the trigger point for the data to be compared (figure 30). In this example, the comparison will be Address A compared to Stored address A when ALE is valid. The measurement will continue to run until the comparison is not equal.

Upon execution of a trace, the analyzer captures new data and performs a bit-by-bit comparison to the stored data. When a fault is found, the analyzer halts execution and displays the faults.

Trace Listing

The trace list that results from an automated comparison of stored and newly acquired data provides a display of the data with the differences clearly identified (figure 31). The date and time when the fault occurred are available for print out to help locate the probable cause. The ability to identify faults with one of the available marks makes the comparison mode extremely easy to use.

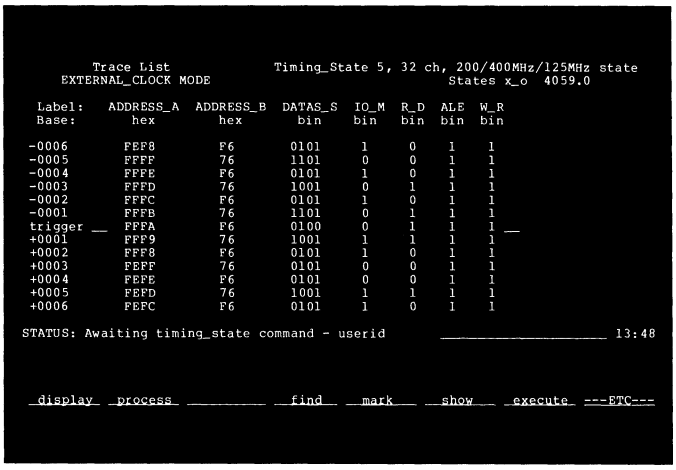


Figure 29. The Trace list resulting from the trigger condition in figure 28 is displayed in the selected format.

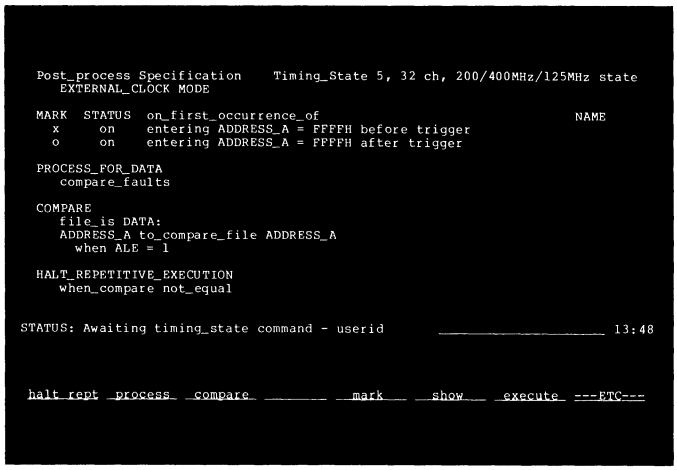


Figure 30. The Post Process Specification is used to define the type of comparison and how it will be executed.

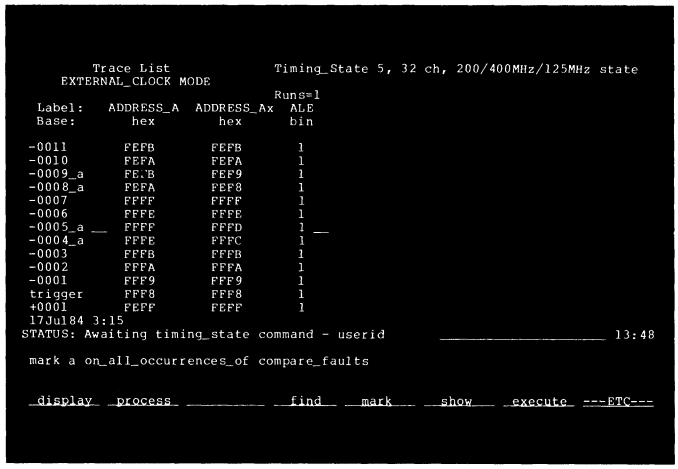


Figure 31. The newly acquired data may then be displayed along with the stored data with the differences marked for easy identification.

Timing/State Compare

The state information may also be displayed in timing diagram form with the currently acquired data displayed adjacent to the stored data for easy comparison (figure 32). Vertical dashed lines across the timing diagram lines being compared indicate where the faults occurred between the stored and newly acquired data. Displayed waveforms are differentiated by labeling the stored waveform with an x. This post processing comparison can be performed in both timing and state analysis modes.

Comparing Stored and Current Measurements

There are times when it is useful to automatically compare stored and current timing waveforms. The postprocessing specification allows designation of a compare file where a timing waveform can be stored, another measurement executed, and then both displayed simultaneously with marks identified with dashed lines (figure 33). Displayed waveforms are differentiated by labeling the compare file waveform with an x. This is in addition to the automated compare mode.

Data Probe

The HP 64604A data probe consists of a cable connected to the acquisition board in the station, a detachable probe pod (figure 34) containing a hybrid circuit with an active comparator, and eight detachable coaxial probe inputs. The probe leads are similar to HP 10017A miniature oscilloscope probes which allows all the accessories (tips, clips, etc.) to be used with the timing probe. A Model 10211A dual-in-line package clip, supplied with the timing probe, allows easy connection to most 0.3, 0.4, 0.6, and 0.9-inch wide IC packages. The HP10211A clip is also stackable, end-to-end, to allow probing all pins on 40 or 60-lead packages.

Probe inputs are compensated to provide the comparator in the pod a high fidelity reproduction of the signal at the probe tip, avoiding the ringing and resulting uncertainty associated with open-wire probes and fast edges. The input impedance at the tip is 100kΩ in parallel with 6 pF capacitence.

The probe has two comparison thresholds, one for channels 0 through 3 and one for channels 4 through 7. The thresholds are set by software from −10 V to +10 V in 0.1 V steps. The dynamic range of the probe is specified as ±10 V. Exceeding this value, as might happen with CMOS circuits using 15 V supplies, causes less than 1 ns of additional skew as the input clamps are activated, and there is essentially no change in loading.

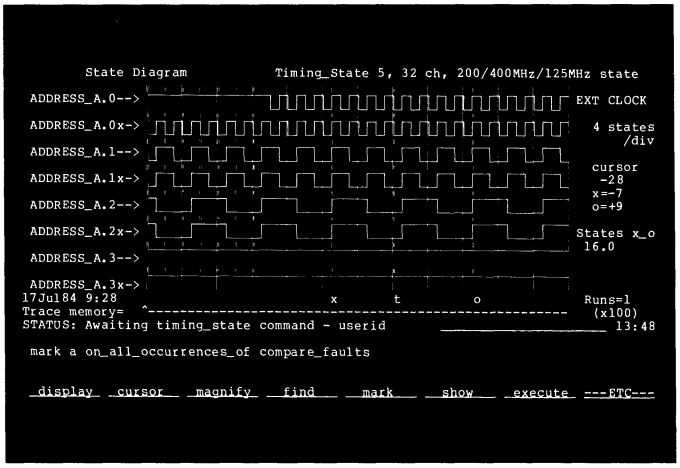


Figure 32. State information may be converted to a timing diagram format to display the compared faults.

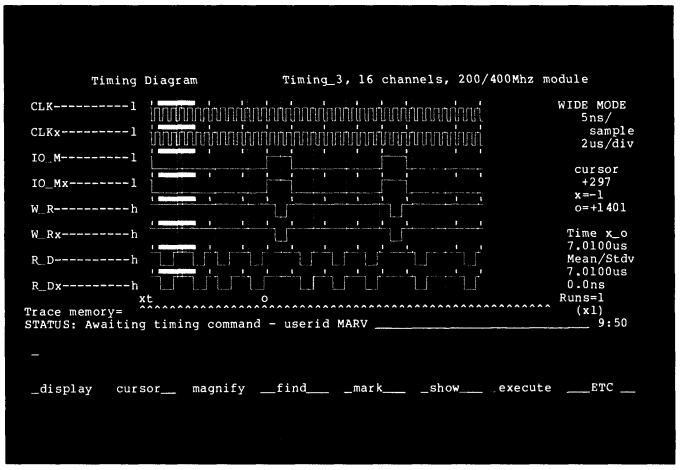


Figure 33. Stored timing diagrams can be recalled for comparison to current measurements, labeled with an x.

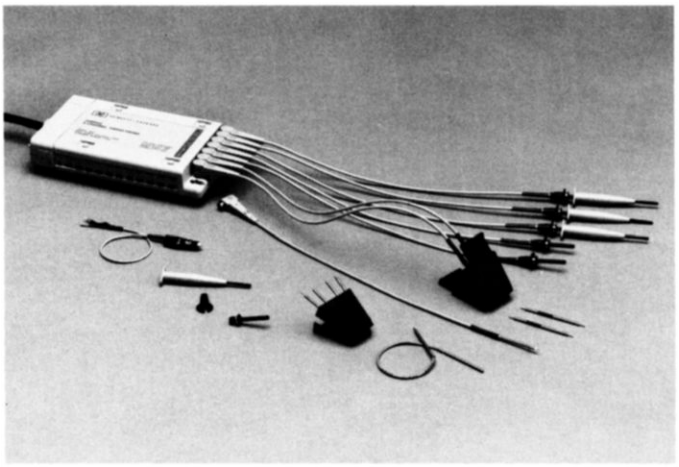


Figure 34. A variety of probe tips and clips simplify connection of the to your system. The miniprobe tip can be used with a variety of accessories including pincer tips, ground leads, and IC test clips.

Clock Probe

Model 64605A Clock Probe consists of a probe pod and cable with two detachable coaxial probe input leads. One probe is for the clock input and the other is the qualify input, both with a dynamic range of ±10 V. Each probe input is conditioned so that there are two outputs to the control board. The control board receives four outputs from the clock probe and selects rising or falling edge clocks, and high or low level qualify signal.

Data Delay Pod

To compensate for delays through the clock probe, a data delay pod, added to the data probe, provides data synchronization during state analysis. The delay pod contains the delay lines that maintain the time relationship between clock and data signals supplied to the acquisition card. A delay pod is inserted between each data pod and its cable to the acquisition board in the development station.

Hard Copy Output

Printouts of timing displays for records are available by adding a Model 64050A Graphics Output Card. HP-IB compatible printers can be used directly without the need for an additional external interface. The graphics output card transmits both text and graphics.

Graphics information is transmitted using raster graphics consisting of 720 dots scanned left to right in 90 8-bit bytes. Model 2631G Option 200 Graphics Printer and Model 2673A Intelligent Graphics Printer are compatible with the HP64050A graphics output card. For more information about the compatibility of other HP graphics printers, please consult with your local HP Instrumentation Field Engineer.

Specifications

RESOLUTION
Overall Resolution: ±(sample period + skew).
Total Skew from Probe Tip: within pod, ±1.5 ns; pod to pod: ±3.0 ns. These specifications are true for input signal, VH=-1.0 V, VL=-1.6 V, VTH at 1.3 V, slew rate 0.25 V/ns without a delay pod. For skew specifications under other conditions, refer to the Operating Manual.
Sample Rate Accuracy: approx ±0.002%, sample rate adjustable from 2 Hz to 400 MHz (in fast-sample modes) in a 1, 2, 4 sequence.

EXTERNAL CLOCK
Clock Frequency: 0 to 125 MHz max.
Minimum Width: 3 ns at threshold.
Setup Time: 4 ns max data to clock, 4 ns max qualify to clock.
Hold Time: 0.5 ns max data and qualify to clock.
These specifications are true for input signal, VH=-1.0 V, VL=-1.6 V, VTH at 1.3 V, slew rate 0.25 V/ns.

MEMORY DEPTH
Wide Sample, Glitch, external Clock,and Dual Threshold Modes: 4k.
Fast Sample Mode: 8k.

DATA AND CLOCK
PROBE CHARACTERISTICS
Input Z: 100 kΩ ±2% shunted by <6 pF.
Dynamic Range: ±10 V.
Maximum Input: ±40 V.
Threshold Accuracy:
±50 mV or ±2%, whichever is greater.
Hysteresis: approx 50 mV.
Drive Requirements
Minimum input amplitude: 600 mV, P-P.
Minimum input overdrive: 200 mV or 25% of input amplitude, whichever is greater.
Minimum pulse width: 3 ns at threshold.

GLITCH MODE
Maximum Sample Rate: 100 MHz.
Minimum Glitch Width:
3 ns at threshold without data delay pod.
Maximum Glitch Width: sample period less 4 ns.

TRIGGERING
Time Duration Accuracy: ±(20% + 2 ns).
Time Duration Restart:
for accurate restarts, pattern must go false for at least 1.5 times the selected time duration.
Minimum Width for "Narrower than" Trigger: approx 5 ns.
Minimum Width for Transition Trigger:
approx 5 ns.
Displayed Position Accuracy:
±2 samples; ±4 samples in Fast Sample mode.
Delay from Input to External BNC Drive:
approx 55 ns.
Delay from Input to Internal IMB Drive:
approx 45 ns.
Dead Time for Restart Measurement Reset: approx 50 ns + the time required to fill the memory with the selected amount of pretrigger information.

BNC DRIVE
Output Signal Swing in Transition Trigger Mode
Amplitude: approx 2.0 V with 50 Ω load.
Width at 50%: approx 10 ns.
Output Signal Swing in "Width Greater than" Trigger Mode
Amplitude: approx 2.5 V.
Width: input trigger width less selected duration.
Output Signal Swing in "Width Less-than" Trigger Mode
Amplitude: same as in transition trigger mode.
Width: same as in transition trigger mode.
Position: occurs when trigger pattern disappears before selected duration times out.

Power Requirements
Current Required for Timing Analysis Subsystem Components

Note: Refer to the HP 64000 Logic Development System Selection and Configuration Guide for power requirements. The chapter on Configuration Requirements contains data for calculating current required for subsystems to be installed, and currents available in development stations. Model 64100A Development Station, serial number prefix 2136 and below, can be retrofitted to accommodate new subsystems if required. Please contact your Hewlett-Packard Logic Systems Field Engineer or System Engineer for further information.

DEVELOPMENT STATION SUPPLY:	+5V	+12V	+17V	-3.25V	-5.2V	-12V
TIMING MODULE						
Timing Control	1.6A	-	-	1.5A	2.1A	0.02A
Timing Acquisition	3.6A	-	-	2.5A	0.8A	-
Timing Probe	0.04A	-	-	-	0.24A	-
Clock Probe	0.04A	-	-	-	0.08A	-

ENVIRONMENTAL
Conforms to environmental specifications of Model 64100A or 64110A Development Station.

Accessories Supplied

Model 64610S: one Model 64601B Control Card, one Model 64602A Data Acquisition Card, one Model 64604A Data Probe, one Model 64605A Clock Probe, one Model 64606A Delay Pod, one Model 64963A 2-position bus cable, Operating Software on flexible disc, and Operating and Service Manuals.

Model 64610S Opt 016: one Model 64601B Control Card, two Model 64602A Data Acquisition Cards, one Model 64605A Clock Probe, two Model 64604A Data Probes, two Model 64606A Delay Pods, one Model 64963A Opt 001 3-position bus cable, Operating Software on flexible disc, and Operating and Service Manuals.

Model 64610S Opt 024: one Model 64601B Control Card, three Model 64602A Data Acquisition Cards, one Model 64605A Clock Probe, three Model 64604A Data Probes, three Model 64606A Delay Pods, one Model 64963 Opt 002 4-position bus cable, Operating Software on flexible disc, and Operating and Service Manuals.

Model 64610S Opt 032: one Model 64601B Control Card, four Model 64602A Data Acquisition Cards, one Model 64605A Clock Probe, four Model 64604A Data Probes, four Model 64606A Delay Pods, one Model 64963A Opt 003 5-position bus cable, Operating Software on flexible disc, and Operating and Service Manuals.

Model 64610S Opt 001: one Model 64601B Control Card, one Model 64602A Data Acquisition Card, one Model 64604A Data Probe, one Model 64963A 2-position bus cable, Operating Software on flexible disc, and Operating and Service Manuals.

Model 64610S Opt 002: one Model 64601B Control Card, two Model 64602A Data Acquisition Cards, two Model 64604A Data Probes, one Model 64963A Opt 001 3-position bus cable, Operating Software on flexible disc, and Operating and Service Manuals.

Model 64610S Opt 003: one Model 64601B Control Card, three Model 64602A Data Acquisition Cards, three Model 64604A Data Probes, one Model 64963A Opt 002 4-position bus cable, Operating Software on flexible disc, and Operating and Service Manuals.

Model 64610S Opt 004: one Model 64601B Control Card, four Model 64602A Data Acquisition Cards, four Model 64604A Data Probes, one Model 64963A Opt 003 5-position bus cable, Operating Software on flexible disc, and Operating and Service Manuals.

Model 64604A Data Probe: eight ground leads (P/N10006-61301), eight probe holders (P/N 10017-62302), eight IC probe tip adapters (P/N 10017-69501), eight timing probe leads (P/N 64604-62101), eight split rings (P/N 64604-23201), one Model 10211A 20-pin dual in-line package clip with one interconnecting ground wire (P/N 10211-61601) and two insulated circuit interface pins and one Model 10024A IC Test Clip with four insulated circuit interface pins.

Model 64605A Clock Probe: two ground leads (P/N 10006-61301), two ground clips (P/N 5061-1258), two probe holders (P/N 10017-62302), two probe tip adapters (P/N 10017-69501), two timing probe leads (P/N 64604-62101), and two split rings (P/N 64604-23201).

Ordering Information

Model 64610S: 8-channel Timing/State Analyzer with one data probe, one clock probe, and one delay pod — $ 7850
Model 64610S Opt 016: 16-channel Timing/State Analyzer with two data probes, one clock probe, and two delay pods — $13,120
Model 64610S Opt 024: 24-channel Timing/State Analyzer with three data probes, one clock probe, and three delay pods — $18,250
Model 64610S Opt 032: 32-channel Timing/State Analyzer with four data probes, one clock probe, and four delay pods — $23,350
Model 64610S Opt 001: 8-channel Timing Analyzer with one data probe — $ 6700
Model 64610S Opt 002: 16-channel Timing Analyzer with two data probes — $11,420
Model 64610S Opt 003: 24-channel Timing Analyzer with three data probes — $16,150
Model 64610S Opt 004: 32-channel Timing Analyzer with four data probes — $20,900
Model 64610S Opt 005: Updates existing Model 64600S 8-channel timing analyzer to state analysis capability — $ 3500
Model 64610S Opt 006: Updates existing Model 64600S 16-channel Timing Analyzer to state analysis capability — $ 4000
Model 64050A: Graphics Output Card — $ 1000

Components

Note:
Order replacement items from the following list.
Model 64601B control card — $2000
Model 64602A 8-channel acquisition card (for 64610A) — $3500
Model 64602A Opt 001 clock cable (for 64600S) — no charge
Model 64604A data probe — $1200
Model 64605A clock probe — $ 750
Model 64606A data delay pod — $ 400
Model 64963A 2-position bus cable — no charge
Model 64963A Opt 001 3-position bus cable — no charge
Model 64963A Opt 002 4-position bus cable — no charge
Model 64963A Opt 003 5-position bus cable — no charge
Model 64964A 2-position IMB cable — no charge
Model 64964A Opt 001 3-position IMB cable — no charge
Model 64964A Opt 002 4-position IMB cable — no charge
Model 64964A Opt 003 8-position IMB cable — no charge
Model 64050A Graphics Output Card — $1000

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