File Number 1620-OEMI
Form A26-5569-0

IBM Systems Reference Library

IBM 1620 Original Equipment Manufacturers' Information

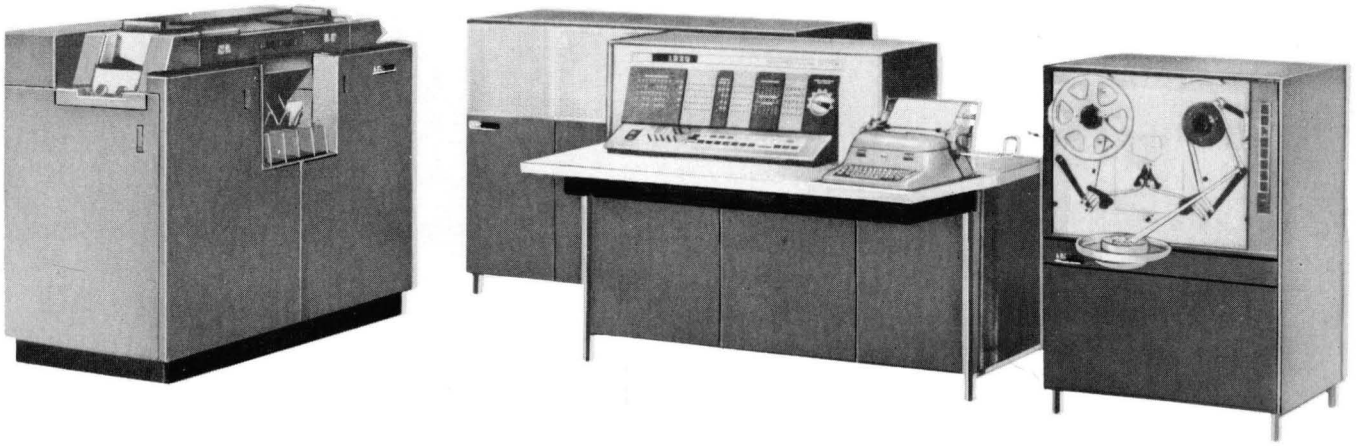
This manual provides non-IBM engineers with sufficient data to attach units of the IBM 1620 System to their equipment. It contains supplemental tie-in data not readily available in other IBM publications, and tables that show characteristics of data and signal lines at the cable connectors.

Address comments regarding the content of this publication to:
IBM, Product Publications Department, San Jose, California

Contents

Preface

Each of the five sections in this manual is designed to provide all the information on interconnecting lines necessary to attach any of the five units of the 1620 Data Processing Unit to non-IBM equipment. The references in each section indicate additional sources of information regarding the manner in which the particular unit operates within the 1620 System.



IBM 1620 Data Processing System

This section provides data to satisfy the special needs of non-IBM engineers who wish to attach other than IBM input/output devices to the 1620 Central Processing Unit. It provides easy access to supplemental tie-in data not so readily available in other IBM publications.

Detailed theory and mechanical principles of operation are not included. These may be found in the following IBM publications relating to the 1620 System.

Title	*Form*
IBM 1620 *CE Manual of Instruction*	227-5507
IBM 1620 *CE Reference Manual*	227-5500
IBM *B1 Electric Typewriter CE Reference Manual*	223-6652
IBM 1620 *Data Processing System Reference Manual*	A26-4500

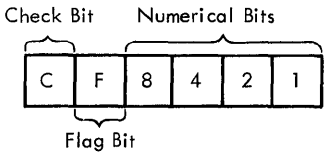
Additional engineering information can be obtained from system diagrams and other available engineering documents.

General Description

The IBM 1620 Data Processing System is a solid-state electronic computer system, designed for technological applications. The system is composed of four separate units as follows:

1620	Central Processing Unit	Contains console, processing circuitry, input/output typewriter and 20,000 positions of core storage.
1621	Paper Tape Reader	Reads 8-channel paper tape. The 1621 also contains space for the 1624 Paper Tape Punch.
1622	Card Read Punch	Contains a buffered card reader and card punch.
1623	Additional Core Storage	Contains one or two additional blocks of 20,000 positions of core storage.
1624	Paper Tape Punch	Eight-channel tape punch. Physically located in the 1621 unit.

Data and instructions can be entered into the system from the typewriter, paper tape reader, or card reader. They are entered in binary-coded-decimal form (BCD) using the bit configuration shown in Figure 1. Each of the 20,000 (basic machine) positions of core storage can be addressed individually by a 5-digit address. The addressing system provides for the selection of any digit or group of digits within core storage.



	C	F	8	4	2	1
0	X					
1						X
2					X	
3	X				X	X
4				X		
5	X			X		X
6	X			X	X	
7				X	X	X
8			X			
9	X		X			X

Figure 1. Bit Positions and Bit Configuration

The computer can perform the 32 basic operations listed in Table 1 and several special feature OP codes. Each operation is specified by a 12-digit instruction which contains a 2-digit operation code and two 5-digit addresses (Figure 2). Instructions comprising a program are normally stored in consecutive locations in memory and are executed sequentially.

Data and Instruction Format

The 1620 is a variable-field length computer. The shortest admissible field is two digits. The longest can be any number of digits within the capacity of core storage. The flag bit (Figure 1) associated with each BCD bit is used as a field mark to designate the high-order position of a numerical field. A flag bit associated with the units position of a numerical field determines

Table 1—Operation Codes

Arithmetic Instructions	CODE
Add	A21
Add (Immediate)	AM11
Subtract	S22
Subtract (Immediate)	SM12
Compare	C24
Compare (Immediate)	CM14
Multiply	M23
Multiply (Immediate)	MM13

Internal Data Transmission Instructions

Transmit Digit	TD25
Transmit Digit (Immediate)	TDM15
Transmit Field	TF26
Transmit Field (Immediate)	TFM16
Transmit Record	TR31

Branch Instructions

Branch	B49
Branch No Flag	BNF44
Branch No Record Mark	BNR45
Branch on Digit	BD43
Branch Indicator	BI46
Branch No Indicator	BNI47
Branch and Transmit	BT27
Branch and Transmit (Immediate)	BTM17
Branch Back	BB42

Input/Output Instructions

Read Numerically	RN36
Write Numerically	WN38
Dump Numerically	DN35
Read Alphamerically	RA37
Write Alphamerically	WA39
Control	K34

Program Control

Set Flag	SF32
Clear Flag	CF33
Halt	H48
No Operation	NOP41

the sign of the field – no flag is a plus field, a flag bit is a minus field. A flag bit is also used in add table storage to indicate a carry.

A digit in memory occupies one memory position and is addressed individually. Fields in memory consist of a number of consecutive digits. A field is addressed by its rightmost (low-order) position which occupies the highest numbered memory position of the field. Fields

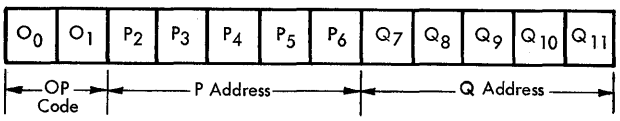


Figure 2. Instruction Format

are processed from right to left into successively lower memory positions until a digit with a flag bit is sensed. Records in memory consist of a field or fields of data related to input/output operations and internal record transmission. A record in memory is addressed at the leftmost (high-order) position, which occupies the lowest numbered memory position of the record. Records are processed serially from left to right into successively higher memory positions. Output and internal record transmission operations are terminated whenever a record mark is sensed.

The 1620 System may be programmed so that input occurs in either a numerical or alphabetical mode. Output from core storage to the output device may also be programmed in either numerical or alphabetical mode. When input or output occurs in a numerical mode, each character in core storage is represented as a single digit occupying one storage position. When input or output occurs in an alphameric mode, each character in storage is represented as two digits occupying two adjacent memory positions. Figure 3 illustrates the code used. In the alphameric mode, data may consist of numerical, alphabetical, or special characters.

Each instruction is stored in memory as a 12-digit number. The instruction contains a 2-digit operation code and two 5-digit addresses (Figure 2). The functions of the P and Q address portions of the instruction are dependent upon the particular operation to be performed. The P part of an instruction may be used to represent an address in memory of a digit, a field, a record, or another instruction. The Q part may represent the address in memory of a digit, a field, a record, or a data field itself. The Q part may also be used in connection with an input/output instruction to specify the address of the I/O device, or the control function to be performed.

Stored Program

To solve a problem or to process data, the programmer selects a logical sequence of operations from those the computer is capable of performing. This series of instructions which designate the operations to be performed is called a program. Because the instructions comprising a program are written into memory from an input device and read from memory for interpreta-

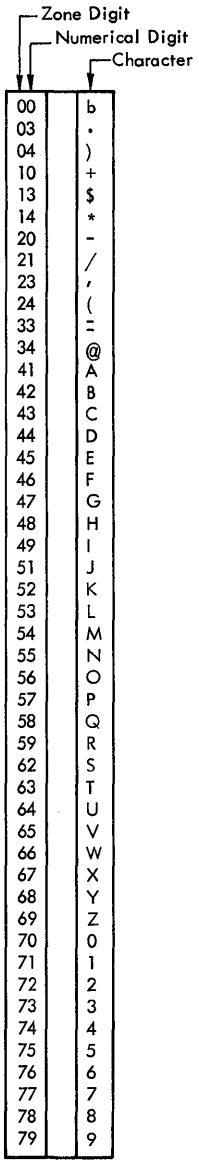


Figure 3. Alphameric and Special Character Codes

tion and execution, the 1620 is called a stored program computer.

In order to be interpreted by the computer, each instruction must be read from memory to registers. The high-order digit (O_0) is read first. The readout continues through successively higher memory positions until Q_{11} is read. Instructions within a program are normally executed sequentially (Figure 4). However, the sequence may be altered by use of conditional branch instructions.

INSTRUCTIONS

The computer can perform the 32 operations listed in Table 1, plus several special feature codes. The instruction complement can be divided into five types as follows:

Arithmetic. Arithmetic operations are accomplished by a table method. Three hundred twenty (320) positions of memory are assigned for use in arithmetic operations. Twenty (20) positions, 00080 through 00099, are used to store products in multiply operations and dividends in divide operations. Two hundred (200) positions, 00100 through 00299, are allocated for the storage of a Multiply Table. The Multiply Table contains all possible 2-digit products. One hundred (100) positions, 00300 through 00399, store an Add Table, used in all arithmetic operations. The Add Table contains all possible 2-digit sums, with carries indicated. The memory positions containing the table data are addressable.

Internal Data Transmission. Internal transmission operations accomplish the transfer of a digit, a field, or a record from one memory location to another. Two memory cycles are required for processing each digit. During the first cycle, the digit to be transmitted is read out of memory to a register. During the second memory cycle, the digit in the register is transferred to the desired memory location.

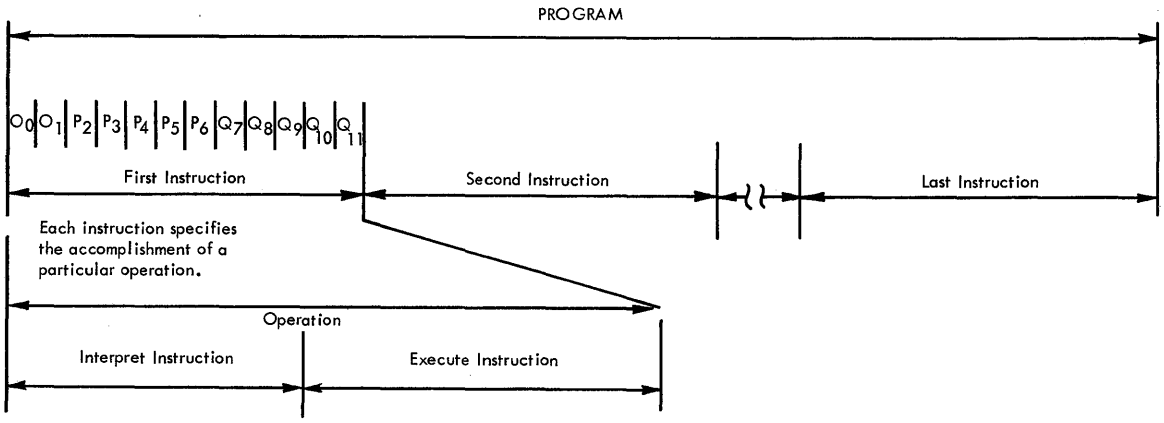


Figure 4. Program

Branch. The normal sequential execution of instructions may be altered at any point in the program by branch instructions. These instructions may be classified into two categories:

1. Unconditional branch instructions always alter the sequential execution of a program when they are executed. Unconditional branch instructions are Branch, Branch and Transmit, and Branch Back.
2. Conditional branch instructions make logical decisions by performing tests on indicators or switches set by the computer or by the operator. The branch on flag, indicator, digit, record-mark instructions are all conditional branch instructions.

Input/Output. The input devices for the 1620 Data Processing System are the 1621 Paper Tape Reader, the console typewriter, and the 1622 Card Read Punch. Instructions or data may be entered into memory by any of these units of the 1620 System. The output devices for the 1620 Data Processing System are the 1624 Paper Tape Punch, the console typewriter, and the 1622 Card Read Punch.

The Q_8 and Q_9 digits of input/output instructions are used to select the desired device using the 2-digit addresses listed below:

01 Typewriter
02 Paper Tape Punch
03 Paper Tape Reader
04 Card Punch
05 Card Reader

Only one device may be selected at a time. The device remains selected until the execution of the input/output instruction is terminated.

The Paper Tape Reader-Punch and the Card Read Punch are special features of the 1620 System. The console typewriter is an integral part of the processing unit. The typewriter can be used to enter instructions and data into memory or to print out data from memory. A record of input data is obtained as a byproduct of an input operation. The output rate is 10 characters per second, the input rate depends on the speed of the operator. Depression of the Insert key on the console allows the direct keyboard entry of instructions or data into memory, starting at address 00000. Depression of the Release key locks the keyboard so entry is no longer possible. Space, carriage return, and tabulate are typewriter functions which may be programmed to permit automatic output format control.

Control Keys and Lights

The console (Figure 5) is an integral part of the central processing unit. It provides for manual or automatic control of the system. The console keys, switches, and typewriter are used to:

1. Place data and instructions in core storage.
2. Display the contents of registers and core storage.
3. Alter the contents of core storage.
4. Display the machine and program status indicators.
5. Instruct the machine manually, that is, start, stop, etc.

Signal lights associated with the control keys provide a visual indication of specific operating conditions in the computer and indicate which step of the keying procedure was last completed. Basic control keys and lights are described below (see Figure 5). Register and

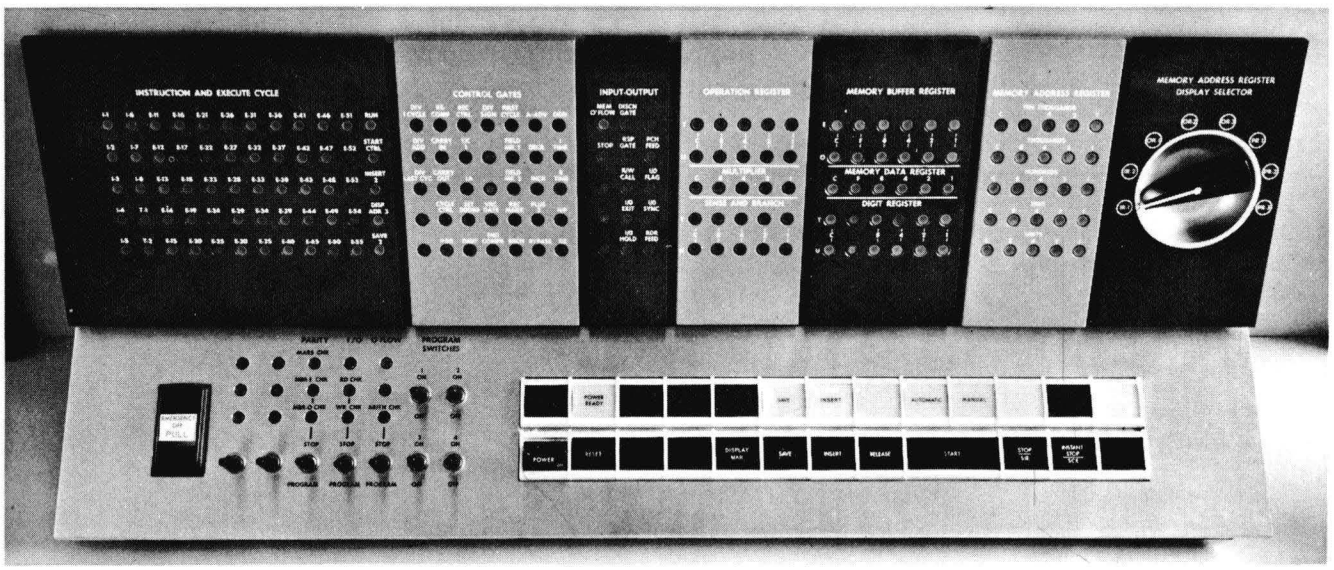


Figure 5. 1620 Console

control gate indicators are described fully in the 1620 *Data Processing Machine Reference Manual,* Form A26-4500.

POWER SWITCH — POWER ON LIGHT

The Power switch has an ON position and an OFF position. The Power switch when set to the ON position applies electrical power to the computer and turns on the Power ON light.

POWER READY LIGHT

The Power Ready light comes on when internal machine temperature and voltages reach proper operating values. There is a delay from the time the Power switch is positioned ON until operating temperature and voltages are reached. This delay varies with room temperature and the time elapsed since power was turned off.

EMERGENCY OFF SWITCH

This switch is for emergency use only. If positioned OFF, all power is turned off in the machine. As a result, the blowers that cool the electronic circuits are stopped. With the blowers off, damage to the machine may result.

AUTOMATIC AND MANUAL LIGHTS

Whenever the Manual light is on, the computer is in manual mode. In manual mode, the computer has terminated all operations and is prepared to accept operator intervention. Whenever the Manual light is off, the computer is in automatic mode, (for example, while it is executing a stored program or entering data into core storage from the typewriter keyboard).

The Manual light is turned on by the execution of a halt instruction or by depression of the Release key or Stop key. Depression of any of the following control keys turns the Manual light off: Start key, Insert key, and Display MAR key. The Save light and/or a No-Feed light can be on when the Manual light is on.

Both the Manual and Automatic lights are on when an instruction is single-cycled with the Single Cycle Execute (SCE) key.

START KEY

The Start key is used to start program processing and to put the computer in automatic mode. It is operative only when the computer is in manual mode.

RELEASE KEY

The Release key is used to terminate any input/output operation, including console keyboard entry of data into core storage. When this key is depressed, manual mode is initiated, the Manual light is turned on, and the Insert light is turned off.

The Release key is operative only when the computer is in automatic mode.

RESET KEY

The Reset key is used to restore all machine status indicators, machine check indicators, and signal lights to their initial or reset condition. Parity errors can occur if the Reset key is used while the computer is in the automatic mode.

INSERT KEY AND LIGHT

Depression of the Insert key turns on the Insert light and activates the typewriter keyboard so that direct entry of instructions may be made in numerical mode, starting at 00000 and continuing into higher-numbered core storage positions. Up to 100 digits may be keyed in. After the 100th digit is entered, an automatic release is initiated and the machine returns to manual mode.

The Insert key is operative only when the computer is in manual mode.

SAVE KEY AND LIGHT

Depressing the Save key saves the address of the next sequential instruction to be executed and turns on the Save light. The saved address is lost if a multiply operation is performed before the saved address is used.

STOP/SIE (SINGLE INSTRUCTION EXECUTE) KEY

Depression of the Stop/SIE key stops the computer in manual mode at the end of the instruction being executed.

The Stop/SIE key also serves as a Single Instruction Execute key. Successive depressions of the key cause one instruction to be executed for each depression. The Manual light remains on.

INSTANT STOP/SCE (SINGLE CYCLE EXECUTE) KEY

Depression of the Instant Stop/SCE key causes the machine to stop at the end of the 20-microsecond machine cycle then in progress. Successive depressions of the key cause single machine cycles. Both the Manual and Automatic lights remain on.

INSTRUCTION AND EXECUTE CYCLE

The Instruction and Execute Cycle lights are a visual aid for the console operator in stepping an instruction through I and E cycles with the Instant Stop/SCE key. The I and E lights progress through each cycle with repeated depressions of this key.

CHECK STOP LIGHT

The Check Stop light is turned on when the machine stops because of a parity check. One or more of the Parity or I/O Check indicators responsible for the stop will also be on. The Check Stop light is turned off when the check indicators are reset or when Parity or I/O switch is set to program.

DISPLAY MAR KEY

The Display MAR key is operative only when the Manual light is on and the Automatic light is off. Depression of the Display MAR key causes display of the MARS register to which the MARS Display Selector switch is set.

The rotary switch should not be turned while the Display MAR key is depressed.

READER NO-FEED LIGHT

The Reader No-Feed light is turned on if:

1. The computer executes a write instruction using the tape punch and there is no paper tape on the feed reel.
2. A parity check occurs while the paper tape is being punched.
3. The paper tape supply is exhausted.
4. The card punch is not ready.

Any of these conditions stops the computer in automatic mode with both the Automatic and Punch No-Feed lights turned on. When a parity error occurs, the I/O Write Check light is also turned on. Depression of the Release key disconnects the punch and puts the computer in manual mode. Depression of the Reset key, while the computer is in manual mode, turns off the Punch No-Feed and I/O Write Check lights. Manual correction and restart procedures can begin after the Release and Reset keys are depressed.

THERMAL LIGHT

The Thermal light is turned on when the internal temperature of the machine becomes too high. At the same time, power is turned off and the Power Ready light turns off. After the internal machine temperature returns to normal, the Thermal light may be turned off by depression of the Reset key. The Power switch must be turned off and on again before power can be applied to the machine.

Input/Output Data and Control Lines

The following material summarizes the key characteristics of all data, control, and power lines between the 1620 console unit and the tape reader-punch, the card read punch, and the additional storage unit. Figure 6 shows the location of cable connectors in the 1620 System.

Lines to the 1621 Paper Tape Reader

Information on the lines that interconnect the 1620 and 1621 is given in terms of the manner in which the 1620 accepts and receives data and control signals. Characteristics of the 1620 input data and control lines are summarized in Table 2. The following comments apply to the shoe connector lines (SC) listed in Table 2 and in System Diagram, 00.00.20.0.

Table 2—1620 Connections from the 1621

1620 Shoe Connector	Title	1620 Card Type	I/O	1620 System Diagram	1621 Card Type	Current Required	Rise Time μsec	Fall Time μsec	Signal Level On	Signal Level Off
SCA11	+S Tape Level 1	MX, CD	I	01.83.20.1	MX	2.1 ma	5	5	+S	−S
SCA12	+S Tape Level 2	MX, CD	I	01.83.20.1	MX	2.1 ma	5	5	+S	−S
SCA13	+S Tape Level 3	MX, CD	I	01.83.20.1	MX	2.1 ma	5	5	+S	−S
SCA14	+S Tape Level 4	MX, CD	I	01.83.20.1	MX	2.1 ma	5	5	+S	−S
SCA15	+S Tape Level 5	MX, CD	I	01.83.20.1	MX	2.1 ma	5	5	+S	−S
SCA16	+S Tape Level 6	MX, CD	I	01.83.20.1	MX	2.1 ma	5	5	+S	−S
SCA17	+S Tape Level 7	2 MX	I	01.83.20.1	MX	2.1 ma	5	5	+S	−S
SCA18	+S Tape Level 8	MX	I	01.83.20.1	MX	1.05 ma	5	5	+S	−S
SCA19	+S Tape Sync Exit	CD	I	01.80.30.1	PK	1.05 ma	5	5	+S	−S
SCA20	+S Nonprocess Runout	CD	I	01.83.10.1	Int	1.05 ma	see Text, SC20		+S	−S
SCA21	+S Clutch Drive	MX	O	01.83.10.1	PG	see text, SC21	see Text, SC21		+S	−S
SCA22	−S RDR Rdy	MH, MX	I	01.83.10.1	MX	4.3 ma	see Text, SC22		−S	+S

Current Required is the current supplied or required for operation

CD	CTRL Inverter
I/O	Refers to lines "In" to the 1620 or "Out" of the 1620
Int	Integrator
MH	CTRL Power Inverter
MX	CTRL Power Inverter, two-way
PG	Clutch Control
PK	Photosense Amplifier
SC	Shoe Connector
+S	0 v (ground level)
−S	−5.56 v to −12 v, depending on the loading

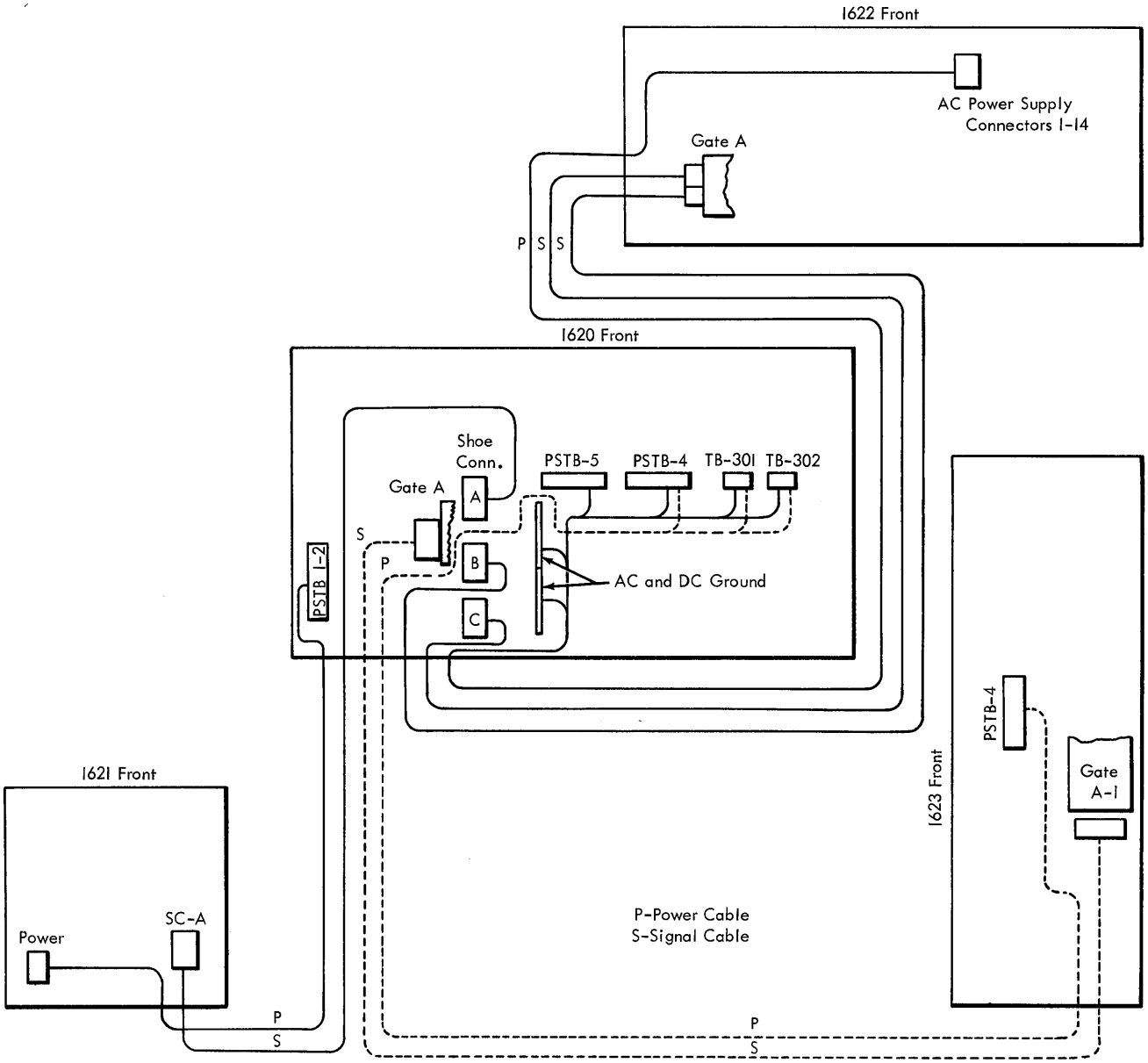


Figure 6. IBM 1620 Cable Connectors

SC 11-18. All are +S data lines from the paper tape reader. The pulse length is 2 ms minimum and 6.5 ms maximum.

SC 11-17. These lines control the 1620 input translator circuit. A combination of the lines defines the character being entered. There must be an odd number to satisfy parity. If Tape Level lines 1 through 7 are +S. the response is blocked, and information cannot be entered.

SC 11 +S Tape Level 1. 1-bit input line.

SC 12 +S Tape Level. 2-bit input line.

SC 13 +S Tape Level 3. 4-bit input line.

SC 14 +S Tape Level 4. 8-bit input line.

SC 15 +S Tape Level 5. C-bit input line.

SC 16 +S Tape Level 6. O-bit input line.

SC 17 +S Tape Level 7. X-bit input line.

SC 18 +S Tape Level 8. This is the input end-of-line (EL) signal. It is used to signal the end of the input data and to terminate the read operation.

SC 19-22. All these are +S level control lines.

SC 19 +S Tape Sync Exit. This line determines the response time on a read paper tape. The pulse must end in the center of the data information pulses. Figure 7 shows the nominal timing involved. SC 11-18 illus-

trate the worse case timing of the data lines, that is, the last line to go plus and the first line to go minus. This condition can be scoped at DIDI4E, System Diagram 01.80.30.1. The level will be inverted. With a suitable tape being read and DIDI4E displayed on the scope, SC 19 Tape Sync should be observed to end in the center of the observed pulse.

SC 20 +S Nonprocess Runout. The nonprocess runout line is switch-operated and has no timing. It blocks the reader data gate which prevents data from entering the machine and conditions the clutch drive SC 21 until the reader ready line SC 22 goes plus.

SC 21 +S Clutch Drive. This line will be +S as long as the following conditions exist in the 1620:

1. Select 3
2. Read call
3. Clock on or Run

The line provides 3.5 ma output current at −5.65 v.

SC 22 +S Reader Ready. The reader ready line signals a tape ready condition. When it is not satisfied it will be −S. It is used to turn off:

1. The Run trigger
2. Nonprocess Runout trigger

and to turn on

3. The Reader No-Feed light

It is generally a steady-state condition. When it changes status, it has no timing.

Lines to the 1622 Card Read Punch

Circuits to operate and control a 1622 Card Read Punch are contained in the 1620. Information concerning the interconnecting lines is provided in the following pages. This information is given in terms of how the 1620 accepts and receives data and control signals. A summary of the characteristics of these connecting lines appears in Table 3. The shoe connectors SCC02 through SCC32 and SCB26 connect the 1620 and the card reader. Connectors SCB02 through SCB 30 (except SCB26) connect the 1620 and the card punch. The following comments apply to the SCC and SCB connectors listed in Table 3.

CONNECTIONS WITH THE CARD READER

SCC02, 04, 06, 08, 10, 12, and 14 Read C, A, B, 8, 4, 2, 1. Signals from the 1622 output register are transmitted to the 1620 input translator by way of these lines.

SCC16 Cd Rd Bff Rdy. The signal on this line indicates that a card has been fed past the second read brushes and that the 1622 read buffer storage has been loaded and checked and is ready to be transmitted to the 1620.

SCC18 Cd Rd Sync. The card read sync signal is used:

1. To indicate that the 1622 clock has started and that the 1622 output register has been loaded from the read buffer.
2. To provide a signal to the 1620 so that the 1622 output register can be gated to the system as required.

SCC20 Cd Rd Data Gate. A signal to the 1622 on this line serves two purposes:

1. The Cd Read Data Gate initiates the transfer of the first 80 characters after this signal interrogates the 1622 circuits to see if the punching of a row of data is in progress. The start of the transfer is delayed until after punching of the row is completed.
2. The signal also gates the transfer of characters from the 1622 output register to the 1620.

SCC22 Set MDR SAM I/O. A Set Memory Data Register (MDR) Sample I/O signal on this line starts the 1622 clock to initiate the transfer to the 1620 of the second and all subsequent characters.

SCC24 Last Card. The Last Card signal from the 1622 indicates that data from the last card (no more cards in read feed) has been transferred to the 1620.

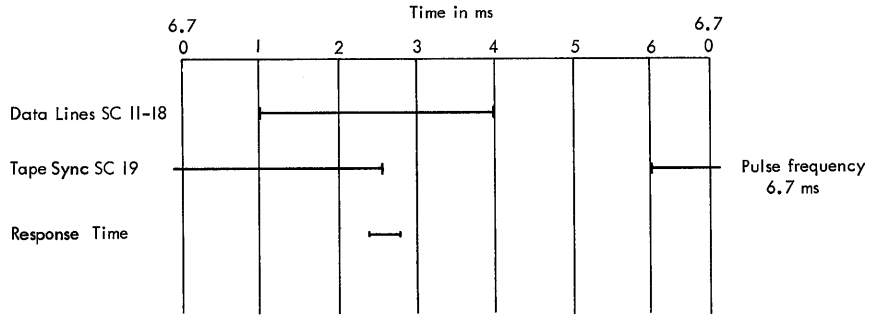


Figure 7. 1621 Data Read Sequence

Table 3—1620 Connections from the 1622

1620 Shoe Connector	Title*	1620 Card Type	I/O	1620 System Diagram	1622 Card Type	Pulse Length	Frequency per Input/Output Card
SCC02**	–C 1622 C Bit	DEE	I	01.81.15.1	DED	38 μsec	Any one line can have as many as 80 pulses, one every 40 μsec, if data being transmitted requires them.
SCC04	–C 1622 0 Bit	DEE	I	01.81.15.1	DED	38 μsec	
SCC06	–C 1622 X Bit	DEE	I	01.81.15.1	DED	38 μsec	
SCC08	–C 1622 8 Bit	DEE	I	01.81.15.2	DED	38 μsec	
SCC10	–C 1622 4 Bit	DEE	I	01.81.15.2	DED	38 μsec	
SCC12	–C 1622 2 Bit	DEE	I	01.81.15.3	DED	38 μsec	
SCC14	–C 1622 1 Bit	DEE	I	01.81.14.3	DED	38 μsec	
SCC16	–C Cd Rd Bff Rdy	DEE	I	01.80.30.1	DED	3.3 ms (A)	Once per card
SCC18	–C Cd Rd Sync	DEE	I	01.80.30.1	DED	8 μsec	80 pulses, one every 40 μsec
SCC20	–C Cd Rd Data Gate	DED	O	01.80.30.1	DEE	3.3 ms	Once per card
SCC22	–C Set MDR Sam I/O	DED	O	01.81.15.1	DEE	3 μsec	80 pulses, one every 40 μsec
SCC24	–C Last Rd Card	DEE	I	01.80.05.1	DED	(B)	——
SCC26	–C Cd Rd Disconnect	DEE	I	01.80.20.1	DED	20 μsec	Once per card
SCC28	–C Rd Chk Trg Off	DED	O	01.81.45.1	DEE	(C)	——
SCC30	–C Run Trg Off Manual	DED	O	01.80.10.1	DEE	Manual	——
SCC32	–C Cd Rd Load	DEE	I	01.80.10.1	DED	(D)	——
SCB02	–C 1620 C Bit (Punch C)	DED	O	01.82.20.2	DEE	25 μsec	Any one line can have as many as 80 pulses, one every 40 μsec, if data being transmitted requires them.
SCB04	–C 1620 A Bit (Punch 0)	DED	O	01.82.20.2	DEE	25 μsec	
SCB06	–C 1620 B Bit (Punch X)	DED	O	01.82.20.1	DEE	25 μsec	
SCB08	–C 1620 8 Bit (Punch 8)	DED	O	01.82.20.3	DEE	25 μsec	
SCB10	–C 1620 4 Bit (Punch 4)	DED	O	01.82.52.1	DEE	25 μsec	
SCB12	–C 1620 2 Bit (Punch 2)	DED	O	01.82.52.1	DEE	25 μsec	
SCB14	–C 1620 1 Bit (Punch 1)	DED	O	01.82.52.1	DEE	25 μsec	
SCB16	–C Cd Pch Disconnect	DEE	I	01.80.20.1	DED	10 μsec	Once per card
SCB18	–C Cd Pch Sync	DEE	I	01.80.20.1	DED	8 μsec	80 pulses, one every 40 μsec
SCB20	–C Cd Pch Bff Rdy	DEE	I	01.80.20.1	DED	3.3 ms (A)	Once per card
SCB22	–C Cd Pch Data Gate	DED	O	01.80.20.1	DEE	3.3 ms	Once per card
SCB24	–C Set I/O Sam MDR	DED	O	01.80.20.1	DEE	6 μsec	80 pulses, one every 40 μsec
SCB26	–C I/O Exit Trg	DED	O	01.81.15.1	DEE	20 μsec	Once per card
SCB28	–C WR Chk Trg Off	DED	O	01.81.45.1	DEE	(C)	——
SCB30	–C Manual Reset	DED	O	01.80.05.1	DEE	Manual	——

*All signal levels (–C) are –2.0 v nominal (+C is nominally +1.5 v); no signal levels are at ground. The current required on each line is 15.5 ma. No restrictions are imposed on signal rise and fall times.

**The TW (twisted pair) wire associated with each signal wire is connected to the odd-numbered terminal immediately preceding the signal connector, i.e., SCC01 in the case of the 1622 C-bit signal.

(A) Assume continuous card feeding
(B) Last read card only
(C) Occurs during error only
(D) During load operation only

SCC26 Cd Rd Disconnect. After the complete buffer contents have been transferred to the 1620, the Cd Rd Disconnect signal from the 1622 initiates a disconnect of the 1620 from the 1622. The 1620 can then continue its sequence of operations. If no error has been detected in the 1620, a Rd Chk Trg Off signal is returned to the 1622 and the 1622 read clutch magnet is energized to initiate a read card-feed cycle. This refills the buffer.

SCC28 Rd Chk Trg Off. Lack of a signal on this line indicates that a test of the data lines in the 1620 System has detected a read error. The feeding of the next card is prevented and the erroneous data remains in the 1622 read buffer.

SCC30 Run Trg Off Manual. A signal on this line indicates that the 1620 is in the manual mode, that is, the system is not running. The Run Trg Off Manual signal is used with the Load key operation.

SCC32 Cd Rd Load. Depression of the Load key on the 1622 causes the feeding of three cards from the hopper. The contents of the first card enter the read buffer. The Cd Rd Load signal is returned to the system to indicate that the contents of the first card are ready to be used in loading. See *Manual of Instruction,* 1620 *Additional Features,* Form 227-5513.

SCB26 I/O Exit Trg. This signal from the 1620 turns off the disconnect control latches in the 1622. The signal occurs at the end of a read operation.

CONNECTIONS WITH THE CARD PUNCH

SCB02, 04, 06, 08, 10, 12, 14, Punch C, A, B, 8, 4, 2, 1. Signals from the 1620 output data lines are placed on these lines for transfer to the 1622 input register and from there, to the 1622 punch buffer.

SCB 16 Cd Pch Disconnect. A Cd Pch Disconnect signal to the 1620 initiates a disconnect of the 1620 from the 1622. The system can then continue its sequence of operations. If no error has been detected in the 1620 during data transfer, a punch card feed cycle occurs. See SCB28 Wr Chk Trg Off.

SCB18 Cd Pch Sync. The Cd Pch Sync signal from the 1622 initiates a 1620 output cycle which puts a BCD character on the output lines to the 1622 (see SCB02-14).

SCB20 Cd Pch Bff Rdy. A signal on this line indicates to the 1620 System that the punch buffer is ready to receive new data.

SCB22 Cd Pch Data Gate. A signal on this line interrogates the 1622 circuits to see if the reading of a row of holes in the card is in progress. If the reading of a row has not been completed, the back signal is delayed until the row is read. When the reading of the row is completed, a Cd Pch Sync signal SCB18 is returned to the system to initiate an output cycle in which the first digit is transferred to the 1622.

SCB24 Set I/O SAM MDR. The Set I/O SAM MDR signal to the 1622 initiates the transfer of the second and all remaining (78) characters from the 1620 to the 1622.

SCB28 Wr Chk Trg Off. Lack of this signal indicates that a test of the 1620 output data lines determined that a write error occurred. Feeding and punching of the next card is prevented and the erroneous data remains in the 1622 buffer.

SCB30 Manual Reset. A signal on this line indicates that the 1620 is in a reset operation. This may be due to a manual reset, a power on reset, or a power off reset. All latches in the 1622 are reset except for the error latches.

Lines to the 1623 Core Storage Unit

Information concerning the lines that interconnect the 1620 and the 1623 is contained in the following material. The information is given in terms of how the 1620 accepts and receives data and control signals from the 1623. A summary of the characteristics of the 1620 data and control lines to the 1623 is given in Table 4. The following comments apply to the shoe connector lines listed in Table 4.

AXF06 to AXG04 MAR Bit Lines. These are 1620 Memory Address Register (MAR) trigger output lines to decode switches in the 1623.

AXG06 and AXG08 Odd SA Gate and Even SA Gate. These two lines control the memory sense amplifiers in the 1623 for the readout of the odd-addressed digit, or even-addressed digit or both.

AXG10 < 50. The < 50 signal gates the 1623 presense amplifier, for addresses less than 50, into the sense amplifier. The < 50 signal is inverted in the 1623 to gate the 1623 presense amplifier for addresses greater than 50.

AXG12 and AXG14 Write OD Gate and Write EV Gate. These signals gate the Memory Data Register (MDR) on an I/O device into the 1623 MBR-Odd register or MBR-Even register or both.

AXG16 I/O Rd Gate. The I/O Rd Gate switches the I/O alpha zone digit into MBR-Even.

AXG18 to AXG24 Gate Mem Sam 40K, 60K. These are pulses for timing the 1623 tens and thousands read and write current drivers. The signals are controlled by the ten thousands position of the memory address register in the 1620.

AXG26 R1D4. This is a timing pulse for the 1623 hundreds read current driver.

AXG28 R1D2. The R1D2 signal switches with the < 50 gate to time the sense amplifier strobe.

AXG30 R0D4. This is a timing pulse for the units read current driver.

AXG32 Wr Mem W0-D5. This signal gates the inhibit driver.

AXH02 Set R2-D1. The Set R2-D1 signal is a timing pulse for the Write OD gate and the Write EV gate.

AXH06 MBR Reset. This signal controls the reset of the MBR-Odd and MBR-Even C, 8, 4, 2, and 1 bit triggers.

AXH08 MBR Reset F. This signal controls the reset of MBR-Odd and MBR-Even F-bit triggers.

AXH10 Gate MBR C. This impulse to the 1623 gates the C-bit transfer from the memory data register to the memory buffer register (MBR) in the 1623.

AXH12 to AXH18 MDR ___ Bit. These impulses to the 1623 are the outputs of the MDR bit triggers in the 1623 memory buffer register.

AXH20 Gate MBR F. This gates the F-bit transfer from MDR to MBR.

AXH22 to AXH28 Rd ___ Zone. These lines are the input translator zone bit output to MBR-Even in the 1623.

AXJ02 to AXJ12 MBR Not ___ Bit OD. These are input lines to the 1620 MBR-Odd register from the 1623 MBR-Odd.

AXJ14 to AXJ24 MBR Not ___ Bit EV. These are input lines to the 1620 MBR-Even register from the 1623 MBR-Even.

Table 4—1620 Connections from the 1623

1620 Shoe Connector	Title	1620 Card Type	I/O	1620 System Diagram	1623 Card Type	Pulse Length μsec
AXF06*	−C MAR 1 Bit 10 Thous	DBU	O	01.41.04.1	TDA	18
AXF08	−C MAR 2 Bit Units	DBU	O	01.41.04.1	TDA	18
AXF10	−C MAR 4 Bit Units	DBU	O	01.41.04.1	TDA	18
AFX12	−C MAR 8 Bit Units	DBU	O	01.41.04.1	TDA	18
AXF14	−C MAR 1 Bit Tens	DBU	O	01.41.04.1	TDA	18
AXF16	−C MAR 2 Bit Tens	DBU	O	01.41.04.1	TDA	18
AXF18	−C MAR 4 Bit Tens	DBU	O	01.41.04.1	TDA	18
AXF20	−C MAR 8 Bit Tens	DBU	O	01.41.04.1	TDA	18
AXF22	−C MAR 1 Bit Hund	DBU	O	01.41.04.1	TDA	18
AXF24	−C MAR 2 Bit Hund	DBU	O	01.41.04.1	TDA	18
AXF26	−C MAR 4 Bit Hund	DBU	O	01.41.04.1	TDA	18
AXF28	−C MAR 8 Bit Hund	DBU	O	01.41.04.1	TDA	18
AXF30	−C MAR 1 Bit Thous	DBU	O	01.41.04.1	TDA	18
AXF32	−C MAR 2 Bit Thous	DBU	O	01.41.04.1	TDA	18
AXG02	−C MAR 4 Bit Thous	DBU	O	01.41.04.1	TDA	18
AXG04	−C MAR 8 Bit Thous	DBU	O	01.41.04.1	TDA	18
AXG06	+C Odd SA Gate	DBU	O	01.41.06.1	TDA	(A)
AXG08	+C Even SA Gate	DBU	O	01.41.06.1	TDA	(A)
AXG10	−C <50	DBU	O	01.41.06.1	TDA	(B)
AXG12	−C Write OD Gate	DBU	O	01.41.06.1	TDA	(B)
AXG14	−C Write EV Gate	DBU	O	01.41.06.1	TDA	(B)
AXG16	−C I/O Rd Gate	DBU	O	01.41.06.1	TDA	(C)
AXG18	−C Gate Mem Sam 40K TN R0-D8	DBU	O	01.41.03.1	TDA	8
AXG20	−C Gate Mem Sam 60K TN R0-D8	DBU	O	01.41.03.1	TDA	8
AXG22	−C Gate Mem Sam 40K Thous R1-D7	DBU	O	01.41.03.1	TDA	7
AXG24	−C Gate Mem Sam 60K Thous R1-D7	DBU	O	01.41.03.1	TDA	7
AXG26	+C R1-D4	DBU	O	01.41.03.1	TDA	4
AXG28	−C R1-D2	DBU	O	01.41.03.1	TDA	2
AXG30	+C R0-D4	DBU	O	01.41.03.1	TDA	4
AXG32	−C WR Mem W0-D5	DBU	O	01.41.03.1	TDA	5
AXH02	+C Set R2-D1	DBU	O	01.41.03.1	TDA	1
AXH04						
AXH06	−C MBR Reset	DBU	O	01.41.05.1	TDA	3
AXH08	−C MBR Reset F	DBU	O	01.41.05.1	TDA	3
AXH10	−C Gate MBR C	DBU	O	01.41.15.1	TDA	(A)
AXH12	+C MDR 8 Bit	DBU	O	01.41.15.1	TDA	15
AXH14	+C MDR 4 Bit	DBU	O	01.41.15.1	TDA	15
AXH16	+C MDR 2 Bit	DBU	O	01.41.15.1	TDA	15
AXH18	+C MDR 1 Bit	DBU	O	01.41.15.1	TDA	15
AXH20	−C Gate MBR F	DBU	O	01.41.15.1	TDA	(A)
AXH22	+C Rd C Zone	DBU	O	01.41.16.1	TDA	2
AXH24	+C Rd 1 Zone	DBU	O	01.41.16.1	TDA	2
AXH26	+C Rd 2 Zone	DBU	O	01.41.16.1	TDA	2
AXH28	+C Rd 4 Zone	DBU	O	01.41.16.1	TDA	2
AXJ02	−C MBR Not C Bit OD	TDA	I	01.41.07.1	TAB	18
AXJ04	−C MBR Not F Bit OD	TDA	I	01.41.07.1	TAB	18
AXJ06	−C MBR Not 8 Bit OD	TDA	I	01.41.07.1	TAB	18
AXJ08	−C MBR Not 4 Bit OD	TDA	I	01.41.07.1	TAB	18
AXJ10	−C MBR Not 2 Bit OD	TDA	I	01.41.07.1	TAB	18
AXJ12	−C MBR Not 1 Bit OD	TDA	I	01.41.07.1	TAB	18
AXJ14	−C MBR Not C Bit EV	TDA	I	01.41.17.1	TAB	18
AXJ16	−C MBR Not F Bit EV	TDA	I	01.41.17.1	TAB	18
AXJ18	−C MBR Not 8 Bit EV	TDA	I	01.41.17.1	TAB	18
AXJ20	−C MBR Not 4 Bit EV	TDA	I	01.41.17.1	TAB	18
AXJ22	−C MBR Not 2 Bit EV	TDA	I	01.41.17.1	TAB	18
AXJ24	−C MBR Not 1 Bit EV	TDA	I	01.41.17.1	TAB	18
AXJ26	+C CE SW3 CF8 T	DBU	O	01.41.01.1	TDA	(D)
AXJ28	−C CE SW5 CF8 C	DBU	O	01.41.01.1	TDA	(D)
AXJ30	+C CE SW4 421 T	DBU	O	01.41.01.1	TDA	(D)
AXJ32	−C CE SW6 421 C	DBU	O	01.41.01.1	TDA	(D)

*The TW (twisted pair) wire associated with each signal wire is connected to the odd-numbered terminal immediately preceding the signal connector, i.e., AXF05 in the case of the MAR 1-bit 10 Thous signal.

+C Nominally +1.5 v.

−C Nominally −2.5 v.

(A) This pulse must be long enough to gate set pulses (MBR-MDR)—approximately 4 μsec.

(B) This pulse must be long enough to gate write pulse (W1-D2)—approximately 3 μsec.

(C) This pulse must be long enough to gate (R1-D4)—approximately 4 μsec.

(D) Manual control.

AXJ26 to AXJ32 CE Sw 3, 4, 5, 6. These lines enable the customer engineer to control MBR inhibit lines for servicing.

Lines to the 1624 Paper Tape Punch

The following material contains information concerning the lines that interconnect the 1620 and the 1624. The information is given in terms of how the 1620 accepts and receives data and control signals. Characteristics of the 1620 output data and control lines to the 1624 are summarized in Table 5. The timing sequence for output data is shown in Figure 8. The following comments apply to the shoe connector lines listed in Table 5 and in System Diagram 00.00.20.0.

SC 1-10. These lines are all thyratron output lines. They are used to energize magnets in the 1624 Paper Tape Punch. The thyratron circuit is conditioned by the 1620 but must have its collector circuit completed as follows: from the collector of the thyratron, through the cable to the 1624, through the punch magnet, through a circuit breaker, and back to the 1620 to the +48-v supply at terminal PSTB 1-8. The circuit breaker is necessary because the thyratron does not extinguish unless the collector circuit is opened. The thyratron must be protected from the inverse voltage caused by the collapse of an inductive load. The output current is a maximum of 300 ma, a minimum of 20 ma. The minimum current requirement is necessary to keep the thyratron in conduction after it has been turned on. The output must be under control of a circuit breaker.

SC 1 Punch EL. An end-of-line punch in the tape (EL) is used to signify an end of record. It is punched at the end of a Write Call, Select 2 operation.

SC 2-8 Data Lines. Signals on combinations of these lines define the bit configuration of the characters to be punched.

SC 9 Punch Feed. The Punch Feed signal causes the clutch in the 1624 Paper Tape Punch to be tripped. This results in the punching of the bit configuration set up by the data lines. To energize the clutch, the 1620 must provide these conditions:

1. Select 2
2. Write Call
3. Run

SC 10 Punch No-Feed. This line is used to prevent spacing of the paper tape. It is under control of the write check circuitry and the tape tension contact.

SC 23-28. These lines are control lines and all are input lines to the 1620 to establish the sequence of operations. The lines are driven by integrators (rise time 5 ms).

SC 23 –S Tape Tension Cont. This line indicates tape is loaded in the 1624 and will feed. The line is usually at a –S level in operating condition. It exerts control

Table 5–1620 Connections from the 1624 (via the 1621)

1620 Shoe Connector	Title	1620 Card Type	I/O	1620 System Diagram	1621 Card Type	Current Required	Rise Time μsec	Fall Time μsec	Signal Level (in volts) On	Signal Level (in volts) Off
SCA01	Punch EL	NP	O	01.84.20.1	R		65	10	0	+48
SCA02	Punch C Bit	NP	O	01.84.20.1	R		65	10	0	+48
SCA03	Punch X Bit	NP	O	01.84.20.1	R		65	10	0	+48
SCA04	Punch 0 Bit	NP	O	01.84.20.1	R	see Text, SC1-10.	65	10	0	+48
SCA05	Punch 8 Bit	NP	O	01.84.20.1	R		65	10	0	+48
SCA06	Punch 4 Bit	NP	O	01.84.20.1	R		65	10	0	+48
SCA07	Punch 2 Bit	NP	O	01.84.20.1	R		65	10	0	+48
SCA08	Punch 1 Bit	NP	O	01.84.20.1	R		65	10	0	+48
SCA09	Punch Feed	NP	O	01.84.10.1	R		65	10	0	+48
SCA10	Punch No-Feed	NP	O	01.84.10.1	R		65	10	0	+48
SCA23	–S Tape Tension Cont	MX	I	01.84.10.1	Int	1.05 ma	see Text, SC23		–S	+S
SCA24	+S P3 Resp	MX	I	01.80.30.1	Int	3.15 ma			+S	–S
SCA25	+S Punch Check	MX	I	01.81.45.1	Int	1.05 ma			+S	–S
SCA27	+S Tape Feed	MX	I	01.84.10.1	Int	1.05 ma			+S	–S
SCA28	+S PCB 1	MX	I	01.80.30.1	Int	1.05 ma			+S	–S

Current Required is the current supplied or required for operation.

I/O	Refers to lines "In" to the 1620 or "Out" of the 1620.	R	Punch Magnet Coil in 1624
Int	Integrator	SC	Shoe Connector
MX	CTRL Power Inverter, two-way	+S	–0 v or ground level
NP	Thyratron Card	–S	–5.56 v to –12 v, depending on the loading

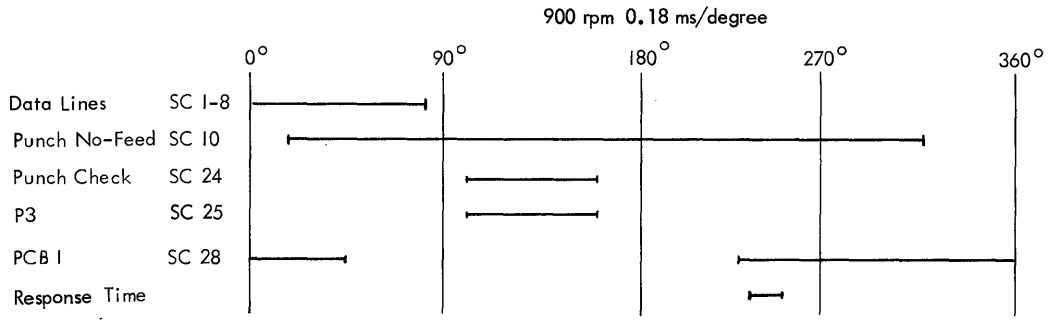


Figure 8. Punch Sequence

over punch no-feed and punch go circuitry when it goes to +S. It also turns the run trigger off under this condition.

SC24 +S P3 Resp (PCB 3). The P3 response line sets the P3 interlock trigger on. This act begins the response operation. When the P3 Interlock trigger is turned off by PCB 1, the response is generated. Response pulse frequency is 64.8 ms. Refer to Figure 8 for timing and pulse length. At PCB 3 time, punching is completed but the punches are still through the tape. The ball check contacts are set up and the punch check signal is generated (+S, if there is an error).

SC 25 +S Punch Check. See SC 24.

SC 26 Not used.

SC 27 +S Tape Feed. The tape feed line from the 1624 is controlled by a manually operated switch. It has no timing. A +S Tape Feed controls the following:

1. Punch data lines (SC 2-8)
2. Punch Feed (SC 9)
3. Punch No-Feed (SC 10)

and turns off the

4. Punch No-Feed light

SC 28 +S PCB 1. See SC 24.

Power Supplies

The power supply connections from the 1620 to other machines in the System (1622, 1623, and 1624) are shown on System Diagram 01.90.32.1. Power connectors labelled 02.XX.XX.1 go to the 1621, connectors labelled 03.XX.XX.1 to the 1623, and connectors labelled 04.XX.XX.1 to the 1622.

IBM 1621 Paper Tape Reader

This section provides data for the use of non-IBM engineers who wish to attach the 1621 Paper Tape Reader to their equipment. Easy access to supplemental tie-in data not so readily available in other IBM publications is provided.

Detailed theory and mechanical principles of operation are not included. These may be found in the following IBM publications relating to the 1621.

Title			*Form*
IBM	1620	*CE Manual of Instruction*	227-5507
IBM	1620	*CE Reference Manual*	227-5500
IBM	1620	*Data Processing System Reference Manual*	A26-4500

Additional engineering information can be obtained from system diagrams and other available engineering documents.

General Description

The IBM 1621 Paper Tape Reader reads 8-channel paper tape at the rate of 150 characters per second. Functionally, the reader has mechanisms for reading, driving the tape past the read head, and turning the tape reels. The read head assembly contains eight photocells to sense the light that passes through the punched holes as the tape moves over the read head. The photocell outputs are amplified and supplied to the system.

Figure 9 shows a section of the paper tape illustrating the eight channels and the coded punching for alphabetic, numerical and special characters. The EL (end-of-line) channel of the tape signals the end of data transmission to or from the tape. When the reader senses a column with an EL hole, a record mark (C, 8, 2 bits) is placed in memory and the read operation is ended. The C bit is used to preserve the odd parity code for checking purposes within the system. Whenever the basic character code consists of an even number of holes, a C bit is added to force an odd number of holes into each character column.

Keys and Lights

The following keys and lights are used in the operation of the 1621.

Power Switch. With this switch on, all necessary power for operation of the 1621 is supplied by the system.

Reel/Strip Switch. In reel mode, tape is fed from the supply reel and to the left, onto the takeup reel. In strip mode, short pieces of tape may be read without reel operation.

Reel Power Key. Depression of this key operates the supply and takeup reels to position the paper tape for reading and causes the Ready light to come on. This places the machine in ready status.

Nonprocess Runout Key. Depression of this key causes paper tape to feed. Ready status is terminated and all data transfer is blocked until all paper tape has passed. The paper tape reel must be reloaded and the reel Power key depressed before the machine can be returned to ready status.

Power On Light. This light when on indicates that power is supplied from the system.

Lines to the 1621 Paper Tape Reader

The using system must contain circuits to operate and control the 1621 Paper Tape Reader. The following material provides information on the lines that interconnect the system and the 1621. This information is given in terms of how the 1621 accepts and receives

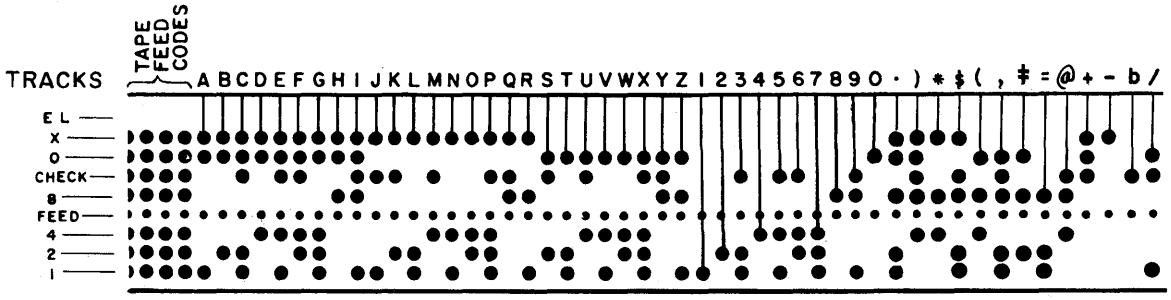


Figure 9. Paper Tape Tracks and Codes

Table 6. 1621 Connections from the 1620

1621 Shoe Connector	Title	1621 Card Type	I/O	1621 System Diagram	1620 Card Type	Current Required	Rise Time (μsec)	Fall Time (μsec)
SCA 11	+S Tape Level 1	MX	O	02.83.50.1	MX, CD	2.1 ma	5	5
SCA 12	+S Tape Level 2	MX	O	02.83.50.1	MX, CD	2.1 ma	5	5
SCA 13	+S Tape Level 3	MX	O	02.83.50.1	MX, CD	2.1 ma	5	5
SCA 14	+S Tape Level 4	MX	O	02.83.50.1	MX, CD	2.1 ma	5	5
SCA 15	+S Tape Level 5	MX	O	02.83.50.1	MX, CD	2.1 ma	5	5
SCA 16	+S Tape Level 6	MX	O	02.83.50.1	MX, CD	2.1 ma	5	5
SCA 17	+S Tape Level 7	MX	O	02.83.50.1	2 MX	2.1 ma	5	5
SCA 18	+S Tape Level 8	MX	O	02.83.50.1	MX	1.05 ma	5	5
SCA 19	+S Tape Sync Exit	PK	O	02.83.50.1	CD	1.05 ma	5	5
SCA 20	+S Nonprocess Runout	Int	O	02.83.60.1	CD	1.05 ma	see Text, SC20	
SCA 21	+S Clutch Drive	PG	I	02.83.60.1	MX	see Text, SC21	see Text, SC21	
SCA 22	−S RDR Rdy	MX	O	02.83.60.1	MH, 2 MX, CD	4.3 ma	see Text, SC22	

Card type is type of card driving the line or being driven.
Current Required is the current supplied or required for operation.

CD CTRL Inverter
I/O Refers to lines "In" to the 1621 or "Out" of the 1621.
Int Integrator
MH CTRL Power Inverter
MX CTRL Power Inverter, two-way
PG Clutch Control
PK Photosense Amplifier
SC Shoe Connector
+S 0 v (ground level)
−S 5.56 v to −12 v, depending on the loading

data and control signals. Characteristics of the 1621 output data and control lines are summarized in Table 6. The timing sequence for reader output is shown in Figure 10. The following comments apply to the shoe connector lines (SC) listed in Table 6 and in System Diagram 00.00.20.0.

SC 11-18. These are all +S Data Lines from the paper tape reader. The pulse length is 2 ms minimum and 6.5 ms maximum.

SC 11-17. These lines control the system input translator circuits. A combination of the lines defines the character being entered. There must be an odd number to satisfy parity. If all of the Tape Level lines are +S, the response is blocked, and information cannot be entered.

The following are lines "Out" of the 1621.

SC 11 +S Tape Level 1. 1-bit line.
SC 12 +S Tape Level 2. 2-bit line.
SC 13 +S Tape Level 3. 4-bit line.
SC 14 +S Tape Level 4. 8-bit line.
SC 15 +S Tape Level 5. C-bit line.
SC 16 +S Tape Level 6. 0-bit line.
SC 17 +S Tape Level 7. X-bit line.
SC 18 +S Tape Level 8. This is the end-of-line (EL) signal. It is used to signal the end of the input data and to terminate the read operation.

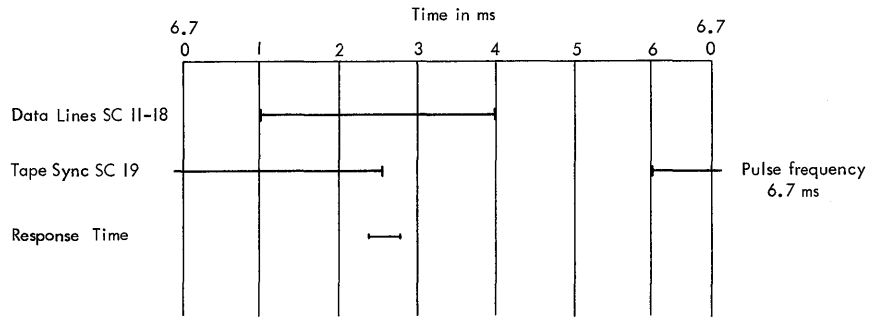


Figure 10. 1621 Data Read Sequence

SC 19-22. These are all S-level control lines.

SC 19 +S Tape Sync Exit. This line determines the response time on a read paper tape. The pulse must end in the center of the data information pulses. Figure 10 shows the nominal timing involved. SC 11-18 are illustrated as the worse case timing of the data lines, i.e., the last line to go plus and the first line to go minus. This condition can be scoped at DIDI4E, System Diagram 01.80.30.1. The level will be inverted. With a suitable tape being read and DIDI4E displayed on the scope, SC 19 Tape Sync will be observed to end in the center of the worse case data line pulse.

SC 20 +S Nonprocess Runout. The Nonprocess Runout line is switch-operated and has no timing. It blocks the reader data gate. This prevents data from entering the system processing unit and conditions the clutch drive SC 21 until the reader ready line SC 22 goes plus.

SC 21 +S Clutch Drive. This line will be +S as long as the following 1620 conditions are satisfied,

1. Select 3
2. Read Call
3. Clock on or Run

and will provide 3.5 ma output current at –5.65 v (see 1620 System Diagram 01.83.10.1).

SC 22 +S Reader Ready. The reader ready line reflects a tape ready condition. When it is not satisfied, it is at –S. The –S signal is used to turn off the Run trigger and Nonprocess Runout trigger and to turn on the Reader No-Feed light in the 1620. It is generally a steady-state condition. When it changes status, it has no timing.

This manual provides data to satisfy the special needs of non-IBM engineers who wish to attach the IBM 1622 Card Read Punch to their equipment. It provides easy access to supplemental tie-in data not so readily available in other IBM publications.

Detailed theory and mechanical principles of operation are not included. These may be found in the following IBM publications relating to the 1622.

Title	*Form*
IBM 1620 *CE Manual of Instruction — Additional Features*	227-5513
IBM 1620 *CE References Manual Additional Features*	227-5540

Additional engineering information can be obtained from system diagrams and other available engineering documents.

General Description

The IBM 1622 Card Read Punch is a solid-state electronic and mechanical unit used to provide a punched card input and output for a data processing system. The read feed operates at a speed of 250 cards per minute. The punch operates at 125 cards per minute. The read and punch feeds are separate and functionally independent, with individual switches, lights, checking circuits, buffer storage, and instruction codes. Reading, punching, and processing may occur simultaneously because the reader and punch have separate buffer storage.

Viewed from the front of the machine, the read feed is at the right side of the unit and the punch feed at the left side with five radial stackers between the two (see Figure 11). The two right-hand stackers are used for normal and selected read cards, the two left-hand stackers are used for normal and selected punch cards. The center stacker is not used. IBM card code data read by the 1622 Read Unit is converted to 7-bit Binary-Coded-Decimal form (C, A, B, 8, 4, 2, 1), is stored in the 1622 read buffer, and is transmitted to the using system in the same 7-bit BCD form. Data is accepted by the 1622 punch buffer in 7-bit BCD form. The punch buffer data is subsequently converted to IBM card code for punching into cards by the 1622 Punch.

The card reader feeds cards 9-edge first, face down, past two reading stations, check and read (see Figure 11). Input buffer storage is initially loaded with 80 columns of card data during the Start key or Load key run-in operation. Thereafter, each card feed cycle is under control of the using system.

The card punch feeds cards 12-edge first, face down, up to the punch station during the Start key operation (see Figure 11). Thereafter, each card punch cycle is under control of the external system.

Switches, Keys, and Indicator Lights

Switches, keys, and indicator lights are mounted on a single panel above the stackers (see Figure 12). The card reader and card punch have separate power switches, start keys, stop keys, nonprocess runout keys, and ready lights. In addition, the card reader has a Reader Ready light, Reader Check light, and a Load key. The card punch has a Punch Ready light, Punch Check light, Select Stop and Select Nonstop switch, and a Check Reset key. The Stacker, Thermal, Fuse, and Transport lights are common to both the read and punch feeds.

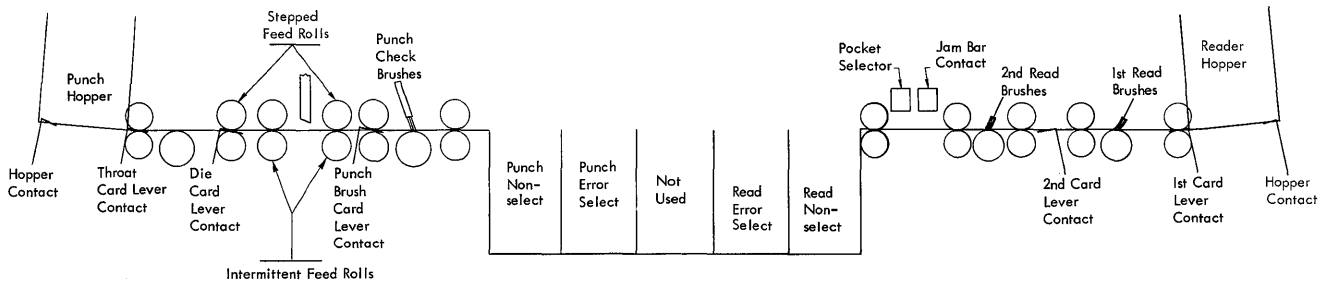


Figure 11. 1622 Feed Schematic

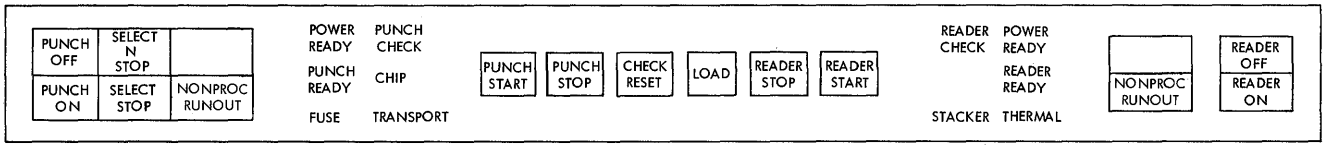


Figure 12. Switch, Key, and Indicator Light Panel

CARD READER CONTROLS

Reader On/Off Switch. This switch is active after the power in the external system comes on. It provides power to the reader circuits and turns on the Reader Power Ready light.

Reader Start Key. This key is used to feed cards on initial run-in (three feed cycles), to set up a reader ready status and to turn on the Reader Ready light. The Start key restores the reader to the ready status after the reader has been stopped by the Stop key, an empty hopper, a full stacker, an error, a misfeed, or a transport jam.

Reader Stop Key. This key stops the read feed at the end of the card feed cycle in progress and/or removes the reader from the ready status. The external system may continue processing until the next read card command causes a reader no-feed stop.

Nonprocess Runout Key. This key runs cards out of the read feed after a reader check error or after the Stop key has been used to stop the reader. The cards are run out into the read error select stacker without transfer of read buffer storage to the external system. The Reader Check light and check circuits are turned off. Cards must be removed from the hopper to make the Nonprocess Runout key active.

Load Key. This key causes three card feed cycles on initial run-in. Data from the first card is checked, read into the read buffer storage, and transferred in numerical mode to the using system. Upon completion of this data transfer, another card feed cycle occurs which loads read buffer storage with the data from the second card. In order to transfer data from the second card to the using system, a read command from the system is required. Run Trg Off Manual line (Table 7) must be up to make the Load key active.

Reader Check Light. This light is turned on by an unequal comparison between the read and check stations or by incorrect parity detected at read buffer storage during card read. When it is on, the reader is stopped, ready status is terminated, and the buffer storage data just read cannot be transferred to the using system on a subsequent read command until the error has been cleared and a new card fed.

CARD PUNCH CONTROLS

Punch On/Off Switch. This switch is active after the power in the external system comes on. It provides power to the punch circuits and turns on the Punch Power Ready light.

Punch Start Key. This key causes cards to feed into the punch station on initial run-in (two feed cycles) and turns on the Punch Ready light. It is also used to re-establish a ready status after an error, a nonprocess runout, an empty hopper, a full stacker, a misfeed, a transport jam, or depression of the Stop key.

Punch Stop Key. This key stops the punch feed at the end of the card cycle in progress and/or removes the punch from ready status.

Punch Nonprocess Runout Key. This key is used to run out and check the last punched card of a group. Depressing the Nonprocess Runout key, following a punch error, causes the remaining cards to follow the error card into the error select stacker. The card following the error is checked and the punch check light is turned on if it, too, contains an error. Cards must be removed from the hopper, and if an error exists the Check Reset key is depressed to make the Nonprocess Runout key operative.

Check Reset Key. This key resets error circuits and turns off the Punch Check light. Depression of the Check Reset key is followed by depression of the Start key or Nonprocess Runout key, depending upon the operation desired.

Select N Stop – Select Stop Key. This switch controls whether the punch stops or continues punching when an error is detected. The error card is selected into the error select stacker. With the switch set to stop, the punch feed stops with the error card in the error select stacker.

Punch Check Light. This light is turned on when an unequal comparison occurs between the data punched and the data written into the punch buffer storage. It is also turned on when a parity error occurs during punching. When this light comes on, the machine is stopped and ready status is terminated.

Table 7. 1622 Connections from the 1620

1622 A-Gate Connector*	Title**	1622 Card Type	I/O	1622 System Diagram	1620 Card Type	Pulse Length	Frequency per Input/Output Card
AZA02***	–C C Bit	DED	O	04.83.01.1	DEE	38 μsec	Any line can have as many as 80 pulses, one every 40 μsec, if data being transmitted requires them.
AZA04	–C A Bit	DED	O	04.83.01.1	DEE	38 μsec	
AZA06	–C B Bit	DED	O	04.83.01.1	DEE	38 μsec	
AZA08	–C 8 Bit	DED	O	04.83.01.1	DEE	38 μsec	
AZA10	–C 4 Bit	DED	O	04.83.01.1	DEE	38 μsec	
AZA12	–C 2 Bit	DED	O	04.83.01.1	DEE	38 μsec	
AZA14	–C 1 Bit	DED	O	04.83.01.1	DEE	38 μsec	
AZA16	–C Cd Rd Bff Rdy	DED	O	04.83.04.1	DEE	3.3 ms (A)	Once per card
AZA18	–C Cd Rd Sync	DED	O	04.83.04.1	DEE	8 μsec	80 pulses, one every 40 μsec
AZA20	–C Cd Rd Data Gate	DEE	I	04.83.06.1	DED	3.3 ms	Once per card
AZA22	–C Set MDR Sam I/O	DEE	I	04.83.06.1	DED	3 μsec	80 pulses, one every 40 μsec
AZA24	–C Last Card	DED	O	04.83.04.1	DEE	(B)	——
AZA26	–C Cd Rd Disconnect	DED	O	04.83.04.1	DEE	20 μsec	Once per card
AZA28	–C Rd Chk Trg Off	DEE	I	04.83.06.1	DED	(C)	——
AZA30	–C Run Trg Off Manual	DEE	I	04.83.06.1	DED	Manual	——
AZA32	–C Cd Rd Load	DED	O	04.83.04.1	DEE	(D)	——
AYA02	–C 1620 C Bit (Punch C)	DEE	I	04.83.05.1	DED	25 μsec	Any line can have as many as 80 pulses, one every 40 μsec, if data being transmitted requires them.
AYA04	–C 1620 A Bit (Punch 0)	DEE	I	04.83.05.1	DED	25 μsec	
AYA06	–C 1620 B Bit (Punch X)	DEE	I	04.83.05.1	DED	25 μsec	
AYA08	–C 1620 8 Bit (Punch 8)	DEE	I	04.83.05.1	DED	25 μsec	
AYA10	–C 1620 4 Bit (Punch 4)	DEE	I	04.83.05.1	DED	25 μsec	
AYA12	–C 1620 2 Bit (Punch 2)	DEE	I	04.83.05.1	DED	25 μsec	
AYA14	–C 1620 1 Bit (Punch 1)	DEE	I	04.83.05.1	DED	25 μsec	
AYA16	–C Cd Pch Disconnect	DED	O	04.83.04.1	DEE	10 μsec	Once per card
AYA18	–C Cd Pch Sync	DED	O	04.83.04.1	DEE	8 μsec	80 pulses, one every 40 μsec
AYA20	–C Cd Pch Bff Rdy	DED	O	04.83.04.1	DEE	3.3 ms (D)	Once per card
AYA22	–C Cd Pch Data Gate	DEE	I	04.83.06.1	DED	3.3 ms	Once per card
AYA24	–C Set I/O Sam MDR	DEE	I	04.83.06.1	DED	6 μsec	80 pulses, one every 40 μsec
AYA26	–C I/O Exit Trg	DEE	I	04.83.06.1	DED	20 μsec	Once per card
AYA28	–C WR Chk Trg Off	DEE	I	04.83.06.1	DED	(B)	——
AYA30	–C Manual Reset	DEE	I	04.83.06.1	DED	Manual	——

*A Gate connectors AZA01 through AZA32 are connected through the cable to shoe connector C, terminals 01 through 32, respectively. A Gate connectors AYA01 through AYA30 are connected through the cable to shoe connector B, terminals 01 through 30, respectively.

**All signal levels are –2.0 v nominal; no signal levels are at ground. The current required on each line is 15.5 ma. There are no restrictions on signal rise and fall times.

***The TW (twisted pair) wire associated with each signal wire is connected to the odd-numbered terminal immediately preceding the signal connector, i.e., AZA01 in the case of the Read C-bit signal.

–C is nominally –2.0 v

+C is nominally +1.5 v

(A) Assume continuous card feeding

(B) Last read card only

(C) Occurs during error only

(D) During load operations only

DED Driver card

DEE Terminator card

I/O Refers to lines "In" to the 1622 or "Out" of the 1622

CARD READ AND PUNCH LIGHTS

Stacker Light. This light is turned on when any stacker is full. Both feeds are stopped and removed from ready status. Operation may be resumed after the stacker is emptied.

Transport Light. This light is turned on when a card in either feed does not feed properly. When a misfeed occurs, both feeds are stopped and removed from the ready status. After the condition is corrected, both Start keys must be depressed to resume operation.

Fuse Light. This light is turned on to indicate an open fuse when a DC signal fuse opens.

Thermal Light. This light is turned on when any one of the four 1622 thermal switches opens due to excessive gate temperature. After clearing the condition responsible for the excessive temperature, a Reset key on the external system must be depressed to cause the manual reset line to come up (see Table 7). Depressing the Reset key turns off the Thermal light and allows operations to be resumed.

Lines to the Card Read Punch

Circuits to operate and control a 1622 Card Read Punch are contained in the using system. Information concerning the interconnecting lines is provided in the following pages. This information is given in terms of how the 1622 accepts and receives data and control signals. Characteristics of these connecting lines are summarized in Table 7. The A-gate connectors AZA02 through AZA32 and AYA26 connect the external system and the Card Reader. Connectors AYA02 through AYA30 (except AYA26) connect the external system and the Card Punch. Terminal block locations on gate A-1 of the 1622 are shown in Figure 13. The following comments apply to the AZA and AYA connectors listed in Table 7.

Connections with the Card Reader

AZA02, 04, 06, 08, 10, 12, and 14 Read C, A, B, 8, 4, 2, 1. Signals from the 1622 Single Character Register (SCR) are placed on these lines to be transmitted to the using system.

AZA16 Cd Rd Bff Rdy. The signal on this line indicates that a card has been fed past the second read brushes and that the 1622 read buffer storage has been loaded and checked.

AZA18 Cd Rd Sync. The Cd Rd Sync signal is used:

1. To indicate that the 1622 clock has started, causing the SCR to be loaded from the read buffer.
2. To provide a signal to the external system so that the output of the SCR can be gated to the system as required.

AZA20 Cd Rd Data Gate. A signal on this line serves two purposes:

1. The Cd Rd Data gate initiates the transfer of the first of 80 characters after the signal interrogates the 1622 circuits to see if punching of a row of data is in progress. The start of the transfer is delayed until after punching of the row is completed.
2. The signal also gates the transfer of characters from the SCR to the external system.

AZA22 Set MDR SAM I/O. A Set Memory Data Register (MDR) Sample I/O signal on this line starts the 1622 clock to initiate the transfer to the using system of the second and all subsequent characters.

AZA24 Last Card. The Last Card signal indicates that data from the last card (no more cards in read feed) has been transferred to the system.

AZA26 Cd Rd Disconnect. After the complete buffer contents have been transferred to the system, the Cd Rd Disconnect signal initiates a disconnect of the system from the 1622. The system can then continue

Locations in 1622 are shown from viewer's right

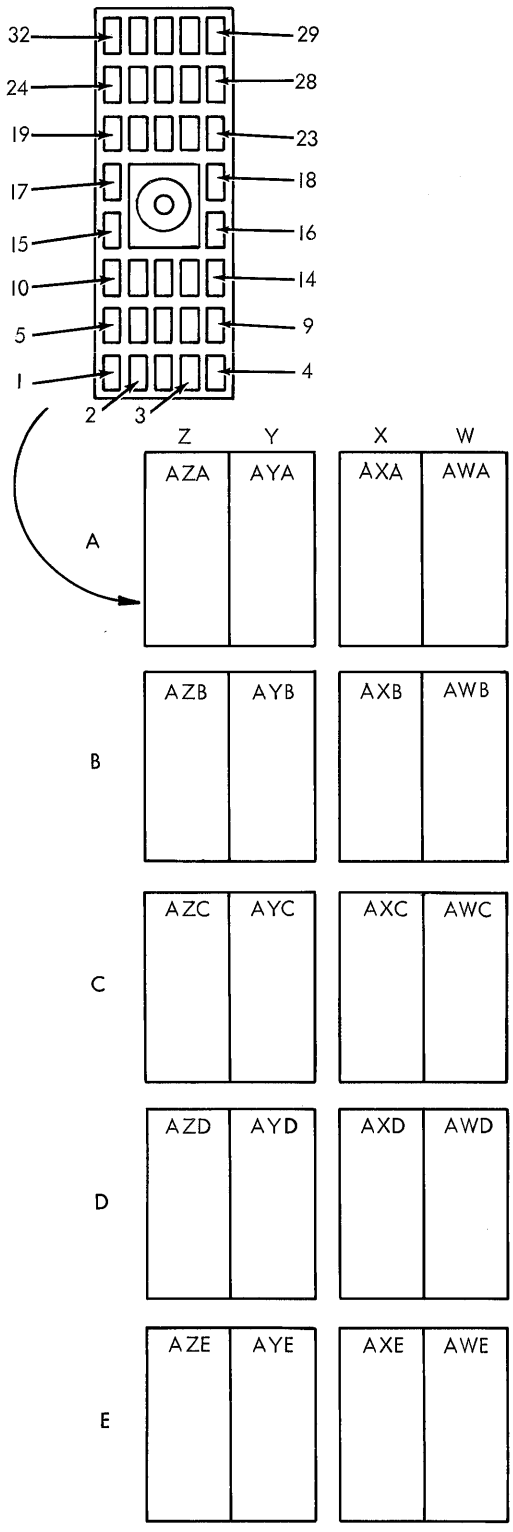


Figure 13. 1622 Signal Cable Connectors

its sequence of operations. If no error has been detected in the using system, a Rd Chk Trg Off signal is returned to the 1622 and the 1622 read clutch magnet is energized to initiate a card feed cycle. The card feed cycle refills the buffer.

AZA28 Rd Chk Trg Off. Lack of a signal on this line indicates that a test of the data lines in the using system has detected a read error. Feeding of the next card is prevented and the erroneous data remains in the 1622 read buffer.

AZA30 Run Trg Off Manual. A signal on this line indicates that the system is in the manual mode, i.e., the system is not running. The Run Trg Off Manual signal is used with Load key operation.

AZA32 Cd Rd Load. Depression of the Load key on the 1622 causes the feeding of three cards from the hopper. The contents of the first card enter the read buffer. The Cd Rd Load signal is returned to the system to indicate that the contents of the first card are ready to be used in loading. See the *CE Manual of Instruction* 1620 *Additional Features,* Form 227-5513.

AYA26 I/O Exit Trg. This signal from the system turns off the disconnect control latches in the 1622, located at A12A19 and A11E10 on System Diagram 04.15.66.1. The signal occurs at the end of a read operation.

Connections with the Card Punch

AYA02, 04, 06, 08, 10, 12, 14, Punch C, A, B, 8, 4, 2, 1. Signals from the system output data lines are placed on these lines for transfer to the SCR and from there into the 1622 punch buffer.

AYA16 Cd Pch Disconnect. A Cd Pch Disconnect signal initiates a disconnect of the external system from the 1622. The system can then continue its sequence of operations. If no error has been detected in the system during data transfer, a punch card feed cycle occurs. See AYA28 Wr Chk Trg Off.

AYA18 Cd Pch Sync. The Cd Pch Sync signal initiates an external system output cycle which puts a BCD character on the input lines to the 1622. See AYA02-14.

AYA20 Cd Pch Bff Rdy. A signal on this line indicates to the system that the punch buffer is ready to receive new data.

AYA22 Cd Pch Data Gate. A signal on this line interrogates the 1622 circuits to see if the reading of a row of holes in the card is in progress. If reading of a row has not been completed, the back signal is delayed until the complete row is read. At this time, a card Pch Sync signal (AYA18) is returned to the system to initiate an output cycle in which the first digit is transferred to the 1622.

AYA24 Set I/O SAM MDR. The Set I/O Sample Memory Data Register (MDR) signal initiates the transfer of the second and all remaining (78) characters from the system to the 1622.

AYA28 Wr Chk Trg Off. Lack of this signal indicates that a test of the system output data lines has determined that a write error occurred. Feeding and punching of the next card is prevented and the erroneous data remains in the 1622 buffer.

AYA30 Manual Reset. A signal on this line indicates that the system is in a reset operation. This may be due to a manual reset, a power on reset, or a power off reset. All latches in the 1622 will be reset except for the error latches.

Clutch Controls

The punch clutch is controlled by the following conditions as shown by circuitry on System Diagram 14.15.06.1.

1. Run-in
2. Nonprocess Runout (NPRO)
3. Control from the external system.
   A –S level at pin P of the OR block at A3 2A25 (System Diagram 04.15.06.1) is required to energize the punch clutch from an external control.

The read clutch is controlled by the following conditions as shown on System Diagram 04.15.06.1.

1. Punch
2. Nonprocess Runout (NPRO)
3. Control from the external system.
   A –S level at pin A of the OR block at A1 2A25 (System Diagram 04.15.06.1) is required to energize the read clutch under external control.

Power Sequencing Interlocks

Terminals AC 9 and AC 10. These may be connected as desired in the using system to give an indication that the 1622 voltages are up (System Diagram 04.01.30.1).

Terminal AC 8. This terminal must be grounded so the thermal relay can be energized (System Diagram 04.01.30.1).

Terminal AC 11. This terminal may be used in an external system as an indicator that the thermostats are normally closed.

Terminal AC 3. The AC 3 terminal must be connected to +24 volts in the using system to start the power on sequence in the 1622.

DC Isolated Ground Terminal, AC Isolated Ground Terminal, and Frame Ground. These lines in the power cable (System Diagram 04.90.35.1) are connected to the power supply line and the frame grounds in the using system.

Power Supplies

The voltages which must be supplied to the 1622 from an external source are shown in Table 8. The voltage supplied within the 1622 are summarized in Table 9.

Table 8. Voltages Supplied to 1622 from the External System

Function	Voltage Supplied	Maximum Current	Terminals Used	System Diagram
Line Voltage	208 or 230 v AC ±10%	10 amp	AC 4 and AC 7	04.90.10.1
Cooling Fans	110 v AC	0.4 amp (not fused)	AC 1 and AC Grd	04.90.10.1
Sequence Voltage	24 v AC	3.2 amp	AC 5 and AC 6	04.90.40.1
Convenience Outlet	110 v AC	7 amp (not fused)	AC 2 and AC Grd	04.90.10.1

Table 9. Voltages Supplied in 1622 for Internal Use Only

Function	Voltage Supplied	Maximum Current	System Diagram
Power Sequencing	24 v DC	3.2 amp	04.90.40.1
Relay Power Supply	20 v DC	15 amp	04.90.20.1
SMS Power Supply	−12 v DC	16 amp	04.90.20.1
SMS Bias Power Supply	12 v DC	8 amp	04.90.20.1
Marginal Checking Voltage	±3 v DC	5 amp	04.90.20.1
Voltage Regulator	208 or 230 v AC to 133 v AC	(1250 watts)	04.90.20.1

The following material provides data for the use of non-IBM engineers who wish to attach the 1623 Core Storage Unit to their equipment. Easy access to tie-in data not readily available in other IBM publications is provided.

Theory of operation and mechanical principles are not included. These may be found in the following IBM publications relating to the 1623.

Title	*Form*
IBM 1620 *CE Manual of Instruction — Additional Features*	227-5513
IBM 1620 *CE Reference Manual — Additional Features*	227-5540

Additional information can be obtained from systems diagrams and other available engineering documents.

General Description

The 1623 Core Storage Unit provides additional core storage for applications which require more than 20,000 storage positions. One or two additional 20,000-position modules of core storage are available in the 1623. Each core storage array is placed in parallel with the basic array in the 1620. Each 20,000-position module of storage contains its own Memory Buffer Registers (MBR), sense amplifiers, inhibit drivers, matrix switches, and decode switches.

The additional MBR units in the 1623 feed through the basic MBR to reach the data paths in the 1620. Information is read into 1623 core storage by impulses from either Memory Data Register (MDR) or I/O device lines to the MBR in the 1623. Selection of a particular core address is accomplished by the Memory Address Register (MAR) in the same manner as in the basic machine.

Connections to the 1623 Core Storage Unit

Information concerning the lines that connect the 1623 to the 1620 is contained in the following material. The information is given in terms of how the 1623 accepts and receives data and control signals from the 1620. Characteristics of the data and control lines to the 1623 are summarized in Table 10. The following comments apply to the shoe connector lines listed in Table 10.

Signal and Timing Lines

AXF06 to AXG04 MAR — Bit Lines. The lines from the Memory Address Register triggers are brought to the decode switches in the 1623.

AXG06 and AXG08 Odd SA Gate and Even SA Gate. These two lines control the memory sense amplifiers in the 1623 for readout of the odd-addressed digit or even-addressed digit, or both.

AXG10 <50. The <50 signal from the 1620 gates the 1623 pre-sense amplifier for addresses less than 50 into the sense amplifier. The <50 signal is inverted within the 1623 to develop a >50 signal. This signal gates the 1623 pre-sense amplifiers into the sense amplifier.

AXG12 and AXG14 Write OD Gate and Write EV Gate. These signals gate the output of the MDR or the I/O device from the 1620 into the 1623 MBR-Odd register or MBR-Even register or both.

AXG16 I/O Rd Gate. The I/O Rd Gate switches the I/O alpha zone digit from the 1620 input translator into the MBR-Even register in the 1623.

AXG18 to AXG24 Gate Mem Sam 40K, 60K. These are timing pulses for timing of 1623 tens and thousands read and write current drivers. The signals are controlled by the ten thousands position of the MAR in the 1620.

AXG26 R1 D4. This is a timing pulse from the 1620. It is used for 1623 hundreds read current-driver timing.

AXG28 R1 D2. The R1 D2 signal switches with the <50 gate in the 1623 to time the sense amplifier strobe.

AXG30 R0 D4. This is a timing pulse for units read current-driver timing in the 1623.

AXG32 Wr Mem W0 D5. This signal gates the inhibit drivers.

AXH02 Set R2 D1. The set R2 D1 signal is a timing pulse for the Write OD gate and the Write EV gate (AXG12, 14).

AXH06 MBR Reset. This signal controls the reset of the MBR-Odd and MBR-Even C, 8, 4, 2, and 1 bit triggers in the 1623.

AXH08 MBR Reset F. This signal controls the reset of the MBR-Odd and MBR-Even F-bit triggers in the 1623.

AXH10 Gate MBR C. This impulse from the 1620 gates the C-bit transfer from the MDR in the 1620 to the 1623 MBR.

Table 10. 1623 Connections from the 1620

1620 Shoe Connector	Title	1623 Card Type	I/O	1623 System Diagram	SMS Card in 1620	Pulse Length (μsec)
AXF06*	−C MAR 1 Bit 10 Thous	TDA	I	03.41.01.1	DBU	18
AXF08	−C MAR 2 Bit Units	TDA	I	03.41.01.1	DBU	18
AXF10	−C MAR 4 Bit Units	TDA	I	03.41.01.1	DBU	18
AXF12	−C MAR 8 Bit Units	TDA	I	03.41.01.1	DBU	18
AXF14	−C MAR 1 Bit Tens	TDA	I	03.41.02.1	DBU	18
AXF16	−C MAR 2 Bit Tens	TDA	I	03.41.02.1	DBU	18
AXF18	−C MAR 4 Bit Tens	TDA	I	03.41.02.1	DBU	18
AXF20	−C MAR 8 Bit Tens	TDA	I	03.41.02.1	DBU	18
AXF22	−C MAR 1 Bit Hund	TDA	I	03.41.03.1	DBU	18
AXF24	−C MAR 2 Bit Hund	TDA	I	03.41.03.1	DBU	18
AXF26	−C MAR 4 Bit Hund	TDA	I	03.41.03.1	DBU	18
AXF28	−C MAR 8 Bit Hund	TDA	I	03.41.03.1	DBU	18
AXF30	−C MAR 1 Bit Thous	TDA	I	03.41.04.1	DBU	18
AXF32	−C MAR 2 Bit Thous	TDA	I	03.41.04.1	DBU	18
AXG02	−C MAR 4 Bit Thous	TDA	I	03.41.04.1	DBU	18
AXG04	−C MAR 8 Bit Thous	TDA	I	03.41.04.1	DBU	18
AXG06	+C ODD SA Gate	TDA	I	03.41.05.1	DBU	(A)
AXG08	+C EVEN SA Gate	TDA	I	03.41.05.1	DBU	(A)
AXG10	−C < 50	TDA	I	03.41.05.1	DBU	(B)
AXG12	−C Write OD Gate	TDA	I	03.41.05.1	DBU	(B)
AXG14	−C Write EV Gate	TDA	I	03.41.05.1	DBU	(B)
AXG16	−C I/O Rd Gate	TDA	I	03.41.05.1	DBU	(C)
AXG18	−C Gt Mem Sam 40K TN R0-D8	TDA	I	03.41.18.1	DBU	8
AXG20	−C Gt Mem Sam 60K TN R0-D8	TDA	I	03.41.18.1	DBU	8
AXG22	−C Gt Mem Sam 40K Thous R1-D7	TDA	I	03.41.18.1	DBU	7
AXG24	−C Gt Mem Sam 60K Thous R1-D7	TDA	I	03.41.18.1	DBU	7
AXG26	+C R1-D4	TDA	I	03.41.18.1	DBU	4
AXG28	−C R1-D2	TDA	I	03.41.18.1	DBU	2
AXG30	+C R0-D4	TDA	I	03.41.18.1	DBU	4
AXG32	−C WR Mem W0-D5	TDA	I	03.41.18.1	DBU	5
AXH02	+C Set R2-D1	TDA	I	03.41.18.1	DBU	1
AXH04						
AXH06	−C MBR Reset	TDA	I	03.41.06.1	DBU	3
AXH08	−C MBR Reset F	TDA	I	03.41.06.1	DBU	3
AXH10	−C Gate MBR C	TDA	I	03.41.19.1	DBU	(A)
AXH12	+C MDR 8 Bit	TDA	I	03.41.19.1	DBU	15
AXH14	+C MDR 4 Bit	TDA	I	03.41.19.1	DBU	15
AXH16	+C MDR 2 Bit	TDA	I	03.41.19.1	DBU	15
AXH18	+C MDR 1 Bit	TDA	I	03.41.19.1	DBU	15
AXH20	−C Gate MBR F	TDA	I	03.41.19.1	DBU	(A)
AXH22	+C Rd C Zone	TDA	I	03.41.20.1	DBU	2
AXH24	+C Rd 1 Zone	TDA	I	03.41.20.1	DBU	2
AXH26	+C Rd 2 Zone	TDA	I	03.41.20.1	DBU	2
AXH28	+C Rd 4 Zone	TDA	I	03.41.20.1	DBU	2
AXJ02	−C MBR Not C Bit OD	TAB	O	03.41.07.1	TDA	18
AXJ04	−C MBR Not F Bit OD	TAB	O	03.41.07.1	TDA	18
AXJ06	−C MBR Not 8 Bit OD	TAB	O	03.41.07.1	TDA	18
AXJ08	−C MBR Not 4 Bit OD	TAB	O	03.41.07.1	TDA	18
AXJ10	−C MBR Not 2 Bit OD	TAB	O	03.41.07.1	TDA	18
AXJ12	−C MBR Not 1 Bit OD	TAB	O	03.41.07.1	TDA	18
AXJ14	−C MBR Not C Bit EV	TAB	O	03.41.17.1	TDA	18
AXJ16	−C MBR Not F Bit EV	TAB	O	03.41.17.1	TDA	18
AXJ18	−C MBR Not 8 Bit EV	TAB	O	03.41.17.1	TDA	18
AXJ20	−C MBR Not 4 Bit EV	TAB	O	03.41.17.1	TDA	18
AXJ22	−C MBR Not 2 Bit EV	TAB	O	03.41.17.1	TDA	18
AXJ24	−C MBR Not 1 Bit EV	TAB	O	03.41.17.1	TDA	18
AXJ26	+C CE SW3 C8 T	TDA	I	03.41.08.1	DBU	(D)
AXJ28	−C CE SW5 C8 C	TDA	I	03.41.08.1	DBU	(D)
AXJ30	+C CE SW4 421 T	TDA	I	03.41.08.1	DBU	(D)
AXJ32	−C CE SW6 421 C	TDA	I	03.41.08.1	DBU	(D)

*The TW (twisted pair) wire associated with each signal wire is connected to the odd-numbered terminal immediately preceding the signal connector, i.e., AXF05 in the case of the MAR 1 Bit 10 Thous signal.

+C Nominally +1.5 v
−C Nominally −2.5 v
TAB Data Line Driver
TDA Line Terminator
DBU Data Line Driver

(A) This pulse must be long enough to gate set pulses (MBR-MDR)—approximately 4 μsec.
(B) This pulse must be long enough to gate write pulse (W1-D2)—approximately 3 μsec.
(C) This pulse must be long enough to gate (R1-D4)—approximately 4 μsec.
(D) Manual control

AXH12 to AXH18 MDR – Bit. These inputs to the 1623 MBR are from the MDR bit triggers in the 1620.

AXH20 Gate MBR F. This gates the F bit from the 1620 MDR to the 1623 MBR.

AXH22 to AXH28 Rd – Zone. These lines are zone bit inputs to MBR-Even in the 1623 from the 1620 input translator.

AXJ02 to AXJ12 MBR Not __ Bit OD. These are output lines from the 1623 MBR-Odd register to the 1620 MBR-Odd register.

AXJ14 to AXJ24 MBR Not __ Bit EV. These output lines from the 1623 MBR-Even register to the 1620 MBR-Even register.

AXJ26 to AXJ32 CE SW 3, 4, 5, 6. These lines enable the customer engineer to control MBR inhibit lines for servicing.

Power Sequencing Interlocks

Terminal PSTB 4-3 Power On. The Power On signal from the external system starts the power on sequence in the 1623 (System Diagram 03.90.40.1).

Terminal PSTB 4-8 Thermal. This terminal must be grounded so the thermal relay can be energized (System Diagram 03.90.42.1).

Terminal PSTB 4-9 and 4-10 Ready In and Ready Out. These terminals allow the system to determine that the 1623 power sequence has been completed (System Diagram 03.90.40.1).

Terminal PSTB 4-11 and 4-12 Reset In and Reset Out. These terminals are used to indicate to the external system that the thermal relay in the 1623 is energized (System Diagram 03.90.42.1).

DC Isolated Ground Terminal, AC Isolated Ground Terminal and Frame Ground. These lines in the power cable are connected from the 1623 grounds to the system grounds (System Diagram 03.90.35.1).

Power Supplies

The voltages which must be supplied to the 1623 from an external source are shown in Table 11. The voltages supplied within the 1623 are summarized in Table 12.

Table 11. Voltage Supplied to 1623 from External System

Function	Voltage Supplied	Maximum Current	Terminals Used	System Diagram
Line Voltage	208 or 230 v AC ±10%	10 amp	PSTB 4-4 PSTB 4-7	03.90.10.1
Sequence Voltage	24 v AC	3 amp	PSTB 4-5 PSTB 4-6	03.90.40.1
Convenience Outlet	110 v AC	7 amp (not fused)	PSTB 4-1 AC Ground	03.90.10.1
–36 Voltage Bias for Current Drivers	–36 v DC	0.1 amp (not fused)	PSTB 4-2	03.90.30.1

Table 12. Voltage Supplied in 1623 for Internal Use Only

Function	Voltage Supplied	Maximum Current	System Diagram
Memory Supply (Matrix Sw)	+30 v DC	4 amp	03.90.21.1
SMS Bias Power Supply	+12 v DC	16 amp	03.90.20.1
SMS Power Supply	–12 v DC	20 amp	03.90.20.1
Marginal Checking Voltage	±3 v DC	5 amp	03.90.21.1
DC Sequence Voltage	+24 v DC	3 amp	03.90.40.1

IBM 1624 Paper Tape Punch

The following material provides data for the use of non-IBM engineers who wish to attach the 1624 Paper Tape Punch to their equipment. Easy access to tie-in data not readily available in other IBM publications is provided.

Theory of operation and mechanical principles are not included. These may be found in the following IBM publications relating to the 1624.

Title	*Form*
IBM 1620 *CE Manual of Instruction*	227-5507
IBM 1620 *CE Reference Manual*	227-5500
IBM 1620 *Data Processing System Reference Manual*	A26-4500
IBM 870 *Document Writing System CE Reference Manual*	223-6890

Additional information can be obtained from system diagrams and other available engineering documents.

General Description

The IBM Paper Tape Punch punches output characters in 8-channel paper tape at the rate of 15 characters per second. The punch accepts a 7-bit code (C, X, 0, 8, 4, 2, 1) from the attached system, punches the coded character, and spaces to the next column. The EL (end-of-line) channel is punched when a record mark is sensed in memory during a write operation with the paper tape punch selected. The EL hole is punched in the column following that occupied by the last character transmitted from memory.

Connections to the 1624 Paper Tape Punch (Table 13)

Signal and Data Lines

SC1-10. These lines are all thyratron output lines from the system. They are used to energize magnets

Table 13. 1621 Connections from the 1620 (for 1624 use)

1621 Shoe Connector (to 1624)	Title	1621 Card Type	I/O	1621 System Diagram	1620 Card Type	Current Required	Rise Time (μsec)	Fall Time (μsec)	Signal Level (in volts) On	Signal Level (in volts) Off
SCA01	Punch EL	PM	I	02.84.50.1	NP		65	10	0	+48
SCA02	Punch C Bit	PM	I	02.84.50.1	NP		65	10	0	+48
SCA03	Punch X Bit	PM	I	02.84.50.1	NP		65	10	0	+48
SCA04	Punch 0 Bit	PM	I	02.84.50.1	NP		65	10	0	+48
SCA05	Punch 8 Bit	PM	I	02.84.50.1	NP	see Text,	65	10	0	+48
SCA06	Punch 4 Bit	PM	I	02.84.50.1	NP	SC1-10	65	10	0	+48
SCA07	Punch 2 Bit	PM	I	02.84.50.1	NP		65	10	0	+48
SCA08	Punch 1 Bit	PM	I	02.84.50.1	NP		65	10	0	+48
SCA09	Punch Feed	PM	I	02.84.50.1	NP		65	10	0	+48
SCA10	Punch No-Feed	PM	I	02.84.50.1	NP		65	10	0	+48
SCA23	−S Tape Tension Cont	Int	O	02.84.50.1	MX	1.05 ma	SC23 see Text		−S	+S
SCA24	+S P3 Resp	Int	O	02.84.50.1	MX	3.15 ma			+S	−S
SCA25	+S Punch Check	Int	O	02.84.50.1	MX	1.05 ma			+S	−S
SCA27	+S Tape Feed	Int	O	02.84.50.1	MX	1.05 ma			+S	−S
SCA28	+S PCB 1	Int	O	02.84.50.1	MX	1.05 ma			+S	-S

Current Required is the current supplied or required for operation.

I/O Refers to lines "In" to the 1621 (for 1624 use) or "Out" of the 1621
Int Integrator
MX CTRL Power Inverter, two-way
NP Thyratron Card
PM Punch Magnet
SC Shoe Connector
+S 0 v (ground level)
−S 5.56 v to 12 v, depending on the loading

in the 1624 Paper Tape Punch. The thyratron circuit is conditioned by the system but must have its collector circuit completed as follows: from the collector of the thyratron, through the cable to the 1621, through the punch magnet, through a circuit breaker and back to the system to a +48 v supply. The circuit breaker is necessary because the thyratron does not extinguish unless the collector circuit is opened. The thyratron must be protected from the inverse voltage caused by the collapse of an inductive load. The output current is a maximum of 300 ma, a minimum of 20 ma. The minimum current requirement is necessary to keep the thyratron in conduction after it has been turned on. The output must be under control of a circuit breaker.

SC 1 Punch EL. An end-of-line punch (EL) is used to signify an end of record. It is punched at the end of a Write Call, Select 2 operation.

SC 2-8 Data Lines. Signals on combinations of these lines define the bit configuration of the characters to be punched.

SC 9 Punch Feed. The Punch Feed signal causes the clutch in the 1624 Paper Tape Punch to be tripped. This results in the punching of the bit configuration set up by the data lines.

SC 10 Punch No-Feed. This line is used to prevent spacing of the paper tape. It is under control of the write check circuitry and the tape tension contact.

SC 23-28. These lines are control lines and all are input lines to the 1620 to establish the sequence of operations. The lines are driven by integrators (rise time, 5 ms).

SC 23 –S Tape Tension Cont. This line indicates that tape is loaded in the 1624 and is in position to feed. It is a switch operated by a tape tension arm. The line is at a –S level when the switch is operated. The Tape Tension Cont controls punch no-feed and punch go circuitry when it goes to +S. It also turns off the Run trigger under this condition.

SC 24 +S P3 Resp (PCB 3). The P3 response line sets the P3 Interlock trigger on. This act begins the response operation. When the P3 Interlock trigger is turned off by PCB 1, the response is generated. Response pulse frequency is 64.8 ms. Refer to Figure 14 for timing and pulse length. At PCB 3 time, punching is completed but the punches are still through the tape. The ball check contacts are set up and the punch check signal is generated (+S, if there is an error).

SC 25 +S Punch Check. See SC 24.

SC 26 Not used.

SC 27 +S Tape Feed. The Tape Feed line is controlled by a manually operated switch. It has no timing. The Tape Feed signal controls the following:

1. Punch data lines (SC 2-8)
2. Punch Feed (SC 9)
3. Punch No Feed (SC 10),

and turns off the

4. Punch No-Feed light.

SC 28 +S PCB 1. See SC 24.

Power Supply

The only power supplied to the 1624 is +48 volts DC (System Diagram 02.84.50.1). This is furnished by the external system.

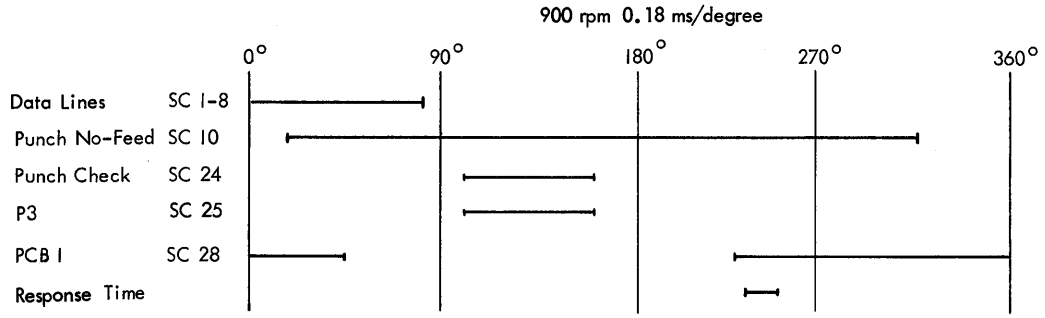


Figure 14. Punch Sequence

IBM®

International Business Machines Corporation
Data Processing Division
112 East Post Road, White Plains, New York