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IBM Series/1 System/370 Channel Attachment Feature and 4993 Model 1 Series/1—System/370 Termination Enclosure Description

First Edition (January 1979)

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Preface

This publication provides reference information relating to the operation and programming of the IBM Series/1–System/370 channel attachment. The attachment is comprised of the following:

- IBM Series/1–System/370 Channel Attachment Feature
- IBM 4993 Model 1 Series/1–System/370 Termination Enclosure

This reference information is provided primarily for experienced programmers who need to plan, correct, and modify programs written in assembler language.

The reader should have a working knowledge of both Series/1 programming and System/370 programming.

The material in this manual is organized as follows:

Chapter 1. Introduction describes the functional characteristics of the attachment and includes a description of the 4993 termination enclosure.

Chapter 2. Series/1 and System/370 Interaction describes how data is transferred between systems and how I/O commands interact between systems. This chapter also describes an IPL of the Series/1 from the System/370 and how time-out conditions can occur in the attachment.

Chapter 3. System/370 Programming Information is a detailed description of System/370 I/O commands, chaining, status, and resets as related to operation of the attachment.

Chapter 4. Series/1 Programming Information describes the Series/1 I/O commands, status information, and resets as related to operation of the attachment.

Appendix A. Reference Information contains a condensed version of the Series/1 and the System/370 I/O commands and status information for quick reference.

Prerequisite Publications

In order to use this manual effectively, the reader must be familiar with two processors; a model of the Series/1 and a model of the System/370 (both connected to the attachment). The publication order number for a particular processor model can be found as follows:

- Series/1 processor description. Refer to the *IBM Series/1 Graphic Bibliography*, GA34-0055.
- System/370 processor functional characteristics. Refer to the *IBM System/370 Bibliography*, GC20-0001.
- System/370 reference information. Use the manual *IBM System/370 Principles of Operation*, GA22-7000.

Related Publications

Additional publications are listed in the *IBM Series/1 Graphic Bibliography*, GA34-0055, or the *IBM System/370 Bibliography*, GC20-0001. This manual also makes reference to the *IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers' Information*, GA22-6974.

Contents

Chapter 1. Introduction

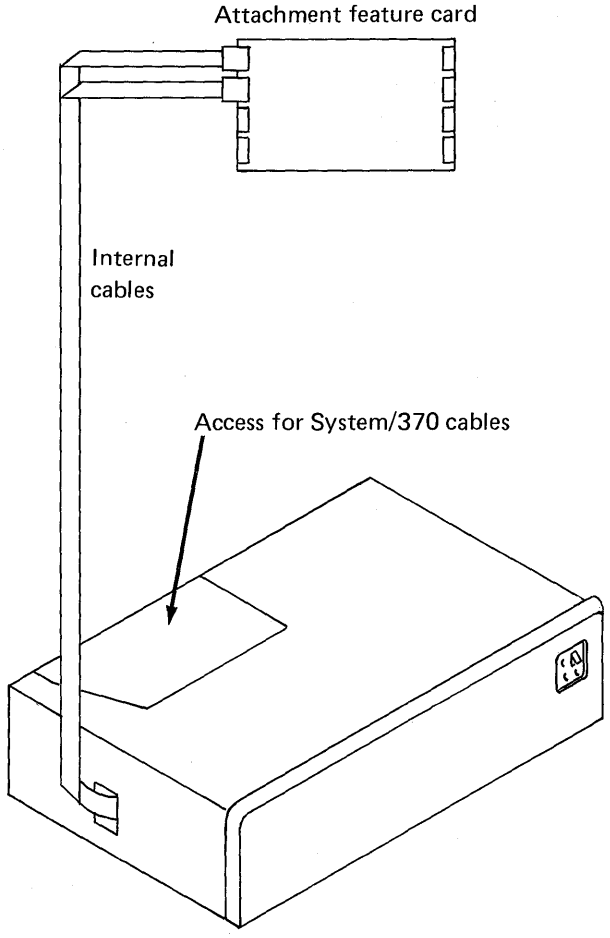
The IBM Series/1-System/370 channel attachment (a feature card and a 4993 termination enclosure) provides a means for storage-to-storage communications between a Series/1 processor and any System/370 Model 135-168 or a 3031, 3032 or 3033 processor. The attachment connects to the I/O channel of each processor and responds to the limited command set defined in this manual. Commands directed to the attachment can initiate and control the transfer of data between the two systems. Appropriate programming permits the Series/1 to act as a front-end processor for typical applications such as graphics processing, teleprocessing, and sensor I/O processing.

When the IBM Series/1-System/370 Channel Attachment Feature card is installed, a companion unit must also be installed. This unit is the IBM 4993 Model 1 Series/1-System/370 Termination Enclosure. The enclosure unit provides receptacles and termination for the System/370 channel cables.

Functional Description

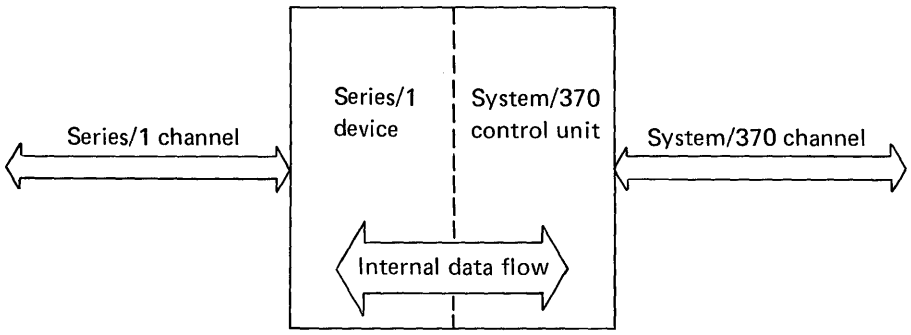
The Series/1-System/370 channel attachment consists of:

- A feature card that plugs into a Series/1 I/O feature card slot.
- A 4993 termination enclosure unit that is installed in the Series/1 rack. The enclosure unit is cabled (via internal cables) to the feature card. It also contains manual controls for power on/off and control unit enable/disable.



4993 termination enclosure

When the attachment is installed, it represents a single cycle-steal device on the Series/1 I/O channel. To the System/370, it represents a control unit with 32 I/O devices. The attachment uses one control unit position on a System/370 selector channel or block multiplexer channel (2860 channel and 2880 channel only, for Models 165 and 168). Logically the attachment is divided into a Series/1 section and a System/370 section.



The Series/1 section responds to Series/1-type I/O commands and operates as a single cycle-steal device. The Series/1 commands are explained in Chapter 4 of this manual. The System/370 section responds to I/O commands that follow the System/370 format. To the System/370 processor, this section appears as a control unit with 32 I/O devices. Refer to Chapter 3 for details of the System/370 I/O commands.

Internal logic in the attachment feature card provides a path to transfer data between the two sections. A four-byte data buffer is also provided in the attachment.

Data transfer operations between the two systems are initiated by the System/370. If the System/370 initiates a read operation, the Series/1 must respond with a write operation before data transfer can begin. The attachment ensures that the operations are "matched" (refer to "Matching Operations" in Chapter 2). When a matching operation has been accepted by the attachment, the systems are defined as being *connected*. Once the two systems are connected, the attachment controls the flow of data by "reading" from one system and then "writing" to the other system.

Performance Characteristics

The hardware transfers data at a data rate of the slower channel up to a maximum of 300,000 bytes per second. The actual throughput is affected by Series/1 processor performance and software overhead. The "I/O media" for both systems is main storage, therefore, the attachment is fully buffered.

Timing Considerations

The attachment uses an internal timer to time certain operations or sequences. A time limit (approximately 480 milliseconds) allows the attachment to terminate an operation if a "no response" condition occurs on the Series/1 system. Additional timing information is contained in "Time-out" in Chapter 2.

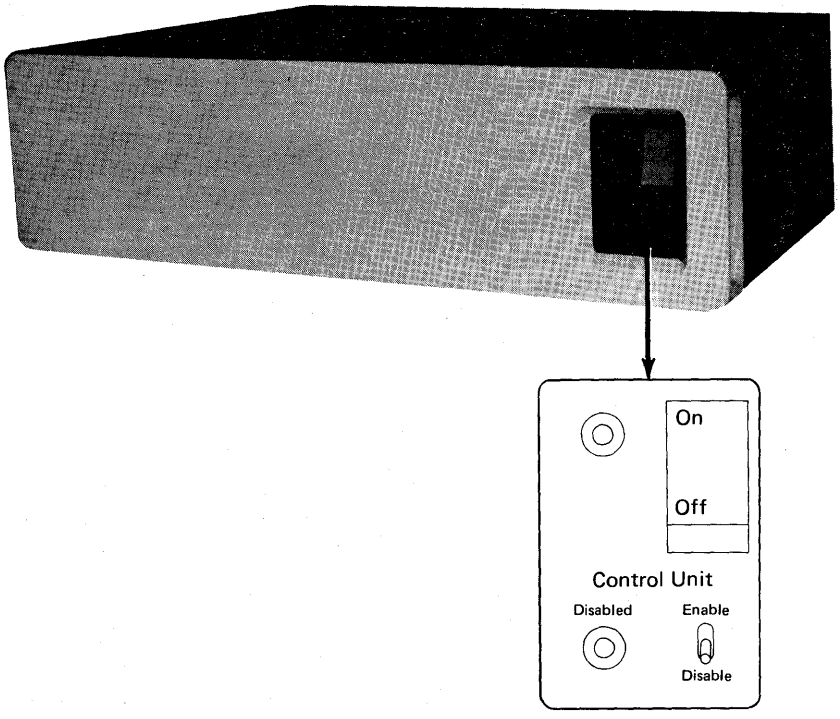
Installation Restrictions

Up to eight Series/1-System/370 attachments may be connected to a single System/370 I/O channel.

Any number of attachments may be installed on a Series/1 I/O channel, up to the addressing limit of the system and within physical limitations. Physical restrictions (due to 4993 location) limit the attachment to 1 per Series/1 rack enclosure. The overall performance of the system (Series/1 and System/370) should be considered when installing multiple units.

IBM 4993 Model 1 Series/1-System/370 Termination Enclosure

The 4993 enclosure unit is part of the Series/1-System/370 channel attachment, and it is cabled to the attachment feature card via internal cables. The unit provides cable receptacles and line driver/receivers for the System/370 interface. A power source for the driver/receivers is also contained in the enclosure.



Manual controls and indicators are provided for power on/off and control unit enable/disable.

Manual Operations

Two switches contained in the 4993 termination enclosure allow limited manual operations. The On/Off switch applies or removes incoming power to the 4993 (not the attachment feature card). An indicator (unlabeled) is turned on when the power source, in the enclosure, is at the proper level. The Enable/Disable switch controls the on-line/off-line state of the attachment relative to the System/370. When the attachment is enabled (on-line), System/370 operations can proceed in a normal manner. When disabled (off-line), the attachment cannot be selected from the System/370. An indicator is turned on when the attachment is in the disabled state.

The attachment must be switched off-line before removing power from the 4993, and it should be switched on-line after power is reapplied.

Chapter 2. Series/1 and System/370 Interaction

This chapter explains:

- Data transfer between systems.
- How the two systems are logically connected for a data transfer operation.
- How certain I/O commands from one system cause interaction with the other system.
- A System/370 IPL of the Series/1.
- Time-out conditions that can occur.

Specific I/O commands, status, and interrupts that are referred to in this chapter are explained in detail in Chapter 3 (System/370) or Chapter 4 (Series/1).

Data Transfer Between Systems

This section discusses the sequence of I/O commands necessary to initiate a data transfer between the Series/1 and the System/370. Refer to Figure 2-1 for an example of data transfer between systems.

Prepare Attachment

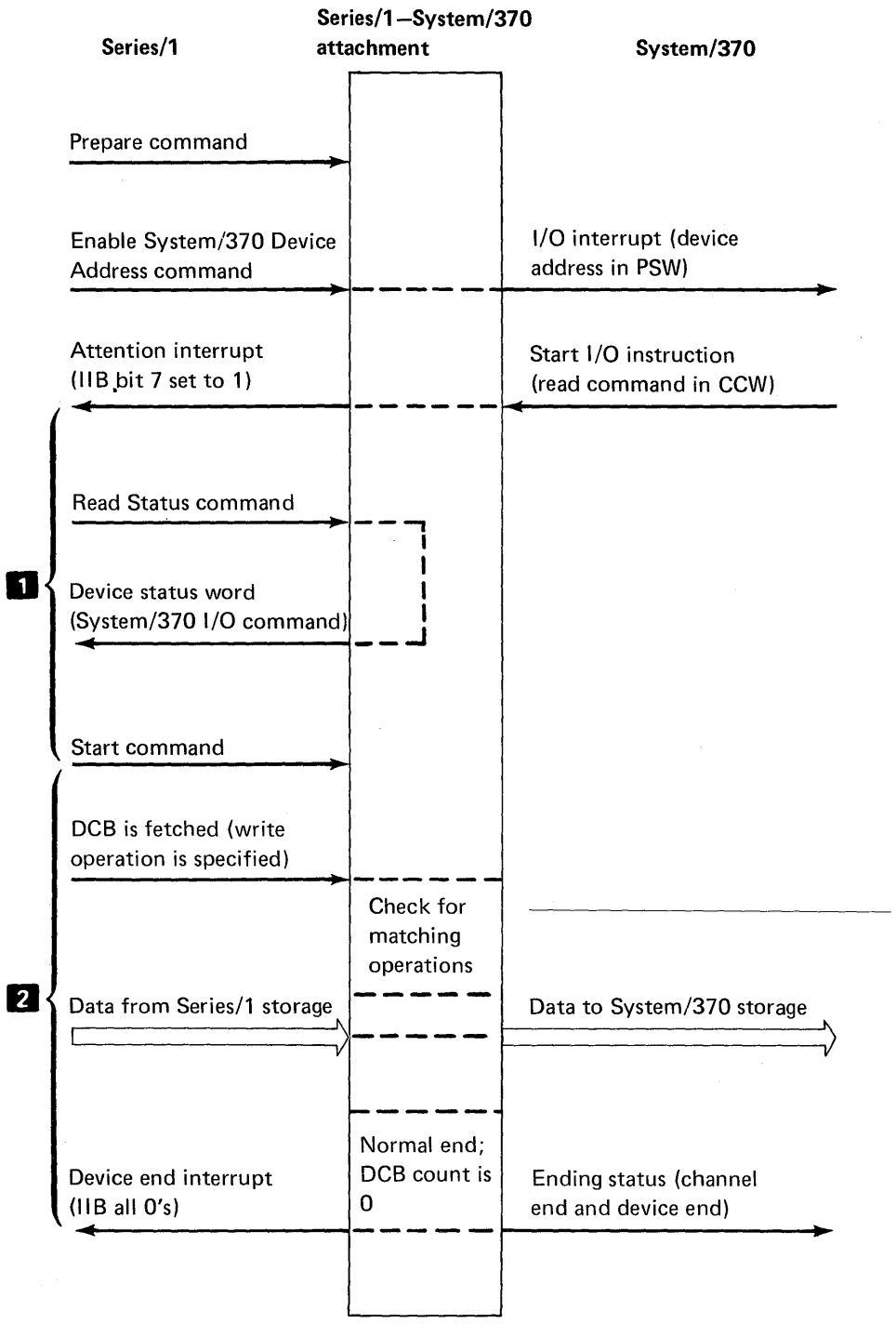
The attachment must be on-line to the System/370. The Series/1 program must prepare the attachment in the following manner:

1. Issue a *Prepare* command. This prepares the attachment to interrupt the Series/1 and assigns a specific priority interrupt level.
2. Issue an *Enable System/370 Device Address* command. This notifies the System/370 that a specific device (1 of 32) is now "ready."

Connection of Systems

All data transfer operations are initiated by the System/370. The System/370 program uses I/O commands such as *Read Buffer* or *Write*. The Series/1 program must respond with a *Start* command. A device control block (DCB) associated with the Start command defines the Series/1 read or write operation. System/370 commands used for this purpose generate an *attention* interrupt to the Series/1. The Series/1 program can then interrogate attachment status information to determine how to respond. If the System/370 initiates a read operation, the Series/1 must respond with a write operation. These operations are checked by the attachment to ensure a proper match; then the two systems are *connected* for the data transfer.

After the two systems are connected, a byte of data is "written" from one system to the attachment, then "read" from the attachment by the other system. The attachment routes the data from one channel to the other at the proper time. Normal termination for the data transfer occurs when the data count specified by the Series/1 DCB reaches 0. Ending status is presented to each system and the operation is terminated.



1 Series/1 program execution affects the channel busy time of the System/370.

2 Series/1 channel throughput affects the channel busy time of the System/370. Data is transferred at the rate of the slower channel up to a maximum of 300,000 bytes per second.

Figure 2-1. Example of data transfer between systems

Matching Operations

The Series/1 program must respond to a System/370 *attention* command by issuing a matching Series/1 I/O command. The attachment checks these commands to ensure a proper match. The Series/1 DCB is also checked (by the attachment) for a matching operation when data is to be transferred between systems. To avoid an error condition, the Series/1 program must respond as follows:

System/370 I/O command	Series/1 I/O command
Read Buffer	Start*
Read Modified	Start*
Diagnostic Read	Start*
Write	Start**
Erase/Write	Start**
Diagnostic Write	Start**
Select	Set System/370 Device End
Erase All Unprotected	Set System/370 Device End

* The DCB must specify a write operation.
** The DCB must specify a read operation.

I/O Command Interaction

Some I/O commands used by the attachment cause events to occur on both systems. For example, a System/370 I/O command that causes an attention interrupt to the Series/1. "System/370 I/O Command Interaction" and "Series/1 I/O Command Interaction" list the events that occur on the non-issuing system; assuming successful execution of the command.

System/370 I/O Command Interaction

System/370 I/O command	Series/1 event
Test I/O	None
Write	Attention interrupt
Read Buffer	Attention interrupt
No-Operation	None
Sense	None
Erase/Write	Attention interrupt or IPL
Read Modified	Attention interrupt
Select	Attention interrupt
Diagnostic Write	Attention interrupt
Diagnostic Read	Attention interrupt
Erase All Unprotected	Attention interrupt
Subsystem Load Enable	None
Sense I/O	None

Note: The System/370 commands that cause an attention interrupt to the Series/1 are referred to as *attention* commands. The Series/1 device status word contains necessary information about the attention interrupt.

Series/1 I/O Command Interaction

Series/1 I/O command	System/370 event
Read ID	None
Read Status	None
Prepare	None
Disable System/370 Device Address	None
Enable System/370 Device Address	I/O interrupt (device not enabled)
Set System/370 Device End*	None
Set Attention to System/370	I/O interrupt
Device Reset	Status presented—systems connected None—systems not connected
Start*	None
Start Diagnostic	None
Start Cycle Steal Status	None
Halt I/O	Status presented—systems connected None—systems not connected

* Issued in response to certain System/370 commands.

System/370 IPL of the Series/1

The Series/1–System/370 attachment is capable of executing a host system (System/370) IPL of the Series/1. An inhibit IPL jumper must be removed from the attachment feature card to allow this function. The System/370 program initiates the IPL by issuing two I/O commands in the proper sequence. This sequence is a *Subsystem Load Enable* command chained to an *Erase/Write* command. Both of these commands must specify a device address that is the lowest address in the domain of the control unit.

Execution of the Subsystem Load Enable command causes the attachment to enter the IPL preparatory state. The preparatory state is exited following receipt of the next command, and the new state of the attachment is determined as follows:

1. If the command is an Erase/Write (properly specified), the attachment enters *IPL state*. Refer to "IPL State" in this chapter for additional information.
2. If the command is improperly specified, the attachment terminates IPL preparation and rejects the command. *Unit check* status is returned to the System/370.

IPL State

Execution of the Erase/Write command during an IPL sequence causes the attachment to enter the IPL state. During IPL state, data is transferred from main storage of the System/370 to main storage of the Series/1 (beginning at location 0000 in the Series/1). The IPL record length (total byte count) is specified in the count field associated with the Erase/Write command. The maximum record length is 64K bytes. When all data has been transferred, IPL state is terminated and ending status is presented to the System/370. A *device end* interrupt (CC=3) is presented to the Series/1, using priority interrupt level 0.

If an error occurs during data transfer, the operation is terminated, but the attachment remains in the IPL state. *Unit check* status is presented to the System/370 to indicate the error condition. The System/370 program must then retry the IPL sequence. The attachment rejects any commands other than those necessary for IPL retry.

IPL Retry

If an error occurs during an IPL operation, the System/370 program can retry by initiating the complete IPL command sequence again. This sequence is a Subsystem Load Enable command chained to an Erase/Write command. If the attachment is waiting in the IPL state (due to a previous IPL error), it rejects any other commands from the System/370.

Time-out

The Series/1–System/370 attachment uses an internal timer to establish a time limit (approximately 480 milliseconds) for certain operations, or command sequences. If the time limit is exceeded, one of two time-outs can occur: command time-out or data transfer time-out. The attachment then terminates the operation in process.

Command Time-out

All System/370 "attention" commands require a response from the Series/1. The appropriate command must be received from the Series/1 within the established time limit; otherwise, a time-out occurs. When command time-out occurs, the attachment terminates the operation and presents *unit check* status to the System/370. An attention interrupt is presented to the Series/1, and the time-out bit (bit 5) in the Series/1 interrupt information byte is set to 1.

Data Transfer Time-out

This condition can occur when (1) the two systems are connected and data is being transferred between them, or (2) an IPL record is being transferred from the System/370 to the Series/1. This time-out condition indicates that the transfer time between successive bytes has exceeded the time limit.

When the two systems are connected, this time-out causes the attachment to terminate the operation. *Unit check* status is presented to the System/370. An exception interrupt is presented to the Series/1, and the time-out bit (bit 5) in the Series/1 device status word is set to 1.

During IPL, this time-out causes the attachment to terminate the IPL data transfer and to present *unit check* status to the System/370. The attachment remains in the IPL state; the System/370 must retry the IPL command sequence.

Chapter 3. System/370 Programming Information

The Series/1–System/370 attachment can be cabled to a System/370 selector channel or a block multiplexer channel. The attachment uses one control unit position on the System/370 I/O interface and has 32 device addresses. I/O interface operations are described in detail in the *IBM System/370 Principles of Operations* manual, GA22-7000.

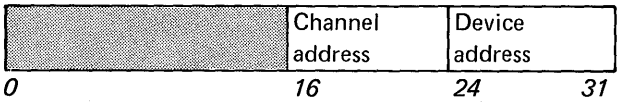
The System/370 program initiates I/O operations by using a Start I/O instruction. This instruction identifies the I/O control unit and device (in this case, the attachment and a device address), and causes the channel to fetch a channel address word (CAW) from a fixed location in main storage. The CAW must contain an address that points to the first channel command word (CCW) that is subsequently fetched by the channel. The CCW specifies the I/O command to be executed plus other necessary information. Once the attachment is selected, the I/O command (CCW bits 0–7) is sent to the attachment. An "initial" status byte is returned to the channel (by the attachment) to indicate if the command can be executed. For operations that involve a transfer of data, the attachment sends the channel a second status byte (called "ending" status) when the operation is terminated. This status indicates either a normal ending or, if errors are detected, an abnormal ending.

System/370 I/O commands that are used by the attachment are explained in a subsequent section of this chapter. Status bytes are explained in "System/370 Status Information" in this chapter. All System/370 I/O instructions are described in the *IBM System/370 Principles of Operation* manual.

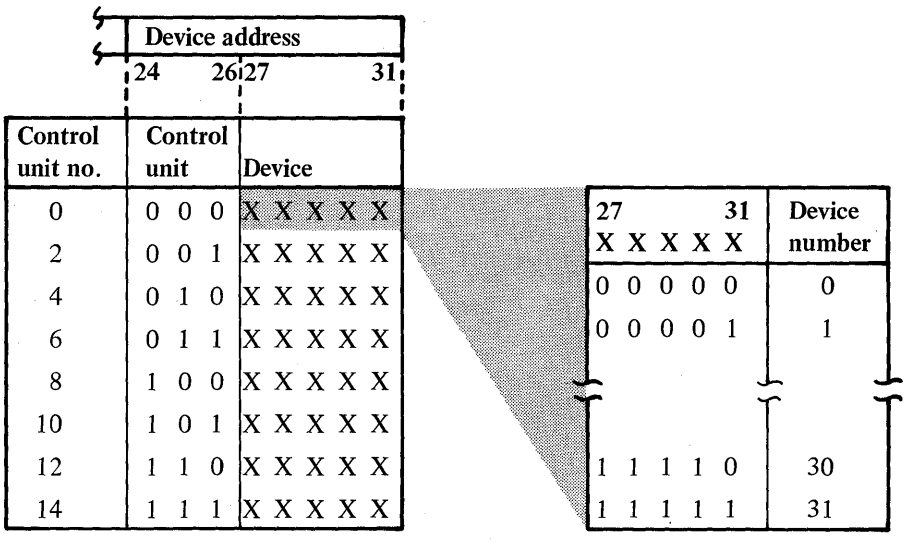
System/370 I/O Addressing

The Series/1–System/370 attachment responds to System/370 I/O instructions in the same manner as a control unit with 32 contiguous device addresses. Device address conventions are explained in the *IBM System/370 Principles of Operation* manual and are presented here as applicable to the attachment.

The System/370 I/O instruction generates an effective address that is used for a channel and device address (instead of a data address). The format is:



For control units with 32 devices, the device address field is interpreted as follows:



Only one device address may be active at a time. A device is in the active state (busy) until the operation is completed and the ending status is accepted by the processor. During this period, the control unit (attachment) is busy if there is an attempt to select any of the other 31 addresses.

The System/370 device address is made available to the Series/1 processor via a Series/1 device status word. The Series/1 program has no need for the control unit addressing bits; therefore, only the five low-order bits (27–31) are contained in the status word.

Device Address Enable and Disable

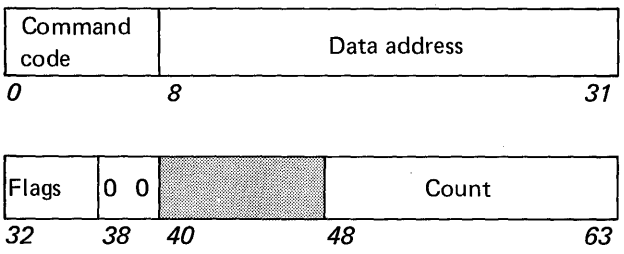
Each of the 32 device addresses has an enable bit (located in the attachment) associated with it. This bit, which controls the ready state of a device address relative to the System/370, is set to 1 to indicate the "ready state" and is set to 0 to indicate the "not ready" state. When a device address is selected and the enable bit is set to 0 (not ready), the attachment returns an initial status of *unit check* to the System/370 for most commands. A sense byte, available to the program, indicates *intervention required.*

The enable bit is set to 1 or 0 under control of the Series/1 program, by two I/O commands: Enable System/370 Device Address and Disable System/370 Device Address. Refer to "Series/1 I/O Commands" in Chapter 4.

Once enabled, a device address remains in that state until (1) a Disable System/370 Device Address command is executed by the Series/1, (2) the attachment is switched off-line to the System/370, or (3) a system reset or power-on reset occurs in the Series/1.

Channel Command Word

The Channel Command Word (CCW) is fetched by the System/370 channel and specifies the information necessary for an I/O operation to be executed. The format is:



The CCW fields or bits that are of special significance to attachment operations are:

Command Code. This field specifies the System/370 I/O operation to be performed. These bits are sent to the attachment when the operation is initiated.

Flags. Bit 32 is the chain-data flag and bit 33 is the chain-command flag. For example, if bit 32 is set to 1, data chaining is specified; if bit 33 is set to 1, command chaining is specified. Command chaining affects attachment operations as explained in "System/370 Chaining" in this chapter. Data chaining is transparent to the attachment.

System/370 I/O Commands

This section describes the following System/370 I/O commands that are used with the attachment:

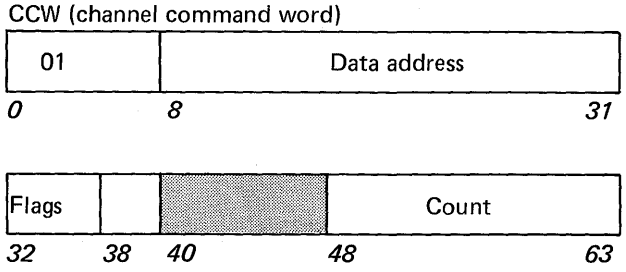
Command code (hex)	*Name*
00	Test I/O
01*	Write
02*	Read Buffer
03	No-Operation
04	Sense
05*	Erase/Write
06*	Read Modified
0B*	Select
0D*	Diagnostic Write
0E*	Diagnostic Read
0F*	Erase All Unprotected
33	Subsystem Load Enable
E4	Sense I/O

* Attention command. These commands cause an attention interrupt to the Series/1 processor. The Series/1 program must respond before a time-out occurs.

Test I/O

The Test I/O command is generated when a Test I/O instruction is directed to the attachment. A channel command word (CCW) is not used by the Test I/O operation. The attachment responds to Test I/O as explained in the *IBM System/370 Principles of Operation* manual.

Write

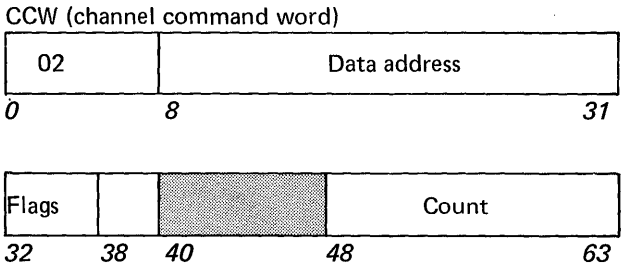


The Write command is used to "connect" the two systems for a data transfer to the Series/1. This command, when issued to the attachment, causes an attention interrupt to the Series/1. The Series/1 must respond with a matching "read operation" in order to establish the connection. Once the connection is established, data is transferred from main storage of the System/370 to main storage of the Series/1. The operation continues until (1) the count goes to 0 in either the Series/1 DCB or the System/370 CCW, (2) an error is detected, or (3) a Series/1 reset occurs.

Unit check initial status is returned to the System/370 if the addressed device is not ready (not enabled).

Write is an attention command and is subject to *command* time-out or *data transfer* time-out.

Read Buffer

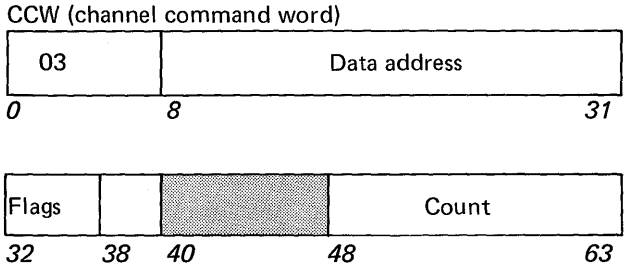


The Read Buffer command is used to "connect" the two systems for a data transfer to the System/370. This command, when issued to the attachment, causes an attention interrupt to the Series/1. The Series/1 must respond with a matching "write operation" in order to establish the connection. Once the connection is established, data is transferred from main storage of the Series/1 to main storage of the System/370. The operation continues until (1) the count goes to 0 in either the Series/1 DCB or the System/370 CCW, (2) an error is detected, or (3) a Series/1 reset occurs.

Unit check initial status is returned to the System/370 if the addressed device is not ready (enabled).

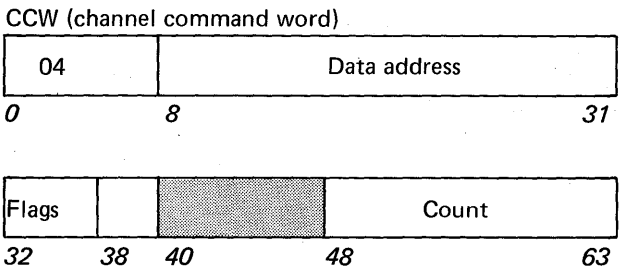
Read Buffer is an attention command and is subject to *command* time-out or *data transfer* time-out.

No-Operation



The No-Operation command performs no functional operation in the attachment, but it may be used to retrieve pending status. No-Operation is an immediate command; therefore, normal ending status is presented as initial status, assuming that the attachment is idle.

Sense



The Sense command CCW must specify a byte count of 1. Execution of this command causes the attachment to transfer one byte of sense data to the System/370. Sense should be issued in response to *unit check* status for further definition of the unit check condition.

Bits in the sense byte are defined as follows:

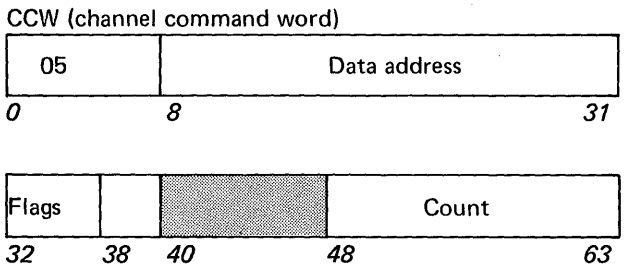
Bit	*Meaning*
0	Command reject
1	Intervention required
2	Bus out check
3	Not used—always 0
4	Data check
5	Unit specify
6	Control check
7	Not used—always 0

Refer to "Sense Data" in this chapter for complete definitions of the sense bits.

The attachment does not provide a separate sense byte for each System/370 device address. Any pending sense data associated with a device address is always cleared (and lost) if a different address is used for the next I/O operation. The sense data is also cleared if any command other than No-Operation, Sense, Sense I/O, or Test I/O is issued to the attachment.

To ensure valid sense data, the Sense command must be issued immediately following receipt of the unit check status, and must use the device address that presented the unit check status.

Erase/Write

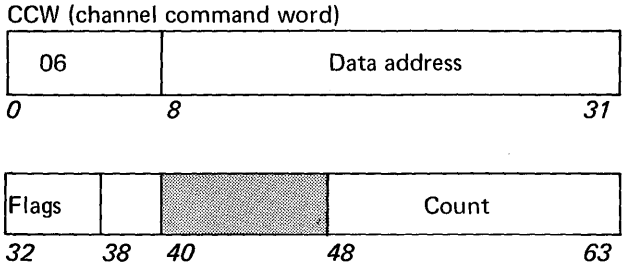


The Erase/Write command can be used for either of two operations:

1. If this command is chained from a Subsystem Load Enable command, it causes an IPL of the Series/1.
2. If this command is not chained from a Subsystem Load Enable command, its operation is identical to that for a Write command.

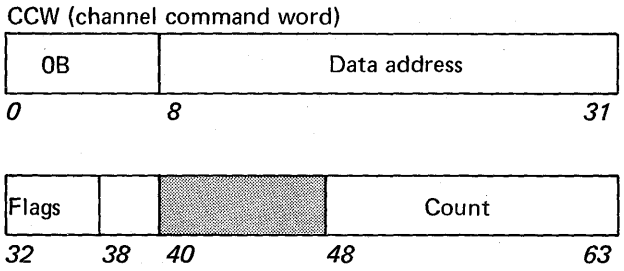
When used for an IPL operation, the CCW for the Erase/Write command must not specify chaining; otherwise, the results are unpredictable. IPL is explained in "System/370 IPL of the Series/1" in Chapter 2.

Read Modified



The Read Modified command functions in the same manner as a Read Buffer command. Refer to "Read Buffer" in this chapter for additional information.

Select



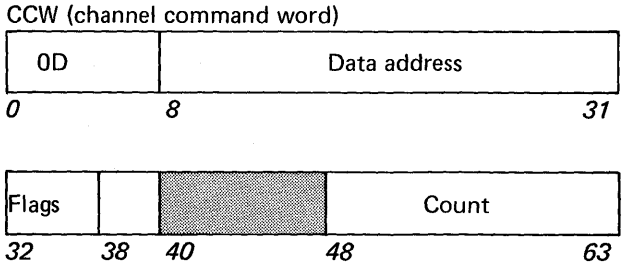
When the Select command is issued, the Series/1 program must respond with a Set System/370 Device End command. The initial status returned to the System/370 by the attachment contains *channel end.*

Execution of the Set System/370 Device End command causes an interrupt to the System/370 with a status byte that contains *device end.*

Unit Check initial status is returned to the System/370 if the addressed device is not ready (not enabled).

Select is an attention command and is subject to *command* time-out.

Diagnostic Write

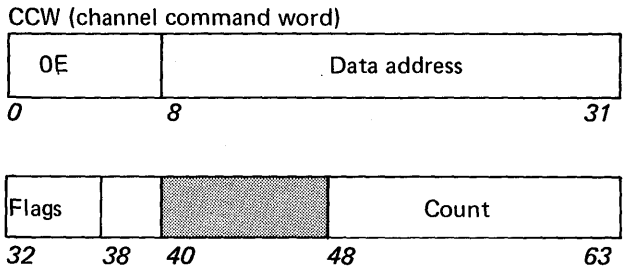


The Diagnostic Write command is used for diagnostic purposes and should only be used by a diagnostic program in the System/370. Its operation is identical to that for a Write command.

The Series/1 program can distinguish between a normal write operation and a diagnostic write operation by checking bits 13–15 of the Series/1 device status word.

Diagnostic Write is an attention command and is subject to *command* time-out or *data transfer* time-out.

Diagnostic Read

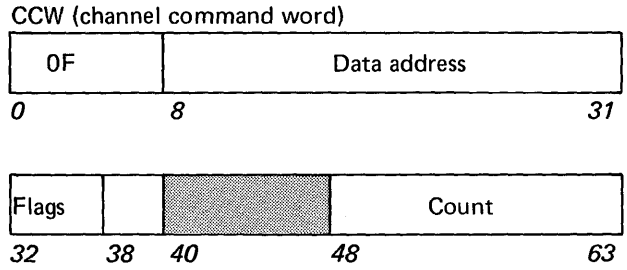


The Diagnostic Read command is used for diagnostic purposes and should only be used by a diagnostic program in the System/370. Its operation is identical to that for a Read Buffer command.

The Series/1 program can distinguish between a normal read operation and a diagnostic read operation by checking bits 13–15 of the Series/1 device status word.

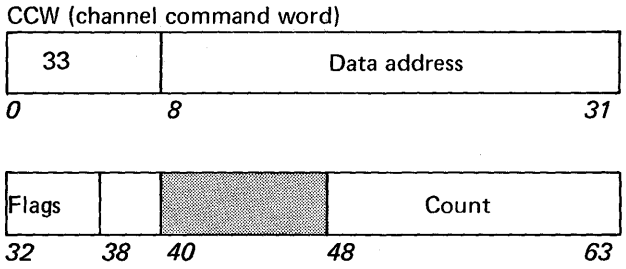
Diagnostic Read is an attention command and is subject to *command* time-out or *data transfer* time-out.

Erase All Unprotected



Operation of the Erase All Unprotected command is identical to that for a Select command. Refer to "Select" command in this chapter for additional information.

Subsystem Load Enable



The Subsystem Load Enable command prepares the attachment for IPL from the System/370. This command is executed when all of the following conditions are met:

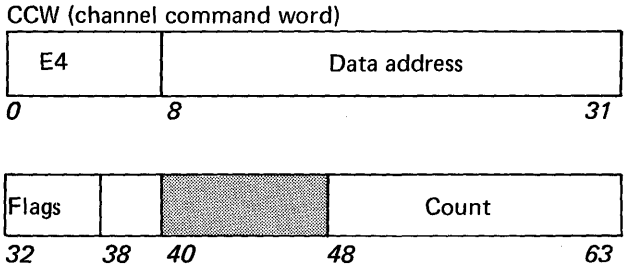
- The attachment is on-line.
- The specified device address is the lowest address in the domain of the control unit.
- The inhibit IPL jumper is removed from the attachment card.

The initial status, returned to the System/370, indicates *channel end* and *device end*.

Note: This command should be chained to an Erase/Write Command. The IPL begins when the Erase/Write command is executed. Refer to "System/370 IPL of the Series/1" in Chapter 2.

If the Subsystem Load Enable command is chained to a command other than Erase/Write, the second command is rejected and IPL does not occur; the complete IPL sequence must be restarted.

Sense I/O



The Sense I/O command CCW must specify a byte count of 4. Execution of this command causes the attachment to transfer four bytes of sense data to the System/370. This data provides information about the Series/1 processor and indicates the condition (installed or not installed) of the inhibit IPL jumper.

The Sense I/O command can be directed to any device address in the domain of the control unit.

The four bytes of data are:

Byte	*Data (hex)*
0	FF
1	49
2	50
3	0X

X = 0 Inhibit IPL jumper installed
X = 1 Inhibit IPL jumper not installed

Refer to "Sense Data" in this chapter for additional information.

System/370 Chaining

When the channel has completed the operation specified by a CCW, it can continue the activity initiated by a Start I/O instruction by fetching a new CCW. Such fetching of a new CCW is called chaining, and the CCWs belonging to such a sequence are said to be chained.

Two types of chaining can be specified in the current CCW: data chaining or command chaining. Bits 32 and 33 of the CCW flag field are used for this purpose.

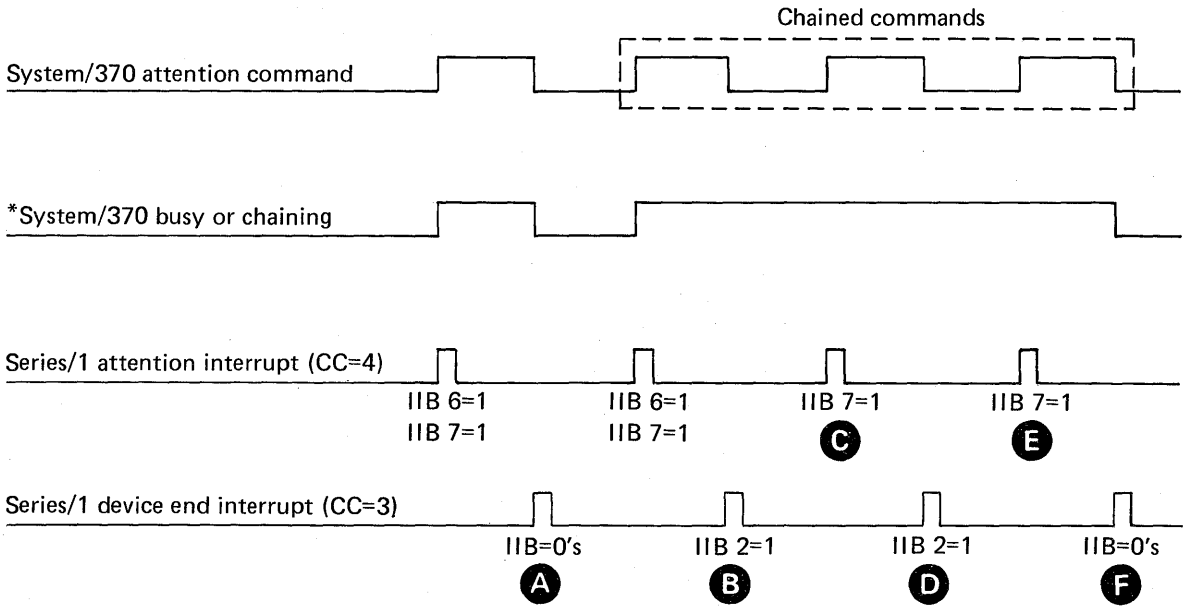
CCW bit		
32	*33*	*Type*
1	0	Data chaining
0	1	Command chaining

Data chaining is transparent to the Series/1–System/370 attachment. When chaining is referred to during attachment operations, the reference is to command chaining. During command chaining, each CCW initiates a new operation by specifying a new command and data address. Additional information about command chaining is contained in the *IBM System/370 Principles of Operation* manual.

Chaining conditions are reported to the Series/1 program via bits in the interrupt information byte (IIB). Bits 2, 6, and 7 are used for this purpose, as shown in Figure 3-1. Note that when chaining is indicated in the IIB (bit 2 is set to 1), the Series/1 program can refer to the previous IIB (bits 6 and 7) for further definition of the chaining condition. Refer to "Interrupt Information Byte (IIB)" in Chapter 4 for a complete definition of the IIB bits.

The chaining conditions shown in Figure 3-1 are explained as follows:

- (A) Chaining is not indicated (IIB 2 = 0). The previous IIB has no chaining significance.
- (B) Chaining to the next command is indicated. The previous IIB indicates the beginning of a new chain.
- (C) This command is a continuation of chaining.
- (D) Chaining to the next command is indicated. The previous IIB indicates a continuation of chaining.
- (E) This command is a continuation of chaining.
- (F) Further chaining is not indicated.



*Indicated by Series/1 device status word bit 2

Note: If attention and device end are presented together (CC=7), the IIB bits are ORed

Figure 3-1. System/370 chaining conditions.

When chaining is in effect, the Series/1 program must respond to each new command in the chain in the same manner as it would to unchained commands. Normal termination of chaining occurs when the operation specified by the last CCW in the chain is completed. Abnormal termination of the chaining sequence can occur if the attachment detects a condition that causes a System/370 unit check (for example, a Series/1 error or a time-out).

System/370 Status Information

This section presents the System/370 status information relating to the Series/1–System/370 attachment feature. Status information consists of:

- Condition codes
- Sense data
- Status byte

Condition Codes

During execution of an I/O instruction the System/370 channel returns one of four condition codes to the processor. This code indicates that the channel has performed the instruction or, if not, the reason for rejection. In most cases, the channel checks an "initial" status byte returned by the attachment in order to set the proper condition-code value. The condition codes are fully explained in the *IBM System/370 Principles of Operation* manual. A condition code chart (Figure 3-2) is included in this chapter for reference. Refer to "Status Byte" in this chapter for additional information about the initial status byte.

Input/output instruction	Condition code			
	0	1	2	3
Clear I/O	No operation in progress	CSW stored	Channel busy	Not operational
Halt Device	Interrupt pending, or busy	CSW stored	Channel working	Not operational
Halt I/O	Interrupt pending	CSW stored	Burst op. stopped	Not operational
Start I/O	Successful	CSW stored	Busy	Not operational
Start I/O Fast Release	Successful	CSW stored	Busy	Not operational
Store Channel ID	ID stored	CSW stored	Busy	Not operational
Test Channel	Available	Interrupt pending	Burst mode	Not operational
Test I/O	Available	CSW stored	Busy	Not operational

Figure 3-2. System/370 condition codes for I/O instructions

Sense Data

Two System/370 commands cause a transfer of "sense" data from the attachment to the System/370 processor: *Sense* and *Sense I/O*.

Data for a Sense Command

The sense command causes one byte of data to be transferred to the System/370. Bits within the byte are defined as follows:

Bit	*Meaning*
0	*Command reject*. This bit is set to 1 if any of the following conditions are detected: • An invalid System/370 command is issued to the attachment. • A Subsystem Load Enable command is issued and the inhibit IPL jumper is installed, or the device address is incorrect. • An improper command is issued following a Subsystem Load Enable command. *Note:* An improper command is any command other than Erase/Write, or an Erase/Write command that is not chained from the Subsystem Load Enable. • A command not involved in "IPL retry" is issued when the attachment is in the IPL state. IPL state and IPL retry are explained in "System/370 IPL of the Series/1" in Chapter 2.
1	*Intervention required*. This bit is set to 1 if a command (other than those noted) is issued to the attachment and the addressed device is not ready. *Note:* Exceptions are the Sense, Sense I/O, Subsystem Load Enable, and Erase/Write (when used for IPL) commands.
2	*Bus out check*. This bit is set to 1 if the attachment detects bad parity on any command byte or data byte received from the System/370 channel.
3	*Unused*. Always zero.
4	*Data check*. This bit is set to 1 when a Series/1 error (storage error or command mismatch) is detected during execution of a command involving the Series/1.
5	*Unit specify*. This bit is set to 1 under the same condition as bit 4 (data check).
6	*Control check*. This bit is set to 1 when the attachment detects a time-out condition due to (1) excessive time between data transfers, or (2) excessive time for the Series/1 response to a System/370 attention command.
7	*Unused*. Always zero.

After execution of a Sense command, all bits are set to 0's.

Data for a Sense I/O Command

The Sense I/O command causes four bytes of data to be transferred to the System/370. This data represents (1) a Series/1 identification number, and (2) the condition of the inhibit IPL jumper on the attachment feature card.

Inhibit IPL jumper installed.

Byte	0	1	2	3
Data (hex)	FF	49	50	00

Inhibit IPL jumper not installed.

Byte	0	1	2	3
Data (hex)	FF	49	50	01

Bytes 0, 1, and 2 contain the Series/1 identification number. Byte 3 indicates the condition of the inhibit IPL jumper.

Status Byte

The attachment generates a status byte to inform the System/370 channel of certain attachment and device conditions. This status byte can be generated synchronously (while the attachment is selected and performing a command operation with the channel) or asynchronously (while the attachment is not selected). Synchronous status is passed to the channel as both "initial status" and "ending status" to a command. Asynchronous status reflects (1) ending status for certain commands, (2) an action that requires program intervention, or (3) an equipment malfunction.

Under certain conditions, the attachment status byte is presented to the System/370 processor as part of the channel status word (CSW). CSW bits 32–39 contain the status byte from the channel.

Bits within the status byte are:

Status bit	*CSW bit*	*Name*
0	32	Attention (A)
1	33	Status modifier (SM)
2	34	Control unit end (CUE)
3	35	Busy (B)
4	36	Channel end (CE)
5	37	Device end (DE)
6	38	Unit check (UC)
7	39	Unit exception (UE)

For Series/1–System/370 attachment operations, the bits are defined as follows:

Attention. This bit is set to 1 when a Set Attention to System/370 command is executed by the Series/1. Attention is always presented as asynchronous status.

Status Modifier. This bit is set to 1 (with the busy bit) in initial status to indicate control unit (attachment) busy. This means that the attachment has pending status for a device other than the one selected.

Control Unit End. This bit is set to 1 to indicate that a previously reported busy condition (control unit busy) has been cleared and that the attachment is now free to execute a new command.

Busy. This bit is set to 1 and presented alone in initial status when the addressed device is busy. This indicates that (1) the device has pending status and the present command is not Test I/O, or (2) the device is executing an Erase All Unprotected command or a Select command.

The busy bit is set to 1 and presented with the status modifier bit to indicate control unit busy.

Channel End. This bit is set to 1 to indicate that all data transfers are complete. It is normally presented as synchronous status.

If channel end status is pending when the device operation is completed, it is presented (with the device end bit) as asynchronous status.

Device End. This bit is set to 1 to indicate that the attachment has completed the specified operation and is now free to execute a new command.

Unit Check. This bit is set to 1 when an irregular program condition or equipment condition is detected by the attachment. Sense data in the attachment further defines the unit check condition. Refer to "Data for a Sense Command" in this chapter.

Unit Exception. This bit is not used by the attachment; it is always 0.

Initial Status

Initial status is generated by the attachment in response to initial selection from the System/370. During the initial-selection sequence, the status is sent to the channel after the attachment receives a command. Figure 3-3 shows the normal status for each System/370 command used by the attachment.

Ending Status

When the attachment completes channel operations for a command, it sends ending status to the channel. Ending status indicates that the channel is now free for other operations. Figure 3-3 shows the normal status for each command.

System/370 command	Normal status					
	Initial		Ending			
			Synchronous		Asynchronous	
	Hex	Bits set to 1	Hex	Bits set to 1	Hex	Bits set to 1
Test I/O	*					
Write	00		08	CE	04	DE
Read Buffer	00		0C	CE, DE		
No-Operation	0C	CE, DE				
Sense	00		0C	CE, DE		
Erase/Write	00		08	CE	04	DE
Read Modified	00		0C	CE, DE		
Select	08	CE			04	DE
Diagnostic Write	00		08	CE	04	DE
Diagnostic Read	00		0C	CE, DE		
Erase All Unprotected	08	CE			04	DE
Subsystem Load Enable	0C	CE, DE				
Sense I/O	00		0C	CE, DE		

CE – Channel end
DE – Device end
* – Any pending status or 00

Figure 3-3. Normal status byte for System/370 commands

Pending Status

When a status byte is awaiting transfer to the channel, it is called "pending status." The attachment attempts to pass this status asynchronously to the channel. If the status byte is still pending when the next command is issued, it is passed to the channel as initial status, and the new command is not executed. In this case, the busy bit in the status byte is also set to 1.

System/370 Interface Disconnect

Under certain conditions, the System/370 channel can initiate an interface disconnect sequence. The attachment responds immediately by terminating any operation in process. Normal ending status is presented to the System/370 channel.

If the disconnect occurs when the Series/1 is connected to the System/370, an exception interrupt is presented to the Series/1. If the two systems are not connected, an attention interrupt is presented to the Series/1.

Interface disconnect is described in the *IBM System/360 and System/370 Interface Channel to Control Unit Original Equipment Manufacturers' Information* manual, GA22-6974.

System/370 Reset

The System/370 reset is caused by either an I/O system reset or an I/O selective reset as described in the *IBM System/370 Principles of Operation* manual. This reset causes a reset of the System/370 section of the attachment.

If the reset occurs when the Series/1 is connected to the System/370, an exception interrupt is presented to the Series/1. If the two systems are not connected, an attention interrupt is presented to the Series/1.

Chapter 4. Series/1 Programming Information

The Series/1-System/370 attachment, when attached to the Series/1 I/O channel, appears as a cycle-stealing device, which means that cycle-steal mode is used for certain data-transfer operations. Other operations use direct program control (DPC) mode. I/O commands that initiate cycle-steal operations are: *Start*, *Start Diagnostic*, and *Start Cycle Steal Status*. All other I/O commands initiate DPC operations. The I/O commands are fully explained in subsequent sections of this chapter. Refer to the appropriate Series/1 processor description manual for additional information about cycle-steal and DPC operations.

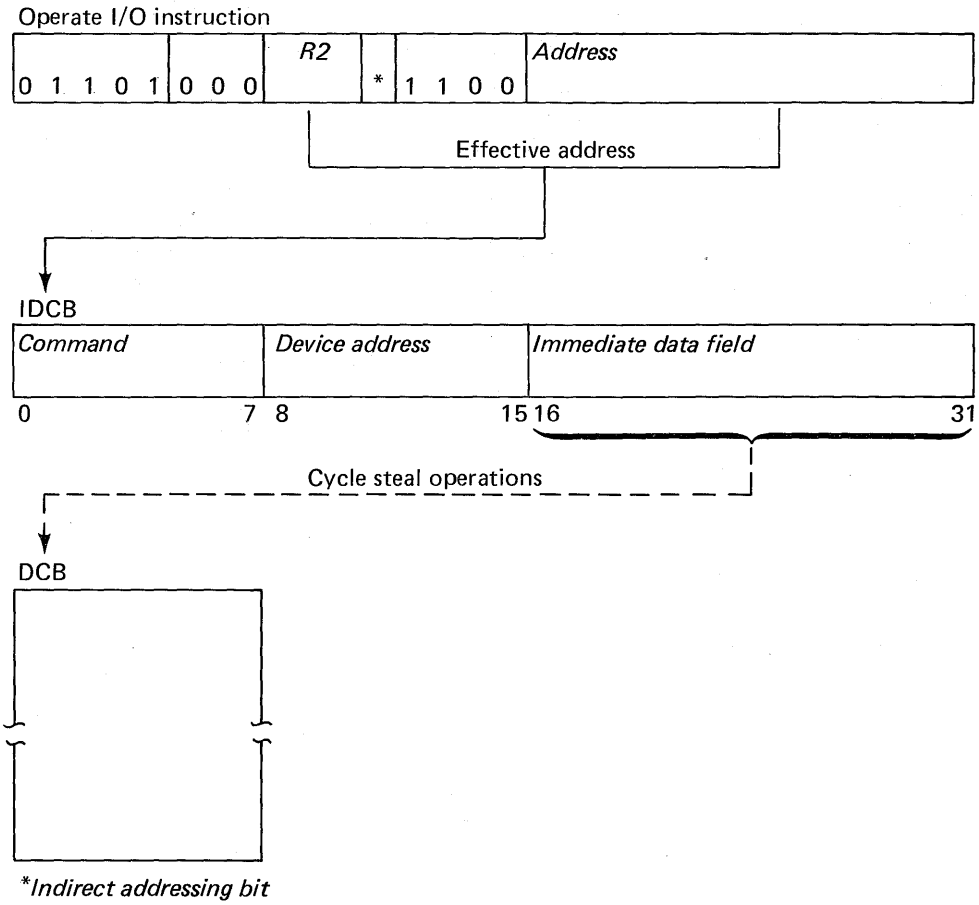
Series/1 I/O Addressing

The attachment responds to one Series/1 device address. This address can be within the range of 0–255 (00–FF hex) and is established by installing the appropriate connectors on the attachment feature card.

Operate I/O (IO) Instruction

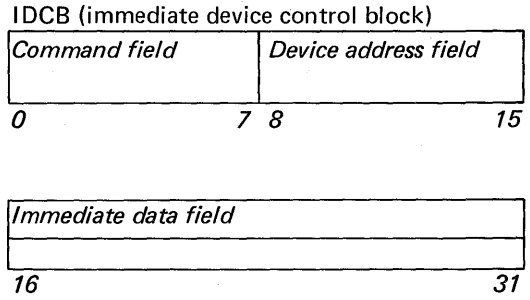
The Operate I/O instruction is used by the Series/1 processor to initiate I/O operations in the Series/1 section of the attachment. Typical operations such as "read" and "write" must be initiated when data is to be transferred to or from the System/370. The Operate I/O instruction generates an effective address that points to an immediate device control block (IDCB) in processor storage. The IDCB consists of two words that contain an I/O command, a device address (the attachment address), and an immediate data field. For DPC operations, the immediate data field is used as a device data word. For cycle-steal operations, the immediate data field points to a device control block (DCB) that provides additional information needed for the operation.

The IDCB and the DCB are explained in the following paragraphs. For more details of the *Operate I/O Instruction* refer to the appropriate Series/1 processor description manual.



Immediate Device Control Block (IDCB)

An IDCB is required for each Operate I/O instruction issued by the processor. The format of the IDCB is:



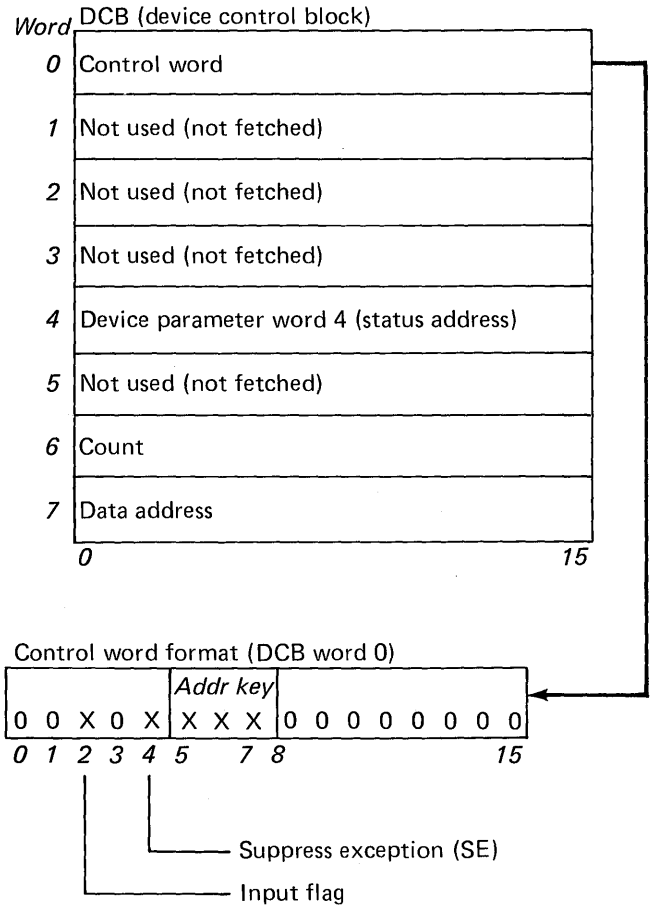
The fields within the IDCB must contain the proper data in order to initiate the required I/O operation. The immediate data field in the IDCB contains a data word, a DCB address, or 0's, depending on the I/O command. "Series/1 I/O Commands" in this chapter describes each command and its associated IDCB.

Device Control Block (DCB)

A DCB, comprised of eight contiguous words, is used for each cycle-steal operation. The DCB is pointed to by the IDCB immediate data field when a cycle-steal command is used. The commands that cause the attachment to fetch a DCB from processor storage are:

- Start
- Start Diagnostic
- Start Cycle Steal Status

The DCB must contain the proper information before it is fetched by the attachment, which uses the cycle-steal mechanism to fetch the DCB. The attachment does not use the extended DCB formats; only the standard format (as explained in this chapter) is used.



The DCB words that are used by the attachment have the following meanings:

Control Word

Bit 0* *Zero*. If this bit is set to 1, the attachment reports a *DCB specification check*.

Bit 1* *Zero*. If this bit is set to 1, the attachment reports a *DCB specification check*.

Bit 2 *Input flag*. The setting of this bit informs the attachment of the direction of data transfer.
0 = Output (Series/1 main storage to the attachment).
1 = Input (attachment to Series/1 main storage).

Bit 3* *Zero*. If this bit is set to 1, the attachment reports a *DCB specification check*.

Bit 4* *Suppress exception (SE)*. This bit, when set to 1, allows the attachment to suppress reporting an incorrect length record to the Series/1 processor, and also causes the attachment to store a residual status block. Refer to "Residual Status Block" in this chapter for additional information. This bit must be 0 for a Start Diagnostic command or a Start Cycle Steal Status command; otherwise, the attachment reports a *DCB specification check*.

Bits 5–7 *Cycle steal address key*. The attachment presents this key (to the processor) during data transfers. Some processors use this key as either a storage protect or a storage access key.

Bits 8–15 *Zeros*. These bits must be set to 0's to avoid future code obsolescence.

*DCB errors are not reported to the processor by a Start Diagnostic command.

Device Parameter Word 4

Device parameter word 4 is fetched by the attachment for all Start commands. It is not used (or fetched) for Start Diagnostic and Start Cycle Steal Status commands. This word is used in different ways for Start commands depending on the setting of the SE bit (bit 4) in the DCB control word.

SE bit = 0. Word 4 is fetched and checked for parity, but is not used by the attachment.

SE bit = 1. Word 4 is fetched and must contain a main storage address on an even-byte boundary. This address is called the *status address* and informs the attachment of the location to store a residual status block following completion of the DCB operation.

Count

The count word contains the number of data bytes to be transferred for this DCB. For a Start command, the count can be 0–65,535. For a Start Diagnostic command, the count must be 4. For a Start Cycle Steal Status command, the count must be 8. If an incorrect count is specified, the attachment reports a *DCB specification check.*

Data Address

The data address word contains the starting main storage address for the data transfer.

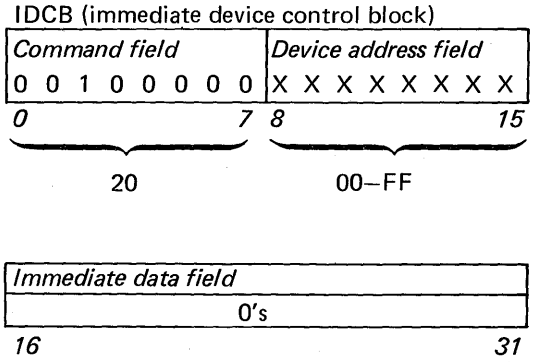
Series/1 I/O Commands

This section describes the Series/1 I/O commands that are used by the attachment. Some commands are unique to the attachment and can cause additional condition codes and/or other status information to be reported to one or both processors. Each command description also contains a brief description of this additional status information. Refer to "System/370 Status Information" in Chapter 3 or "Series/1 Status Information" in this chapter for details.

The attachment responds to the following I/O commands from the Series/1 processor:

Command code (hex)	*Name*
20	Read ID
21	Read Status
60	Prepare
62	Disable System/370 Device Address
63	Enable System/370 Device Address
64	Set System/370 Device End
65	Set Attention to System/370
6F	Device Reset
70	Start
71	Start Diagnostic
7F	Start Cycle Steal Status
F0	Halt I/O

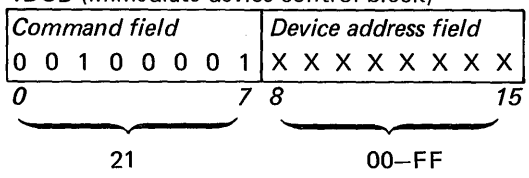
Read ID

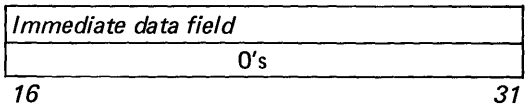


Execution of the Read ID command causes a unique identification word to be transferred from the attachment to the data field of the IDCB. For the Series/1–System/370 attachment, the ID word is 4002 (hex).

Read Status

IDCB (immediate device control block)





The Read Status command causes a 16-bit device status word to be transferred from the attachment to the data field of the IDCB. The bits in the status word are:

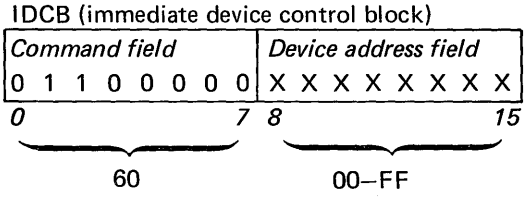
Bit	*Name*
0	Unused—always 0
1	On-line
2	System/370 busy or chaining
3	System/370 reset
4	System/370 interface disconnect
5	Time-out
6	System/370 error
7	Attention command
8–12	System/370 device address
13–15	System/370 command

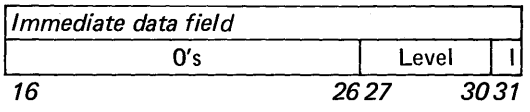
Refer to "Device Status Word" under "Series/1 Status Information" in this chapter for a detailed description of the bits.

Note: This status word is identical to the status word (word 3) transferred to the Series/1 processor when a *Start Cycle Steal Status* command is executed.

Prepare

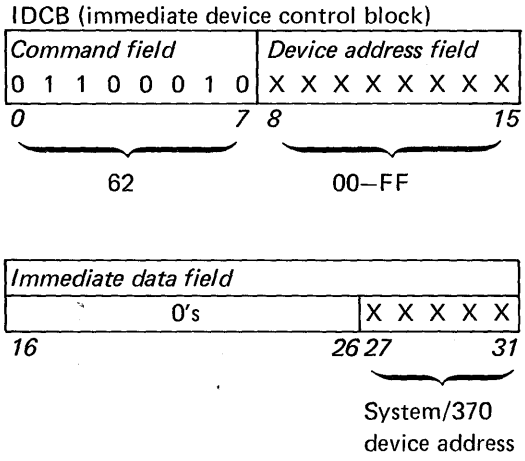
IDCB (immediate device control block)





The Prepare command transfers the IDCB data word to the prepare register in the attachment. The binary value of the level field (bits 27–30) is used to assign a priority interrupt level to the attachment. For example, 0000 = level 0, 0001 = level 1, 0010 = level 2, and 0011 = level 3. The I-bit (bit 31) is a device interrupt mask. If the I-bit equals 1, the attachment can interrupt the Series/1 processor; if the I-bit equals 0, the attachment cannot interrupt.

Disable System/370 Device Address

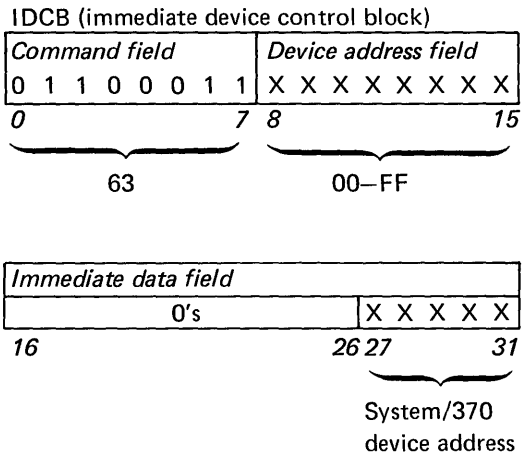


The Disable System/370 Device Address command causes the specified System/370 device address to become unavailable to command selection from the System/370. The command disables the device address by setting the appropriate "enable" bit to 0. The System/370 device address is specified in bits 27–31 of the IDCB. Note that only the five low-order bits of the address are specified. Bits 16–26 of the IDCB are not used, and must be set to 0 to avoid future code obsolescence. Refer to "Device Address Enable and Disable" in Chapter 3 for additional information.

Execution of this command does not cause an interrupt to the Series/1 processor or the System/370 processor.

Command reject (CC=3) is reported if a System/370 chaining sequence is in process (with the attachment) and the Series/1 is not involved in the sequence.

Enable System/370 Device Address



The Enable System/370 Device Address command causes the specified System/370 device address to become available for execution of commands from either processor. The enable bit corresponding to the device address is set to 1 (enabled state). The five low-order bits of the System/370 device address are specified in bits 27–31 of the IDCB. Bits 16–26 of the IDCB are not used, and must be set to 0's to avoid future code obsolescence. Refer to "Device Address Enable and Disable" in Chapter 3 for additional information.

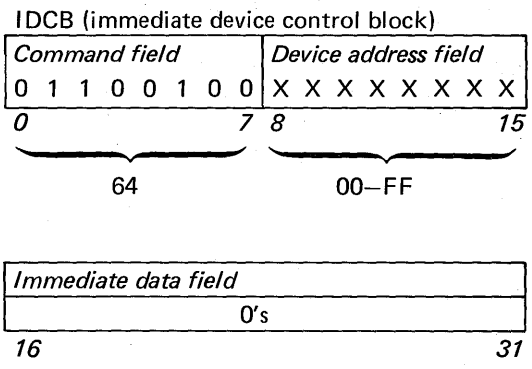
When the attachment is on-line to the System/370 and this command is executed, the following events also occur:

1. An interrupt (with device end status) is presented to the System/370 processor. Note that a System/370 I/O interrupt automatically stores the System/370 device address into processor storage. If the bit is already enabled, this interrupt is not generated.
2. Once the System/370 accepts the interrupt, or if the device address is already enabled, a device end interrupt (CC=3) is presented to the Series/1 processor.

Intervention required (CC=4) is reported if the attachment is off-line to the System/370.

Command reject (CC=3) is reported if a System/370 chaining sequence is in process (with the attachment) and the Series/1 is not involved in the sequence.

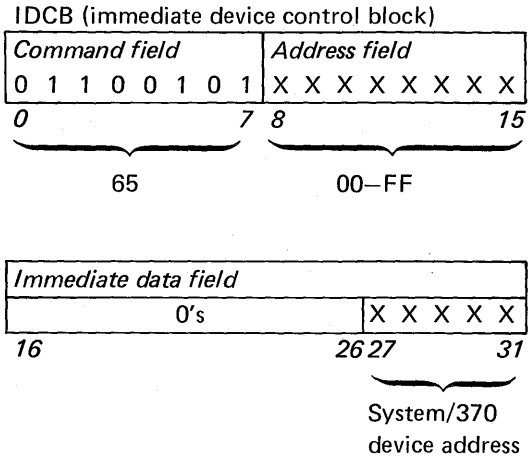
Set System/370 Device End



Execution of the Set System/370 Device End command causes the attachment to generate an interrupt (with device end status) to the System/370. The command is executed only in response to a Series/1 attention interrupt caused by a System/370 "Select" or "Erase All Unprotected" command; otherwise, *command reject* (CC=3) is reported. The data field of the IDCB is unused, but it is checked for parity. The data field should be set to 0 to avoid future code obsolescence.

Intervention required (CC=4) is reported when the attachment is off-line to the System/370.

Set Attention to System/370



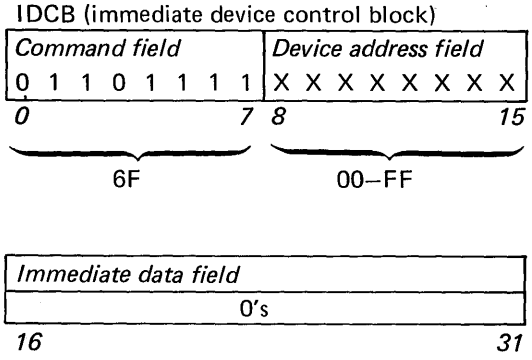
The Set Attention to System/370 command causes an interrupt (with attention status) to the System/370. After completion of the System/370 interrupt, a device end interrupt (CC=3) is presented to the Series/1.

Bits 27–31 of the IDCB specify the System/370 device address and, therefore, the source of the interrupt. Bits 16–26 of the IDCB are unused, and must be set to 0's to avoid future code obsolescence.

Command reject (CC=3) is reported if (1) the specified System/370 device address is not enabled, or (2) a System/370 chaining sequence is in process (with the attachment) and the Series/1 is not involved in the sequence.

Intervention required (CC=4) is reported when the attachment is off-line to the System/370.

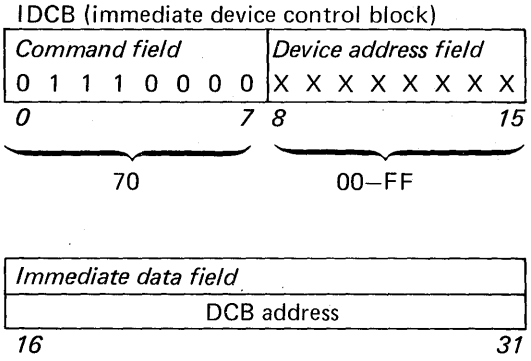
Device Reset



The Device Reset command causes all controls, status, and pending interrupts in the Series/1 section of the attachment to be reset. The prepare register *is not* reset. Bits 16–31 of the IDCB are unused, and should be set to 0's to avoid future code obsolescence.

If the two systems are "connected", any operation between them is terminated. An interrupt (with unit check status) is presented to the System/370 to signal the termination. Refer to "Series/1 Resets" in this chapter for additional information.

IDCB (immediate device control block)



The Start command is used by the Series/1 program to "connect" to the System/370. The connection must be established when the System/370 initiates a storage-to-storage data transfer.

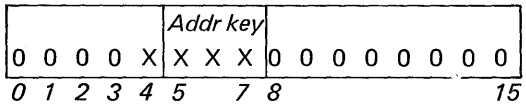
The Start command initiates a cycle steal operation between the attachment and the Series/1 processor. The second word of the IDCB must contain a 16-bit main storage address that points to a DCB. The DCB is fetched by the attachment and contains additional information about the type of operation to be performed. Refer to "Series/1 Write Operation" and "Series/1 Read Operation" in this chapter for additional information.

The Start command is not accepted by the attachment unless a System/370 read-type or write-type command has been previously accepted and is pending. If a System/370 read-type or write-type command is not pending, *command reject* (CC=3) is reported and the DCB is not fetched.

Intervention required (CC=4) is reported when the attachment is off-line to the System/370.

Series/1 Write Operation

A DCB specifying a Series/1 write operation is used to match a System/370 Read Buffer, Read Modified, or Diagnostic Read command. The DCB control word is:

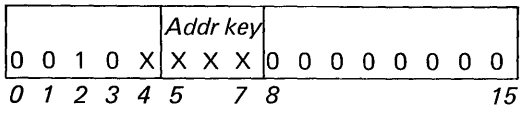


Once the two systems are connected, data is transferred from Series/1 main storage to System/370 main storage. Normal termination for the data transfer occurs when the DCB count reaches 0. Refer to "Start Command Termination" in this chapter for termination conditions.

If a "write" DCB is fetched and a matching System/370 read command is not present, the operation is terminated. An exception interrupt (CC=2) is reported to the Series/1. Bit 0 in the interrupt status byte is set to 1. Ending status (containing channel end, device end, and unit check) is reported to the System/370. Bit 4 in the System/370 sense byte is set to 1.

Series/1 Read Operation

A DCB specifying a Series/1 read operation is used to match a System/370 Write, Erase/Write, or Diagnostic Write command. The DCB control word is:



Once the two systems are connected, data is transferred from System/370 main storage to Series/1 main storage. Normal termination for the data transfer occurs when the DCB count reaches 0. Refer to "Start Command Termination" in this chapter for additional information.

If a "read" DCB is fetched and a matching System/370 write command is not present, the operation is terminated. An exception interrupt (CC=2) is reported to the Series/1. Bit 0 in the interrupt status byte is set to 1. Ending status (containing channel end, device end, and unit check) is reported to the System/370. Bit 4 in the System/370 sense byte is set to 1.

Start Command Termination

Normal Ending. The DCB count reaches 0 before System/370 channel end occurs. The operation is terminated; channel end and device end status are reported to the System/370. A device end interrupt (CC=3), with an interrupt information byte of 0's, is reported to the Series/1.

Incorrect Length Record (ILR). Termination of data transfer occurs on the System/370 when the DCB count is not 0. An exception interrupt (CC=2) is reported to the Series/1; the ILR bit (bit 2) in the interrupt status byte is set to 1.

Note: This error is suppressed if the suppress exception bit (bit 4) of the DCB control word is set to 1.

Series/1 Error. An error is detected between main storage of the Series/1 and the attachment. The data transfer is terminated; channel end, device end, and unit check status are reported to the System/370. An exception interrupt (CC=2) is reported to the Series/1; the interrupt status byte contents identify the error.

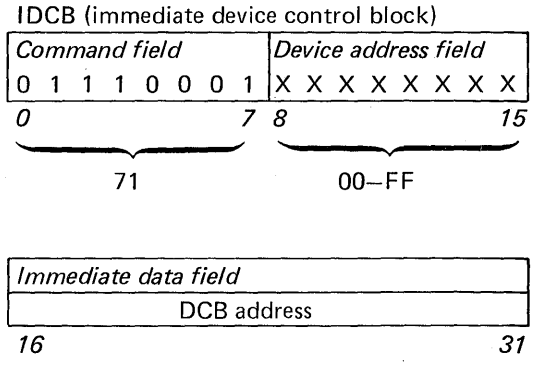
Time-out. The amount of time between successive data transfers exceeds approximately 480 milliseconds. A data transfer time-out occurs. An exception interrupt (CC=2) is reported to the Series/1. Bit 0 of the interrupt status byte set to 1 (indicating device dependent status available).

System/370 Reset. A System/370 reset causes the operation to be terminated. An exception interrupt (CC=2) is reported to the Series/1. Bit 0 of the interrupt status byte set to 1 (indicating device dependent status available).

Interface Disconnect. An interface disconnect sequence occurs on the System/370 channel. An exception interrupt (CC=2) is reported to the Series/1. Bit 0 of the interrupt status byte set to 1 (indicating device dependent status available).

System/370 Error. This termination condition does not apply to a write operation. An error is detected between main storage of the System/370 and the attachment. An exception interrupt (CC=2) is reported to the Series/1. Bit 0 of the interrupt status byte set to 1 (indicating device dependent status available).

Start Diagnostic

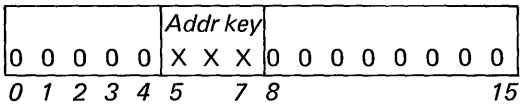


This command is used to exercise internal operations in the attachment and to verify (1) attachment data flow from/to main storage, and (2) presentation of interrupts. The attachment must be off-line to the System/370 when this command is issued, otherwise, *intervention required* (CC=4) is reported to the processor.

The DCB used with this command can specify a "write" or a "read" operation and must specify a count of 4. Any DCB error is considered to be a diagnostic error condition.

Write Diagnostic Operation

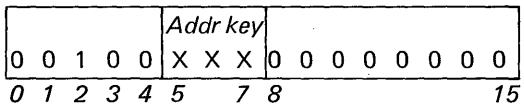
The DCB control word for the Write Diagnostic operation is:



Four bytes of data are transferred from main storage to a diagnostic buffer in the attachment. The beginning main storage address must be specified in DCB word 7. Internal operations in the attachment are cycled and checked for errors and, if no error is detected, the operation terminates with an exception interrupt (CC=2) reported to the processor. The device status word indicates a time-out (bit 5 set to 1). Total time for the write diagnostic operation is approximately 500 msec assuming that there are (1) no errors and (2) no other I/O activity on the Series/1 channel. Refer to "Diagnostic Operation Error Conditions" in this chapter for information about detected errors.

Read Diagnostic Operation

The DCB control word for the Read Diagnostic operation is:

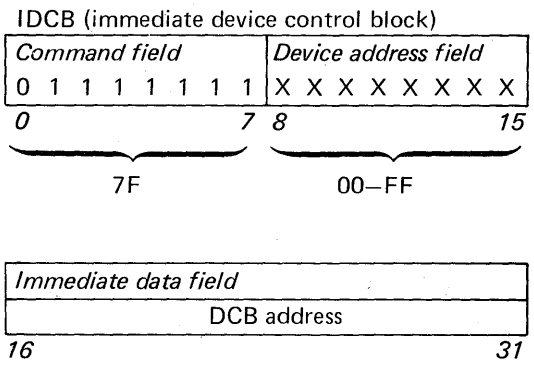


Four bytes of data are transferred from the diagnostic buffer (in the attachment) to main storage. The beginning main storage address must be specified in DCB word 7. If this operation is immediately preceded by a write diagnostic operation, the inverted write-operation data is returned to the Series/1 with the exception of the last 12 bits. These 12 bits should be ignored. Attachment operations are checked for errors, and, if no errors occur, the operation terminates with a device end interrupt (CC=3) reported to the processor. Refer to "Diagnostic Operation Error Conditions" in this chapter for additional information.

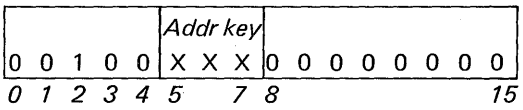
Diagnostic Operation Error Conditions

The diagnostic operations include error checking of internal operations and data flow, but the attachment does not report these error conditions to the Series/1 processor. Any internal errors detected by the attachment, after the IDCB is accepted, cause the attachment to remain busy. The busy condition can be cleared by any Series/1 reset.

Start Cycle Steal Status



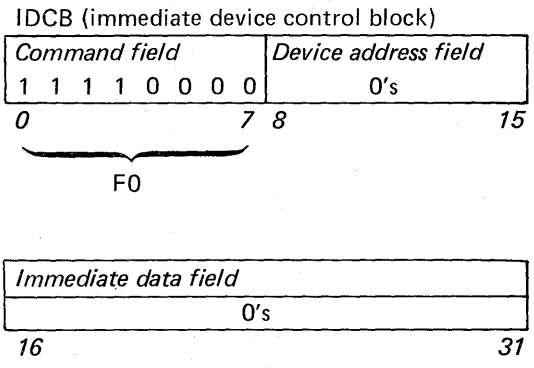
The Start Cycle Steal Status command initiates a cycle-steal operation that transfers eight bytes (four words) of data from the attachment to main storage. The DCB control word is:



DCB word 6 must specify a count of 8. DCB word 7 specifies the starting main storage address for the data.

Refer to "Cycle-Steal Status Words" in this chapter for a description of the eight bytes of data.

Halt I/O



The Halt I/O command, which is directed to the Series/1 channel, causes a halt of all I/O activity on the channel and resets any pending interrupts. The prepare register in the attachment is not reset. Bits 8–31 of the IDCB are not used, but should be set to 0's. The channel returns IO instruction condition code 7 to the Series/1 processor.

Series/1 Status Information

This section describes the status information that is presented to the Series/1 processor by the attachment. This information consists of:

- Condition codes
- Device status word
- Cycle-steal status words
- Residual status block
- Interrupt ID word

The device status word and cycle steal status words must be requested, by the processor, by using the appropriate I/O commands. All other status information is presented automatically when required by a particular I/O operation.

Condition Codes

Two types of condition codes are reported to the Series/1 by the attachment: (1) Operate I/O (IO) instruction condition codes and (2) interrupt condition codes.

Operate I/O (IO) Instruction Condition Codes

Operate I/O instruction condition codes are reported to the processor in response to an Operate I/O (IO) instruction directed to the attachment. The codes are related to conditions that can be detected during execution of the instruction. The following chart shows the I/O commands and the IO instruction condition codes that can be reported for each command:

I/O command	Hex	I/O instruction condition codes							
		0	1	2	3	4	5	6	7
Read ID	20	X					X		X
Read Status	21	X	X	X			X		X
Prepare	60	X					X		X
Disable System/370 Device Address	62	X	X	X	X		X		X
Enable System/370 Device Address	63	X	X	X	X	X	X		X
Set System/370 Device End	64	X	X	X	X	X	X		X
Set Attention to System/370	65	X	X	X	X	X	X		X
Device Reset	6F	X							X
Start	70	X	X	X	X	X	X		X
Start Diagnostic	71	X	X			X	X		X
Start Cycle Steal Status	7F	X	X	X			X		X
Halt I/O*	F0								X

*Channel-directed command

CC Value	*Meaning*
0	Device not attached
1	Busy
2	Busy after reset (refer to "Series/1 Resets" in this chapter)
3	Command reject
4	Intervention required
5	Interface data check
6	Not reported
7	Satisfactory

Interrupt Condition Codes

The following condition codes are reported when the Series/1 processor accepts a priority interrupt from the attachment:

CC Value	*Meaning*
0	Not reported
1	Not reported
2	Exception
3	Device end
4	Attention
5	Not reported
6	Not reported
7	Attention and device end

The condition codes are defined as follows:

CC=2 *Exception*. Reported when an abnormal end has occurred while executing an interrupt-causing command. The Series/1 program can interrogate the interrupt ID word for additional status.

CC=3 *Device end*. Reported when normal completion of an interrupt-causing command has occurred. Additional status information may also be in the interrupt ID word.

CC=4 *Attention*. Reported when an attention interrupt is generated by one of the following conditions:

1. The attachment receives an "attention" command from the System/370.
2. The attachment detects a System/370 reset, or a System/370 interface disconnect, when the two systems are not connected.
3. The attachment is manually set on-line to the System/370.
4. A time-out occurs before the Series/1 processor responds to an "attention" command attention interrupt. (Refer to item 1 of this list.)

Status information, indicating the type of attention interrupt, is available in the interrupt ID word.

CC=7 *Attention and device end*. Reported when attention and device end are both present. The interrupt ID word provides additional status information.

Device Status Word

The device status word is transferred to the Series/1 processor when a Read Status command or a Start Cycle Steal Status command is executed.

Bit definitions are:

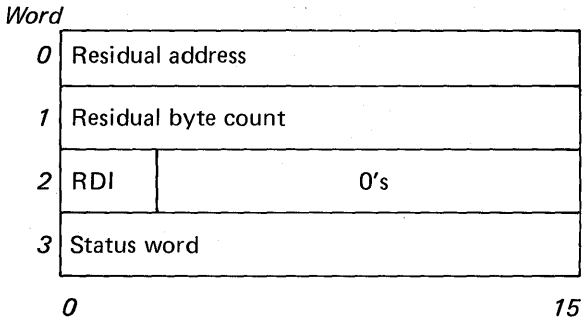
Bit	*Meaning*
0	Unused—always 0
1	*On-line*. This bit indicates the on-line/off-line state of the attachment with respect to the System/370. 0 = off-line state (control unit disabled) 1 = on-line state (control unit enabled) The Enable/Disable switch on the 4993 termination enclosure must be used to change states.
2	*System/370 busy or chaining*. This bit is set to 1 when the attachment accepts a command from the System/370. It is set to 0 when device end is reported to the System/370. *Note:* If System/370 chaining is in effect, this bit is not reset until device end is reported at the end of chaining.
3	*System/370 reset*. This bit is set to 1 if the attachment detects a System/370 reset condition while the two systems are connected. (Refer to "System/370 Reset" in Chapter 3.) This bit is set to 0 by a Series/1 reset or by successful execution of the next Series/1 I/O command.
4	*System/370 interface disconnect*. This bit is set to 1 if the attachment detects an interface disconnect sequence from the System/370 while the two systems are connected. (Refer to "System/370 Interface Disconnect" in Chapter 3.) This bit is set to 0 by a reset from the Series/1 or by successful execution of the next Series/1 I/O command.
5	*Time-out*. This bit is set to 1 when the attachment detects a data transfer time-out. (Refer to "Time-out" in Chapter 2.) This bit is set to 0 by a reset from the Series/1 or by successful execution of the next Series/1 I/O command.
6	*System/370 error*. This bit is set to 1 when a parity error is detected by the attachmentt while transferring data *from* the System/370 to the attachment. (A parity error detected by the System/370 channel is not reported to the attachment and is not indicated by this bit.) This bit is set to 0 by a reset from the Series/1 or by successful execution of the next Series/1 I/O command.

Bit	*Meaning*
7	*Attention command.* This bit is set to 1 when a System/370 "attention" command is received by the attachment. When set to 1, this bit indicates that bits 8–15 of this status word are valid and that they contain the last device address and command issued by the System/370. The "attention" command is encoded in bits 13–15 of this status word. Other System/370 commands do not affect the setting of this bit. This bit is set to 0 by (1) normal termination of the associated command, (2) a System/370 reset, (3) a System/370 interface disconnect, (4) a Series/1 reset or (5) a time-out condition.
8–12	*System/370 device address.* These bits reflect the five low-order bits of the last System/370 device address selected by the System/370. The address value can range from 0 to 31, but it is useful only when bit 7 of this status word is set to 1. These bits are not changed until the attachment receives a different device address.
13–15	*System/370 command.* These bits contain a binary value indicating the last "attention" command received from the System/370. This command is valid only when bit 7 of this status word is set to 1. These bits are not changed until the attachment receives a different command.

Bit			
13	*14*	*15*	*Command*
0	0	0	Read Buffer
0	0	1	Read Modified
0	1	0	Write
0	1	1	Erase/Write
1	0	0	Select
1	0	1	Erase All Unprotected
1	1	0	Diagnostic Read
1	1	1	Diagnostic Write

Cycle-Steal Status Words

Four status words (eight bytes) are transferred to the Series/1 processor when a Start Cycle Steal Status command is executed. The format is:

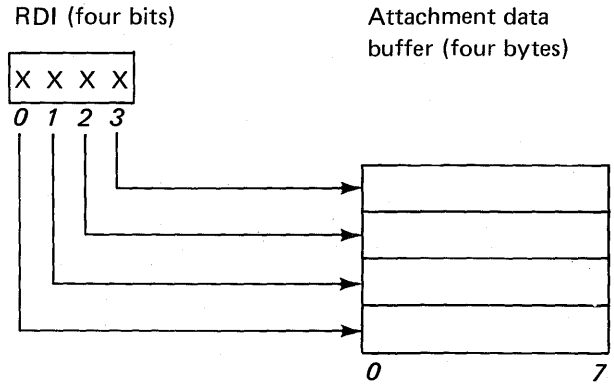


RDI – Residual data indicator (bits 0–3)

Residual Address. This is the main storage address of the last attempted cycle-steal transfer associated with a Start command or a Start Diagnostic command. The residual address can be a data address, a DCB address, or a residual-status-block address. Execution of a Start Cycle Steal Status command does not alter this address, which is set to 0000 (hex) by a power-on reset.

Residual Byte Count. When an operation is terminated, this word indicates any remaining byte count in the Series/1 section of the attachment. Execution of a Start Cycle Steal Status command does not alter this byte count.

Residual Data Indicator (RDI). Each RDI bit corresponds to one byte location in the attachment data buffer, as follows:



When a data transfer operation has ended, any byte of data remaining in the buffer is indicated by setting the appropriate RDI bits to 1's. This is a flag to the Series/1 program that all data was not completely transferred.

The RDI bits are set to 0's when no data remains in the buffer.

Status Word. This word is identical to the device status word. Refer to "Device Status Word" in this chapter for detailed bit definitions.

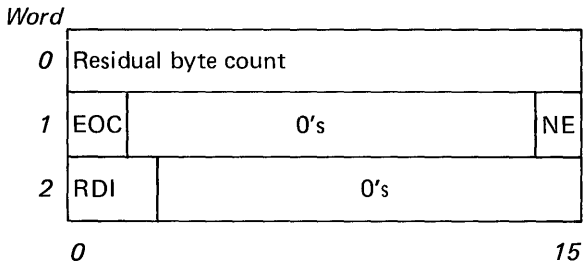
Bit	*Name*
0	Unused—always 0
1	On-line
2	System/370 busy or chaining
3	System/370 reset
4	System/370 interface disconnect
5	Time-out
6	System/370 error
7	Attention command
8–12	System/370 device address
13–15	System/370 command

Residual Status Block

When the suppress exception (SE) bit (bit 4) in the DCB control word is set to 1 for a Start command, the attachment stores the three-word residual status block into main storage after the data transfer for the DCB is completed. The starting main storage address is specified in DCB word 4.

The SE bit (when set to 1) also allows the attachment to suppress reporting an exception interrupt to the Series/1 when an incorrect-length record is detected. The incorrect-length-record condition is indicated by setting the *no exception* bit (bit 15 of word 1 in the status block) to 0.

The format of the residual status block is:



EOC – End of chain (bit 0)
NE – No exception (bit 15)
RDI – Residual data indicator (bits 0–3)

Residual Byte Count. When an operation terminates, this word indicates any remaining byte count in the Series/1 section of the attachment.

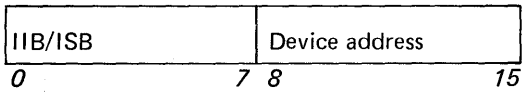
End of Chain (EOC). This bit is always set to 1 when the residual status block is stored.

No Exception (NE). This bit is set to 0 when an incorrect-length record is detected; otherwise, it is set to 1.

Residual Data Indicator (RDI). These bits indicate residual bytes of data that remain in the attachment data buffer after a data transfer has ended. Refer to "Cycle Steal Status Words" in this chapter for additional details.

Interrupt ID Word

The interrupt ID word is transferred to the Series/1 processor when an interrupt from the attachment is processed. The format is:



IIB – Interrupt information byte
ISB – Interrupt status byte

The IIB is presented when interrupt condition codes 3, 4, and 7 are reported. The ISB is presented when interrupt condition code 2 is reported. The device address field contains the Series/1 address assigned to the attachment.

Interrupt Information Byte (IIB)

The bits in the IIB are defined as follows:

Bit	*Meaning*
0	*Permissive device end.* This bit is set to 1 when an incorrect-length record is detected and suppress exception is in effect. Suppress exception is indicated when the SE bit in the DCB control word is set to 1.
1	*On-line.* This bit is set to 1 when the attachment goes from an off-line state to an on-line state. These states are explained in "Manual Operations" in Chapter 1.
2	*Chaining device end.* This bit is set to 1 if System/370 chaining is indicated while the two systems are connected. It is used to notify the Series/1 processor that chaining is in effect, and is presented (in the IIB) with a normal device end interrupt.
3	*System/370 reset.* This bit is set to 1 if the attachment detects a system reset from the System/370 while the two systems are not connected. This condition causes an attention interrupt to the Series/1. If an attention interrupt request is already active, only the System/370 reset is indicated in the IIB.
4	*System/370 Interface disconnect.* This bit is set to 1 if a System/370 interface disconnect sequence is detected while the two systems are not connected. This condition causes an attention interrupt to the Series/1. If an attention interrupt request is already active, only the interface disconnect is indicated in the IIB.

Bit	*Meaning*
5	*Time-out*. This bit is set to 1 by a command time-out, as follows: When an "attention" command is received from the System/370, the attachment presents an attention interrupt request to the Series/1, sets IIB bit 7 (attention command) to 1, and starts a timer. If a time-out occurs before the interrupt is accepted, IIB bit 7 is reset and this time-out bit is set to 1. When the time-out bit is set, the System/370 command is terminated. A time-out can also occur after the "attention" command interrupt has been accepted, but before the Series/1 responds with a matching operation. In this case, another attention interrupt request, with the IIB time-out bit set to 1, is presented to the Series/1. A third condition can occur where both the time-out bit and the attention command bit (bit 7) are set to 1's. This condition indicates that the attachment has received a System/370 command while a "time-out" attention interrupt is still active for a previous command.
6	*Chaining attention*. Bit 6 is used with IIB bit 7 to further define a System/370 chaining condition. These bits indicate that the System/370 command received by the attachment is either the beginning of a new chain or a continuation of chaining, as follows: *IIB Bit* *6 7 Meaning* 1 1 Beginning of a new chain 0 1 Continuation of chaining Note that bit 6 has meaning only when bit 7 is set to 1 and the command is involved in a chaining sequence. Refer to "System/370 Chaining" in Chapter 3 for additional details.
7	*Attention command*. This bit is set to 1 when an "attention" command is received from the System/370. This condition generates an attention interrupt request to the Series/1. *Note:* A time-out condition, a System/370 reset, or a System/370 interface disconnect can reset this bit before it is presented to the Series/1 (refer to IIB bits 3, 4, and 5).

Interrupt Status Byte (ISB)

The ISB is presented to the Series/1 processor when an exception interrupt (CC=2) is reported. For a cycle-steal device, the bits within the ISB have standard definitions, as follows:

Bit	*Name*
0	Device-dependent status available
1	Not reported
2	Incorrect-length record
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

Refer to the appropriate Series/1 processor description manual for complete descriptions of the bits.

Series/1 Resets

This section discusses the Series/1 resets that affect the attachment.

Power-on Reset. Both the Series/1 and the System/370 sections of the attachment are reset. The prepare register in the Series/1 section is reset. All System/370 device addresses are disabled, and the Series/1 residual address is set to 0000 (hex).

System Reset. This reset causes the Series/1 section of the attachment, including the prepare register, to be reset. All System/370 device addresses are disabled. If an operation is in process when this reset occurs, ending status (with *unit check*) is presented to the System/370. The System/370 sense byte defines the Series/1 reset condition. The Series/1 section of the attachment is in a *busy after reset* state until the System/370 accepts or clears the ending status.

Halt I/O Reset. This reset is generated when a Series/1 Halt I/O command is executed. It is identical to a system reset except that the prepare register and the System/370 device addresses are not reset.

Machine Check Reset. This reset is generated when a machine-check interrupt (not caused by a storage parity error) is processed. It is identical to a system reset except that the prepare register and the System/370 device addresses are not reset.

Device Reset. This reset is generated when a Series/1 Device Reset command is executed. It is identical to a system reset except that the prepare register and the System/370 device addresses are not reset.

Busy After Reset

This state is entered when the attachment detects a Series/1 reset while the two systems are connected. If an operation is in process when this reset occurs, ending status (with *unit check*) is presented to the System/370. The *busy after reset* state is exited when the status is accepted by the System/370 or when a System/370 reset occurs or when a power-on reset in the Series/1 occurs. During the busy after reset state, the attachment returns IO instruction CC=2 to most Series/1 commands.

Note: Two Series/1 commands, Enable System/370 Device Address and Set Attention to System/370, initiate a System/370 interface sequence that can be interrupted by a Series/1 reset. The *busy after reset* state is also entered at this time.

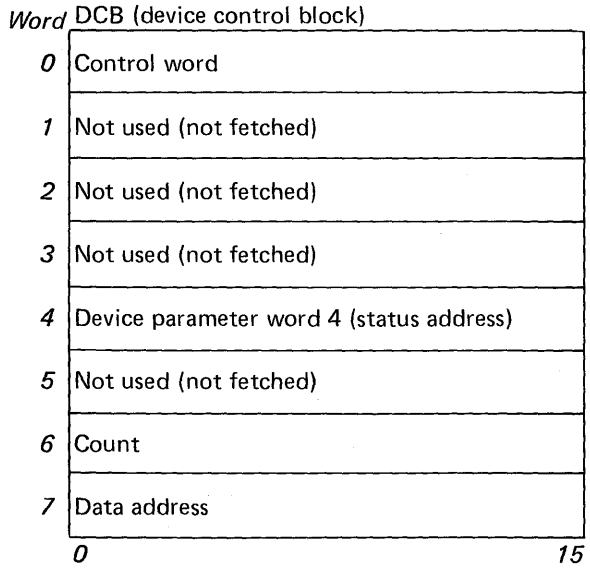
Appendix A. Reference Information

Series/1-System/370 Channel Attachment

Series/1 I/O Commands

Hex	*Command*	*IO instruction CCs reported*
20	Read ID	0, 5, 7
21	Read Status	0, 1, 2, 5, 7
60	Prepare	0, 5, 7
62	Disable System/370 Device Address	0, 1, 2, 3, 5, 7
63	Enable System/370 Device Address	0, 1, 2, 3, 4, 5, 7
64	Set System/370 Device End	0, 1, 2, 3, 4, 5, 7
65	Set Attention to System/370	0, 1, 2, 3, 4, 5, 7
6F	Device Reset	0, 7
70	Start	0, 1, 2, 3, 4, 5, 7
71	Start Diagnostic	0, 1, 4, 5, 7
7F	Start Cycle Steal Status	0, 1, 2, 5, 7

Series/1 Device Control Block (DCB)



Control Word

Bit	*Meaning*
0–1	Not used—must be 0's
2	Input flag
3	Not used—must be 0
4	Suppress exception
5–7	Cycle-steal address key
8–15	Not used—must be 0's

Series/1 Device Status Word

Bit	*Meaning*
0	Not used—0
1	On-line
2	System/370 busy or chaining
3	System/370 reset
4	System/370 interface disconnect
5	Time-out
6	System/370 error
7	Attention command
8–12	System/370 device address
13–15	System/370 command

Series/1 Cycle-Steal Status Words

Word 0

Bit	*Meaning*
0–15	Residual address

Word 1

Bit	*Meaning*
0–15	Residual byte count

Word 2

Bit	*Meaning*
0–3	Residual data indicator (RDI)
4–15	Not used—0's

Word 3

Same as Series/1 Device Status Word.

Series/1 Residual Status Block

Word 0

Bit	*Meaning*
0–15	Residual byte count

Word 1

Bit	*Meaning*
0	Always set to 1
2–14	Not used—0's
15	No exception

Word 2

Bit	*Meaning*
0–3	Residual data indicator (RDI)
4–15	Not used—0's

Series/1 Interrupt Condition Codes Reported

CC2, CC3, CC4, CC7

Series/1 Interrupt Information Byte (IIB)

Condition code	*IIB contents*
2	Cycle-steal interrupt status byte
3, 4, 7	

Bit	*Meaning*
0	Permissive device end
1	On-line
2	Chaining device end
3	System/370 reset
4	System/370 interface disconnect
5	Time-out
6	Chaining attention
7	Attention command

System/370 I/O Commands

Hex	*Command*
00	Test I/O
01	Write
02	Read Buffer
03	No-Operation
04	Sense
05	Erase/Write
06	Read Modified
0B	Select
0D	Diagnostic Write
0E	Diagnostic Read
0F	Erase All Unprotected
33	Subsystem Load Enable
E4	Sense I/O

System/370 Data for a Sense Command

Bit	*Meaning*
0	Command reject
1	Intervention required
2	Bus out check
3	Not used—0
4	Data check
5	Unit specify
6	Control check
7	Not used—0

System/370 Data for a Sense I/O Command

Byte	*Data (hex)*
0	FF
1	49
2	50
3	0X

X = 0 Inhibit IPL jumper installed
X = 1 Inhibit IPL jumper not installed

System/370 Status Byte

Bit	*Meaning*
0	Attention
1	Status modifier
2	Control unit end
3	Busy
4	Channel end
5	Device end
6	Unit check
7	Not used—0

Index

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