IBM

Series/1

SY34-0082-0

IBM Series/1
4963 Disk Subsystem
and Attachment Feature
Theory Diagrams

First Edition (February 1979)

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Preface

This manual describes the 4963 Disk Subsystem and Attachment Feature.

This manual is designed to be used in the classroom as an aid in teaching the personnel that maintain the 4963. This manual may also be used in the field as a recall document.

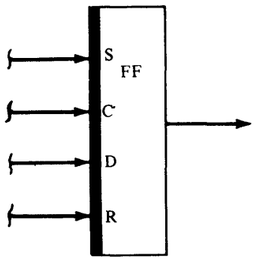
Sequence charts and diagrams are intended for instructional purposes only and are not to be used in troubleshooting procedures. The 4963 machine logic diagrams (MLDs) are to be used in diagnosing problems not found using the maintenance analysis procedures (MAPs) that accompany the 4963 maintenance information manual.

Chapter 1 is an introduction to the 4963. Cahpter 2 describes the functional units of the 4963. Chapter 3 contains an explanation of the circuit functions for the attachment feature, the disk unit controls, and the disk unit circuits. A legend is included in the Preface that describes the symbols used in the diagrams. Chapter 4, the operations chapter, describes how the processor transfers data to and from the disk units.

Related Publications

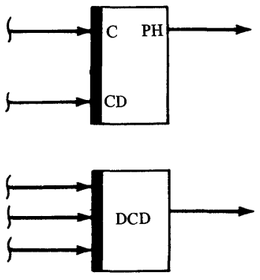
- *IBM Series/1 4953 Processor and Processor Features Theory Diagrams*, SY34-0042
- *IBM Series/1 4955 Processor and Processor Features Theory Diagrams*, SY34-0041
- *IBM Series/1 4963 Disk Subsystem and Attachment Feature Maintenance Information*, SY34-0035
- *IBM Series/1 4963 Disk Subsystem Parts Catalog*, S134-0034
- *IBM Series/1 4955 Processor and Processor Features Description*, GA34-0021
- *IBM Series/1 4953 Processor and Processor Features Description*, GA34-0022
- *IBM Series/1 4963 Disk Subsystem Description*, GA34-0051
- *IBM Series/1 User's Attachment Manual*, GA34-0033

Legend



Flip Flop

The flip flop (FF) is a storage element that may have a set (S), reset (R), control (C), or controlled data (D) inputs.

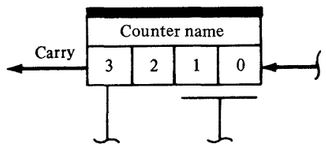


Polarity Hold

The polarity hold (PH) is a storage element that may have control (C), controlled data (D), or reset (R) inputs.

Decode

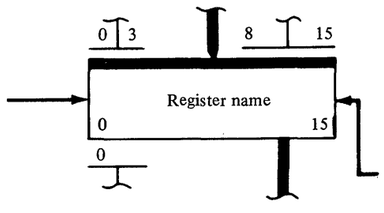
The decode (DCD) block may have multiple inputs of individual lines, a bus input, or a combination of both.



Counter

+1 for up

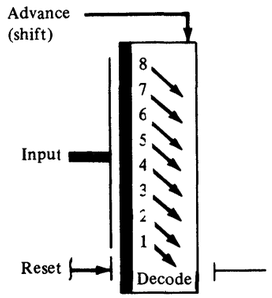
-1 for down



Register

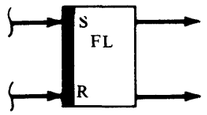
Input side is denoted by thick line. A partial transfer of contents is shown by numbered input and/or output lines.

Carry or increment



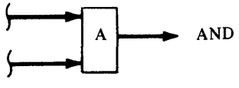
Shift registers

The shift registers are commonly used to seralize and deserialize data. Input side is denoted by the thick line. A partial transfer of contents is shown by numbered input/output lines.

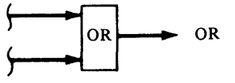


Flip latch

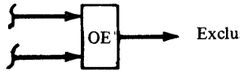
Input side is denoted by thick line. Circuit multiples shown by numeral in lower right corner.



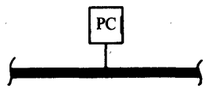
AND



OR



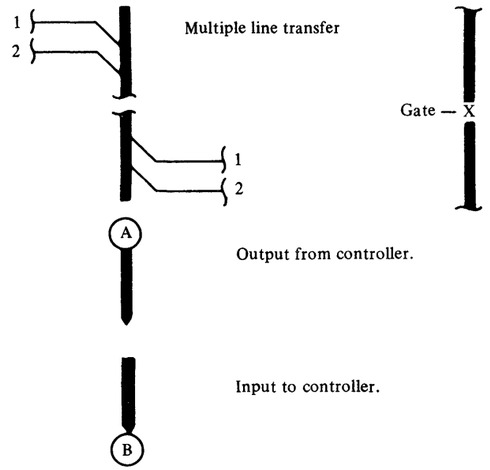
Exclusive OR



Parity check data bus

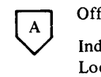
Parity generate data bus

Negator (invertor)



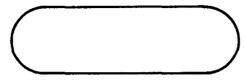
On-page connector

Indicates connection between two parts of the same page. Arrow leaving symbol points (line-of-sight) to correspondingly-numbered symbol.



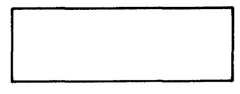
Off-page connector

Indicates connection between diagrams located on separate pages. Location of correspondingly-lettered symbol shown adjacent.



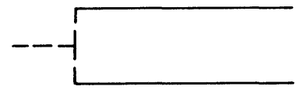
Terminal

Indicates beginning end or event.



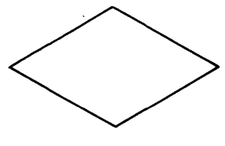
Process

Indicates beginning or end of event.



Annotation

Gives descriptive comment or explanatory note.

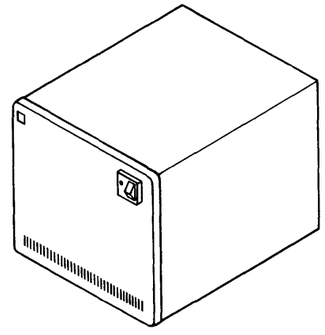


Decision

Indicates a point in a flowchart where a branch to alternate paths is possible.

Contents

Chapter 1.
Introduction



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Introduction

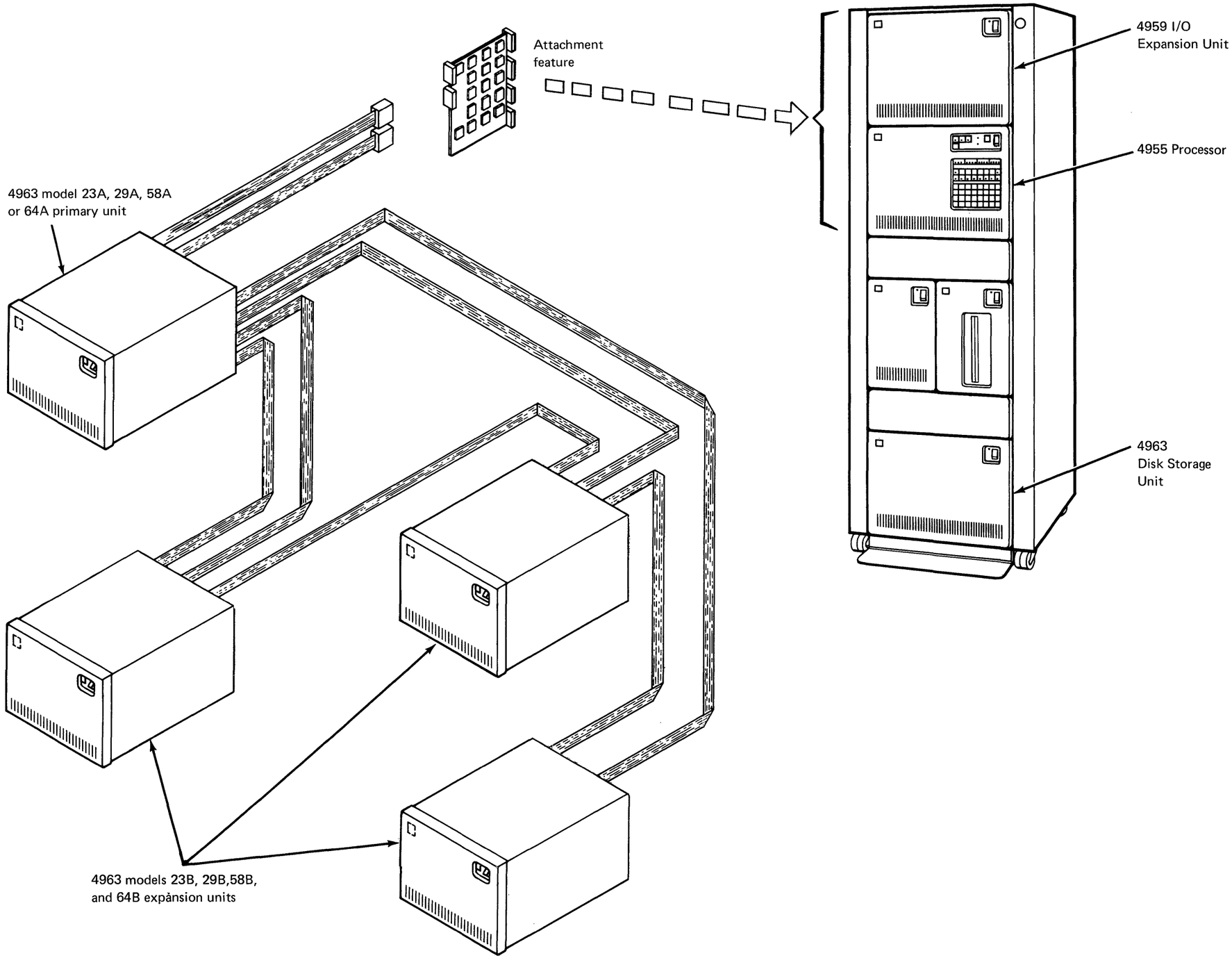
The IBM Series/1 4963 Disk Subsystem and Attachment Feature consists of one primary unit and up to three expansion units (eight models are available), their associated cables, and an attachment feature that provides a connection to the Series/1 processor I/O channel. Each disk storage unit communicates with the processor through controls in the primary disk storage unit and through the attachment feature.

4963 Primary Unit

Each 4963 subsystem must contain either a 4963 Model 23A, 29A, 58A, or 64A primary unit. The primary unit contains the disk unit controls that provide control functions for all disk storage units in the subsystem.

4963 Expansion Unit

A 4963 subsystem can contain, in any combination, up to three 4963 Model 23B, 29B, 58B, or 64B expansion units. The expansion units do not contain disk unit controls; these controls are in the located primary unit.



Disk Unit

A disk storage unit is a device that magnetically stores data on a spinning disk. The 4963 disk enclosure contains either four or six of these disks. The four-disk models use only three of the disks to store information; the fourth disk is used for balance and air circulation. Movable read/write heads access data on the disks via an access mechanisim that moves the heads to specified locations in the data areas of the disks. In the models that have fixed heads, movable-head 0 is replaced by eight fixed heads are installed. The fixed-head operations require significantly less time than the movable-head operations, because the access mechanism does not move. The disk storage unit can read or write the data without first performing a seek operation.

Model	Number of disks*	Primary or expansion unit	Number of fixed heads	Number of movable heads
23A	3	Primary	8	4
23B	3	Expansion	8	4
29A	3	Primary	0	5
29B	3	Expansion	0	5
58A	6	Primary	8	10
58B	6	Expansion	8	10
64A	6	Primary	0	11
64B	6	Expansion	0	11

*Disk units with 3 disks actually have 4 physical disks. The 4th disk is not used to store data.

Disk Unit Specifications

The functional specifications of the disk storage unit are:

Rotational speed	3125 RPM
Time for one rotation	19.2 ms
Average rotational delay or latency	9.6 ms (nominal)
Data transfer rate	
to or from channel (average over one track)	426,666 bytes/sec
on and off disk (instantaneous)	1,030,000 bytes/sec
Movable-head storage	
Sectors per track	32 usable 1 reserved
Data records per sector	2
Bytes per data record	256
Data bytes per track	16,384
Tracks per cylinder	
Models 23A and 23B	4
Models 29A and 29B	5
Models 58A and 58B	10
Models 64A and 64B	11
Data Bytes per cylinder	
Models 23A and 23B	65,536
Models 29A and 29B	81,920
Models 58A and 58B	163,840
Models 64A and 64B	180,224
Cylinders	360 total
1 track is reserved	
1 track is reserved for write-diagnostic purposes	
358 usable tracks	
Total movable-head storage capacity	
Models 23A and 23B	23,592,960 bytes
Models 29A and 29B	29,491,200 bytes
Models 58A and 58B	58,982,400 bytes
Models 64A and 64B	64,880,640 bytes
Fixed-head storage (models 23A, 23B, 58A, and 58B only)	
Number of heads	8
Sectors per track	32
Data records per sector	2
Bytes per data record	256
Bytes per track	16,384
Total storage capacity in bytes	131,072

Device Addresses, Locations, and Cabling

Device Addresses

Disk storage units in the 4963 subsystem are designated as physical units 0, 1, 2, and 3. The device address for the primary unit (physical unit 0) can be any even address from hex 00–FE (decimal 0–254) with the following restrictions:

1. If one or two units are installed (a primary unit or a primary unit and an expansion unit), the device address of the primary unit must be divisible by two.
2. If three or four units are installed (a primary unit and either two or three expansion units), the device address of the primary unit must be divisible by four.

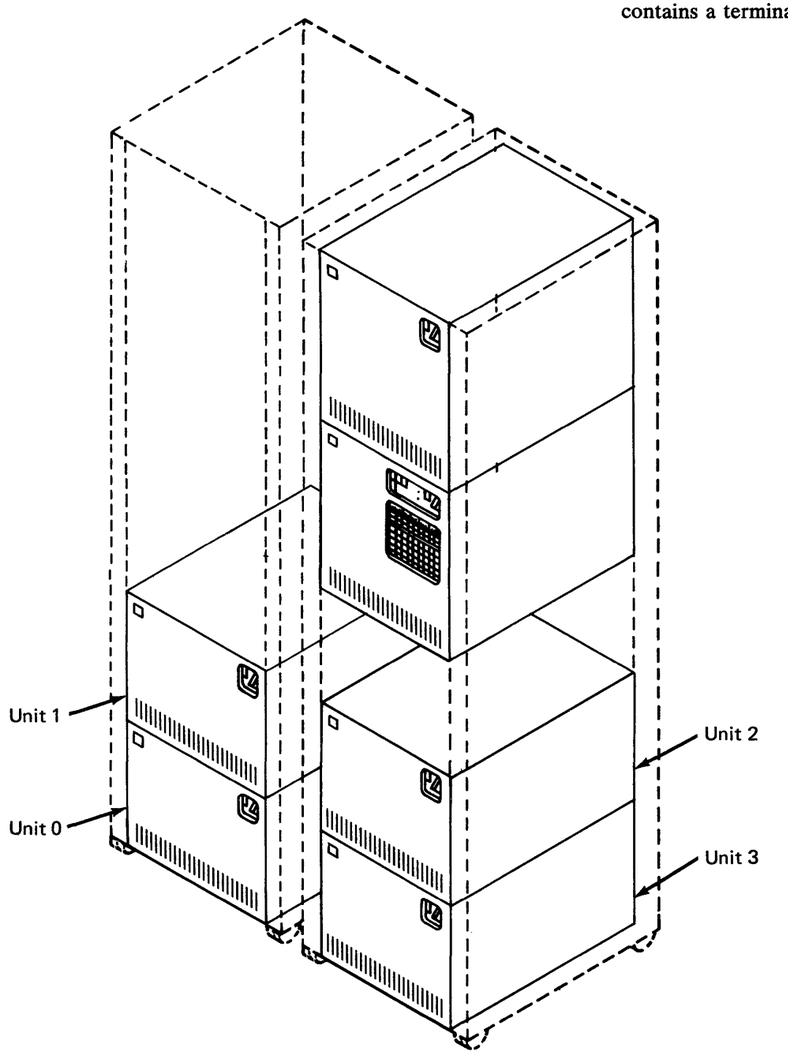
Expansion unit device addresses are sequentially numbered in ascending order from the primary unit's device address.

Examples:

primary unit device address	= 6
expansion unit device address	= 7
or	
primary unit device address	= C
first expansion unit device address	= D
second expansion unit device address	= E
third expansion unit device address	= F

Locations

The disk storage units in the 4963 subsystem are mounted in the enclosure in specific locations, as shown in the illustration. If the subsystem includes more than two disk storage units, a second enclosure is required. The units must be mounted in the locations shown for the cables to connect.



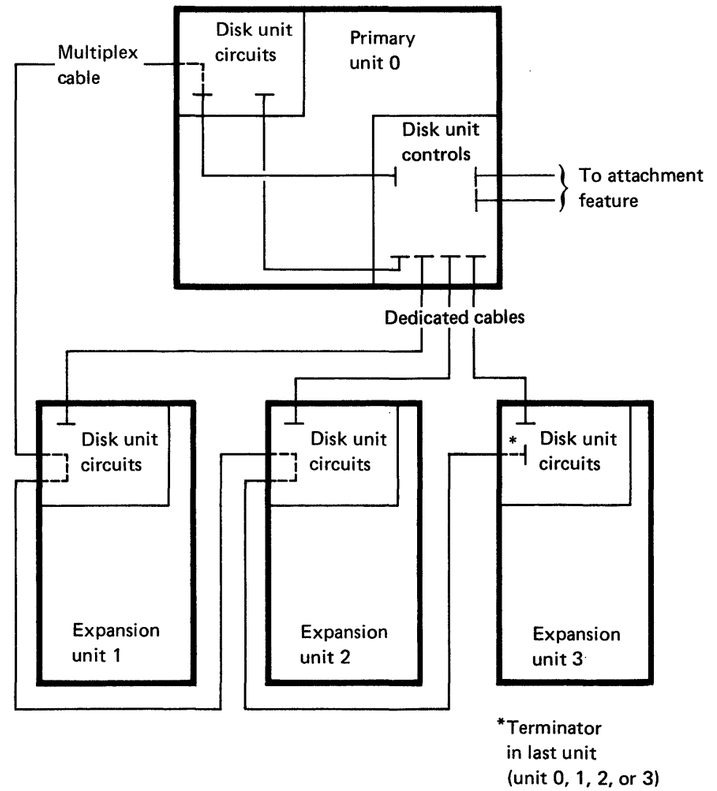
Cabling

The primary unit (unit 0) is connected to the attachment feature by two cables. Each expansion unit (units 1–3) is connected into the subsystem by two cables: a dedicated cable, which contains control lines and the read and write data lines, and a multiplex cable, which contains the tag and control lines. The last unit in the subsystem contains a terminator card.

The dedicated cable from each expansion unit connects directly to the disk unit controls subassembly in the primary unit.

The multiplex cable from each expansion unit connects to the preceding disk storage unit. The multiplex cable from the disk unit circuits located in unit 0 connects to the disk unit controls located in the same unit. The cable from expansion unit 1 connects to the disk unit circuits located in unit 0, the cable from expansion unit 2 connects to expansion unit 1, and the cable from expansion unit 3 connects to expansion unit 2.

A terminator card in the last disk storage unit in a subsystem provides a termination for the multiplex cable. If the subsystem does not include expansion units, the terminator card must be installed in the primary unit.



Basic Data Flow

Data is transferred between the 4963 disk subsystem and the processor I/O channel via the attachment feature card. Data is transferred within the disk subsystem by the disk unit controls and the disk unit circuits.

Attachment Feature Card

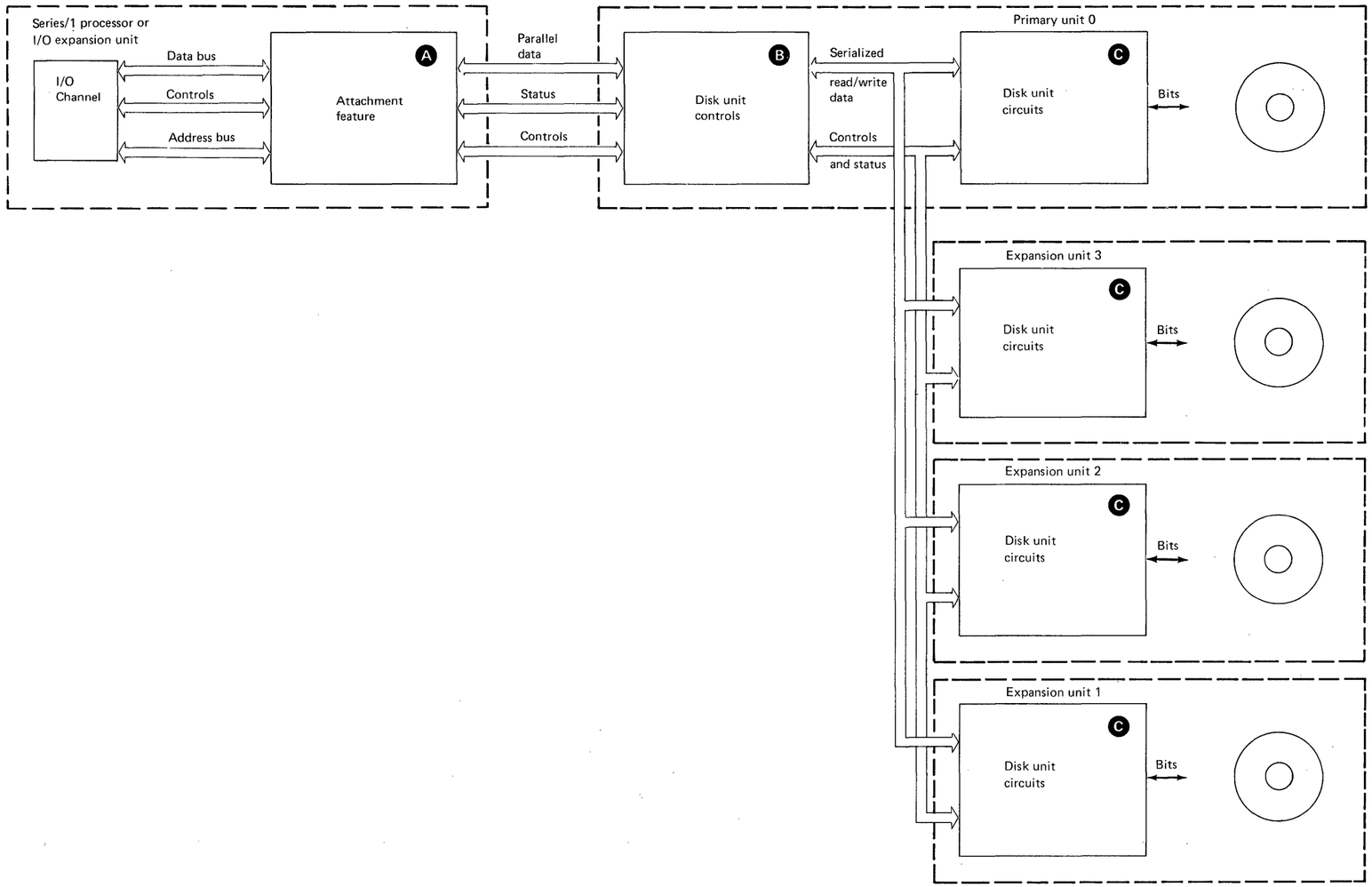
The attachment feature card Ⓐ is mounted in either the processor or the I/O expansion unit. The attachment feature, which physically connects the subsystem to the processor I/O channel, provides the logical controls for transferring data between the subsystem and the channel. The processor issues I/O commands for the individual disk storage units to the attachment feature. The attachment feature then initiates operations to the individual disk storage units via the disk unit controls.

Disk Unit Controls

The disk unit controls Ⓑ is mounted in the primary disk storage unit. The disk unit controls accepts controls status and data from the attachment feature, and then directs the disk storage units to locate the data and transfer it to or from the attachment.

Disk Unit Circuits

Each disk storage unit contains the circuits that control the disk access mechanisms and the reading and writing of data. The disk unit circuits Ⓒ. convert the analog pulses read from the disks to the digital signals required by the disk unit controls. The disk unit circuits also convert digital signals from the disk unit controls to analog pulses to be written on the disks.

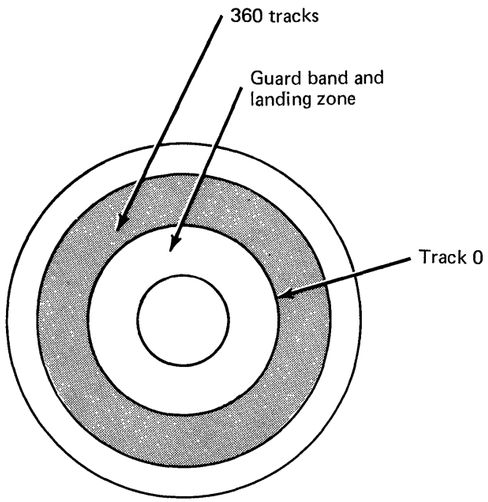


Disk Format

Each disk surface is organized into a set of concentric tracks that can be accessed by the data heads. A track is the area of the disk that passes under a data head during a revolution of the disk. The data area of a disk surface contains 360 tracks numbered hex 000–167 (decimal 0–359).

The 16 additional/tracks that are located between the disk spindle and the data area, are designated as a guard band and landing zone. They provide an area where the heads can settle when power is removed from the disk storage unit.

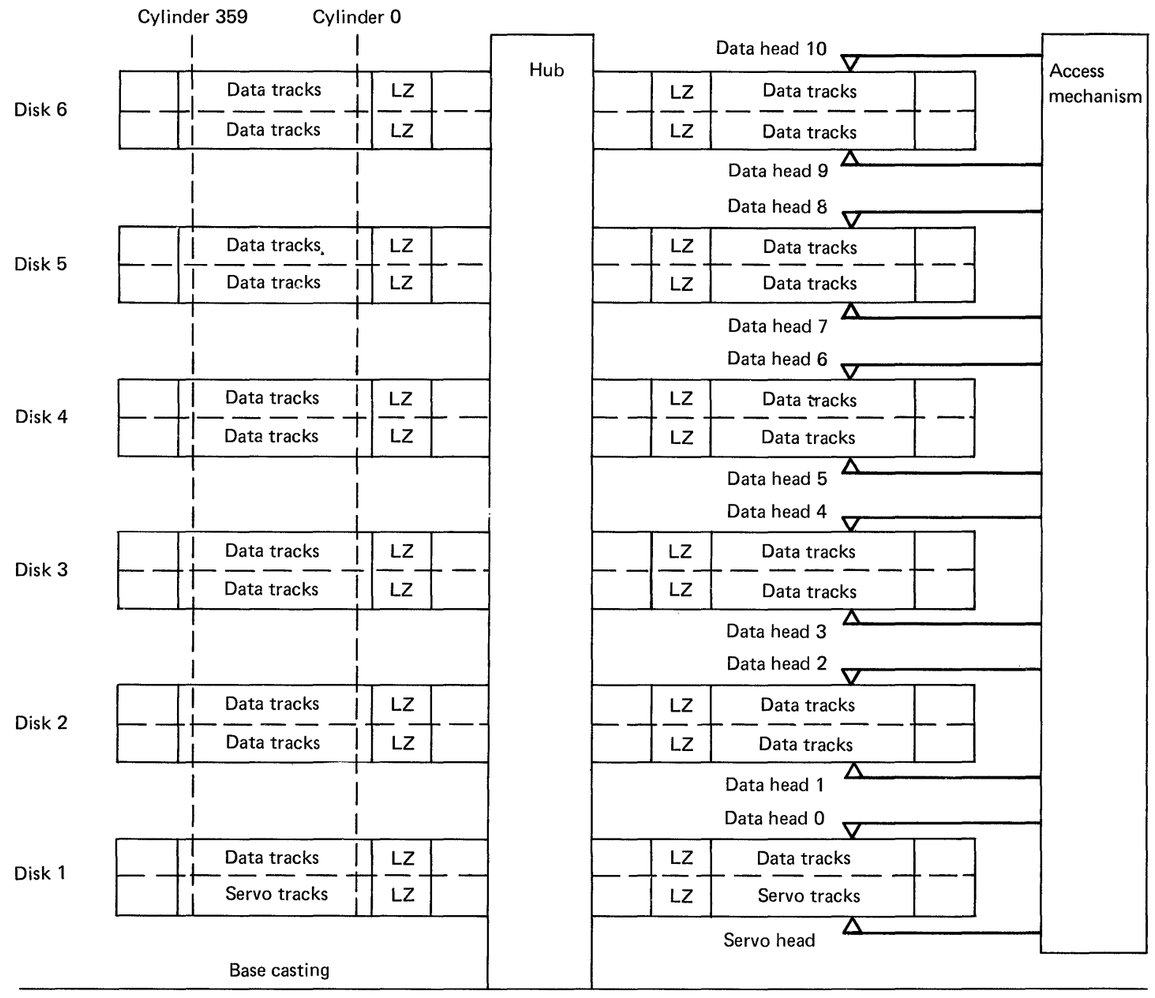
The first 16 tracks in the guard band and landing zone on the dedicated servo surface are written with information that indicates to the disk unit circuits that the head is between the disk spindle and cylinder 000.

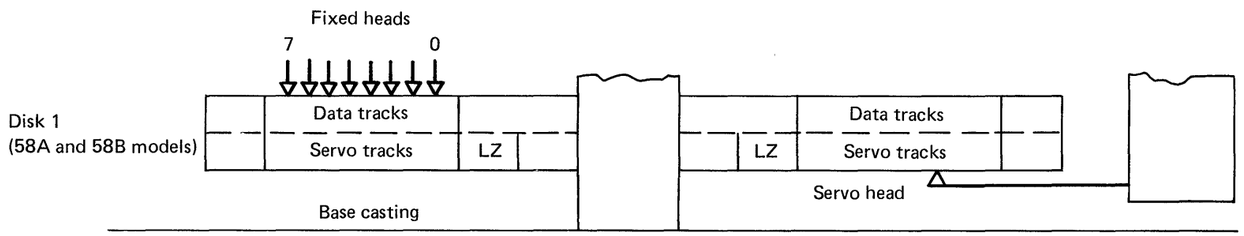


Cylinders

The 4963 has either four or six disks mounted on a single hub. There are either six or twelve recording surfaces. All recording surfaces, except the surface closest to the base casting, are used for reading and writing data. A group of tracks (one track for each movable head) is referred to as a cylinder. The cross-sectional view of the disks shows how the data tracks, data heads, and cylinders relate to each other.

The data tracks under the eight fixed heads do not coincide with the cylinder numbers assigned to the movable heads. For addressing purposes, the cylinder number for fixed heads is defined as having all cylinder number bits on (see chapter 4, under "Sector/Record Addressing").





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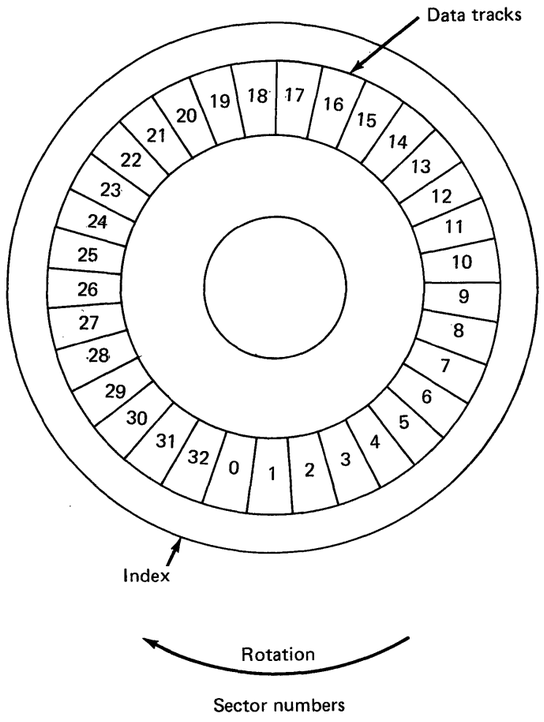
Data Track Organization

Each data track on a disk is divided into 33 sectors, numbered hex 00–20 (decimal 00–32). Special coding in the servo tracks signals the beginning of each sector. Of the 33 sectors on the track, 32 can be used for data. Sector number 32 is designated as an alternate sector and can be used if one of the first 32 sectors (0-31) develops a defect. The first defective sector on a track is assigned to the alternate sector for that track.



Physical Sectors and Logical Sectors

An index code, written on each track of the dedicated servo surface, identifies the beginning of all tracks for a specific cylinder. Timing considerations require that sector 0 be offset from one disk surface to the next. Therefore, the sectors are given logical sector numbers that do not necessarily correspond to their physical locations. The 4963 performs automatic head switching when a multiple-record data-transfer operation requires more records than one track has available. For head switching to occur between the time the operation is completed on record number 63 of sector 31 and the time record number 0, logical sector 0, for the next track is available for use, the logical sectors are physically offset by 8 sectors between adjacent disk surfaces, as shown in the chart. Note that the location of sector 32, the alternate sector, always precedes the index code.

For all fixed heads, logical sector 0 and physical sector 0 coincide. When fixed heads are installed and head 0 is not present, the logical sectors on the recording surface for head 1 remain offset.

Physical sector numbers	Logical sector numbers			
	Heads 0*, 4, 8**	Heads 1, 5**, 9**	Heads 2, 6**, 10**	Heads 3, 7**
0	0	24	16	8
1	1	25	17	9
2	2	26	18	10
3	3	27	19	11
4	4	28	20	12
5	5	29	21	13
6	6	30	22	14
7	7	31	23	15
8	8	0	24	16
9	9	1	25	17
10	10	2	26	18
11	11	3	27	19
12	12	4	28	20
13	13	5	29	21
14	14	6	30	22
15	15	7	31	23
16	16	8	0	24
17	17	9	1	25
18	18	10	2	26
19	19	11	3	27
20	20	12	4	28
21	21	13	5	29
22	22	14	6	30
23	23	15	7	31
24	24	16	8	0
25	25	17	9	1
26	26	18	10	2
27	27	19	11	3
28	28	20	12	4
29	29	21	13	5
30	30	22	14	6
31	31	23	15	7
32	32	32	32	32

← Index (row 0)

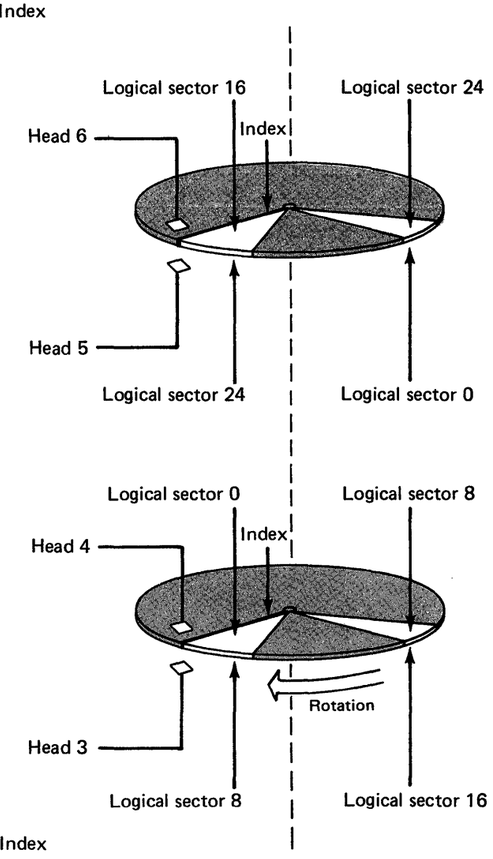
← Index (row 32)

Sector 32 is the alternate sector, and always precedes the index code.

* Head 0 is used only on models 29A, 29B, 64A, and 64B.

**Heads 5, 6, 7, 8, 9, and 10 are used only on models 58A, 58B, 64A, and 64B.

Note: in the following example the logical sector numbers for adjacent heads are offset by 8.

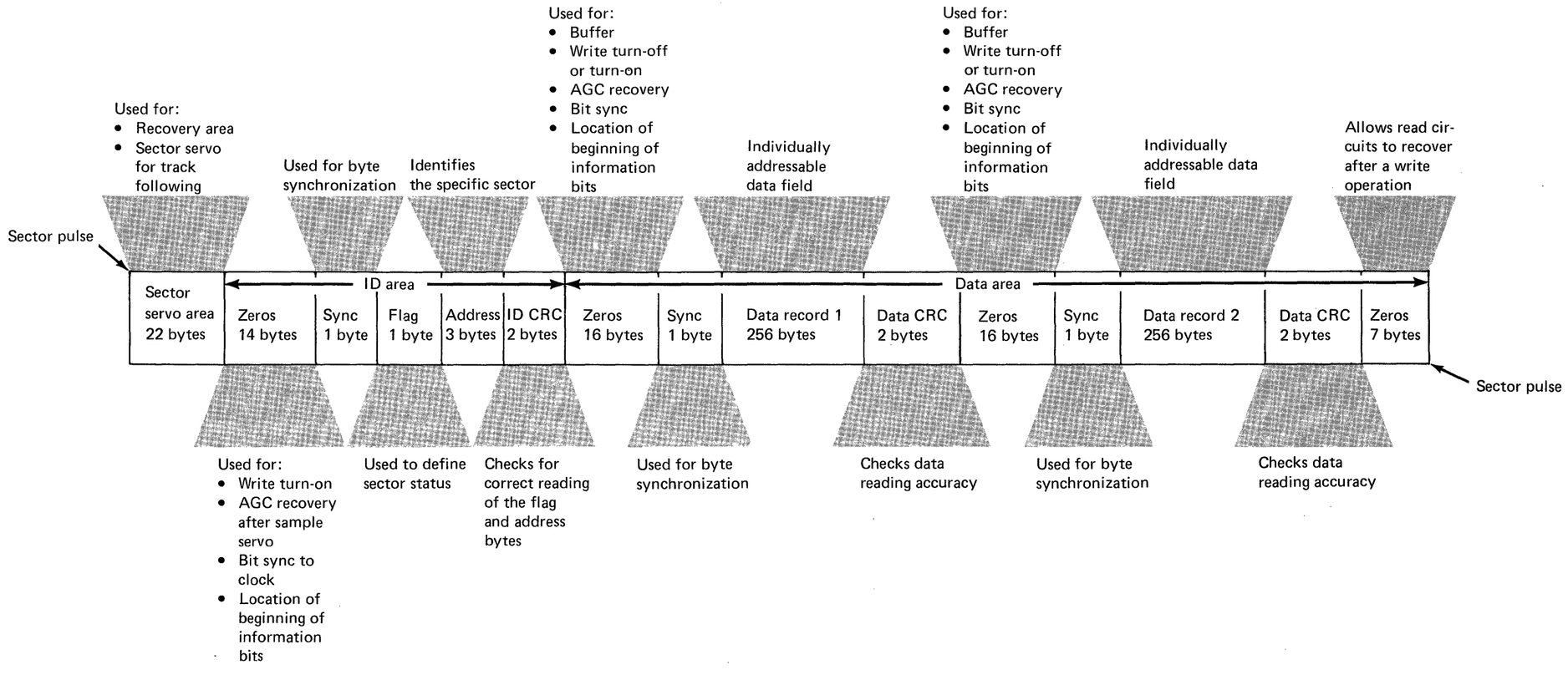


Sector Format

A sector is partitioned into three basic areas:

1. A sector servo area, which is used in conjunction with the servo head to position the data head in the center of the track.
2. An ID area, which contains the flag field, the address field, and the cyclic redundancy check (CRC) character field.
3. A data area, which contains two 256-byte data fields and a CRC character field for each data field.

The fields of the sector are shown here:



Sector Servo Area

Manufacturing tolerances can cause a misregistration of a fraction of a track between the servo head and any of the movable data heads. This misregistration can result in poor quality signals being received from the disk. The sector servo area in each sector acts as a reference for the access mechanism, to correct for misregistration.

When a data head is selected for reading or writing, it reads the sector servo area of each sector first. If the information read from the sector servo field indicates that the data head is not in the center of the track, the access mechanism moves the data head to the center of the track.

Zeros (0's) Fields

These fields are used to provide buffers for recovery times and for bit synchronization. Recovery times are necessary to allow the automatic gain control (AGC) circuits to stabilize and to allow the heads to switch between the read state and the write state. Bit sync ensures that the clock in the disk unit control circuits is in step with the clocking pulses received from the servo head.

Sync Fields

These fields, which consist of a single byte that contains hex 01, are used to set the disk unit control circuits to a byte boundary so that serial bits from the disk can be converted to parallel bytes for use in the disk subsystem.

Flag Field

The flag field defines the status of the sector and indicates if an alternate sector has been assigned. It also indicates if the sector was defective when the disk storage unit was manufactured or if the defect occurred during use. The bits of the flag field are:

Bit	Meaning
0	Defective data record 2
1	Defective data record 1
2	User-assigned defect
3	Protected data area
4	Sector is displaced
5	Sector is reassigned to an alternate cylinder on another track
6	Manufacturer-assigned defect
7	An assigned alternate sector

The use of bits 0, 1, and 3 is optional for the user.

Address Field

The address field contains the sector, head, and cylinder numbers that identify a particular sector.

Sector number	Head number	Cylinder number
0 7	*0 6 7*	*0 7*

Bit	Value	Bit	Value	Bit	Value
0	**	0	**	7	256
1	32	1	*	0	128
2	16	2	8	1	64
3	8	3	4	2	32
4	4	4	2	3	16
5	2	5	1	4	8
6	1	6	**	5	4
7	**			6	2
				7	1

* Designates a fixed head when equal to a 1.
** These bits must be 0.

Physical sector numbers	Logical sector numbers: Sector number on disk	Heads 0, 4, 8	Sector number on disk	Heads 1, 5, 9	Sector number on disk	Heads 2, 6, 10	Sector number on disk	Heads 3, 7	
0	00	0	30	24	20	16	10	8	← Index
1	02	1	32	25	22	17	12	9	
2	04	2	34	26	24	18	14	10	
3	06	3	36	27	26	19	16	11	
4	08	4	38	28	28	20	18	12	
5	0A	5	3A	29	2A	21	1A	13	
6	0C	6	3c	30	2C	22	1C	14	
7	0E	7	3E	31	2E	23	1E	15	
8	10	8	00	0	30	24	20	16	
9	12	9	02	1	32	25	22	17	
10	14	10	04	2	34	26	24	18	
11	16	11	06	3	36	27	26	19	
12	18	12	08	4	38	28	28	20	
13	1A	13	0A	5	3A	29	2A	21	
14	1C	14	0C	6	3C	30	2C	22	
15	1E	15	0E	7	3E	31	2E	23	
16	20	16	10	8	00	0	30	24	
17	22	17	12	9	02	1	32	25	
18	24	18	14	10	04	2	34	26	
19	26	19	16	11	06	3	36	27	
20	28	20	18	12	08	4	38	28	
21	2A	21	1A	13	0A	5	3A	29	
22	2C	22	1C	14	0C	6	3C	30	
23	2E	23	1E	15	0E	7	3E	31	
24	30	24	20	16	10	8	00	0	
25	32	25	22	17	12	9	02	1	
26	34	26	24	18	14	10	04	2	
27	36	27	26	19	16	11	06	3	
28	38	28	28	20	18	12	08	4	
29	3A	29	2A	21	1A	13	0A	5	
30	3C	30	2C	22	1C	14	0C	6	
31	3E	31	2E	23	1E	15	0E	7	
32	40	32	40	32	40	32	40	32	← Index

CRC Character Fields

The CRC character fields are used for checking the reading and writing accuracy. Three separate two-byte CRC characters are written on the disk; the ID area CRC character, the data record 1 CRC character, and the data record 2 CRC character. During a write operation, the CRC is generated. While information is being read, another CRC character is being developed. After the information and the CRC character are read, the developed CRC character is compared to the CRC character read from the disk. If the two CRC characters are not equal, a CRC occurs.

Data Records 1 and 2

Each sector contains two 256-byte records: data record 1 and data record 2. Because the disk storage unit operates in interleaved mode, the record number for data record 2 is 32 greater than the record number for data record 1. Interleaved mode means that when reading or writing data, data record 1 and data record 2 of the same sector are not operated on during the same revolution of the disk. The disk unit must make two revolutions to read or write both records contained in a sector, and each record must be addressed individually. The following chart illustrates the data record numbers within the sectors.

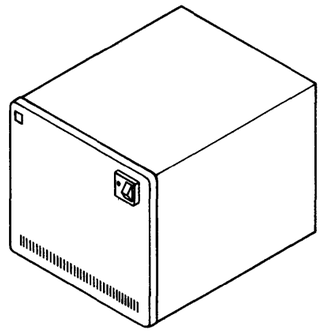
Sector number	Data record 1 record number	Data record 2 record number
Decimal	Decimal	Decimal
0	0	32
1	1	33
2	2	34
3	3	35
31	31	63
32	Reserved for alternate sector usage	

Maintenance

The 4963 requires no scheduled maintenance. To repair a 4963, adjust internal components or replace field replaceable units (FRUs) as directed by the MAP charts.

For proper use of the MAP charts and diagnostic programs, see the introductory pages of the MAP charts and the Diagnostic User's Guide.

Chapter 2.
Functional Units

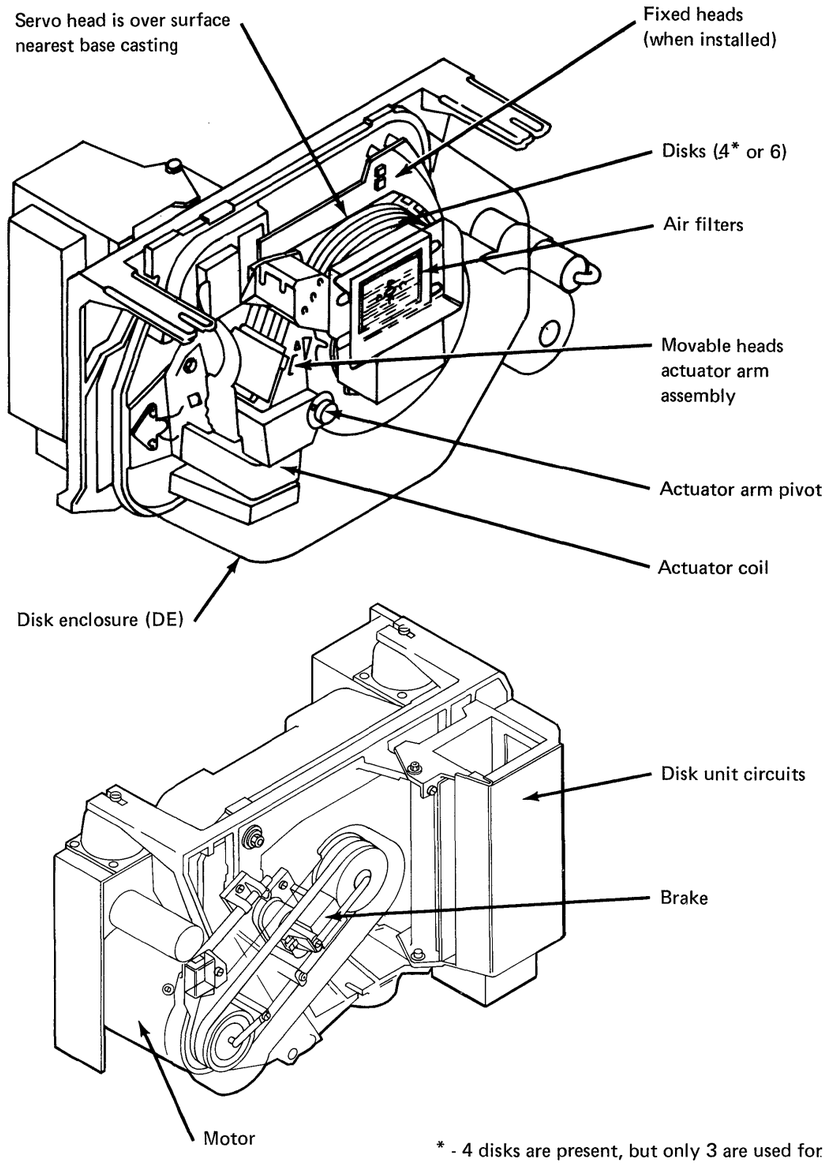


Disk Enclosure and Drive

The disk enclosure is a sealed unit containing the data and servo heads, the actuator arm assembly, the disks, the spindle, and some of the disk unit circuits. The drive motor, the brake assembly, and the remaining disk unit circuits are attached to the disk enclosure base casting.

Air Circulation System

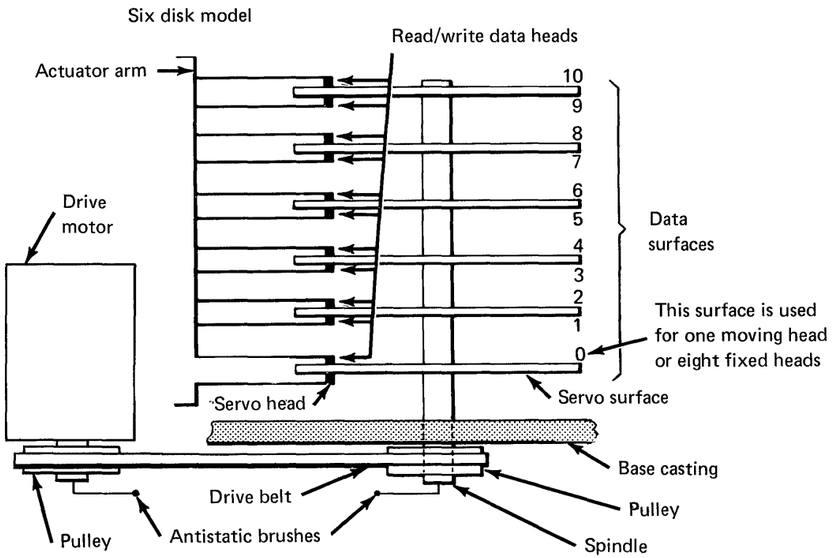
Because head-to-disk spacing is small, contamination within the disk enclosure must be controlled. Two filters, an absolute filter and a breather filter, minimize contamination within the disk enclosure. The disk enclosure has a closed-loop air circulation system that uses blades on the spindle hub to continuously circulate air through an absolute filter located within the enclosure. A breather filter equalizes the air pressure during startup and during air pressure changes caused by ambient temperature variations that occur during operation. The absolute filter and the breather filter are not accessible and require no scheduled maintenance.

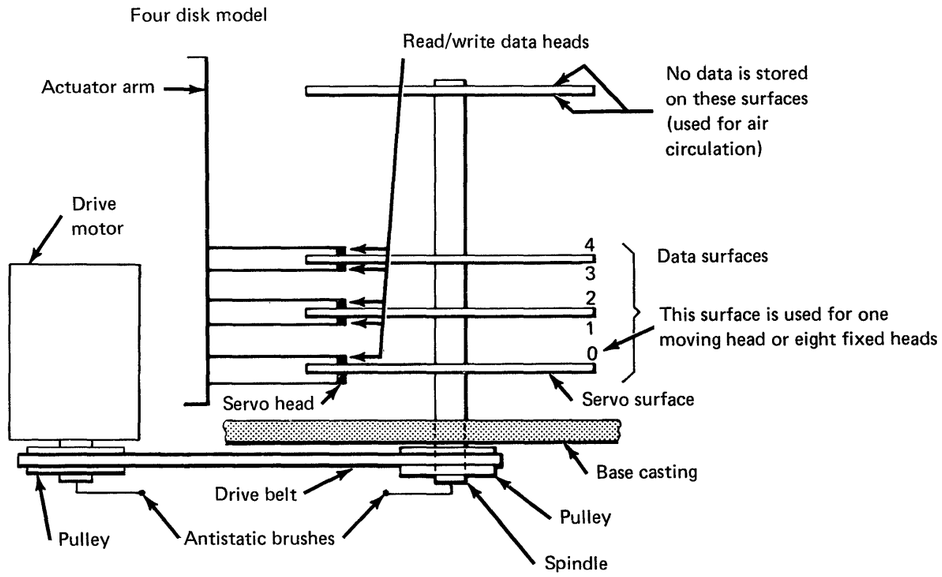


* - 4 disks are present, but only 3 are used for recording information. The fourth disk is used for balance and air circulation.

Disk Spindle

Depending on the type of disk enclosure installed, either four or six disks are clamped onto the spindle hub. The spindle, which is supported in the base casting by two bearings, is coupled to the drive motor through a pulley attached to the end of the spindle, a conductive drive belt, and a motor pulley. The spindle and the drive belt are grounded to the disk enclosure base casting by two antistatic brushes located adjacent to the spindle and motor pulleys.





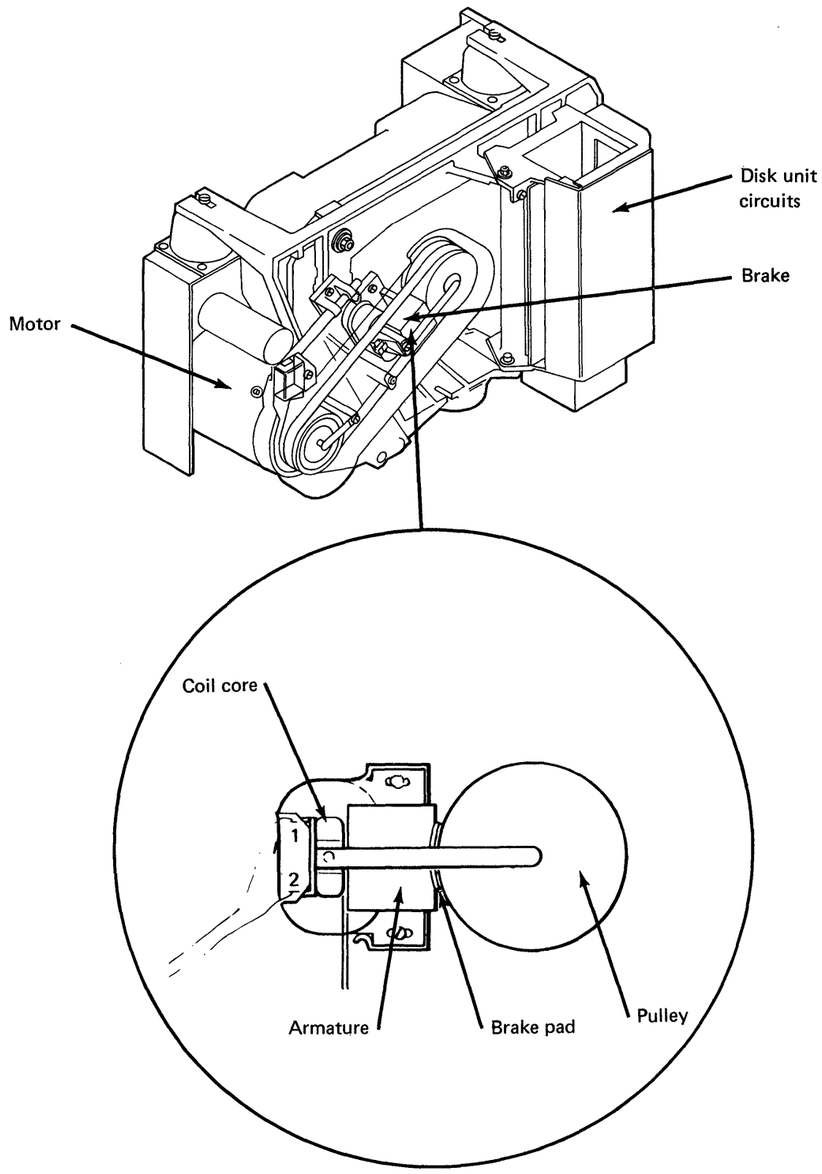
Drive and Brake System

The disk drive system consists of the drive motor, the spindle and motor pulleys, the belt, the belt tensioner, and the brake assembly.

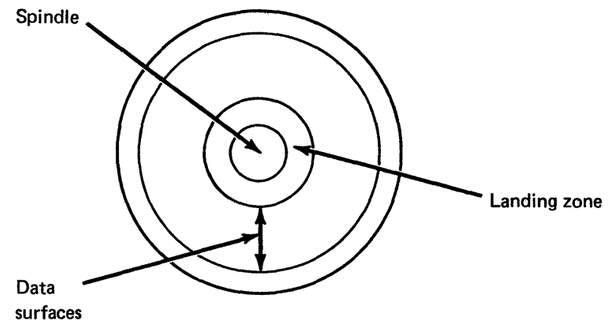
Motor and Brake

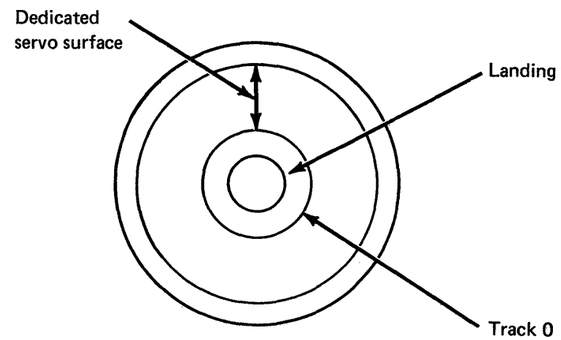
The disk drive motor is a high-torque motor that quickly brings the disks up to an operating speed of 3125 rpm. When power is turned off or if power fails, a spring-loaded pad on the brake assembly operates against the spindle pulley to ensure correct deceleration of the disks. When the disks are stationary, the heads are in the landing zones and are in contact with the disks.

To minimize head and disk wear during start and stop operations, the time that the heads are in contact with the rotating disks must be limited.



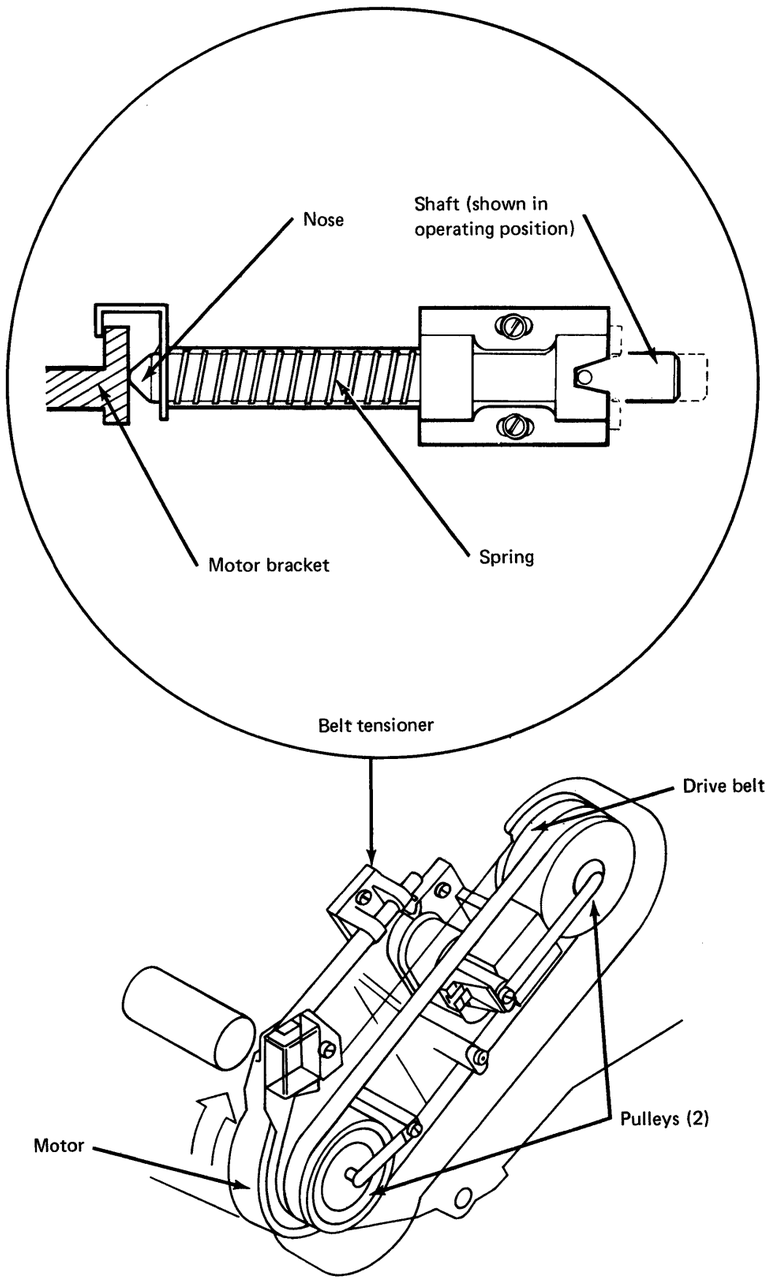
Brake assembly





Drive Belt Tensioner

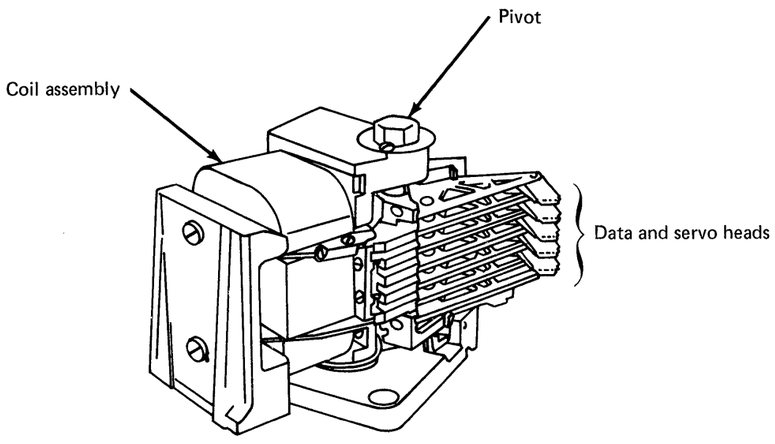
The drive belt tensioner is a spring-loaded shaft assembly that maintains a constant pressure against the motor bracket. The pressure on the motor bracket ensures that the drive belt remains tight and does not slip during operation.



Actuator Assembly

The actuator assembly is mounted on a pivot beside the outer edges of the disks. The movable data heads and the servo head, which are attached to arms located on one end of the actuator assembly, are moved over the disk surfaces to the specified cylinder by the actuator.

A rectangular coil, positioned in the field of a permanent magnet, is mounted on the other end of the actuator assembly. When current passes through the coil, it moves the servo and data heads in an arc across the disk surface, and allows all cylinders to be accessed.

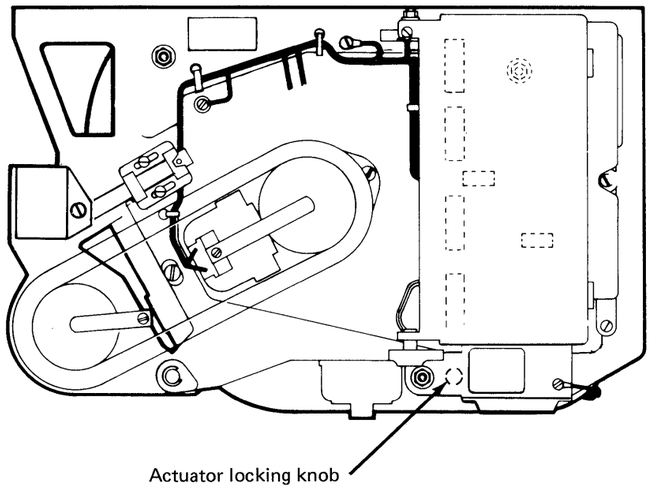


Actuator assembly

The read preamplifiers for the servo and data heads, the head-selection circuits, and the write-driver circuits are also mounted on the actuator assembly.

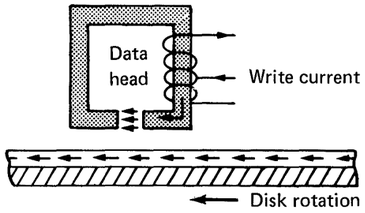
During start/stop cycles, the actuator retracts the heads to an area on the disk surfaces not used for data recording. If power fails or if a loss of disk speed occurs, a retract spring moves the heads to the guard band and landing zone. A magnetic catch on the actuator holds the heads over the zone when the heads are retracted and when the power has been removed.

Actuator Locking Knob. A mechanical lock located on the base casting is used to lock the actuator in the retracted position during removal or installation of the disk enclosure, or during shipment.

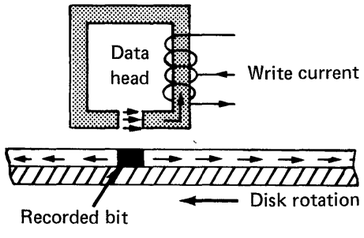


Data Heads

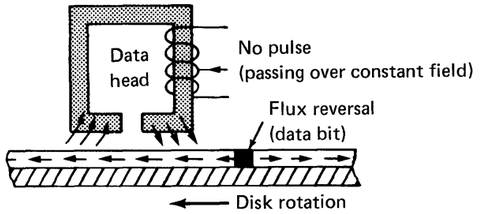
Data is read and written by the data heads when the disk is spinning at 3125 rpm. When writing, a 0-bit or 1-bit is recorded by reversing the direction of the current in the data-head coil (with the exception of a 0 followed by a 1), which reverses the flux direction in the pole piece and reverses the flux in the gap.

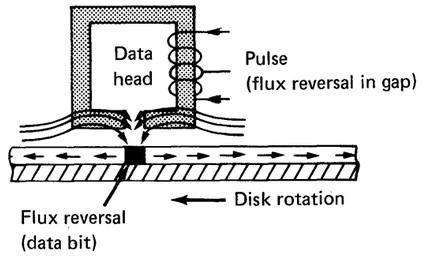


At the instant that the flux in the pole piece gap reverses, the direction of magnetization changes on the disk surface. Each reversal represents a recorded 0-bit or 1-bit.

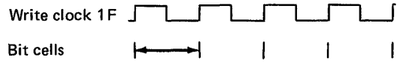


During a read operation, when the recording surface is magnetized in one direction, a constant flux flows and no output voltage is induced into the data-head coil. However, when a recorded bit (a 180-degree flux reversal) passes the gap, the flux flowing through the ring and the coil reverses and induces a pulse in the data-head coil.



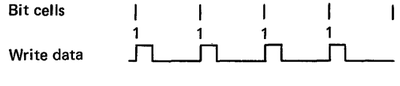


When writing data, pulses read by the dedicated servo head from the servo surface are used by the disk unit circuits to develop the write clock. The period of time during which a data bit may be written is referred to as a bit cell. A bit cell is defined by the 'write clock 1F' line.



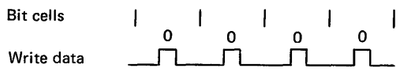
Writing 1-Bits

The 1-bits are always written at the beginning of a bit cell.

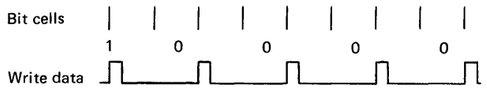


Writing 0-Bits

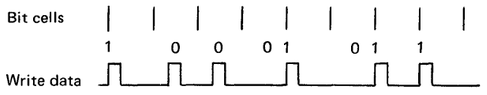
With one exception, 0-bits are written in the middle of the bit cell.



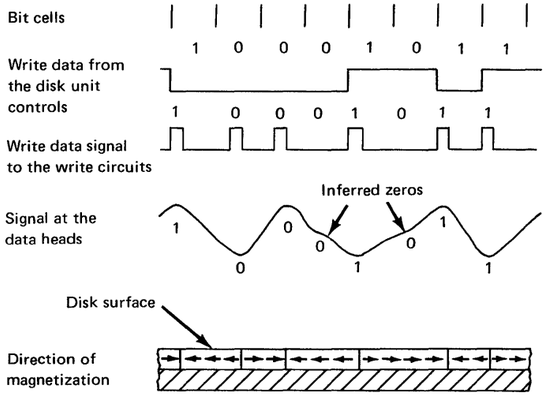
When a 0 immediately procedes a 1, no bit is written. The absence of a change in flux reversal during bit-cell time represents a 0.



By writing hex 8B both methods of writing 0-bits and the method of writing 1-bits can be illustrated:

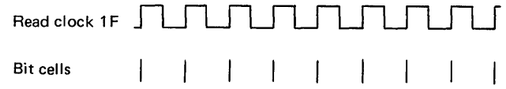


The data to be written is transmitted to the disk unit circuits from the disk unit controls (located in the primary unit) via the 'write data' line. The data is then modulated and encoded and then sent to the write driver, which controls the direction of the current flow in the data head. The change in current flow direction results in changes to the direction of magnetization on the disk surface.



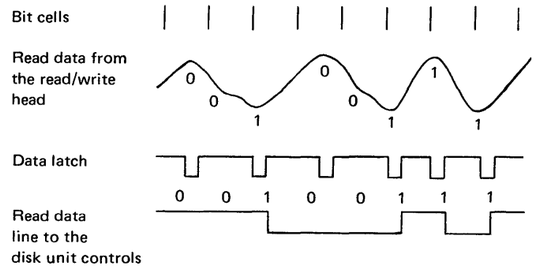
Reading Data Bits

A voltage-controlled oscillator develops the read-clock pulses and synchronizes them to the data pulses being read from the disk. The 'read clock 1F' line is used to define the bit cells.



Pulses that occur on the 'read data' line are identified as either 0's or 1's, depending on when they occur relative to the bit cells.

If the pulse occurs at the beginning of the bit cell, it signifies a 1; if the pulse occurs in the middle of the bit cell, it signifies a 0. If no pulse appears either at the beginning or in the middle of a bit cell, a 0 (inferred zero) is designated for that cell.

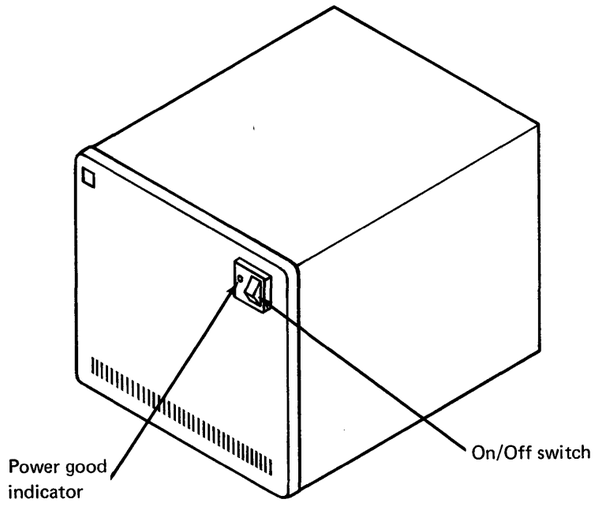


The read data signal from the data head is shaped and amplified by the disk unit circuits. The voltage-controlled oscillator, that develops the read-clock pulses, constantly monitors the bits being read and varies the oscillator frequency to keep the read clock and read data in synchronization.

Operator Panel

The operator panel, which is located on the front of the disk storage unit, contains an On/Off switch and a power-good indicator.

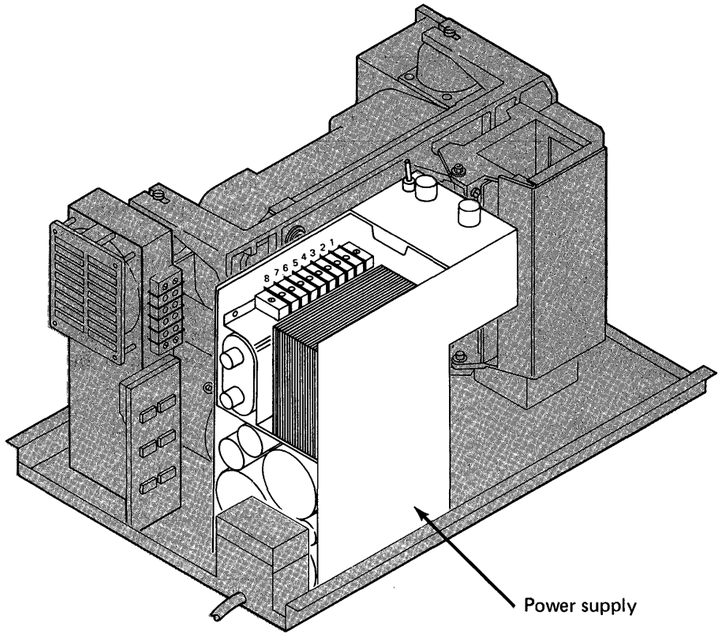
- On/Off switch—this switch turns the unit's ac power on or off.
- Power-good indicator—when the indicator lights, it signifies that the dc voltages are within tolerance and that the ac voltage has been applied to the drive motor. The indicator is a light emitting diode (LED).



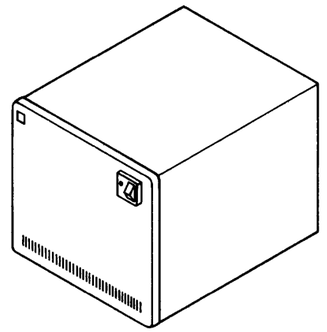
Power Supply

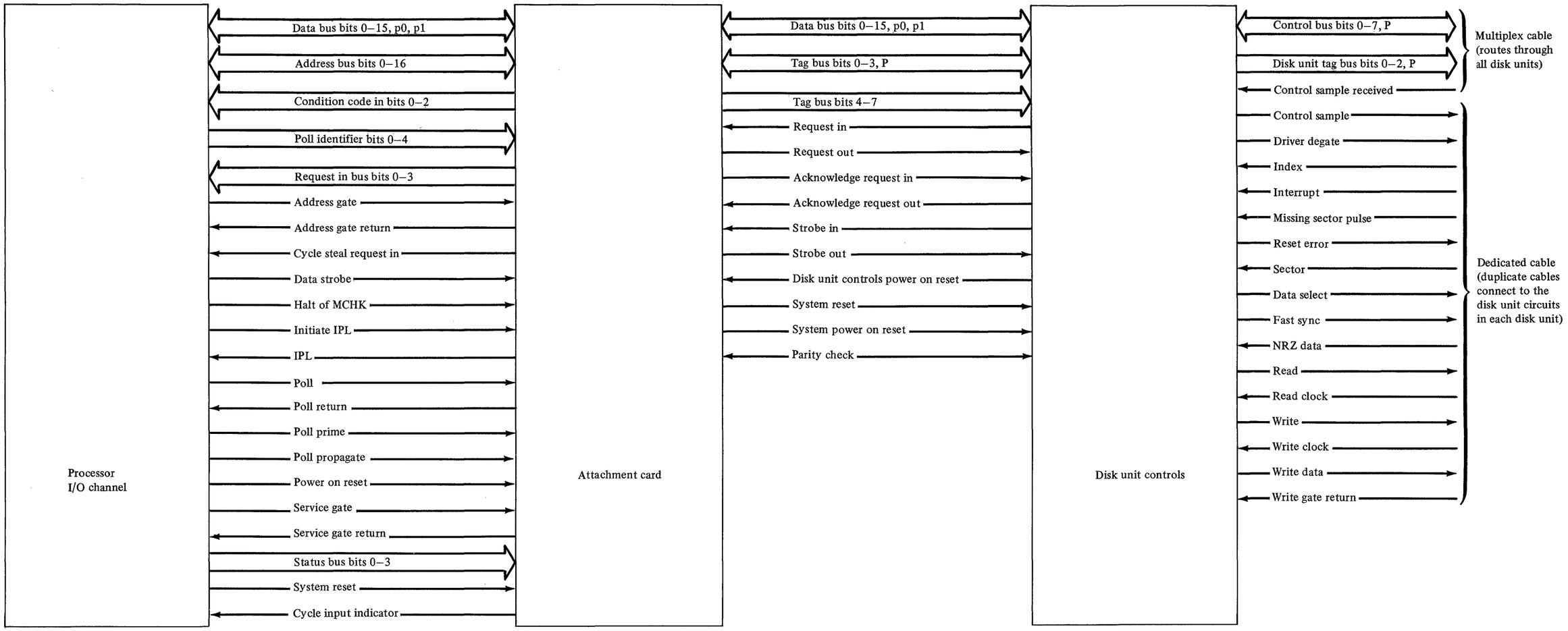
The power supply provides all of the ac and dc power used within the disk storage unit; it uses a single-phase ac power source to provide ac voltages to the drive motor and cooling fans, and the following dc voltages:

- −4 volts, −12 volts, +5 volts, +12 volts, and +24 volts for the disk enclosure and disk unit circuits
- −5 volts, −8.5 volts, and +5 volts for the disk unit controls



Chapter 3.
Circuit Functions




Processor
I/O channel
Data bus bits 0–15, p0, p1
Address bus bits 0–16
Condition code in bits 0–2
Poll identifier bits 0–4
Request in bus bits 0–3
Address gate
Address gate return
Cycle steal request in
Data strobe
Halt of MCHK
Initiate IPL
IPL
Poll
Poll return
Poll prime
Poll propagate
Power on reset
Service gate
Service gate return
Status bus bits 0–3
System reset
Cycle input indicator
Attachment card
Data bus bits 0–15, p0, p1
Tag bus bits 0–3, P
Tag bus bits 4–7
Request in
Request out
Acknowledge request in
Acknowledge request out
Strobe in
Strobe out
Disk unit controls power on reset
System reset
System power on reset
Parity check
Disk unit controls
Control bus bits 0–7, P
Disk unit tag bus bits 0–2, P
Control sample received
Control sample
Driver degate
Index
Interrupt
Missing sector pulse
Reset error
Sector
Data select
Fast sync
NRZ data
Read
Read clock
Write
Write clock
Write data
Write gate return
Multiplex cable (routes through all disk units)
Dedicated cable (duplicate cables connect to the disk unit circuits in each disk unit)

Line Definitions

The diagram on the previous page represents the signal lines between the processor I/O channel, the attachment feature, the disk unit controls, and the disk storage unit. The following text is a brief definition of these lines; the diagram is repeated on succeeding pages for ease of reference.

Note: For a complete description of all processor I/O channel lines, refer to the appropriate Series/1 processor theory diagrams.

Processor I/O Channel to Attachment Feature

Address Bus (Bits 0–16)

The 'address bus' is used for direct program control (DPC) selection of the 4963 and for storage address presentation by a cycle-stealing disk unit. The 'address bus' is 17 bits; it is received by all attachments installed on the processor I/O channel. All I/O devices that are capable of cycle stealing activate bits 0–15. The processor drives bits 0–16.

During DPC sequences, the 'address bus bits' 0–15 are equal to bits 0–15 of the first word of the immediate device control block (IDCB). If bit 16 is active, it indicates that a DPC sequence is taking place. During a cycle steal data transfer, the attachment places the main storage address on the 'address bus', using bits 0–15. Bit 16 is activated by an I/O device.

During a main storage access, address bits 0–15 represent a true main storage address. Bit 16 is not used, indicating to the processor that a main storage access is taking place.

Data Bus (Bits 0–15, P0, and P1)

The 'data bus', an 18-bit bidirectional bus consisting of two 8-bit bytes of data (bits 0–7 and 8–15) and two parity bits (P0 and P1), transfers data and control information between the processor and the attachment. Parity bit P0 is used to maintain an odd parity for bits 0–7; parity bit P1 is used to maintain an odd parity for bits 8–15.

During command sequences, 'data bus' bits 0–15 are the same as bits 16–31 of the IDCB.

During interrupt service sequences, the data bus transfers the interrupt identification (ID) word to the processor. Data bus bits 0–15, sent by the attachment to the processor, correspond to bits 0–15 of the interrupt ID word (see "Interrupts" in Chapter 4).

During a cycle-steal sequence, the 'data bus' bits have the following meanings:

- *Output word transfer*—bits 0–15 are the same as the contents of the word at the main storage location that is addressed by the attachment. The storage address must be an even address. The attachment specifies that an output word transfer is taking place by presenting the 'cycle input indicator' signal equal to a logical 0.
- *Input word transfer*—bits 0–15 are the same as the contents of the word at the main storage location that is addressed by the attachment. However, the attachment specifies that an input word transfer is taking place by presenting the 'cycle input indicator" signal equal to a logical 1.

Odd parity is maintained on the data bus during all I/O sequences.

Cycle Input Indicator

The 'cycle input indicator' tag defines the direction of data transfer over the 'data bus'. The tag is activated to a logical 1 by either the attachment or by the processor when a data transfer to main storage occurs. When a data transfer from main storage occurs, the tag is not activated, indicating a logical 0 (the normal state of the line).

This line is valid from the rise of 'service gate return' until the fall of 'service gate'; it must not change state during this period.

Address Gate

When the 'address gate' tag (an outbound tag) is active, it indicates that the attachment may now respond to initial selection and can begin the execution of the command specified by bits 0–7 of the address bus.

Address Gate Return

The attachment raises the 'address gate return' tag to indicate that it has received the 'address gate' tag, that immediate status is on the 'condition code in' bus, and that data is on the data bus if bit 1 of the address bus is inactive (logical 0).

If the 'address gate return' tag does not become active within three microseconds after the 'address gate' tag becomes active, an I/O instruction condition code of 0 (device not attached) is generated, the sequence is terminated, the 'address gate' tag becomes inactive, and the 'address bus' is reset.

Request In Bus

The 'request in bus' is a 4-bit bus (bits 0–3) used by the attachment to either request an interrupt or to access main storage.

When the attachment detects an interrupt condition, it activates one of the 'request in bus' bits. The level field of the Prepare command determines which bit is activated.

The attachment may activate an interrupt request bit only when the I-bit (bit 31 of the IDCB for a Prepare command) is equal to a 1. The interrupt request remains active until the attachment captures a poll, receives 'halt or MCHK', receives a device or a system reset, or receives a 'power-on reset'.

Cycle-Steal Request In

The attachment activates this line if a disk storage unit requires cycle stealing to access main storage. The line remains active until the attachment feature captures a poll, receives 'halt or MCHK', receives 'system reset', or receives 'power on reset'.

Poll or Poll Prime

The 'poll' tag is generated by the processor I/O channel and is sent serially to all attachments on the channel. The purpose of this tag is to resolve any contentions that exist between two or more attachments, on the same level, that have interrupt requests or cycle-steal requests pending. Each attachment receives the 'poll' tag. If an interrupt or a cycle-steal request is not pending, the attachment sends the 'poll' tag to the next device on the I/O channel via its 'poll propagate' line.

When the 'poll' tag and the 'poll prime' tag are received by the attachment, the attachment recognizes that a poll is occurring. The attachment performs a logical compare of the poll ID bits from the processor I/O channel and the ID bits in the prepare level register. An equal compare of the poll ID bits logically ANDed with 'poll' and 'poll prime' is called a poll capture. Once the poll is captured, the attachment responds with 'poll return'. If the poll capture does not occur, the 'poll' tag is propagated to the next device on the channel and the attachment takes no further action as a result of the poll until the next poll occurs.

Because of the serial nature of the 'poll' line, the physical position of the attachment on the channel is a major determinant of the priority for servicing contending cycle-steal requests and for servicing contending interrupt requests at the same interrupt level. The attachments that are located in positions closest to the processor are the first attachments in the serial poll chain and, therefore, have the highest priority.

Poll Propagate

The 'poll propagate' tag is activated by the attachment within 200 nanoseconds after the 'poll' tag has been received, if the 'poll' tag has not been captured. However, if the attachment receives a 'power on reset', a 'system reset', or a 'halt or MCHK', this tag deactivates regardless of the state of the 'poll' tag.

Poll Identifier Bus

The poll identifier is a 5-bit bus that is used to indicate the type of poll occurring on the processor I/O channel. The channel places a value on the poll identifier bus prior to raising the 'poll' tag; the value remains valid until the channel receives a poll return.

The significance of the poll identifier bus bits is as follows:

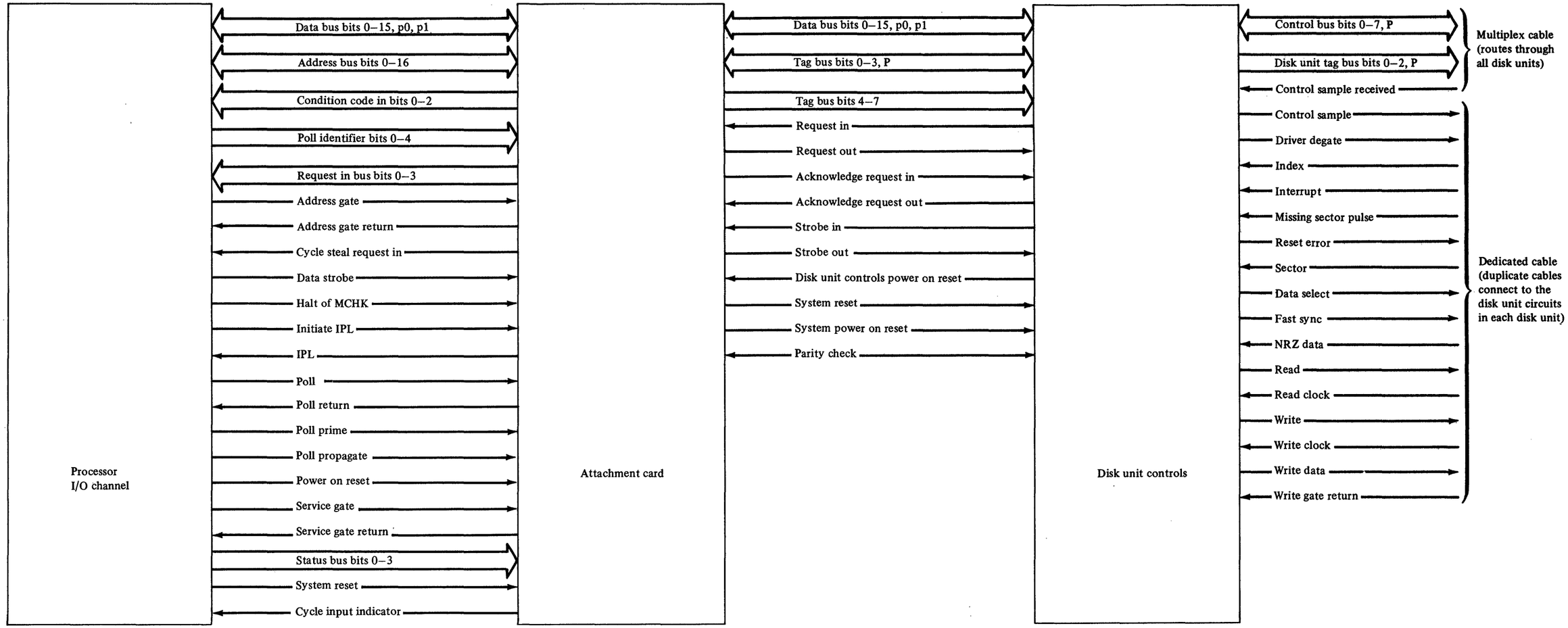
Poll ID bits 0 1 2 3 4	
0 0 0 0 0	Poll for interrupt level 0
0 0 0 0 1	Poll for interrupt level 1
0 0 0 1 0	Poll for interrupt level 2
0 0 0 1 1	Poll for interrupt level 3
1 0 0 0 0	Quiescent value
1 X X 1 1	Poll for a cycle-steal

Service Gate

The outbound 'service gate' tag indicates to the attachment that a cycle-steal or interrupt service sequence can begin, if the attachment captured the last poll.

Service Gate Return

'Service gate return' is an inbound tag sent by the attachment to the I/O processor channel to indicate that it has recognized 'service gate' and that the inbound information required by either the cycle-steal sequence or the interrupt service sequence has been placed on the channel.


Data bus bits 0–15, p0, p1
Address bus bits 0–16
Condition code in bits 0–2
Poll identifier bits 0–4
Request in bus bits 0–3
Address gate
Address gate return
Cycle steal request in
Data strobe
Halt of MCHK
Initiate IPL
IPL
Poll
Poll return
Poll prime
Poll propagate
Power on reset
Service gate
Service gate return
Status bus bits 0–3
System reset
Cycle input indicator
Processor
I/O channel
Attachment card
Data bus bits 0–15, p0, p1
Tag bus bits 0–3, P
Tag bus bits 4–7
Request in
Request out
Acknowledge request in
Acknowledge request out
Strobe in
Strobe out
Disk unit controls power on reset
System reset
System power on reset
Parity check
Disk unit controls
Control bus bits 0–7, P
Disk unit tag bus bits 0–2, P
Control sample received
Multiplex cable (routes through all disk units)
Control sample
Driver degate
Index
Interrupt
Missing sector pulse
Reset error
Sector
Data select
Fast sync
NRZ data
Read
Read clock
Write
Write clock
Write data
Write gate return
Dedicated cable (duplicate cables connect to the disk unit circuits in each disk unit)

Condition Code In Bus

The 'condition code in bus' is a 3-bit bus used by the attachment to indicate I/O instruction condition codes, interrupt condition codes, or cycle-steal address key information to the processor I/O channel. 'Condition code in' information is sent to the channel with the appropriate inbound tag (either 'address gate return' or 'service gate return') during command, interrupt, and cycle-steal sequences.

Information on the 'condition code in bus' is valid from the time that either 'address gate return' or 'service gate return' becomes active until the time that either 'address gate' or 'service gate' becomes inactive.

Status Bus

The 'status bus' is a 4-bit outbound bus used by the processor I/O channel to indicate to the attachment that an error condition has been detected. The bits have the following meaning:

Bit	Meaning
0	Storage data check
1	Invalid storage address
2	Protect check
3	Interface data check

The attachment automatically retries the specified operation one time for these error conditions when the suppress exception (SE) bit of the DCB control word is on. If the operation fails a second time, a hard error condition is posted (condition code 2 or 6) and the appropriate bit in the interrupt ID word is set to 1.

The attachment retains this information in the interrupt status byte for presentation to the processor I/O channel via the interrupt ID word at interrupt presentation time. Bits 0–3 of the "status bus" are represented by bits 4–7 of the interrupt ID word.

Data Strobe

The 'data strobe' line is an outbound tag to the attachment. It is activated during command, interrupt, or cycle-steal service sequence.

Initiate IPL

The 'initiate IPL' line is an outbound tag from the processor I/O channel to the IPL source on the system. The tag is a signal to the IPL source that the processor requires an IPL. It is held active until the IPL source responds with the 'IPL' tag. Bits 0 and 1 of the 'status bus' are used to select the primary or alternate IPL source, respectively; the bit is activated concurrently with 'initiate IPL'.

IPL

'IPL' is an inbound tag activated by the IPL source attachment either to respond to the 'initiate IPL' tag or to indicate to the processor that a another processor is initiating the IPL. The IPL information is loaded into storage via cycle-steal sequences.

The attachment activates the 'IPL' tag and begins transferring information to the processor after the processor performs a system reset. The 'IPL' tag remains active until the IPL is complete.

Halt or MCHK

The 'halt or MCHK' tag is an outbound tag that indicates that either a Halt command has been encountered in the program or that a machine check class interrupt has occurred. This tag resets any error or busy conditions that exist in the disk subsystem.

System Reset

The 'system reset' tag is an outbound tag sent by the channel to all I/O devices. It resets any error or busy conditions that exist in the disk subsystem.

Power-On Reset

'Power-on reset' is a control line sent by the power supply in the processor to all system components; it holds them in a system reset state. The 'power on reset' line is activated during power-on or power-off sequences.

Attachment to Disk Unit Controls

There are 37 lines between the attachment and the disk unit controls. The lines consist of:

- 18 data bus lines—two 8-bit bytes and two parity bits
- 13 control lines—9 'tag bus' lines, plus request in, request out, acknowledge request in, and acknowledge request out
- 2 data strobe lines—strobe in and strobe out
- 3 reset lines—disk unit power on reset, system reset, and system power on reset
- 1 bidirectional parity check line

Data Bus

Two bytes of data (plus a parity bit for each byte) are transferred in parallel either to or from the attachment via the 'data bus'. The bidirectional 'data bus' lines are gated to the disk unit controls during write operations and are gated to the attachment during read operations.

Tag Bus

The 'tag bus' lines define the type of operation that is occurring between the attachment and the disk unit controls. Five lines (bits P, 0, 1, 2, 3) are bidirectional; four lines (bits 4, 5, 6, 7) are outbound lines. During an inbound sequence, only bits P, 0, 1, 2, and 3 are used. The parity bit is used to maintain an odd parity for these bits. During an outbound sequence, bits P, 0, 1, 2, 3, 4, 5, 6, and 7 are used. The parity bit, in this instance, is used to maintain an odd parity for all 'tag bus' bits. The definitions of the various 'tag bus' patterns are given in Chapter 4 "Disk Operations".

Request In

'Request in' is an inbound control line used by the disk unit controls. It indicates to the attachment that the disk unit controls either has data to transfer or requires an interrupt. The line is used by the attachment to gate-in the 'tag bus' bits P, 0, 1, 2, and 3.

Request Out

This line is activated by the attachment when it has data to transfer to the disk unit controls. The nine outbound 'tag bus' lines are activated by 'request out'. If 'request out' and 'request in' become active concurrently, 'request out' takes precedence over 'request in'. Under these conditions, 'request in' is deactivated and inhibited by the disk unit controls; however, 'request out' is not activated if 'request in' has been accepted by the attachment. The attachment indicates that it has accepted 'request in' by activating the 'acknowledge request in' line.

Acknowledge Request In

The attachment activates this line in response to the 'request in' line that has been activated by the disk unit controls. When the 'acknowledge request in' line becomes active, it indicates that the attachment is ready to begin the type of operation defined by the 'tag bus' lines.

Acknowledge Request Out

The disk unit controls activates this line when it receives 'request out' from the attachment and is ready to begin the type of operation defined by the 'tag bus' lines. If a parity check occurs on the 'tag register bus', the 'parity check' line is activated instead of 'acknowledge request out'.

Strobe In

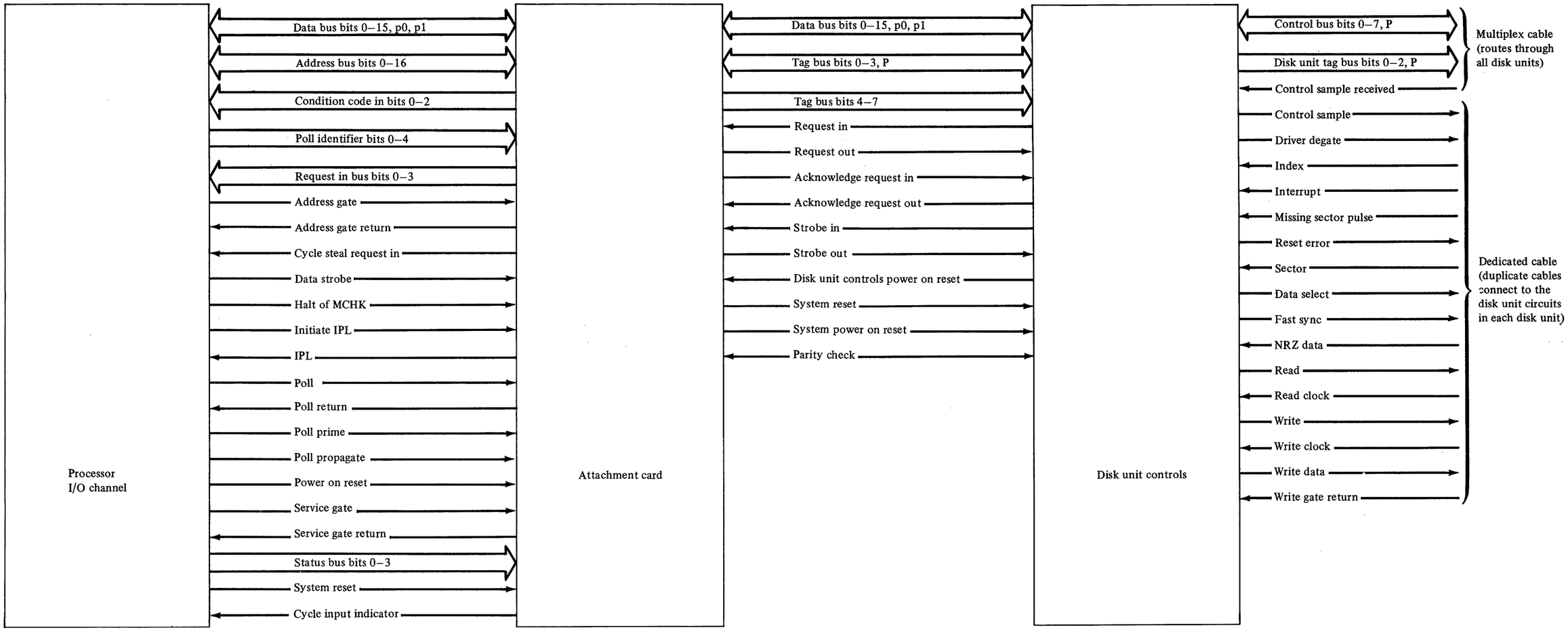
The inbound line, 'strobe in', is used to gate data into the attachment data register. Data is gated into the register at the leading edge of the 'strobe in' pulse and latched into the register at the trailing edge of the pulse.

Strobe Out

'Strobe out' is an outbound line from the attachment to the disk unit controls. It is used by the disk unit controls to latch the data into the data register.

Disk Unit Controls Power-On Reset

This line is activated by the disk unit controls to inhibit the 'strobe in' and 'request in' lines going to the attachment when a 'power good' condition does not exist in disk storage unit 0.


Processor
I/O channel
Data bus bits 0–15, p0, p1
Address bus bits 0–16
Condition code in bits 0–2
Poll identifier bits 0–4
Request in bus bits 0–3
Address gate
Address gate return
Cycle steal request in
Data strobe
Halt of MCHK
Initiate IPL
IPL
Poll
Poll return
Poll prime
Poll propagate
Power on reset
Service gate
Service gate return
Status bus bits 0–3
System reset
Cycle input indicator
Attachment card
Data bus bits 0–15, p0, p1
Tag bus bits 0–3, P
Tag bus bits 4–7
Request in
Request out
Acknowledge request in
Acknowledge request out
Strobe in
Strobe out
Disk unit controls power on reset
System reset
System power on reset
Parity check
Disk unit controls
Control bus bits 0–7, P
Disk unit tag bus bits 0–2, P
Control sample received
Control sample
Driver degate
Index
Interrupt
Missing sector pulse
Reset error
Sector
Data select
Fast sync
NRZ data
Read
Read clock
Write
Write clock
Write data
Write gate return
Multiplex cable (routes through all disk units)
Dedicated cable (duplicate cables connect to the disk unit circuits in each disk unit)

System Reset

'System reset' is an outbound line from the attachment used to reset the disk unit controls to a non-busy, error free, cleared state. The line is activated when either 'halt or MCHK', 'power on reset', or 'system reset' from the processor I/O channel becomes active.

System Power On Reset

During a system power-on reset, this outbound line is used to initialize the disk unit controls to a known cleared state. It performs the same functions as the 'system reset' line.

Parity Check

'Parity check', a bidirectional line, is activated when an out-of-parity condition is detected on either the 'data bus' or the 'tag bus'. The direction of the 'parity check' line is determined by the origin of the previous request. If the previous request was a 'request in', the attachment activates the line. If the previous request was a 'request out', the disk unit controls activates the line.

Data parity is checked at the trailing edge of the 'strobe in' or 'strobe out' pulses. The disk unit controls must reset the 'parity check' line before deactivating 'acknowledge request out' or before activating the next 'request in'.

Disk Unit Controls to Disk Storage Unit

Control Bus

The bidirectional 'control bus' consists of 8 bits (0–7) and a parity bit (P); the parity bit is used to maintain odd parity. The bus is used to transfer information to and from each disk unit. The significance and the direction of the information on the bus is determined by the decode of the disk unit 'tag bus'. Parity is checked by the disk unit for outbound information; parity is generated by the disk unit for inbound information.

Disk Unit Tag Bus

This bus is an outbound bus going from the disk unit controls to all disk units. It defines the significance and the direction of the information on the 'control bus'. The disk unit 'tag bus' consists of 3 bits (0–2) and a parity bit (P) that is used to maintain odd parity.

This bus is used to gate head and cylinder selection information located on the 'control bus' from the disk unit controls into the disk unit circuits. It is also used to gate sense, status, and diagnostic sense information onto the 'control bus' from the disk unit circuits.

Control Sample Received

This is an inbound line that indicates to the disk unit controls that 'control sample' has been received and responded to.

Control Sample

'Control sample' is used with disk unit 'tag bus' codes 001 and 010 to gate the head or cylinder selection information to the selected disk unit. 'Control sample' also gates sense and status information to the control bus for codes other than 001 and 010.

Driver Degate

When active, this outbound line prevents sense and status information from being gated to the 'control bus'.

Index

This inbound line indicates that the beginning of the first sector of any track is occurring.

Interrupt

This inbound line becomes active after the disk unit is powered on, when the disk unit is at 'home' and 'ready', when 'seek complete' has occurred, and when certain error conditions have occurred within the disk unit.

Missing Sector Pulse

This line indicates to the disk unit controls that the disk unit circuits failed to detect a sector pulse during the time that the pulse was expected.

Reset Error

This line is used to reset the 'data unsafe' or 'command error' sense bits. It is also used to clear an interrupt.

Sector

This inbound line is active at the beginning of all sectors after the first sector.

Data Select

This line is used by the disk unit circuits to gate 'read' or 'write'. 'Data select' is active only in one disk unit at any time.

Fast Sync

This outbound line forces the phase-locked oscillator (PLO) into synchronization when any operation occurs that would normally require a long period of time to resynchronize. An example of when fast synchronization is necessary is during a change from a write status to a read status.

NRZ Data

This inbound line is used to send serial data read from the disks to the disk unit controls.

Read

This outbound line is used to activate the read circuits located in the disk unit. It is gated into the disk unit circuits by the 'data select' line.

Read Clock

This inbound line is used by the disk unit controls to clock read data into the deserializer. It is synchronized to the data being read during read operations.

Write

This line is an outbound line used by the disk unit circuits to activate the write circuits. It is gated into the disk unit circuits by the 'data select' line.

Write Clock

This inbound line is used by the disk unit controls to synchronize the 'write data', being sent to the disk unit circuits, to the servo clock pulses that are read from the dedicated servo surface. This line is the same as the '1F write clock' line generated in the disk unit circuits.

Write Data

This line is used to send serialized binary data to the disk unit circuits. 'Write data' is synchronized to the 'write clock' line.

Write Gate Return

This inbound line indicates to the disk unit controls that the write current to the data heads is active.

Attachment Feature Card

The attachment feature physically connects and logically adapts the processor I/O channel to the disk units.

It consists of the following components:

- A digital controller
- Two 16-bit (plus two parity bits) I/O data registers that provide a cycle-steal data bypass (with minimum controller intervention) between the processor I/O channel and the disk unit controls, using auto mode
- Interrupt status and control circuits for the processor I/O channel and the disk unit controls

The attachment's digital controller performs the following functions:

- Interprets the immediate device control block (IDCB) of the operate I/O instruction
- Executes the IDCB command
- It fetches, in cycle-steal mode, the device control block (DCB) specified by the IDCB
- Controls the starting and stopping of the automatic cycle-steal data transfers in auto mode
- Monitors and checks the accuracy of all data transfers
- Provides status information, reports condition codes, and handles interrupts to the processor
- Provides automatic error-recovery procedures
- Provides built-in automatic diagnostics
- Handles, automatically, alternate sector recovery
- Provides for variable length initial program load (IPL) records (up to 64K bytes)
- Allows the attachment circuits to be tested without disconnecting the attachment-to-disk unit controls cables
- Optimizes data transfers when instructions are issued to more than one disk unit

Information is transferred from the processor I/O channel to the disk unit controls in either control mode or in auto mode. Control mode includes all attachment initiated transfers that are begun by activating the 'request out' line. In this mode, the information passes through the controller in the attachment. In auto mode, data is transferred using the cycle-steal data bus. Auto mode is the normal mode of operation for data transfers. In this mode, the controller acts as a supervisor and intervenes only during the beginning and ending of data transfers, during interrupt servicing, and during error handling.

When the controller is operating in control mode, it requests information transfers by activating the 'request out' line going to the disk unit controls. The controller loads the information to be transferred to the disk unit controls directly into the attachment data register. If information is to be transferred from the disk unit controls to the attachment, the information must be loaded into the cycle-steal data register (after being strobed into the attachment data register) before it can be transferred to the controller. When data is being transferred between the processor I/O channel and attachment controller, the data passes only through the cycle-steal data register.

When the controller is operating in auto mode, it sets or verifies the condition of the status latches that apply to the cycle-steal data bus. The disk unit controls initiates data transfers by activating 'request in'; then, the data records are transferred between the processor I/O channel and the disk storage unit. If the last record to be transferred (during a write operation) is less than 256 bytes, zeros are inserted (padded) to complete the record. During the read operation, padded zeros are read from the disk unit, but they are not transferred to the processor I/O channel.

The following diagrams of the attachment feature card are for instructional purposes only. The keys in the text refer to keys in the diagrams. Refer to the 'Legend' located in the beginning of this document for an explanation of the symbols.

The first word of the IDCB is placed in the command register 3 and the device address compare 4. If the device address compares with the attachment's address jumpers, the controller 1 analyzes and executes the command that is in the command register 3.

If the command initiates a DPC type of operation, the immediate data field (second word of the IDCB) is used for data. If the command initiates cycle-steal type operation, the immediate data field is the address of the DCB.

When a Prepare command is issued to the attachment, the prepare level register 5 is loaded with IDCB immediate data field bits 11 through 14. The disk unit's address is also set into the I-bits FFs 6 which sets a disk unit request trigger 7 that corresponds to the disk unit address. This operation designates the disk units that are permitted to interrupt and on which level the units can interrupt the processing operations. The Prepare command is a DPC command.

When a Start command is issued to the attachment, the DCB address register 8 is loaded with the IDCB's immediate data field. This is the address in processor storage of the first word of the DCB. The controller 1 reads the DCB address register 8 and sets the address register 10, the byte counter 11 and the condition code/cycle-steal address key register 12. The controller then sets the cycle-steal input mode latch 13; the cycle-steal request latch 14 begins to cycle-steal 8 DCB words to the controller storage 1 via the cycle-steal data register 15.

When the DCB fetch is complete, the controller 1 loads the address counter 9, the cycle-steal address register 10, the byte counter 11, and the condition code/cycle-steal address key register 12. The cycle-steal input mode latch 13 is set during an input operation and reset during an output operation. The controller 1 then gives control of the cycle-steal data handling to the attachment's data-bypass circuits. This operation is initiated by setting the auto mode latch 2. Cycle-stealing is placed under control of the following automatic cycle-steal control triggers and latches:

- Load data registers trigger 17
- Cycle-steal data register full trigger 18
- Attachment data register full trigger 19
- Cycle-steal request latch 14

The automatic circuits control the address counter 9 incrementing and gating, the byte counter 11 decrementing, the data register 16 gating, zero padding during a write operation, and the disk unit controls signal sequencing.

During an output operation, the cycle-steal data register 15 is gated to the attachment data register via the cycle-steal data bus 20. The ANDing of the 'write' and the 'load data register' 17 signals provides the gate. The cycle-steal data register full trigger 18 sets the load data registers trigger 17.

During an input operation, the attachment data register 16 is gated to the cycle-steal data register 15 via the cycle-steal data bus 20. The ANDing of the 'read' and the load data register trigger 17 signals provides the gate. The attachment data register full trigger 19 sets the load data register trigger 17.

At the completion of an automatic cycle-steal data transfer operation (byte count = 0), the controller 1 resumes control by resetting the auto mode latch 2. At this time, it also reports the condition code, handles interrupts, and if chaining is necessary, fetches additional DCBs.

The signal line sequencing between the attachment and the disk unit controls is controlled by the controller 1. The intput and output lines to the tag register 21 define the type of data transfer operation in progress to the disk unit controls. The request out trigger 22, the 'request in' line 23, the 'acknowledge request out' line 24, and the 'acknowledge request in' line 25 define the direction of data transfer between the attachment and the disk unit controls. The 'strobe in' 26 and 'strobe out' 27 signal lines strobe the data being transferred into the attachment or the disk unit controls, respectively. The attachment 'data bus' 28 is a bidirectional bus that functions as a data path between the attachment and the disk unit controls. The interrupt register 29 is a four-bit register (one bit for each disk unit) that allows interrupts to be posted during automatic cycle-steal operation.

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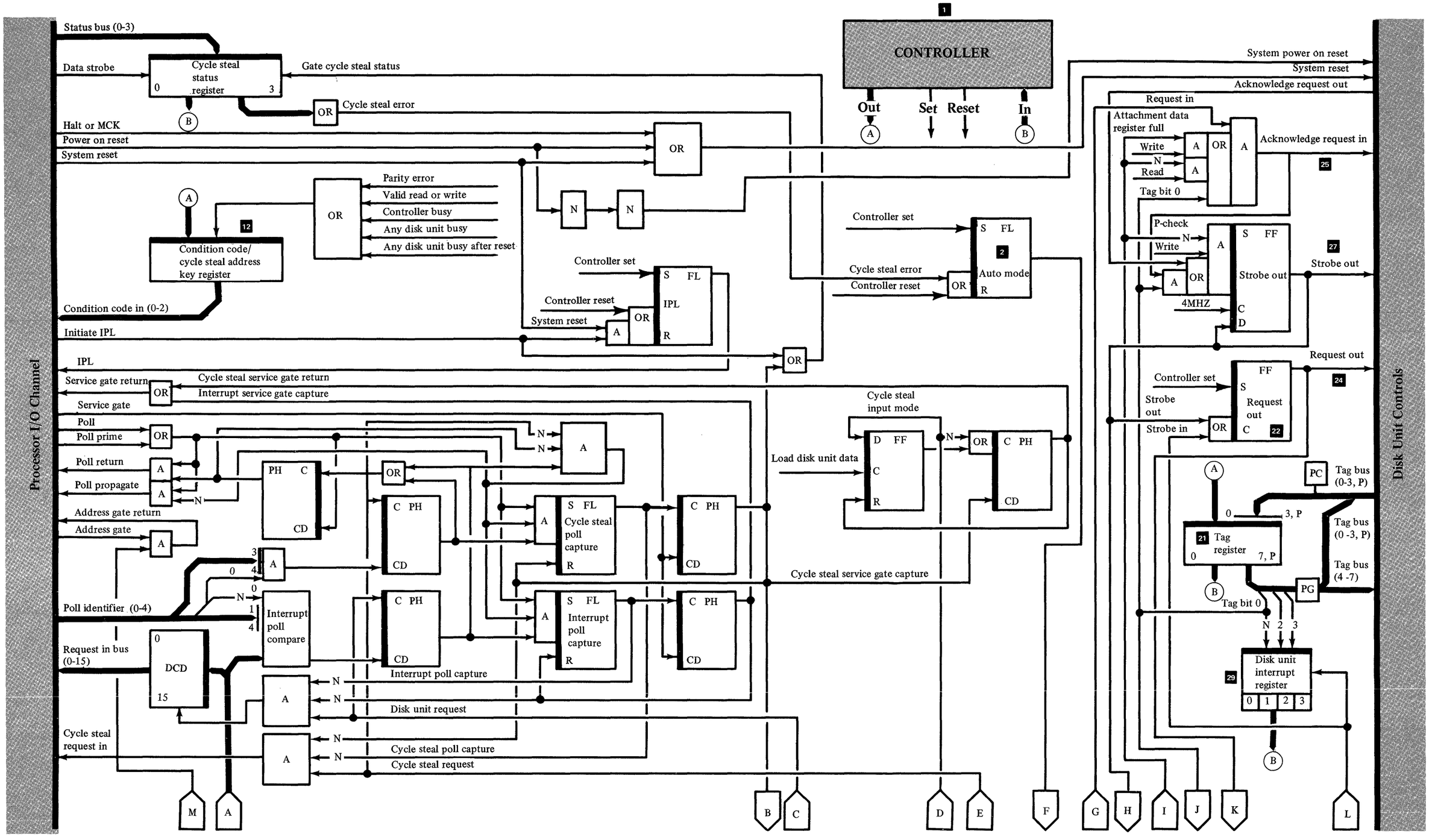
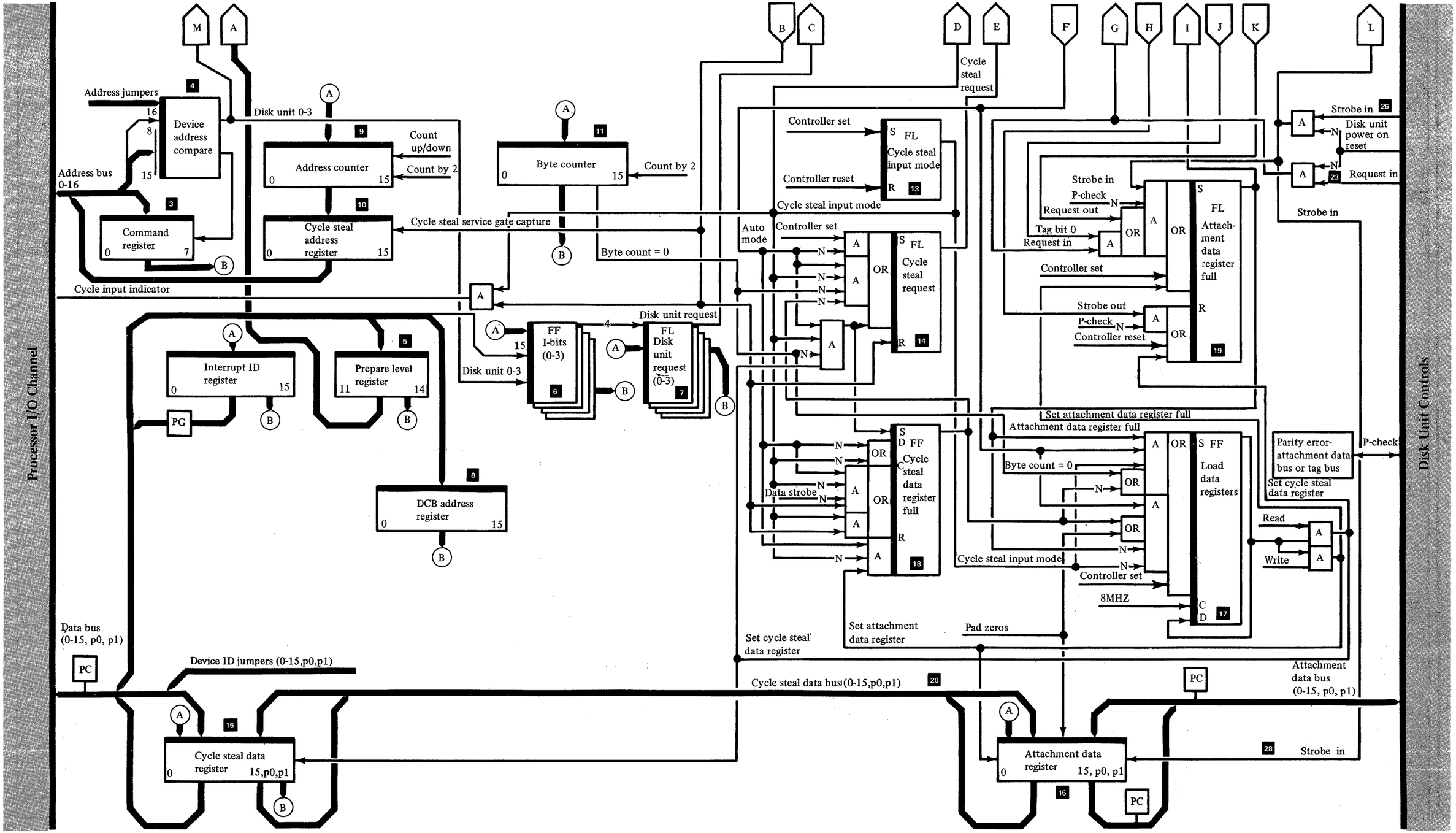
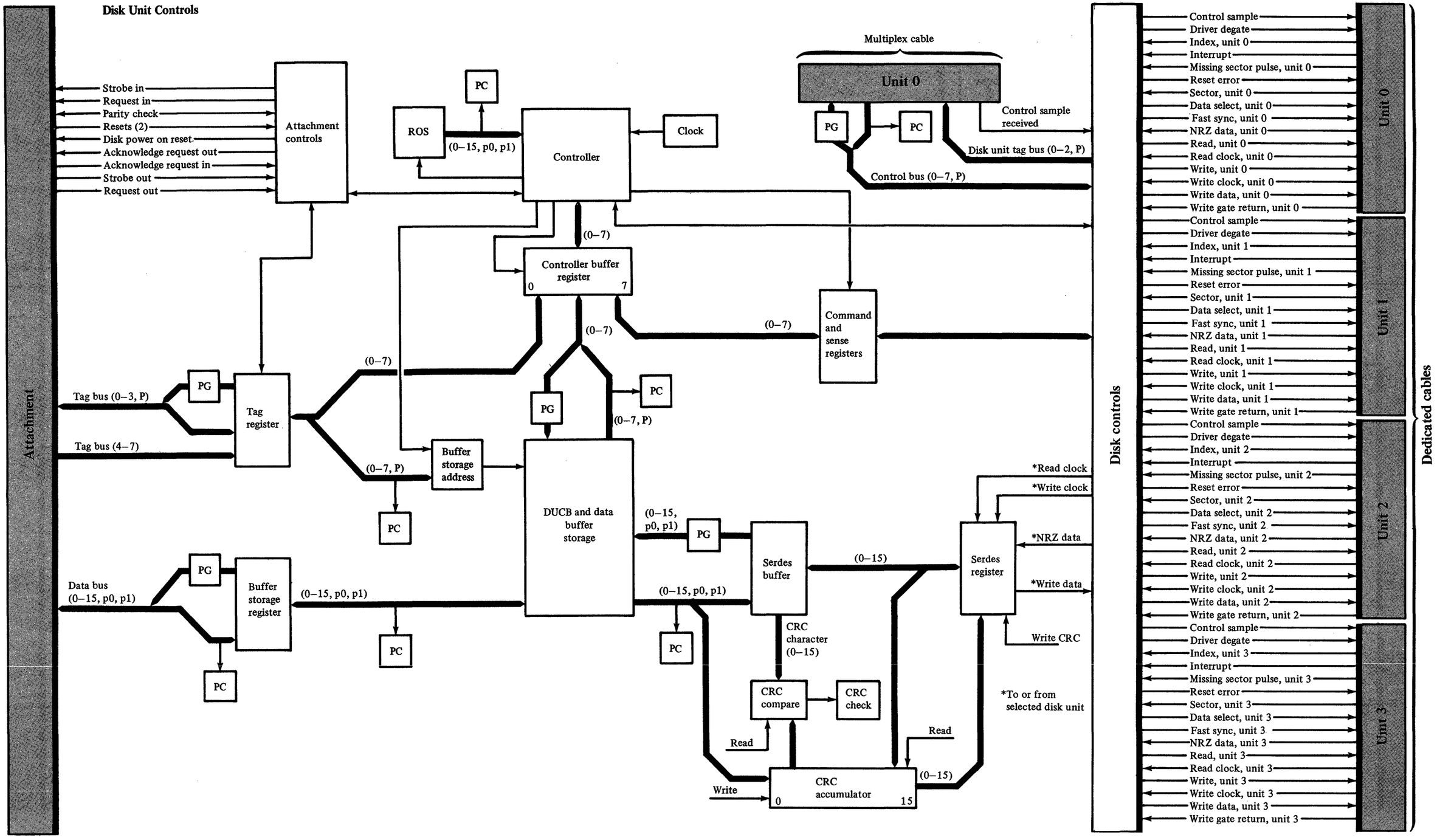

Processor I/O Channel
Disk Unit Controls
CONTROLLER
Out
Set
Reset
In
Status bus (0-3)
Data strobe
Cycle steal status register 0 3
Gate cycle steal status
Cycle steal error
Halt or MCK
Power on reset
System reset
Parity error
Valid read or write
Controller busy
Any disk unit busy
Any disk unit busy after reset
Condition code/ cycle steal address key register
Condition code in (0-2)
Initiate IPL
IPL
Service gate return
Cycle steal service gate return
Interrupt service gate capture
Service gate
Poll
Poll prime
Poll return
Poll propagate
Address gate return
Address gate
Poll identifier (0-4)
Request in bus (0-15)
Cycle steal request in
Interrupt poll compare
Interrupt poll capture
Disk unit request
Cycle steal poll capture
Cycle steal request
Controller set
Controller reset
System reset
Cycle steal error
Auto mode
Cycle steal input mode
Load disk unit data
Cycle steal service gate capture
System power on reset
System reset
Acknowledge request out
Request in
Attachment data register full
Write
Read
Acknowledge request in
Tag bit 0
P-check
Strobe out
4MHZ
Request out
Strobe in
Tag register 0 7
Tag bus (0-3, P)
Tag bus (0 -3, P)
Tag bus (4 -7)
Tag bit 0
Disk unit interrupt register 0 1 2 3
M
A
B
C
D
E
F
G
H
I
J
K
L


Processor I/O Channel
Disk Unit Controls
Address jumpers
Device address compare
Disk unit 0-3
Address bus 0-16
Command register
Address counter
Count up/down
Count by 2
Cycle steal address register
Cycle steal service gate capture
Byte counter
Count by 2
Byte count = 0
Cycle input indicator
Interrupt ID register
PG
Prepare level register
DCB address register
FF I-bits (0-3)
Disk unit request
FL Disk unit request (0-3)
Cycle steal request
Controller set
Controller reset
Cycle steal input mode
Auto mode
FL Cycle steal request
FL Cycle steal input mode
Strobe in
Disk unit power on reset
Request in
P-check
Request out
Tag bit 0
FL Attachment data register full
Strobe out
Set attachment data register full
Attachment data register full
Byte count = 0
Parity error-attachment data bus or tag bus
P-check
Set cycle steal data register
Read
Write
Load data registers
Data strobe
FF Cycle steal data register full
Cycle steal input mode
Controller set
8MHZ
Set attachment data register
Pad zeros
Set cycle steal data register
Data bus (0-15, p0, p1)
Device ID jumpers (0-15,p0,p1)
Cycle steal data bus (0-15,p0,p1)
Attachment data bus (0-15, p0, p1)
Cycle steal data register 15,p0,p1
Attachment data register 15, p0, p1
Strobe in
PC

Disk Unit Controls



Disk Unit Controls

The disk unit controls physically connect and logically adapt the attachment and the disk units. The disk unit controls is on two circuit cards installed on board A2 in the primary disk storage unit. The cards are located adjacent to each other because the tops of the two cards connected via four top-card connectors. These connectors conduct control signals and data between the two cards.

The cards perform the following functions:

- Provide controls between the attachment and the disk units
- Provide a data path between the attachment and the disk units
- Serialize and deserialize data
- Check for cyclic redundancy
- Control the sequencing of all data operations
- Select the data to be read or written, from attachment commands
- Select the head, sector, record, and cylinder numbers for data operations
- Parity check the information coming from the attachment and the disk unit circuits; they generate parity for the information going to the attachment and the disk unit circuits
- Provide a temporary storage area for information going to or coming from the disk units

The preceding simplified diagram and the following text are for instructional purposes only and represent an overview of the disk unit controls. Refer to the 'Legend' located at the beginning of this book for an explanation of symbols.

Data Card

The data card contains the circuits that are used to transfer data and commands between the attachment and the disk unit controls. It contains a controller that uses a data bus and several control lines to send information (data or commands) to the attachment, to the disk units, and to the buffer storage. The controller receives its instructions from a read only storage (ROS) module. This card also contains the attachment controls that are used to sequence the operations between the attachment and the disk unit controls. The tag register buffers the 'tag bus' information.

Disk Unit Card

The disk unit card contains the disk unit control block (DUCB) and data buffer storage, the data serializer-deserializer (serdes) circuits, the CRC character accumulation and compare circuits, and the disk control circuits.

DUCB and Data Buffer Storage

The buffer storage is a 1024-byte storage device that is used to:

- Store a DUCB for each disk unit
- Provide data buffers for up to three 256-byte records
- Provide an ID compare area

Also, the controller uses a part of storage as a work area for various operations.

Serializer-Deserializer (Serdes)

During write operations, the serdes register serializes parallel data from the serdes buffer. The data is sent to the selected disk unit, bit-by-bit, on the 'write data' line. The write clock from the selected disk unit is used to synchronize the data going to the unit.

During read operations, the serdes register receives the data from the selected disk unit, bit-by-bit, on the 'NRZ data' line. The serdes register deserializes the data and sends it to the serdes buffer in a parallel, 2-byte format (bits 0–15).

CRC Generation and Checking

CRC characters are read and written for the ID field, for data record 1 field, and data record 2 field of each sector.

During a read operation, the CRC accumulator assembles a CRC character from the data being read from the disk. When the disk unit reads a CRC character (previously written on the disk) at the end of one of the previously mentioned fields, the CRC character read and the assembled CRC character are compared by the CRC compare circuits. If the CRCs are equal, the next operation begins. If the CRCs do not compare, a CRC check is indicated and an error recovery procedure is performed.

During a write operation, the CRC accumulator assembles a CRC character while data is being sent to the disk. When the last byte of the data or ID fields is written, the assembled CRC character is gated to the disk unit for writing on the disk.

The CRC characters are not sent to the buffer storage.

Data is parity checked as it is read from buffer storage; parity is generated for data being stored.

Disk Controls

The disk controls checks the accuracy of the data being read or written by the disk units, executes seek and recalibrate commands, and assembles disk unit sense and status information. The disk controls provides a communication path between the disk unit controls and the disk units.

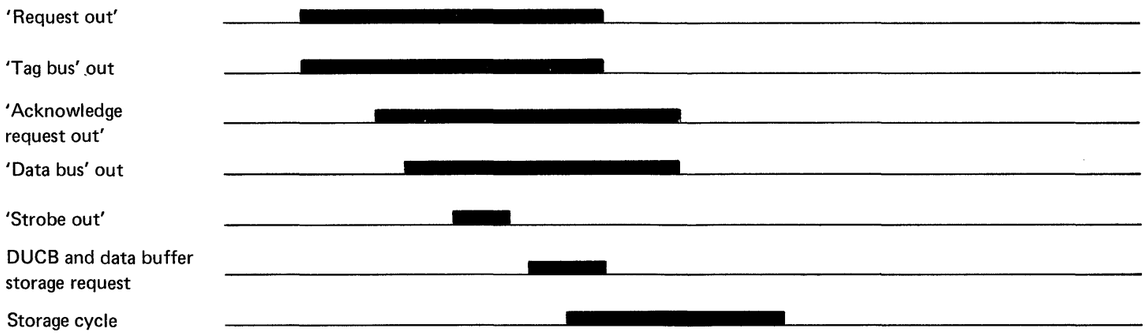
Start Disk Unit Controls

'Start disk unit controls' causes the disk unit controls to execute the command that is in the DUCB for the selected disk unit.

DUCB Transfer

The attachment begins a write operation by transferring the disk unit control block (DUCB) for the specified disk unit to the DUCB and data buffer storage, located in the disk unit controls. The information on the 'tag bus' indicates which DUCB word is to be transferred and to which disk unit DUCB field. The 'data bus' is activated with the actual DUCB word.

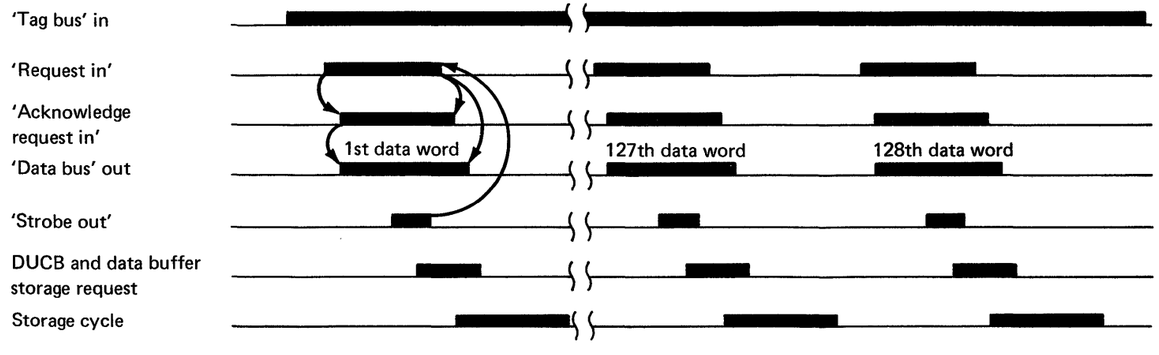
Write DUCB



This sequence is repeated until the required DUCB words are transfered.

Write Data Transfer

The data to be written on the disk is sent from the attachment to the data buffer field of the DUCB and data buffer storage. The data is sent one word at a time until 128 words (256 bytes) have been transferred. If the data record is less than 128 words, the attachment adds zeros to complete the record. The sequence is as follows:

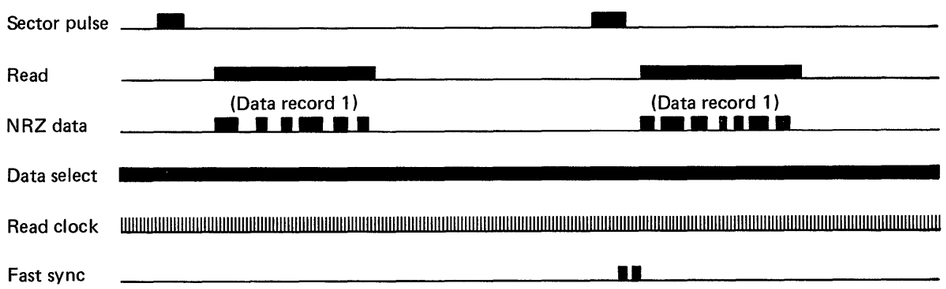


Read Data to the Disk Unit Controls

The disk unit controls causes the selected disk unit to read consecutive records and loads the data from these records into the data buffer for transmission to the attachment and the processor I/O channel.

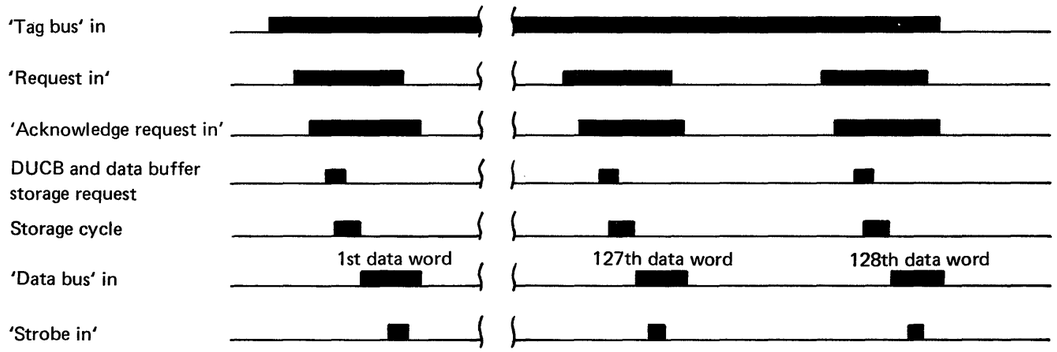
During a read data operation, the disk unit controls:

- Causes the disk unit to perform an automatic seek (unless automatic seek is inhibited).
- Analyzes the cylinder, head, and sector numbers and puts them in the ID compare area of the DUCB and data buffer storage.
- Checks the record count to determine the number of records to be read (the record count is zero to read one 256-byte record).
- Compares the ID numbers read with those already stored in the ID area of the DUCB and data buffer storage to ensure starting at the correct sector.
- Transmits the selected data to the DUCB and data buffer storage. If a complete record is in the buffer storage and the CRC is correct, the disk unit controls requests cycles to transmit the data to the processor I/O channel via the attachment.



Read Data Transfer

The data read from the disk unit is placed in a data buffer field in the DUCB and buffer storage. During multiple sector operation (either write or read data), one, two, or three of the data buffer fields may be used, depending on timing conditions of the data transfers. However, only one disk unit can use the data buffers during an operation. Data is sent to the attachment, one word at a time, until 128 words (256 bytes) have been transferred. The sequence for transferring data to the attachment is as follows:



The information on the 'data bus' first enters the attachment data register and it is sent to the processor I/O channel 'data bus' via the 'cycle-steal data bus' and the 'cycle-steal data register'.

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Tag Register

The information in the tag register specifies the direction and the type of information to be transferred over the data bus. The following illustration indicates the tag codes used to control information transfers between the attachment and the disk unit controls. Note that when the attachment initiates and controls the transfer, the 'tag bus' is *outbound*. 'Tag bus' bits 0–7 and P are gated into the tag register by an active 'request out' line. However, when the disk unit controls initiates the transfer, only 'tag bus' bits 0–3 and P are *inbound* to the attachment (gated by 'request in').

Tag bus in—disk unit controls controlled transfer

Tag bus bits	P	0	1	2	3	(bits 4–7 not used)
	P	1	0	D	D	Transfer data to attachment
	P	1	1	D	D	Transfer data from attachment
	P	0	0	D	D	Interrupt

Tag bus out—attachment controlled transfer

Tag bus bits	P	0	1	2	3	4	5	6	7		
	P	0	S	D	D	0	0	0	0	DUCB word 0	Fetch from or store into buffer storage for selected disk unit
	P	0	S	D	D	0	0	0	1	DUCB word 1	
	P	0	S	D	D	0	0	1	0	DUCB word 2	
	P	0	S	D	D	0	0	1	1	DUCB word 3	
	P	0	S	D	D	0	1	0	0	DUCB word 4	
	P	0	S	D	D	0	1	0	1	DUCB word 5	
	P	0	S	D	D	0	1	1	0	DUCB word 6	
	P	0	S	D	D	0	1	1	1	DUCB word 7	
	P	0	S	D	D	1	0	0	0	DUCB word 8	
	P	0	S	D	D	1	0	0	1	DUCB word 9	
	P	0	S	D	D	1	0	1	0	DUCB word 10	
	P	0	S	D	D	1	0	1	1	DUCB word 11	
	P	0	S	D	D	1	1	0	0	DUCB word 12	
	P	0	S	D	D	1	1	0	1	DUCB word 13	
	P	0	S	D	D	1	1	1	0	DUCB word 14	
	P	0	S	D	D	1	1	1	1	DUCB word 15	
	P	1	S	D	D	0	0	0	0	Reserved	
	P	1	S	D	D	0	0	0	1	Reserved	
	P	1	S	D	D	0	0	1	0	Reserved	
	P	1	S	D	D	0	0	1	1	Reserved	
	P	1	S	D	D	0	1	0	0	Reserved	
	P	1	S	D	D	0	1	0	1	Reserved	
	P	1	S	D	D	0	1	1	0	Reserved	
	P	1	S	D	D	0	1	1	1	Reserved	
	P	1	S	X	X	1	0	0	0	Load/sense diagnostic word 1	
	P	1	S	X	X	1	0	0	1	Load/sense diagnostic word 2	
	P	1	S	X	X	1	0	1	0	Reserved	
	P	1	S	X	X	1	0	1	1	Reserved	
	P	1	1	D	D	1	1	0	0	Start disk unit controls	
	P	1	1	D	D	1	1	0	1	Force end operation	
	P	1	1	D	D	1	1	1	0	Reset selected disk unit	
	P	1	1	0	0	1	1	1	1	Reset disk unit controls	

Legend

P = used to maintain odd parity

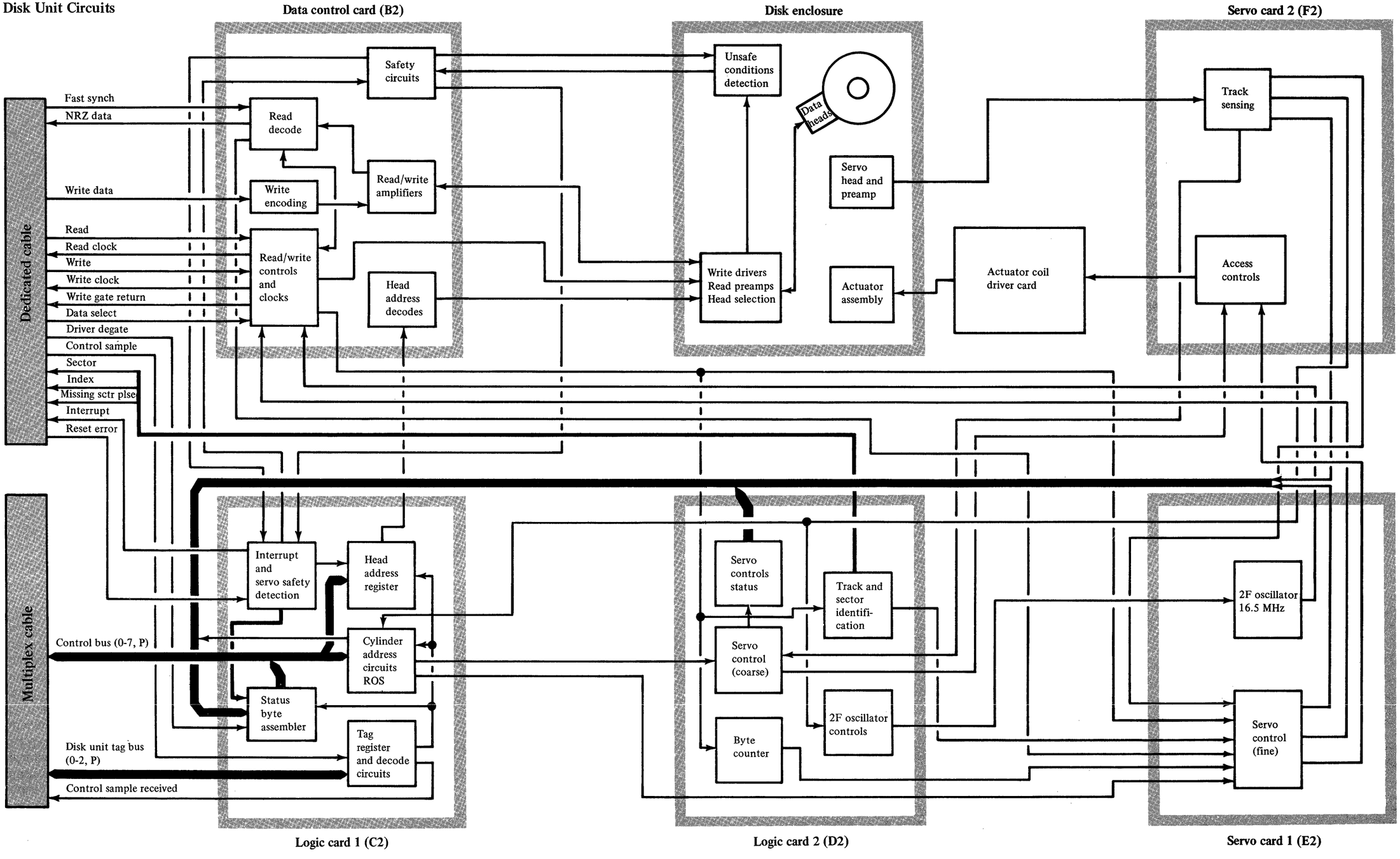
S = fetch or store
- 0 = fetch
- 1 = store

X = These bits are included in the parity count but have no significance

D = used to select a disk unit

bits 2	3	
0	0	selects disk unit 0
0	1	selects disk unit 1
1	0	selects disk unit 2
1	1	selects disk unit 3

Disk Unit Circuits



Disk Unit

The disk unit circuits include:

- Five circuit cards mounted on board A1
- An actuator coil driver card mounted on gate A1
- Circuits within the disk enclosure

The five circuit cards are the servo card 1, the servo card 2, the logic card 1, the logic card 2, and the data control card.

The circuits on the cards are grouped, by function, into the servo circuits, the access control circuits, and the data control circuits. The diagram on the facing page is for instructional purposes only and represents an overview of the disk unit circuits.

Data Control Circuits

The data control card contains the following:

- Data detection circuits
- Write encoding and read decoding circuits
- Head selection decode circuits
- Read/write controls and clocks
- Write safety detection circuits
- Read and write amplifiers

Data to be written on the disk is received from the disk unit controls in a serialized NRZ format. The data is encoded to a modified frequency modulation (MFM) format for recording on the disk.

During a read operation, data is decoded to a serial NRZ format and is time-standardized to the read clock.

Access Control Circuits

When the access control circuits receives a cylinder address from the disk unit controls, it calculates the required move length and the direction. The actuator is then accelerated at a maximum rate for approximately half of the seek. During the remainder of the seek, the actuator is decelerated according to a predetermined velocity profile. When the data heads are within 12% of the center of a track, the control of the actuator is given to the sector servo circuits for fine control of the data head position.

The control circuits interpret and execute a recalibrate operation.

During normal and diagnostic operations, the status information is continually updated. The disk unit controls can perform a sense operation when it requires status information.

Servo Circuits

During seek operations, information from the dedicated servo is used to control the current in the actuator coil. The signals from the dedicated servo surface are used to determine the position (cylinder) of the movable heads and to provide velocity information during a seek operation.

When the servo head arrives at the desired cylinder, the sector servo is used to position the data head over the center of the data track. The sector servo uses information from the dedicated servo and the sector servo (read by the data head at the beginning of each sector) to maintain the data head at the center of the data track.

Actuator Coil Driver Card

The actuator coil driver card is mounted on gate A1.

The card contains the driver transistors for the actuator coil in the disk enclosure.

Disk Enclosure Circuits

The disk enclosure contains the following internal circuits:

- Write drivers
- Data and dedicated servo head read pre-amplifiers
- Head selection circuits
- Unsafe-conditions detection circuits

Power On Sequencing

When the power-on switch, located on the front of the disk storage unit, is turned on, ac power is applied to the power supply and the cooling fans on gates A1 and A2. The 'power good' line, when activated by the power supply, indicates that all dc voltages are within tolerance and that the ac voltage is now applied to the drive motor. The 'power good' line is also used by the disk unit circuits to perform an initial reset and to cause the brake to be retracted from the spindle pulley.

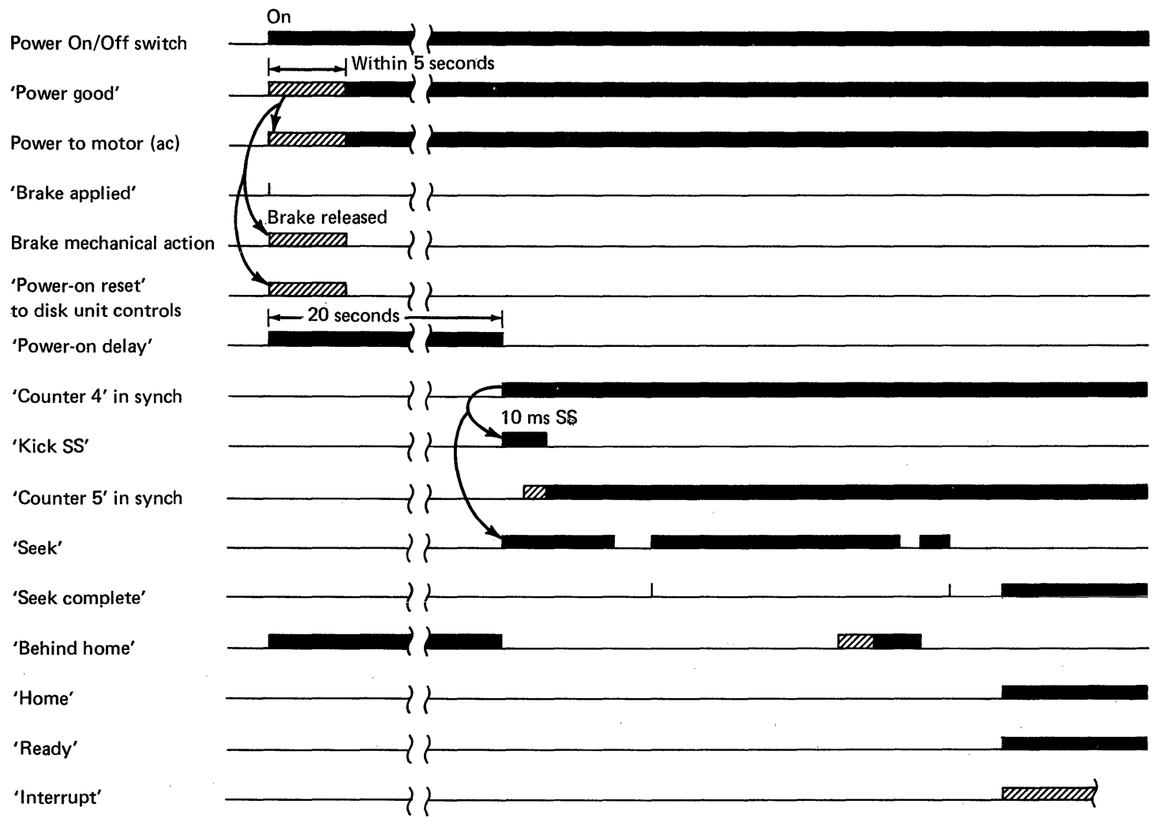
The 'power-on reset' line from the power supply in the primary unit to the disk unit controls is used to keep the circuits located in the disk unit controls, in a known, cleared, and error-free condition until the dc voltages are within tolerance. This line is not present in an expansion unit.

The 'power-on delay' line is held active for approximately 20 seconds from the time that power is turned on. During this time, the disks attain a stable operating speed of 3,125 rpm.

After the power-on delay, 'counter 4' of the counter synchronizes with the clock pulses written on the servo surface in the guard band and landing zone. When 'counter 4' synchronizes, indicating that the disks are up to speed, it activates the 'kick SS'. The 'kick SS' activates the 'seek' line, causing the actuator to accelerate for approximately 10 milliseconds and move the data heads into the data areas. 'Counter 5' synchronizes to the normal and alternate cells as the actuator moves. The counter is now in sync.

When the actuator assembly stops moving, 'seek complete' is activated to initiate a recalibrate cycle. At the completion of the recalibrate cycle, 'home' and 'ready' become active and the 'interrupt' line is activated. The data heads are now at the *home* position (cylinder 0) and the disk storage unit is ready to begin operations.

Power on sequencing



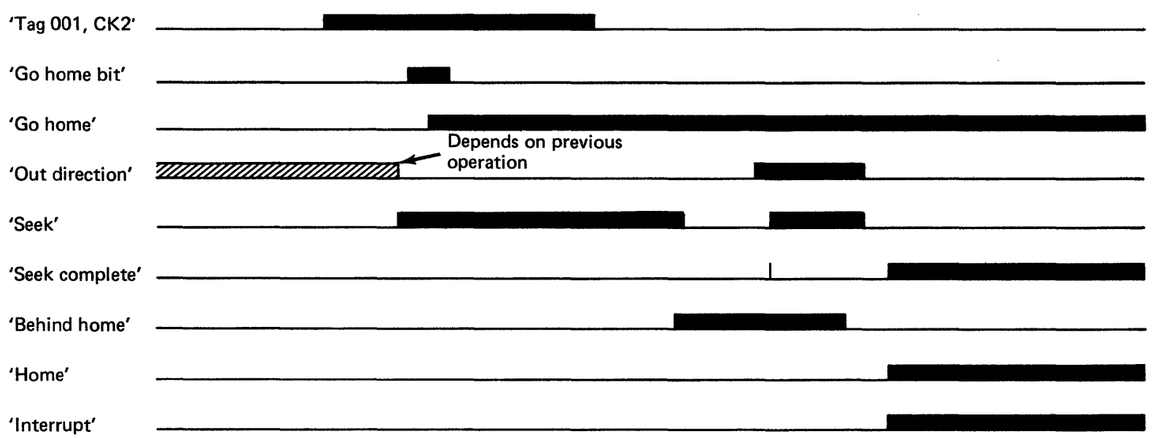
Recalibrate

A recalibrate operation moves the heads first into the guard band and landing zone area and then to cylinder 000 (home) with moveable-head 1 selected.

A recalibrate operation is initiated by the disk unit circuits during a power-on sequence and by the program during error recovery procedures.

The disk unit controls activates a tag code of 001 on the tag bus and activates control bus bit-0. The lines 'tag 001 clock 2' and 'go home bit' being active activate the line 'go home'. 'Out direction' is deactivated and 'seek' is activated. The actuator assembly then moves the data heads toward the *behind home* position (in the guard band and landing zone area). When the data heads arrive in the behind home position, the 'seek' line is deactivated and, approximately four milliseconds later, the 'seek complete' line is activated. When 'seek complete' and 'behind home' are active, the 'out direction' line is activated and another seek is initiated to move the data heads to the home position. Approximately four milliseconds later, 'seek complete' is again activated and, together with the 'home' line, activates the 'interrupt' line to the disk unit controls to signify the completion of the recalibrate operation.

During a power-on sequence, a recalibrate operation is initiated automatically by the disk unit circuits after the 'kick SS' moves the data heads into the data areas.



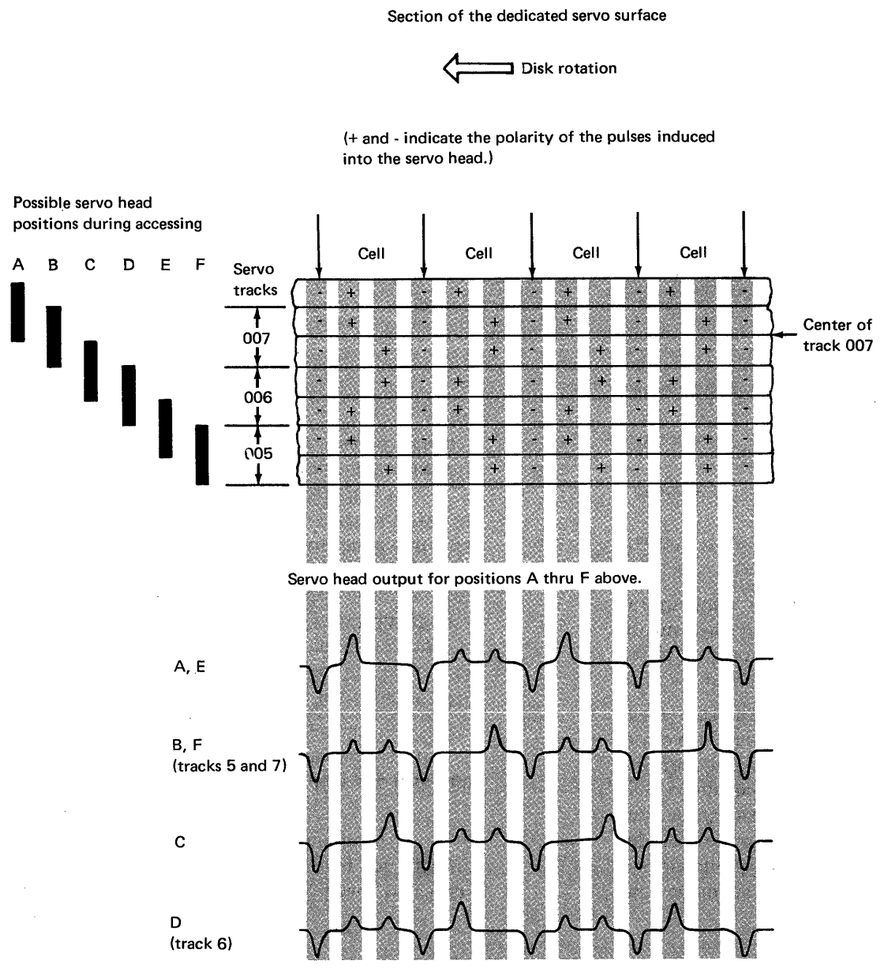
Servos

Initial actuator positioning is controlled by the dedicated servo. The information read from the dedicated servo surface is used to position the actuator at the required cylinder. The dedicated servo information is also used to detect index and sector pulses and to indicate when a track is crossed.

The sector servo is used to align the data head directly over the center of the data track after the dedicated servo system has positioned the access mechanism at the specified cylinder.

Dedicated Servo

The dedicated servo surface is written during the disk enclosure manufacturing process. The information on the servo surface is read by the servo head and is used by the disk unit circuits to position the movable heads over a selected data cylinder. The information is also used to develop clock pulses that synchronize the data transfers taking place within the disk subsystem. Special coding on the dedicated servo surface identifies the beginning of a track (index) or sector.



There are servo tracks on the servo surface; each track is comprised of servo cells. The beginning of a servo cell is defined by a negative pulse induced in the servo head. The beginning of one servo cell to the beginning of the next cell is equal in length to two data bytes on a data track. Each sector contains 300 servo cells.

The illustration below shows a small section of the servo surface and the pulses that are induced into the servo head in its possible positions.

The pattern for track 005 is repeated on all odd-numbered tracks; the pattern for track 006 is repeated on all even-numbered tracks. Also, note that alternate cells within each track are repeated.

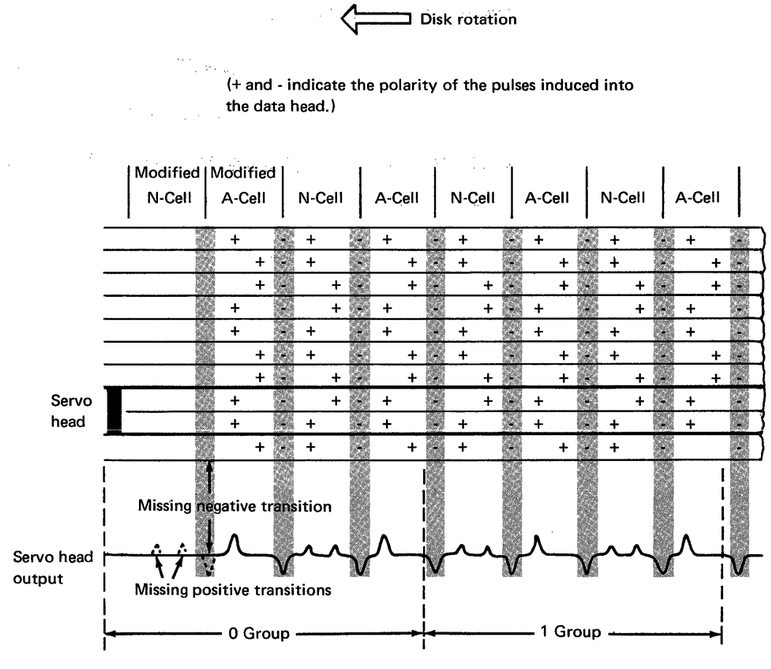
A cell is designated as either a *normal* cell or an *alternate* cell for the purpose of identifying cells within a track. Every other cell is called an alternate (A) cell; the cells located between the alternate cells are called normal (N) cells.

The first 24 cells at the beginning of each sector are modified to indicate either the beginning of a track (index) or the beginning of a sector. Clusters of four adjacent cells form a group, and each group is coded to represent either a 0 or a 1.

The index pulse at the beginning of a track consists of six groups of 4 cells coded 000010. The sector pulse in each succeeding sector is coded 001111. The servo circuits in the disk unit circuits is able to identify and synchronize to the N- and A-cells when these patterns are read. The first cell at the beginning of a sector is always an N cell.

The negative pulse that occurs at the start of each cell is used by the disk unit circuits to develop clock pulses. The clock pulses are generated from the information read by the servo head even when the access mechanism is moving at high speed across the surface of the disk.

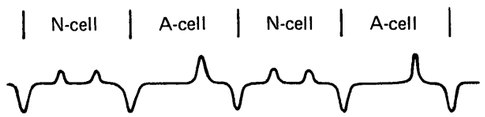
To code a 0, the pattern consists of a group of four cells in which the positive pulses have been omitted from the first normal cell and the negative pulse has been omitted from the beginning of the next alternate cell. A 1 is indicated if a group of four cells has not been modified.



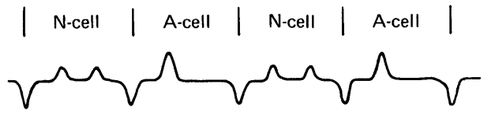
Track Counting

As the actuator assembly moves across the tracks, the signal from the servo head is constantly monitored by the track counting circuits. The first dedicated servo cell at the beginning of a sector is designated as a normal or N-cell; the next servo cell is designated as an alternate or A-cell. The N-cell, A-cell, N-cell pattern is repeated throughout the track.

The signal induced into the servo head for an odd-numbered track (001, 003, 005, etc.) when the servo is on track is:



The signal induced into the servo head for an even-numbered track (000, 002, 004, 006, etc.) when the servo is on track is:



An *on-track* condition occurs when one of the previous signal patterns is detected. An 'on-track' line updates the track count each time an even track or odd track is crossed during a seek.

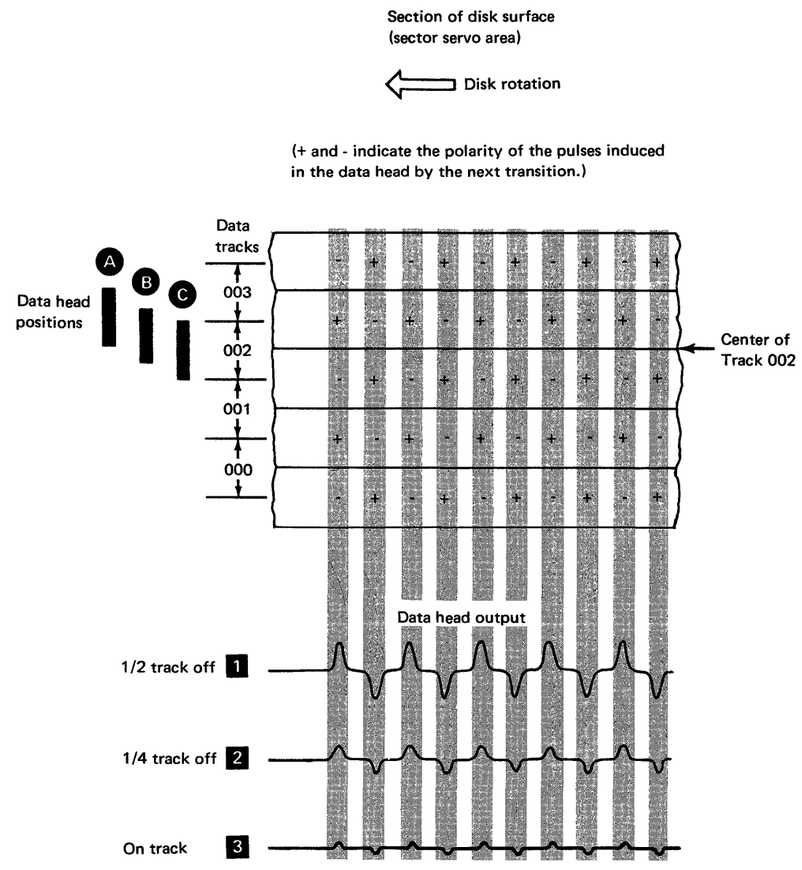
Sector Servo

Because data is densly packed on the data tracks of each disk surface, any minor misalignment between the data head and the data track can cause errors. The sector servo is used to accurately align the selected data head over the data track of each sector. The disk unit circuits uses the sector servo information read by the data head to position the data head on track after the dedicated servo positions the access mechanism at the selected cylinder. The sector servo information is 12.5 bytes long, and is included in a write-protected area of 22 bytes at the beginning of every sector, on each of the data surfaces.

The sector servo information is written (during manufacture) in synchronism with the dedicated servo pattern. Note that when the data head is on track, it is centered between two adjacent sector servo tracks. If the data head is located one-half track Ⓐ from the center of the data track, a maximum correction signal 1 is induced into the read head.

If the data head is located one-quarter of a track Ⓑ from the center of the data track, the head is still receiving strong signals from the upper magnetic pattern. However, the lower magnetic pattern is now inducing pulses of a smaller amplitude and of an opposite polarity. These signals combine to reduce the output signal 2.

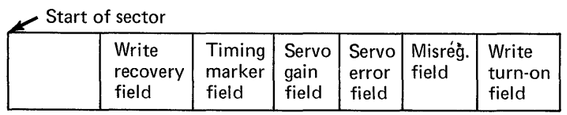
When the data head is on track Ⓒ, both signals effectively cancel each other. However, the output signal 3 does have a small signal induced due to minor surface irregularities and data head imperfections.



Track Following

Track following is accomplished by the disk unit circuits using the sector servo information. The sector servo area at the beginning of a sector for each track consists of the following fields:

- Write recovery field
- Timing marker field
- Servo gain field
- Servo error field
- Misregistration field
- Write turn-on field



Write Recovery Field

This field provides a stabilization time for the read circuits if the previous operation was a write operation.

Timing Marker Field

This field is used as a reference for the read circuits. It allows the circuits to synchronize to the information written in the sector servo area.

Servo Gain Field

This field consists of a series of magnetic transitions that induce a constant output in the data head. The servo gain field is used as a reference for the automatic gain control amplifiers.

Servo Error Field

This field induces a signal into the data head proportional to the distance that the head is off track. The signal is used by the servo circuits to position the data head precisely over the center of the data track.

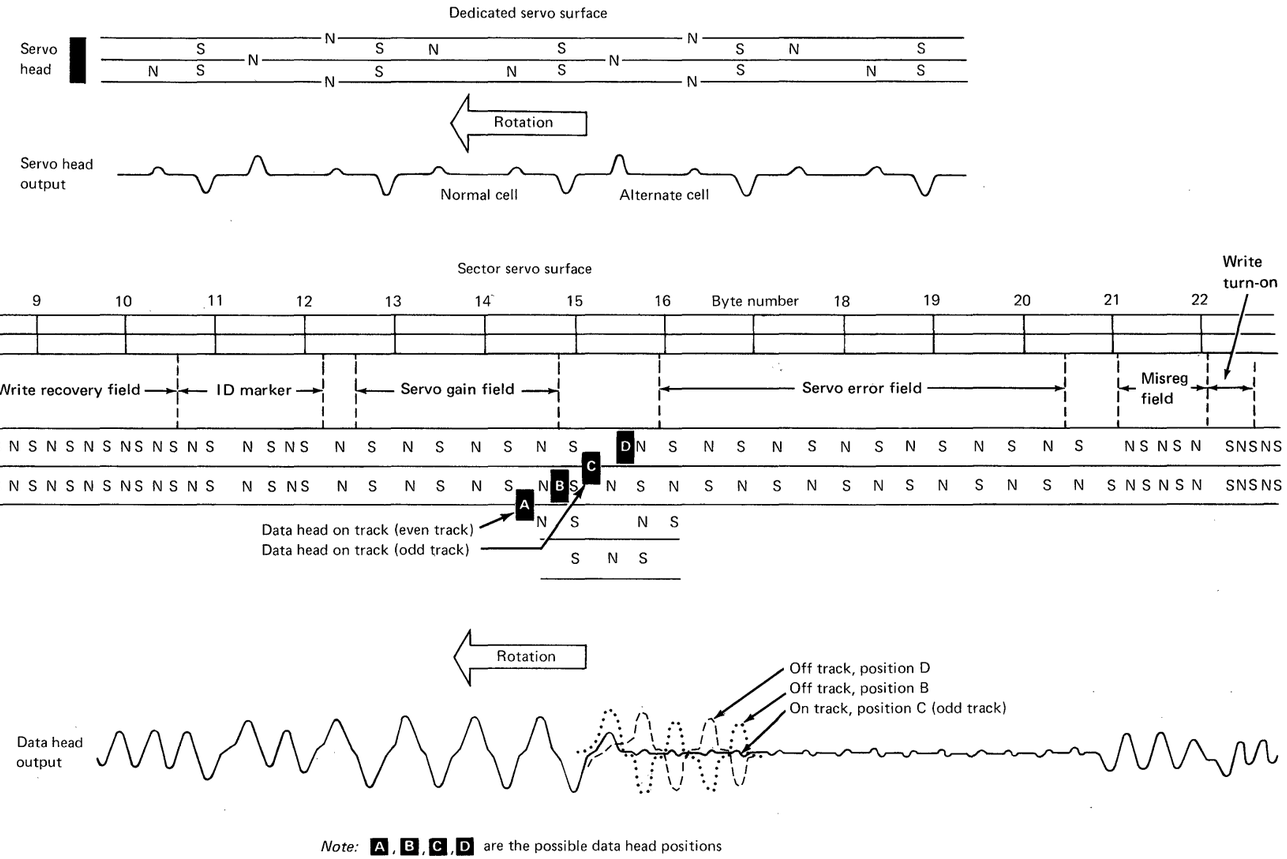
Misregistration Field

This field is used by the servo circuits to compensate for any misregistration between the dedicated servo head and the selected data head.

Write Turn-On Field

This field provides time for the circuits to switch from a read status to a write status when the following operation is a write operation.

The following illustration shows the physical relationship between the dedicated servo surface and the sector servo surface. The magnetic transitions (labeled N and S) on both surfaces and the expected outputs from both the servo and data heads are shown.

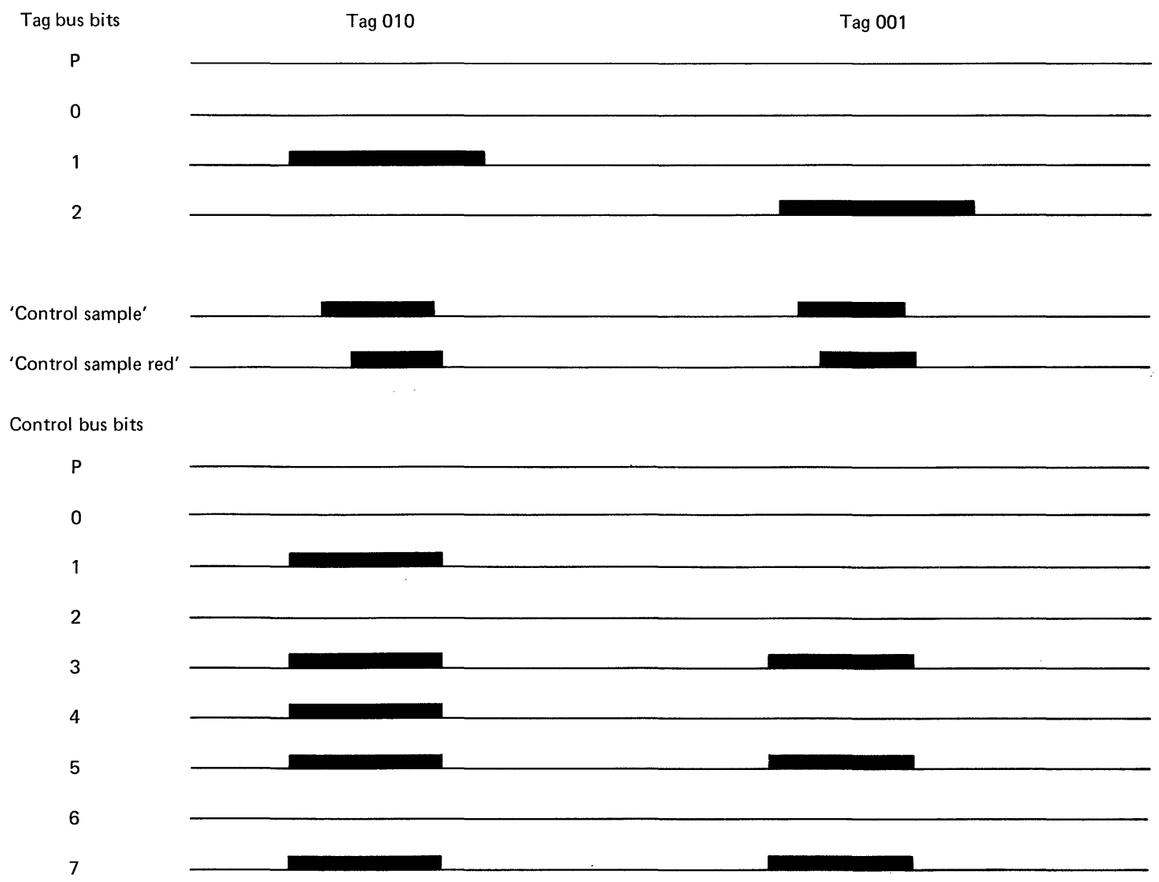


Note: A, B, C, D are the possible data head positions

Seek

A seek operation is initiated by control information received on the 'control bus'. The disk unit controls places the binary equivalent of the low-order eight bits of the desired cylinder address on the 'control bus' and encodes a tag of 010 on the 'tag bus'. The disk unit controls then activates the 'control sample' line, which permits the tag register in the disk unit circuits to accept and decode the 'tag bus'. After the 'tag bus' is decoded, it gates 'control bus' bits 0–7 to the cylinder address circuits, for cylinder address bits 128, 64, 32, 16, 8, 4, 2, and 1. At the same time that the disk unit circuits is gating the 'control bus' to the cylinder address circuits it is also gating the 'control sample received' line to the disk unit controls.

The disk unit controls then places the head address and the high-order bit (256) of the cylinder address on the 'control bus' and encodes a tag of 001 on the 'tag bus'. The disk unit controls then activates the 'control sample' line; the disk unit circuits decodes the 'tag bus', gates the 'control bus' to the cylinder and head address circuits, and activates 'control sample received'. Bits 1–5 of the 'control bus' select the data head; bit 7 is the high-order bit (256) of the desired cylinder address. Bits 0 and 6, in this instance, are not used. The following diagram shows a seek to cylinder 349 with data head 5 selected.



Direction and Distance

The cylinder address circuits determines if the seek is to be in or out. The 'out direction' line is activated, depending on the direction that the actuator is required to move.

The cylinder address circuits also determines the difference count (the number of cylinders that the actuator must move), based on the current cylinder address and the desired cylinder address. Each time the servo head passes through the center of a track, the 'on track' line is activated. This line being active causes the difference count to be decremented until the current cylinder address and the desired cylinder address are equal.

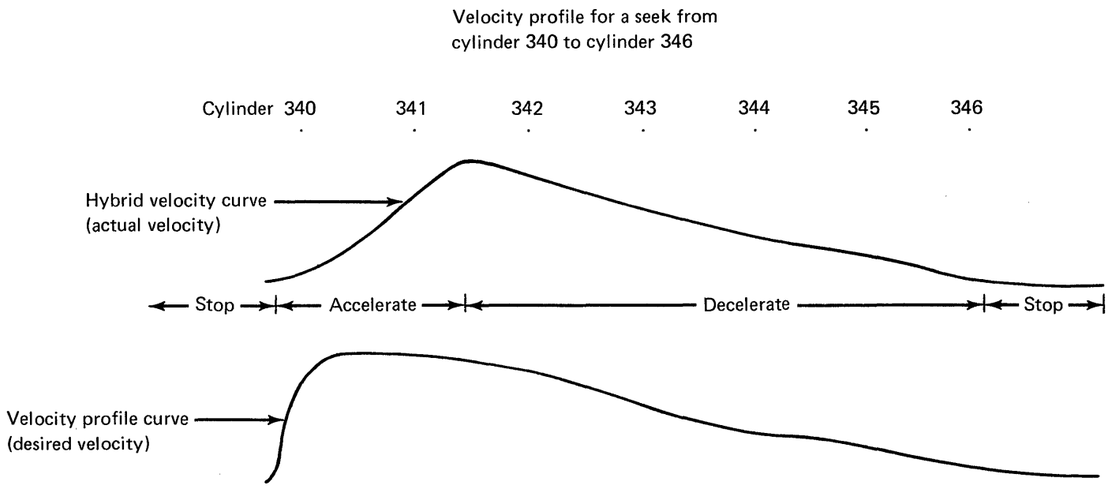
Control bus bits

	P	0	1	2	3	4	5	6	7
Tag 010	Odd parity bit	Cylinder address 128	Cylinder address 64	Cylinder address 32	Cylinder address 16	Cylinder address 8	Cylinder address 4	Cylinder address 2	Cylinder address 1
Tag 001	Odd parity bit	Not used	Fixed head select	Head select 8	Head select 4	Head select 2	Head select 1	Not used	Cylinder address 256

Velocity Profile

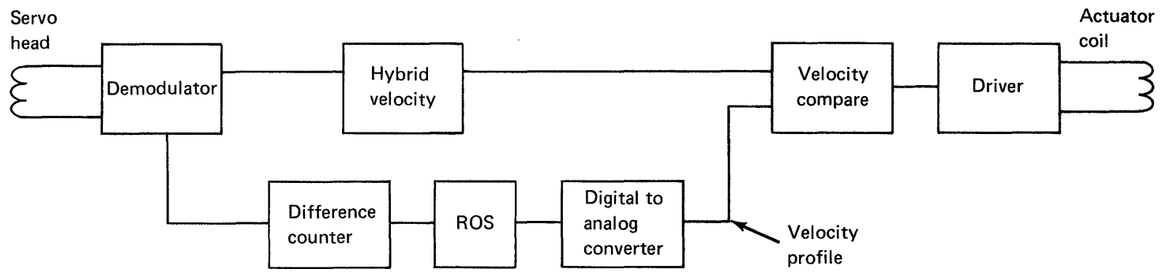
To obtain the fastest movement of the actuator during a seek operation, it is driven at the maximum speed for as long as possible; then it is decelerated to stop at the desired cylinder without an overshoot or an undershoot. The acceleration and deceleration of the actuator is controlled by the disk unit circuits to follow a predetermined velocity profile. The read only storage, on logic card 1, contains the velocity profile information.

During a seek operation, the disk unit circuits calculates the difference between the actual cylinder address and the desired cylinder address. This difference count is used to address the ROS at 1/4-cylinder intervals. Seeks of the same number of cylinders follow the same velocity profile.

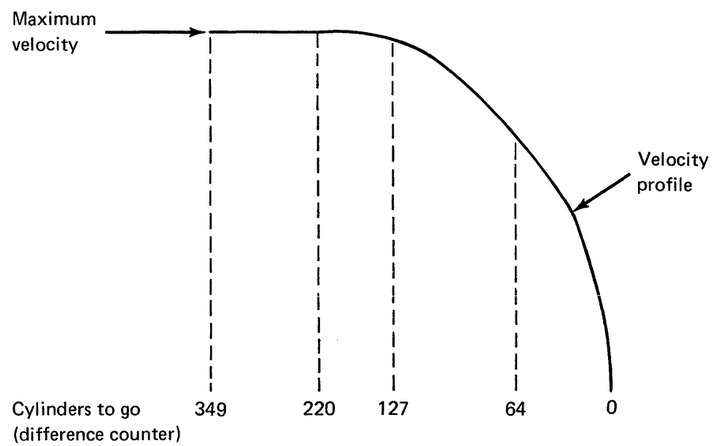


When the difference counter is greater than 128 cylinders (512 quarter cylinders), the ROS address is forced to 511; the actuator moves at its maximum speed until the difference counter equals 128.

The output of the ROS (a digital 8-bit signal) goes to a digital-to-analog converter, and an output is produced that corresponds to the desired velocity profile, as the difference count is decremented from 127 to 0.



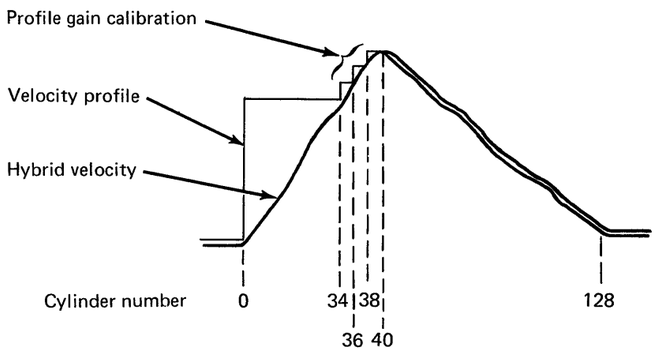
The hybrid (actual) velocity of the actuator and the velocity profile are compared during the acceleration and the deceleration. If the actuator is moving too fast or too slowly, the current in the actuator coil is decreased or increased, respectively, to keep the hybrid velocity equal to the velocity profile.



Profile Gain

The fastest accesses are obtained if the actuator accelerates for as long as possible and then decelerates as quickly as possible. To compensate for mechanical and electrical manufacturing tolerances and any drift that might occur due to environmental conditions, the velocity profile is variable and is controlled by the 'profile gain' voltage. By slightly varying the velocity profile, the optimum perforance of an individual actuator is achieved.

If, during a 128-cylinder seek, the actuator speed achieves the desired velocity before 40 cylinders have been crossed, the desired velocity (the output of the DAC) is increased. In this instance, the actuator assembly is capable of achieving a velocity that is faster than the velocity profile for a given distance. To take advantage of this particular actuator, the velocity profile is increased.



The profile gain counter, which increases the output of the DAC, is incremented by 1 every 2 cylinders when the hybrid velocity and the velocity profile first coincide. The incrementing, controlled by the 'vel>profile' line, is continued until 40 cylinders have been crossed. At this point, the incrementing stops and the profile gain is established until the power is turned off.

The profile gain voltage is set by performing the following operations:

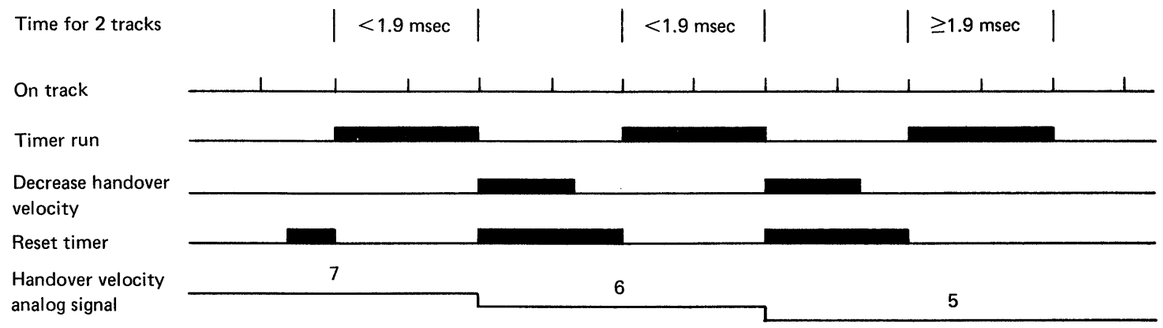
1. Recalibrate—this causes the actuator assembly to seek to the home position with movable head 1 selected.
2. Seek to cylinder 128 with movable head 1 selected—during this seek, the profile gain voltage is set.

Handover Velocity

Handover velocity controls the velocity profile in a manner that prevents the actuator from overshooting or undershooting the desired cylinder,during the last 1/4 cylinder of a seek.

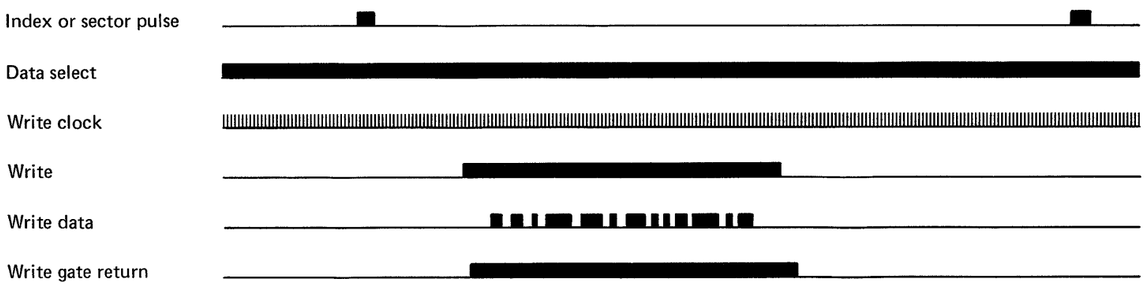
Handover velocity is calibrated during a recalibrate operation. The sequence is as follows:

1. The actuator assembly is forced to seek in two-track increments.
2. The handover velocity counter is set to its maximum value: seven.
3. The time taken to move the actuator assembly for two tracks is calculated.
4. If the time is less than 1.9 milliseconds, the counter is decremented by 1 and the actuator coil current is decreased.
5. The cycle is repeated until the seek time for two cylinders is equal to or greater than 1.9 milliseconds or until the handover velocity counter is decremented to zero.
6. The handover velocity signal is now set and is used to modify the output of the DAC for the last 1/4-track of a seek operation.



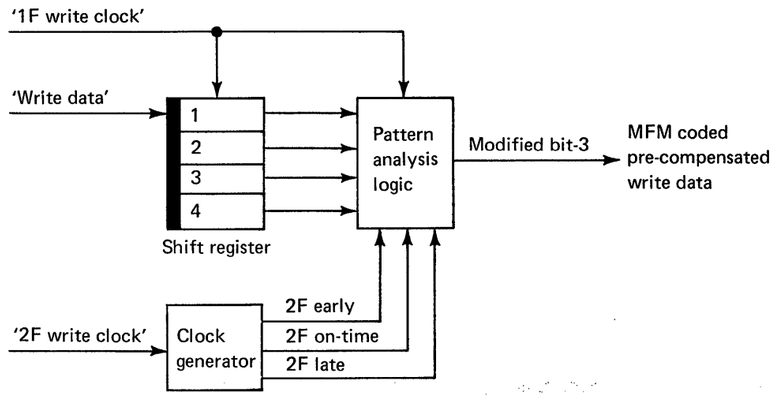
Write Data to Disk Unit

The following diagram illustrates the sequence of events for writing data in the disk unit.



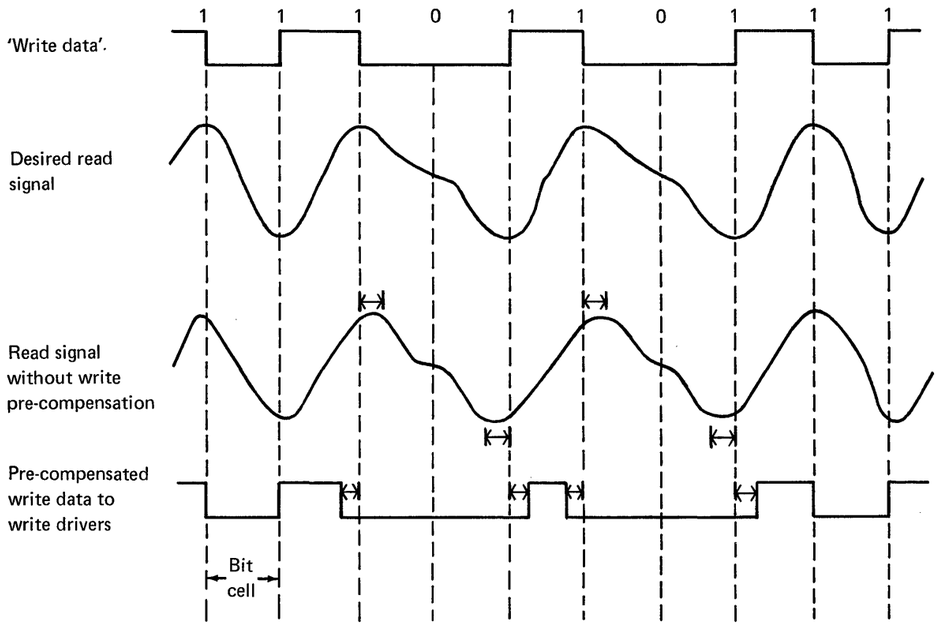
Write Data

'Write data' from the dedicated cable enters a four-bit shift register and is clocked through the shift register by the '1F write clock' pulse. The four bits of the shift register are fed to a 'pre-compensation' encoder, at which time the bit pattern is encoded to become a modfied frequency modulation (MFM) signal. The data is then amplified and sent to the write drivers for writing by the selected movable or fixed head.



Pre-compensation

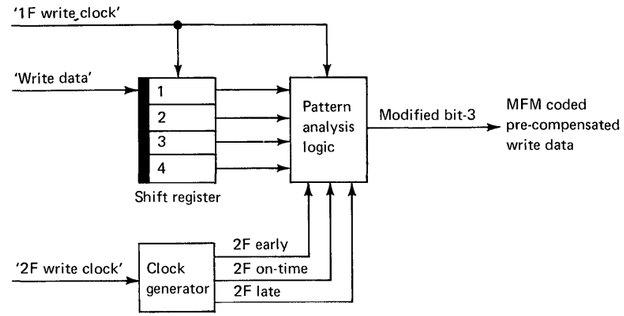
Pre-compensation is a technique that is used to counteract timing errors that occur in the read signal due to the high density of data recorded on the disk surface. The following illustration shows how a read signal would appear if it were not pre-compensated when written:

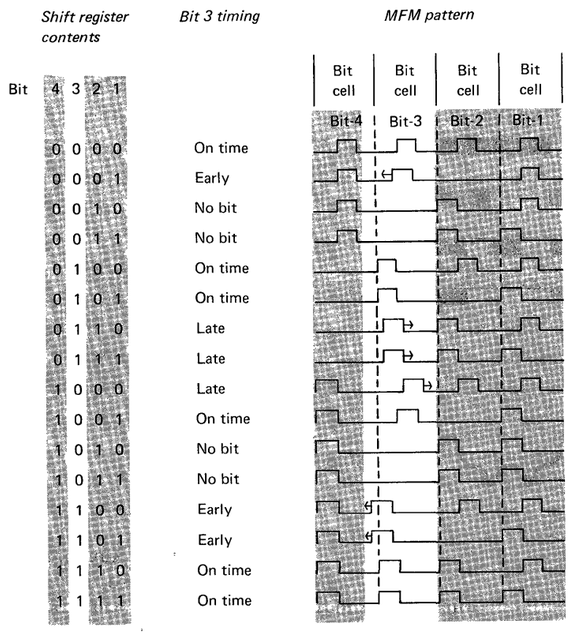


Data enters the 1-bit position of the shift register and is shifted through positions 2, 3, and 4. Bit 3 of the shift register is the bit being written, bit 4 is the bit that was previously written, and bits 1 and 2 are yet to be written.

The timing circuits develops three clocking lines at the 2F clock frequency that are used by the pattern analysis and encoder circuits to pre-compensate the data. The lines are '2F early', '2F on-time', and '2F late'.

The four bits in the shift register are analyzed and bit 3 is written on the disk on time, late, or early.

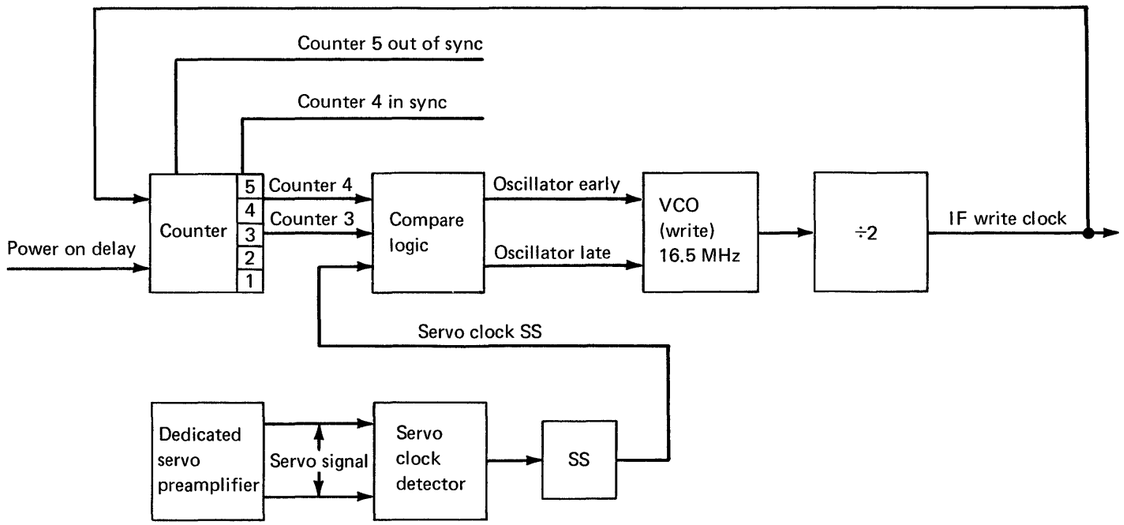




Phase Locked Oscillator (PLO)

The write PLO is used to keep the write clock in synchronization with the dedicated servo signal. The output of the write voltage-controlled oscillator (VCO), the '2F write clock' line, is divided by 2 to develop the '1F write clock' that is used to clock the write data onto the disk.

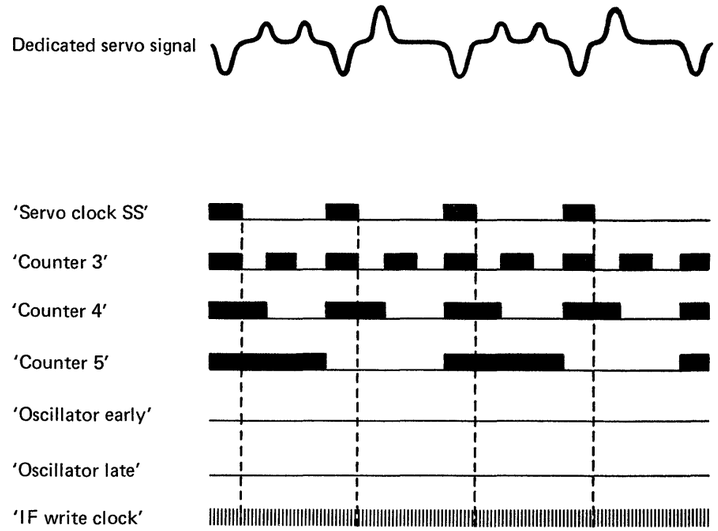
The '1F write clock' controls a 5-bit counter; 'counter 4' produces a complete square wave for every 16 oscillator pulses.



The PLO is in synchronization if the trailing edge of the dedicated 'servo clock' single-shot coincides with the midpoint of the active level of the 'counter 4' signal. A compare circuit looks for this coincidence and produces an output of 'oscillator early' or 'oscillator late' to the write VCO to correct any misalignment.

During normal operation, narrow oscillator late and early pulses are produced continuously, as shown in the illustration.

The '1F write clock' signal is used by the disk unit controls to serialize write data.



Read

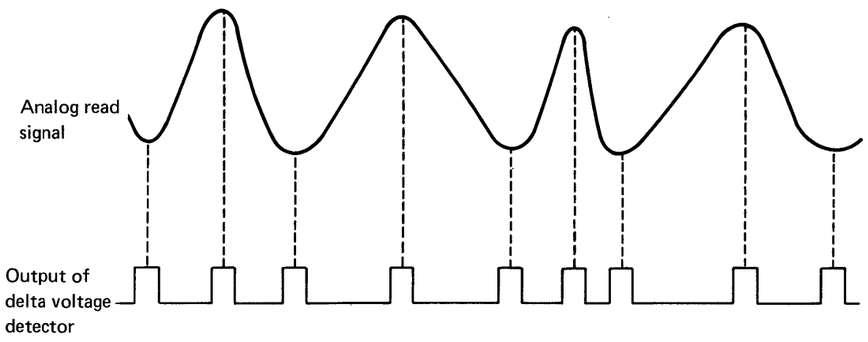
A read operation begins when the attachment sends a DUCB and a 'start disk unit controls' to the disk unit controls.

Read Data from the Disk

Any time that a head is selected and not writing, it is reading information from the disk. Read data is amplified within the disk enclosure and is sent to the read/write amplifiers over the 'actuator I/O' line. Two outputs are available from the amplifiers. The first output provides sector servo information to the servo circuits; the second output is amplified by a variable gain amplifier. The variable gain amplifier provides a differential output signal at a constant level, regardless of the variations of the input signal.

Delta Voltage Detector

The 'delta voltage detector', which is part of the data control card, produces an output pulse for each peak in the analog read signal. The output is sent to the voltage controlled oscillator (VCO) control circuits.



Voltage Controlled Oscillator

The read voltage controlled oscillator is used to time the read data going to the disk unit controls. It tracks the frequency and the average phase of the read signal and corrects for any signal drift.

The raw (untimed) data signal is sent to the 'data SS' and the 'data latch'. If the 'data SS' pulse ends before the 'data latch' has been reset by the '2F clock', the 'increase' line is activated to increase the VFO frequency. If the 'data SS' pulse ends after the 'data latch' has been reset, the 'decrease' line is activated.

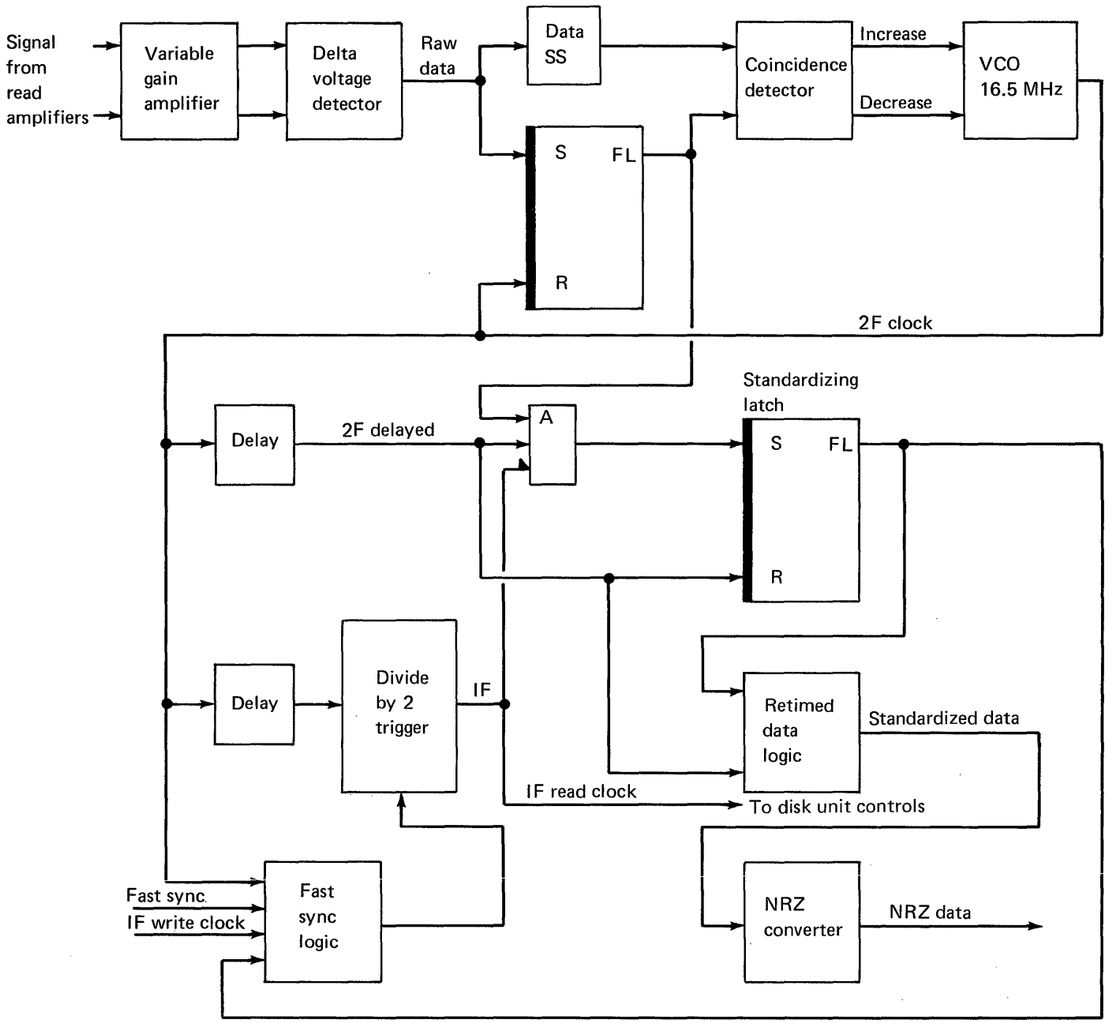
The 'increase' and 'decrease' lines are analog control voltages used by the VCO to maintain the coincidence of the 'data SS' and 'data latch' pulses.

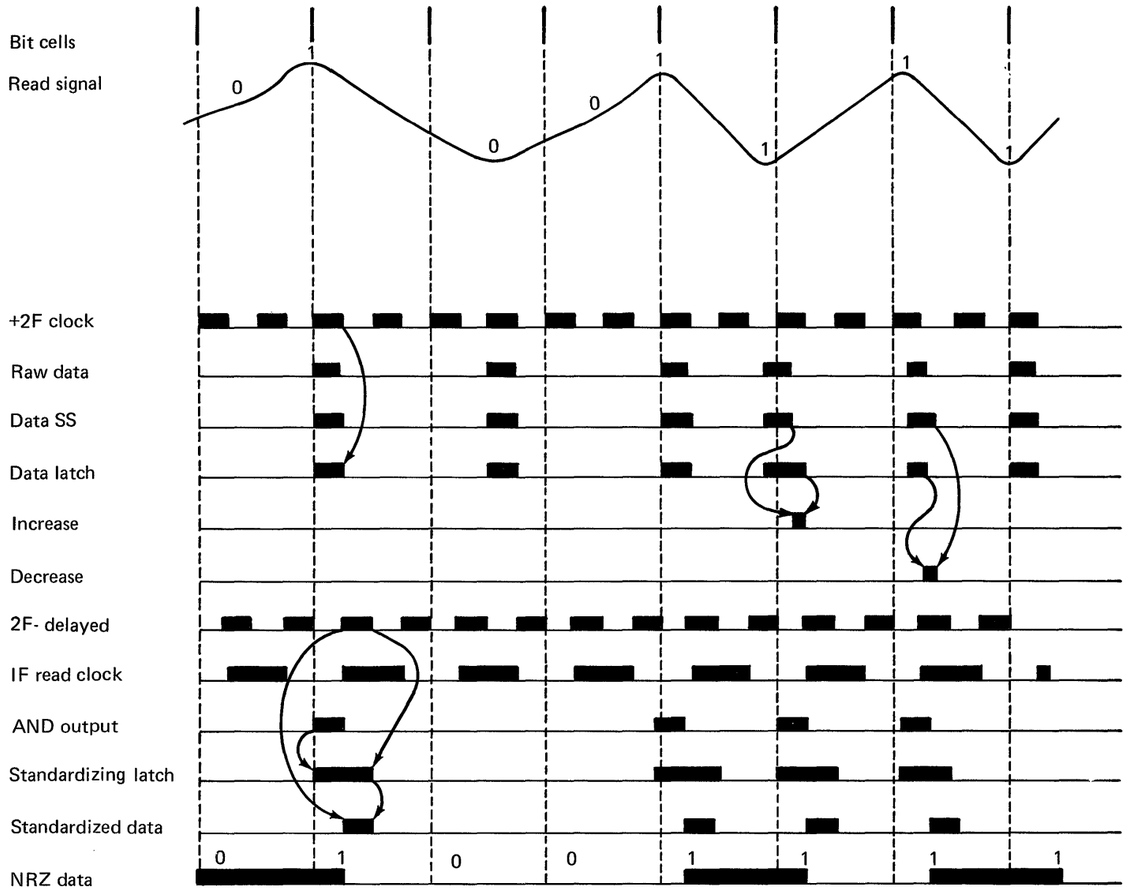
NRZ Data

Data sent to the disk unit controls is in an NRZ format. The AND circuit is used to eliminate 0-bits. The 'standardizing latch' and the 'retimed data logic' lengthen the detected 1-bits and retime the bits to the '1F read clock'. The 'NRZ converter' converts the standardized data to an NRZ format for use by the disk unit controls.

Fast Sync

When the source of the data signal changes (when changing from writing to reading), the VCO control circuits are momentarily switched to the 'fast sync' state. The 'fast sync' circuits forces the '1F read clock' line to correspond to the bit cells.





Error Detection and Safety Circuits

Attachment Error Detection

The attachment checks the parity of the following circuits:

- 'Attachment data bus' for information coming from the disk unit controls
- Output of the attachment data register for information going to the disk unit controls
- Information going to or coming from the processor I/O channel via the 'data bus'
- Information coming from the disk unit controls via the 'tag bus' (bits 0–3, P)

The attachment hardware will automatically retry the following operations if the suppress exception (SE) bit of the DUCB control word is set on:

- Read operation—retried a minimum of eight times
- Write operation—retried a minimum of four times
- Data unsafe—retried once

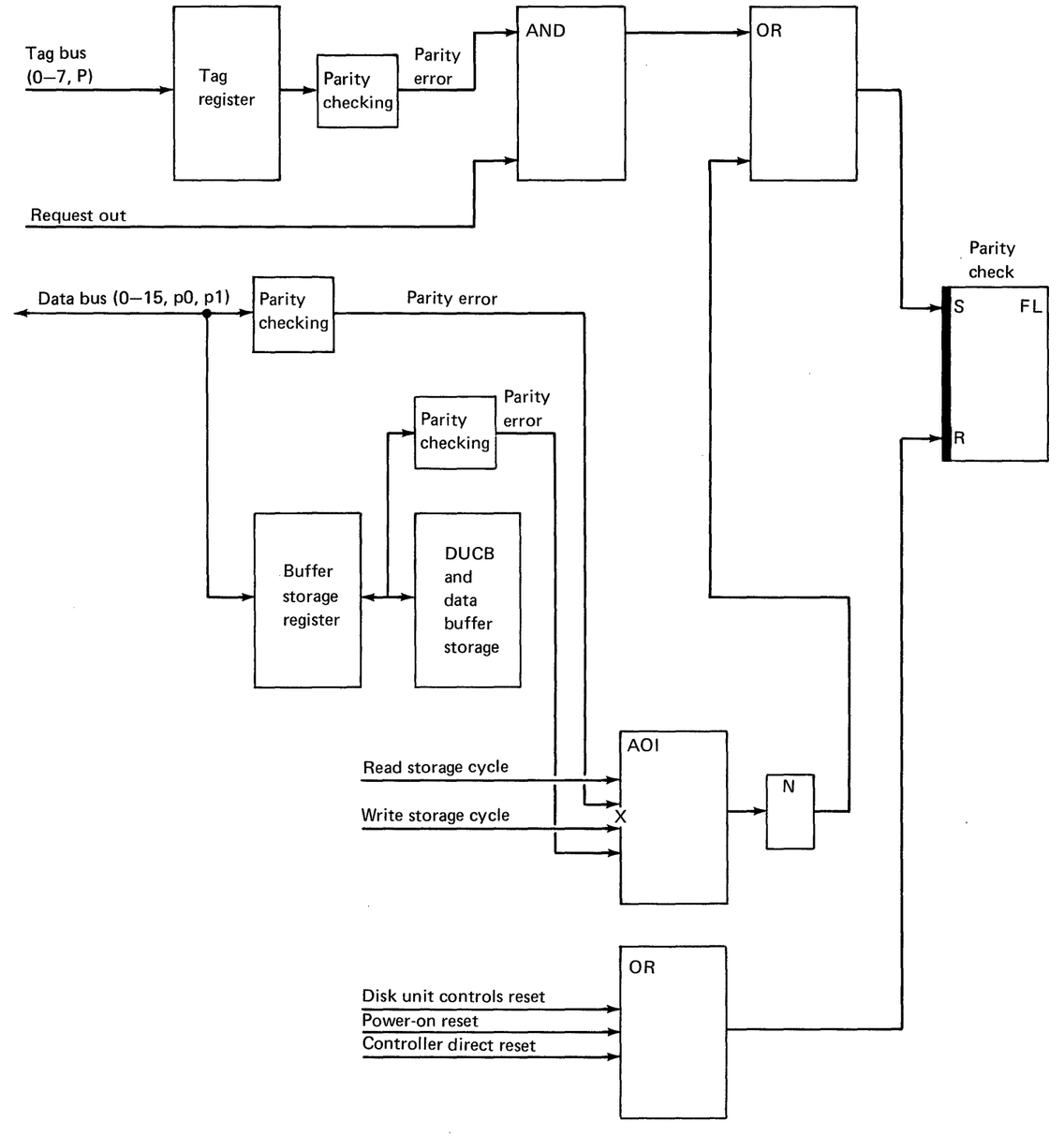
Disk Unit Controls Error Detection

Parity Error on 'Tag Bus' or 'Data Bus'

The 'parity error' line between the attachment and the disk unit controls indicates that a parity error has occurred on the 'tag bus', the 'data bus', or on both busses.

The 'parity error' has the indicated significance for the following operations:

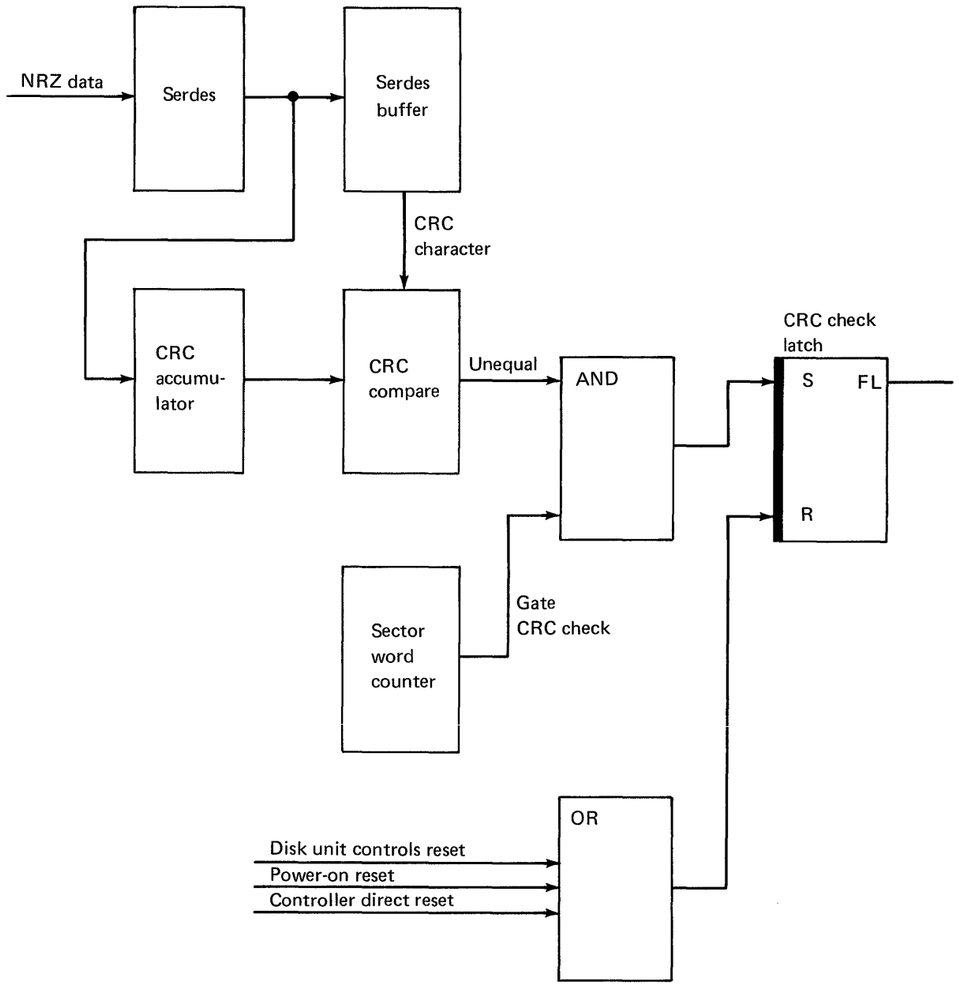
- Write data—the disk unit controls indicates that the parity error occurred on the 'data bus'
- Read DUCB—the disk unit controls indicates that the error is on the 'tag bus'
- Write DUCB—the disk unit controls indicates that the error is on either the 'tag bus' or the 'data bus'



CRC Error

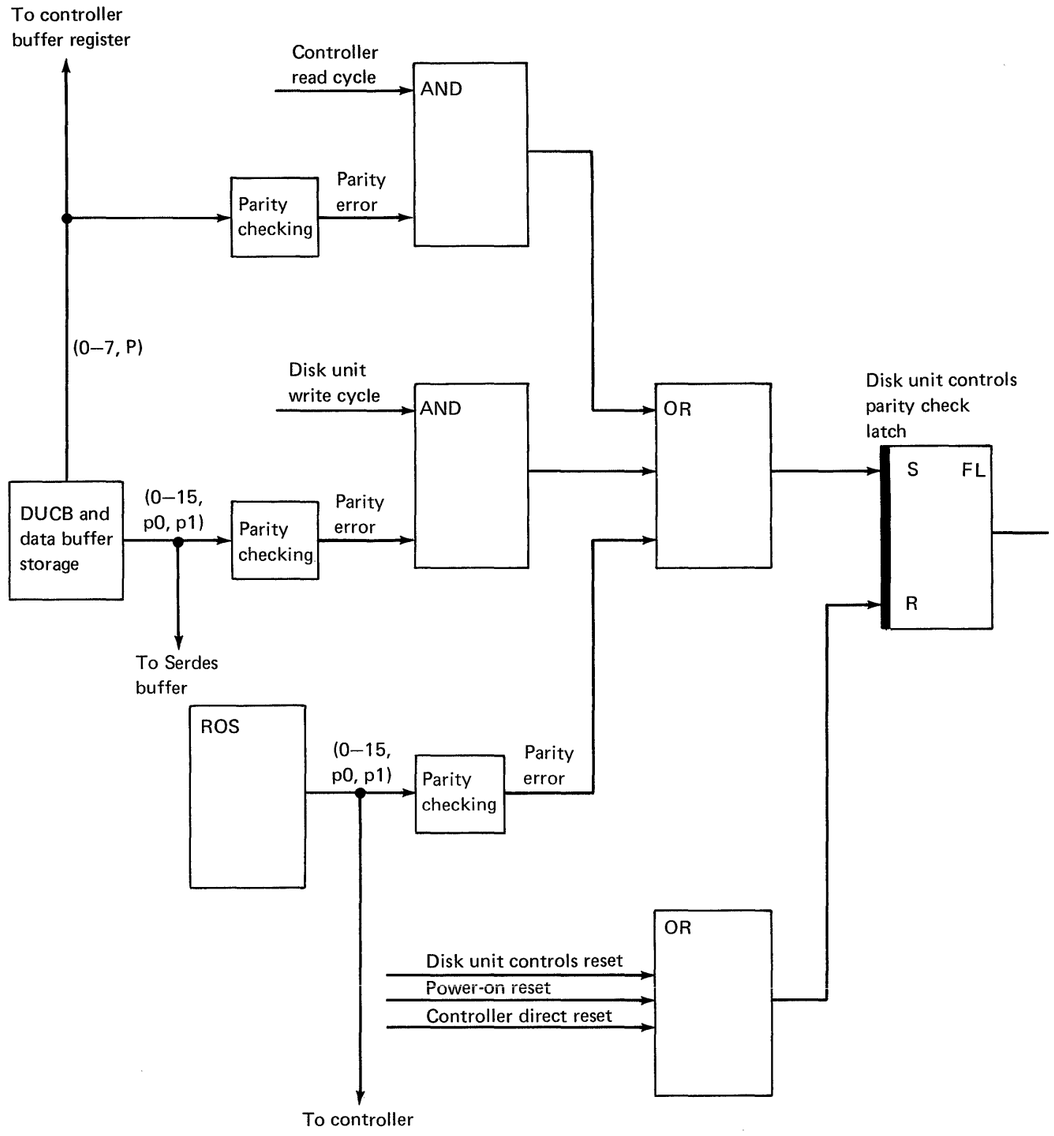
If, during a read operation, the disk unit controls detects an unequal comparison between the generated CRC character and the CRC character read from the disk, the CRC check latch is set.

If an error is detected while the disk unit is searching for a specific ID, the error is not reported to the attachment. However, if the error occurs while reading the ID that the disk unit has been searching for, the disk unit controls sends a 'no record found' error to the attachment. The disk unit controls retries the operation up to eight times.



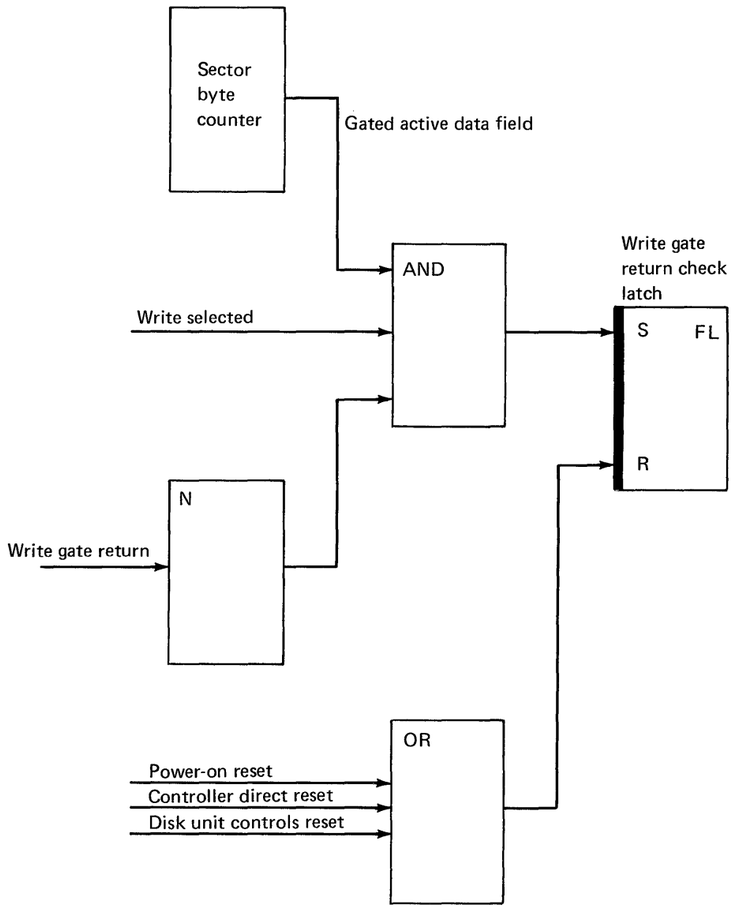
Disk Unit Controls Parity Check

This error condition indicates that the disk unit controls detected an internal parity check.



Write Gate Return Check

This error indicates that the 'write' and 'data select' lines to the selected disk unit are active, but the 'write gate return' line is inactive (indicating that the write current has not been turned on). This error condition can be retried up to four times by the disk unit controls.



Missing Sector Pulse

This error is set if the 'missing sector pulse' line is active during a Read ID, Write ID, or a Read diagnostic command. If the error occurs at the selected sector, the disk unit controls indicates a 'no record found condition' to the attachment. This error can be retried up to eight times before a hard error condition is posted.

Disk Unit Error

This error is indicated if the disk unit controls detects either a parity error on the 'control bus' from the disk unit or if a disk unit cable continuity check occurs.

The signal cabling between the disk unit controls and the disk units is checked by the circuits in the disk unit controls to ensure that the cables are seated and plugged properly.

Write Safety Detection

The write safety detection circuits check the operations of the disk unit for conditions that could adversely affect the data written on the disks or the data being written.

No Transitions

When the data head current is reversed during normal write operations, voltage spikes are produced in the data head winding. If these spikes are missing (indicating no transitions), either the data head or the write driver has failed.

Head Grounded

When a head-to-ground short causes the current in the center-tapped line to exceed the threshold set in the current threshold sense circuit, a 'head-grounded' error is indicated.

Multi-Chip Selection

If the current in the positive supply to the disk unit exceeds the threshold set in the current threshold sense circuit, a 'multi-chip selection' error is indicated. This error indicates that more than one head has been selected.

Servo Unsafe

If unsafe conditions in the servo circuits are detected, this error is indicated.

Write Current When Not Writing

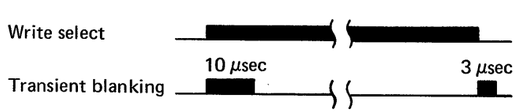
This error is indicated if write current is detected when 'write' is inactive.

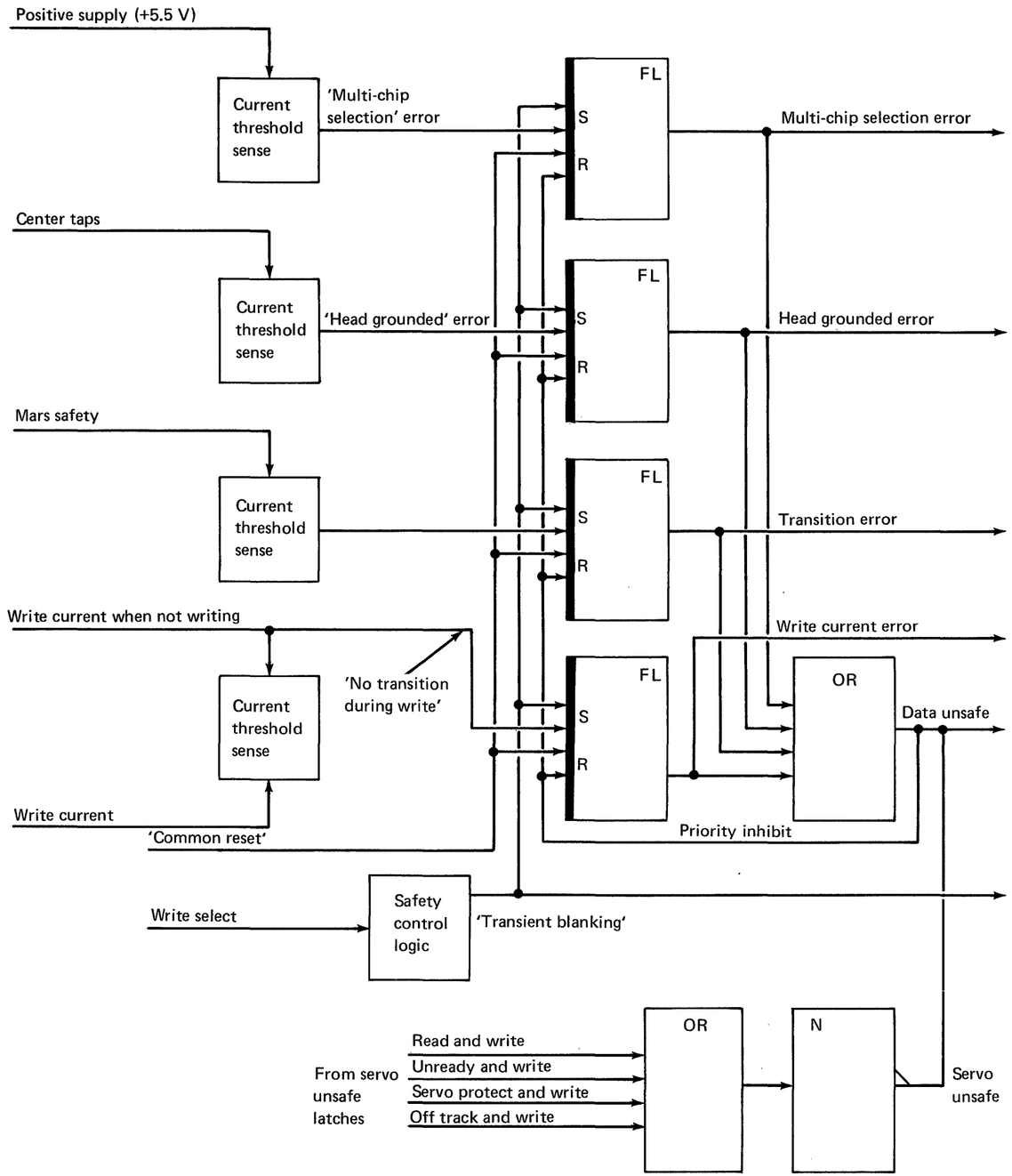
Priority Inhibit

This line, when active, prevents any subsequent errors from setting the safety detection latches; only the first error condition sets the latches.

Transient Blanking

Transient pulses at the beginning or end of a write operation that would incorrectly set the safety detection latches are inhibited by the 'transient blanking' line.

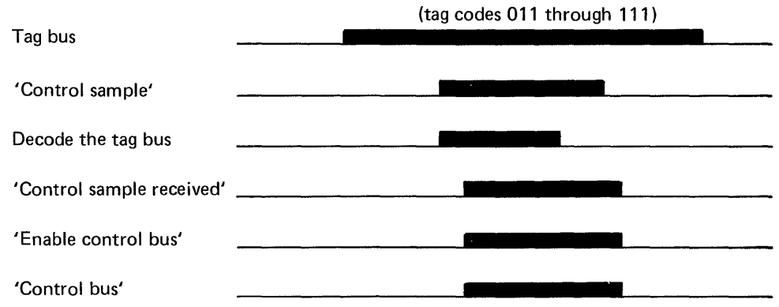




Sense/Status Cycle

A sense or status cycle is initiated when the disk unit controls encodes a sense or status tag code (codes 011 through 111) on the 'tag bus' and activates 'control sample'. The cycle is initiated in response to an interrupt or as a part of normal operations.

The disk unit decodes the 'tag bus' and activates 'control sample received'. 'Control sample' or 'control sample received' is ANDed with 'not tag codes 000, 001, or 010 to activate the internal 'enable bus' line. The 'enable bus' line gates the information in the 'status byte assembler' onto the 'control bus'.

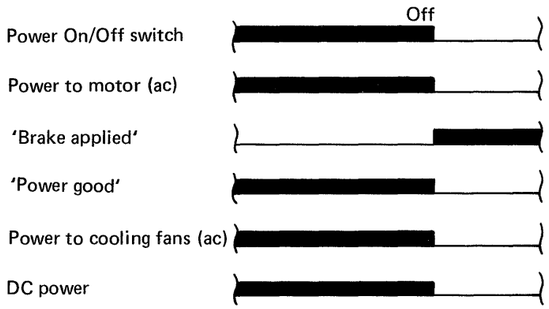


Power Off and Power Interlocks

Power Off

When power is turned off on the disk unit, the following sequence occurs:

- The 'power good' line becomes inactive.
- The ac power to the motor drops and the brake is applied; the actuator is retracted by the retract spring.
- The dc power to the circuits drops.
- The ac power to the cooling fans drops.



Power Interlocks

The 'power good' line becomes inactive if any of the following conditions exist:

- Loss of disk speed
- A motor thermal trips
- A gate thermal switch opens
- The motor switch on the power supply is turned off
- DC voltages are out of tolerance
- A motor brake failure

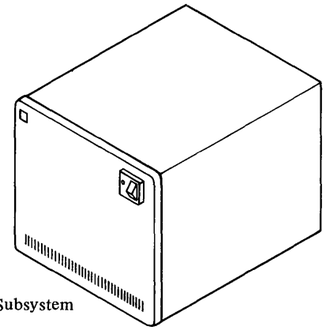
The 'brake applied' signal line, from the disk unit circuits to the power supply, indicates that the disk speed has decreased due to a brake or a drive belt failure. Ac and dc power to the drive motor and the disk unit circuits is removed within five seconds of the line becoming active.

When one of the above conditions exists, the ac power to the motor is removed within five seconds, and the disk unit powers off per the power-off sequence.

The ac power to the motor must always drop before the dc power. Also, the ac power to the gate-cooling fans must be on if the dc power is supplied to the circuits cards.

The 'brake applied' signal line, from the disk unit circuits to the power supply, indicates that the disk speed has decreased due to a brake or a drive belt failure. Ac and dc power to the drive motor and the disk unit circuits is removed within five seconds of the line becoming active.

Chapter 4.
Operations



Operate I/O Instruction Summary

All commands are initiated by an operate I/O instruction which points to an IDCB containing the command.

0	4	5	7	8	10	11	12	15	16	31
0 1 1 0 1				R2			1 1 0 0		IDCB address	

IDCB / Commands	Command field 0–7	Device address field 8–15	Immediate data field 16–31	Condition code
Prepare This command loads the interrupt level and I-bit into the disk unit.	0 1 1 0 0 0 0 0	X X X X X X X X	Zeros (16–30) | Level | I (31) Interrupt disabled = 0 Enable interrupt = 1	0, 5, 7
Read ID This command transfers the identification (ID) word to the immediate data field of the IDCB.	0 0 1 0 0 0 0 0	X X X X X X X X	Zeros	0, 5, 7
Device Reset This command resets any pending interrupt requests or busy condition in the disk unit.	0 1 1 0 1 1 1 1	X X X X X X X X	Zeros	0, 7
Halt I/O This is a channel-directed command that halts all I/O activity on the I/O channel and resets all devices.	1 1 1 1 0 0 0 0	X X X X X X X X		not reported
Load Sense Diagnostic Word 1 This command moves data from the IDCB to the disk unit control's data buffer register.	0 1 0 0 1 0 0 0	X X X X X X X X	Data word	0, 5, 7
Load Sense Diagnostic Word 2 This command allows the disk unit controls and the disk attachment to operate in single-cycle mode for diagnostic purposes.	0 1 0 0 1 0 0 1	X X X X X X X X	Data word	0, 5, 7
Attachment Storage Diagnostic This command instructs the attachment to execute a storage diagnostic test.	0 1 0 0 1 1 1 0	X X X X X X X X	Data word	0, 5, 7
Load Disk Unit Control Block 0 This command moves the first word of the disk unit control block into the immediate data field.	0 1 0 0 0 0 0 0	X X X X X X X X	Data word	0, 5, 7
Attachment General Diagnostic Test This command causes the attachment to test its data registers and control latches.	0 1 0 0 0 0 0 1	X X X X X X X X	Data word	0, 5, 7
Load Seek Required Address Direct This is a special diagnostic command and must be issued sequentially prior to the Load Seek Control Direct command.	0 1 0 1 0 0 1 0	X X X X X X X X	Data word	0, 5, 7
Load Seek Control Direct These commands are special diagnostic commands for the disk unit controls. They perform special diagnostic wrap functions and must be issued in this sequence. Load Seek Required Address Direct command followed by a Load Seek Control Direct command.	0 1 0 1 0 0 1 1	X X X X X X X X	Data word	0, 5, 7

Start Command

DCB (device control block)

Word	0	4	5	7	8	15
0	Control word					
	X 0 X 0 X		*Addr key*		Modifier bits	
1	Byte 0				Byte 1	
	Flag				Sector or record no.	
2	0	Bits 1–5	6	Bits 7–15		
	0	Head	0	Cylinder		
3	Byte 0				Byte 1	
	Reserved				Scan/repeat count	
4	Residual status block address					
5	DCB chain address					
6	Byte count					
7	Starting data address					

Start command DCB word 0 modifiers

Operations	Bit 2	Bits 8–15
Seek	0	0000 0000
Recalibrate	0	0000 0001
Calibrate	0	0000 1001
Overlapped seek	0	0000 1000
Timed seek diagnostic	0	0000 1011
Read data	1	0001 X000
Read verify	0	0001 X001
Read data repeat	1	0001 X010
Read disk unit data buffer diagnostic	1	0001 0011
Read sector ID	1	0001 X100
Read sector ID extended	1	0001 X101
Read diagnostic record 1	1	0001 X110
Read diagnostic record 2	1	0001 X111
Write data	0	0010 X000
Write data with read verify	0	0010 X001
Write data repeat	0	0010 X010
Write data repeat with read verify	0	0010 X011
Write sector ID with read verify	0	0010 1101
Write sector ID extended with read verify	0	0010 1111
Write data security with read verify	0	1010 X001
Scan equal	1	0011 X000
Scan low/equal	1	0011 X001
Scan high/equal	1	0011 X010

Start Cycle Steal Status Command

DCB (device control block)

Word	0	4	5	7	8	15
0	Control word					
	0 0 1 0 0		*Addr key*		0 0 0 0 0 0 0 0	
1	Not used (zeros)					
2	Not used (zeros)					
3	Not used (zeros)					
4	Not used (zeros)					
5	Not used (zeros)					
6	Byte count					
	0 0 0 1 1 0 1 0					
7	Data address					

Operate I/O Instruction Summary (continued)

All commands are initiated by an operate I/O instruction which points to an IDCB containing the command.

0 4 5 7	*8 10 11 12 15*	*16 31*
0 1 1 0 1	*R2*	*1 1 0 0*	*IDCB address*

IDCB / Commands	*Command field* *0 7*	*Device address field* *8 15*	*Immediate data field* *16 31*	*Condition code*
Sense Disk Unit Direct This command causes the disk unit controls to read the sense byte from the selected disk unit.	0 1 0 1 0 1 0 0	X X X X X X X X	Data word	0, 5, 7
Sense Disk Unit Diagnostic Bytes 1, 2, and 3 This command causes the disk unit controls to read three sense bytes from the selected disk unit.	0 1 0 1 0 1 0 1	X X X X X X X X	Data word	0, 5, 7
Multisample Pulse Test This command executes the multisample pulse test to the selected disk unit to determine if any of the lines are active.	0 1 0 1 0 1 1 0	X X X X X X X X	Data word	0, 5, 7
Sense Disk Unit Diagnostic Wrap This command causes the disk unit control to read the low-order byte of the cylinder number.	0 1 0 1 0 1 1 1	X X X X X X X X	Data word	0, 5, 7
Disk Speed Timing Diagnostic This command times the disk for 20 revolutions and returns the loop count in diagnostic sense bytes 1 and 2.	0 1 0 1 1 0 1 0	X X X X X X X X	Data word	0, 5, 7
Disk Unit Control Diagnostic This command allows access to the disk unit controls to operate in an interleaved or noninterleaved mode.	0 1 0 1 1 1 0 1	X X X X X X X X	Data word	0, 5, 7
Diagnostic Reset Disk Unit Controls This command resets the disk unit controls.	0 1 0 0 1 1 1 1	X X X X X X X X	Data word	0, 5, 7
Force End Operation This command sets the end operation trigger equal to 1, and causes the disk unit to post status, terminate any disk operations in progress at the next end store time, terminate the data transfer to the processor, and interrupt the processor with end operation and any other interrupt conditions on.	0 1 0 0 1 1 0 1	X X X X X X X X	Data word	0, 5, 7
Start The Start command initiates I/O disk operations that transfer data to or from processor storage in cycle-steal mode.	0 1 1 1 0 0 0 0	X X X X X X X X	DCB address	0,1,2,3 5,6,7
Start Cycle Steal Status The Start Cycle Steal Status command causes 13 words of status information to be transferred, in cycle-steal mode, from the 4963 to processor storage.	0 1 1 1 1 1 1 1	X X X X X X X X	DCB address	0,1,2,3, 5,6,7
Start Cycle Steal Diagnostic The Start Cycle Steal Diagnostic command initiates diagnostic disk operations.	0 1 1 1 1 1 0 1	X X X X X X X X	DCB address	0,1,2,3, 5,6,7

Issue a Cycle-Steal Status Command

Cycle-Steal Status Word 2

Bit	Meaning
0-3	CRC check
4-7	Write echo check
8-11	Missing sector pulse
12	Data unsafe
13	Disk unit not ready
14-15	Not used

Cycle-Steal Status Word 3

Bit	Meaning
0-3	No record found
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check
8	Disk unit interface parity check
9-11	Not used
12-15	Write error

Interrupt Status Byte

Bit	Meaning
0	Device dependent status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

Interrupt Condition Codes

CC value	Meaning
0	Controller end
1	Not used
2	Exception
3	Device end
4	Attention
5	Not used
6	Attention and exception
7	Attention and device end

Operate I/O Instruction Condition Codes

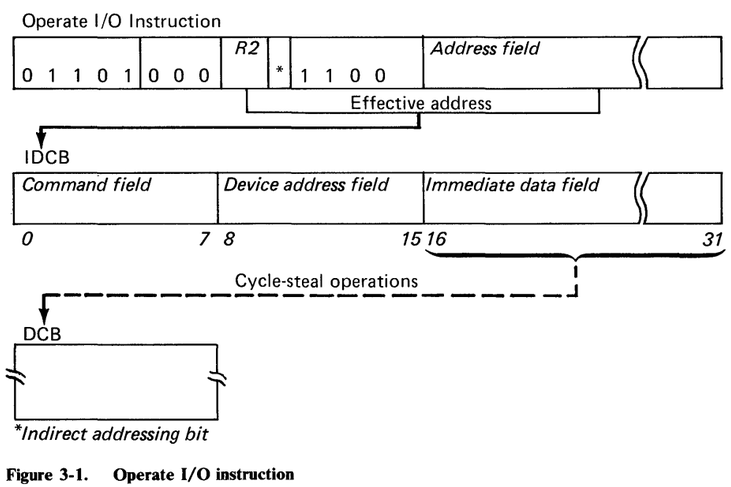
CC value	Meaning
0	Device not attached
1	Busy
2	Busy after reset
3	Command reject
4	Not used
5	Interface data check
6	Controller busy
7	Satisfactory

Operations

This chapter describes how the processor transfers data to and from the disk unit. It includes descriptions of the Operate I/O instruction and its associated commands, status words, and condition codes. The processor initiates all disk operations by issuing an Operate I/O instruction, and then uses the processor I/O channel to transfer data to and from the disk unit.

The Operate I/O instruction is a privileged instruction. Its effective address (the combination of the R2 and address fields) points to an immediate device control block (IDCB) in processor storage. The IDCB contains a command, a device address, and an immediate data field.

The command defines the type of I/O operation; the device address identifies the device on which the operation is to be performed.



*Indirect addressing bit

Figure 3-1. Operate I/O instruction

The use of the information in the IDCB's immediate data field depends on the mode of operation. For direct program control (DPC) operations, the immediate data field is used as a data word; for cycle-steal operations, this field points to a device control block (DCB) that contains additional information needed to perform the operation. The IDCB must be on a fullword boundary. Refer to an appropriate processor description manual listed in the Preface for a more detailed description.

Sector/Record Addressing

Each data record (data record 1 or data record 2) must be addressed individually; however, multiple-data-record operations can be performed If, during a multiple-data-record operation data record 1 is specified, the operation is performed first on all data record 1's then on data record 2's. For example, when reading six data records starting at sector 29, data record 1, the data records would be read in the following order:

Sector	Data record number
29	1
30	1
31	1
00	2
01	2
02	2

Because the 4963 operates in interleaved mode, the disk must make two complete revolutions to read or write all data records on a track.

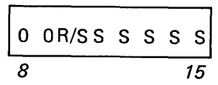
The address of the data record to be operated on (or the first data record of a multiple record operation) is contained in device control block (DCB) words 1 and 2. Word 1 contains the flag field and the sector/record number field; word 2 contains the head and cylinder number information. The sector/record number byte of word 1 contains the physical sector number for a read ID, read ID extended, write ID, write ID extended, or a read diagnostic operation. If a data or scan operation is to be performed, the sector/record number byte contains the record number.

Flag Field (DCB word 1)

For bit designations of the flag field, refer to "Flag Field" under "Sector Format" in this chapter. The flag field must match the field previously written on the disk, except for bit 4. Bit 4 is not used for comparison by the disk unit controls.

Sector and Record Number Field (DCB word 1)

The format of this byte is:



Up to 33 sectors (numbered hex 00–20) can be addressed by the bits labeled S, which specify the sector number. The bits labeled S plus the bit labeled R specify a record number. When the R-bit is 0, data record 1 is selected; when the R-bit is 1, data record 2 is selected. Up to 64 records (numbered hex 00–3F) can be addressed.

Physical sector numbers	Logical sector numbers							
	Sector number on disk	Heads 0, 4, 8	Sector number on disk	Heads 1, 5, 9	Sector number on disk	Heads 2, 6, 10	Sector number on disk	Heads 3, 7
0	00	0	30	24	20	16	10	8
1	02	1	32	25	22	17	12	9
2	04	2	34	26	24	18	14	10
3	06	3	36	27	26	19	16	11
4	08	4	38	28	28	20	18	12
5	0A	5	3A	29	2A	21	1A	13
6	0C	6	3c	30	2C	22	1C	14
7	0E	7	3E	31	2E	23	1E	15
8	10	8	00	0	30	24	20	16
9	12	9	02	1	32	25	22	17
10	14	10	04	2	34	26	24	18
11	16	11	06	3	36	27	26	19
12	18	12	08	4	38	28	28	20
13	1A	13	0A	5	3A	29	2A	21
14	1C	14	0C	6	3C	30	2C	22
15	1E	15	0E	7	3E	31	2E	23
16	20	16	10	8	00	0	30	24
17	22	17	12	9	02	1	32	25
18	24	18	14	10	04	2	34	26
19	26	19	16	11	06	3	36	27
20	28	20	18	12	08	4	38	28
21	2A	21	1A	13	0A	5	3A	29
22	2C	22	1C	14	0C	6	3C	30
23	2E	23	1E	15	0E	7	3E	31
24	30	24	20	16	10	8	00	0
25	32	25	22	17	12	9	02	1
26	34	26	24	18	14	10	04	2
27	36	27	26	19	16	11	06	3
28	38	28	28	20	18	12	08	4
29	3A	29	2A	21	1A	13	0A	5
30	3C	30	2C	22	1C	14	0C	6
31	3E	31	2E	23	1E	15	0E	7
32	40	32	40	32	40	32	40	32

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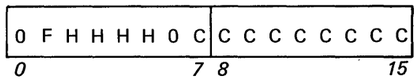
Head and Cylinder Word (DCB word 2)

The format for this word is:



Bits 2–5 (labeled H) specify the head number, bits 7–15 (labeled C) specify the cylinder number. (For further information, refer to "Address Field" under "Sector Format" in this chapter.)
The highest movable-head number than can be addressed without an error is hex A (decimal 10); therefore, 11 movable heads can be addressed (hex 0–A). If bit 1 (labeled F) is on, a fixed head is specified and all cylinder bits (labeled C) are set on. If bit 1 is off, movable heads are specified. The highest fixed head that can be addressed without an error is 7; therefore, eight fixed heads can be addressed (0–7). When fixed heads are installed, the addresses of the movable heads are hex 1–A.

The maximum value for the cylinder number during a movable-head operation is hex 167 (decimal 359). When a fixed head is specified, a value of hex 1FF (decimal 511) must also be specified (all cylinder bits on).

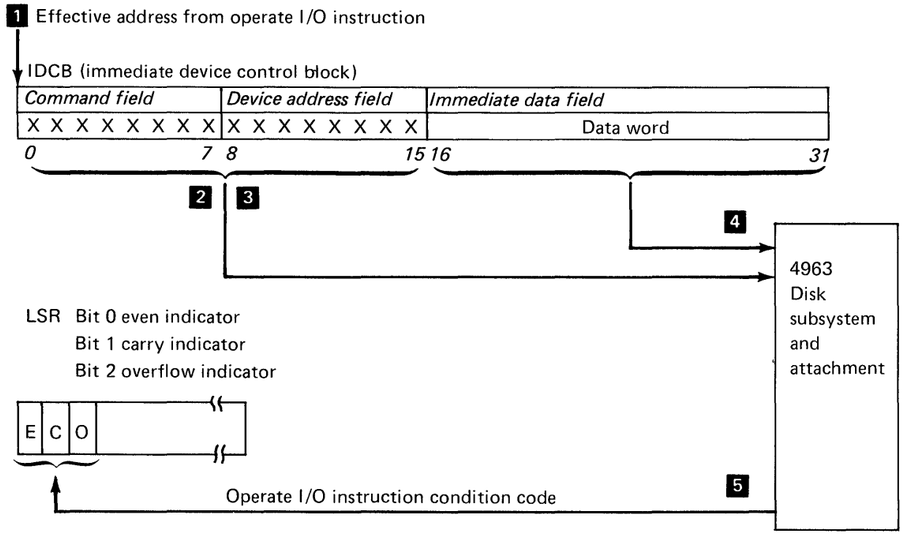
The use of the information in the IDCB's immedidate data field depends on the mode of operations. For direct program control (DPC) operations, the immediate data field is used as a data word; for cycle-steal operations, this field points to a device control block (DCB) that contains additional information needed to perform the operation. The IDCB must be on a word boundary. Refer to an appropriate processor description manual listed in the Preface for a more detailed description.

DPC

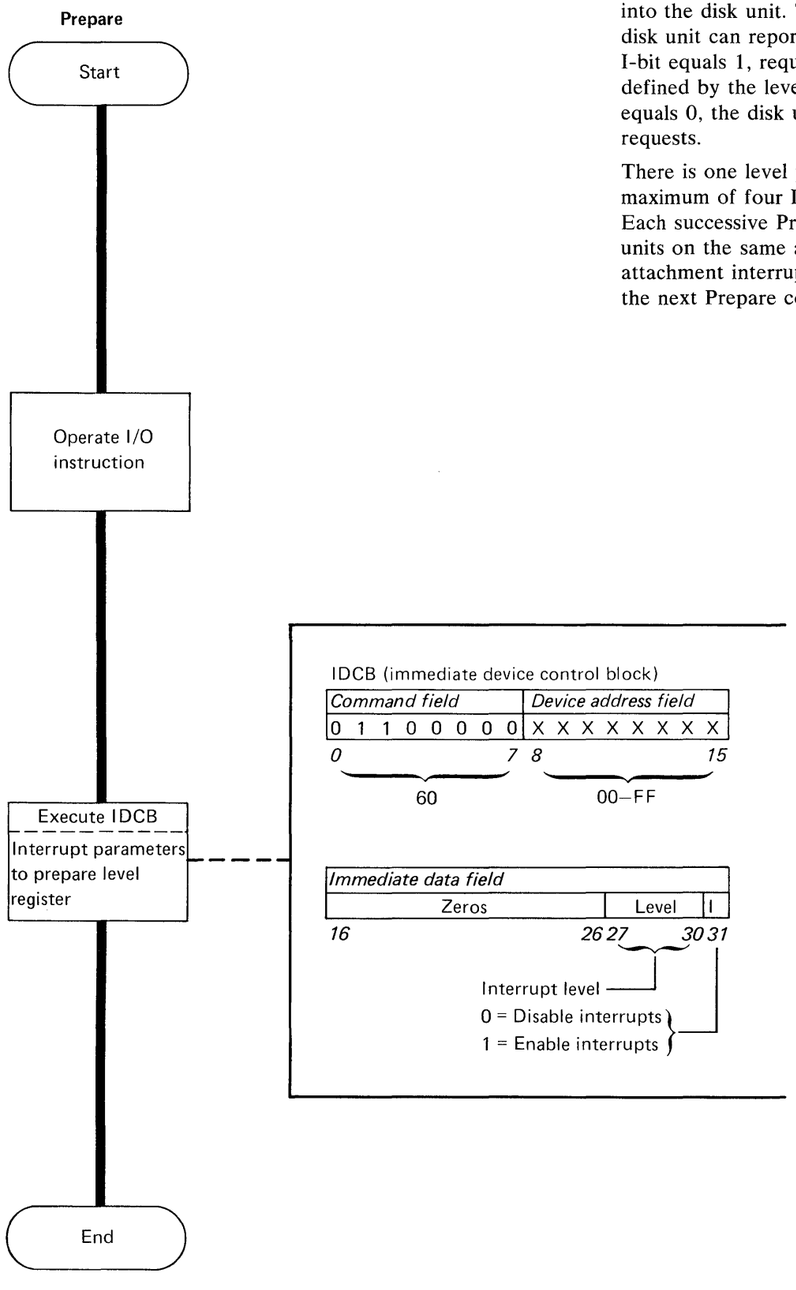
A DPC operation causes an immediate transfer of data or control information to or from the disk unit.

An Operate I/O instruction must be executed for each data transfer. Each execution causes the following:

1. The Operate I/O instruction's effective address points to an IDCB in processor storage 1.
2. The I/O channel uses the IDCB's device address field 3 to select the disk unit, and the command field 2 to determine the operation to perform.
3. The processor transfers the contents of the immediate data field to the disk unit, or transfers information from the disk unit to the immediate data field, depending on the command being executed 4.
4. The disk unit sends a condition code to the level status register (LSR) in the processor 5. Condition codes are explained under "Condition Codes" later in this chapter.



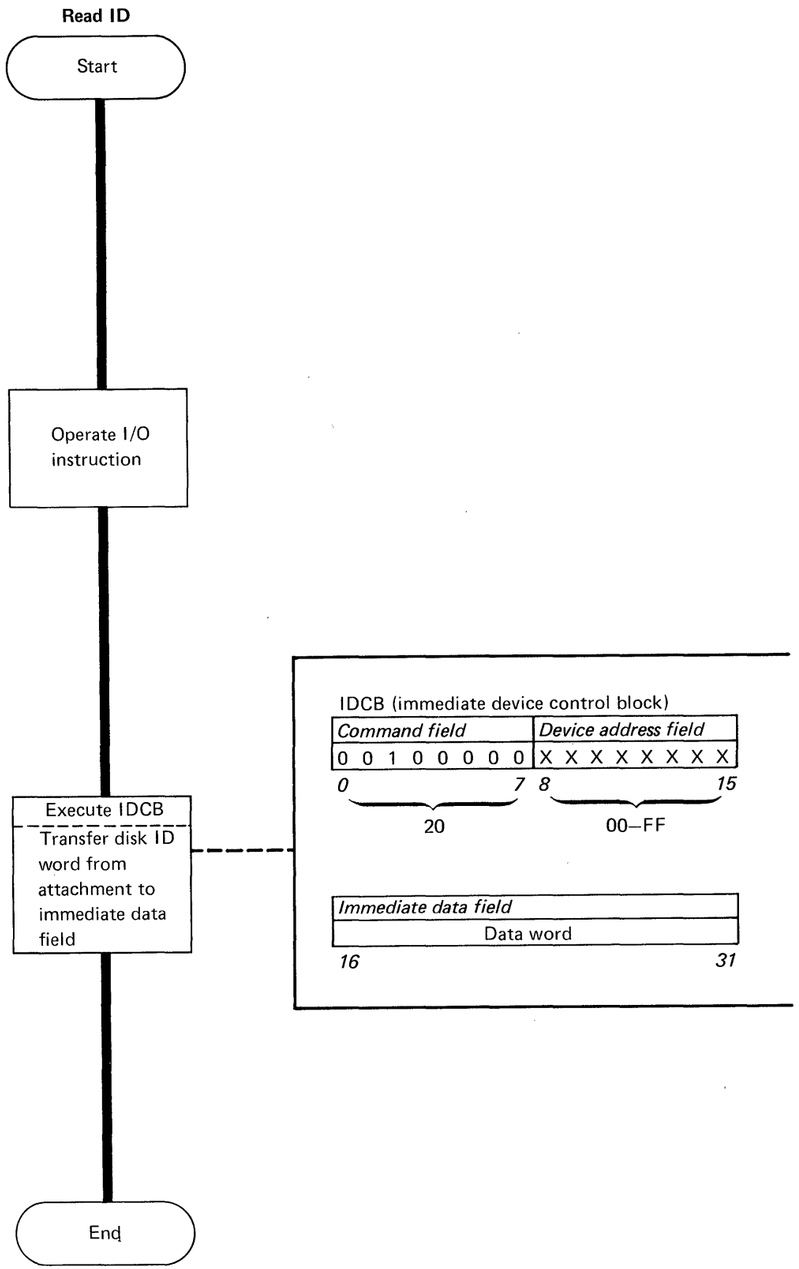
Commands



Prepare

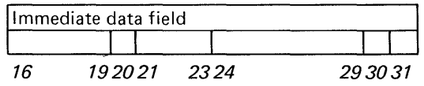
This command loads the interrupt level and I-bit into the disk unit. The I-bit (31) determines if the disk unit can report I/O interrupt requests. If the I-bit equals 1, requests are presented on the level defined by the level bit field (27–30); if the I-bit equals 0, the disk unit cannot present interrupts requests.

There is one level per attachment bit, up to a maximum of four I-bits, one for each disk unit. Each successive Prepare command issued to disk units on the same attachment reassigns the attachment interrupt level to remain in effect until the next Prepare command.



Read ID

This command transfers the identification (ID) word from the disk unit to the immediate data field of the IDCB. After command execution, the immediate data field contains:

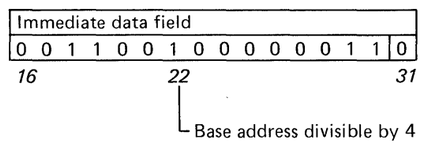


Bits 16–19 class code (subsystem configuration)
20 reserved
21–23 base address divisibility code:

bit	21	22	23	base address divisibility of
value	0	0	1	2
	0	1	0	4

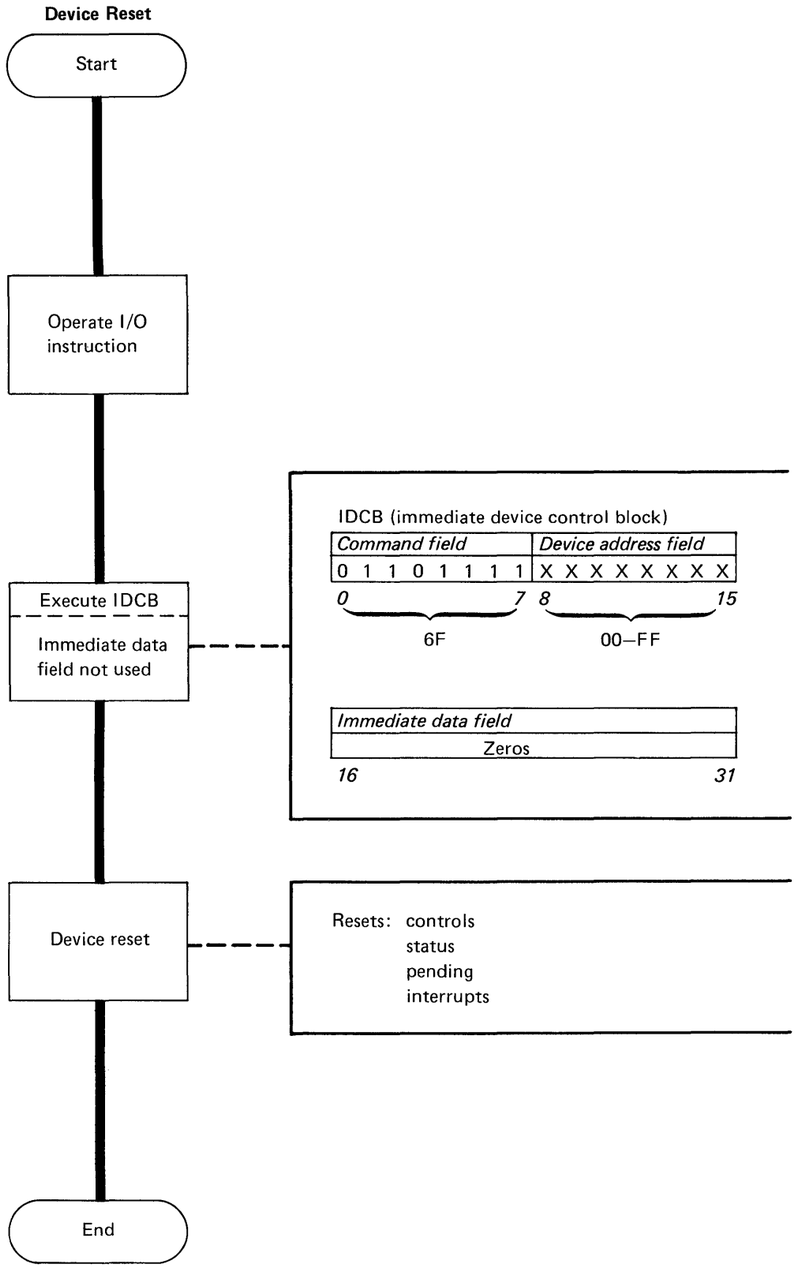
24–29 4963 disk unit
30 1 = cycle steal device
0 = not cycle steal device
31 1 = OEM device
0 = IBM device

The Attachment Feature ID is used to determine the existing subsystem configuration. For example, a Read ID command issued to device address 8 (first device) contains 3026 in the immediate data field.



This indicates a base divisibility of 4, and that a 4963 is attached. A second Read ID command must be issued to base address plus 3, or in this case, to base address 11. Because the fourth disk unit in this example is not attached, a condition code of 0 is posted. If a fourth disk unit is attached, the condition code value is not 0.

As another example, assume that two disk units are attached and a Read ID command issued to base device address 6 contains 3106 in the immediate data field. This indicates a base divisibility of 2 and that a 4963 is attached. A second Read Device ID command is issued to base address plus 1, or in this case, to base address 7. Since a second disk unit is attached, the condition code value is not 0.



Device Reset

This command resets any pending interrupt requests or busy conditions in the disk unit. The prepare level and the residual address are not affected. The immediate data field is not used.

Halt I/O

IDCB (immediate device control block)

Command field								*Device address field*							
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
0							*7*	*8*							*15*
F0								00							

Immediate data field
16 … *31*

This is a channel-directed command that halts all I/O activity on the I/O channel and resets all devices. The immediate data field of the IDCB is not used. Any pending interrupt or busy condition is reset. The prepare level and the residual address are not affected.

Diagnostic Commands

The following commands are used to test the 4963 subsystem operations in DPC mode.

Load Sense Diagnostic Word 1

IDCB (immediate device control block)

Command field	Device address field
0 1 0 0 1 0 0 0	X X X X X X X X
0 7	8 15
48	00–FF

Immediate data field
Data word
16 31

This command moves data from the IDCB to the disk unit controls' buffer storage register.

Load Sense Diagnostic Word 2

IDCB (immediate device control block)

Command field	Device address field
0 1 0 0 1 0 0 1	X X X X X X X X
0 7	8 15
49	00–FF

Immediate data field
Data word
16 31

This command allows the disk unit controls and the disk attachment to operate in single-cycle mode for diagnostic purposes. A diagnostic register is read into the immediate data field and has the following significance:

Bit	Meaning
0–11	Unassigned
12	Diagnostic control
13	Single-cycle control
14	Diagnostic instruction
15	Unassigned

Attachment Storage Diagnostic

IDCB (immediate device control block)

Command field	Device address field
0 1 0 0 1 1 1 0	X X X X X X X X
0 7	8 15
4E	00–FF

Immediate data field
Data word
16 31

This command instructs the attachment to execute a storage diagnostic test. Any detected failure in the attachment storage is reported as an exception interrupt request with more status available. The attachment equipment check bit (10), in cycle steal status word 4, is set to 1 if an error occurred. The data word of the Write Immediate command is not used, but is checked for parity. A normal device-end interrupt indicates a successful storage check. This is an interrupt causing operation.

Load Disk Unit Control Block 0

IDCB (immediate device control block)

Command field	Device address field
0 1 0 0 0 0 0 0	X X X X X X X X
0 7	8 15
40	00–FF

Immediate data field
Data word
16 31

This command moves the first word of the disk unit control block into the immediate data field.

Attachment General Diagnostic Test

IDCB (immediate device control block)

Command field	Device address field
0 1 0 0 0 0 0 1	X X X X X X X X
0 7	8 15
41	00–FF

Immediate data field
Data word
16 31

This command causes the attachment to test its data registers and control latches. Any detected failure causes an exception interrupt request with the attachment equipment check bit (10) set to 1 in cycle-steal status word 4.

Load Seek Required Address Direct

IDCB (immediate device control block)

Command field	Device address field
0 1 0 1 0 0 1 0	X X X X X X X X
0 7	8 15
52	00–FF

Immediate data field
Data word
16 31

This is a special diagnostic command and must be issued sequentially prior to the Load Seek Control Direct command.

Load Seek Control Direct

IDCB (immediate device control block)

Command field	Device address field
0 1 0 1 0 0 1 1	X X X X X X X X
0 7	8 15
53	00–FF

Immediate data field
Data word
16 31

These commands are special diagnostic commands for the disk unit controls. They perform special diagnostic wrap functions and must be issued in this sequence: Load Seek Required Address Direct command followed by a Load Seek Control Direct command. The immediate data field from these commands is not used. The correct head and cylinder numbers must be loaded in the disk unit controls prior to issuing these commands. Loading the head and cylinder numbers can be accomplished by issuing a Start command that includes a DCB.

Note: Word 2 of the DCB is always loaded into the disk unit controls even though it is not required to perform the operation.

Recommended issuing sequence and expected response:

1. Issue a Start command, word 2 of the DCB loads the head and cylinder numbers in the disk unit controls.
2. Issue Load Seek Required Address Direct command. No seek operation is initiated. An interrupt is posted at the completion of this command.
3. Issue Load Seek Control Direct command. A seek operation is executed. An interrupt is posted at the end of this operation.

Sense Disk Unit Direct

IDCB (immediate device control block)

Command field	Device address field
0 1 0 1 0 1 0 0	X X X X X X X X
0 7	8 15
54	00–FF

Immediate data field
Data word
16 31

This command causes the disk unit controls to read the sense byte from the selected disk unit. An interrupt request is presented at the completion of the execution. In order to read the byte into processor storage, a Start Cycle Steal Status command must be issued. Status word 5, bits 8–15, contains the sense byte. The sense byte bit definitions are listed under status words 11 and 12 of the start cycle steal status operation found later in this chapter.

Sense Disk Unit Diagnostic Bytes 1, 2, and 3

IDCB (immediate device control block)

Command field	Device address field
0 1 0 1 0 1 0 1	X X X X X X X X
0 7	8 15
55	00–FF

Immediate data field
Data word
16 31

This command causes the disk unit controls to read three sense bytes from the selected disk unit. An interrupt request is presented at the completion of the execution. A subsequent cycle steal status operation must be issued to retrieve the diagnostic sense bytes into processor storage. The sense byte bit definitions are listed under status words 11 and 12 of the start cycle steal status operation found later in this chapter.

Multisample Pulse Test

IDCB (immediate device control block)

Command field	Device address field
0 1 0 1 0 1 1 0	X X X X X X X X
0 7	8 15
56	00–FF

Immediate data field
Data word
16 31

This command executes the multisample pulse test to the selected disk unit to determine if any of the lines are active. An interrupt request is presented at the completion of the execution. A cycle steal status operation cycle steals the diagnostic bytes into storage. The sense byte bit definitions are listed under status words 11 and 12 of the start cycle steal status operation found later in this chapter.

Sense Disk Unit Diagnostic Wrap

IDCB (immediate device control block)

Command field	Device address field
0 1 0 1 0 1 1 1	X X X X X X X X
0 7	8 15
57	00–FF

Immediate data field
Data word
16 31

This command causes the disk unit controls to read the low-order byte of the cylinder number. This byte contains error information if it is read following an error. An interrupt request is presented at the completion of the execution. This byte is read into processor storage via the cycle steal status operation. The sense byte bit definitions are listed under status words 11 and 12 of the start cycle steal status operation found later in this chapter.

Disk Speed Timing Diagnostic

IDCB (immediate device control block)

Command field	Device address field
0 1 0 1 1 0 1 0	X X X X X X X X
0 7	8 15
5A	00–FF

Immediate data field
Data word
16 31

This command times the disk for 20 revolutions and returns the count in diagnostic sense bytes 1 and 2. The system can calculate the elapsed time using the following formula:

T(time in microseconds)=(10509*B_1 + 41*B_2) .55

Resolution is less than 40 microseconds.

B_1 = Disk Unit Diagnostic Sense Byte 1 (start cycle steal status word 11 bits 0–7).

B_2 = Disk Unit Diagnostic Sense Byte 2 (start cycle steal status word 11 bits 8–15).

In order to read the sense bytes into storage, a start cycle steal status operation must be initiated. The sense byte bit definitions are listed under status words 11 and 12 of the start cycle steal status operation found later in this chapter.

Note: The diagnostic timing commands require dedication of the attachment such that no other operations will be serviced during execution of the command. Therefore, timing diagnostics cannot be used during a normal operation without the risk of degraded performance. Also, channel activity during execution could degrade the timing resolution.

Disk Unit Controls Diagnostic

IDCB (immediate device control block)

Command field	Device address field
0 1 0 1 1 1 0 1	X X X X X X X X
0 7	8 15
5D	00–FF

Immediate data field
Data word
16 31

This command permits the disk unit controls to operate in an interleaved or noninterleaved mode during diagnostic operations. The IBM Series/1 4963 Disk Subsystem operates in interleaved mode only.

Note: A disk unit controls reset or a system reset will reset the format (interleaved or noninterleaved) to the interleaved mode. If nondiagnostic operations are attempted in noninterleaved mode, the results will be unpredictable. Therefore, the use of the noninterleaved mode should be limited to diagnostic purposes only.

The immediate data field for this command performs the following operations:

04AE - Set format (interleaved)

05AE - Set format (noninterleaved)

These operations set the format for interleaved or noninterleaved diagnostic operations. This operation overrides the state of the format originally designated by "jumper" wiring.

Diagnostic Reset Disk Unit Controls

IDCB (immediate device control block)

Command field	*Device address field*
0 1 0 0 1 1 1 1	X X X X X X X X
0 *7*	*8* *15*
4F	00–FF

Immediate data field
Data word
16 *31*

This command resets the disk unit controls. All disk unit operations in progress, but not yet interrupted to the attachment, are terminated and end with an error or unpredictable results. Therefore, its use should be limited to diagnostic purposes only.

Force End Operation

IDCB (immediate device control block)

Command field	*Device address field*
0 1 0 0 1 1 0 1	X X X X X X X X
0 *7*	*8* *15*
4D	00–FF

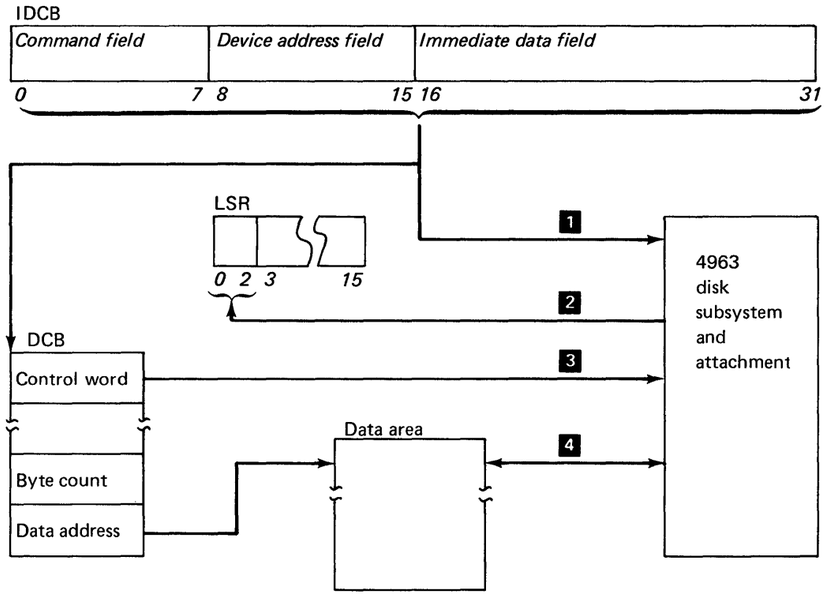
Immediate data field
Data word
16 *31*

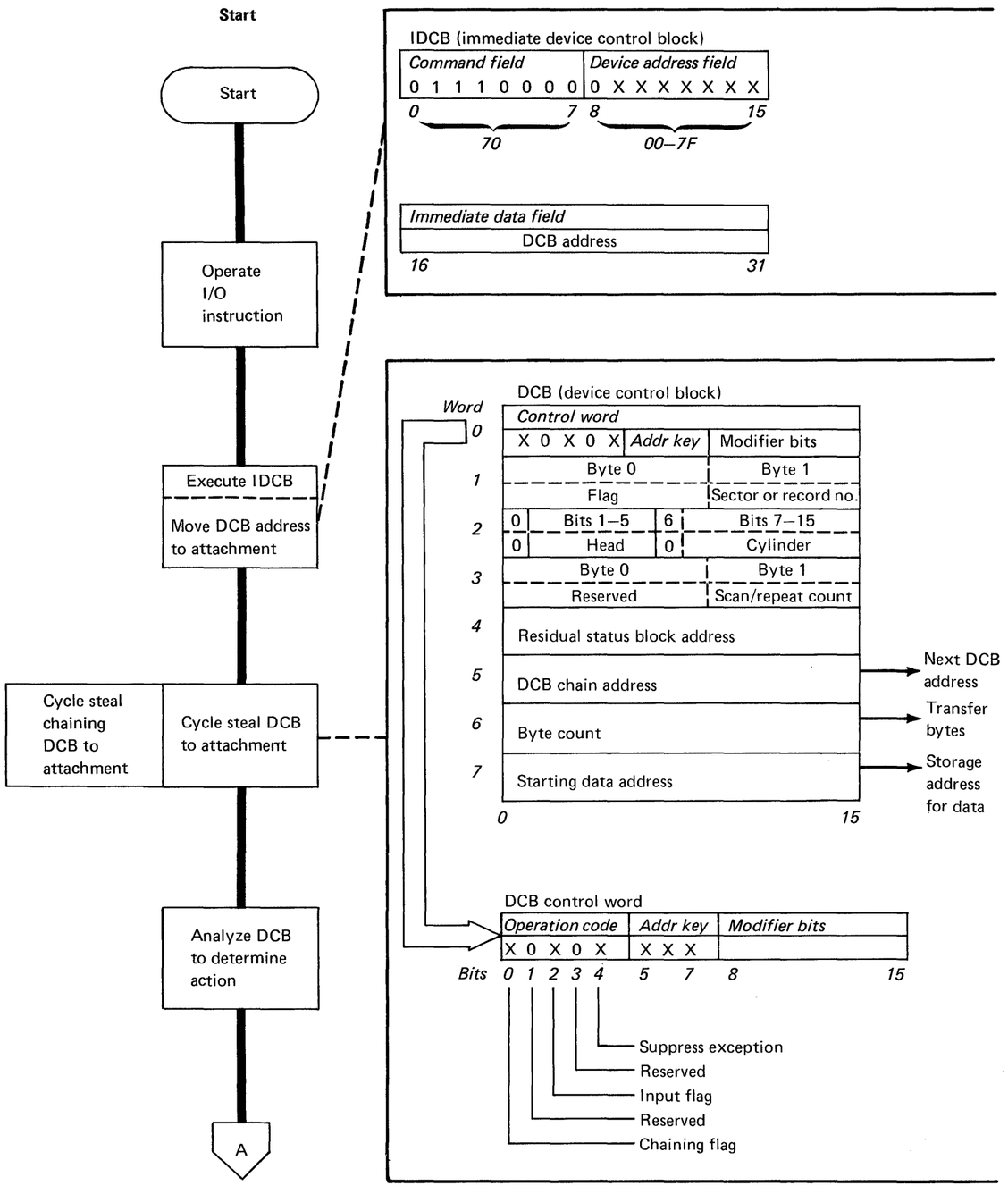
This command sets the end operation trigger equal to 1, and causes the disk unit to post status, terminate any disk operations in progress at the next end store time, terminate the data transfer to the processor, and interrupt the processor with an end operation interrupt and any other interrupt conditions on. The end operation interrupt is transmitted to the processor only if an operation is in progress.

Cycle Steal

Command execution in cycle-steal mode permits overlapping an I/O operation with processor operations and other I/O operations.

As is true for other commands, the processor transfers the IDCB under direct program control from processor storage to the attachment 1, and after the attachment accepts the IDCB, it sends a condition code back to the processor 2. The processor is now free to continue with other operations while the attachment uses the information in the IDCB to execute the command. The IDCB's immediate data field contains the address of a DCB. This eight-word DCB contains parameters that define and control the I/O operation. The attachment "steals" the DCB words 3 and the data 4 it needs to execute the operation. DCBs and RSBs are cycle stolen with an address key equal to 0. Each data transfer reduces a preset byte count in DCB word 6. When the data transfer ends (byte count equals 0), an interrupt request is sent to the processor. The processor then accepts the interrupt condition code and an interrupt ID word from the attachment.





Start

The Start command initiates I/O operations that transfer data to or from processor storage in cycle-steal mode. An interrupt request is sent to the processor when the I/O operation ends. The control information and parameters required for a particular disk operation must be stored in the DCB associated with that operation.

The eight words in the DCB and their bit configurations are as follows:

DCB Word 0—Control Word

This is a 16-bit word that defines the cycle-steal operation. This word contains two bytes of control parameters to be used with the particular Start command to be performed.

Bit 0 Chaining flag. When this bit equals 1, it tells the attachment to perform a chaining operation. Chaining means the attachment completes the current operation but does not present an interrupt request to the processor. Instead, the attachment fetches the next DCB in the chain and performs the next operation. DCB word 5 tells the attachment where to look for the next DCB. Chaining continues until a DCB is fetched that has the chaining bit in the control word (DCB word 0) equal to 0, indicating the last operation in the chain. If an error occurs, chaining to succeeding DCBs is automatically suspended, and an interrupt request is sent to the processor. Normally, an interrupt is not requested until the disk unit has completed the last operation in the chain. DCB chaining for the 4963 is valid only for a Start command.

Bit 1 This bit is not used and must remain 0 or a DCB specification check occurs.

Bit 2 Input flag. The condition of this bit determines the direction that data is to be transferred. When this bit equals 1, data is transferred from the disk unit into processor storage. When this bit equals 0, the cycle-steal data transfer is from processor storage to the disk unit.

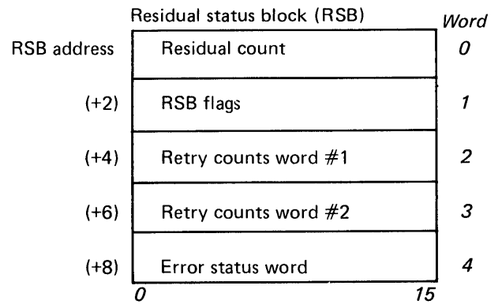
Bit 3 This bit is not used and must remain 0 or a DCB specification check occurs.

Bit 4 Suppress exception (SE). When this bit equals 1, it suppresses the reporting of some exception conditions that otherwise would cause an exception interrupt request.

When this bit equals 1, automatic error recovery procedures are invoked and the disk unit status is stored at the address specified by the residual status block (RSB) address field of DCB word 4, before chaining or terminating. The residual status block is not stored if a permanent error condition has occurred. Also, the SE bit, when on, initiates automatic alternate sector processing. If a defective sector has been assigned to an alternate sector, and the SE bit equals 1, the disk access mechanism seeks to the alternate address, processes the data as indicated, and returns to the original track to complete the operation.

A

The residual status block is available at the end of the operation that uses suppress exception. The format and a description of the residual status block words follow:



Word 0—residual count—always 0 for 4963 subsystem

Word 1—residual status block flags

Bit 0	end of chain
Bit 1	retry
Bits 2–14	reserved
Bit 15	no exception

Word 2—retry count word 1—temporary error retry counts

Bits 0–3	cyclic redundancy check (CRC)
Bits 4–7	write echo check
Bits 8–11	missing sector pulse
Bit 12	data unsafe
Bit 13	not ready
Bits 14–15	reserved

Word 3—retry counts word 2—extension of temporary error retry counts

Bits 0–3	no record found
Bit 4	storage data check
Bit 5	invalid storage address
Bit 6	protect check
Bit 7	interface data check
Bit 8	disk unit interface parity check
Bits 9–11	reserved
Bits 12–15	write error

Word 4—error status word

Bits 0–2	reserved
Bit 3	an assigned alternate sector has been successfully processed
Bit 4	temporary error retry operation has been retried by the attachment error count of one or more in RSB words 2 or 3
Bits 5 6 7	configuration
0 0 0	reserved
0 0 1	reserved
0 1 0	model 29A&B (no fixed heads)
0 1 1	model 64A&B (no fixed heads)
1 0 0	disk unit not attached
1 0 1	reserved
1 1 0	model 23A&B (eight fixed heads)
1 1 1	models 58A&B (eight fixed heads)
Bit 8	scan not equal, a requested scan operation has not been met
Bit 9	scan equal—an equal condition has occurred on a scan operation
Bits 10–12	reserved
Bit 13	end of disk—an operation has caused automatic cylinder switching to cylinder (359), the customer engineer (CE) cylinder, which is reserved for diagnostic purposes
Bits 14–15	reserved

Bits 5–7 Address key. This is a three-bit key that the disk unit presents, during data transfers, to verify that the program has authorization to access processor storage. An incorrect address key causes an exception interrupt (condition code 2).

Bits 8–15 Modifier field. The bits in this field describe the specific cycle-steal operation requested with this DCB.

This disk operations initiated by a Start command are:

	Bit 1	Bits 8–15
Seek	0	0000 0000
Recalibrate	0	0000 0001
Calibrate	0	0000 1001
Overlapped seek	0	0000 1000
Timed seek diagnostic	0	0000 1011
Read data	1	0001 X000
Read verify	0	0001 X001
Read data repeat	1	0001 X010
Read disk unit data buffer diagnostic	1	0001 0011
Read sector ID	1	0001 X100
Read sector ID extended	1	0001 X101
Read diagnostic record 1	1	0001 X110
Read diagnostic record 2	1	0001 X111
Write data	0	0010 X000
Write data with read verify	0	0010 X001
Write data repeat	0	0010 X010
Write data repeat with read verify	0	0010 X011
Write sector ID with read verify	0	0010 1101
Write sector ID extended with read verify	0	0010 1111
Write data security with 0 read verify	1	1010 X001
Scan equal	1	0011 X000
Scan low equal	1	0011 X001
Scan high equal	1	0011 X010

The X under bit 12 is the automatic seek option for the operation. If bit 12 equals 0, the cylinder, head, and sector number are checked against the current location and a seek operation is initiated as required.

B

DCB Word 1—Flag and Sector or Record Number

The flag byte (bits 0–7) describes the condition of the sectors.

DCB word 1 flag

X	X	X	X	X	X	X	X
0	1	2	3	4	5	6	7

The following bits are described as when equal to 1:

Bit 0—defective data record 2—assigned at factory.

Bit 1—defective data record 1—assigned at factory.

Bit 2—user assigned defect.

Bit 3—protected data area.

Bit 4—sector displaced.

Bit 5—sector reassigned to an alternate sector.

Bit 6—defective sector assigned at factory (when this bit equals 1, it must be maintained to preserve the integrity of the disk).

Bit 7—an assigned alternate sector.

The sector/record number byte (bits 8–15) contains the identity of the sector or the data record to be processed.

The six bits of information must be right-justified within the byte.

DCB word 1 sector or record

X	X	X	X	X	X	X	X
8	9	10	11	12	13	14	15

Sector numbers are used for the following operations:

- Read sector ID
- Read sector ID extended
- Write sector ID
- Write sector ID extended
- Read diagnostic

Data and scan operations use the data record number.

DCB Word 2—Head and Cylinder

0	H	H	H	H	H	0	C	C	C	C	C	C	C	C	C
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

This word contains the head and cylinder number to be selected. The head number is located in bits 1–5 of the first byte. The cylinder number is located in bits 7–15 of the remainder of the word. Bits 0 and 6 must be written as 0's, otherwise a DCB check occurs.

DCB Word 3—Scan/Repeat Count

This word contains the record count for the total length involved with a scan operation or multiple read/write operations.

DCB Word 4—Residual Status Block Address

The address contained in this word points to five words that are the beginning of a processor storage area where the residual status block is stored. The residual status block is stored only when the SE bit equals 1, and a permanent error did not occur.

DCB Word 5—Chaining Address

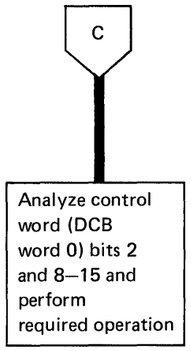
This word contains the location of the next DCB to be executed. If the chain address is odd, an interrupt is posted and a DCB specification check is set in the ISB. The chaining address is not checked unless the chaining flag (bit 0) equals 1 in control word 0.

DCB Word 6—Byte Count

This word contains a 16-bit unsigned integer representing the number of data bytes to be transferred for the current DCB. If the byte count equals 0, no data is transferred. An odd byte count causes a DCB specification check. When the byte count is greater than the maximum allowed for a particular operation, an interrupt is posted and the DCB specification check (bit 3) is set to 1 in the ISB.

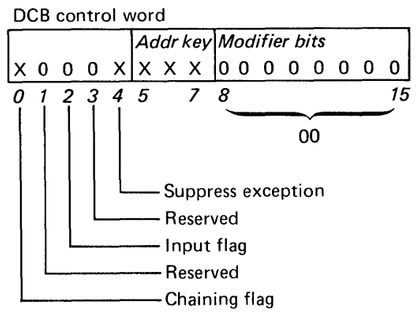
DCB Word 7—Data Address

This word contains the starting storage address for the data associated with the operation to be performed. An odd byte count in this word causes a DCB specification check.

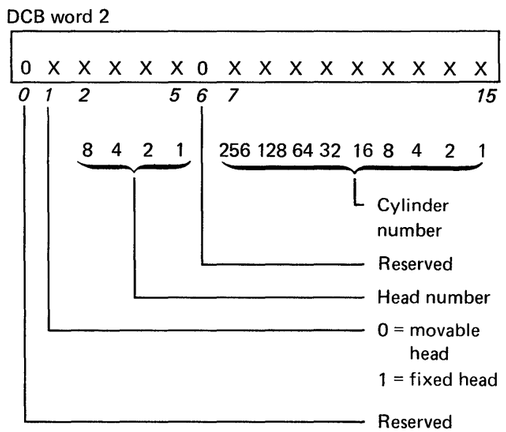


Start Command Operations

Seek



Disk unit I/O operations requiring head movement or selection, must be preceded by a seek operation unless seeking is implied in the DCB. An implied seek requires longer access time. The seek operation causes the movable heads to seek to the cylinder and select the head specified in DCB word 2.

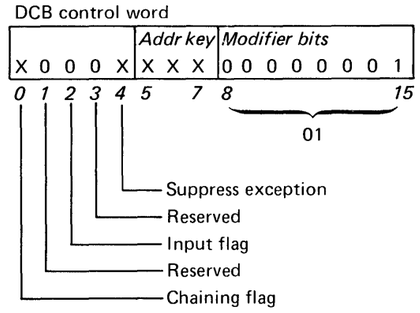


If a fixed head is specified in the DCB, the head is selected and the cylinder is ignored. The DCB associated with a seek operation is transferred from processor storage in cycle-steal mode. An interrupt request is sent to the processor when the disk unit completes the operation. A condition code and interrupt ID word are transferred to the processor when the interrupt is serviced.

Programming considerations:

- If an invalid head is specified in the DCB, no error will be reported until a command that uses the selected head is executed.
- An error condition is returned if a time-out occurs and the seek operation is not complete.

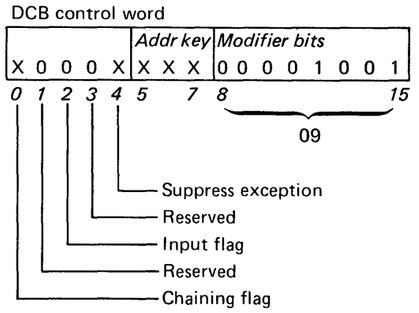
Recalibrate



The recalibrate operation causes the access mechanism to move to cylinder 0, head 1. When the disk unit completes the operation, an interrupt request is sent to the processor, and ready and home conditions are set in the disk unit control block. When the interrupt request is serviced, a condition code and an interrupt ID word are transferred to the processor.

The control information and parameters required for a recalibrate operation must be stored in a DCB containing a control word (DCB word 0) that specifies a recalibrate operation to the disk unit.

Calibrate

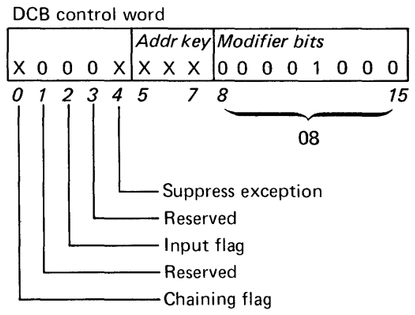


An excessive access time could indicate that a servo mechanism is out of calibration. This operation calibrates the servo mechanism by causing the following events:

1. Executes a recalibrate operation
2. Executes a 128-track seek operation
3. Executes a recalibrate operation

At the end of the second recalibrate operation, the servo mechanism is calibrated, and ready and home conditions are set in the cycle-steal status block. A power on reset causes a calibrate operation. DCB words 1, 2, 3, 6, and 7 are not used for this operation, but are fetched and must have correct parity.

Overlapped Seek

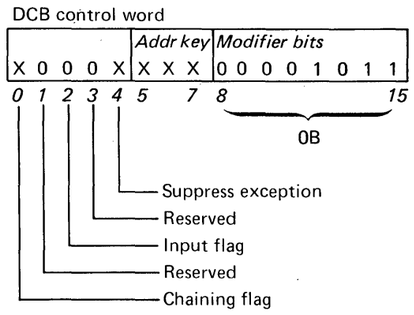


The overlapped seek operation allows overlapping of moving-head seeks with fixed head read, write, or scan operations. This operation can be immediately followed by a seek, or implied seek, to a fixed head. The overlapped seek operation posts an end-operation interrupt after the seek operation is initiated to the disk unit, not on completion, as does the seek operation.

Programming considerations:

- Errors occurring subsequent to the end operation interrupt will not cause an interrupt unless another command to the disk unit is in process when the error is detected.
- If the overlapped seek operation is followed by an operation that requires a moving-head seek before the previous moving-head seek is completed, it results in the second seek being executed after the first overlapped seek is complete.

Timed Seek Diagnostic



This operation measures the elapsed time from when the seek operation begins until the seek-complete interrupt is received. An excessive access time could indicate the need to calibrate the access mechanism. This can be done by turning disk unit power off and then on again, or by initiating a calibrate operation. Counts are returned in diagnostic sense bytes 1 and 2 of cycle steal status word 11. To read the sense bytes into storage, a Start Cycle Steal Status command must be issued. The elapsed time can be calculated by using the following formula:

T(time in microseconds = $(10509*B_1 + 41*B_2)$ .55

B_1 = Disk unit diagnostic sense byte 1 (cycle steal status word 11, bits 0–7).

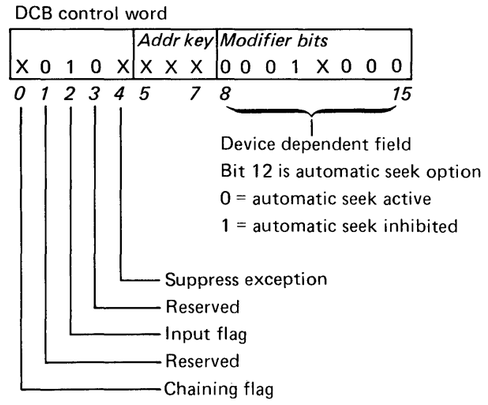
B_2 = Disk unit diagnostic sense byte 2 (cycle steal status word 12, bits 8–15).

Note: To read the sense bytes into storage, a cycle steal status operation must be initiated. Cycle steal status word 11 contains the sense bytes.

Resolution is less than 40 microseconds, excluding the disk unit controls' oscillator error.

Note: Diagnostic timing commands require dedication of the attachment such that no other operations are serviced during execution of this operation. Therefore, timing diagnostics cannot be used during normal operation without the risk of degrading performance. Also, channel activity during execution may degrade the timing resolution.

Read Data



This operation causes data to be read from the disk unit into processor storage in cycle-steal mode. The DCB contains the data address search argument and byte count necessary to complete the operation.

The record is specified by the search argument and is transferred to processor storage as indicated by the data address field of the DCB. The byte count specifies the number of bytes to be transferred. The byte count must be an even number to reflect word boundaries.

If after one revolution, a record has not been found, a no-record-found error is posted, as well as any other errors present.

Up to 65,534 bytes (two bytes less than 256 records) can be read without regard to track or cylinder boundaries and without intermediate interrupts.

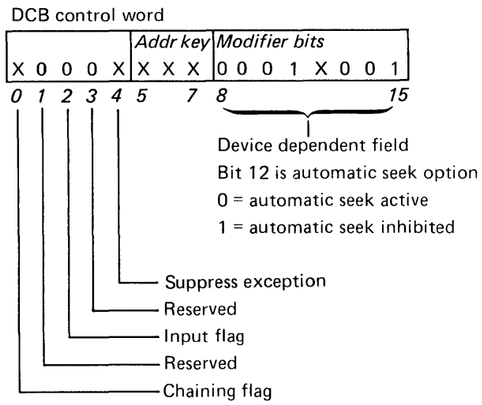
The error recovery procedure for this operation is determined by the setting of control word 0 bit 4. When the SE bit equals 1, the attachment retries the operation eight times before posting a permanent error. When the operation is finished, the status is stored at the location indicated by the residual status block address in the DCB unless an exception condition occurs. In this case, status is available to a Start Cycle Steal Status command.

Note: If a permanent CRC error (data field) is encountered, the data record read from the disk on the last retry will be transferred (cycle stolen) to processor storage before the end-operation interrupt is posted)).

If the SE bit equals 0, there are no retries attempted and any errors result in an exception end of the operation, with status available to a Start Cycle Steal Status command.

This operation supports the auto seek option (bit 12) in the control word of the DCB. If bit 12 equals 0, the search argument is checked against the current location; automatic head and cylinder switching take place at logical end of track. When bit 12 equals 1, the disk unit returns a no-record-found error, if after one revolution, a record has not been found. Also, no data transfer takes place if the correct cylinder and head are not selected.

Read Verify

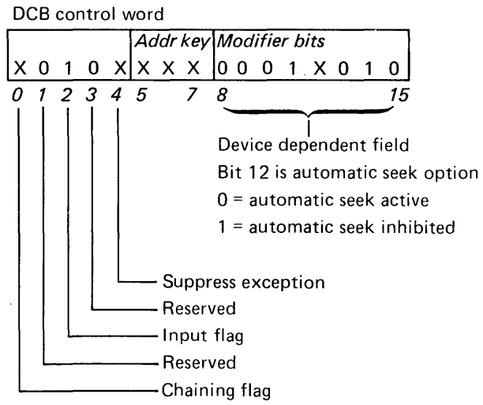


This operation is used to validate data written on the disk. It operates the same as the read data operation except data is not transferred to processor storage during the operation. This operation would normally use the search argument of a previous write data operation. The DCB contains the byte count, the residual status block address, and the search argument.

The error recovery procedure for this operation is determined by the setting of control word bit 4, the SE bit. When the SE bit equals 1, the attachment retries the operation eight times before posting a permanent error. When the operation is completed, the status is stored at the location indicated by the residual status block address in the DCB, unless an exception occurs. In this case, status is available to a Start Cycle Steal Status command.

If the SE bit equals 0, the attachment does not retry the operation and any errors will result in an exception end of the operation with status available to a Start Cycle Steal Status command. This operation supports the auto seek option (bit 12) in the control word of the DCB. If bit 12 equals 0, the search argument is checked against the current location and a seek operation is initiated as required. When bit 12 equals 1, the attachment returns a no-record-found error and no data transfer takes place if the correct cylinder and head are not selected.

Read Data Repeat



This operation is similar to a read data operation except only data for the last record read is transferred to processor storage. All records up to the last record are not transferred but are instead verified for correct CRC error. Only full records may be specified. The byte count in the DCB must be 256 or an exception interrupt occurs with DCB specification check active in the ISB. The number of records to be operated on is contained in the scan/repeat byte of the DCB and must be the number of full records involved in the operation minus one.

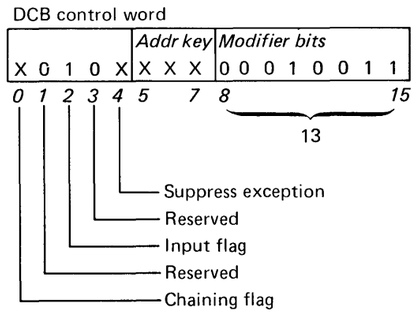
If bit 12 of the control word modifier equals 0, and the record count has not been reduced to 0, automatic head and cylinder switching takes place at logical end of track. Up to 65,536 bytes (256 full records) may be involved in this operation without regard to track or cylinder boundaries and without intermediate interrupts. Regardless of the number of records operated on, only the last 256 bytes of data are transferred to storage.

The error recovery procedure for this operation is determined by the setting of control word bit 4. When the SE bit equals 1, the attachment retries the operation eight times before posting a permanent error. When the operation is finished, the status is stored at the location indicated by the residual status block address in the DCB, if there was no permanent error. After a permanent error, the status is available to a Start Cycle Steal Status command.

If the SE bit equals 0, the attachment does not retry the operation and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports the auto seek option (bit 12) in the control word of the DCB. If bit 12 equals 0, the search argument is checked against the current location and a seek operation is initiated as required. When bit 12 equals 1, the attachment returns a no-record-found error, and no data transfer takes place if the correct cylinder and head are not selected.

Read Disk Unit Data Buffer Diagnostic



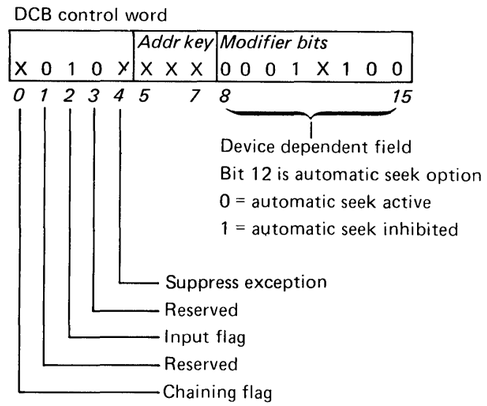
This operation causes the disk unit to cycle steal one 256-byte record from the designated disk unit data buffer into processor storage. The DCB contains the data address, buffer number, and byte count needed by the operation.

The buffer number must be specified in word 3 (8–15) of the DCB. The associated byte count must be specified in word 6 of the DCB.

Valid buffer number	Byte count	Buffer being read
Word 3 (8–15)	Word 6	
00	0100	Disk unit controls buffer area
01	0100	Data buffer area 1
10	0100	Data buffer area 2
11	0100	Data buffer area 3

Note: There is no DCB specification check for this operation.

Read Sector ID



This operation transfers the ID field of a sector into processor storage at the data address specified in the DCB. The count in the byte count field of the DCB is used to determine the number of sector IDs to be read into processor storage. The byte count must be four bytes per sector up to a maximum of 33 sectors per track.

The sector ID field is as follows:

Flag byte								Sector number							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
F	F	F	F	F	F	F	F	0	S	S	S	S	S	S	0

Head number								Cylinder number							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	H	H	H	H	H	0	C	C	C	C	C	C	C	C	C

The starting ID on the track is determined from the sector/record number in word 1 of the DCB. A 00 denotes the first sector ID following index. A count of 01 denotes the second, and so forth.

Head switching does not take place with this operation. All transfers crossing "index" will continue on the same track until the logical end of the track.

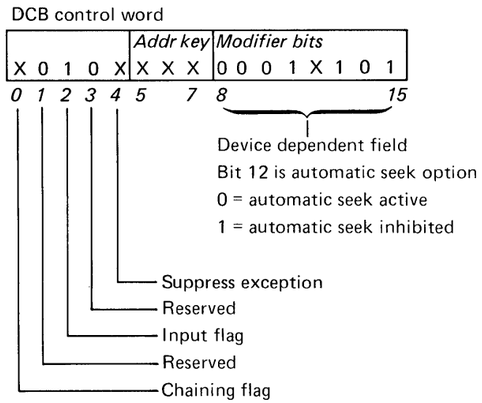
The error recovery procedure for this operation is determined by the setting of control word bit 4, the SE bit. When the SE bit equals 1, the attachment retries the operation eight times before posting a permanent error. When the operation is completed, the status is stored at the location indicated by the residual status block address in the DCB, unless an exception condition occurs. In this instance, status is available to a Start Cycle Steal Status command.

If the SE bit equals 0, the attachment does not retry the operation, and a CRC error results in hex FF (all bits equal to a 1 in all four bytes) being inserted into the ID area for the attempted ID. The read sector ID operation is then resumed, and continues to the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports the auto seek option (bit 12) in the control word of the DCB. If bit 12 equals 0, the search argument (word 2) is checked against the current location and a seek operation is initiated as required.

Note that read sector ID and read sector ID extended do not require word 2 of the DCB except when an auto seek is specified.

Read Sector ID Extended



This operation transfers the ID field of a sector, which has been displaced by 64 bytes from its normal location on the disk, into processor storage at the data address specified in the DCB. The byte count field must be four bytes per sector up to a maximum of 33 sectors per track.

The starting ID on the track is determined from the sector/record number in word 1 of the DCB. A 00 denotes the first sector ID following index. A 01 denotes the second, and so forth.

Head switching does not take place with this operation. All transfers crossing "index" will continue on the same track until the logical end of the track.

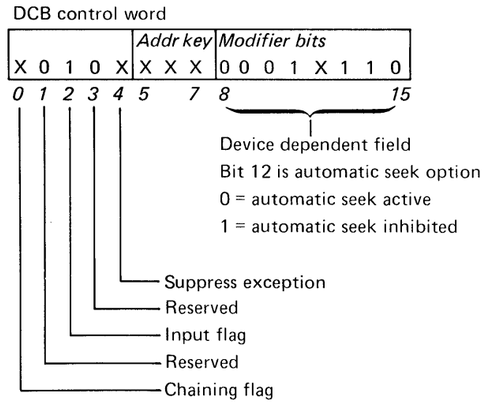
The error recovery procedure for this operations is determined by the setting of control word bit 4, the SE bit. When the SE bit equals 1, the attachment retries the operation eight times before posting a permanent error. When the operation is finished, the status is stored at the location pointed to by the residual status block address in the DCB, unless an exception condition occurs. In this case, status is available to a Start Cycle Steal Status command.

If the SE bit equals 0, the attachment does not retry the operation and a CRC error results in hex FF being inserted into the ID data area for the attempted ID. The read sector ID operation is then resumed, and continues to the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports the auto seek option (bit 12) in the control word of the DCB. If bit 12 equals 0, the search argument (word 2) is checked against the current location and a seek operation is initiated as required.

Note that read sector ID and read sector ID extended do not require word 2 of the DCB except where auto seek is called for.

Read Diagnostic Record 1



This operation is used to recover the first data record associated with a defective sector ID.

The starting ID on the track is determined from the sector/record number in word 1 of the DCB. A 00 denotes the first sector ID following index. A 01 denotes the second, and so forth.

The byte count in the DCB must be 256 bytes and the sector number must be the physical sector containing the record to be recovered.

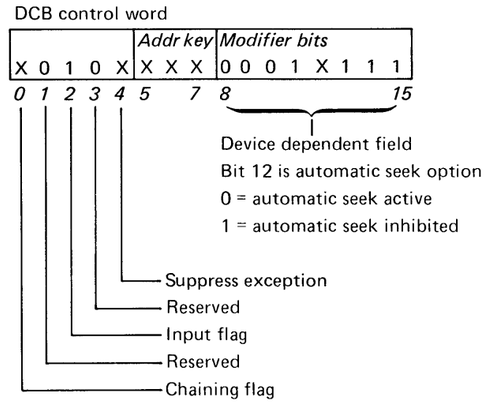
Most automatic error recovery procedures are not supported under the read diagnostic operation. Only disk unit parity check and data check conditions are retried if the SE bit equals 1.

Note: If a permanent CRC error (data field) is encountered, the data record that was read from the disk on the last attempt to retry the operation, will be transferred (cycle steal) to the system before the end-operation interrupt is posted.

This operation supports the auto seek option (bit 12) in the control word of the DCB. If bit 12 equals 0, the search argument is checked against the current location and a seek operation is initiated, as required.

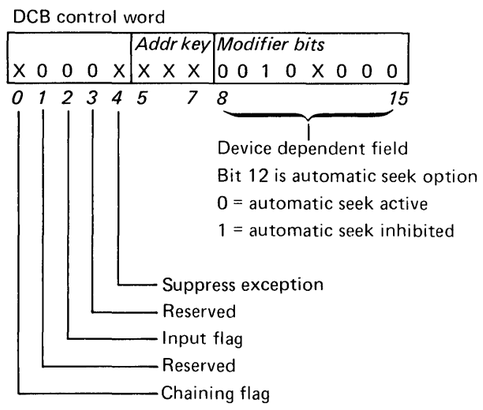
Note that the read diagnostic record 1 and read diagnostic record 2 operations do not require word 2 of the DCB except where auto seek is called for.

Read Diagnostic Record 2



This operation is identical to read diagnostic record 1 except that it is used to recover the second data record associated with a defective sector ID.

Write Data



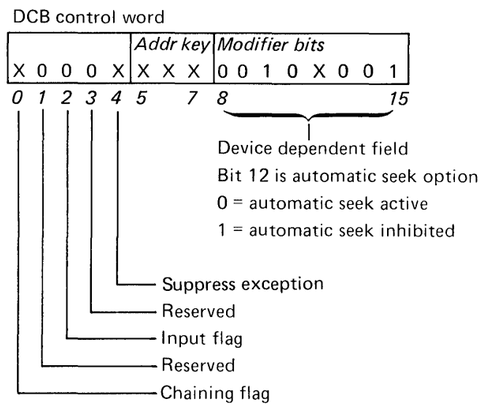
This operation transfers data to the disk unit from the data area designated by the DCB data address, starting at the search argument location specified in the DCB.

If bit 12 of the control-word modifier equals 0, automatic head and cylinder switching take place at the logical end of the track. Up to 65,534 bytes (two bytes less than 256 records) may be written without regard to track or cylinder boundaries and without intermediate interrupts. If the byte count goes to 0 before the end of the complete 256-byte record, the attachment "pads" the remainder of that record with 0's.

The error recovery procedure for this operation is determined by the setting of control word bit 4, the SE bit. When the SE bit equals 0, the attachment retries the operation four times before posting a permanent error. When the operation is finished, the status is stored at the location indicated by the residual status block address in the DCB, unless a permanent error occurs, in which case, the status is available to a Start Cycle Steal Status command. If the write data with verify option is used, only one read operation is used each time the operation is retried.

If the SE bit equals 0, the attachment does not retry the operation and any errors will result in the end of the operation with status available to a Start Cycle Steal Status command.

Write Data with Read Verify



This operation is the same as the write data operation except that data is automatically read back and CRC checked before the operation is completed.

It is recommended that the write data with read verify operation be used instead of separate operations so that automatic error recovery procedures can retry both the write and verify operations if the verify operation fails.

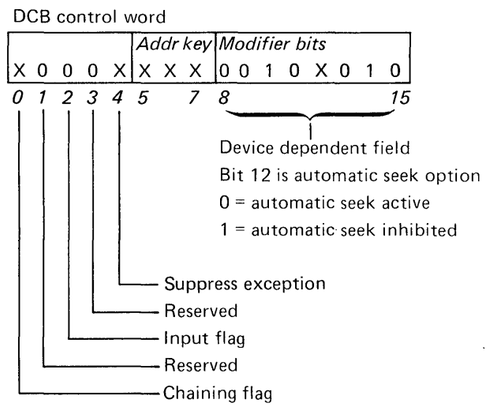
This operation supports the auto seek option (bit 12) in the control word of the DCB. If bit 12 equals 0, the search argument is checked against the current location and a seek operation is initiated as required. When bit 12 equals 1, the attachment returns a no-record-found error, and no data transfer takes place if the correct cylinder and head are not selected.

Fixed Head Data Integrity. Fixed heads physically contact the disk surface when the disk unit power is off and data could be destroyed. Data under the fixed heads can be protected if the following precautions are taken:

- Read and store the ID and data fields before the disk subsystem power is turned off, and

  write the same ID and data fields after the disk subsystem power is restored.
- Do not remove the disk unit from the system enclosure.
- Do not execute the write diagnostic program.

Write Data Repeat



This operation is similar to a write data operation except data is transferred to the disk in full-record increments only and all records are written with the same data. The byte count in the DCB must be 256 or an exception interrupt occurs with a DCB specification check active in the ISB. The attachment transfers the 256 bytes of data addressed by the data address word in the DCB and writes it into the record specified by the search argument. Each successive record is written with the same 256 bytes of data until the end of the operation. The number of records to be written is contained in the scan/repeat count byte of DCB word 3, and is one less than the number of full records to be written.

If bit 12 of the control word modifier equals 0, automatic head and cylinder switching takes place at logical end of track. Up to 65,536 bytes (256 full records) can be written without regard to track or cylinder boundaries and without intermediate interrupts. Regardless of the number of records written, only 256 bytes of data are transferred to the attachment. Therefore, this operation is well suited for initializing large data areas on the disk where minimal storage is needed.

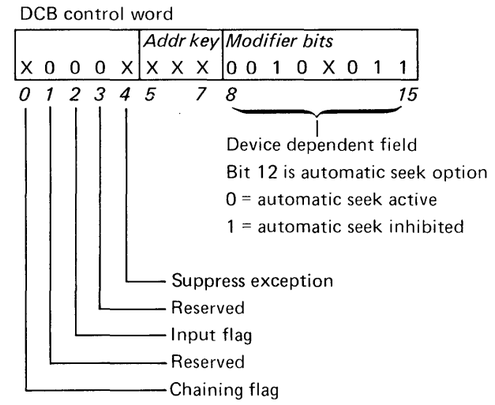
The error recovery procedure for this operation is determined by the setting of control word bit 4.

When this SE bit equals 1, the attachment retries the operation four times before posting a permanent error. When the operation is finished, the status is stored at the location indicated by the residual status block address in the DCB, if there was no permanent error. After a permanent error, the status is available to a Start Cycle Steal Status command. If the write data repeat with read verify operation is used, the verify operation is retried eight times for each time the operation is write retried.

If the SE bit equals 0, the attachment does not retry the operation and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports the auto seek option (bit 12) in the control word of the DCB. If bit 12 equals 0, the search argument is checked against the current location, and a seek operation is initiated as required. When bit 12 equals 1, the attachment returns a no-record-found error, and no data transfer takes place if the correct cylinder and head are not selected.

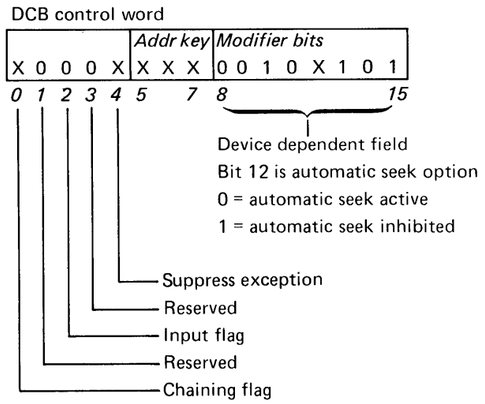
Write Data Repeat with Read Verify



This operation is the same as write data repeat except that data is automatically read back and CRC checked before the operation is completed.

It is recommended that the write data repeat with read verify operation be used instead of separate operations so that automatic error recovery procedures can retry both the write and verify operations if the verify operation fails.

Write Sector ID with Read Verify



This operation writes four bytes of sector ID information onto a specified sector. The data pointed to by the data address field in the DCB is written into the sector ID field specified by the physical sector number byte in the DCB. A write ID with read verify operation causes the written data to be automatically read back and CRC checked before the operation is completed.

The sector ID field is as follows:

Flag byte								Sector number							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
F	F	F	F	F	F	F	F	0	S	S	S	S	S	S	0

Head number								Cylinder number							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	H	H	H	H	H	0	C	C	C	C	C	C	C	C	C

The physical sector number byte in the DCB is used as the starting location to write on the disk. A 0 in this byte specifies the first sector after index, a 1 specifies the second sector after index, and so forth to the end of the track.

The byte count is specified as a multiple of 4 up to a maximum of one full track (132 bytes). Head switching does not take place with this operation. All transfers crossing "index" will continue on the same track until logical end of track.

During initialize operations, a read ID must be executed before write ID to preserve the integrity of the flag byte bits, set at factory for defective sectors. A previously flagged defective sector should not be rewritten as valid. It might pass as valid the second time but could become defective again resulting in loss of user data.

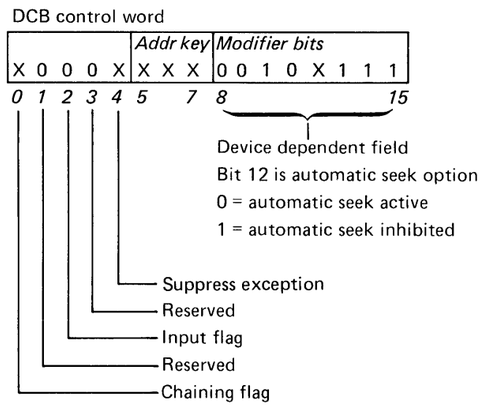
When writting sector IDs for fixed heads, the cylinder number must be written as hex 1FF.

The error recovery procedure for this operation operates in accordance with the countrol word bit 4 (SE setting). When the SE bit equals 1, the attachment retries the operation four times before posting a permanent error. When the operation is finished, the status is stored at the location indicated by the residual status block address in the DCB, unless a permanent error occurs, in which case, the status is available to a Start Cycle Steal Status command.

If the SE bit equals 0, the attachment does not retry the operation and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

This operation does not support the auto seek option (bit 12) in the control word of the DCB. If bit 12 equals 0, a DCB specification check occurs.

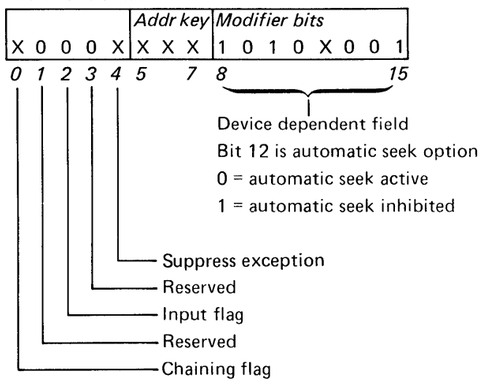
Write Sector ID Extended with Read Verify



This operation is similar to the write sector ID with read verify operation with one exception. The sector ID information is written onto the disk 64 bytes past the normal location to compensate for a surface defect in the normal location. Because of this displacement, the data area of the sector is destroyed. This operation, therefore, is only to be used where a disk defect prevents writing the ID in the normal position and is only used for flagging a defective sector. The defective sector flag bit must always be active when using this operation. All options available to a write sector ID with ready verify operation are also available to a write sector ID extended with read verify operation.

Note: If multiple sector IDs are specified in the byte count (greater than 4), all IDs will be written skewed.

Write Data Security with Read Verify



This operation can be used to overwrite existing data with 0's. The byte count specifies the number of bytes to be written as 0's. This byte count must be even or a DCB specification check is returned. The data address given in the DCB is ignored.

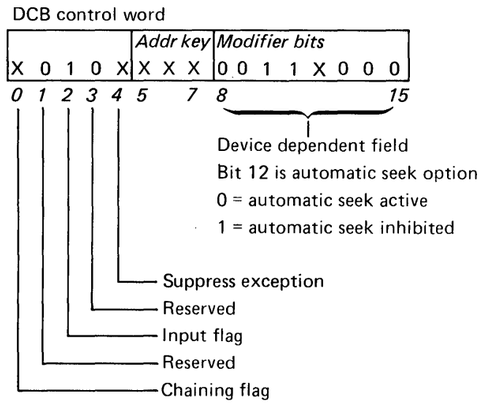
Automatic head and cylinder switching takes place when, at logical end of track, further data transfer is required. Up to 65,536 bytes (256 records) can be written without regard to track or cylinder boundaries and without intermediate interrupts. If the byte count goes to 0 before the end of a complete 256 byte record, the attachment "pads" the remainder of that record with 0's. Therefore, in effect, only full sections are padded by this operation.

The error recovery procedure for this operation is determined by the setting of control word bit 4. When the SE bit equals 1, the attachment retries the operation four times before posting a permanent error. When the operation is finished, the status is stored at the location indicated by the residual status block address in the DCB, unless a permanent error occurs, in which case, the status is available to a Start Cycle Steal Status command.

If the SE bit equals 0, the attachment does not retry the operation and any errors will result in the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports the auto seek option (bit 12) in the control word of the DCB. If bit 12 equals 0, the search argument is checked against the current location and a seek operation is initiated, as required. When bit 12 equals 1, the attachment returns a no-record-found error, and no data transfer takes place if the correct cylinder and head are not selected.

Scan Equal



This operation causes a data comparison search to be conducted between a scan argument record and data records contained on a given disk unit. A single 256-byte record, the scan argument record, is transferred from storage to the disk unit. The starting addresses of the scan argument record are specified in DCB word 7, data address. The DCB record number, head, and cylinder specify the starting point on the disk unit for the search. The number of data records to be searched is defined by the DCB scan repeat count field. If an equal condition is found, 258 bytes of data will be transferred to storage, otherwise, no transfer of data to storage will occur. The byte count for all scan operations in the DCB must be 258 or an exception interrupt occurs with DCB specification check set in the ISB. The interrupt information byte (IIB) and the residual status block both contain status bits indicating whether or not an equal condition was found.

The scan argument record (256 bytes) can contain multiple scan arguments. The delimiter between each scan argument contained within the entire scan argument record is hex FF. The delimiter byte itself (hex FF) causes a comparison of immediately previous data. When an hex FF is encountered, the equal condition is tested. If valid, the data comparison is terminated and the rest of the disk unit data record is placed into the scan argument record in the attachment. The total scan data record, the modified scan argument record, is now returned to storage at the original location specified. The length of the scan data record returned is 258 bytes. The two additional bytes are required for turnaround time. Hence, 258 bytes of storage should be allocated to receive the scan data record, if the equal condition is found. Note that only the first 256 bytes of the original scan argument record are used in the search operation.

If a not equal condition occurs after the hex FF byte delimiter, the search continues. If the last byte of the last scan argument occupies the 256th byte of the scan argument record, it is assumed that there is a delimiter byte hex FF in byte position 257. If the equal condition is found on the 256th byte, the original scan argument record is returned to storage.

The input flag, bit 2 of the DCB control word, must equal 1 for this scan operation.

The error recovery procedure for this operation is determined by the setting of control word bit 4. If the SE bit equals 1, the attachment retries the operation eight times before posting a permanent error. When the operation is finished, the status is stored at the location indicated by the residual status block address in the DCB, unless a permanent error occurs, in which case, the status is available to a Start Cycle Steal Status command.

If the SE bit equals 0, the attachment does not retry the operation and any errors result in the end of the operation with status available to a Start Cycle Steal Status command.

This operation supports the auto seek option (bit 12) in the control word of the DCB. If bit 12 equals 0, the attachment checks the search argument against the current location and initiates a seek operation as required. If bit 12 equals 1, the attachment returns a no-record-found error, and no data transfer takes place if the correct cylinder and head are not selected.

The scan operation stops with the first scan hit, permanent error, or when the scan/repeat count is 0.

Scanning starts with the data record pointed to by the search argument in the DCB. The number of records to be scanned is determined by the scan/repeat count byte in the DCB. A count of 0 causes one record to be scanned, a count of 1 for two records, and so forth to 256 records maximum. Automatic head and cylinder switching is supported.

Note: If an error occurs that prevents reading data (for example, no-record-found), the residual address points to the last byte of the DCB and the residual count is 258. This indicates that the search argument record was read from processor storage into the disk unit, and no data was transferred to processor storage.

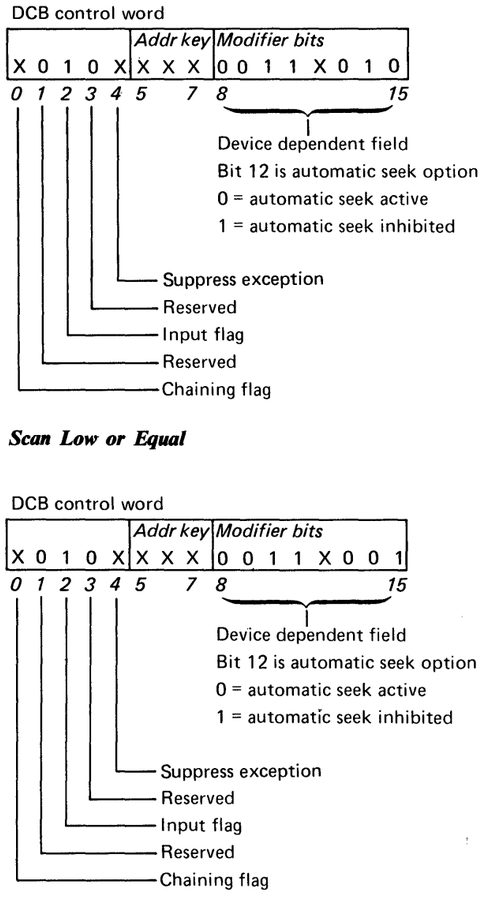
The same residual address and residual byte count indication is returned if a 'scan not equal' condition is encountered.

		Scan argument record read from storage		Data record on the disk		Scan data record read into storage	
Word	0	S.A.	S.A.	FD0	FD1	S.A.	S.A.
	1	S.A.	S.A.	FD2	FD3	S.A.	S.A.
	2	S.A.	S.A.	FD4	FD5	S.A.	S.A.
	3	S.A.	S.A.	FD6	FD7	S.A.	S.A.
	4	X'FF'	X'FF'*	FD8	FD9	'FF'	'FF'
	5	X'FF'	X'FF'*	FD10	FD11	'FF'	'FF'
	6	S.A.	S.A.	FD12	FD13	S.A.	S.A.
	7	S.A.	S.A.	FD14	FD15	S.A.	S.A.
	8	X'FF'	YY**	FD16	FD17	X'FF'	YY***
	9	XX	XX	FD18	FD19	FD16	FD17
	10	XX	XX	FD20	FD21	FD18	FD19
	•	•	•	•	•	•	•
	•	•	•	•	•	•	•
	127	XX	XX	FD254	FD255	FD252	FD253
	128	XX	XX			FD254	FD255

*'FF' causes Scan Equal to be tested.
**'FF' causes Scan Equal to be tested again.
***These two bytes allow storage address turnaround.

S.A. = Scan argument (for data comparison).
FD = Disk unit data (byte) N as read from disk unit.
XX = Not used
YY = This byte does not get altered in the transfer. It's contents are neither examined or used by the attachment.

Scan High or Equal



Scan Low or Equal

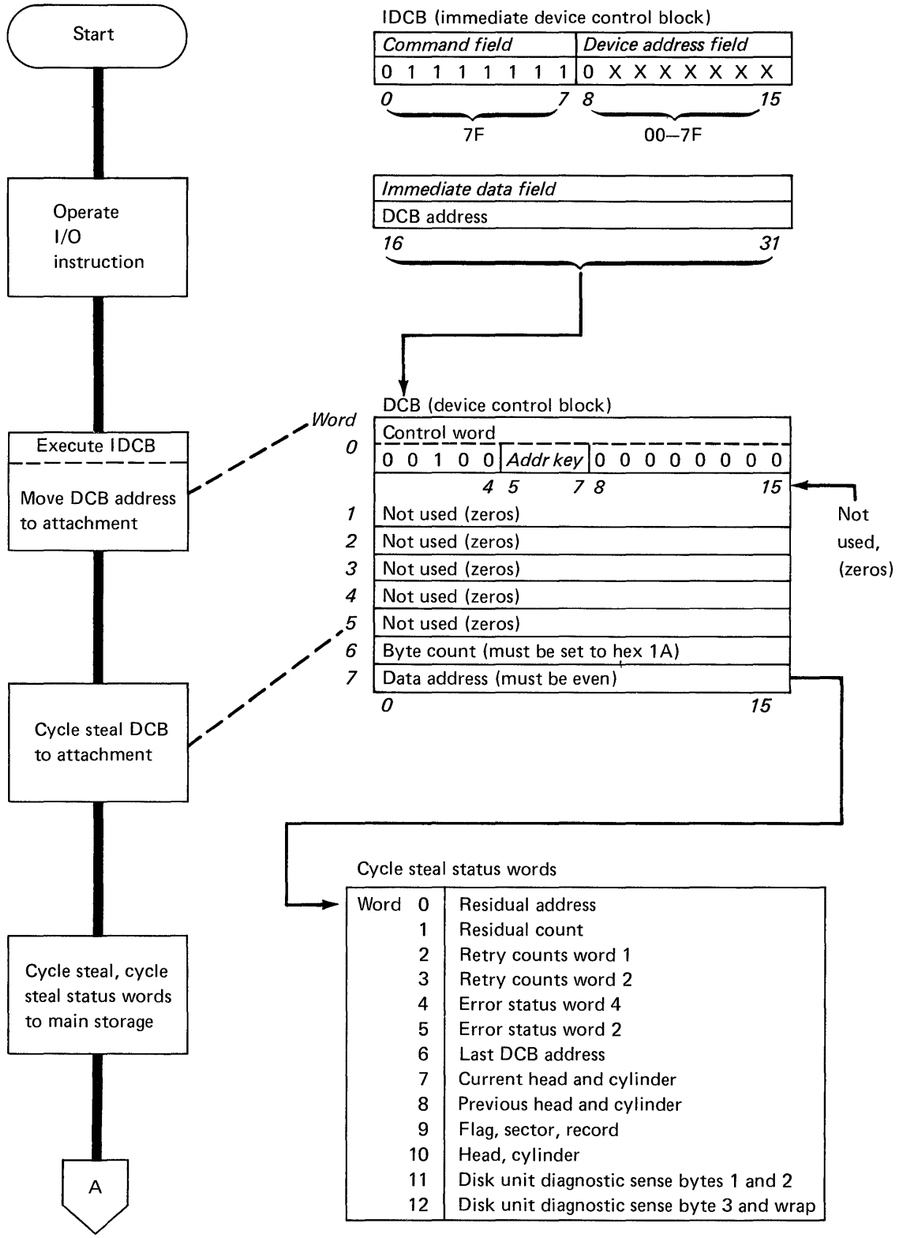
These operations operate in the same sequence as the scan equal except for the data compare. The following table summarizes the compare operations:

Scan equal	Scan argument	= Disk unit data
Scan high or equal	Scan argument	<=Disk unit data
Scan low or equal	Scan argument	>=Disk unit data

'Scan equal' and 'scan not equal' bits are used together to define the status of the scan commands. These status indicators are posted in both the residual status block and the cycle-steal status block. Note carefully the interpretation of the scan equal and scan not equal bits. The scan not equal bit, when equal to 1, indicates that the requested scan condition was not met. The scan equal bit, when equal to 1, indicates the *equality* condition only. Thus, for example, the scan low or equal condition could have been met (scan not equal to 0). Now the scan equal bit = 0, indicates that the disk unit data was less than the scan argument.

Operation	Data compare	Scan not equal	Scan equal
Scan equal	Equal	0	1
	Not equal	1	0
Scan low or equal	Equal	0	1
	Low	0	0
	High	1	0
Scan high or equal	Equal	0	1
	Low	1	0
	High	0	0

Start Cycle Steal Status



Start Cycle Steal Status

The Start Cycle Steal Status command causes 13 words of status information to be transferred, in cycle-steal mode, from the 4963 to processor storage. The information is used to determine the status of an operation that did not execute correctly. The processor storage data address is specified in word 7 of the applicable DCB. This command causes the 4963 to present an interrupt request when execution is complete.

Status Word 0—Residual Address

This address is the processor storage location of the last attempted cycle-steal transfer associated with a Start command. This address might be a DCB address or a data address. If the last transfer attempted was a word transfer, the residual address points to the odd byte of the word. If an error occurs during a start cycle steal status operation, this address is not altered. A device reset, system reset, or a Halt I/O command might cause the residual address to be indeterminate. Only a power-on reset resets the residual address to 0.

Status Word 1—Residual Count

This word contains the residual byte count of data requested for the last DCB operation. The count reflects the number of bytes of data not transferred by the last operation that can be retried, or the last individual operation if more can be retried.

Status Word 2—Retry Count Word 1

This word contains temporary-error retry counts. The error conditions and their respective bit fields are as follows:

Bits	
0–3	CRC check
4–7	Write echo check
8–11	Missing sector pulse
12	Data unsafe
13	Disk unit not ready
14–15	Spare

Status Word 3—Retry Counts Word 2

This word is an extension of the temporary-error retry counts. The error conditions and their respective bit fields are:

Bits	
0–3	No record found
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check
8	Disk unit interface parity check
9–11	Reserved
12–15	Write error

Status Word 4—Error Status Word 1

The following bit format and respective error conditions are described with the bits equal to 1, unless otherwise specified.

Bit 0 Premanent error. A permanent error has occurred. When the suppress exception bit equals 0, any error causes bit 0 to be set to 1.

Bit 1 Attachment detected interface parity check. A parity error has been detected.

Bit 2 Attachment time-out. An operation has taken too long.

Bit 3 Alternate sector processed. A data record has been sought that has been reassigned to an alternate sector and automatic alternate sector processing is being used.

Bit 4 Temporary error retry. A temporary error condition has occurred, and the operation that revealed it has been retried and cleared before the end of the retry count.

Bits 5–7 Disk unit configuration. This three-bit field reflects the disk unit capacity.

Bits 5, 6, 7	Specifies
000	Reserved
001	Reserved
010	Reserved
011	Model 64 A&B (no fixed heads)
100	Disk unit not attached
101	Reserved
110	Reserved
111	Model 58 A&B (eight fixed heads)

Bit 8 Scan not equal. A request for a scan operation has not been met.

Bit 9 Scan equal. An equal condition has occurred on a scan operation.

Bit 10 Attachment equipment check. A circuit error has been detected by the attachment.

Bit 11 Write error. A permanent CRC check has occurred on a write data with read verify operation. Setting the suppress exception (SE) bit to 1 permits the write operation to be retried up to four times before the write error is posted.

Bit 12 Cycle steal status error. An error has occurred while obtaining status from the disk unit during the execution of a start cycle steal status operation.

Bit 13 End of disk. An attempt has been made to use cylinder 359 for other than write diagnostic purposes, or to select a nonexistent fixed head.

Bit 14 Attachment load time-out. This bit is set to 1 if a cable circuit sequence has timed out.

Bit 15 Disk unit interface error. Any of the following conditions have been detected in the disk unit.

- Cable open
- Missing control sample
- Multiplex bus parity check
- Disk unit failed to reset interrupt

Status Word 5—Error Status Word 2

The following bit format and respective error conditions are described with the bits set to 1, unless otherwise specified.

Bit 0 Cyclic redundancy check. A permanent cyclic redundancy check has occurred during a sector ID or data record read operation. If the SE bit equals 1, the attachment retries the operation eight times posting a permanent error. A cyclic redundancy check, in an ID field, during an ID search operation is posted as a no record found error, not as a CRC check.

Bit 1 Disk unit parity check. An internal parity check in the disk unit controls has been detected. This check cannot be retried by the disk unit controls.

Bit 2 Disk unit detected interface parity check. A parity error has been detected on the data bus or tag bus on the cable between the disk controls and the attachment feature. This check cannot be retried by the disk controls.

Bit 3 Write gate return check. Write gate is active in the disk controls but not in the disk unit. If the SE bit equals 1, the attachment retries the operation four times posting a permanent error.

Bit 4 No record found. A sector is addressed, but cannot be found within one revolution. This error occurs if the suppress exception bit equals 0, or if the retry count is 0.

Bit 5 Invalid operation parameter. The disk controller has detected an invalid operation parameter. The conditions that cause this bit to be set to 1 are:

- Invalid operation modifier byte
- Byte count greater than hex 84 (132 decimal) for write sector ID and read sector ID operations
- Bit 0 or 6 in DCB word 2 does not equal 0
- Record number is greater than 63 for read/write scan commands (DCB word 1)
- Sector number is greater than 32 for read ID, write ID, and equal diagnostic commands (DCB word 1)

Bit 6 Missing sector pulse. The dedicated cable for this disk unit has an active "missing sector pulse" line. If the SE bit equals 1, the attachment retries the operation eight times before posting a permanent error.

Bit 7 Disk unit time-out. A disk operation has not been completed in a specified time. It forces an exception interrupt.

Bit 8 Fixed head not selected. Movable head operations are attempted or executed.

Bit 9 Brake applied. An error has occurred that caused the disk brake to be applied while the disk is still being driven.

Bit 10 Track unavailable. An access request has specified a nonexistent cylinder.

Bit 11 Disk unit tag code error. The disk unit has encountered an illegal tag code.

Bit 12 Data unsafe. This is caused by any of the following conditions in the disk unit:

- Write or read mode and multiple module select error
- Write and sector servo unsafe
- Write and no write transitions
- Not write and write current detected
- Write and not on track and moving head selected
- Write and read
- Write and head short detected
- Write and movable head selected during sector pulse
- Write and not ready

Bit 13 Seek incomplete. Access motion is in progress.

Bit 14 Home. A successful power-on sequence or a recalibrate operation to the disk unit has been completed.

Bit 15 Not ready. The disk unit has not come to a complete ready condition.

Status Word 6—Last DCB Address

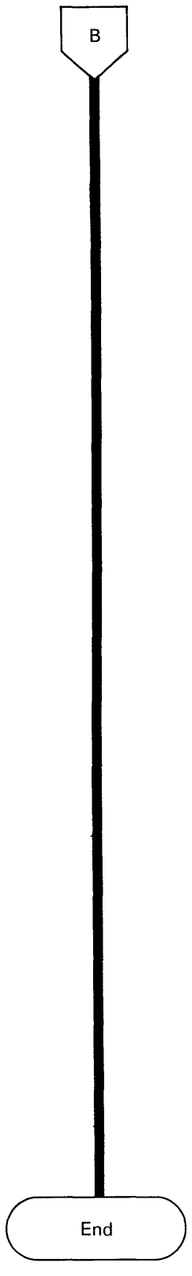
This word contains the starting address of the last DCB used by the attachment.

Status Word 7—Current Head/Cylinder

This word contains the head and cylinder address of the current physical access location on the disk unit. A system reset will set this word to hex 8000.

Status Word 8—Previous Head/Cylinder

This word contains the head and cylinder address of the previous location of the access mechanism. The first seek performed, following a system reset, sets this word to hex 8000. This invalid head/cylinder number is used by the disk unit controls as a flag to indicate that another seek for the next auto-seek operation is required.



Status Word 9—Flag/Sector/Record

This word is used, with status word 10, to identify the last record on the disk unit that access was completed or attempted during the last DCB operation.

Status Word 10—Head/Cylinder

This word is used, with status word 9, to identify the last record number on the disk unit that access to was completed or attempted during the last DCB operation. This number represents the last record access attempted during the last retry of the operation, if a permanent error occurs and the SE bit equals 1. Therefore, it does not necessarily represent the highest record number attempted to be accessed during all previous attempts of the operation.

Status Word 11—Disk Unit Diagnostic Sense Byte 1&2

Diagnostic sense byte 1 occupies the high-order byte, and diagnostic sense byte 2 occupies the low-order byte.

Diagnostic sense byte 1

Bit 0 On track. This bit indicates the ability of the dedicated servo to maintain the position of the data cylinder within ±10% of track center.

Bit 1 Linear region normal. This bit sets the linear boundaries of the dedicated servo circuits. This bit is set to 1 for even tracks, and 0 for odd tracks.

Bit 2 Not index sector pulses. This bit is set to 0 if either an "INDEX" or a "SECTOR" pulse is detected.

Bit 3 Out direction. This bit indicates the seek direction of the actuator.

Bit 4 Not drive out. Logical level indication of voice coil driver out.

Bit 5 Not drive in. Logical level indication of voice coil driver in.

Bit 6 Tag parity error. An error condition between the disk unit controls and the disk unit has been detected. This sense bit separates parity errors from tag parity errors.

Bit 7 Velocity profile error. This bit is set on by the disk unit circuits if an error is detected in the circuits that determine the velocity of the actuator.

Diagnostic sense byte 2

Bit 0 Behind home. This bit indicates the position of the heads. When set to 1, the heads are over the cylinder located between the landing zone and track 0.

Bit 1 Missing clocks divided by 2. This bit set to 1 indicates missing clock pulses used for sector and index generation. A divider circuit is provided for maintenance purposes to ensure detection of pulses during worst-case sampling periods.

Bit 2 Not missing clock error latch. This bit set to 1 indicates that dedicated servo clock pulses are detected.

Bit 3 Coil current low. This bit set to 1 indicates the coil current is low. This is a maintenance dedicated circuit.

Bit 4 Missing servo signal. This bit set to 1 indicates the loss of dedicated servo signal. A loss of the servo signal is indicated when more than six consecutive pulses are expected but not detected. This is a maintenance dedicated circuit.

Bit 5 Off data track. This bit set to 1 indicates the ability of the sector servo to maintain the position of the data cylinder within ±10% center of track.

Bit 6 Not missing position error signal. This bit set to 0 indicates the loss of one or more position-error signals in the servo sector circuits and the loss of automatic gain control. This is a maintenance dedicated circuit.

Bit 7 Counter 5 in sync. This bit set to 1 indicates that the phased-lock oscillator is in sync with the clock.

Status Word 12—Disk Unit Diagnostic Sense Byte 3 and Wrap Byte

Diagnostic byte 3 occupies the high-order byte and diagnostic wrap byte occupies the low-order byte.

Bit 0 Not shift. This bit set to 0 indicates a set seek operation is set.

Bit 1 Not off track and write. This bit set to 0 indicates an 'off track' condition during a write operation, an unsafe condition.

Bit 2 Not outside automatic gain control window. This bit set to 0 indicates the logic level of the sector servo signals in the servo circuits.

Bit 3 Not automatic gain control freeze. This bit set to 0 indicates the existance of an automatic gain control freeze to the sector servo circuits.

Bit 4 Demod pulsing. This bit set to 1 indicates a missing dedicated servo demodulator pulse. This is a maintenance dedicated circuit.

Bit 5 Not read and write. This bit set to 0 indicates an unsafe condition where read and write are active simultaneously.

Bit 6 Not servo protect and write. This bit set to 0 indicates an unsafe condition where an attempt has been made to write over the sector servo pattern.

Bit 7 Illegal move. This bit set to 1 indicates that the sense line that separates parity errors is active due to a tag value of 000 being posted to the disk unit.

Bits 8–15 Disk unit cylinder number. This is the lower-order byte of the cylinder number from the disk unit if it is preceded by the Sense Disk Unit Diagnostic Wrap command.

Start Cycle Steal Diagnostic

IDCB (immediate device control block)

Command field								*Device address field*							
0	1	1	1	1	1	0	1	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*
7D								00–FF							

Immediate data field
DCB address
16 *31*

The Start Cycle Steal Diagnostic command and the operations performed by the command are described in this section. The format of the DCB for this command is as follows:

DCB (device control block)

Word																
0	*Control word*															
	0	0	X	0	0	*Addr key*		0	0	0	0	0	0	0	0	
					4	*5*	*7*	*8*							*15*	
1	Not used (zeros)															
2	Not used (zeros)															
3	Not used (zeros)															
4	Not used (zeros)															
5	Not used (zeros)															
6	Byte count															
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
7	Data address															
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	0															*15*

Attachment Diagnostic Write Test

DCB control word

					Addr key			*Modifier bits*							
X	0	0	0	X	X	X	X	0	0	0	1	0	1	0	0
0	*1*	*2*	*3*	*4*	*5*		*7*	*8*							*15*

14

- *4* — Suppress exception
- *3* — Reserved
- *2* — Input flag
- *1* — Reserved
- *0* — Chaining flag

This diagnostic operation exercises the data bus of the attachment feature as in a write operation. During the execution of this operation, the attachment feature isolates itself electrically from the disk unit controls. The attachment feature cycle steals words from processor storage beginning at the data address location specified in the DCB and continues until the specified byte count is 0. Only even byte counts are accepted. The data is checked for parity errors only. If a parity error occurs for any of the words transferred, the attachment feature posts an exception interrupt. The error is noted as an equipment check in cycle steal status word 4. A cycle-steal error on the Series/1 I/O attachment is reported in bits 4–7 of the ISB. The byte count is not DCB specification checked.

Attachment Write Diagnostic Patch

DCB control word

					Addr key			*Modifier bits*							
X	0	0	0	X	X	X	X	0	0	0	1	0	0	0	1
0	*1*	*2*	*3*	*4*	*5*		*7*	*8*							*15*

11

- *4* — Suppress exception
- *3* — Reserved
- *2* — Input flag
- *1* — Reserved
- *0* — Chaining flag

This diagnostic operation is used to write the first 512 bytes of the attachment storage with special patch data provided from the system. Special tests are provided throughout the read-only storage to check for the presence of patch flags in storage. These flags can be used to patch the microcode and provide the temporary fixes until a new read-only storage diagnostic is released. The byte count must be 512. The byte count is not DCB specification checked.

Write Disk Unit Control Block Diagnostic

DCB control word

					Addr key			*Modifier bits*							
X	0	0	0	X	X	X	X	0	0	1	0	0	0	0	0
0	*1*	*2*	*3*	*4*	*5*		*7*	*8*							*15*

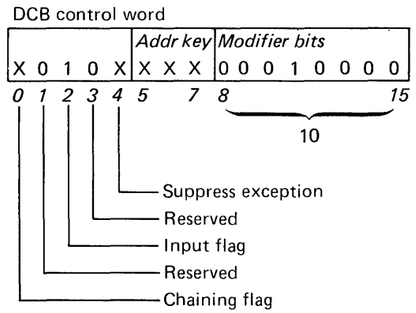
20

- *4* — Suppress exception
- *3* — Reserved
- *2* — Input flag
- *1* — Reserved
- *0* — Chaining flag

This diagnostic operation is used to write the disk unit control block of the selected disk unit. Up to 16 words can be written, depending on the byte count in the DCB. The byte count can be any number between 2 and 32. The disk unit control block is written in ascending order, starting with word 0.

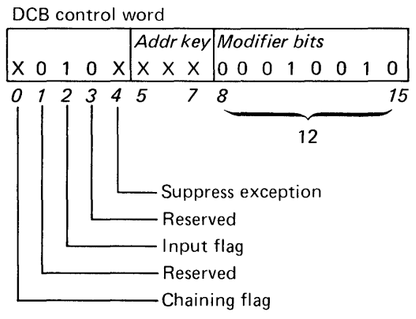
Note: If a byte count greater than 32 is specified, the selected disk unit control block wraps continuously until the byte count is 0. The byte count is not DCB specification checked.

Attachment Read Diagnostic Patch



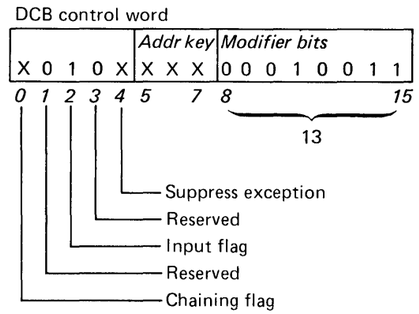
This diagnostic operation is used to read the first 512 bytes of the attachment storage into the system. The purpose is to check for the presence of old patch information if a new patch is to be added, or to verify that a patch was written correctly. The byte count must be 512. The byte count is not DCB specification checked.

Attachment Read Only Storage Diagnostic



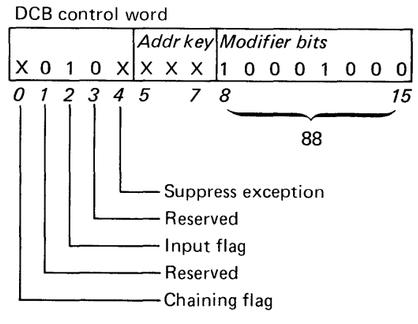
This operation causes the attachment feature to generate a read-only storage check-sum word and to cycle steal two words into storage. The word stored at the location indicated by the data address in the DCB is the reference check-sum total, and the word stored at the data address plus 2 contains the calculated check-sum total. The byte count must be set to 4. The byte count is not DCB specification checked.

Attachment Diagnostic Read Test



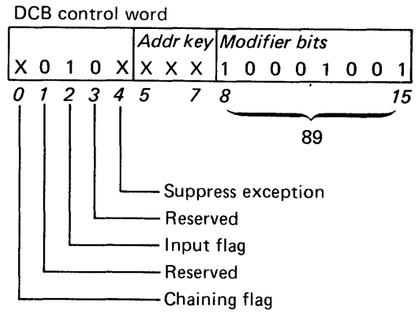
This diagnostic operation exercises the data bus of the attachment feature as in a read operation. The byte count is set to the number of bytes to be stored beginning at the data address location specified in the DCB. The byte count must be even or a DCB specification check is returned. A minimum count of 256 is recommended. Upon completion of the operation the first word in storage at the data address location should contain hex 0000, the second word should be hex 0101, the third word hex 0202, and so on. The attachment feature is electrically isolated from the disk unit controls during this operation.

Read Diagnostic Word 1



This operation cycle steals a word from the attachment data buffer register in the disk unit controls to the location indicated by the data address in the DCB. The byte count must be 2. The byte count is not specification checked.

Read Diagnostic Word 2



This command cycle steals a word from register 2 in the disk unit controls to the location indicated by the data address in the DCB. The byte count must be 2. The bit significance of the word is:

Bit	Meaning
0–5	Not used
6	Reserved
11	Controls cycle complete
12	Diagnostic control
13	Not used
14	Diagnostic control
15	Diagnostic load program store

The byte count is not DCB specification checked.

Condition Codes and Status Information

Condition Codes

A condition code is reported to the processor (1) at the completion of every Operate I/O instruction and (2) upon presentation of a priority interrupt request. The condition code is available in the even, carry, and overflow bit positions of the level status register (LSR) in the processor. For information on the LSR, refer to an appropriate processor description manual listed under "Prerequisite Publications" in the Preface. For commands that do not cause interrupts, the condition code reported after the instruction is executed is the only status information required or available.

Operate I/O Instruction

Condition Code 0—Device Not Attached

This code is reported by the channel when the 4963 is not attached to the Series/1.

Condition Code 1—Busy

This code is reported by the 4963 when it is unable to execute a command because it is in the busy state. The 4963 enters the busy state upon acceptance of a command that requires an interrupt for termination. The 4963 exits the busy state when the attachment accepts the interrupt.

Condition Code 2—Busy After Reset

This code is reported by the 4963 when it is unable to execute a command because of a reset and the 4963 has not had sufficient time to return to the inactive state. There is no interrupt to indicate termination of this condition.

Condition Code 3—Command Reject

This code is reported by the 4963 or the channel when:

- A command is issued that is outside the 4963 command set.
- The 4963 is in an improper state to execute the command.
- The IDCB contains an incorrect parameter, such as an odd-byte DCB address, or an incorrect function/modifier combination.

When the 4963 reports command reject, it does not fetch the DCB.

Condition Code 4—Not Used

Condition Code 5—Interface Data Check

This code is reported by the 4963 or the channel when a parity error is detected on the I/O data bus during a data transfer.

Condition Code 6—Controller Busy

This code is reported by the attachment when the controller is busy and is always followed by a controller end interrupt.

Condition Code 7—Satisfactory

This code is reported by the 4963 when it accepts a command.

Interrupt

Condition Code 0—Controller End

This code is reported by the attachment when controller busy has been previously reported. The code indicates that the 4963 attachment is now free to accept I/O commands. The device address reported with the condition code is always the lowest address of the devices serviced by the system.

Condition Code 1—Not Reported by 4963 Disk Subsystem

Condition Code 2—Exception

This code is reported when an error or exception condition is associated with the priority interrupt. This condition is described in the interrupt status byte (ISB) and further described in the 26 bytes of status information contained in the cycle steal status block.

Condition Code 3—Device End

This code is reported when no error exceptions or attention conditions occur during the I/O operation and a normal termination of the operation has occurred.

Condition Code 4—Attention

This code is reported when the 4963 becomes ready after being in the not ready state. Along with the interrupt condition code, the attachment also transfers an interrupt ID word which provides additional information on interrupting conditions.

Condition Code 5—Not Reported by 4963 Disk Subsystem

Condition Code 6—Attention and Exception

This code is reported when attention and exception are both present.

Condition Code 7—Attention and Device End

This code is reported when attention and device end are both present.

Status

Status information is transferred from the 4963 to the processor as the result of:

- A Start Cycle Steal Status command (see "Start Cycle Steal Status" in this chapter)
- Storing a residual status block (see "DCB Word 0—Control Word" in this chapter)
- A priority interrupt

The interrupt status information is explained under "Interrupt Identification Word" and "Interrupt Status Byte".

Interrupt Identification Word

Accepting an I/O interrupt causes the attachment to present an interrupt ID word to the processor. The interrupt ID word consists of an interrupt information byte (IIB) and a 4963 disk unit device address. This word is stored in processor register 7. The format is as follows:

Interrupt ID word

IIB (ISB)	*Device address*
X X X X X X X X	0 X X X X X X X
0 *7*	*8* *15*

For controller-end condition and attention interrupts, the IIB is always 0's. For device end and attention/device end interrupts, the IIB can have the following bit meanings:

Bit 0 Permissive device end. This bit set to 1 indicates that information about temporary errors is available in the residual status block.

Bit 1 Scan not equal. This bit set to 1 indicates that the requested scan condition was not met.

Bit 2 Scan equal. This bit set to 1 indicates that the requested scan condition was met.

Bits 3–7 Reserved. All 0's at interrupt time.

Note: The condition of IIB bits 1 and 2 pertains to the last executed DCB only. Information concerning other DCBs executed can be derived through a residual status block, providing the SE bit of the DCB was equal to 1.

For exception and attention/exception interrupts, the IIB has a special format called the interrupt status byte (ISB).

Interrupt Status Byte

The ISB stores accumulated status information. The format of the ISB is:

Bit	Meaning
0	Device-dependent status available
1	Delayed command reject
2	Incorrect record length
3	DCB specification check
4	Storage data check
5	Invalid storage address
6	Protect check
7	Interface data check

Bit 0 Device-dependent status available. This bit is set to 1 when additional stauts information (residual address and status bits) is available from the 4963. A Start Cycle Steal Stauts command must be issued to get this information.

Bit 1 Delayed command reject. This bit is set to 1 when the 4963 cannot execute a command because of an incorrect parameter in the IDCB.

This bit is only set in the ISB when the 4963 is incapable of recording the condition with condition codes during the I/O instruction execution. The operation in progress is terminated and an interrupt request is generated. Condition code 2 is reported at interrupt time. The residual address is not relevant to error recovery. (See "Cycle Steal Status Word 0".)

Bit 2 This bit is not supported and should always be returned as 0.

Bit 3 DCB specification check. This bit is set to 1 when the 4963 cannot execute the operation because a parameter in the DCB is incorrectly specified to perform the desired operation.

Examples: An odd-byte chaining address, an odd address for start cycle steal status, an invalid command or an incorrect byte count was found in the control word. Condition code 2 is reported at interrupt accept time. The residual address will be the last word of the DCB.

Bit 4 Storage data check. This bit is set to 1 during cycle steal output operations only. It indicates that the storage location accessed during the current output cycle contained incorrect parity. The parity in processor storage is not corrected. The attachment issues the status in the ISB and terminates the operation. Condition code 2 is reported at interrupt accept time.

Bit 5 Invalid storage address. This bit is set to 1 as a result of a cycle-steal I/O operation when the processor storage address, presented by the 4963 for data or DCB access, exceeds the specified address space. The attachment records the status and terminates the operation. Condition code 2 is reported at interrupt accept time.

Bit 6 Protect check. This bit is set to 1 when the 4963 attempts to access a processor storage location without the correct storage protect key. For a more detailed description, refer to an appropriate processor description manual listed under "Prerequisite Publications" in the Preface of this manual. The operation is terminated and condition code 2 is reported at interrupt accept time.

Bit 7 Interface data check. This bit is set to 1 when a parity error is detected on a cycle-steal data transfer. The condition can be detected by the 4963 or by the channel. In either case, the operation is terminated and an interrupt is reported to the processor.

Condition code 2 is presented at interrupt accept time.

Error Recovery Procedures

The following error recovery procedures are initiated by the 4963 subsystem when an error occurs with the suppress exception bit equal to 1. If an error occurs and the suppress exception bit equals 0, the following user program events are recommended:

- A read operation is retried a minimum of eight times prior to posting a permanent read error.
- A write operation is retried a minimum of four times prior to posting a permanent write error. Each write-verify operation is followed by one read operation. A rewrite occurs only if the read operations fail.
- Unresolved errors result in termination of the operation. The program should issue a message and an error log to the operator at termination.
- The information placed in the flag byte (bits 2 through 7) during the factory's alternate sector assignment procedures should be rewritten during all write ID operations.

The user program must implement the required error recovery procedures if all DCBs use the SE bit option. The attachment handles all error recovery procedure requirements under the SE bit option, except those listed below under "Actions". The check conditions can be tested in the ISB, and words 4 and 5 of the cycle steal status block.

Actions

The following processor actions allow for the entire error recovery procedure to be repeated once prior to posting a permanent error, requiring operator intervention. It is intended that the user retry the error recovery procedures to distinguish a permanent error from a transient condition.

1. Initiate a device reset operation.
2. Initiate a calibrate operation.
3. Reseek to the original track.
4. Retry the original operation. If still unsuccessful, issue an operator message and exit the error recovery procedures.
5. Ensure that the device is powered on, and is prepared to allow interrupts, and to wait for an attention interrupt. An operator message can be used here. Exit the error recovery procedures.

Note: If end of disk is expected, due to the manner in which the user handles multiple sector read or write operations, then the error recovery procedure is to calculate the next disk address, the starting record search argument, and the proper byte count to the operation. If end of disk is not normally expected, there might be an error in the user porgram or in the hardware. Therefore, initiate a device reset operation.

Resets

Several methods of resetting controls and registers are available.

Power-on Reset

Resets the residual address register, the prepare register, the last sector register, the data register (16 bits), and the cycle-steal request.

System Reset

Resets the prepare register, the last sector register, and the cycle-steal request.

Initial Program Load (IPL)

Resets the prepare register, the last sector register, and the cycle-steal request.

Halt I/O Command

Resets the last sector register and the cycle-steal request.

Device Reset Command

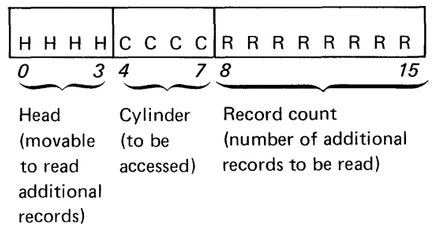
Resets the last sector register.

Initial Program Load (IPL)

The 4963 attachment supports IPL from the primary and secondary disk units. Disk 0 and disk 1 can be designated as primary or secondary, interchangeably, and designation is done by the user, through hardware jumpers.

At IPL, when the designated disk unit is ready, and the IPL signal is received from the Series/1 I/O channel, the attachment initiates a recalibrate operation, and the disk unit positions itself to cylinder 0, head number 1. After recalibration, the attachment issues a read data operation for logical record 0, byte count 256, and a storage starting address of 0. If an error occurs during the read operation, the attachment retries both the recalibrate and the read operations up to eight times before the system stops with the LOAD indicator on.

The attachment can transfer up to 256 data records into processor storage. After the first data record is transferred, the attachment reads the last word transferred to determine if further records are to be transferred, transparent to the user, and where they are to be stored. Specifically, the bit configuration of the last word is as follows:



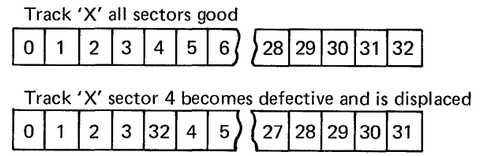
A record count of 0 in the second byte of the last word means no additional records are to be transferred into processor storage.

Disk Defects

When defects are found on the disk, either during manufacture or during use, the sector can be assigned to an alternate sector to make the track and the disk usable again. The first defective sector that occurs on a track is referred to as a *primary* defect. Any subsequent errors that occur on a track are referred to as *secondary* defects.

Primary Defects

There are 33 sectors on each track, but only 32 are addressable for data transfers. When the first defective sector appears on a track, that sector and all following sectors are *displaced*, as shown here:

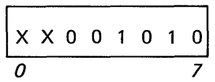


Secondary Defects

If secondary defects occur on a track, the sectors can be assigned to another track's alternate (spare) sector by a sector reassignment program. A recommended method is to have the program begin by testing track 0 (using head 0 for nonfixed-head disk units) or track 1 (using head 1 for fixed-head disk units) of the same cylinder for an unused nondefective alternate sector (sector 32). If the alternate sector has been used, the next track is tested. If all of the alternate sectors on a cylinder have been tested and the program determines that they are in use, a seek to the next higher cylinder is performed (current cylinder number +1). If an unused alternate sector is not found on any of the tracks on this cylinder, a seek to the opposite direction is performed (previous current cylinder number −1). Seeking and testing is continued until an unused nondefective alternate sector is found.

Manufacturer Reassignment of Sectors

If, during manufacturing, a sector is found to contain a primary defect, the sector is reassigned as a displaced sector. The flag field for the defective sector is:



Bit	Meaning
0	Defective data record 2
1	Defective data record 1
2	User-assigned defect
3	Protected data area
4	Sector is displaced
5	Sector is reassigned
6	Manufacturer-assigned defect
7	An assigned alternate sector

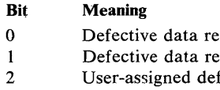
Bits 0 and 1 are set to reflect the location of the defect within the sector. If bits 0 and 1 are both 0's, the defect is located in the ID area. Under these conditions, the ID area of the defective sector is written 64 bytes after the beginning of the original ID area.

The sector number assigned to the address field of the defective sector is hex 20 (decimal 32).

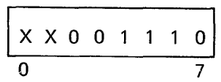
The flag field for all other sectors, after they have been displaced, is:

The address field of a displaced sector contains the same information as if the sector had not been displaced.

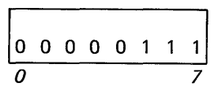
If the alternate sector on the track has been used indicating a secondary defect, the defective sector is assigned to an alternate sector on another track. If the secondary defect occurs between logical sector 0 and the primary defect, the flag field of the defective sector contains:



If the secondary defect occurs between the primary defect and logical sector 31, the flag field of the defective sector contains:



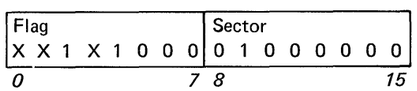
The address field of the secondary defective sector contains the address of an alternate sector on another track to which the defective sector has been assigned. The address field of the alternate sector that receives the reassigned sector is set to the address of the reassigned sector. The flag field of the reassigned sector on the alternate sector contains:



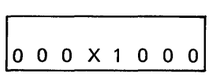
User Reassignment of Sectors

When a sector becomes defective during use, it can be reassigned, as follows:

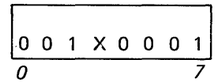
1. Read the ID area of sector 32 for that track.
2. Examine the flag field to determine if sector 32 has been assigned.
3. If sector 32 has not been assigned:
   a. Read the data from the defective sector.
   b. Rewrite the ID area of the defective sector as:



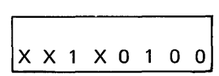
   c. Read the data and ID areas from the next sector.
   d. Write the ID area of the previous sector into the ID area of the sector just read. The flag field is written as:



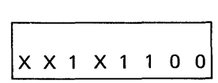
   e. Write the data from the previous sector into the sector that was just reassigned.
   f. Repeat steps c through e until all of the sectors following the defective sector have been displaced.
4. If sector 32 has been displaced indicating that this defect is a secondary defect, the sector is reassigned to an alternate sector, as follows:
   a. Read the data from the defective sector.
   b. Find the closest available nondefective alternate on another track using either the movable head sequence (if the secondary defect occurs on a movable-head track) or the fixed-head sequence (if the secondary defect occurs on a fixed-head track), as follows:
      (1) Movable-head sequence
         (a) Test all the tracks on the same cylinder for an unused nondefective alternate sector beginning with track 0 or track 1.
         (b) If an alternate sector is not found, seek to the next higher cylinder (current cylinder +1) and test all the tracks for an unused alternate sector.
         (c) If an alternate sector is not found, seek to the next lower cylinder (previous current cylinder −1) and test all the tracks for an unused alternate sector.
         (d) If an alternate sector is not found, continue to seek and test each track on a cylinder, increasing and decreasing the cylinder number (+2, −2, +3, −3, etc.) until an unused alternate sector is found. If a cylinder boundary is encountered, such as cylinder 000 or 358 (cylinder 359 is not used), the seek direction will be away from the boundary.
      (2) Fixed-head sequence
         (a) Test the eight fixed-head tracks, beginning with fixed-head 0 for an unused alternate sector.
         (b) If an alternate sector is not found, seek to cylinder 000 and test all the tracks, beginning with movable head 1, for an unused alternate sector.
         (c) If an alternate sector is not found, seek to cylinder 001 and test all the tracks for an unused alternate sector.
         (d) If an alternate sector is not found, continue seeking to the next higher cylinder number and testing the tracks until an unused alternate sector is found.
      (3) If the alternate sector on a track has already been assigned as an alternate sector for another track when the track develops a primary defect, the following sequence is recommended:
         (a) Read the alternate sector's ID area and data (data records 1 and 2).
         (b) Assign the first defective sector on this track as a *primary defect*.
         (c) Seek to the cylinder of previously assigned alternate sector.
         (d) Assign this sector using the *secondary defect* method.
   c. Write the ID area of the defective sector into the ID area of the unassigned alternate sector of the alternate cylinder. The flag field is written as:



   d. Write the ID area of the alternate sector assigned in step c into the ID area of the defective sector. If the second defective sector occurs between logical sector 0 and the first defective sector, write the flag field as:



   If the second defective sector occurs after the first defective sector, write the flag field as:



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International Business Machines Corporation

SY34-0082-0
Printed in U.S.A.