Technical Newsletter

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IBM Series/1
Multi-Function Attachment Feature
Theory Diagrams

This Technical Newsletter provides replacement pages for the subject publication. Pages to be inserted and/or removed are:

3-11, 3-12	3-85, 3-86
3-17, 3-18	3-105, 3-106
3-55, 3-56	3-115 through 3-118
3-59, 3-60	3-123 through 3-126
3-75, 3-76	3-131, 3-132

A technical change to the text or to an illustration is indicated by a vertical line to the left of the change.

Summary of Amendments

This Technical Newsletter corrects several errors in the base publication and should be reviewed in its entirety.

Note. Please file this cover letter at the back of the manual to provide a record of changes.

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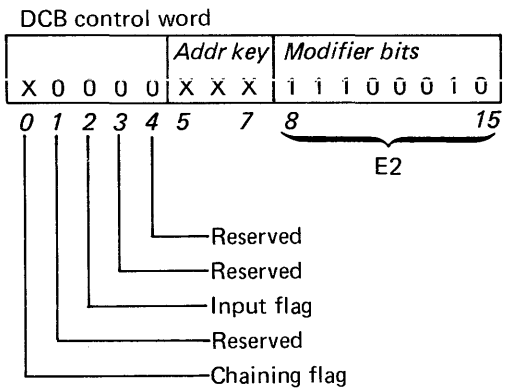
Programming Consideration: The DCB associated with a load attachment storage operation must specify the following:

- Bit 2 of the DCB control word is a 0.
- The byte count in DCB word 6 is within the maximum value of F00 hexadecimal (3,840 decimal) bytes.
- The start address in DCB word 1 is hexadecimal 4080 or above, up to and including 4F7F.

A device-end interrupt follows successful operation. If the boundaries of the attachment storage are exceeded, or if bit 2 of the DCB control word is a 1, a DCB specification check occurs.

For information on the use of the load and initialize attachment-storage operations, and configuring an attachment-storage load, refer to IBM Series/1 Multi-Function Attachment Feature Initialization User's Guide, GA34-0147.

Initialize Attachment



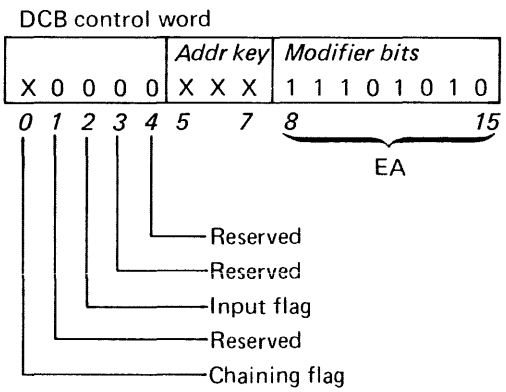
This initialize attachment operation performs an attachment-storage checksum and hardware check; if the results are not correct, an exception interrupt with device dependent status in the interrupt status byte (ISB) is presented.

> **Note:** If the communications indicator panel is connected to the attachment card, the DISPLAY/FUNCTION SELECT switches should be set off (00000) during attachment initialization.

Programming Consideration: Bit 2 of the DCB control word must be 0 and the byte count must be 0. Attachment storage must be loaded with a properly configured attachment-storage load before the attachment can be issued an initialize attachment operation.

For information on the use of the load, read, and initialize attachment-storage operations, and configuring an attachment-storage load, refer to IBM Series/1 Multi-Function Attachment Feature Initialization User's Guide, GA34-0147.

Load Attachment Storage and Initialize



The load attachment storage and initialize operation performs a load attachment storage operation followed by an initialize operation. If a hardware failure occurs during any of the tests or checks that occur during this operation, the attachment does not initialize, and an exception interrupt with device-dependent status in the ISB is presented.

The attachment can exit the initialized state only after one of the following:

- A power-on reset
- Acceptance of a Start Control command that specifies a load attachment storage operation

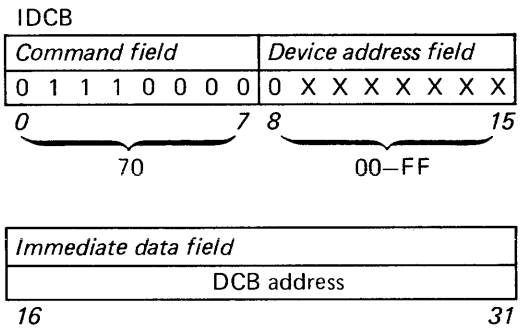
Note: If the communications indicator panel is connected to the attachment card, the DISPLAY/FUNCTION SELECT switches should be set off (00000) during attachment initialization.

COMMANDS

The following commands for the 4975 are described in this section:

- Start
- Start Cycle Steal Status

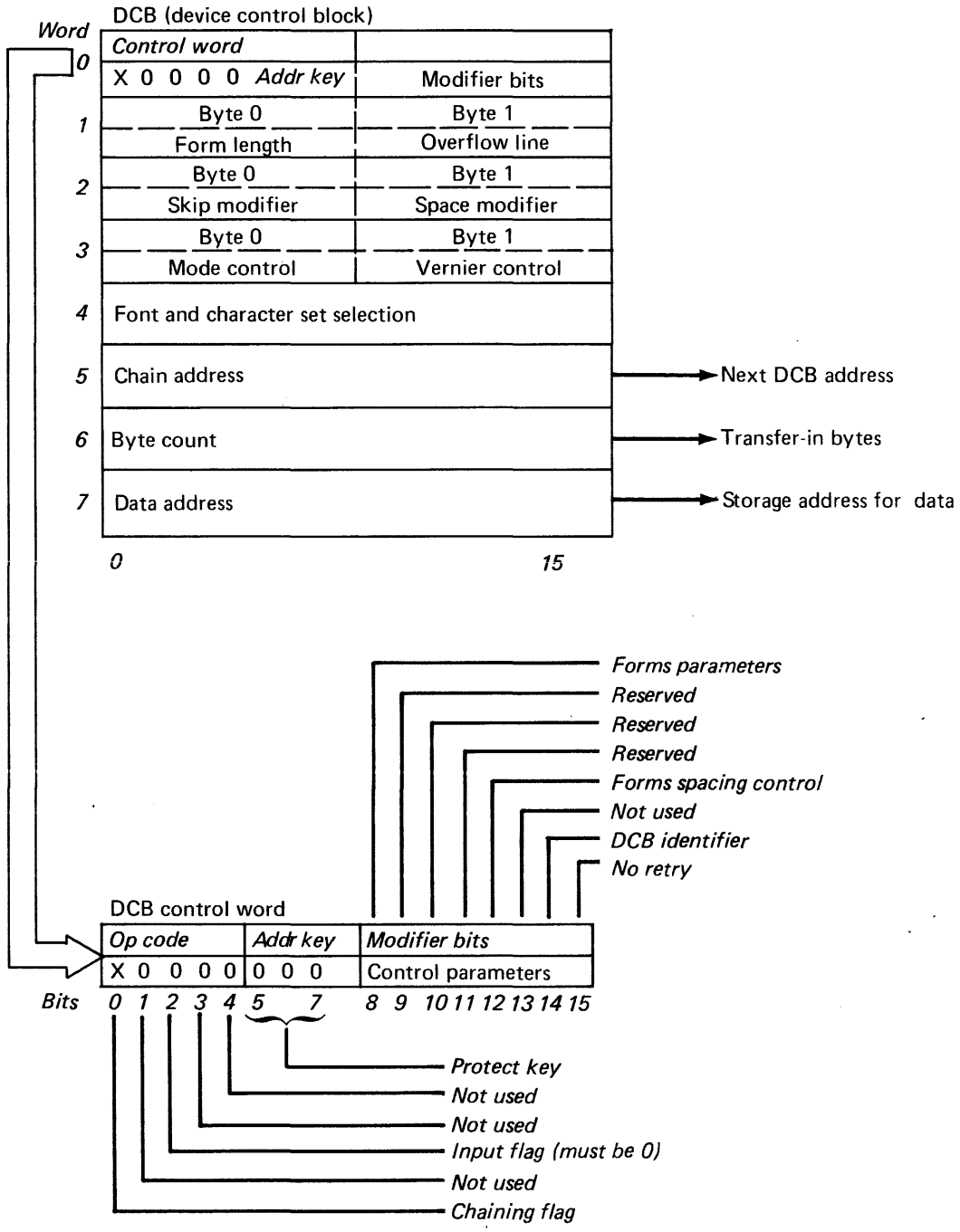
START



The Start command initiates 4975 I/O operations that transfer data from processor storage to the printer in cycle-steal mode. An interrupt request is sent to the processor when the I/O operation ends. The control information and parameters required for a particular 4975 operation must be stored in the DCB associated with that operation.

Programming Consideration: Forms parameters, located in the DCB words for a Start command, must be specified by the program after printer power is switched on.

The eight words in the DCB and their bit configurations are explained in the following text and illustration:



Device control block

BIT 1—PROGRAM-CONTROLLED INTERRUPT (PCI) REQUEST: If this bit is set to 1, the attachment presents a PCI request at the completion of the DCB fetch and places DCB word 3, bits 8 through 15, in the interrupt information byte (IIB). Data transfers associated with the DCB can begin if the PCI request is pending. This bit is recognized only during transmit or receive-type operations. If this bit is set to 1 in any other type of operation, bit 3 of the interrupt status byte (DCB specification check) is set to 1 and the operation terminates with an exception-interrupt request.

Programming Consideration: PCI interrupts must not be used if priority interrupts can be disabled for the duration of the Operate I/O command.

BIT 2—INPUT FLAG This bit indicates to the device the direction that the data is transferred. When this bit is a 1, the device transfers data into processor storage; when this bit is a 0, the data transfer is from processor storage to the device.

BITS 3 AND 4—NOT USED: These bits are not used and must be 0's.

BITS 5-7—CYCLE-STEAL ADDRESS KEY: This is a three-bit key that the device presents to the processor during data transfers to verify that the program has authorization to access processor storage. An invalid address key causes an exception-interrupt request (condition code 2).

BIT 8—SET MODE: If this bit is set to 1, bits 9-15 are used to establish the characteristics of the attachment as described in the set-mode operation. (See "Set Mode," under "DCB Word 0—Control Word" later in this chapter.) If bit 8 is a 0, bits 9-15 specify the operations performed by the Start command.

Programming Consideration: Synchronous operations may be specified only with external clocking on port 0.

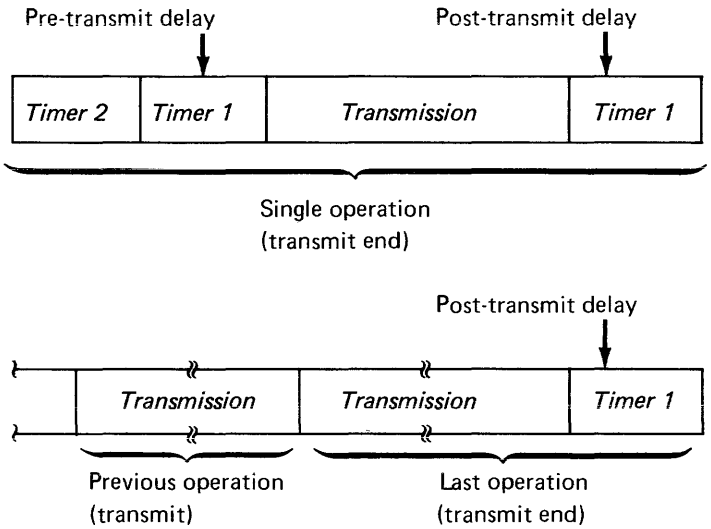
BITS 9-15: Bits 9 through 15 specify the operations performed by the Start command if bit 8 is a 0.

Bits 9	10	11	12	13	14	15	Operation
0	0	0	0	0	0	0	Transmit*
0	0	0	0	0	0	1	Transmit end*
0	0	1	0	0	0	1	Transmit end with pre-receive*
0	0	0	0	0	1	0	Transmit allow break*
0	0	0	0	0	1	1	Transmit end allow break*
0	0	1	0	0	1	1	Transmit end allow break with pre-receive*
0	0	0	0	1	0	0	Receive
0	0	0	0	1	0	1	Receive with time-out
0	0	1	0	1	0	0	Receive with block-check character
0	0	1	0	1	0	1	Receive with time-out and block check character
0	1	0	0	1	0	0	Receive with echoplex
0	1	0	0	1	0	1	Receive time-out and echoplex
0	1	1	0	1	0	0	Receive with echoplex and block-check character
0	1	1	0	1	0	1	Receive with echoplex, time-out, and block-check character
1	0	0	0	1	0	0	Receive transparent
1	0	0	0	1	0	1	Receive transparent with time-out
1	1	0	0	1	0	0	Receive transparent with echoplex
1	1	0	0	1	0	1	Receive transparent with echoplex and time-out
1	1	1	0	1	0	0	Read attachment buffer/ enable extended functions
0	0	0	0	1	1	0	Ring monitor
0	0	0	0	1	1	1	Ring monitor with time-out
0	0	0	1	0	0	0	DTR enable
0	0	0	1	0	0	1	DTR enable with time-out
0	0	0	1	0	1	0	DTR enable with answer-tone
0	0	0	1	0	1	1	DTR enable with answer-tone and time-out
0	0	0	1	1	0	0	DTR disable
0	0	1	1	1	0	1	Set control
0	0	0	1	1	1	0	Program delay
0	0	0	1	1	1	1	Reset
X	X	X	X	X	X	X	Set mode**

* For data characters that contain less than eight bits, the program must right-justify the data in storage before beginning the transmit operation.

** See "Set mode," under "Start" later in this section.

TRANSMIT END: This operation is used to transmit the last block of data in a chain of transmit-type operations or when only one block of data is being transmitted. An example of the use of this operation is shown here:



This operation is the same as the transmit operation, except that the attachment exits transmit mode and starts timer 1 after the last character is transmitted. This delay allows the last character to be sent by the modem (if a modem is used) before the attachment resets 'request to send' (RTS). When timer 1 times out, the attachment resets RTS, if RTS was not set on during the attachment initialization. The timer-1 delay at the end of this operation is called "post-transmit delay." Note that timer 1 is used twice in this operation (pre-transmit and post-transmit delays).

TRANSMIT END WITH PRE-RECEIVE: This operation is the same as a transmit-end operation, except that there is no post-transmit delay. (Pre-receive time starts after the last character has been transmitted.) When pre-receive time starts, incoming data is received and saved in the attachment during the DCB chaining process. This operation must be chained to a receive-type operation. If the chain bit is not set to 1, an exception interrupt occurs with interrupt status byte (ISB) bit 3 (DCB specification check) set to 1. To ensure data integrity during line turnaround, a direct connection or a four-wire interface must be used for a transmit end with pre-receive operation.

TRANSMIT ALLOW BREAK: This operation is the same as a transmit operation, except that it allows the receiving station to stop the transmission. The receiving station may "break" the line by driving its transmit data line to a "space" condition. When in continuous receive, a "break" is defined as one character of 00 and a stop-bit error detected. When the transmission is stopped, the residual address contains the processor storage address that contains the last byte transmitted.

If attention interrupt mode is selected, the transmission stops when an error occurs or a COD character is received. If the attachment detects either condition, it presents an exception-interrupt request (CC2) to the transmit allow break operation with bit 0 of the ISB set to 1 and transmit mode is reset. An attention and exception interrupt request (CC6) is presented with the received character in the IIB. The exception interrupt (CC2) occurs after any received characters are presented by attention interrupts (CC4 or CC6).

Programming Consideration: Interrupt status byte bit 2 (incorrect-length record) may also be set if a COD character is received.

If attention interrupt mode is selected and a COD character is received, the transmission stops. An attention interrupt request (CC4) is presented with the received character in the IIB.

If attention interrupt is selected and a receive error is detected, the transmission stops. An attention and exception interrupt request (CC6) is presented with the received character in the IIB.

Programming Consideration: Continuous receive should not be used with buffered terminals or in synchronous mode when large amounts of data are received because overruns occur. Continuous receive is disabled when a receive error occurs (such as an overrun, parity, or framing error). The program may enable continuous receive and attention interrupt after the receive error occurs by issuing a read attachment buffer/enable extended functions, a receive, or a DCB reset operation. The read attachment buffer/enable extended functions operation clears the attachment buffer of any data that was received after the error.

ATTENTION INTERRUPT: Attention interrupt can be used only in conjunction with continuous receive. When a character is received and a receive-type operation is not in process, received characters are presented to the processor with an attention-interrupt request. The received character is placed into the interrupt information byte (IIB) of the interrupt identification (ID) word.

If an error occurs in this mode, an attention and exception interrupt request (CC6) is presented and the IIB contains the character in error. The type of error is indicated in cycle-steal status. If a transmit allow break operation is not in process and a "break" occurs, an attention interrupt (CC6) is reported with 00 in the IIB. If a parity error is detected on the received characters, the IIB contains 00 unless inhibit 0 insertion is enabled.

If a transmit-allow-break operation is terminated because of an error or break condition (while in this mode), all attention interrupts (CC4) and attention and exception interrupts (CC6) are presented before the ending interrupt for the transmit operation is presented. Residual attention interrupts can occur during command processing in continuous receive mode.

Programming Consideration Continuous receive is disabled when a receive error occurs (such as an overrun, parity, or framing error). The program may enable continuous receive and attention interrupt after the receive error occurs by issuing a read attachment buffer/enable extended functions, a receive, or a DCB reset operation. The read attachment buffer/enable extended functions operation clears the attachment buffer of any data that was received after the error.

CONTINUOUS ECHOPLEX: Continuous echoplex causes the attachment to transmit data that was received from a terminal (or other device) back to the terminal for display. If continuous echoplex is specified in conjunction with continuous receive, any characters received are saved in the attachment and echoed back to the device. If attention interrupt is also specified, any characters presented by way of the attention interrupt are also echoed to the device. Continuous echoplex is intended for situations where the device or terminal requires echoplex but no system processing of the echoed character is required.

Programming Consideration: If continuous receive and attention interrupt are selected with continuous echoplex during a transmit operation, any characters received are not saved and are not echoed to the terminal. Continuous receive is disabled when a receive error occurs (such as an overrun, parity, or framing error). The program may enable continuous receive and attention interrupt after the receive error occurs by issuing a read attachment buffer/enable extended functions, a receive, or a DCB reset operation. The read attachment buffer/enable extended functions operation clears the attachment buffer of any data that was received after the error. Continuous echoplex is disabled when a receive error occurs.

- CC5—Interface data check

  This condition code is reported when a parity error is detected on the processor I/O channel data bus during a data transfer.

- CC6—Controller busy

  This condition code is reported when the attachment feature is "busy" processing a command.

  Reissue the instruction, about every millisecond, until it is accepted. Controller busy does not stay active for more than 2 milliseconds, with an average period of about 150 microseconds.

- CC7—Satisfactory

  This condition code is reported when the attachment feature accepts a command.

INTERRUPT CONDITION CODES

The following condition codes are presented with a priority interrupt request.

- CC0—Not used

  This condition code is not reported by the multi-function attachment.

- CC1—PCI

  This condition code is reported at the completion of a DCB fetch if a program-controlled interrupt (PCI) request is specified (bit 1 set to 1) in the DCB control word. Bits 8–15 of DCB word 3 are placed in the interrupt information byte (IIB).

- CC2—Exception

  This condition code is reported when an error or exception condition is associated with the interrupt request. The condition is described in the interrupt status byte (ISB) or in the cycle steal status words. The status words can be obtained by executing a Start Cycle Steal Status command.

- CC3—Device end

  This condition code is reported when an operation has terminated under normal conditions.

- CC4—Attention

  This condition code is reported when expanded mode is active and continuous receive and attention interrupt are specified. Each received character is placed in the interrupt information byte (IIB) and an attention interrupt is presented.

- CC5—Not used

  This condition code is not reported by the asynchronous/synchronous communications.

- CC6—Attention and exception

  This condition code is reported when expanded mode is active and continuous receive and attention interrupt are specified. This condition code indicates that an error was detected on a received character or a COD character was received while a transmit-allow-break type operation is in process. If a "break" is received, the IIB contains 00.

- CC7—Not used

  This condition code is not reported by asynchronous/synchronous communications.

STATUS

Interrupt Identification Word

The attachment, when presenting an interrupt request along with an interrupt condition code, also transfers an interrupt ID word to the processor.

Interrupt ID word

IIB (ISB)								*Device address*							
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
0							*7*	*8*							*15*

IPL

Initial program load (IPL) by a host system may be accomplished through the attachment, using EBCDIC characters only. IPL may be used with point-to-point leased line, switched line, or multipoint operations.

If the disable IPL jumper is not installed or if IPL is not deselected by an attachment-storage load from the CE initializer diskette or the user's program, the attachment monitors the line for the following sequence: SYN, SYN, (address character), (address character), DC1, DC1, ENQ. (The address characters are used only if the attachment is a multipoint-tributary station.)

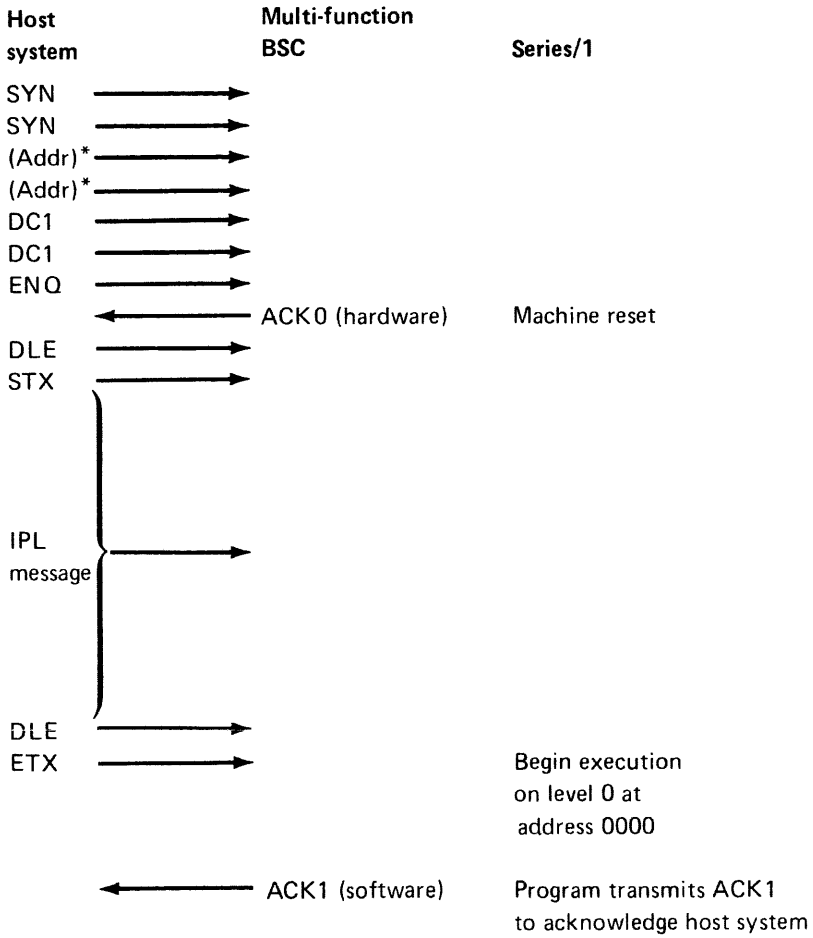
Any eight-bit secondary station address can be assigned if an attachment-storage load is configured from the initialization diskette. The multipoint secondary-station address selected during attachment initialization overrides the secondary station address assigned during installation of the attachment feature.

The secondary station address is limited to hexadecimal characters C0 through C7, before initialization from the CE initializer diskette or user's operating system.

Before attachment initialization, by the initialization diskette or the user's operating system, the attachment defaults to half-rate select. After attachment initialization, half-rate select is programmable. See DCB word 0, bit 8, later in this section.

When the IPL sequence is received, the attachment hardware responds with an EBCDIC acknowledgment (ACK0). The host system must then transmit DLE-STX, followed by the IPL program.

If the attachment is a multipoint-tributary station, its address must be included in the IPL sequence, as shown in the following example (it must also have been placed in control mode):



*Used only if the attachment is a multipoint tributary.

The attachment presents a device-end interrupt request or begins a DCB chaining operation if a line control character associated with change of direction (COD) is received and the byte count is decremented to 0.

Programming Consideration: Bit 12 (start timer) of DCB word 0 may be used in conjunction with a receive operation to limit the time that the attachment allows for establishing character synchronization to 3 seconds. Failure to establish character synchronization within 3 seconds results in an exception- interrupt request with interrupt status byte bit 0 set to 1. If bit 15 is set to 1 in conjunction with bits 2 and 12, a receive time-out occurs when the count in DCB word 2 (timer) is decremented to 0.

Programming Consideration: When no operation is being processed the attachment receives characters in anticipation (pre-receive) of the next receive operation. Errors may occur during pre-receive. When a receive operation is issued, errors that occurred during pre-receive are reported when the receive operation is issued. A transmit operation clears all pre-received characters.

BITS 3 AND 4—NOT USED: These bits are not used and must be set to 0's.

BITS 5 THROUGH 7—CYCLE-STEAL ADDRESS KEY: This is a three-bit key presented to the processor by the device, during cycle-steal data transfers. It is used by the processor to determine if the device is authorized to access certain blocks of processor storage.

BIT 8—HALF-RATE: If bit 8 is a 1, the modem (if it is equipped to recognize half-rate) runs at one-half of its normal bit rate. If bit 8 is a 0, the modem runs at its normal bit rate. The status of bit 8 must only be changed in conjunction with an enable-terminal operation (bit 10 set to 1).

Programming Consideration: After the program changes the status of bit 8, the program must provide the appropriate delay (usually about 13 seconds) before issuing any transmit or receive operations.

Programming Consideration: If half-rate is specified and the answer-tone option is selected as a result of attachment initialization, the attachment resets the bit rate to its normal speed when the answer-tone is generated. Another enable terminal operation with bit 8 (half-rate) set to 1 must be issued to set half-rate active.

Note: Half-rate may also be called data rate select.

BIT 9—ASCII MODE: If this bit is a 1, the attachment uses the ASCII transmission code; if bit 9 is a 0, the attachment uses the EBCDIC transmission code. (Refer to Appendix B, "Transmission Codes," for a list of the ASCII and EBCDIC characters.)

Programming Consideration: In ASCII mode, the program must maintain odd parity in bits 0–7 of each byte.

BIT 10—ENABLE TERMINAL: This operation is used to activate DTR.

Programming Consideration When this bit is set to 1, a device-end interrupt request occurs 50 milliseconds after DSR becomes active. If DSR is always active, a device-end interrupt request occurs immediately.

A start timer operation (bit 12 set to 1) may be used in conjunction with an enable terminal operation to limit the time that the attachment waits for DSR to become active. If bit 12 is a 1, DSR must become active within 13 seconds; otherwise, the attachment resets DTR and an exception-interrupt request occurs with interrupt status byte bit 0 set to 1.

For leased-line applications, DTR is normally set on during attachment initialization.

BIT 11—DISABLE TERMINAL: A disable terminal operation causes the attachment to deactivate DTR. Bit 12 should not be set to 1 in conjunction with bit 11.

Programming Consideration: For switched- line applications, when DTR is deactivated, the line disconnects. The attachment presents a device-end interrupt request or begins a chaining operation 2 seconds after DSR becomes inactive. If DSR is not deactivated within 3 seconds, the attachment presents an exception-interrupt request with interrupt status byte bit 0 set to 1.

DTR is not deactivated by a disable terminal operation if DTR is activated by the initialization program; however, a device-end interrupt is presented.

BIT 12—START TIMER: The start timer operation causes the attachment to start a 2-second time-out. After 2 seconds, the attachment presents a device-end interrupt request. Bit 11 should not be set to 1 in conjunction with bit 12.

Programming Consideration: Bit 12 can be used in conjunction with an enable terminal operation (bit 10) or a receive operation (bit 2). When bit 12 is used in conjunction with bit 10, a 13-second time-out occurs. When bit 12 is used in conjunction with bit 2 and bit 15 is set to 0, a 3-second time-out occurs.

When bit 12 is used in conjunction with bit 2 and bit 15 is set to 1, the timer value in DCB word 2 determines when the time-out occurs.

BIT 13—TRANSMIT OPERATION: The transmit operation starts a 3-second timer and activates RTS. After CTS becomes active, character synchronization is established between the attachment and the BSC terminal or host system, and the attachment transmits data.

Programming Consideration: The attachment presents a device-end interrupt request if a line-control character associated with a change-of-direction is transmitted and the byte count is decremented to 0; if chaining is specified, the next operation begins.

If DSR is not active when the transmit operation begins, an exception-interrupt request occurs with interrupt status byte bit 0 set to 1. Cycle-steal status word 1, bit 2 (communications interface error), is set to 1.

If CTS is not detected within the 3-second time-out period, or CTS is active for 3 seconds without RTS being active, an exception-interrupt request occurs with bit 0 set to 1 in the ISB. Cycle steal status word 1, bit 2 (communications interface error) is set to 1.

The attachment resets transmit mode and RTS after transmitting the pad character following a COD character. If block checking is used, the attachment resets transmit mode and RTS after transmitting the pad character following the BCC.

BIT 14—EXIT TRANSPARENT This operation is used to transmit the control sequences shown here, following a block of transparent text, to reset transparent mode.

- DLE-ETX
- DLE-ETB
- DLE-ITB
- DLE-ENQ

The exit transparent operation requires its own DCB and a byte count of 2. Unexpected results may occur if the byte count is greater than 2.

BIT 15—RECEIVE WITH PROGRAMMABLE TIME-OUT: The receive with programmable time-out operation causes the attachment to wait the time specifed in DCB word 2 for character phase to be established. An exception-interrupt request occurs if the timer is decremented to 0 before character phase is established. Bit 15, when set to a 1, must be used in conjunction with bit 2 (receive) and bit 12 (start timer) in the DCB control word.

DCB Word 1—Not Used

DCB word 1 is not used and should contain 0's.

DCB Word 2—Timer

The value specified in bits 0–15 of this word determines the value set in the attachment timer used with a receive with programmable time-out operation. The timer is decremented by 1 every 3.33 milliseconds.

DCB Words 3, 4—Not Used

DCB words 3 and 4 are not used and should contain 0's.

Status Word 2—Status

Refer to IBM Series/1 Multi-Function Attachment Feature Initialization User's Guide ,GA34-0147, for additional information about attachment initialization and communications options.

BIT 0—DATA TERMINAL READY: This bit is a 1 to indicate that data terminal ready (DTR) is active. DTR is set by an enable terminal operation or during attachment initialization.

BIT 1—DATA SET READY: This bit is a 1 to indicate that the attachment detected data-set ready (DSR). It may be either in response to DTR (bit 0) from the attachment or it may be a power-on indication from a leased-line modem.

BIT 2—REQUEST TO SEND: This bit is a 1 to indicate that request to send (RTS) is active in the attachment.

BIT 3—CLEAR TO SEND: This bit is a 1 to indicate that the attachment detected clear to send (CTS).

BIT 4—RING INDICATOR: This bit is a 1 to indicate that the attachment received a signal from the modem when the modem detected a 'ring condition' on the line. An attention-interrupt request occurs for each ring cycle detected.

BIT 5—HALF-RATE SELECTED: This bit is a 0 to indicate that a half-rate operation (bit 8 set to 1 in the DCB control word) was issued. (The modem may or may not be equipped to operate at half-rate.)

Note: Half-rate may also be called data rate select.

BIT 6—TRANSMIT MODE LATCH: This bit is a 1 to indicate that the attachment is transmitting data.

BIT 7—NOT USED: This bit is not used and is a 0.

BITS 8-15—INDICATOR PANEL SWITCH SETTING: These bits indicate the setting of the communications indicator panel DISPLAY/FUNCTION SELECT switches (if the panel is installed); these bits are 0's if the communications panel is not installed.

OPERATE I/O INSTRUCTION CONDITION CODES

Each time the attachment receives an Operate I/O instruction, it immediately sends the processor a condition code pertaining to the execution of the I/O command. This three-bit code, representing a decimal number 0 through 7, is stored in the even, carry, and overflow positions of the level status register (LSR) located in the processor. Refer to the appropriate processor description manual for additional information about level status registers.

Condition codes reported after execution of an Operate I/O instruction are:

- CC0—Device not attached

  This condition code is reported when the device address specified is not recognized by the multi-function attachment.

- CC1—Busy

  This condition code is reported when the addressed device is unable to execute a command because it is in a "busy" state. The device enters the busy state upon acceptance of a command that requires an interrupt request for termination. It exits the busy state when the processor accepts the interrupt request.

- CC2—Busy after reset

  This condition code is reported when the device is in the process of being reset.

- CC3—Command reject

  This condition code is reported when a command is issued to the device and the command is outside the device command set or the IDCB contains an incorrect parameter.

- CC4—Not used

  This condition code is not reported by binary synchronous communications.

- CC5—Interface data check

  This condition code is reported when a parity error is detected on the processor I/O channel data bus during a data transfer.

- CC6—Controller busy

  This condition code is reported when the attachment feature is "busy" processing a command.

  Reissue the instruction, about every millisecond, until it is accepted. Controller busy does not stay active for more than 2 milliseconds, with an average period of about 150 microseconds.

- CC7—Satisfactory

  This condition code is reported when the attachment feature accepts a command.

INTERRUPT CONDITION CODES

The following condition codes are presented with a priority interrupt request.

- CC0—Not used

  This condition code is not reported by the multi-function attachment.

- CC1—Not used

  This condition code is not reported by binary synchronous communications.

- CC2—Exception

  This condition code is reported when an error or exception condition is associated with the interrupt request. The condition is described in the interrupt status byte (ISB) or in cycle-steal status words. The status words can be obtained by executing a Start Cycle Steal Status command.

- CC3—Device end

  This condition code is reported when an operation has terminated under normal conditions.

- CC4—Attention

  This condition code is reported when the attachment receives a ring indication from the modem. An attention-interrupt request occurs for each ring cycle detected.

- CC5—Not used

  This condition code is not reported by binary synchronous communications.

- CC6—Attention and exception

  This condition code is not reported by binary synchronous communications.

- CC7—Not used

  This condition code is not reported by binary synchronous communications.

STATUS

Interrupt Identification Word

The attachment, when presenting an interrupt request along with an interrupt condition code, also transfers an interrupt ID word to the processor.

Interrupt ID word

IIB (ISB)	*Device address*
X X X X X X X X	X X X X X X X X
0 *7*	*8* *15*

The interrupt information byte (IIB) contains all 0's for interrupt requests from the binary synchronous communications for any interrupt condition code other than 2 or 6. When an interrupt condition code of 2 or 6 occurs, the eight-bit IIB takes on a different format, called an interrupt status byte.

Command	Operate I/O CC	Recommended action
Halt I/O	0,1,3,5,6	Exit the error-recovery procedure (equipment error).
Device Reset	0	Exit the error-recovery procedure (device not attached).
	1,2,6	Exit the error-recovery procedure (equipment error).
	3	Examine IDCB function modifier; exit the error-recovery procedure if the IDCB is correct.
	5	Retry three times; exit the error-recovery procedure if the problem persists.
Start, Start Cycle-Steal Status, and Start Control	0	Exit the error-recovery procedure (device not attached).
	1	Issue a Device Reset; retry the failing operation. (The attachment may be busy after reset when the retry occurs following a Device Reset command. Exit the error-recovery procedure if the problem persists.
	2	The attachment may be busy as a result of a Device Reset command. The program should provide a delay between retries and retry three times.) Exit the error-recovery procedure if the problem persists (equipment error).
	3	Examine the IDCB function modifiers; exit the error-recovery procedure if the IDCB is correct.
	5	Retry three times; exit the error-recovery procedure if the problem persists.
	6	Retry until the command is accepted.

2. Inspect the interrupt condition code.

   - If the interrupt condition code is 3 or 4, exit the error-recovery procedure. (Condition code 4 is reported when a 'ring indication' is detected from a modem; it is not an error condition.)

   - If the interrupt condition code is 2, use the following charts.

Interrupt status byte (hex)	Recommended action
A0	During a transmit or a receive operation, the attachment detected a COD character and the byte count is not 0. Issue a Start Cycle Steal Status command to determine the residual address. The residual address contains the processor storage address where the COD character is located.
80	Issue a Start Cycle Steal Status command and go to step 3.
40	Ensure that the IDCB contains a valid function modifier and that the DCB address in the immediate data field is even. Correct any error conditions and retry the operation. Exit the error-recovery procedure if the problem persists.