

IMSAI 8080 FRONT CONTROL PANEL

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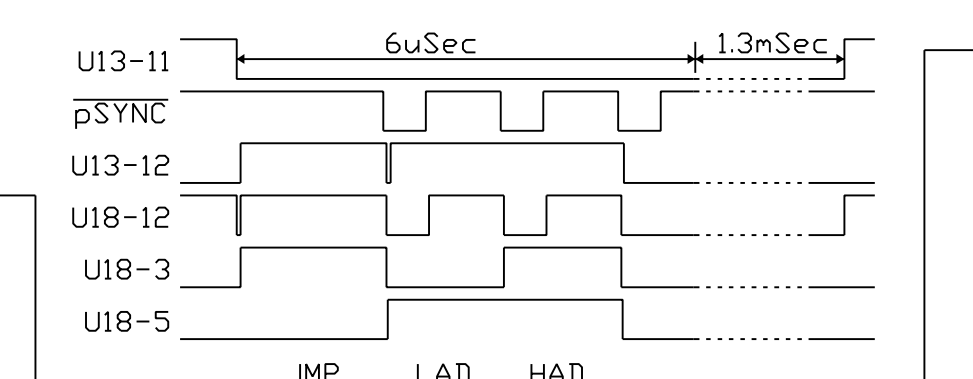
NOTE 1: FORCES DIRECTION OF DATA BUS DRIVERS ON MPU TO "LOOK THE OTHER WAY" WHILE DATA FROM THE CPA IS IMPOSED ON THE MPU'S LOCAL DATA BUS.
 A '0' FROM SSW DSB, DIRECTION FORCED TO PREVENT BUS CONTENTION
 WHILE NOT IN RUN MODE (RUN=0)
 A '1' FROM ANY OF THE FOLLOWING WILL FORCE DATA TO S-100 BUS
 DEPOSIT TO RAM, DIRECTION FORCED TO ROUTE DATA SWITCHES TO RAM
 EXEC NOP, DIRECTION FORCED TO PREVENT BUS CONTENTION
 EXEC JUMP, DIRECTION FORCED TO PREVENT BUS CONTENTION

- R1 - 270kΩ
- R2,6,7,10,11,13-15,60 - 1kΩ
- R3-5,8,9,12 - 47kΩ
- R16-59 - 220Ω
- C1,2,5,6,7,11-22 - 0.1μF
- C3,8 - 0.001μF
- C4 - 0.01μF
- C9,10 - 33μF
- CR1 - 1N914
- U1,3,4,6,7 - 7405
- U2 - DATA HEADER SOCKET
- U5 - 8212
- U8,15 - 74LS04
- U9 - 74LS30
- U10 - 7404
- U11 - 74LS10
- U12 - 7410
- U13,16 - 7402
- U14,25 - 7400
- U15,5 - 7427
- U17,20,23 - 74123
- U18,19,22 - 74107
- U21 - 7430
- U24 - 8T97

CAUTION! HIGH VOLTAGE LIVE MAINS POWER

- 96 sINTA
- 97 sW0
- 98 sSTACK
- 48 sHLTA
- 45 sOUT
- 44 sM1
- 46 sINP
- 47 sMEMR
- 28 pINTE
- 26 pHLDA
- 27 pWAIT
- 79 A0
- 80 A1
- 81 A2
- 31 A3
- A4
- 30 A5
- 29 A6
- 82 A7
- 83 A8
- 84 A9
- 34 A10
- 37 A11
- 87 A12
- 33 A13
- 85 A14
- 86 A15
- 32

- 220 R40 LS0
- R41 LS1
- R42 LS2
- R43 LS3
- R44 LS4
- R45 LS5
- R46 LS6
- R47 LS7
- R48 LIE
- R49 LHT
- R50 LWT
- 220 R24 LA0
- R25 LA1
- R26 LA2
- R27 LA3
- R28 LA4
- R29 LA5
- R30 LA6
- R31 LA7
- R32 LA8
- R33 LA9
- R34 LA10
- R35 LA11
- R36 LA12
- R37 LA13
- R38 LA14
- R39 LA15



NOTE 1 (CAN ONLY HAPPEN WHEN RUN=0)
 FORCE LOCAL BUS ONTO CPU INSTEAD OF THE S-100 BUS

NEXT HAPPENS FIRST, DEPOSIT IS DELAYED BY THE FALLING EDGE AFTER THE U20 ONE-SHOT

DISABLE S5, DEPOSIT & EXAMINE WHEN CPU IS RUNNING

99 PDC

76 pSYNC

70 PROTECT

24 Ø2

39 D05 (M1 STATUS BIT)

