MIDWAY REPORT

ANTACCS PROJECT

July 1964

INFORMATICS INC.

MIDWAY REPORT

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TECHNOLOGY, METHODOLOGY AND INTEGRATION
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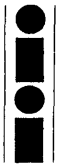
ANTACCS MIDWAY REPORT

SUMMARY

This is a report of the technology, methodology, and integration aspects of the ANTACCS study project sponsored by the Office of Naval Research, in conjunction with various Naval organizations including BuShips, BuWeps, Chief of Naval Operations, and Commandant Marine Corps. It is the preliminary report of work performed by Informatics Inc. under Contract Nonr-4388(00). It is a Midway Report representing that portion of the work accomplished during the first half of the 12 month project.

The project members of Informatics Inc. are indebted to Mr. R. Tuttle, the ONR Scientific Officer who is guiding this effort. They are also indebted to the Study Monitor Group, a group consisting of knowledgable and experienced persons from BuShips, BuWeps, Chief of Naval Operations, NAVCOSSACT and Marine Corps Headquarters for their advice in this effort. The knowledge of the Scientific Officer and the Study Monitor Group in Naval requirements and environment as well as their experience with present Naval efforts has been of valuable assistance in the assurance of a more useful product.

The technical staff of Informatics has been supplemented in certain technical areas by subcontracting efforts of Hobbs Associates. Hobbs Associates has provided many of the sections on hardware techniques, especially those in the circuits and packaging areas. Hobbs Associates has also contributed in the area of memories and display devices.



The purpose of this project is to develop and present information concerning technology, methodology and integration which will be of assistance to planners in the design and implementation of command control systems. The project scope and emphasis is restricted to the application of its techniques and data to the solution of problems concerning the Advanced Naval Tactical Command Control System. This system is identified by an SOR as being visualized for the 1970-1980 time period, and for which a TDP is to be developed in 1966.

The three areas of the project are: Technology, Methodology, and Integration. Technology deals with scientific and technical material of potential use to Naval command control systems. This material includes both hardware and software subjects. Methodology is concerned with technical and managerial techniques used in the planning and implementation of Naval systems. Integration covers the unification of technology, methodology, and requirements into candidate approaches to the design of Naval systems and their parts.

This Midway Report represents work in progress. An attempt has been made to organize the report in such a way that all areas are included, at least structurally, as they will appear in the final report. Since this is a preliminary report, many sections are incomplete. In many cases only a foundation of information for the technical area has been collected and organized. Still to be accomplished in most of the areas is the translation of that basic information to opinions and conclusions concerning the usefulness or future application of this particular information. For instance, in the display area the techniques have been identified, classified and analyzed. Remaining is a discussion

of the relative merits of the various approaches, especially related to operational requirements in ANTACCS.

It is the express desire of the Informatics project personnel that this report be examined with a critical eye by the Scientific Officer, the Study Monitor Group and others who may also be qualified to criticize it. It is hoped that the critical viewpoint is taken within the framework of the fact that this is a preliminary report representing work in progress. The major useful contribution of the contract effort will be developed and reported during the last half of the project effort. We believe that sufficient information is presented in this present report to indicate the general direction in which the project is proceeding. It should provide the basis to allow the ONR Scientific Officer and the Study Monitor Group to redirect the efforts as appropriate.

1. INTRODUCTION

1.1 GENERAL

Perhaps the fastest growing technology within the military at the present time is that of command and control systems for strategic and tactical uses. This technology deals with the application of modern electronic computer techniques to modern military operational requirements. The subject matter of this report is techniques for design and implementation of tactical command and control systems. Although the work deals principally with the techniques, equipments, technology and methodology involved in the implementation of Advanced Naval Tactical Command and Control Systems (ANTACCS) for the 1970-1980 time period; the information is of interest in other military command and control systems.

The technology stemming from and involved with the modern stored program electronic computer is only 14 or 15 years old. It has not benefited from the many years of experience and discipline of such important Naval technologies as naval architecture or armament design. The technology is very new and rapidly growing; methodology in the sense of unified, universally-used techniques is virtually nonexistent. The object of the ANTACCS study project is to provide information on information processing technology and information systems design methodology to serve as a resource document for the use of planners of future Naval tactical data systems.

Military command and control systems provide a greater challenge to electronic data processing than any other application. Some of the characteristics of command and control systems which account for this challenge are:

1) Considerable emphasis on man/machine interactions and requirements; the command and control system is, in the final analysis, designed to facilitate the decision processes of the commander and his staff.

2) The computer is imbedded in an on-line or real-time environment involving a large amount of instrumentation and peripheral equipment with which it must interact.

3) In most command and control applications there are large-scale file management tasks involving the receipt, collation, and retrieval of facts.

4) Most command and control system are very large information handling systems involving a multiplicity of input and output information channels. These systems are further complicated by the requirement to interact logically with many command levels and with much remote instrumentation.

5) There are especially challenging operational and environmental problems; reliability requirements are exceedingly high, and physical and logical environmental constraints are very often especially restricting.

Together these create a special challenge for the designer, from the component level to the system integration level.

Naval tactical command and control systems supply even greater challenges than command and control systems in general. There are additional physical factors which become important; space limitations and the movement of a ship or vehicle are simple examples. There are additional logical and operational factors: missions change for a given vehicle or platform, the entities with which the system communicates may change depending on the mission or operation, and there are extraordinary problems of logistics in installing, maintaining and operating equipment on a fighting ship.

To assure a meaningful product and remain responsive to the requirements of ANTACCS, the project will illustrate the techniques developed by applying them to the requirements developed and discussed by Booz Allen Applied Research, Inc. in a companion report. Accordingly, this volume discusses

technical material useful to system designers in defining, designing, and implementing systems such as ANTACCS. This is done from the standpoint of the electronic equipments involved, and with special regard for the people who will use them. It deals with the technology of future command and control systems, that is, the hardware and software techniques available for or necessary to system implementation. It also deals with the methodology of system implementation, that is, the techniques of system engineering management and the application of these techniques to satisfy requirements and to thereby produce an operational system. Although this work is related to the requirements which have been developed in a companion project by Booz Allen Applied Research, Inc., to a very great extent, it can stand on its own as a document for future use of planners of Naval command and control systems.

The scope of the present work is of extraordinary magnitude. The subject matter of technology ranges from integrated circuitry of a computer to computer systems organization. Methodology subjects range from simulation languages to techniques for planning and implementing ANTACCS.

1.2 STUDY OBJECTIVES AND APPROACH

There are three aspects of the study treated in this report: Technology, Methodology and Integration. Technology deals with the techniques and embodiments - both hardware and software--for implementing data processing functions. Methodology deals with the techniques for the design, evaluation, and synthesis of equipments of all levels within the system as well as the management techniques for accomplishment of an operational system.

The principal objective of the integration subtask is to illustrate technology and methodology by developing certain approaches to the design of various portions of ANTACCS, as prescribed by the requirements developed by BAARINC. It is visualized that this subtask will analyze and evaluate synthesized system components at various levels, thus illustrating how the various aspects of technology and methodology are unified and integrated into usable concepts.

The objectives of the ANTACCS project are visualized to the the following:

1) To identify, analyze and evaluate hardware and software techniques of potential use in ANTACCS.
2) To develop resource information and to provide reference documentation representing information of use to future Naval command and control system planners.
3) To supply a unifying force to integrate the concepts developed or available in technology and methodology.
4) To develop approaches to a number of candidate systems which illustrate, in a practical way, techniques of technology and methodology in ANTACCS.

The information developed in this project can be used in a number of ways:

1) As reference documentation.
2) To identify research and development needs for future system implementation.
3) As a specific guide to planners of future systems.

1.3 REPORT ORGANIZATION

The principal organization of this report is a division of the presentation into the three main efforts: technology, methodology and integration. Section 2 covers technology. The following items are covered: displays, input/output devices, memories, components and packaging, packaging techniques, advanced usage techniques and machine system organization.

In each portion of the technology there is first a classification of the techniques. Next, the sources of information are discussed and presented. This refers to the people, companies, and the literature from which information was obtained. The characteristics appropriate for ANTACCS are discussed, the application of the technology in the Naval environment is further presented, as well as a review of the current status of the equipments and techniques. Following this, the availability of technology in the 1975 era, the limitations of the present and planned technology and the recommended developments for the future are presented. Each portion is concluded with a discussion of evaluation criteria, conclusions and recommendations. Although the specific sections may deviate from this order in certain instances, in general in each section there is an attempt to cover all of these points.

Section 3 deals with methodology. For the purposes of project organization, methodology has been split into three major areas: general methodology, implementation procedures, and specific methodology. General methodology deals with:

1) Tools and techniques which the system designer has at his disposal.
2) A methodology generally or universally applicable and not necessarily restricted to systems of a special purpose nature or a special class.
3) A methodology which is generally available, exists as a tool, and can be readily applied.

Implementation procedure deals with the understanding of tasks - both technical and managerial - which must be accomplished in the implementation of modern command and control systems. Specific methodology relates to the special requirements of selected equipment configurations and design problems which might arise in ANTACCS.

In general, the elements discussed above under technology with regard to classification, sources, requirements, status, limitations, evaluations, developments, conclusions and recommendations are covered in each methodology section. Under general methodology simulation languages and techniques of simulation are covered in some detail. Under implementation procedures, system design, implementation and evolutionary aspects of systems have been described. In specific methodology some quantitative design tools are presented.

In the section on integration the scope and objectives of integration are first discussed. Following this there is a comparison of implications of alternate system operating concepts. This concerns the various operational philosophies which the Navy might adopt relating to the structure and organization of the various tasks to be performed and involving such aspects as platforms, missions and command structures. Following this there is a discussion of the synthesis and evaluation of a system node. This illustrates how the information developed under requirements with regard to system technical functions can be translated into data processing functions. A matrix technique is described which relates platforms together with their missions and command levels, to operational tasks and data processing tasks.

Included in each section is an extensive bibliography. Generally, in the text reference is made at appropriate points to items in the bibliography. Also, at the close there is a general bibliography for the entire project effort.

(In the future final report there will be certain additions and modifications to the organization described above. For instance, in the final report there will be an extensive list of opinions, conclusions and recommendations for the entire project effort and for the various tasks. There will also be a cross reference index to assist the reader in finding his way through the technical information. Another item to be added in the final version is an extensive glossary of terms.)

2. TECHNOLOGY

2.1 GENERAL AND INTRODUCTORY

The purpose of this study of present and advanced technology is to identify, analyze, evaluate and document those areas of technology which will have significant impact on future Navy tactical data systems. This study will probably not uncover any new areas of technology or disclose any new areas of application to the experienced system designer. It will, however, provide analyses which will place the new technologies in proper perspective and provide criteria and examples to aid in evaluating and selecting future equipment.

As the first phase of this study is necessarily devoted to the collection of information and the analysis of that information, rather than its evaluation and documentation, it follows that little completed work is available to include in this report.

It is, therefore, intended that this section should indicate those areas in which progress has been made and show the type of work being done, rather than present some small sample of the finished product.

2.2 DISPLAY TECHNOLOGY

2.2.1 Classification of Display Types

Display types can be classified in a number of different ways that are not mutually exclusive. Associated groupings of display technology will vary with the method of classification. Among the ways in which displays can be classified are:

1)	Functional	Console Large-Screen
2)	Nature of Data to be presented	Status Displays Real-time or Dynamic Displays
3)	Type of Data	Alphanumeric Symbols Graphical
4)	Type of Mechanization	Cathode ray tube Electroluminescent Character lights Photographic Projection Light-valve Mechanical Inscriber Photochromic Ferro-electric Opto-Magnetic Laser-luminescent

In this report, displays will be classified by the type of mechanization. In the discussion of each type of display that has been investigated to date, the functional use and the nature and type of data to which it is adaptable will be considered. Any factors that make a particular type of display unsuitable for a certain function or for certain kinds of data will also be noted. For example, the fact that a cathode ray tube is not suitable for a large-screen display, or the fact that a photographic projection type, large-screen, display cannot present real-time dynamic information, will be discussed as limitations of these techniques that make them unsuitable for certain functional uses and for certain types of data.

2.2.2 Sources of Information

2.2.2.1 People and Organizations

The following lists the companies and governmental agencies with whom displays have been discussed during this study, and the type of displays discussed with each.

1)	Bunker-Ramo Corporation Canoga Park, California	Light-valve displays Continuous-strip photographic projection displays CRT displays
2)	General Dynamics/Electronics San Diego, California	Charactron CRT displays Light-valve displays
3)	General Telephone Laboratories Bayside, Long Island, N. Y.	Continuous-sheet electroluminescent displays with XY matrix addressing Acoustic/electroluminescent displays
4)	RCA Laboratories Princeton, New Jersey	Ferroelectric displays
5)	Laboratory for Electronics Boston, Mass.	Magnetic thin-film displays
6)	NCR El Segundo, California	Electro-mechanical photochromic displays CRT-Photochromic projection displays
7)	Sylvania Waltham, Mass.	Discrete alphanumeric character displays Continuous-sheet electro-luminescent displays with XY matrix selection
8)	Stanford Research Institute Menlo Park, California	Magnetic thin-film displays Modulated crystal filter displays

9)	Rome Air Development Center Rome, New York	Light-valve displays Modulated crystal interference-filter displays Thermo-plastic displays Laser displays
10)	USAER&DL Fort Monmouth, New Jersey	Photochromic displays Laser-luminescent displays Fiber-optic CRT displays Photographic projection displays Display memories
11)	U.S. Navy Bureau of Ships Washington, D.C.	Photographic projection displays CRT displays

Much of the information presented in subsequent portions of this section are based on discussions with display experts in the organizations listed above. Their descriptions of specific display techniques and their opinions of the advantages, disadvantages, and limitations of display techniques were relied upon heavily in the preparation of this report.

2.2.2.2 Literature

An extensive list of references pertinent to the study of display technology are given in the Bibliography. To date, only a few of these have been studied in detail. Some of the material in this section has been extracted from these references. The more important and pertinent of these references will be studied in detail during the remainder of this study and new references will be added to the Bibliography to reflect material published or discovered subsequent to the preparation of this report.

2.2.3 Display Characteristics for ANTACCS

The display characteristics required for ANTACCS cannot be fully identified at this time since the results of the requirements analysis have not been available. However, it is anticipated that both console and large-screen displays will be required; that alphanumeric, graphical, and dynamic real-time data must be presented; and that multi-color displays (particularly for large-screen applications) will be required.

It is further believed that electro-mechanical display systems and photographic projection systems will not be acceptable for a 1970 system.

The analysis of display technology and the information presented in the final report will permit the selection of display technologies with the appropriate characteristics for any functional use in an NTDS or MTDS system. This analysis will include all the more important and feasible types of displays that might be applicable to such systems in 1970.

2.2.4 Applications of Displays in the Naval Environment

It is anticipated that applications of displays for shipboard and ground-based military environments in the 1970 era will include console and large-screen presentation of both status information and real-time dynamic information such as target track data. The applicability of specific types of displays to different applications will be considered in further detail in the remainder of this study.

2.2.5 Current Status Review

The investigation of new display technology has not progressed as far at this point in the study as that of some other areas, such as, for example, memory technology. The information collected to date is summarized here, but comparisons and evaluations of different types of displays are not yet available. Detailed comparisons of specific existing display devices were presented and discussed in the initial proposal for this study. Although these are available, they are not included in this report since they are representative of past technology rather than that to be anticipated for the 1970 era. Since a number of satisfactory techniques for console type displays are now available, there will be no problem with respect to the availability of console type displays for a 1970 system. Existing cathode ray tube technology and anticipated improvements in this technology should meet all requirements for small-screen console type displays, even if none of the new technologies prove to be superior.[1,2*] However, with respect to

* References are listed at the end of each subsection.

large-screen displays the situation is much less favorable. In an RADC Technical Documentary Report[3] published in 1962, the state-of-the-art and development efforts for large screen displays were described as follows:

> "Display developments are being undertaken in three major technological areas. These areas may be differentiated in terms of the basic processes being applied and on the basis of development time required to provide fully operational subsystems.
>
> The first of these processes is based on projection and employs a stable light modulator, such as film or selenium plate, to provide the display. Operational subsystems of this sort are considered to be achievable within months.
>
> The second process, the light valve, in theory should provide adequate performance for systems applications, and it has the dual advantages of operation at electronic speeds and of the elimination of expensive film. However, the performance potentials have not been realized in practice, and major technological improvements must be made before the light valve can be useful for most systems applications. The presently available models exhibit major weaknesses in their capability to provide high resolution and brightness.
>
> This low brightness makes it impossible to use the light valve in the high-ambient lighting conditions of most of the systems. The interactions of the oil film and the lens systems are such that it is not possible to increase the display brightness level without major improvements in the characteristics of the modulation surface. Improvement, very likely, is contingent on the development of suitable thermoplastic materials. Light valve techniques show considerable promise, and with suitable development may eventually supersede film systems. However, it should be clearly recognized that full realization of the light valve's potential may require years of additional research.
>
> The third process, electroluminescence, does not require projection since the display surface itself acts both as light source and modulator. Only small laboratory devices for demonstration and experimentation are available at the present time. Electroluminescence is appealing in its apparent simplicity, its capability to eliminate projection, and its characteristic of non-catastrophic failure. In addition, there is a potential for full color operation at high brightness levels, and the large surface reduces the problems of obtaining high resolution. Unfortunately, there is an impressive number of technical obstacles that must be overcome before electro-luminescent devices can meet the requirements of the systems. The

> most immediate problem is that of modulating the display surface, and a number of promising efforts are underway in this area at the present time. This effort is concurrent with others that are aimed at the development and application of new phosphors to obtain high brightness levels and multiple colors. However, even allowing for impressive technological improvements, years will be required to advance the capability of electroluminescent displays to the point where they can serve as dynamic large scale displays for system applications.
>
> Desirable as these advanced displays are, most immediate requirements of Command and Control Systems can only be met by projection techniques using film or xerographic techniques for light modulation."

Unfortunately, developments during the past two years have not significantly altered the views quoted above, except that improved technologies are of course somewhat closer to realization now than they were in 1962.

Photographic projection techniques are still the only feasible means of meeting operational requirements for large-screen displays in Command and Control Systems. Significant progress has been made in light-valve type displays during the last two years, but the reliability and life of these devices does not permit their use at this time in an operational system in which minimum down time is an important requirement. However, new and improved light-valve type devices offer great promise for a system to be operational in 1970.

Display techniques that have been developed or that appear promising for the future include individual character lights, cathode ray tubes, mechanical inscriber systems, film or photographic projection systems, light-valves, photochromic systems, electroluminescent devices, ferroelectric devices, opto-magnetic devices, and laser systems. Of the above techniques, it is believed that mechanical inscriber systems and film and photographic projection systems will be obsolete by 1970. Improved light-valves, electroluminescent panels, photochromic displays and, possibly, laserluminescent displays appear very promising for that time period. The display technologies that have been investigated to date are discussed briefly in the following parts of this section.

2.2.5.1 Mechanical Inscribing Machine

A mechanical inscribing system permits the large-screen display of real-time dynamic information at a relatively slow rate[4]. In this type of display, a glass slide coated with an opaque material is inserted into a projection system. Another glass plate with a stylus mounted in its center is positioned parallel to the first slide so that tipping the glass plate causes the stylus to penetrate the opaque material. When the stylus is moved in the X and Y directions by a servo-mechanism under the control of external signals, a trace is inscribed in the opaque material on the face of the slide. The light from a lamp is projected through this trace on the glass slide and focused on a projection screen. Thus, the trace will appear on the screen and can be drawn in real-time.

The use of color filters in the light path permits color traces to be generated. A composite multi-input or multi-color display can be generated by superimposing the images from several projection systems. Additional projectors can be used to superimpose static information, such as maps, on the dynamic information. Since the inscribed trace remains on the glass slide, no external memory is required for this type of display.

With a trace width of 0.001 inches on the slide, the projected trace will be about 0.1% of the screen size. Recent systems require approximately 50 milliseconds to inscribe a trace across the full width of the screen. Alphanumeric characters can be inscribed at a rate of approximately 20 characters per second.

2.2.5.2 Charactron Shaped-Beam Cathode Ray Tube

The Charactron is basically a cathode ray tube which includes a character generating mask and the necessary electrodes for shaping the beam inside the tube[5]. The electron beam is deflected to the proper position in the character mask corresponding to the character to be generated. As the beam passes through the mask, it is extruded

into the shape of the character. The shaped beam is then returned to the axis of the tube by deflection electrodes and deflected to the desired position on the face of the tube.

Random display rates of 50,000 characters per second are possible with this technique. The limiting factor is the time required to position the character on the face of the tube rather than the time required to shape the beam. The Charactron tube is not limited to the generation of alphanumeric characters but can also generate any symbol fabricated in the mask. A typical mask has 64 different characters or symbols, but 144 symbol masks have been used, and several hundred are considered possible.

The Charactron is claimed to have three major advantages over the stroke or dot matrix method of symbol generation:

1) Reliability
2) Legibility or definition
3) System complexity

Since the charactron is basically a cathode ray tube, it can be operated as a conventional cathode ray tube to generate graphical data and target traces in real time. Any shape and size of symbol can be chosen since this is a function of the fabrication of the mask. Charactron tubes are useful for image generation in photographic projection systems for large-screen displays as well as for direct viewing in console displays. Recent development permits the simultaneous generation of alphanumeric and real-time video information by the use of two electron guns in the tube. Another recent development provides a rear window in the tube so that a photographic image can be projected through the window and superimposed on the face of the tube with the electronically generated picture. Fiber-optic face plates have been used to avoid parallax by bringing the image from the inner surface to the outer surface of the tube.

2.2.5.3 Film or Photographic Projection Systems

Large-screen display systems based on projection of photographic images have been used in a number of existing Command and Control Systems and several specific systems have been described in the literature[6,7,8]. In essence, these systems involve:

1) A symbol generator for converting the digital information to a shaped symbol or character on the face of the CRT

2) An image generator for positioning the symbols and generating graphical data on the face of the CRT

3) Processing equipment for exposing film to the image on the CRT, for developing the film, and, if necessary, for making prints

4) Slide or film storage and selection equipment for storing the film images and making them available upon call

5) A projector and screen for projecting and displaying the selected image.

Usually, a multiple projection system is used to permit the simultaneous projection and superimposing of multiple images to generate multi-color displays or to superimpose multiple overlays over a map background. Systems that superimpose three or four independently selected images encounter difficult registration problems in the final projected display. Other systems that contain the multiple images on a single film chip overcome the registration problem, but the image size is reduced and flexibility in selecting the combination of images to be displayed simultaneously is lost. A more recent development proposes the use of a lenticular type film in which three separate color images are contained on the same film image.

A number of the photographic projection systems in current use employ discrete slides as described above, but a few use a continuous film strip to provide more rapid updating of the display and to permit a simpler mechanical system than one in which individual slides are selected independently. The flexibility offered by random slide selection is sacrificed. The continuous film strip type projection system is more suitable to rapid updating of pseudo-real-time displays where the same type of information is displayed continuously but updated rapidly. The individual slide approach is more suitable to situation displays where a large number of different kinds of situations or pictorial combinations are available, any of which may be required at a given time and in any sequence.

The photographic projection type systems are currently the most practical solution to a large-screen display where continuous operation is required. However, because of the relatively slow response time, the inability to display dynamic information, and the mechanical equipment involved, this is not a desirable long range solution. It is believed that this type of system will be obsolete before the 1970 period and should not be considered for a 1970 system.

2.2.5.4 Photochromic Display Systems

The use of photochromic materials offers considerable promise for future display systems[9]. Photochromic materials are organic dyes which become opaque when exposed to ultraviolet light, and return to the transparent state when exposed to heat or infrared light. By coating a transparent film with a thin layer of photochromic material, a "photographic" type media can be produced in which the chemical process is reversible. An image can be exposed with ultraviolet light and erased with infrared light.

The exposed image will decay at room temperature at rates depending upon the particular chemical compound. Typical persistency times for photochromic materials used in display systems range from approximately 2 seconds to 15 minutes. Faster decay times can be obtained but this is usually not desirable for display purposes. Achieving longer persistence times would probably require cooling the image since the photochromic decay is inhibited by cold temperatures.

Photochromic materials exhibit a fatigue characteristic at present, after a few hundred cycles of a particular spot. Red, blue, or green colors can be obtained with a resolving power capability in excess of 1,000 lines per millimeter. The sensitivity varies with the photochromic material but is about 1/3-watt-second per square centimeter. The persistency of the image can be controlled by varying the temperature, the material, or the method of applying the material to the base. The earlier photochromic display systems generated a dynamic display by focusing an ultraviolet light through a lens system onto a photochromic film; the ultraviolet light being mechanically positioned by a servo-mechanism. Since the photochromic material becomes opaque at the point at which the ultraviolet strikes, projection type displays can be generated by inserting the photochromic material between the lamp and the lens of a projection system. Moving the lens through which the ultraviolet light is focused causes the opaque spot on the photochromic film to move, generating a dynamic display on the screen. Shining an ultraviolet light beam through a character-matrix mask permits the generation of alphanumeric characters on the display screen. Special symbols can be generated in a similar manner. This type of display is interesting for tracking a limited number of targets or for generating displays that change relatively slowly. However, the speed of the photochromic material and the mechanical motions involved in deflecting the ultraviolet light limit the speed of this type of device.

In a newer development, a cathode ray tube is combined with the photochromic film to permit the electronic generation of an image. In this development, a fiber-optic face plate cathode ray tube is used to generate an image on the outer surface of the face of the cathode ray tube by conventional techniques. The ultraviolet light from the phosphor on the inner surface of the face of the cathode ray tube is transmitted through the fiber-optic face plate to generate an opaque image on the photochromic film. A dichroic mirror that transmits ultraviolet light and reflects visual light is sandwiched between the fiber-optic face plate and a photochromic film. Visual light from an external source is projected through the photochromic film onto the dichroic mirror which reflects it back to a viewing screen. The opaque image on the photochromic film prevents the light from the projector from striking the dichroic mirror. Hence, this image is reflected onto the screen.

At the present time, the speed of photochromic materials limits the character generation rate to approximately 10 characters per second in this type of display. If work on faster photochromic materials is successful, this approach could provide an attractive all-electro-optical dynamic large-screen display with no mechanically moving parts. Photochromic display systems combining electronic, photochromic, and projection techniques are very promising for use in a 1970 system.

2.2.5.5 Light-Valve Systems

The term light-valve in a generic sense refers to any system in which light passing through the system is modulated. However, the term is usually used in a narrower sense to refer to a cathode ray tube projection display system using a Schlieren optical system.

In a typical system of this type, a metallic mirror-like surface covered with a thin film of oil is placed inside an evacuated cathode ray tube type device. An electron beam is used to generate an image

on the oil film. This is similar to the operation of a normal cathode ray tube except that the image is generated on the oil film rather than on a phosphor face. The electrons impinging on the oil film create electro-static forces that cause a temporary deformation of the oil film. When a high intensity light source is focused on the oil film, the light is reflected at a different angle for those areas that have been deformed by the electron beam than for the remainder of the oil film. Passing the reflected image through a ladder-like grating permits selective passing of the light, depending upon whether it was reflected from a deformed area or a non-deformed area of the oil film. Hence, the desired image is displayed on the viewing screen.

Light-valves are promising for future display systems and will probably be in widespread use in 1970. At present, they suffer from the severe disadvantage of short cathode life (20 to 200 hours MTBF). Since it is necessary to have an oil film inside the vacuum, it is difficult to maintain a good vacuum. As a result, there is a tendency for the cathode to be poisoned by evaporated oil. Light-valve systems of this type are in common use in large-screen theatre-television systems. However, these systems are operated for short periods of time for special events, and considerable time can be allotted prior to the event for bringing the system up to proper operation. Unfortunately, in the military command and control environment, the system is required to be in almost continuous operation. Another disadvantage is that multi-color displays require multiple projection units with a consequent registration problem.

Considerable development efforts are being expended toward improving the performance, reliability, and life of light-valve systems. The Rome Air Development Center, in particular, is sponsoring extensive efforts toward improving light-valve systems. It is their belief that light-valve projection systems will constitute the next generation of large-screen display systems. It is likely that projection light-valve systems will constitute the next generation of large-screen display systems, but this is an interim solution. Such systems will probably be surpassed by other techniques for a system designed for 1970.

2.2.5.6 Electroluminescent Displays

The major applications of electroluminescent materials in display equipment so far have been in the form of individual character or symbol indicators[11]. In these devices, each character position in an alphanumeric display is represented by an electroluminescent panel which can be caused to display any one of a predetermined set of characters depending upon the electrical signals applied to the device. However, extensive research and development efforts have been devoted to the use of electroluminescent materials to fabricate a complete display screen capable of displaying graphical data as well as alphanumeric characters.

Electroluminescent displays offer the advantages of an all-solid-state display without moving parts or projection optics, a flat display requiring very little depth, and sufficient brightness for viewing under normal ambient room lighting conditions. An electroluminescent element consists of a thin layer of phosphor powder that is embedded in a dielectric medium and sandwiched between two parallel plate electrodes, one of which is transparent. The application of an alternating voltage to the electrodes causes the phosphor to emit light.

Aside from the discrete character display, the electroluminescent display which has been developed further than others to date has been the electroluminescent crossed grid display[12]. This display uses a continuous electroluminescent sheet with the electrodes on one surface subdivided into parallel strips in the X direction and with the electrodes on the other surface subdivided into parallel strips in the Y direction. Applying excitation to an X and a Y strip will cause the electroluminescent material to emit light at the intersection. In this XY selection, each wire carries approximately one-half the

voltage necessary to excite the electroluminescent material so that full excitation voltage occurs only at the intersection. A continuous sheet of non-linear resistor material is coated on the electroluminescent material between two sets of electrodes to avoid partial excitation and partial light at points along the selected X and Y strips other than the point of intersection.

This approach is useful for a large-screen or console type display. Real-time dynamic displays, such as target tracks, can be generated by properly sequencing the selection of X and Y grids. Alphanumeric characters and symbols can be drawn on the same display. However, it is necessary to regenerate each spot on the display periodically since it has no storage characteristic. As a result, this type of display requires either an external storage or computer controlled regeneration. To avoid noticeable flicker, the picture must be regenerated at least 30 times per second. The frame rate of 30 per second, and the fact that 1 - 5 microseconds are required to energize each spot on the display, limit the total number of positions that can be activated. Periodic action is required for active spots that remain static as well as for those that are changing.

One display of this type provides a 256 x 256 matrix in a 16 x 16 inch display panel. This display panel is $3\frac{1}{2}$ inches thick. The spot size is approximately 1/10 of an inch. It is expected that spot sizes of 1/40 to 1/50 of an inch are realizable in the near future, and that 1/100 of an inch is feasible.

In another type of electroluminescent display, a continuous sheet of electroluminescent material is deposited over a sheet of piezo-electric ceramic[13]. With the proper voltage applied to the electroluminescent material, a mechanical shock wave travelling through the piezo-electric ceramic can generate sufficient voltage to energize the electro-luminescent material in the vicinity of the shock wave. Introducing

a shock wave to one edge of the ceramic causes a light signal to propagate across the electroluminescent material as the shock wave propagates across the ceramic beneath it. A reduced shock wave on one edge, combined with a shock wave on a perpendicular edge, can cause a point of light corresponding to the intersection of the two wave motions to propagate across the display. A non-linear resistor material is again used to suppress partial excitation. Controlling the time of the two shock waves provides the ability to position the spot of light as it moves.

A third approach to electroluminescent displays can provide a dynamic large-screen display that does not require periodic regeneration. In this approach, the display screen is fabricated with a matrix of discrete electroluminescent elements, each having an associated storage element. An XY selection matrix is used to energize a specific electroluminescent element. The associated storage element then maintains the electroluminescent element in that state until it is cut off by another XY selection operation. At present, the addressing rate is limited to a switch-on time of approximately 10 microseconds per element. The switch-off time is approximately 30 microseconds, but it is not necessary to maintain the electrical signal for this length of time. It is anticipated that the switch-on time can be reduced to 5 microseconds in the near future. Resolving powers of 10 lines per inch can be realized now with16 - 20 lines per inch considered feasible in 1970.

This approach provides a true dynamic large-screen display with exact registration and positioning without mechanically moving parts and without an optical projection system. Since the individual storage elements eliminate the necessity for periodically regenerating the picture, only those elements that change must be activated and energized or de-energized.

A multi-color display would be difficult but is conceivable by segmenting each element of the display into three elements corresponding to a three color system. This type of display would be quite expensive due to the electronic selection of individual elements and the electronic

storage associated with each element. However, it is a practical display in that a dynamic large-screen display of this type can be built in a relatively short time with a high assurance of success. Future developments in integrated circuit techniques may lower the cost of the electronic elements sufficiently to make this approach attractive for a 1970 system.

2.2.5.7 Opto-Magnetic Displays

A different approach to solid-state displays is based on the magnetic properties of certain thin-film materials that affect their reflection of light. If a thin-film of magnetic material of this type is deposited on a substrate, areas that have been magnetized will reflect light in a different way than other areas of the film. An XY matrix selection can be used to generate a magnetic image on the surface. If a high intensity light is projected on the magnetic film, a visual image will appear as the result of the effect of the magnetic image on the reflection of the light.

Contrast ratios of 75 to 1 have been obtained, providing a good display under normal ambient light conditions. Only a few percent of the incident light is reflected. Resolutions in the order of 5 mils have been obtained in the laboratory. The intensity varies with the viewing angle but there is very little variation within angles of approximately 90^{o}.

This is an interesting approach to a dynamic large-screen display, but it is too early in the development stage to determine with confidence whether it will be available and feasible for a 1970 system.

2.2.5.8 Crystal Light Modulators

A projection display device using a birefringent KDP crystal element has been proposed[14]. An electron beam in a cathode ray tube is used to control the passage of light through a KDP crystal in the face of the tube. This permits a system in which a polarized light is projected through a rear window in a cathode ray tube and then through

the crystal modulating element in the face of the tube and onto a screen. The electron gun in the cathode ray tube generates an image on the crystal modulator, the polarized light passing through the modulator then projects this image onto the screen. This approach is being followed with interest, but there is no indication at this time as to whether it will be feasible for a 1970 system.

2.2.5.9 Laser Luminescent Display Systems

Conceptually, a large-screen display can be generated by writing on a luminescent screen with a laser beam. This would be somewhat equivalent to an "outdoor" cathode ray tube in which the laser beam replaces the electron beam and the luminescent screen replaces the phosphor coating and the face plate of the tube. This approach would offer an advantage over a cathode ray tube in that a vacuum is not required and a large-screen image can be generated directly. The difficulty lies in the deflection of the laser beam. However, a number of development efforts have been aimed at this problem with some laboratory success[15]. An operational system of this type may not be developed by 1970, but it offers long range promise. Continuing efforts in the development of improved lasers and advances in the ability to deflect laser beams will contribute directly to the ultimate success of this type of display.

2.2.6 Display Availability in the 1970-80 Period

The investigation of display systems has not progressed far enough at this point of the study to permit a complete determination of the availability of different types of display systems in 1970. From the investigations to date, it is believed that film-based photographic projection systems and mechanical inscribers will be obsolete. Light-valve projection systems will be in widespread use but may be phasing out by 1970. Cathode ray tubes will continue to be a dominant factor in the generation of displays and in console viewing screens.

Electroluminescent and photochromic systems offer promise for 1970-80 systems. Ferroelectric and opto-magnetic displays offer possibilities depending upon the success of current development efforts. Laser display systems appear to offer great promise but significant research and development efforts are required.

2.2.7 Limitations of Present and Planned Displays

Most of the present large-screen displays are limited by the use of electro-mechanical film based projection systems. Photochromic and electroluminescent displays are currently limited by the rate at which individual positions can be altered. Light-valve systems are limited by short cathode life. It is not possible at this point of the investigation to discuss the limitations of future display systems.

2.2.8 Recommended Developments to Meet ANTACCS Needs

Development efforts sponsored by the Navy to meet ANTACCS needs for the 1970-80 period should be concentrated on solid-state techniques that are adaptable to both fabrication methods. Electroluminescent, opto-magnetic and laser displays appear to be the most fruitful areas for development efforts pointed toward the 1970-80 period.

2.2.9 The Evaluation Criteria Recommended

Characteristics and parameters to be considered in evaluating display systems should include the following:

Display technique
Display media
Console or large-screen
Static or dynamic
Hard copy
Legibility
Color
Brightness
Screen Size
Resolution
Frame generation rate
Response time
Character generation rate
Character generation technique
Image storage capability
Image storage method
Storage and regeneration requirement
Capacity

Character repertoire
Character size
Symbol shapes
Accuracy of position
Registration
Stability
Color capability
Contrast
Image quality
Optical quality
Processing requirements (if any)
Image handling requirements
Accessability
Background illumination permissible
Viewing distance
Physical space requirements
Weight
Power Requirements

It will not be necessary to make detailed comparisons and evaluations of each of these characteristics since many of them are common to most display types. Such characteristics would be used to rule out a limited number of displays that do not posses the characteristic. Other characteristics might be common for most displays but a unique property of a specific display technique could enhance this characteristic to offer a strong advantage to that technique. Those characteristics that vary significantly from display to display, but within acceptable limits, will be compared to permit evaluation of the characteristics of acceptable display technologies.

2.2.10 Conclusions and Recommendations

Only brief preliminary conclusions and recommendations can be made at this time. Emphasis should be placed on the development and use of solid-state displays that do not require periodic regeneration and on batch-fabrication of display screens and arrays.

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2.3 DISPLAYS--USER TECHNOLOGY AND SOFTWARE

2.3.1 Introduction

2.3.1.1 Objective

Real time data processing systems have become an important point of interest. The development of digital transmission systems and the availability of bulk data storage devices have stimulated the use of on-line systems in which information is entered into the data processor as it is generated, and outputs are requested from the computer as they are required, and in fact limited to that information needed at the moment. The on-line concept established a requirement for an intimate relationship between man and computer--one in which not only the characteristics of the computer are important, but where equal concern must be given the communication devices by which man interacts with the system. This study is concerned withthe application of on-line displays to military command and control.

2.3.1.2 Historical Review and Perspective

Perhaps one of the first display devices associated with a computer system was the simple cathode ray tube (CRT) display. For example, such a device was available in 1953 on the ILLIAC (University of Illinois) computer where two tubes were driven in parallel. One CRT was mounted for visual observation whereas the second was associated with a camera capable of photographing the computer generated display. The computer controlled the film advance. While the primary use of this device was the rapid generation of graphic information, another use was the on-line monitoring of the progress of a calculation by the programmer. By appropriate displays, he was able to detect programming errors or, during production runs, make better initial guesses during iterative procedures or parameter studies. This was perhaps one of the first on-line display devices.

It is important to define what constitutes an on-line display device. From many points of view, all of the following can be considered as display devices:

Typewriter
Plotter
Printer
Closed circuit TV
Document viewers
CRT consoles

For purposes of this investigation, however, we limit considerations to essentially two types of devices, the single operator console and the group display. These must satisfy the following criteria:

1) Directly tieable to data processing system.
2) Ability to initiate messages or control signals from a data entry keyboard or switches for transmission to the computer.
3) Ability to receive messages or control signals from the computer and display them to the operator or viewer.

"Off-line" devices are included if they receive information which is computer generated. Conventional printing and plotting equipment, however, are excluded. So are document viewing devices associated with the information retrieval problem. These devices generally operate on reference libraries and not on digitized data.

Based on the above, the typewriter station, the keyboard with CRT console and the large screen viewing system are the basic items applicable to this study.

2.3.1.3 Typical Systems and Operating Modes

SAGE

Perhaps the first, or at least most well-known display system was that associated with the SAGE System. The operating principle in SAGE Direction Centers is the interplay of man and computers via display consoles for the purposes of making a composite number of simple decisions concerning the air threat at any instant in time. To do this, geographic information is presented by the computer to the console operator on a volatile CRT screen, and the human responds to the machine by operating a light gun and button keyboard. Alarms

and alerts, in both audible and visual form, are available. In a typical center, there are close to one hundred consoles. Depending upon the function, the console features differ from one another, there being over a dozen "special purpose" configurations. Operating characteristics have been cited where the computer reads up to 5000 console switch actions every 2.5 seconds. During this period, 200 different displays may be generated consisting of 20,000 characters, 18,000 points and 5000 lines.

Typically, a console has a 19 inch Charactron tube and a 9 inch Digitron tube manufactured by General Dynamics/Electronics and Hughes respectively. The larger scope is used as a situation display capable of showing alphanumeric characters and lines, whereas the small CRT is a data summary display capable of only alphanumeric information. Whereas the former leads to considerable flicker to the casual observer, it is maintained that operational personnel who are subject to a special environment of blue light find no problem in working with the displayed information.

In the SAGE System, on-line devices first came to be used on a large scale. The significant application principle here is the use of the console in the area of computer assistance where human judgment can be applied.

NORAD

Another area of interest in the application of display techniques and devices is NORAD.

The current NORAD Complex at Colorado Springs (apart from the plans of 425L) include two major installations, the Space Detection and Tracking System (SPADATS) and the Combat Operation Center (COC). The display devices and techniques used here are:

SPADATS - a) 5 ft. x 6 ft. wall map of the world with pins showing locations of sensors, communication elements, and data processing stations.

b) Tote board presenting tabular information of all space vehicles currently in orbit. Manual updating of perigee, apogee, period, etc. is performed daily.

c) Closed circuit Wollensak TV for transmitting parts of the display on the tote board to other operation rooms.

COC - a) Large screen of the North American continent capable of showing tracks. This system uses the Iconorama projection system which automatically updates film chips from teletype messages.

b) Smaller screen devoted to showing the BMEW's system on a map background of the Arctic region.

c) Weapon Status Board - registers which display the status of forces.

Of considerable interest here is the Iconorama system which is perhaps the first on-line, multi-color, group display system to be installed. The NORAD System generates information which can be displayed in the following additional sites:

Joint War Room, Pentagon
Air Force Command Post, Pentagon
SAC Command Post, Offutt Field
Canadian Joint Chiefs of Staff
National Resource Evaluation Center

Air Force Command Post

The display activity to data at the Air Force Command Post has been limited to several rear projection screens capable of showing slides and films. Perhaps the most dynamic display is the Iconorama System which is fed by NORAD. In addition, there are status boards exhibiting the defense conditions (DEFCON). Also there is a Bomb Alarm display which consists of a map of the United States consisting of colored regional blocks. Upon an indicator going off, an appropriate light goes on behind the map and lights up the endangered area.

During the spring of 1962, this system was augmented by the first stage of the 473L program called the Operational and Training Capability (OTC) phase. This was implemented by IBM Federal Systems Division by the Introduction of the IBM 1401/1405 (disc) systems together with the DC400B/DIB display and interrogation system of Thompson Ramo Wooldridge.

The latter system consisted of two RW consoles having single 10-inch CRT displays together with a sophisticated keyboard. Of these, one console was a remnant of earlier equipment while the second console was a newly manufactured copy. Both consoles were interfaced with the 1401 by use of a Display Interface Buffer which is a core storage device. These consoles were to be used in the Command post by placing them at the disposal of the various area desks as an on-line tool for information retrieval and analysis. The following functions were selected for this initial application:

Emergency Actions
Defcon Actions
Plan Abstracts
Flight Following
Status of Forces
Airfield Facilities
Aircraft and Missile Characteristics

The purpose of the OTC was twofold: to achieve some automated capability rapidly; and to experiment with equipment and techniques in anticipation of the next phase of 473L development. The latter point motivated the interest in on-line display devices so that experience would be obtained for design of the Interim Operational Capability.

4) Defense Communication Agency: Defense National Communication Control Center

The Defense National Communications Control Center (DNCCC) is the focal point for the controlling and supervising function of the Defense Communication Agency over the Defense Communication System. The latter encompasses all of the telecommunication requirements for the Department of Defense. The basic function of the DNCCC is the maintenance of world-wide communication traffic status. In this capacity three basic on-line displays are generated to show operational conditions; traffic status, system status and read-out panel.

These displays are computer driven, wall-lined panels. The first two are static in composition, that is, they are fixed format displays on which status is demonstrable by the manipulation of colored lights as generated by the Philco 2000 computer system.

The System Status panel is an 8 ft. x 15 ft. map of the world on which are etched major trunk lines and system relay stations for which the back lighting can be red, green or yellow.

Another panel is the Traffic Status Board which is an 8 ft. square display. It consists of four bays of nine columns each, showing station backlog status by use of coded illuminators opposite each identified station.

Finally there is a readout panel which is a 7 ft. square rear projection display. This display can present tabular and textual information generated by the computer as a result of an inquiry. The process incorporates a modified Anelex High Speed Printer which generates text on special material from which a film transparency is generated by non-chemical means. This film is sequentially added to and is, therefore, spool fed and wound with 70 characters per line at 100 lines per minute. The letter image is 1 inch high, and is large enough to be read at 25 ft. distance in a room with ambient lighting of 25 ft. lamberts.

These three display devices are tied together through a System Supervisor Console which is under the control of the human operator. The console serves both to initiate queries of the system and to display results via the station lights, typewriter, and printer stations.

In addition to the above, there are three special Network Boards including the station and trunk conditions for the CRITICOMM Network, the JCS Voice and Teletypewriter Network and the JCC Network.

Operational experience has shown that the read-out display has found very little use. This is probably due to the lack of requirement for large group display of textual material.

The DNCCC represents stage one of the development of the Defense Communication Control Complex.

The current DCA procurement is expanding the Control Central Complex by adding to the DNCCC four area control centers, called Defense Area Communication Control Center (DACCC), and five regional control centers, known as Defense Regional Communication Control Centers (DRCCC). Those centers will perform on a decentralized basis, many of the same kinds of functions performed at the higher level DNCCC. In particular, they will be more responsive to local problems and system management.

The display requirements for the DACCC have been spelled out considerably and serve as an example of what is currently demanded. Specifically, a visual display is specified which will exhibit "in a completely unambiguous manner" current operationsl status. To this end the following guide lines are parameters by which a responsive display system was to be proposed:

a) Alteration: Ability to make changes to the display within 4 hours per unit change and without removing the display from normal service.

b) Expansion: Have a residual capacity to allow a 25% increase in information displayed.

c) Legibility and Resolution: Permit personnel with 20/20 vision and normal color perception to comprehend the large wall displays and small individual displays at 15 ft. and 30 inches respectively.

d) Information Content: Of twenty information items, eight are semi fixed and 12 are variable. The average frequency of change for these items varied from a low of 15 minutes to hourly for 13 items, and infrequently for the remainder.

2.3.2 Application Technology in Command and Control

The technology of integrating man/machine communication devices must take into consideration both programming and user techniques. The former is concerned with achieving system operation and the latter with the design of proper operating procedures.

Always the on-line application and problem characteristics must be understood to arrive at an economical system.

2.3.2.1 Man/Machine Coordination

There is close interrelationship between man and machine in a command and control environment. During both pre-attack and post-attack times, the machine receives information from communication devices and displays it. The man analyzes the incoming information as to the status of his forces and those of the enemy. The machine receives additional information and updates the situation display. The man evaluates the military situation based on the information the machine has displayed. In so doing, he makes requests of the machine to which the machine responds, since it is impossible for the system to cover, under normal output procedure, data reflecting all contingencies in which the commander might be interested. The man identifies certain courses of action, and the machine computes hypothetical effects based on the various possible choices. The man makes the decision and the machine communicates the commands and records them.

The function "computes hypothetical effects" is probably futuristic. At the present time, there is little real-time or operational war gaming capability in command systems to help the commander make his decision during the actual post-attack period.

Figure 2-1 refers to the overall command function. There are obviously many support functions which require close man/machine coordination.

To fix the user concepts, it is convenient to illustrate by an actual example indicative of a commander's requirements. Consider the problem of interrogating the information files in a system. If these files contain status information regarding forces and resources, then some typical interrogations of the system might be:

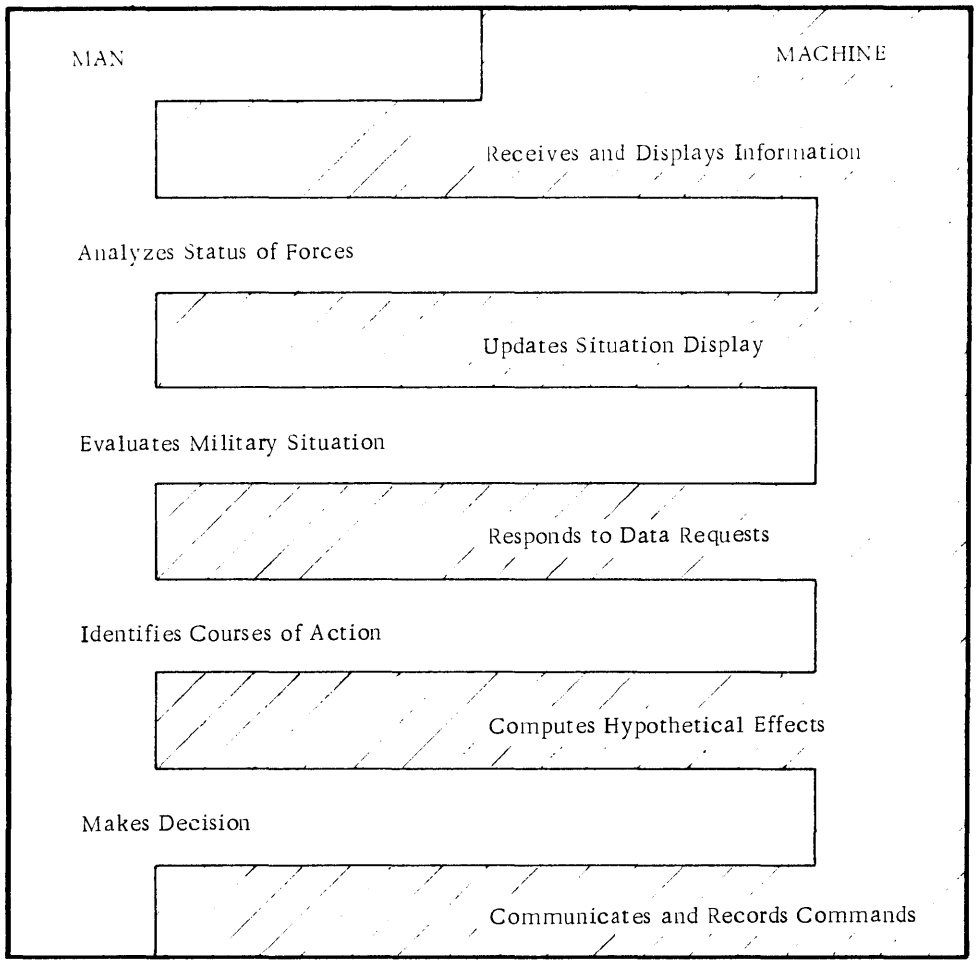


Figure 2-1 MAN/MACHINE COORDINATION

1) Tabulate all POL facilities on Russian and Chinese Bomber Air Bases whose capacity is greater than 500 metric tons of jet fuel.

2) List all NATO air defense bases with a probability of survival greater than 0.85.

3) List all Navy Bases with a greater than 75% probability of survival and whose residual capacity of P02 is greater than 20%.

The conventional procedure in fulfilling these requests is for the consumer to fill out a request form and then await the manual and machine steps, shown in Figure 2-2, to be completed. The computer input format required in step 4 typically demands a trained specialist to convert the free text and terminology used by the requestor to machine understandable nomenclature and fixed form. This process requires table look-ups and transcription from code books, indexes and tables of acceptable terms.

Disadvantages encountered in this process are:

1) Need to carefully adhere to spelling and to form; for example, abbreviations, plurals, possessives, etc. may be excluded.

2) Use of special words. Synonyms may be prohibited. The terminology of users varies so that a common vocabulary acceptable to all is impossible.

3) Punctuation. The compounding and marking off of segments of the query may lead to logical errors.

4) Need to learn special rules and codes. Change of codes will affect all users at the problem originating level.

The on-line display console permits a short circuit of almost all of these steps by providing the consumer with a direct entry on the files. Not only are time delays eliminated by the simple brute force approach of by-passing at least eight manned stations, but some of the inconveniences of maintaining security and generating possible errors at each point are also avoided.

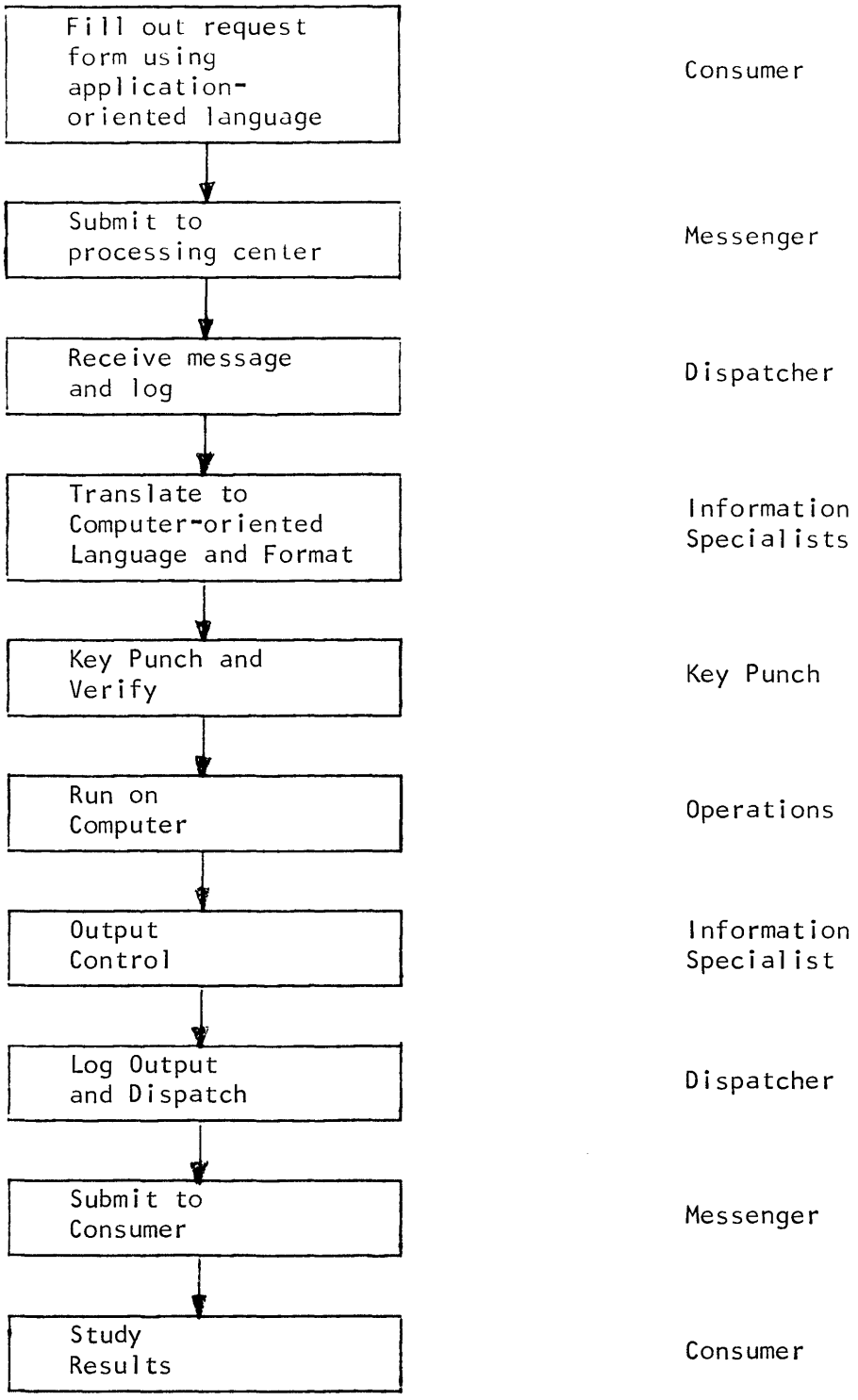


Figure 2-2

OVER-ALL COMMAND FUNCTION

CONVENTIONAL PROCEDURE IN REQUEST FULFILLMENT

The advantages of this approach are:

1) Direct consumer/system interface

   Fast service
   No intermediaries that can cause errors or delays
   Complete control
   Remote operation
   Direct response

2) User oriented language

   No code books
   No dictionaries
   No syntax rules

3) Error checking and control

The procedures that may be employed with the displays under discussion here are illustrated in the following example. Assume that the display console keyboard includes the labelled buttons:

Military installations
Geographical limits
Political limits
Owner limits
User limits
Current totals
Amount degraded
Residual capacity
Hard-copy output
CRT output

The steps in entering query (1) are:

1) Pressing military installations, the display given in the Figure 2-3 is presented. The operator selects AIR BASES.

2) The selection of one item, AIR BASES, causes a second display to appear automatically as shown in Figure 2-4. The operator selects BOMBER.

3) The selection of BOMBER causes a third display to appear as shown in Figure 2-5. It represents the possible choices in selecting attributes about Bomber Air Bases. The sample query dictates that the operator choose FUEL STORAGE.

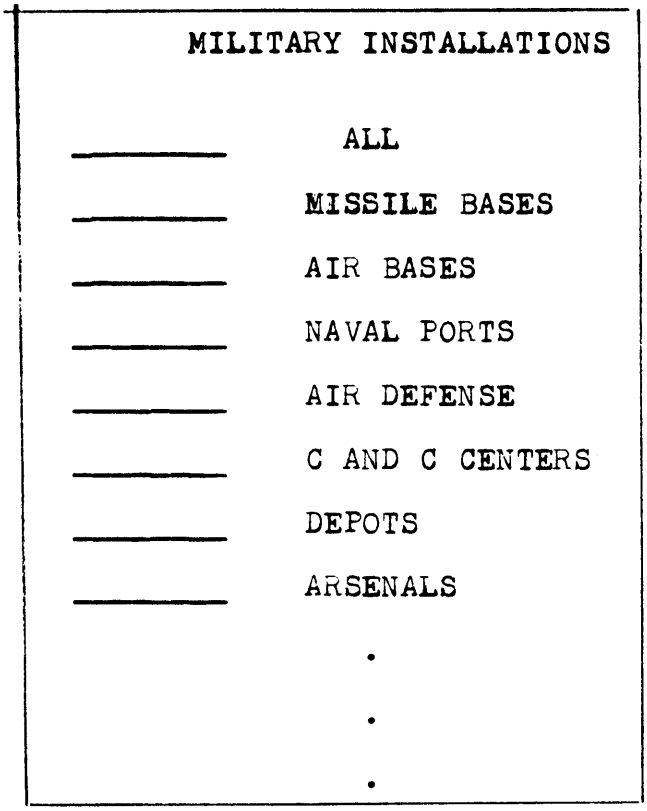


FIGURE 2-3
LIST DISPLAY OF MILITARY INSTALLATIONS

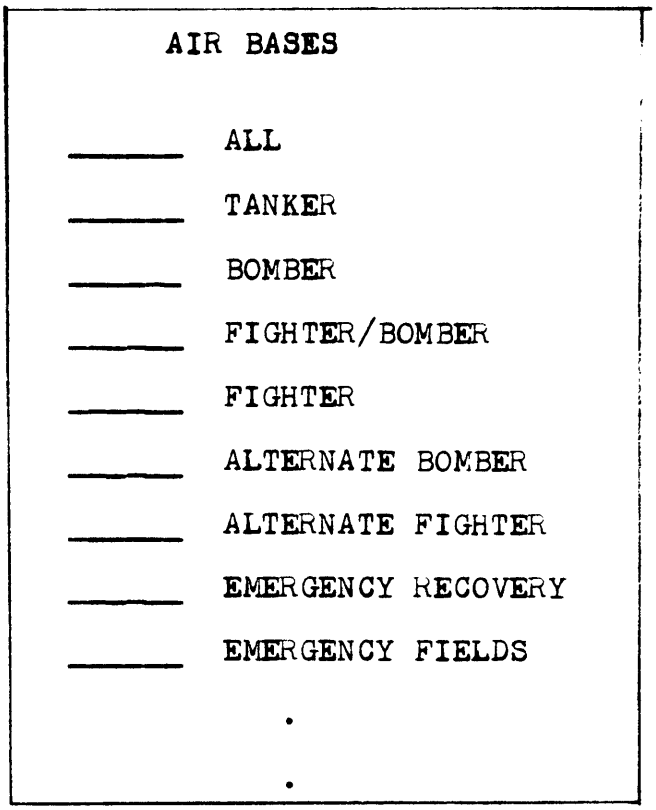


FIGURE 2-4
LIST DISPLAY MODIFYING MILITARY INSTALLATIONS

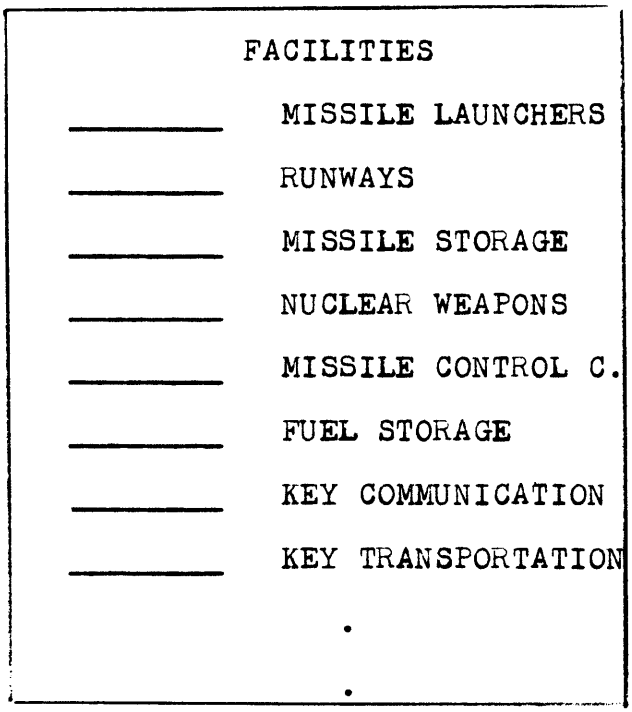


FIGURE 2-5
LIST DISPLAY MODIFYING BOMBER AIR BASES

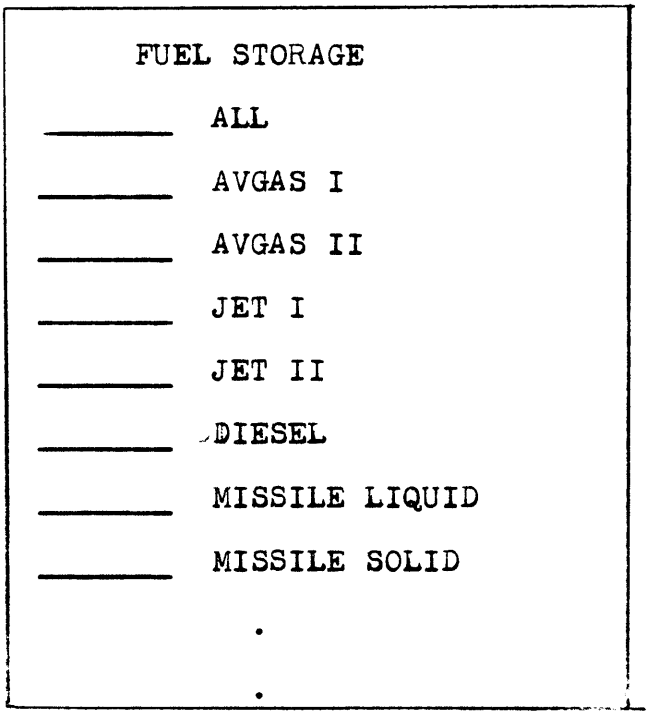


FIGURE 2-6
LIST DISPLAY MODIFYING FUEL STORAGE

4) The next display, shown in Figure 2.6, modifies Fuel Storage and two selections are made, JET I and JET II, completing this sequence of displays.

5) The next function key pressed is one labelled Political Limits. This causes the display shown in Figure 2-7 to appear. From it, two selections are made; RUSSIA and CHINA.

6) Next, Current Totals is pressed, causing a format display to appear as given in Figure 2-8. The operator will insert 500 in the third blank.

Having completed the entry of the query, the operator now selects the output media. This choice will be dictated by urgency for results, amount of detail desired, size of list likely to be generated, and desire for permanence of copy. The selection of either of the output media will terminate the request procedure and cause the request item to be added to the internal processing queue.

POLITICAL LIMITS

_____ RED

_____ BLUE

_____ NEUTRAL

_____ U.S.

_____ RUSSIA

_____ CHINA

_____ TREATY GRPS

_____ BLOCS

_____ NATIONS

FIGURE 2-7
LIST DISPLAY, POLITICAL LIMITS

TOTALS

SELECTED BY PER CENT

GREATER.....

LESS .....

SELECTED BY AMOUNT

GREATER.....

LESS .....

FIGURE 2-8
FORMAT DISPLAY, CURRENT TOTALS

2.3.2.2 Problem Characteristics

Typical problem characteristics associated with on-line display systems are as follows:

1) Real-time - this refers to both the performance of the total problem and the responsiveness of the system to individual operator action. By definition, since operator response and action is involved, real-time is measured in human terms. Two different operations are identified. The first involves entry of information, under program guidance, to make up a complete message or action request. The second is the processor response to the message.

An example of the former is the step-by-step composition of a message by use of a keyboard or function keys as described in the previous section. Typically, each key generates one or more characters of information which are collected, operated on and stored by the computer. Pressing a key may also cause a display to be generated, providing guidance for the next stop, or requiring the filling in of further information. This mode of operation must permit the operator to enter data at his own speed, which effectively means that he must be permitted to press keys at a 60 word per minute typing rate or within 200 millisecond intervals.

The second aspect of response is the fulfillment of a particular request by the processing central. The total action may involve:

Request validation
Information retrieval
Information transformation
Data formatting
Output generation

Depending upon the specific application, the response time required of the system may vary from a few seconds in a command and control system to several minutes for an inventory search. In one particular strategic command and control system the response times for fulfilling requests were specified as shown in Table 2-1.

	Form of Output Presentation		
	Hard Copy	Console	Group Display
Individual	10-30 minutes	3-10 sec.	X
Group	X	3-10 sec.	30 seconds

TABLE 2-1 - Response Time for Fulfilling Requests

2) Random Transactions - Since the input associated with display devices is generated by people, and the reaction time to outputs is dependent on people, the system transactions observe no fixed time pattern or schedule. Hence the processor must be capable of supplying random servicing of the on-line stations.

3) Large Storage Capacity Requirement - Systems with on-line displays invariably involve much information in the form of a data base in data handling applications, or as a program library in scientific computing. Otherwise, on-line devices can hardly be economically justified. Since man and his judgment are involved, there is a requirement that this information be randomly accessible. Hence bulk storage media and their efficient utilization are important in system design.

4) Many Stations - typically, the on-line system will have many transaction stations. For example, a logistics system may involve thousands of inquiry sets, while a CIC will include dozens of consoles. Multiple users compete for servicing from the central processor.

5) Independent Functions - As well as many users operating in parallel, individual functions or tasks vary from one station to the next. For example, in NTDS, many different operations are defined, any of which may be initiated at any of these stations.

6) File Access - The multi-functions and multi-users operate on common files. Hence, file order and file integrity must be maintained. The latter is a problem since the functions operating in parallel can be both extracting information or modifying the data base at the same time.

2.3.2.3 The Naval Application

In Figure 2-9 there is shown schematically the data processing system from the point of view of the commander. He receives information from the machine; from console displays and group displays, and from hardcopy print-outs. Console displays reflect the working display to help prepare and format group displays and to react to particular requests of the commander. Group displays represent the major standard output to the commander reflecting tactical situations, i.e. situations which change rapidly. Hardcopy output represents the back-up data which is frequently used for reference in this perspective. The data processing system itself is simply a "black box" from the commander's viewpoint.

The most important aspect from the standpoint of the commander is that he must communicate with the machine in his own language--the military language. This implies that the hardware and the procedures providing the input/output to him must be so designed to allow this. Communication with the machine in a programmer's language, totally foreign to the military man, is unacceptable. There must be an intermediate translation from the military language to the language of the console displays, group displays, or hardcopy print out.

The "commander" in the above paragraphs is used in a generic sense. It is meant to include the commander's staff activities and all support functions necessary to the mission.

2.3.3 Hardware Aspects from the User's Point of View

2.3.3.1 Equipment Features

2.3.3.1.1 Display Console Features

To illustrate the principles of the techniques and operating concepts to be presented in this section, it is well to define a typical display console in terms of the capability and tools it affords the user/operator. The following features are assumed:

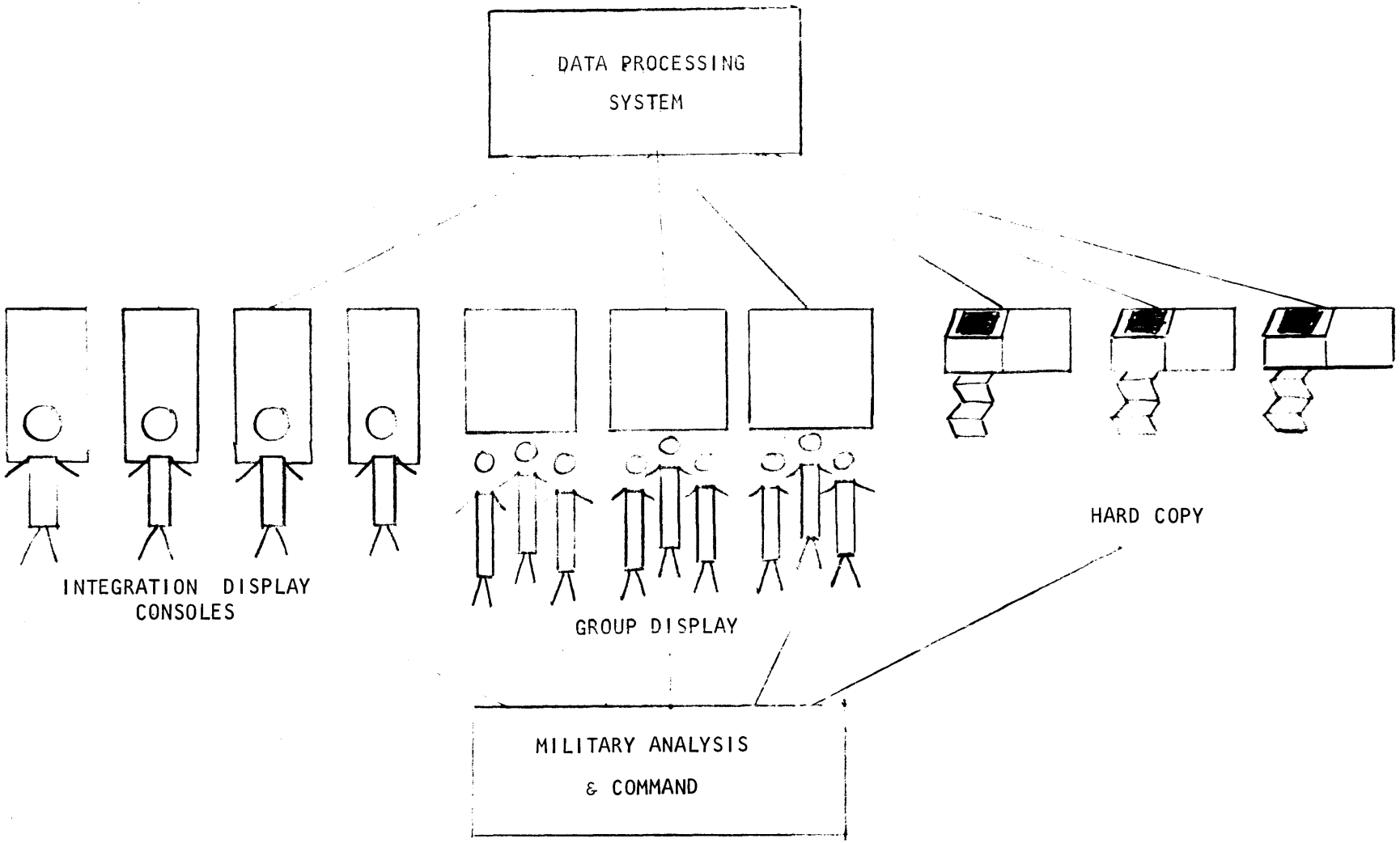


Figure 2-9 SCHEMATIC OF COMMANDER'S DATA PROCESSING SYSTEM

1) Alphanumeric Keyboard - This consists of a set of keys comparable to a standard typewriter keyboard. In addition to the letters and figures, punctuation and special symbols will be included. There are usually sixty-four possible characters available since 6 bits are conventionally used for symbol representation. Since there are 43 keys on a typewriter, this implies the need for a shift key or augmented keyboard.

2) CRT - A readout unit capable of displaying a set of characters or symbols with line drawing as a possible option. There is typically a one-to-one correspondence between the symbols available on the alphanumeric keyboard and those that can be generated with the CRT.

3) Function Keys - This set is dedicated to application-oriented procedures. Single keys may represent a call for an action, or groups of keys may be tied together to form a message calling for an action. To make the device general purpose or multi-purpose, it is desirable to have the significance of these keys vary on demand of the operator. One convenient way to achieve this variability is by a replacable mask or overlay as is done in at least several commercial products such as the Bunker·Ramo BR 85, IBM 4554 and ITT Integrated Console.

4) Status Indicators - System status, both internal computer and console, is shown by status indicators. These indicators may be labeled neons; their on or off condition show status.

5) Alarm Indicators - Alarms or error indications are conveyed by a set of labeled neons. Buttons may be associated with these lights so that operator recognition and resetting can be accomplished.

6) Control Keys - These keys are dedicated to general tasks and support functions by which system control, data entry, and status requests are made.

7) Light Gun - This is a hand-held photoelectric device by which the user/operator can index any symbol on the CRT.

We illustrate typical assignments to some of the panel elements:

1) Alphanumeric Keyboard

Alphabet
Numbers
Punctuation
Special Symbols
"Carriage" Control
Shift Control

2) Control Keys

Hardware Configuration Control
On-line system Function Control
Queue Control
Display Control

3) Status Indicators

Equipment Status
Queue Status
Processing Modes

4) Alarm Indicators

Data Errors
Procedure Errors
Equipment Alarms

2.3.3.2 Equipment Operating Concept

2.3.3.2.1 Console Operating Concept

The basic operation of the display console is in sequencing through the Function Keys. A desired action is defined by pressing an individual key, or more typically, a group of keys in some ordered sequence.

The following events represent a typical operating pattern:

1) Press key i
2) Get positive response that key i was pressed
3) Computer presents a display on the CRT
4) Enter data into display
5) Visually validate inserted data
6) Make corrections to inserted data if necessary
7) Signal end of entry

The actual sequence followed by the operator for a particular key is shown in Figure 2-10.

While this sequence of operator events is underway the computer engages in a number of actions paced by the speed of the operator. These steps are shown in Figure 2-11.

2.3.3.3 System Configurations

There are several possible methods for tieing the on-line display device to the computer. The appropriate method for each application must be determined during the system design when the system equipment is being specified. The various configurations are illustrated in Figure 2-12. It should be noted that for a given system, not all of the configurations illustrated may be possible. The remainder of this section is a brief description of each configuration.

Configuration	Description
a) and b)	The on-line device is connected to a buffered or unbuffered computer I/O channel. Additional devices may be connected to the same channel up to some maximum number. Then additional devices must be assigned to another channel.
c) and d)	The on-line device is connected to a separate buffer unit which in turn is connected to the computer via an unbuffered or buffered I/O channel. Additional on-line devices may be connected to the buffer unit up to some maximum number.
e) and f)	The on-line device is connected to its own buffer unit which in turn is connected to the computer via an unbuffered or buffered I/O channel. Each on-line device requires a separate buffer unit.

The separate buffer units appearing in configurations c), d), e), and f) perform such functions as automatic CRT display regeneration and character-by-character message accumulation for subsequent transmission to the computer or on-line device.

Operational examples of these configurations include the following: DODDAC uses configuration a) with the CDC-160 computer. System 473L uses configuration c) with two consoles and the IBM-1401 computer. Configuration c) was used at Ramo-Wooldridge for the RW-400 computer and for the IBM-7090 computer.

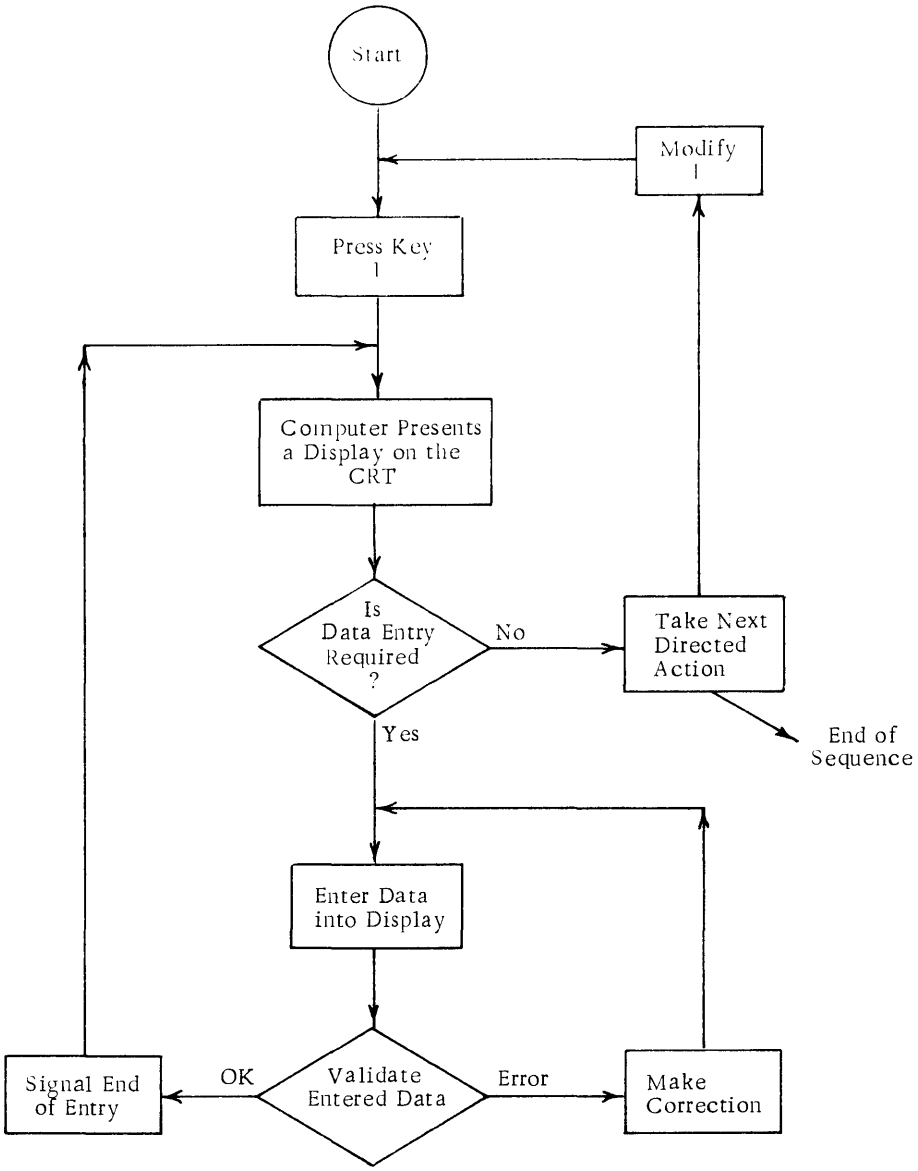


Figure 2-10

Typical Operator Steps in Use of Function Keys

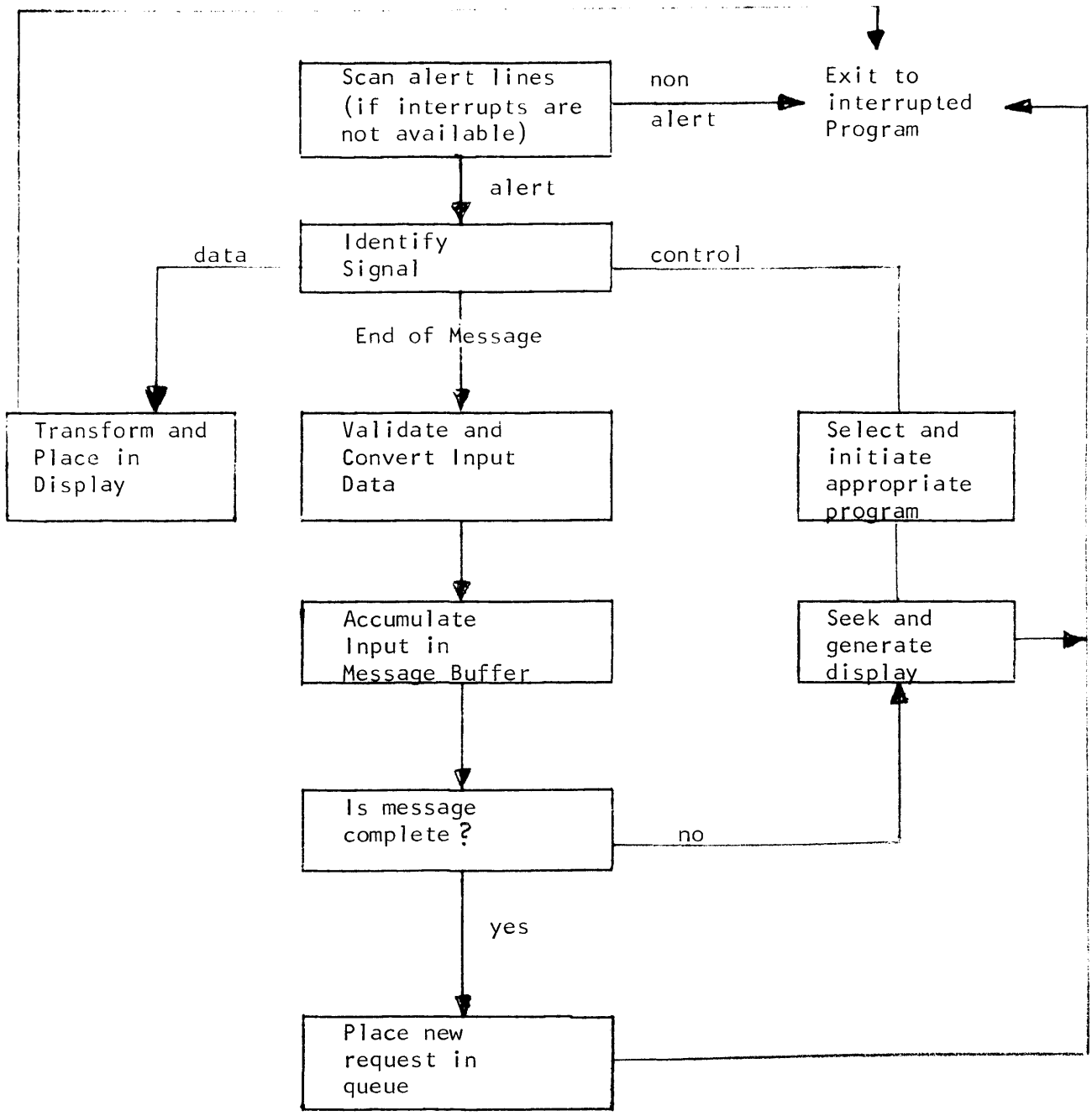
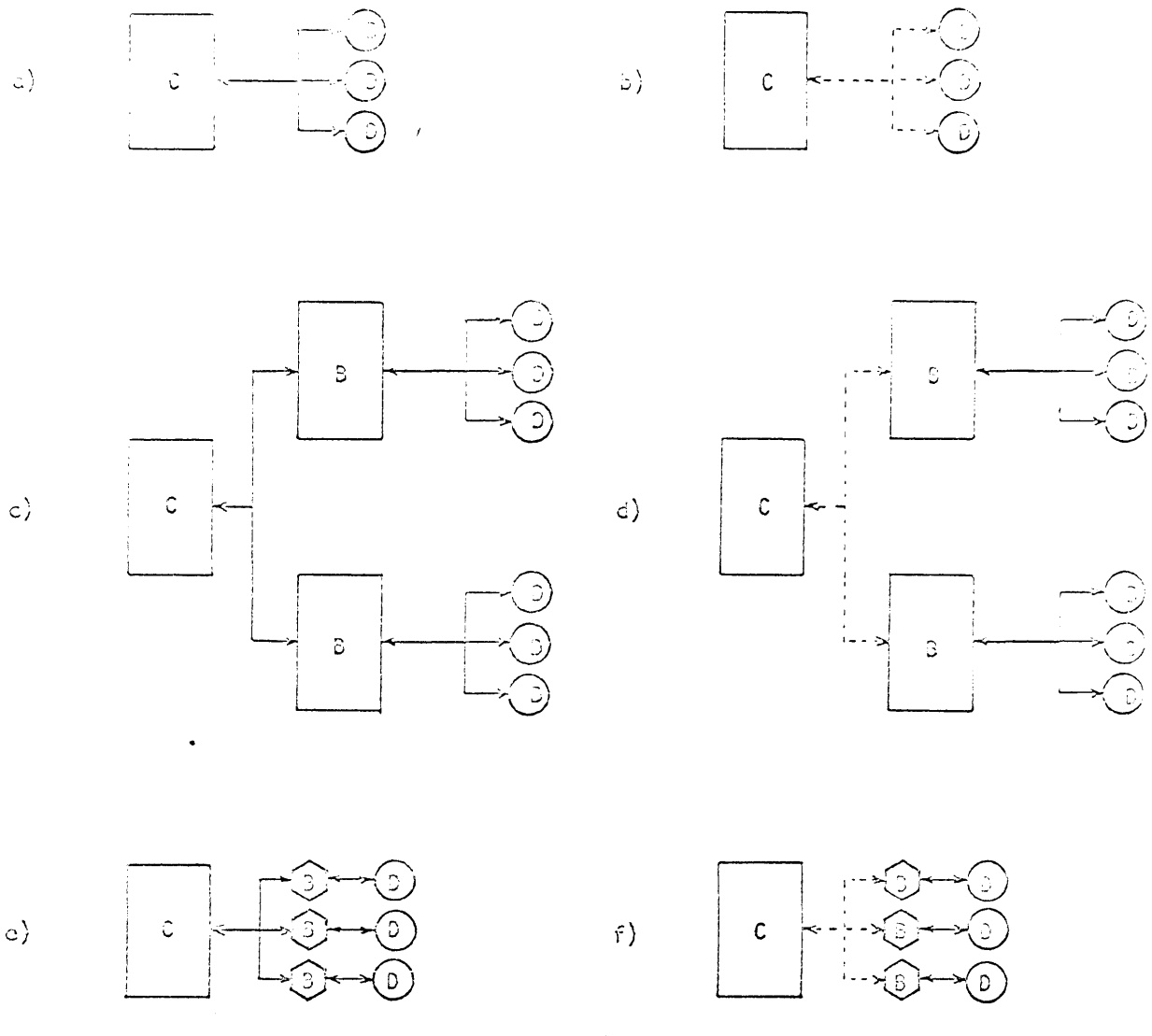


Figure 2-11

Computer Steps in Conjunction with Function Keys



C = COMPUTER

B = BUFFER

D = ON-LINE DEVICE

——— UNBUFFERED I/O CHANNEL

- - - - - BUFFERED I/O CHANNEL

FIGURE 2-12

COMPUTER/ON-LINE DEVICE CONFIGURATIONS

2.3.4 Software Considerations

2.3.4.1 Implementing and Using the System

From the point of view of the user/operator the display subsystem should possess the following:

1) Standard procedures - It is well to establish clear rules with regard to console functions and operations so that there is a minimum of confusion by the operator. This refers to the following items:
   a) Maintain uniform use of groupings of keys. If, for example, the console keyboard has several physically distinct arrays of lights or buttons then it is wise to have each unit in the group consistent with the function of the group. Thus all alarm indicators should be grouped together.
   b) Define simple steps for using console buttons that are consistent within each physical panel grouping. Thus the alphanumeric keys should all cause a character to appear on an associated display for each key depressed. System alarm indicators should behave in identical ways for all alarms.
   c) Require all data input via the alphanumerical keyboard to fit a prescribed format whenever possible. This has the advantage of allowing the computer to guide the operator and permit computer transformation of data from external to internal representation.

2) Ease of Use - Program as much as possible and provide as many flexibilities as possible. Do not sacrifice user simplicity and flexibility at the expense of more complicated "one time" programming.

3) Flexibility - Usage of display devices will invariably lead to improvements in procedure and technique. Hence it will be desirable to be able to make changes often and easily. This implies providing the ability to alter individual steps and the logic flow.

4) Growth - Application areas will grow as new uses are found for the displays, especially if the devices are general purpose. Hence, it should be possible to add new functions to the programming system.

5) User Orientation - The display subsystem should be as much user oriented and user understandable as possible. Hence, it is desirable that the design, implementation, and modification of specific functions be as much "professional" programming independent as possible. Optimally, the system should be manageable by the user, once the basic programming has been done.

The following operating principles should be preserved:

1) Lights that present status should uniformly all present either negative or positive information whenever possible. This rule may be compromised for a second rule which states that indicators should go in the "on" position for the exception, and not the rule. (This rule is, however, often violated by the equipment "on" indicator. This violation is probably justified).

2) Whenever a button is pressed by an operator, some positive and identifiable response should be given by the computer to the operator. Thus, if a control button is pressed, an associated neon should go on or the display should indicate the action. This redundancy should be caused by a return message from the computer to serve as an intermodule communication check (and hence not require hardware error check).

3) The console buttons should have associated markers to indicate a functioning keyboard. The operator should be made aware of a full buffer if keys are pressed too rapidly. This can be served by an indicator or by locking the keyboard.

2.3.4.2 User/Operator Techniques

2.3.4.2.1 CRT Displays and Their Use

CRT displays may be classified into four basic types:

1) Message displays, which do not require modification in any manner by the operator.

2) List displays, which require the operator to make selections from a prepared list of items.

3) Format displays, which require the operator to make entries in well specified positions.

4) Free displays, which allow the operator to make entries into any position.

Of these four display types, the first is computer generated (e.g. outputs), the middle two are computer presented or computer generated for operator use, and the last is operator generated. Typically, only the first three are employed, the last being useful only for free text entry.

One of the important features that should be available with CRT displays to aid in data entry is knowledge of current "position" of the "platum". That is, the position on the CRT where the next character will be placed. This can be handled either by hardware or by programming. In either case, some symbol is dedicated to serve as a "marker" having the property that it will always move one character position to the right (or to the first location of the next row if it now occupies the last position of a row) whenever an alphanumeric key is pressed. The position previously occupied by the marker will be taken up by the data symbol just entered.

The message display is generally information supplied by the computer regarding operational status, actual output, and such items as file indices and reference tables. The free display would be information supplied to the system for future reference purposes. Also, the free display could serve as the input for generating certain data bases for say, intelligence files.

The list and format displays are the work horses of the system. The former consists of a list of items from which the operator may choose in making parameter selections. By use of special selection keys, the operator is able to select any number of items from the list. Furthermore, choice of an item from one list could lead to the presentation of a second list, permitting further choices. Such an arrangement leads to the concept of multi-level sequencing through an indentured index taking the analyst from the general category to the specific by the most direct route. For example, if the operator had selected Air Bases from the choices open to him, then the

system may next present him a breakdown of this category as was illustrated. This process could, of course, continue to any level. The item chosen at the lowest level reached will then serve as a selection parameter in whatever action is being generated. In effect, the parameter will be the logical "and" of this item with all the higher level choices made to get to this particular list.

In a list display it is also possible to make multiple selections within a particular level. To establish some bounds to these selections, if a multiple choice is made, the operator is prohibited from going to a next lower level. This limitation is imposed to avoid the unlimited handling otherwise possible. Thus, of the two "trees" shown in Figure 2-14 case (B) is now allowed.

The format display facilitates input of data that is structured. It has a well established form and the input data must conform to the limits set by the format. An example of such a display is given in Figure 2-13. Emphasis is made on the user oriented format and the utilization of application oriented language leaving necessary conversion and data packing to internal machine codes.

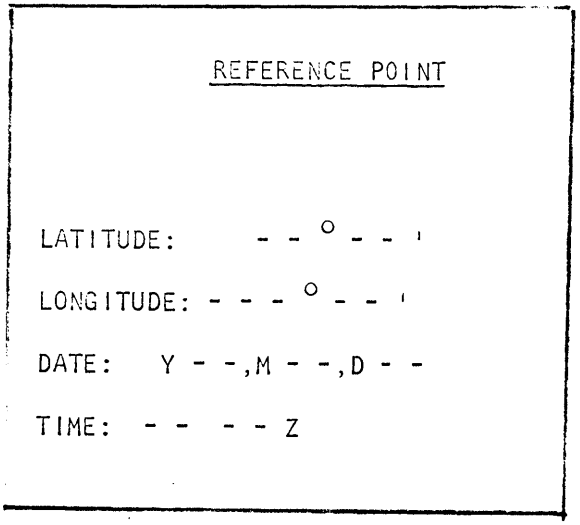
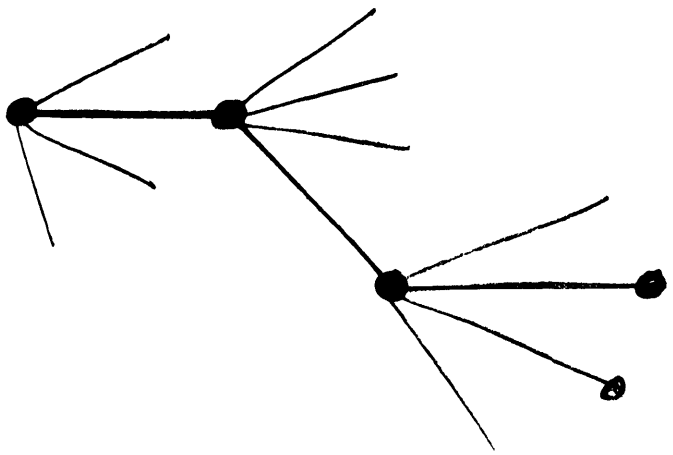


Figure 2-13

Example of Format Display

CASE (A)



CASE (B)

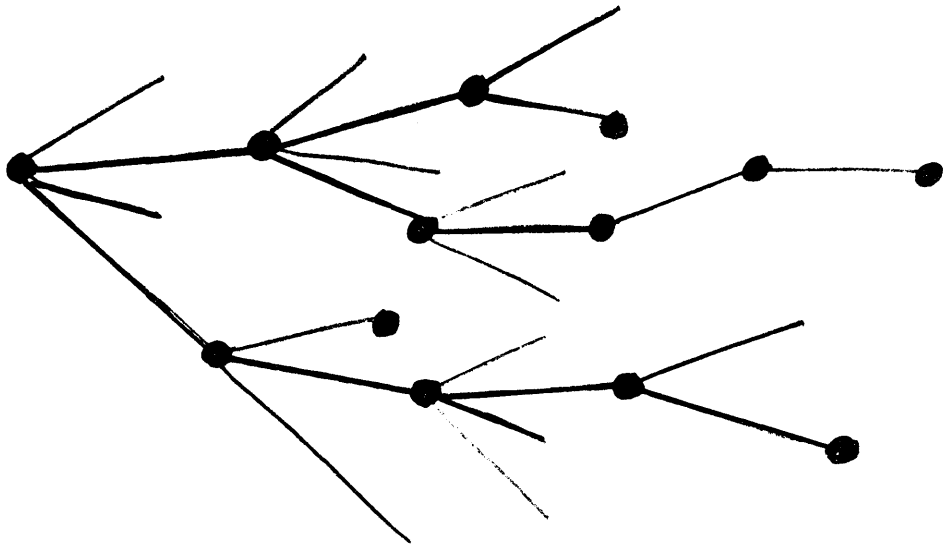


FIGURE 2-14

2.3.4.3 Programming Aspects

2.3.4.3.1 Programming System Requirements

To meet the requirements posed by the application characteristics identified in Section 2-2, both hardware and software considerations must be given. The extent of the software will, of course, depend upon the specific features provided by the hardware.

In designing the programming system it is necessary to recognize the following "internal" operating characteristics:

1) Many short demands - Perhaps the single, most important observation regarding the operation of multiple, on-line stations is the large number of short duration service demands made on the processor. These demands generate individual information entries that are built up into a complete message. In turn, a number of messages may be connected to form a complete transaction.

   Consider, for example, a simple alphanumeric message entry by a keyset station. The operator would press a key indicating his desire for service. The computer would respond with a ready signal (display) or would present a message (display) requesting the operator to select a format number. The operator would now enter a selected code-say 2 characters-and press the "end of message" key. The selected format would be displayed, and the operator would enter his data.

   The sequence performed by man and machine up to, and including, the first character of data entered into the selected format is, using the steps shown in Figure 2-15 as follows:

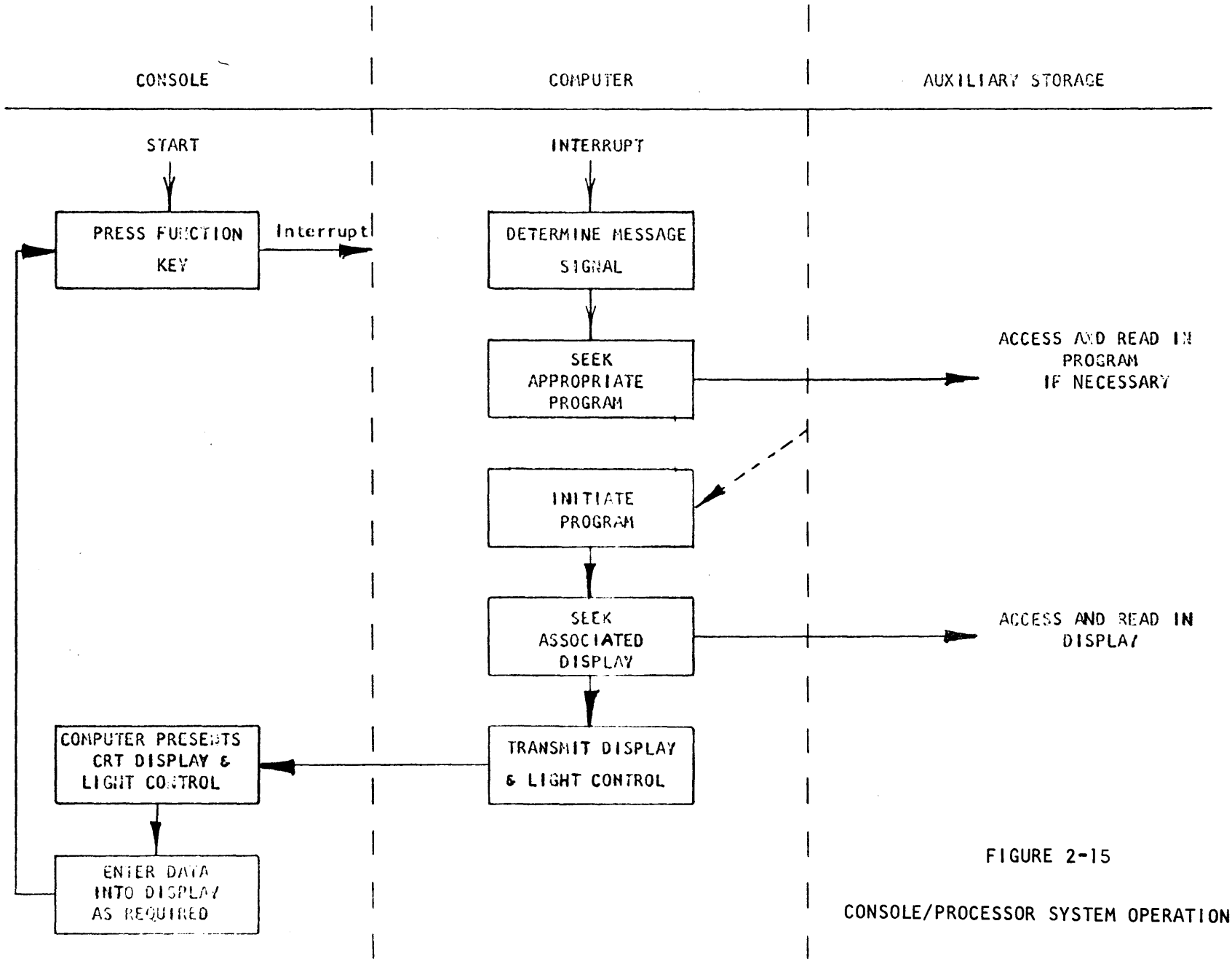


FIGURE 2-15

CONSOLE/PROCESSOR SYSTEM OPERATION

Step		Interpretation
a)	A	Indicates desire for service
	1,2,3	Generate response
b)	B	Receive ready signal/message
c)	C	Continue if no error, otherwise back to a)
d)	D	Enter first character of format number code
	1,2,3*	Accept input
e)	B	Validate the character
f)	C	Continue if no error, otherwise back to d)
g)	D	Enter second character of format number code
	1,2,3*	Accept input
h)	B	Validate the character
i)	C	Continue if no error, otherwise back to g)
j)	A	"End of message"
	1,2,3	
k)	B	Validate the format presented
l)	C	Continue if no error otherwise back to a)
m)	D	Enter first character of alphanumeric message
	1,2,3*	Accept input
n)	B	Validate the character

* The typewriter itself provides an automatic presentation of inserted data and, therefore, for this example, frees the computer from those steps 3 marked with an asterisk.

The total internal processing time for the above actions may be about 50 milliseconds for a medium speed computer. In addition, up to several hundred milliseconds may be required for accessing and presenting displays if they are needed and auxiliary storage is used. Since the total elapsed time for the entry of the above example may be about 10 seconds, it can be seen that very little of the total computer capacity has been used. If the I/O transfers are buffered, then the references to auxiliary storage will not be additive with the processing time. On this basis, a single station would use $\frac{50}{10,000}$ or 0.5 percent of computer processor capacity, and k stations would require 0.5k percent of capacity. It is interesting to note that for larger and faster computers the denominator remains constant whereas the numerator decreases. In fact, for computers of the CP 667 class, this may be only one or two milliseconds. Hence, it is concluded that a single processor is capable of servicing many stations and still have large capacity left over for functions.

2) Time sharing of Processor - Based on the foregoing, there will be a considerable amount of processor capacity available for tasks other than the routine servicing required by consoles. A good part, if not all, will be required to actually execute the functions that may be initiated by the completed console message or request. In addition, there will be other computations, related to the total problem or, for that matter, secondary in nature, that will use up excess capacity. Because of these interactions and the step-by-step processing associated with each console, the entire system must be time shared, and more than likely, multi-programmed.

3) Special Timing - The special nature of the display device interface and possible electromechanical responses may impose special timing requirements on the computer program. This depends, of course, upon how much of the detailed bookkeeping and control is actually committed to hardware. Consideration must be given to the following representative items:

a) Refresh - if automatic buffers do not refresh the volatile CRT's then the computer must re-transmit the information sufficiently often, say every 20-25 milliseconds.

b) Scanning - it may be necessary to insure the clearing out of the console output register sufficiently often, say every 200 milliseconds, if keyboard entry is to continue at operator pace.

c) Outputs - special devices may require output data that must meet specified timings. This may be true, for example, of electromechanically driven devices where start/stop problems may arise.

The actual implementation of these response requirements will depend upon the availability of suitable interrupt features, an active or passive clock, and sufficiently long buffers. If none of these features are available, detailed programming may take their place at the expense of possibly affecting total efficiency. In this regard, an important point is that timing may not always be critical, and cycles can be skipped now and then. For example, a CRT image would not suffer from occasional misses at refreshing, or from a 5-10 millisecond delay in a cycle. However, while random pertubations will not adversely affect the viewer, periodic misses will be noticed.

4) Auxiliary Storage - The requirement for rapid response and the servicing of many stations, each actively spread over a long period of time relative to the effective computing rate, leads to the need for rather large capacity auxiliary storage. This store will hold programs, working displays and the basic data base. While this discussion points to the need for random access--bulk storage, such as drums and discs--it is still possible under appropriate program design, to be reconciled with magnetic tapes.

2.3.4.3.2 The Display Subsystem Programming System

As discussed above, multi-station, multi-purpose display systems require random and unscheduled servicing by the computer. Further, the interactions between man and machine are spread over relatively long periods of time and are completely asynchronous with respect to each of the users.

Systems of this type require access to programs, pre-stored display and data on a random basis if reasonable response times are to be met. Because of the expected time sharing of the central processor between multistations for intermittant servicing, it is necessary to maintain console "history tables" which reflect the transactions that have been generated by each user to some point in time. In addition, it is necessary to maintain "position" in a particular procedure since unpredictable time lapses will occur when human responses are required in fulfilling individual steps of the procedure.

Effectively, the program must wait (or do something else) whenever a display is presented to the operator. As the operator enters data (if required) the computer must momentarily return control and monitor each entry. Upon completing the entries for a single display, an appropriate "end of message" will dictate that the next logical step in the procedure is to be initiated. At the end of the final step, a complete and meaningful message or direction will have been generated from which the computer will now determine action independent of the operator. It is thus possible to continually generate directions and have the computer respond to them on an overlapping basis.

It is possible to separate the application oriented tasks from those that are general purpose and apply to most on-line display system applications and processes. The division is made between the processes required in generating a message and the actual procedures for executing the action that may be called. The former concerns the mechanics of handling displays and composing messages, whereas the latter is concerned with actual file handling, retrieval, processing, summarizing and formatting. In this disucssion, attention is restricted to the first aspect, the general purpose processes.

The objectives for the programming system are as follows:

1) Provide general capability and flexibility so that virtually all applications can be accommodated.

2) Standardize techniques and procedures so that individual program segments or subroutines can be shared by as many functions as possible.

3) Maintain order among contending users for the same files.

4) Service each console as if its operator is the only user making demands on the processor.

Based on the above discussion, the programming system must include:

1) Display Subsystem Executive Control

This program performs the basic scanning, sequencing, and queue control for servicing the on-line devices. In addition, it links to the Master Executive Control which may be supervising the total processing system.

2) Function Monitor

This program maintains the history tables and establishes the action sequences to be carried out as a function of the keys that are pressed.

3) Utility Program Package

This is a collection of service routines used primarily by the Function Monitor and Executive Control. The availability of these general purpose programs precludes recoding of common functions.

4) User Language

This is the language which must be used by the application programmer in writing his program. The system must provide the programmer with the ability to express his program in both the symbolic language of the computer where each command generates one machine instruction and in higher order languages where each command generates many machine instructions.

In order to be effective, the higher order language must possess the following chief attributes:

a) It must be powerful enough to express the application problem.

b) It must be such that nonprogrammers can use it with a minimum amount of training.

c) It must be readily expandable so that new commands and functions can be added.

The existence of a system such as this implies that application programmers must conform to certain coding restrictions and procedures so that all of the possible programs can be accommodated by this approach. While this may seem a disadvantage, it is, in fact, a saving grace since:

1) It simplifies the programming because of the existing of service routines.

2) It simplifies the implementation of a new application since the design must fit within the logical framework set forth by the system.

The importance of the second point cannot be overemphasized. Without a well-defined organizational and procedural philosophy, the programming design and implementation of the individual application can become a major undertaking.

2.3.4.3.2.1 Display Subsystem Executive Control

The real-time requirements associated with on-line displays present a problem of priority of interrupt handling and servicing. Hence, it is necessary to design an executive system which will be responsive to these requirements. Such a program will be equipment dependent in the sense that many hardware/software tradeoffs are possible.

The basic requirement of the display subsystem is the control of a great number of I/O. This includes: *

1) Scanning the input lines for messages
2) Refreshing the CRT's
3) Accessing programs, displays and data from auxiliary memory
4) communicating with other processors that may be in the system
5) Maintaining timing responses for special purpose on-line display equipment.

* Initially, it is assumed that the system has a minimum number of desirable hardware features.

It has already been stated that typical timing requirements range from refreshing the CRT within 20-25 ms periods, to scanning of inputs from the console keyboards every 200 ms. Unless certain hardware features are available, such as automatic interrupts and I/O buffering, the programs will have to take these into account.

Assuming no dependence on hardware, the executive program must maintain continuous cognizance and control over the I/O. This is done by the basic control loop shown by the dotted lines in Figure 2-16. Each of the five indicated functions could potentially generate a processing task as the cycle is traversed. For example, the tasks associated with scanning the input message lines is shown in Figure 2-17.

To meet real-time requirements, this loop must be passed at a rate which will insure return to the task which has the tightest timing constraint within a specified amount of time. This time will be called the "basic cycle time". Thus, if the CRT refreshment is the critical task, then the basic control loop must return to that task within a basic cycle time.

There is also the further implication that the processing requirements for each of the five identified functions must be completed within a time which will not compromise the total cycle time.

There are three ways of achieving this:

1) Allow processing to proceed in increments of the basic cycle time so that temporary return to the cycle is permitted after each such segment. This leads to difficulties of recursive entries into the various processing tasks.

2) Spot-place a particular task in more than one position in the loop. Thus, for example, the "refresh CRT' might be placed in every other position in the loop if the other functions have a period which is very much larger than that of the CRT refresh cycle.

3) Permit only a minimum of processing as each of the tasks are reached and place in a queue those functions not completed. This queue is then processed during the residual time which is left over during every cycle. This is shown in Figure 2-16 by the box which is part of the loop indicated by the heavy lines. It is, of course, necessary that the residual be non-zero enough of the time if any processing is to occur.

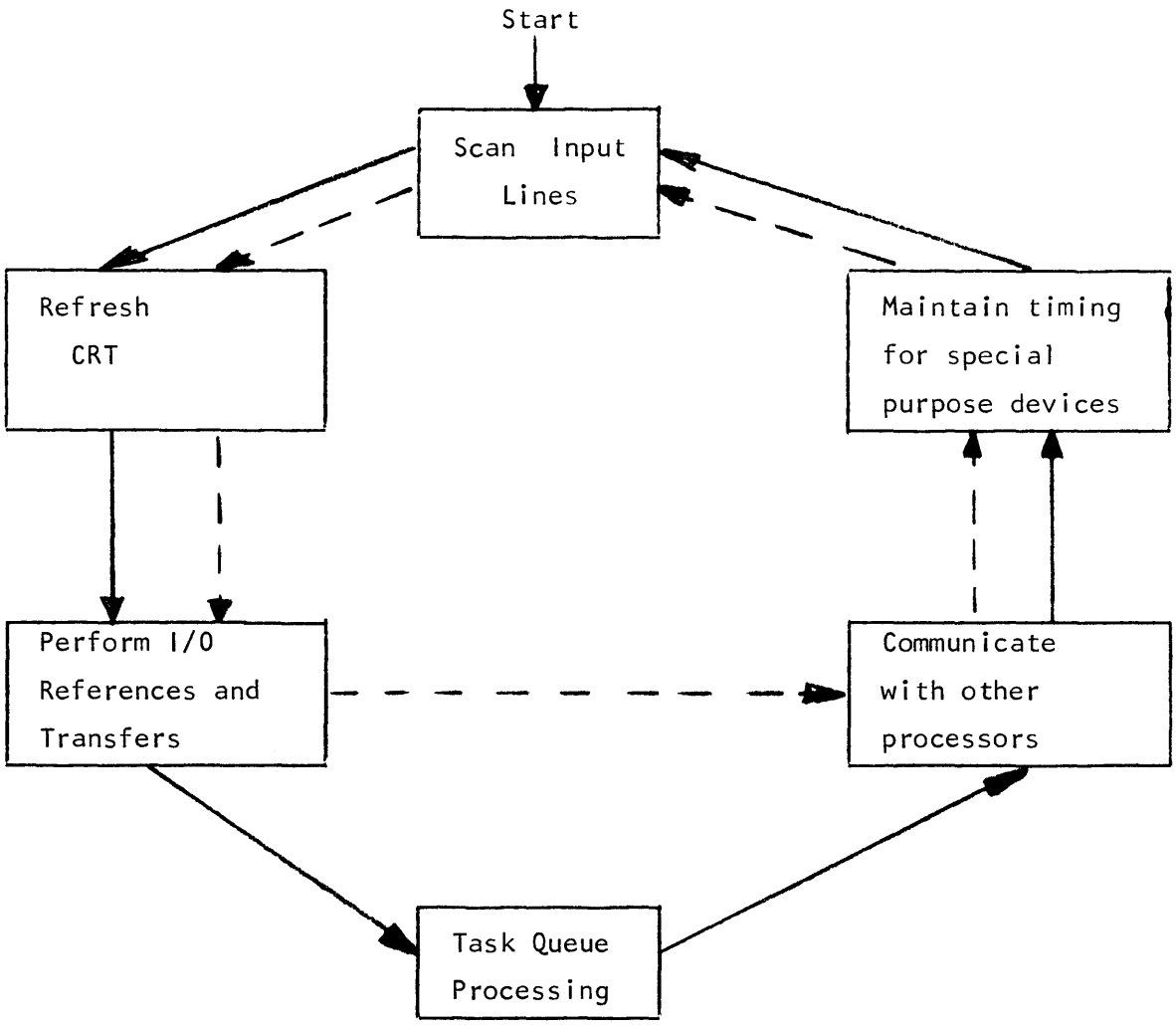


Figure 2-16

Basic Executive Control Loop

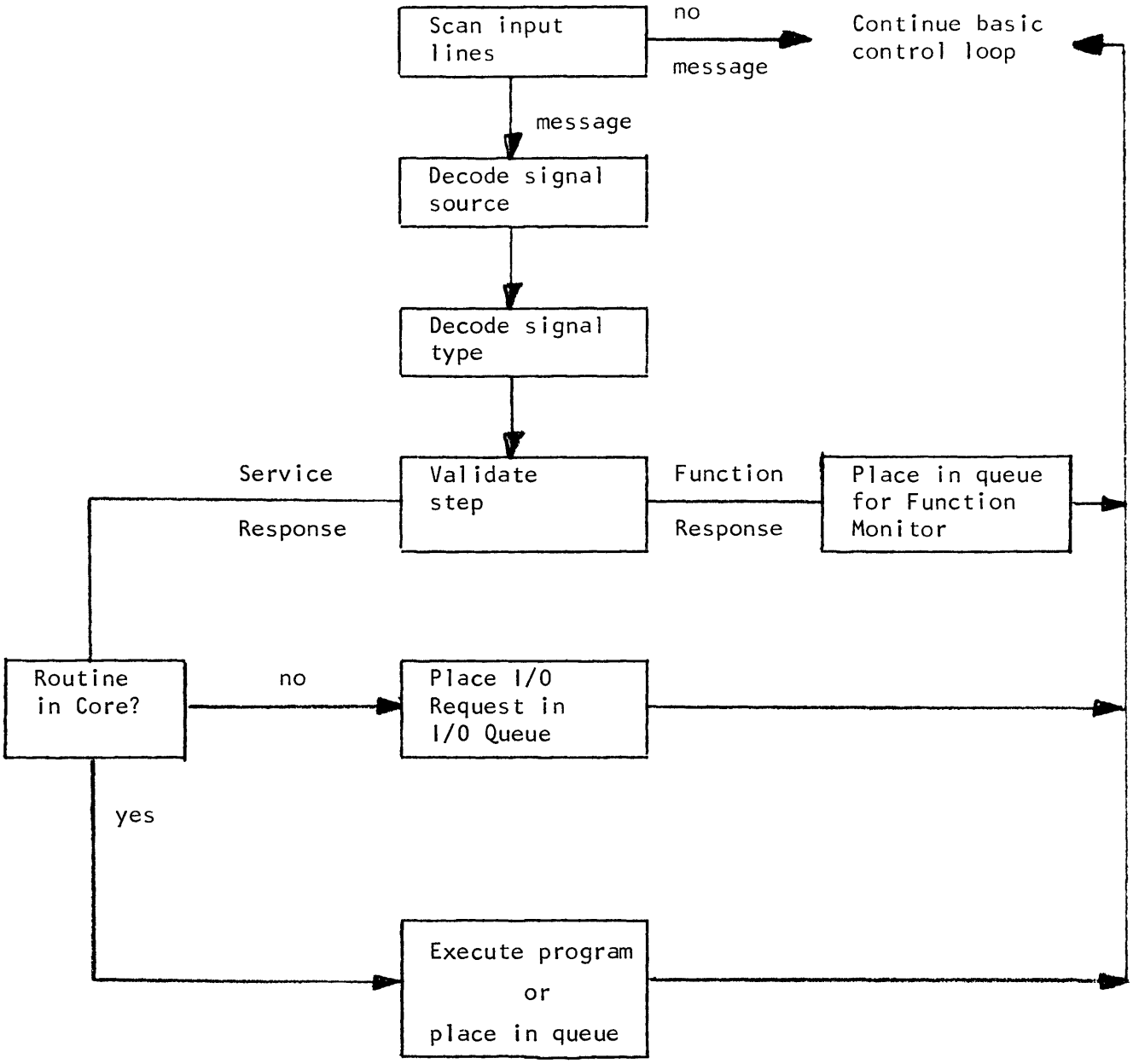


Figure 2-17

Tasks Associated with Scanning the Input Message Lines

A particular system will include any number of these possibilities depending on the details of the system interface and hardware characteristics. The example shown in the figure employs the last of the above alternatives.

If one has m consoles in the system and each one is generating input at the nominal 60 wpm rate, then m consoles would require servicing every 200 milliseconds. Based on experience, the typical processing time per character (command) entry is one millisecond for computers of the 12 microsecond memory class. Hence, if m is 20, then 20 milliseconds out of every 200 (or 10% of the available processor time) is spent in console servicing if the entry rate is sustained.

A more realistic analysis of processor support to displays is given in Figure 2-18. Here it is shown that if messages can be entered in 30 seconds, a single console will require a total of 1.0 seconds of processing and 1.6 seconds of I/O time assuming a 12μs. computer memory and the availability of a fast disc system for auxiliary storage. Azimuth m=20 consoles would require 20 seconds of the processor's time and 32 seconds for I/O. The latter is, of course, impossible in a 30 second period unless there are multiple buffered channels in the system. It can be seen that a multiple console configuration can saturate the computer capacity so that while all of the consoles may be serviced, the other processing tasks are not satisfied. Based on tables such as shown in the figure, a proper balance of number of stations, speed of processor and total processing tasks is achieved as a result of a system analysis.

	Rate of Occurrence	Average Processing Time	Number Per Message	Total Processing Time	
				Computing	I/O (Assumes disc)
Alphanumeric Entry	200 ms	1 ms	150	150 ms	
Display Change	4 sec	250 ms	8	400 ms	1600 ms
Function Key	6 sec	150 ms	5	250 ms	
Complete Message	30 sec	200 ms	1	200 ms	
Total				1000 ms	1600 ms

Figure 2-18

Processor Servicing Required in Support of Console Message Entry

(exclusive of refreshing)

The following comments are presented concerning the implementation of the executive control with respect to the presence or absence of the indicated hardware features:

1) If neither external interrupt nor a real time clock are available, then the tasks associated with each of the control loop functions and all other calculations must be programmed in segments so that each segment will permit return to the control loop and maintain the timing.

2) If a clock is available then the executive can preset it at the beginning of each cycle so that it will interrupt the processing of the queue at the proper time.

3) If external interrupts are available then the function of the basic control loop has been absorbed by the hardware and no executive function is needed. Consoles are then serviced on demand.

2.3.4.3.2.2 Function Monitor

The function monitor is a specially designed program to facilitate the responses to a special set of keys on the console. Although not all consoles have a set of keys of this type, it is deemed necessary that a truly general purpose console will have such a set. They are characterized by the fact that their labels and also their identifying codes can be changed at will by the operator.

The process of entering information into the computer for the purpose of making a request has been discussed in detail earlier. It is primarily to ease this process that the function monitor is designed. Knowing that different applications will require different displays and different sequences of presentation, it is apropos to design a scheme which is not application oriented and is professional programmer independent so that the user can design his own data entry scheme and query language.

The function monitor is an interpretive program which operates on a very special language useful in display manipulation. When one of the special keys mentioned above is pressed, the executive control recognizes this and passes control to the function monitor. There, the specific key is identified and an associated table of instructions in the special display language is executed interpretively. It is the ease with which a user can modify this table of instructions which makes the function monitor so valuable. To illustrate the capability of the display language some of the possible instructions are:

1) Turn the specified console lights on (off) - the lights are specified in parameter words following the instruction.
2) Display the following characters on the CRT - the characters along with their location coordinates are listed following the instruction.
3) Locate a display in auxiliary storage - the identification of the display follows the instruction.
4) Clear a specified buffer - the buffer area may be either pre-established or specified in the words following the instruction.
5) Enter the specified characters in the buffer - the characters are listed following the instruction.
6) Process the "list" display - special codes (specified by the query language) are extracted from the list display as dictated by the selections of the operator and are placed in the buffer.
7) Process the "format" display - the parameters entered by the operator are extracted from the format display and stored in the buffer.

A more sophisticated language can easily be designed to cover more applications. The above language, however, is completely adequate along with its function monitor to service the kinds of retrieval requests set forth as examples in Section 2.3.2.

2.3.4.3.2.3 Utility Programs

Utility or service programs extend the hardware in a general way so that certain functions become available to the application programmer without his concern for programming. This software is primarily concerned with facilitating the entry of alphanumeric information onto the CRT in an expeditious manner. Also included are useful functions for data handling and in the control of displays.

In some instances the recommended features described below may be part of the hardware, thereby precluding a need for the programming.

1) Marker Routines

The marker is a special symbol which is used to indicate current writing position on the CRT. The following control keys are defined for manipulating this marker:

a) Marker Enable - This key causes the marker to appear at some fixed location on the CRT. This position could be, for example, the (1,1) character location. As alphanumeric characters are entered, the marker is displaced one character position to the right, the newly entered character taking its place. The marker moves from the end of one row to the beginning of the next and upon reading the lowest right hand position, it will return to the (1,1) position. A character that is dislocated by the marker will be replaced when the marker is moved again, unless a new character has been entered.

b) Marker Disable - This key removes the marker from the CRT.

c) Marker Backspace - This key causes the marker to move one position left, or to the end of a previous line, if now at the beginning of a line.

d) Marker Up - Depressing this key causes the marker to move to a position in the preceding line which is directly above its current position. If the current position is in the first line, the marker is moved to a position in the last line vertically below its position in the first line.

e) Marker Down - This key causes the marker to move exactly opposite to the motion described in "Marker Up."

f) Marker Left - Depressing this key causes the marker to move in positions to the left in the same line. The marker moves "end around" from the first to the last position of a particular line. If n=1, then this key is identical to the backspace key except that the latter is not restricted to a specific line.

g) Marker Right - This key causes the marker to move exactly opposite to the motion described in "Marker Left" except that the number of positions moved is n'. A relationship should exist between n and n' such that one of them is equal to one and the other is some small integer greater than or equal to one. A recommended system is n=5 and n'=1.

h) Advance Marker - This key is used in conjunction with the format display, i.e., a display in which the operator enters A/N data into various labeled slots. Depressing this key causes the marker to be moved from its current position in some slot to the first position of the next slot. If the current position is at the last slot, the marker is moved to the first position of the first slot.

i) Accept Item - This key affects the marker only with respect to list displays. The depressing of this key will move the marker along the first column, from one row to the next, replacing the marker by "X", indicating that a particular item was selected.

j) Reject Item - This key affects the marker only with respect to list displays. The depressing of this key will move the marker along the first column, from one row to the next, replacing the marker by "space". This feature is used to reject a previously accepted item.

2) Display Control Keys

The operation of the CRT display is aided by the availability of the following keys. For convenience, a distinction is made with respect to the CRT display which is viewed by the operator and the CRT display image, (or just image) which is the computer stored analog of the CRT display.

a) Display On - This key causes the CRT display image to be presented on the CRT.

b) Display Off - This key removes the CRT display leaving the image in a passive state.

c) Clear Display - This key causes the CRT image to be completely cleared except for the marker which, if on, is restored to its origin.

d) End of Message (EOM) - This key is used in conjunction with data entry to indicate to the processor that a message has been completed. It serves as an interrupt which signals the computer to act on the CRT data.

e) Data Insert - This key is used in order to insert a set of alphanumeric data on the CRT between two consecutive characters. The marker is first positioned to the leftmost of the two characters. Then the Data Insert key is pressed and new data is entered appearing as it is generated and causing all of the data to the right and down to be shifted by one position. Exit from this mode is made by pressing the EOM key.

f) Data Delete - This key is used to delete a set of continuous alphanumeric data on the CRT, followed by a closing up of the display. The marker is first positioned at one end of the set, the Data Delete key is pressed and then the marker is set at the other extreme. Pressing of the EOM key causes the desired action and exits from this mode.

g) Sequence Display - This key is used to call for the next part of a multi-part display should the size of the CRT prohibit the display of the entire message at one time.

h) Display to Printer - This key generates a hard copy version of the CRT display on an associated typewriter or line printer, whichever is available.

i) Monitor Display - This key permits the selection of any other CRT associated with another console for purposes of monitoring that console's activity.

j) Save Display - This key interchanges the CRT image with the contents of an alternate location. Thus, effectively it permits saving information for future reference purposes. Typically, after pressing this key one will also press Clear Display if one is disinterested in the display brought forth from the alternate image location.

3) System Control

In this section representative functions are identified and assigned to the Control Keys. In a particular system more descriptive and extensive keys may actually be called for.

a) Display Message - This key permits interruption of the current CRT display for purposes of viewing the message which is being held by the computer for the operator. The availability of a message is indicated by a status light (see below). Return to the current procedure is by pressing of the Display On key.

b) Display Queue - This key causes the internal tasks queue (if there is one) to be displayed. Shown are priority ordering and status. The operator is now able to modify this queue by manipulating the CRT display and using the Modify Queue key (see below).

c) Modify Queue - This key can only be operated after the Display Queue key was pressed. It causes the CRT display to be sent to the processor where the queue is then modified.

d) Change Procedure - This key provides a display which permits the operator to modify, select or cease system operation. Typically, this feature is an overall control procedure which should be assigned to only one of the on-line stations.

e) System Breakpoint - This key is essentially an external interrupt which performs two functions. The first is to save-store system status for rollback purposes in case of hardware failures. The second is for modifying the system configuration or operating procedure.

4) Status Indicators

Status indicators reflect the composition of the configuration, intermodule communication situation, internal machine control situation and system operating modes.

a) Power On - Indicates whether console is in operating mode.

b) Processor not Communicating - Indicates if the communication between console andprocessor has lapsed more than some pre-established period of time (say 500 milliseconds).

c) Queue Full - Indicates that the internal task queue is full, and that no further inquiries can be made of the system.

d) Message Ready - Indicates that a message has been generated by the processor for the operator. The operator can select this message on the above-mentioned Display Message key, which, when selected, turns this indicator off unless a second message is also present.

e) Operating Mode - Indicates which mode is currently in operation. An indicator is dedicated to each operating mode identified by the system.

f) Configuration - Indicates which peripherals are on-line with the system. An indicator is dedicated to each of the relevant devices. This indicator is useful as a means of assigning peripherals to different consoles, It is used to display legal or illegal connections for any one console.

5) Error Indicators

The following alarm indicators are indicative of the signals that are useful to the operator. These indicators have an associated button with which the operator can cause a "reset" action to take place and attempt the procedure once more. The indicators should be placed in an obvious position so that the operator will be cognizant of alarms. One procedure is to cause the indicator to blink on and off at an appropriate rate, say twice per second.

a) Parity - Indicates parity error in transmission from, or to, the console.

b) Keyboard Locked - Indicates that illegal use was made of the keyboard, such as pressing two keys within a disallowed time interval.

c) Data Entry - Indicates that some rule regarding data entry on the CRT was violated.

d) Procedure - Indicates violation of order regarding the use of the function keys.

e) Control - Indicates violation of rules regarding the use of a control key.

2.3.5 System Design Steps and Considerations

2.3.5.1 Identification of Evaluation Parameters

The determination of "best" display is a function of system balance where cost, computer programming, and demands on the computer must be measured for the application.

While the first of these is evident and simple - i.e., a dollar cost for the display and all interface boxes and cables - the second is more elusive, while the third is often a neglected consideration.

2.3.5.1.1 Display Hardware Costs

Display hardware costs are not only measured by the cost of the particular keyboard and CRT unit but must also include the black boxes and cables which connect the device to the processor. Total display subsystem costs are also a function of number of units. Since displays are often custom designed to each user's specifications, single unit purchases are usually more expensive than buying them in lots of five or more. Also, in many cases, parts of the hardware can be time shared, and the unit price decreases as the number of units increase.

It is desirable to consider alternatives in system configurations since cost is related. There are several methods for tieing the on-line device to the computer. The appropriate method for each application must be determined during the system design when the system equipment is being specified.

2.3.5.1.2 Computer Programming Requirements

The use of on-line communication devices places software requirements upon the total system. The extent of the software which is developed will depend upon the specific features provided by the hardware. For example, the programming developed for a specific display console connected to a CDC 160 computer system is given in Figure 2-19.

CDC 160 PROGRAMS	NUMBER OF CDC-160 WORDS
PROGRAMS	
MASTER CONTROL PROGRAM	150
A/N SUBROUTINE	125
A/N LEGALITY	15
CHARACTER TO CRT DISPLAY	32
COMPUTER MARKER POSITION	20
MARKER KEYS PROGRAM	131
ENTER/CANCEL	20
REGENERATE CRT	14
ERROR LIGHTS SUBROUTINE	17
TAPE SEARCH ROUTINE	246
CRT DISPLAY	20
DISPLAY REQUEST QUEUE	16
CRT DISPLAY TO 1604	46
CHANGE REQUEST QUEUE	19
MODE/MODEL CHANGE	186
STOP MODEL	3
NO DISPLAY	37
CLEAR DISPLAY	29
DUPLICATE DATA BASE	3
1604 ON-LINE	18
1604 MESSAGE READY	104
INSERT ROUTINE (2)	155
DELETE ROUTINE (2)	96
OVERLAY INTERPRETATION PROGRAM	556
SEQUENCE DISPLAY	86
BUFFERS	
CONSTANTS	64
CRT DISPLAY IMAGE	448
CONSOLE LIGHTS	5
OVERLAY TABLE	512
SUPPLEMENTARY RECORDS	256
TOTAL WORDS	3429

Figure 2-19
Programs for a Display Console Connection to a CDC 160.

2.3.5.1.3 Demands on the Computer

To analyze the demands on the computer system by on-line consoles it is necessary to define a problem mix and the detailed types of operations that will be employed in the execution of the task. The typical problem studied is the composition of a query to the data processing system.

To carry out this job, the operator will:

a) Depress function key 1
b) Get positive response that key 1 was depressed
c) Computer presents a display on the CRT
d) Enter data into display
e) Visually validate inserted data
f) Make corrections to inserted data if necessary
g) Signal end of entry

While this sequence of user/operator events is underway, the computer is engaged in a number of actions paced by the speed of the console operator.

The conclusions are to be drawn. First the tieing of on-line displays to a computer will require dedication of memory.

The second conclusion concerns the amount of computer time actually used by the displays for display activity independent of retrieval, formatting, and presentation.

The third conclusion concerns the potential traffic problem which multiple consoles may cause with respect to the data channel to which they are connected and with respect to the I/O transfers required between auxiliary storage and processor and in the processor itself.

Using the data presented earlier as a basis, we can obtain an upper limit on waiting for a multiple console system. We assume a worst case model where the total processor and I/O time of 1.5 seconds is lumped together as the service time. Using the theory associated with Poisson processes, we can estimate the waiting time form knowing the service factor. This number is the ratio of service time to total elapsed time between requests and is 1.5/30 or 0.05 for the problem at hand. The results of the traffic analysis are given in Figure 2-20 where a service factor of 0.03 is also added. The latter figure leads to a model which assumes buffering and better organization of the processing tasks.

Number of Consoles	Number of Consoles Waiting	Probability of n Consoles requiring service: Service Factor = .05	Probability of n Consoles requiring service: Service Factor = .03	Cumulative Waiting Probability: Service Factor = .05	Cumulative Waiting Probability: Service Factor = .03
0	0	.538	.712		
1	0	.269	.214		
2	1	.121	.057	.121	.057
3	2	.049	.013	.170	.070
4	3	.017	.003	.187	.073
5	4	.004	.001	.192	.074
6	5	.001	.000	.193	
7	6				
		1.000	1.000	.193	.074

Figure 2-20

Probability of n Consoles of Ten Requiring Service at the Same Time

The results shown that a waiting time will exist 19% of the time for the 0.05 service factor. Since the service time is 1.5 seconds, the average wait on the waiting line will be slightly under 3 seconds. For the second model, a waiting line will exist about 7.4% of the time. The average wait on the waiting line will be approximately one service time of 1.5 seconds.

These results are sufficiently favorable and tolerable that in a practical sense the console operations will experience no appreciable waiting, especially when it is realized that these statistical estimates reflect a pessimistic model.

2.4 INPUT/OUTPUT TECHNOLOGY

2.4.1 Classification of Input-Output Technology

Input-output technology deals with the techniques which a computing system uses to communicate with the outside world. Functionally, there are two different classes of subsystems in the outside world with which the computer must exchange usable information. The first subsystem is the human, who communicates in a wide variety of non-exact languages that require elaborate interpretation. The second class of subsystem is the non-human or machine, which uses a relatively smaller number of languages, all of which are exact and defined. These two problem domains are quite divergent. The relations of man and machine in a typical military information system are shown in Figure 2-21.

2.4.1.1 The Man-Machine Interface

Although a machine (and its attachments) is quite versatile in its ability to sense a wide variety of inputs, e.g. visual, sound, pressure, radiation, etc., man is capable of producing only two outputs which are relatively controllable. These are sound and pressure or motion.

2.4.1.1.1 Sound

The human is able to produce a greater bandwidth of information vocally than in any other manner. This information is produced with built-in identification characteristics such that two people may be talking at the same time and yet their conversations may be distinguished from each other. Unfortunately, the associative characteristics of human thought are such that it is difficult for the same person to express himself in exactly the same terms twice in succession, and it is nearly impossible for two different people to express the same thought in the same manner.

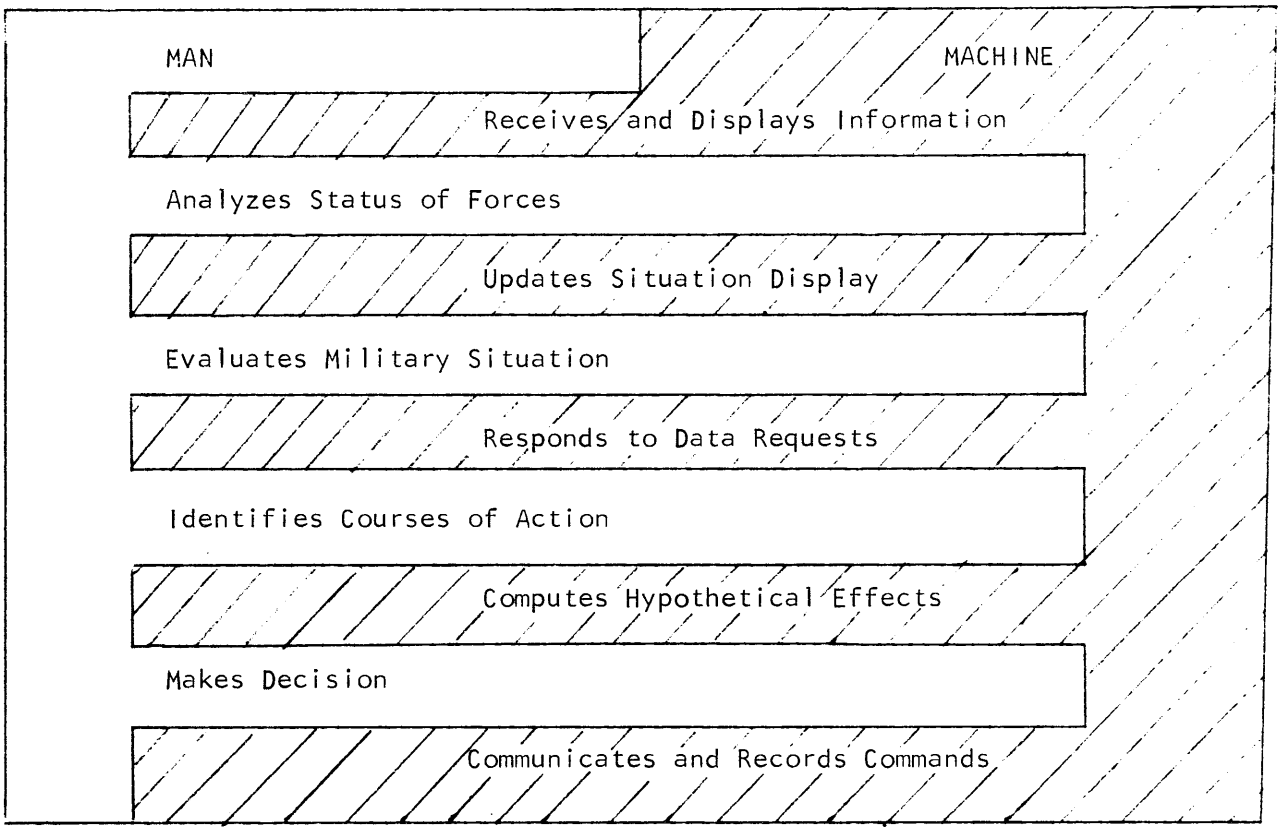


FIGURE 2-21

Relations of Man and Machine in a Typical Military Information System

Although sound input transducers for computer usage are relatively inexpensive, vocal human interface is seriously hampered by the lack of an interpretive concept to allow the machine to understand the wide varieties of expression that a human may produce, even when vocalizing a concept held constant.[1*]

2.4.1.1.2 Pressure or Motion

The only alternative means of man-machine communication is the use of pressure or motion. Here, a human is quite inefficient, being able at a peak to produce only about three hundred controlled, distinguishable yes-no motions per second. At this rate, the motion must be of a reflex nature and the data involved must be preconceived and prerecorded. The 10-key adding machine operator can copy data at a peak rate of about 20 numeric characters per second, when selecting these characters from a total of ten possibilities. A good typist can select from about 50 characters at the rate of ten per second.

It is evident that although the action speed increases as the choice is reduced, the total bandwidth of information that can be transmitted increases as the action rate is reduced; thus, even greater information flow can be created in a situation in which a computer presents to a human a number of complex alternatives and the human makes a selection of the alternatives he wishes. Here, although there is a yes-no decision made by the human, the information content of this yes-no decision is quite great because of the human's preprocessing of a volume of data to make the decision.

* Numbers refer to references listed at the end of each subsection.

2.4.1.1.3 Human Language Interface

There exists a category of information transfer in which the information to be transferred is machine recorded in a human language. To further process this information, it is necessary for the machine to be able to read the human language even though the data itself is not being, at this point in time, originated by the action of a human. Typical of such human language interface machines would be character recognition equipment. The problems in the design of such equipment are similar in nature to those that occur in the design of equipment where the data is actually originating with the human.[2] All the vagueness and lack of exactitude of human language exist within the data and a rather sophisticated means of interpretation is required.[3] One might think, however, in just reading and transferring, that this can be done by blind rote if the meaning does not have to be deciphered. The parallel is not really exact since the data is only being transferred as over a communication link, and a true man-machine interface does not exist. Telephone lines certainly deal with the human language but they need a human at each end. Whenever the data has to be entered into a machine for the machine to operate on the data, the interface exists and the problem of data interpretation has to be solved.

2.4.1.2 Machine-Man Interfaces

Sensitivity of a man is such that he is quite limited in the number of techniques by which he may receive a reasonable quantity of meaningful information. There are in fact, only two channels available with useable, effective bandwidths. These are visual and auditory. Through both channels the man is able to sense a wide disparity of information, select that which is of interest to him, reject all superfluous information, and fill missing gaps from context or redundancy.

The computer, on the other hand, is not a particularly good generator of audio visual information despite the work at synthesizing speech using canned phrases or phonemes and the sending of audio codes which might be interesting in some application. Although computers can generate complex displays, their ability to produce and display visual information in no way approaches that of the human. This is probable due to its own limited language structure and the lack of variety in ways in which a computer can express itself.

2.4.1.2.1 Visual Interface

As the human is an excellent classifier, sorter and filterer for information, he is capable of accepting a very wide band of visual input, taking cognizance of those items of interest to him and ignoring all other items until they reach a status that calls them to his attention or until he reaches a status that calls them up. The bandwidth of information which he is able to accept visually is related to the language in which it is presented and the human's facility to handle that language.

Typical of the languages in which a human can accept information visually are:

1) The various printed and symbolic representations of spoken languages,

2) Non-spoken symbolic representation languages such as mathematical formulae and chemical formulae,

3) Geometric forms, diagrams and other forms of special relation intelligence,

4) Miscellaneous visual differences such as color and motion.

As there is a great deal of difference in the technology necessary to generate these different forms of visual presentation, and as the different forms are used for quite widely divergent functions, visual interface will be discussed in two separate parts of the technology study. The printed and symbolic forms of spoken language, some type of graphic and geometric communications and display of formula, when presented on a permanent document, will be considered under input-output equipment. All forms of

visual communication, when not created for record purposes, will be considered as display equipment. In present day connotation, display equipment implies a degree of real-time response or rapport between the human and the computer.

2.4.1.2.2 Auditory Interface

Auditory interface between a computer and a human can exist in two different ways. The human can be trained to recognize some form of auditory output of the machine code. Such an artificial system could be devised to allow the machine to generate Morse Code.* Changes in repetition rate of a signal may shift the frequency of a tone, or "operate" commands can ring a bell. All such forms of sound discrimination provide a very narrow bandwidth of communication between the machine and the human.

An alternative means of sound communication between the machine and the human is to allow the computer to generate, or select from storage, an appropriate series of phonetics, words or phrases and assemble them into a meaningful spoken sentence.

A human receptor is quite capable of tolerating and filtering out noise and other unmeaningful trivia and, where necessary, filling in missing gaps from context. Even a relatively crude human vocal simulation can transmit meaningful information between the machine and the human. The human can receive a bandwidth up to 300 words per minute and at relatively low noise levels.

* This has, in fact, been done to allow a program to send over its audio console monitor, the path which a complex program is taking during its cycling in non-real time (or free-time).

2.4.1.3 Machine-to-Machine Communication

The problem of communicating from one machine to another is quite different from that of communicating from a man to a machine or a machine to a man. The difference is that the human has already been designed and his limitations must be accepted, whereas a machine may be designed to do a specific job. The result is that a machine may use any media for communication with any other machine and the two machines may jointly use any conceivable coding system. Machine-to-machine communication, therefore, is essentially a question of coded energy transfer. The efficiency of machine-to-machine communication depends upon the efficiency of energy transfer of the media selected and the true data content of the coding system used. The reliability of the communication will depend upon the redundancy of the code used and the amount of noise or interference which occurs during the communication.[4]

Two different sets of criteria may be used in the analysis of machine-to-machine communication. These are:

1) The function of machine-to-machine communication
2) The technique of machine-to-machine communication

2.4.1.3.1 Machine-to-Machine Communication Functions

It is obvious that the prime function of machine-to-machine communication is the transfer of data; however, this data may be transmitted to or from a machine to provide data which the other machine will work upon, or it may be transferred to the machine to control the machine.

Such control data, unlike information data, frequently requires the transmission of power to drive a unit, (e.g. close a relay, close a valve) or it requires the transmission of an analog, (e.g. a change in voltage, a change is pressure, etc.). Although not frequently recognized by the digital engineer when he lifts the level of a line or pulses a line with an on or an off pulse, he creates an electrical analog of the opening and closing of a switch which in turn opens or closes a second switch. Such control information may be considered analog unless it is transmitted through a series of digitally coded pulses.

The most efficient means of transferring information from one point to another is usually the use of digitally coded data. Efficiency is gained by allowing more than one type of data to be transferred over a single line. Where a line exists between two points, any combination of pulses may be transmitted over this line. The data transmitted over this single line may be used by a multiplicity of different types of equipment all attached to the common line but each equipment capable of listening for its own coded "call signal" and decoding the data that follows.

2.4.1.3.2 Techniques of Machine-to-Machine Communication

As with man-to-machine and machine-to-man communication, the two critical factors involved with machine-to-machine communication are the form in which the data to be transmitted exists and the efficiency of compatible transmitting media. There are essentially three classes of data transmitting media available to the computer designer. These are:

1) Mechanical transmitting media including pressure, movement, sound
2) Electrical conductivity
3) Electromagnetic radiation including heat, light, and radio waves

Within each of these three major categories, there are many sub-categories which could receive consideration for data transmission in some special application.

2.4.1.3.2.1 Pressure, Movement and Sound

This study is concerned with communication of data from one machine to another rather than a broadcast of data for general receipt. Pressure, movement and sound media must be considered as directed or ducted devices when the data is transmitted from one machine to another. In general, the frequency response of pressure, movement and sound systems is much lower than that of electrical conductors. In addition, the propagation rate of sound is very much lower than that of electricity, resulting in undue delays where a feedback system is involved. The one great advantage of pressure, movement and sound systems is that they have the inherent ability to transmit relatively large amounts of power from one machine to another and have, therefore, found application in the process control field. In some cases,

it has proved to be economical to use these media as a form of data communication by virtue of the fact that the data already existed as a pressure or movement and would be used as a pressure or movement by the receiving machine.

2.4.1.3.2.2 Electrical Conductivity

At this time, most of the technology used in the design of digital computing equipment utilizes the controlled flow of electrical energy along wires. As a result, all input must be converted into electrical pulses and all output exists as electrical pulses unless otherwise converted. There appears little likelihood that there will be any change in this situation within the next 20 years. If anything, better transducers, microminiaturization of equipment, larger production volumes, and improved production techniques probably will produce an even more entrenched position for the electronics industry. The communication media required for electrical conductivity (a length of wire) is inexpensive. It has a very high propagation rate and a wide bandwidth. In most cases, no transducers are involved since the information both exists, and is required, in electrical form. Without doubt, electrical conductivity will continue to be the major means of machine-to-machine communication in the 1970-1980 period.

2.4.1.3.2.3 Electromagnetic Phonomena

Electromagnetic phonomena including radiated heat, light, and radiowaves, have a propagation rate roughly equal to that of electricity in wire. They possess two drawbacks in their application to machine-to-machine communication:

1) They do not readily lend themselves to "ducting" and, therefore, dissipate large amounts of energy in the process of transmission and allow the receiver to pick up unwanted energy from other sources requiring that the unwanted energy must be filtered out.

2) The transducers required to create a carrier, modulate it, receive it, radiate it, demodulate it and amplify it are relatively less reliable than equipment designed to transmit through a fixed conductor, and their use must be justified and more expensive.

Electromagnetic radiation, does, however, have one advantage as a media for machine-to-machine communication. It allows the rapid transmission of a

wide band of data from one point to another when the two points are mobile in relationship to each other, thereby allowing machine-to-machine communication when one or more pieces of the system is in motion relative to the other pieces. It also allows fast set up of equipment under field conditions since no interconnections are required. For these advantages, electromagnetic radiation pays a heavy penalty in cost, complexity, and unreliability.

2.4.2 Sources of Information

The following sources of information are the ones that have been dealt with to date. It is anticipated that as this study continues, there will be additions made to both the people and companies contacted and the literature used.

2.4.2.1 SOURCES OF INFORMATION - PEOPLE AND COMPANIES

Analex Corp.
Mr. John Simms
Disc Files and Printers

Army Electronic Research & Development Group, Computer Division
Ft. Monmouth, New Jersey
Input-Output Equipment
Mr. Burkhart, 53-51241
Mr. McGee, 53-51446

Bridge, Inc.
Philadelphia
Mr. Lou Sauerwin
Card Readers and Card Punchers

Bryant Computer Products
Disc Files

Control Data Corporation
St. Paul, Minnesota
Mr. Bob Windsor
Peripheral Equipment Dept. Computer Division
Mr. D. E. Lundstrom
Product Planning Peripheral Equipment Division

Cook Electric
Incremental Magnetic Tape Recorder

Data Equipment Co.
Tustin, California
Digital Plotters Graphical Input Methods
Mr. Raymond Davis

Digidata Corp.
4908-46 Ave.
Hyattsville, Maryland
Phone: 301-277-9397
Incremental Magnetic Tape Recorder

Digital Equipment Corp.
Maynard, Massachusetts
Analog-to-Digital and Digital-to-Analog Equipment

General Dynamics Electronics
San Diego, California
Mr. James Redman
Manager, Gov't. Requirements
Mr. R. Glaeser
Manager, Requirements Research Printers

General Kinetics
Variable Speed Magnetic Tape Reader

Honeywell Corp.
Boston, Massachusetts
Mr. Vince Porter and Mr. Dave Bernard
Input-Output Equipment

Philco Corp.
Mr. Gordon Gibbs
Character Recognition

Potter Instrument Co.
Magnetic Tape Transports, Printers

Radio Corporation of America Laboratories
Princeton, New Jersey
Dr. Jan Rajchman
Solid State Magnetic Tape Unit

Soreban Engineering, Inc.
Melbourne, Florida

Royal McBee Industrial Products Division
Paper Tape Equipment

Sylvania Corp.
Newton, Massachusetts
Mr. D. Lilly
Read-only magnetic Cards

Sylvania Corp.
Newton, Massachusetts
Mr. R. D. MacNaughton
Mr. R. A. Barbary
Militarized Magnetic Tape Transport

Tally Corp.
Seattle, Washington
Punched Paper Tape Equipment

Uptime Corp.
Punched Card Equipment

Wyle Labs
Mr. E. Gamson
Input-Output Keyboard & Display Unit

2.4.2.2 Sources of Information - Literature

A list of references pertinent to the study of input-output technology is given in the Bibliography. Some of the material presented in subsequent parts of this section has been extracted from these references. During the remainder of this study, the more pertinent and important of these references will be studied in more detail and new references reflecting materials published or discovered subsequent to the preparation of this Bibliography will be included.

2.4.3 Input-Output Technology Characteristics Required for ANTACCS and Their Application in the Naval Environment.

This Section is largely a requirement function and, therefore, it depends heavily upon information to be obtained from the study being performed by Booze Allen Applied Research, Inc. Work on this section has, therefore, been postponed until better information is available as to the requirement of future Naval Tactical Data Systems and the environment within which they are expected to operate. It is anticipated that the requirement study will furnish information as to the data flow, the sources of data, and the form in which the data occurs or is required. Such information will allow us to obtain a better perspective of the input-output technologies in relationship to the Naval environment.

2.4.4 Current Status Review

The purpose of this section is to provide a review of current technology in the input-output area. It is intended that the technology covered be that technology embodied in currently existing equipment and modifications of current practice.

2.4.4.1 Man-machine Interface

Currently, the man-machine interface has not been heavily exploited. In most computers, there is a man-machine interface in the form of an alphanumeric keyboard and some function switches, both of which are usually used only in conjunction with program debuging and machine operations. Other than this, the man-machine interface seems to be limited to the command and control area where the human must be interfaced as a part of an open loop control system.

2.4.4.1.1 Sound

There is no known present equipment where a human generated sound is used as a computer input. Laboratory work is being done in this area and will be discussed in a later section. However, it is not possible for the systems designer to specify a human generated sound input for current or near current delivery.

2.4.4.1.2 Pressure or Motion

There are three classes of pressure or motion devices that are currently available. These are keyboards, function switches, and position indicators. Theoretically, any of these may be used either off-line or on-line. In practice, certain types of information such as instructions in human language, are stored up for later use while other types of information, such as function selection, are used as a part of a feedback loop.

1) Keyboards

Keyboards are designed primarily to enter symbolic representation of human spoken languages. These symbols or letters are usually supplemented with other non-spoken symbology. Keyboards may be numeric, alphabetic, symbolic or any combination thereof; they can be designed to meet any need.

Although many non-standard keyboards are designed for special purposes, there are three standard keyboards that are accepted in this country: The alphanumeric or typewriter keyboard, the numeric ten key keyboard, and the numeric bank or columnar keyboard. There are many variations within each of these standards. However, there is enough standardization to allow the training of personnel in their operation.

Alphanumeric keyboards are designed to operate at a peak repetition rate for a single character of ten or fifteen times per second. As must alphanumeric keyboards are not interlocked to prevent the simultaneous depression of characters, it is possible to operate such keyboards at speeds up to 20 characters per second providing that the same character is not repeated in sequence. Typical operator rates are about five characters per second when copying from legible data.

Ten-key numeric keyboards are designed to be operated by one hand using the middle three fingers for the digits 1 through 9 and the thumb for zero. There is no horizontal movement of the hands required in such a keyboard and it is possible to obtain fast operator speed. A trained operator can produce output at the rate of ten to twenty characters per second for reasonably long periods of time.

The bank or columnar keyboard provides a column for each digit position. Each column contains all of the digits which may be inserted in that position, usually 1 through 9. This keyboard is a type of forced entry device in that the format is produced in all zeroes except where digits have been added. Further, it is impossible to enter an unacceptable digit in the wrong column. This is avoided by omitting unacceptable digits from the column for that digit position.

The bank keyboard is frequently used in applications where close control over the entry is required. Unlike the ten key keyboard, the bank keyboard is operated by hand movement rather than finger movement and requires the entry of only non-zero digits. A trained operator will enter more than one digit at a time in the bank keyboard by pre-positioning her fingers prior to moving her hand to the keyboard and depressing it. In this manner, the number 871,532,000 would be entered in two movements or key depressions. The 8, 7 and 5 (digits 1, 2 and 4) would first be entered as a single movement by the operator. The operator would then lower her hand on the keyboard and enter the digits 1, 3 and 2 (digit positions 3, 5 and 6). The last three zeroes would not be entered as they are already standing in the machine.

This type of keyboard is particularly desirable where dealing with large numbers that include a number of following zeroes and in applications where a format control is required. Each column is usually interlocked so that not more than one number can be entered. It is, possible to make an error by depressing the wrong digit key. However, it is difficult to make an error in the magnitude of the number such

as might be made with a ten key machine by omitting the last zero or by inserting an extra zero accidentally. Further, as the bank keyboards retain the entered information until released, it is possible to inspect the number prior to entry, and where a series of numbers are to be entered in which only one or two digits are changing, it is possible to let the numbers stand and change only the varying digits.

2) Function Switches

Function Switches represent a form of selection device in which the operator indicates to the machine that he wishes to make a change and have the initiated action taken or not taken by the machine. Usually the function switch is a two-position switch, although it may be a rotary switch or a multiple depression switch in which the color of a light changes with each depression. Function switches may be used singly or they may be used in groups whereby the selection of one function switch from one group modifies a selection of another function from another group.

A systems designer's greatest problem in the use of function switches is usually where to put them. Since each switch represents an idea or "concept communication" to the computer there are usually not enough "finger holes" available to the operator to express all of the ideas that he wishes to communicate. One approach which has been taken to this problem by designers of command and control consoles is to produce a matrix of switches, each of which generates the unique code. This matrix is covered by an overlay which identifies the function of each switch within the matrix (See Fig. 2-22). The matrix overlay is, itself coded in a manner that the computer can sense which overlay is being used, and therefore, by first sensing which overlay is being used and then sensing which switch is being depressed can tell the function to be performed. In this manner, a 10 x 20 matrix of switches with 100 overlays could be used to provide unique identification of 2,000 separate functions. The obvious problem in such a system is

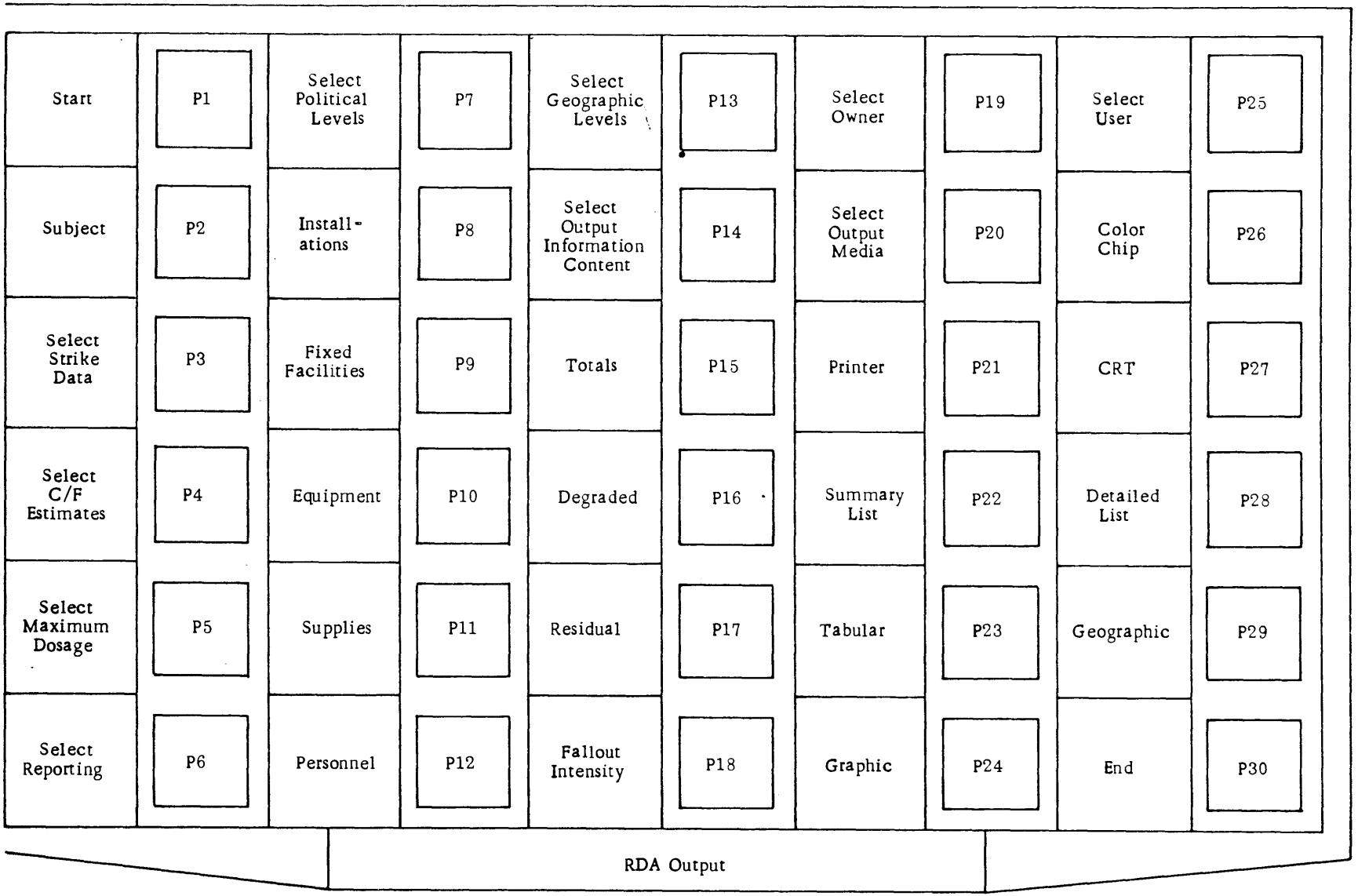


Figure 2-22 Typical Display Overlay

that it takes an excessive amount of time to sort out the correct overlay and position it.

Another approach to the problem is to allow the computer to generate a series of labeled boxes or points on a display, and allow the operator at any time to select any one of these with a light pen or similar device. In this manner, it is possible for the computer to keep the operator continually informed of what switches it is capable of accepting information from. Further, if there are a large number of "overlays" that the computer uses, it is possible to allow the computer to display a number or description for each overlay allowing the operator to select the one which he wants and then choose a switch on an overlay.

Figure 2-23 shows a typical series of operator steps in using function keys.

3) Position Indicators

A wide variety of position indicators suitable for computer input are currently available. They include light pens, panagraphs, etc. Most can be used either on-line or off-line. They depend upon digitizing a series of points of a geometric figure.

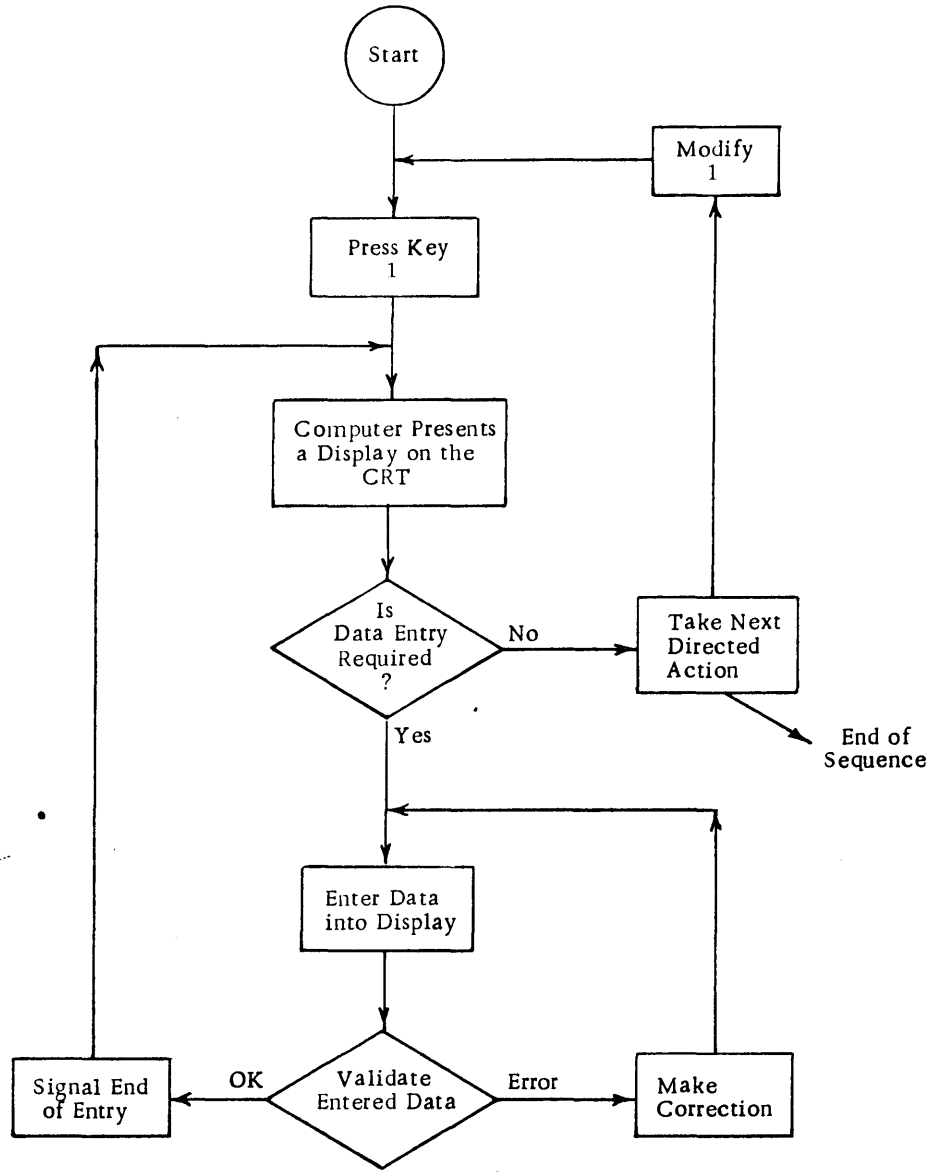


Figure 2-23 Typical Series of Operator Steps in Using Function Keys

2.4.4.1.3 Human Language Interface

The present state-of-the-art of human language interface is currently in the data collection stage. The primary group of devices in this category is character recognition equipment used for alphanumeric and symbolic input from printed and handwritten media. There are currently devices available which can read limited fonts of printed data. Further work is anticipated in this section during the next three months.

2.4.4.2 Machine-Man Interface

2.4.4.2.1 Visual Interface

Two forms of recorded visual interface are currently used as computer output equipment, printed and graphical. Although it is possible for printing equipment to produce graphical output in the form of a series of dots, bars, etc., and for graphical output equipment to produce printing to label the graph, they are separate and well defined classes of equipment which are best separated for detailed study.

2.4.4.2.2 Printed Output Devices

Two basic types of printed output devices are available for use under machine control. They are: the line printer, which produces a line of print at a time, and the character printer or mechanized typewriter, which produces one character at a time.

2.4.4.2.3 Line Printers

Line printers are computer output devices designed to provide a recorded form of human language and symbolic language interface between machines and man. They are designed to print one line of data at a time with the result that a printing speed is dependent on the number of lines printed and independent of the number of characters printed per line or of the total number of characters printed. Such printers can be divided into four classes according to their functional printing characteristics. These classes are:

1) Electromechanical
2) Electro-optical
3) Electrographic
4) Magnetic

1) Electromechanical Printers

Electromechanical printers are characterized by their ability to produce carbon copies. The structure of these printers is such that the paper is set between the controllable mechanical character forming device (type) and a backing. These two are brought into contact at an appropriate time creating pressure between them thereby transferring ink from a ribbon or other source to the paper. This forms the character on the paper. Since mechanical pressure is involved, this machine can produce carbon copies. Since electromechanical printers depend upon an ink transferrence process, it is necessary to somehow renew the ink supply. Moreover, unprepared papers can be used with these printers.

To more readily explore the state-of-the-art of electromechanical line printers, we may divide them into the following seven groups:

a) Rotating Drum Printers
b) Impact Wheel Printers
c) Matrix Printers
d) Stylist Printers
e) Chain Printers
f) Stick and Rack Printers
g) Miscellaneous Printers

a) Rotating Drum Printers (Fig. 2-24)

The rotating drum printer is characterized by a solid drum or series of wheels joined together on a shaft which contains one or more complete type fonts for each column position to be printed. An inked ribbon is passed slowly in front of the type font to provide the source of ink to be transferred. Paper is fed between this inked ribbon, and a hammer or actuator strikes the back of the paper when the desired character is opposite the hammer position. The pressure of the hammer is thus transferred through the piece or pack of paper to the carbon ribbon and thus to the surface of the character on the drum.

Selection of characters is accomplished by indexing the position of the drum and firing the hammer at the appropriate time to print the desired character. Rotating wheel printers are characterized by clean, high-quality impressions of individual characters. However, there is a tendency for smear of the horizontal parts of letters and numbers at high speeds. Such printers are plagued by more or less serious problems of horizontal alignment as a result of timing differences between hammers.

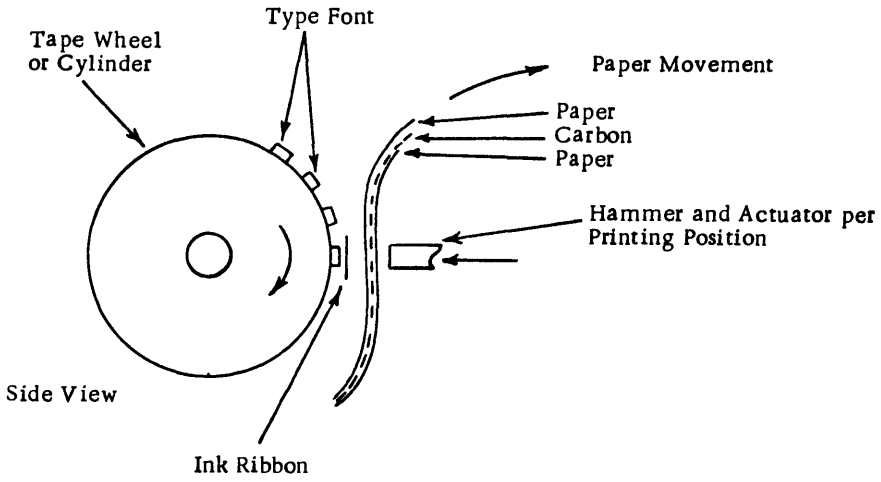


Figure 2-24 Rotating Drum Printer

b) Impact Wheel Printers (Fig. 2-25)

Impact wheel printers are a class of line printer commonly used in adding machines. Such printers are usually limited to numerics and a few symbols, and they operate at relatively low speeds. In this class of printer, a separate wheel is provided for each column position containing all of the digits to be printed in that position. An indexed stop is used to cause the wheel to stop rotating at a point so that the character to be printed will be opposite the print position. All wheels are rotated until they reach a stop position, at which time they are thrown forward against a platen. Interposed between the type and the platen is a carbon ribbon and the paper to be printed.

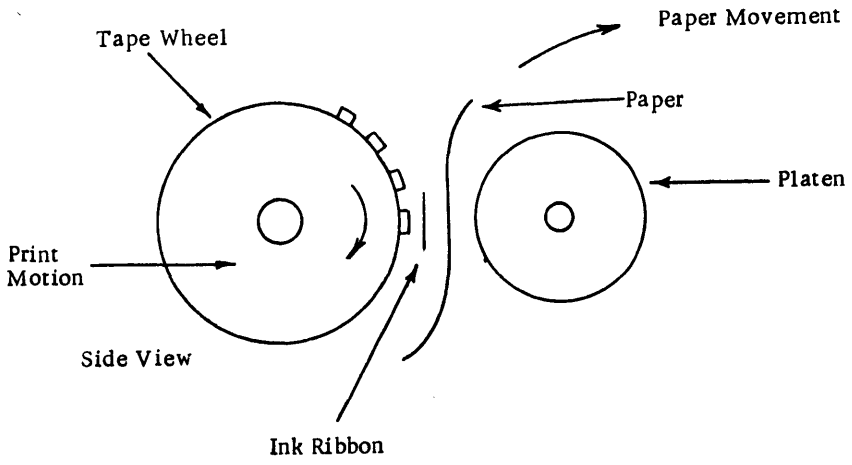


Figure 2-25 Impact Wheel Printer

c) Matrix Printers (Fig. 2-26)

The matrix printer is a mechanism for impressing a number of "dots" on paper to form a character. The dots are formed by the ends of wires which are moved forward by energy supplied from an actuator. These wires are usually placed in a rectangular array causing the printing of a 5 x 7 dot matrix (the smallest matrix which will print all alphabetics and numerics). A character generation device must be used to determine the dots necessary to print the selected character. The number of actuators required for this approach is very large since each wire requires a separate actuator.

As the wires forming the character are fired against the paper through an inked ribbon, the printing occurs from the front rather than the back as with the wheel or cylinder printer. The result is that such printers are capable of producing a greater number of carbon copies than are printers which require that the impact be presented from the back of the pack of paper. Ten or so carbons are usually considered maximum even with relatively thin paper. The use of a small number of wires or dots to form a character results in a low print quality; however, this may sometimes be partially compensated for by the improvement in alignment that results from the simultaneous firing of all wires. Since the character forming matrix is external to the machine, a large number of actuators is required, and since the wires that transfer the force to the paper are small and delicate, these systems require a very high level of maintenance to stay in operation, and they are very complex in their construction.

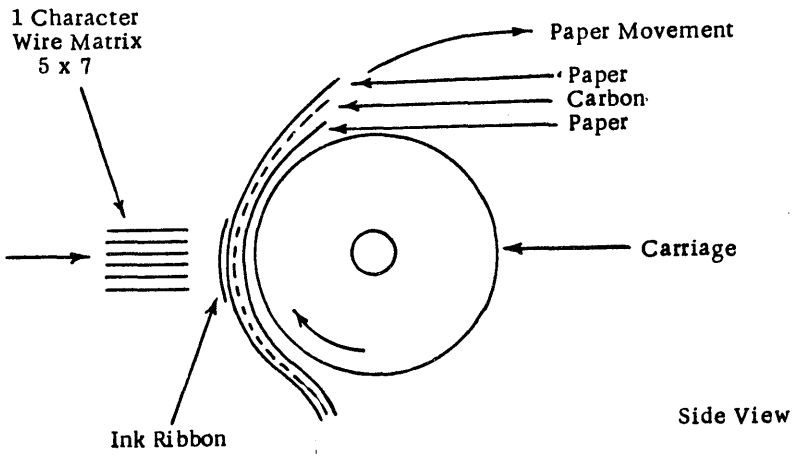


Figure 2-26 Matrix Printer

d) Stylus Printers (Fig. 2-27)

The stylus printer, though an outgrowth of the matrix printer, is quite different in its concept and performance characteristics. As with the matrix printer, a web of paper is passed over a carriage behind an inked ribbon. Printing is by moving a series of styli horizontally between the inked ribbon and a series of actuators (usually one actuator is used for each character position). As the styli move horizontally across the paper, the actuators press them against the inked ribbon at those points where the black part of a letter is crossed. The result is a line of characters composed of a series of horizontal lines that are spaced closely together. The effect achieved is much the same as that obtained by a television raster.

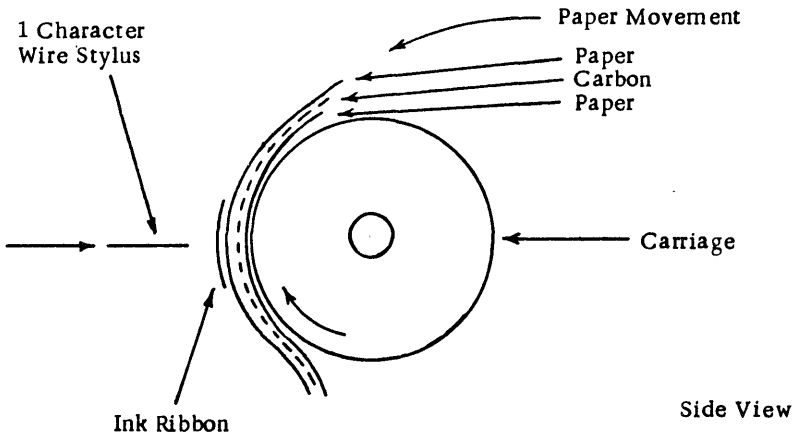


Figure 2-27 Stylus Printer

e) Belt and Chain Printers (Fig. 2-28)

Belt and chain printers are much like wheel and drum printers in their configuration in that an inked ribbon is interposed between the type and the face of the paper, and the character to be printed is selected by firing a hammer against the back of the paper when the selected character reaches that hammer position. The major difference between the two classes of printers is that in the chain printer, type travels parallel to the line of print, and in the wheel printers, type rotates perpendicular to the direction of paper travel. Belt and chain printers are able to produce about the same quality of print, the same number of carbons and with the same speeds as wheel or drum printers. The horizontal movement of the type reduces the horizontal alignment problem that results from the vertical type movement of wheel printers; however, substituted for this is the problem of vertical alignment. Specifically, the horizontal movement of the chain tends to drag the paper in a direction of chain movement and thus pulls the printing out of registration with the background printed on the paper.

Flexing required by the chain or belt limits the top speed that can effectively be reached with the chain printer to somewhat below that which can be reached by the wheel or drum printer in which the type does not flex. Since the chain is travelling in a direction horizontal to that of the paper, it must be at least twice as long as the total line length of the paper. If the line length of the paper is 13 inches (130 characters) it follows that the chain must contain more than twice this number of characters to double back upon itself. The result is that the type font is usually repeated several times on the chain.

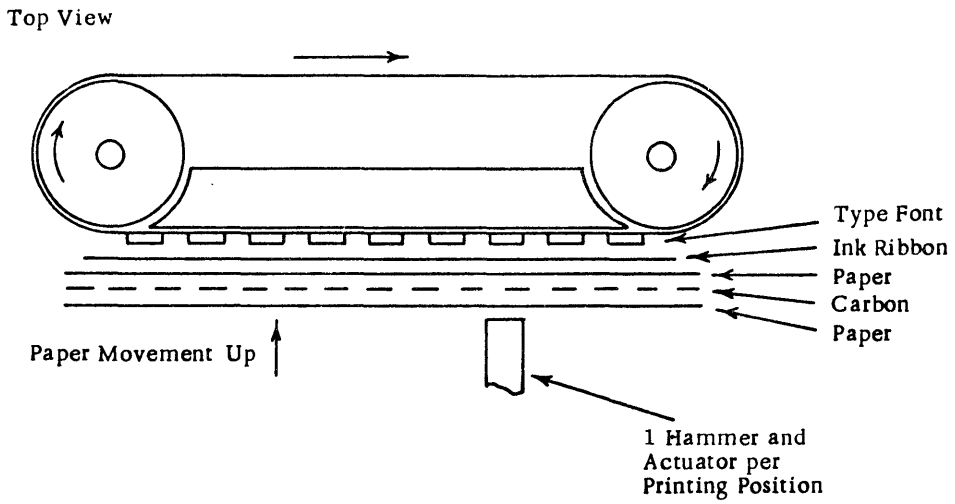


Figure 2-28 Chain Printer

f) Rack and Stick Printers (Fig. 2-29)

Rack and stick printers are an early class of line printer widely used in tabulating equipment and adding machines. Such printers use a bar of type for each columnular position. This bar holds individual sprint loaded pieces of type for each character to be printed in that columnular position. During each print cycle, the bar of type is raised vertically until it reaches a stop which holds it at the position of the character to be printed. When all type bars have been raised to their print position, the print hammers (one for each type bar) are fired against the type bars, thus extending simultaneously selected pieces of type from the type bars. This type impacts against a ribbon transferring ink to the paper which is supported on a platen or roller. During the print cycle, no horizontal or vertical movement of the paper or the type takes place. As a result, it is possible to obtain accurate control of horizontal and vertical alignment upon the form. Type impact is through the ribbon to the front of the form allowing a greater number of copies than can be obtained with the back-hitting technique used by the rotating wheel and chain printers.

Rack and stick printers are inherently slow as the stick or rack of type represents a large reciprocating mass. This, combined with the large number of moving parts, tends to require a relatively higher amount of maintenance per million lines printed than more modern types of printers.

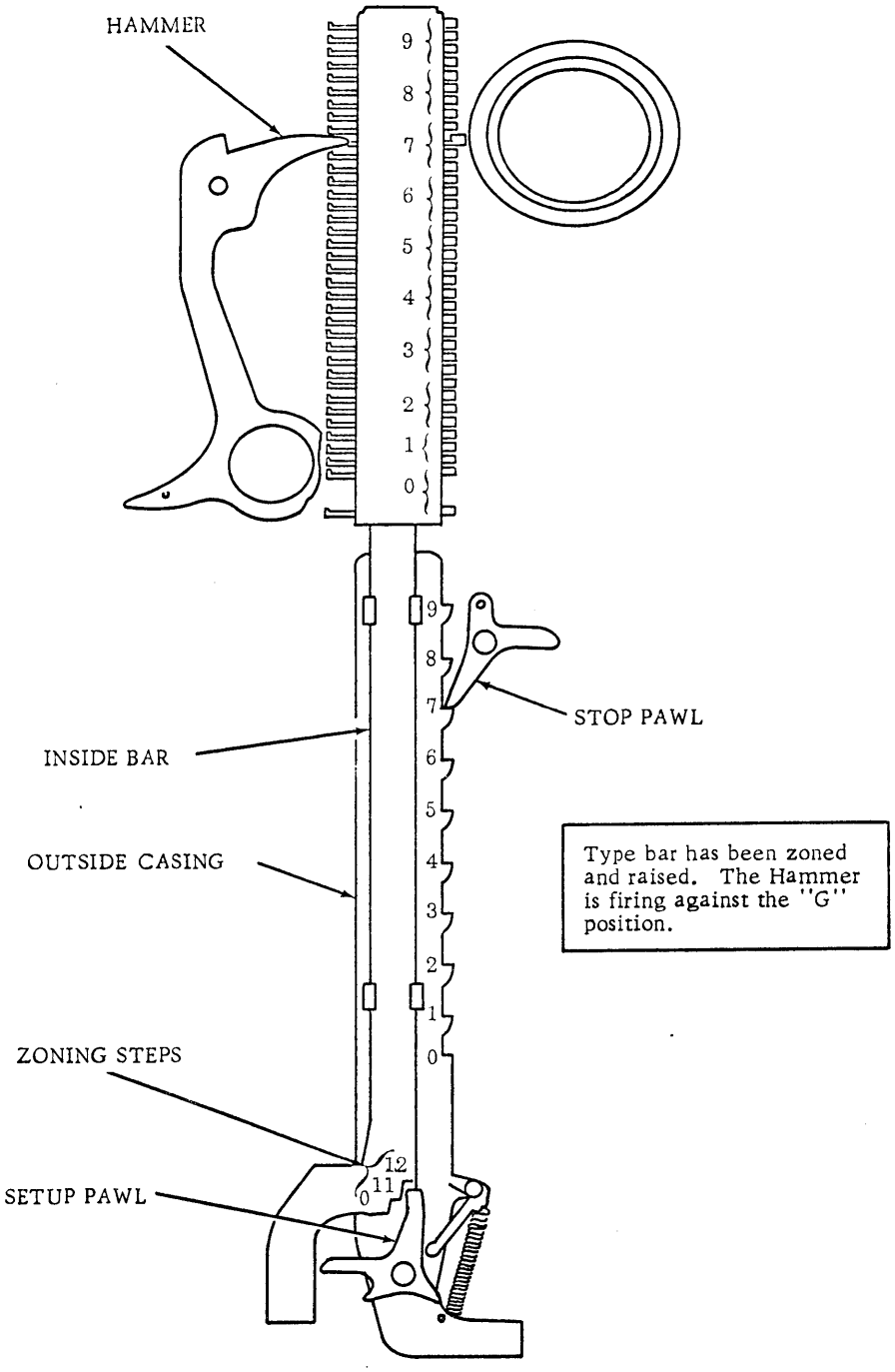


Figure 2-29

Stick-Type Printer Bars

g) Miscellaneous Printers

The hypocycloidic printer, like the stick printer, forces type against the face of the paper with no relative horizontal or vertical movement between the type and the paper during the movement of impact. The type is contained on a type drum in much the same manner as it is on a wheel or drum printer. Unlike the drum printer, the type cylinder of the hypocycloidic printer does not revolve about its center line; rather, it is geared to provide surface motion that advances a line of type perpendicular to the center of rotation, then retracts and rotates one character position.

Although the drum is in continuous rotation at the moment of peak advance, there is no component of relative rotational movement. The result is that printing obtained from such a system exhibits no smear and, except for paper wrinkling, will always be in excellent horizontal and vertical alignment.

Printing may be accomplished either by firing a hammer against the back of the paper or by fixing a stop in position at some time prior to the advance of the type. This stop may be fixed in a forward print position or removed to a no print position. When the line of type advances to the stop, it impinges upon the paper and presses it against the stop when it is in a print position. The stop is not reached and thus no pressure is applied. in a non print position. Such an arrangement requires some flexing in the paper and does not lend itself to the use of a carbon ribbon. Instead, the surface of the type is inked as it would be in a letter press. Conventional inks dry and cake on the face requiring frequent cleaning, so aniline dye is usually used.

Hypocycloidic printers are not well suited to printing many columns or large type fonts since the requirement for strength in the central drive shaft becomes too great. They can effectively produce a limited number of columns of numerics or mixed numerics and symbols. Speed of such devices is relatively slow because the internal drive shaft must make one complete revolution for each character printed. Thus, to print at 100 lines per minute from a 16 character type font, the central shaft must revolve at 1600 revolutions per minute. Hypocycloidic printers have found some application in military situations due to their small number of moving parts and relatively good reliability at low speeds.

In summary, the characteristics of electromechanical line printers are compared in Table 2-2.[5,6,7]

2) Electro-Optical Printers (Fig. 2-30)

The electro-optical printers print by the projection of a direct optical output onto a sensitized surface which is then developed to provide a printed output. As the optical output and character generation equipment used is the same as that used in displays, it will not be discussed in this section.

Probably the best example of an electro-optical printer is the General Dynamics/Electronics SC7330 Printer. This printer is rated at 3000 to 5000 words per minute but can operate over a range of 10 characters per second (100 words per minute) to 71,000 characters per second (on a line basis). The particular printer is designed to print 128 characters per line.

The image generated on the face of the Charactron tube is projected through an optical system onto a sheet of plasticized paper which has previously been given a surface charge. Since the Charactron tube presents the characters in serial fashion across the face of the tube, the character presentation is asynchronous. The light generated from the phosphor is projected through the optical system and falls on the charged surface of the plasticized paper. This charge is held on the paper until it is advanced through a "dusting" bath. At this point, the surface charge in the location of the characters attracts fine particles of black polyethylene dust which temporarily adhere to the surface of the paper. The paper is then advanced at a fixed rate over a heating element that fuses the black polyethylene to the surface of the paper, thus completing the printing process.

The process involved is very similar to the Xerographic process except that the paper is directly charged. The light impinging upon its surface can be used to "fix the charge" and thus attract the "ink" directly to the area to be printed. In the Xerographic process, a selenium drum is used and an electrostatic charge is placed upon it attracting the "ink" to the surface of the drum. The image must then be transferred to an offset roller and then to the paper itself where it is fused in place. Because of the offset nature

TABLE 2-2

CHARACTERISTICS OF ELECTROMECHANICAL LINE PRINTERS

	Rotating Wheel	Chain	Matrix	Stylus	Stick and Rack	Hypo-Cycloidic	Impact Wheel
Print Quality	Good	Good	Poor	Fair to Good	Good	Good	Good
Vertical Alignment	Good	Fair	Good	Good	Excellent	Excellent	Good
Horizontal Alignment	Fair	Fair	Good	Fair	Good	Excellent	Fair
Number of Copies Produced	6	6	10	10	6	2	8
Speed-Lines/Min (with indicated type font)	2000	1100	1000	300	150	300	150
Type Font - No. of Characters	64	48	48	64	37	12	12
Type Font - Variable with Change in Speed	Yes	Yes	Yes	Yes	No	No	No
Electrical Complexity	Low	Low	High	High	Low	Low	Low
Mechanical	Medium	Medium	High	Low	Medium	Low	Low
Maintenance Requirements	Low	Low	Very High	Medium	Medium	Low	Low
Advantages	High Speed						

of Xerography, it is possible to use any type of paper. However, in the process used in the General Dynamics/Electronics printer, a specially plasticized-surface paper must be used. We are informed, however, that this paper is relatively inexpensive and has an indefinite shelf life.

Advantages of a printer such as this are:

1) No moving parts except the paper advance mechanism
2) Very high speed printing
3) Large type font possible (perhaps 200 characters) without decrease in printing speed
4) Type font readily changeable by changing charactron tube
5) Very quiet printing
6) Long life, high reliability with low maintenance
7) Cost
8) Essentially asynchronous operation
9) Can be used to present graphical output
10) Printed output may be used directly as a multilith master

Disadvantages of Charactron Printer are:

1) Produces only original - no copies available
2) In its present form, machine is relatively heavy and bulky.

A similar printer to the General Dynamics unit is the Rank Printer developed by Rank Precision Industries of England. This unit uses the Xerographic principle and a standard cathode ray tube with a resistive voltage divider in the deflection circuits to form individual letters.

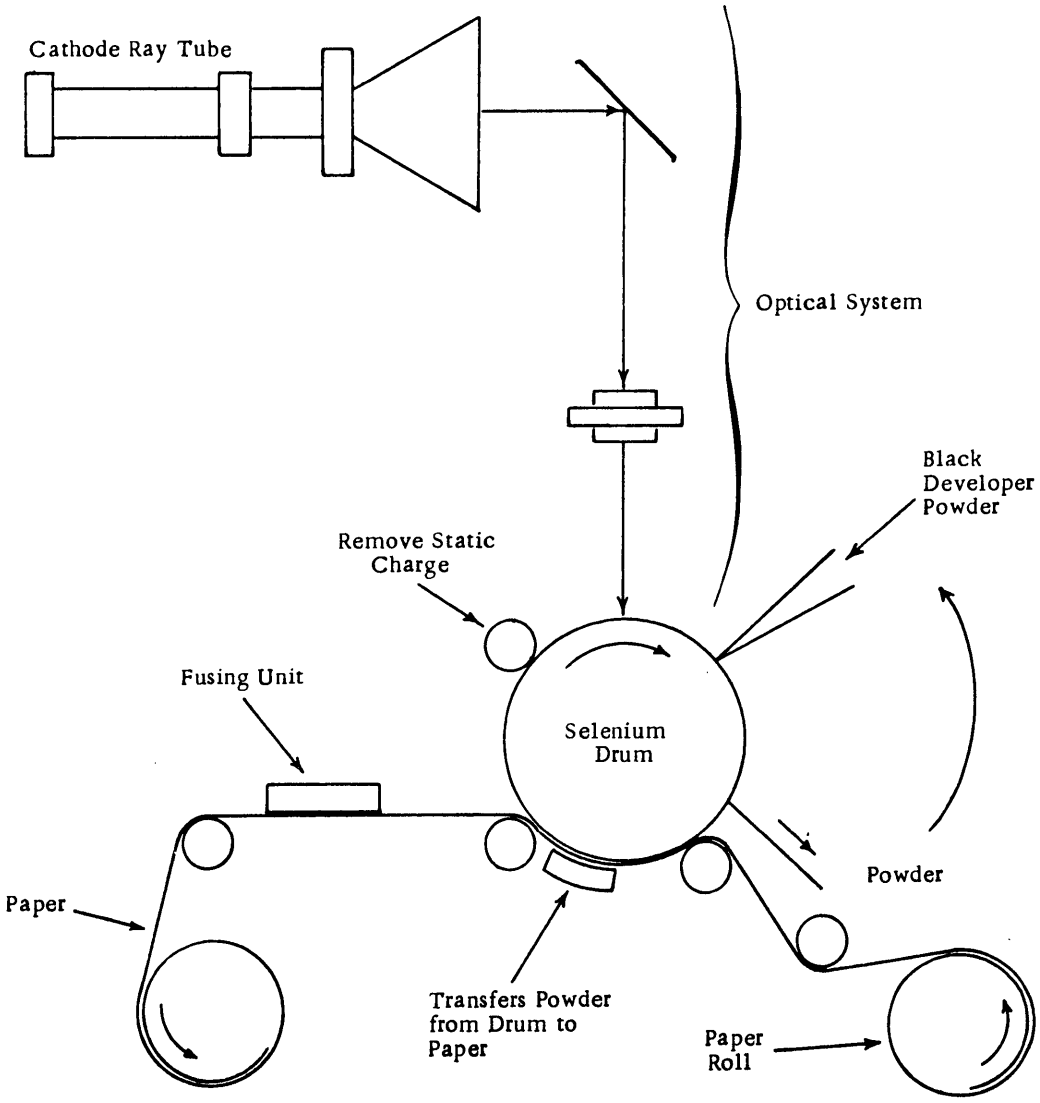


Figure 2-30 Electro-Optical Printer

3) Electrographic Printers (Fig. 2-31)

As yet, there has been little commercial exploitation of the electrographic printer as a computer output device. This is probably due to the requirement for special paper and the difficulties in producing multiple copies.

The electrographic printer requires the use of specially coated paper with high dielectric properties. This paper is moved across the matrix consisting of wires imbedded in plastic. As the paper moves in front of the matrix, it is charged by the selected application of high voltage to the matrix wires. The charged image is developed by running the paper through a hopper containing a "toner" or powdered ink in combination with dies and thermosetting material. The "toner" adheres to the charged areas of the paper and is then carried across the surface of the heating element which fixes the image by melting the thermosetting material enough to fuse it to the surface of the paper.

Systems of this type have been built by Burroughs and A B Dick. The Burroughs System employs a matrix of wires imbedded in plastic in standard 5 x 7 form as the character generation media. The system is able to print at very high speeds, about one or two microseconds per character. As recording takes place in parallel, paper feed becomes the major speed limitation.

The A B Dick electrographic printer uses a special matrix tube built by the Stanford Research Institute. The tube consists of a cathode ray gun aimed toward an assembly of fine wires imbedded in the glass face plate. The electron beam is controlled by character-forming circuits external to the tube. The wires provide a path for the charge from the beam to flow outward to a special coated paper in front of the tube leaving the character as an electrostatic charge on the paper. The use of the vacuum tube is considered a disadvantage for some applications; however, a much higher resolution is obtained than can be obtained with the Burroughs System.

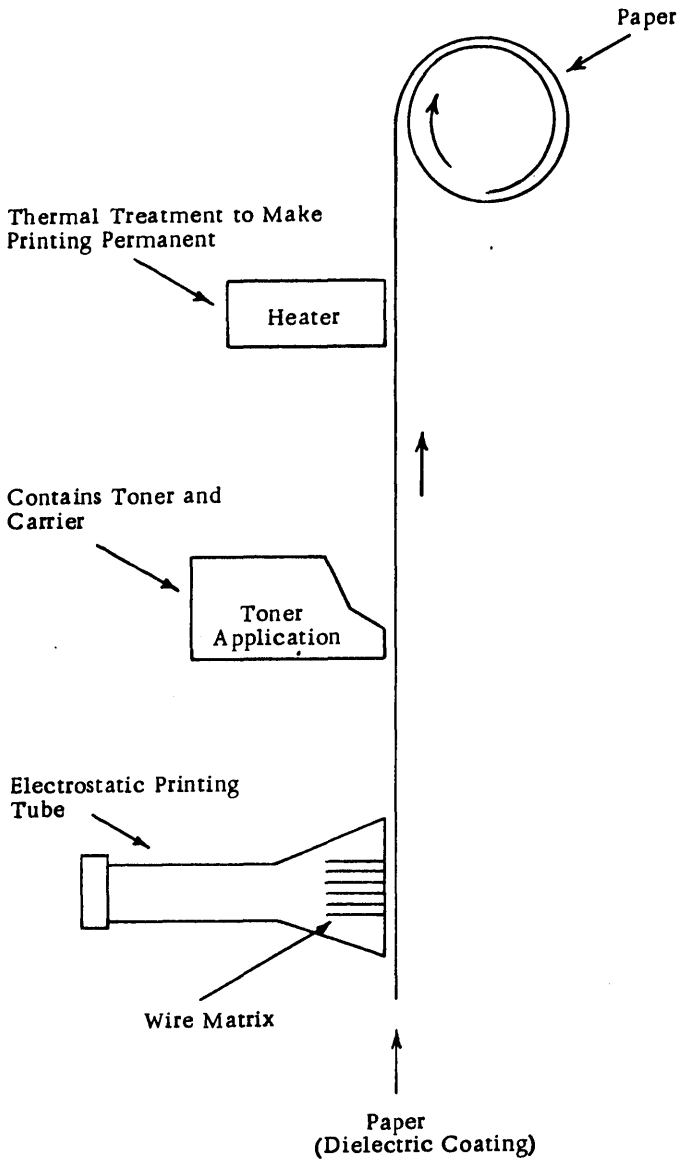


Figure 2-31 Electrographic Printer

A third family of printers uses a Hogan facsimile stylus print head and amplifiers. Printing is in the form of a 7 x 11 matrix on a 10 x 15 dot field with 100 dots per inch.

It is possible for the electrographic printer to produce at least two copies of the same document in a single printing, since the voltage applied is high enough to pass through two sheets of paper simultaneously. As each copy produced requires its own ink hopper and heating element, it is not possible to quickly change from one number of copies to another.

Advantages of electrographic line printers are:

1) very high speeds
2) possibility of more than one copy
3) ability to form large type font
4) simplicity of electrical design

4) Magnetic Printers (Fig. 2-32)

Currently, there are no magnetic printers in production. However, developmental work has been done by the General Electric Corporation, Schenectedy; Univac Division, Sperry Rand Corporation, Philadelphia; and National Cash Register.

The magnetic printer produces a shaped magnetic field which is recorded on a magnetizable surface. This surface is then exposed to some form of magnetic particles which will be attracted to it and form the shape of the magnetized character. This "inked" surface is brought into contact with the paper and the ink is transferred from the magnetized surface to the paper. The ink is fused to the paper and the magnetizable surface is then erased for reuse.

The shaped magnetic field may be created by the use of a magnetized type wheel, matrix or stylus, and the quality of output will depend both upon the character-forming system used and the resolution obtained in magnetization of the magnetizable surface. Like all transfer printing devices, the magnetic printer can produce only original copy. All magnetic printers require the use of magnetic material in the ink.

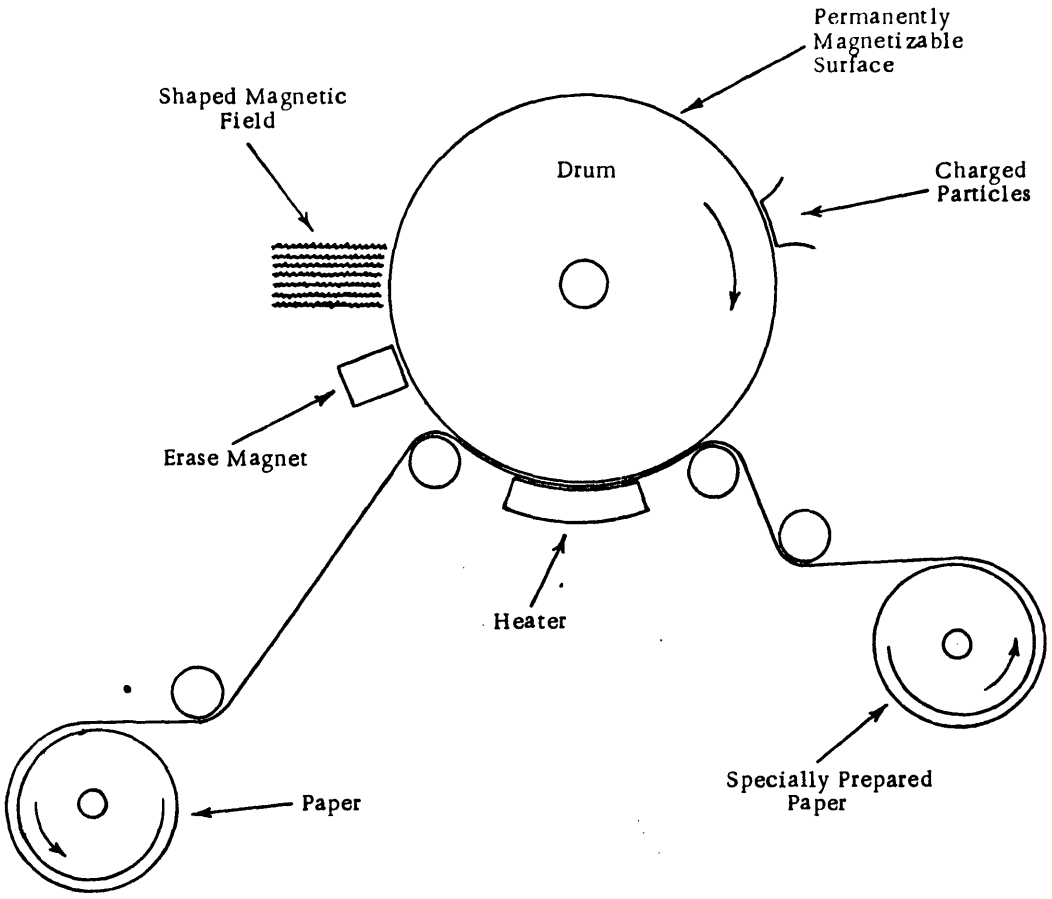


Figure 2-32 Magnetic Printer

2.4.4.2.4 Character Printers

Character printers are computer output devices designed to provide a recorded form of human language and symbolic language interface between the machine and man. They are designed to print one character at a time horizontally across a piece of paper. Printing speed is directly proportional to the number of characters and control actions that must be taken by the printing device. The use of this type of device usually requires a number of special control functions and corresponding special control codes. Typical of these are: space, back space, precedence, e.g. upper and lower case.

The character printer is usually used as a communications device, as a part of a document originating device, as an output on an operator's console, or as a very low speed output device. Character printers are electromechanical in nature and are, therefore, capable of producing carbon copies. All operate at speeds between ten and twenty characters per second and use alphanumeric type fonts. For purposes of detailed examination, electromechanical character printers can be divided into five classes:

1) Typewriter
2) Drum Printers
3) Ball Printers
4) Matrix Printers
5) Stick Printers

1) Typewriters

One of the early forms of character printers was the modified electric typewriter in which the keys were operated under computer control. This type of device is still frequently used and is often found without the keyboard operating solely as a printer. Most such devices are capable of presenting a font of 44 characters. If a precedence code is used, 88 characters are available; however, 26 of these are usually lower case alphabetics leaving a net type font of 62 characters. Most typewriters operate at a maximum speed of 10 to 12 characters per second. This speed is reduced by the time required for the execution of special function codes, e.g. carriage return, back space, carriage shift.

In operation, the typewriter selects one of many levers, each containing a character, and throws it into engagement with a power source in a manner such that the character on the lever is fired against an inked ribbon bringing it into contact with the surface of paper to be printed. The array of type containing levers, or type basket, cannot be moved, with the result that a carriage containing a platen and paper must be moved back and forth in front of the print position of the type basket. Disadvantages of such a system are that the paper must continually be moved both horizontally and vertically, thus putting unusual stress on perforations. As the type basket is a rather complex mechanical arrangement of levers, springs, clutches and pulleys, there are many moving parts that may fail. An advantage of this system is the front impact hammer which allows many carbon copies to be produced.

2) Drum Printers (Fig. 2-33)

The drum printer is an electromechanical character printer in which the type is contained in one or more rows around the circumference, or partial circumference, of a cylinder. This type drum is backed by a carbon ribbon, the paper to be printed, and a hammer. The character to be printed is brought into position by lateral and rotary movements of the type drum.

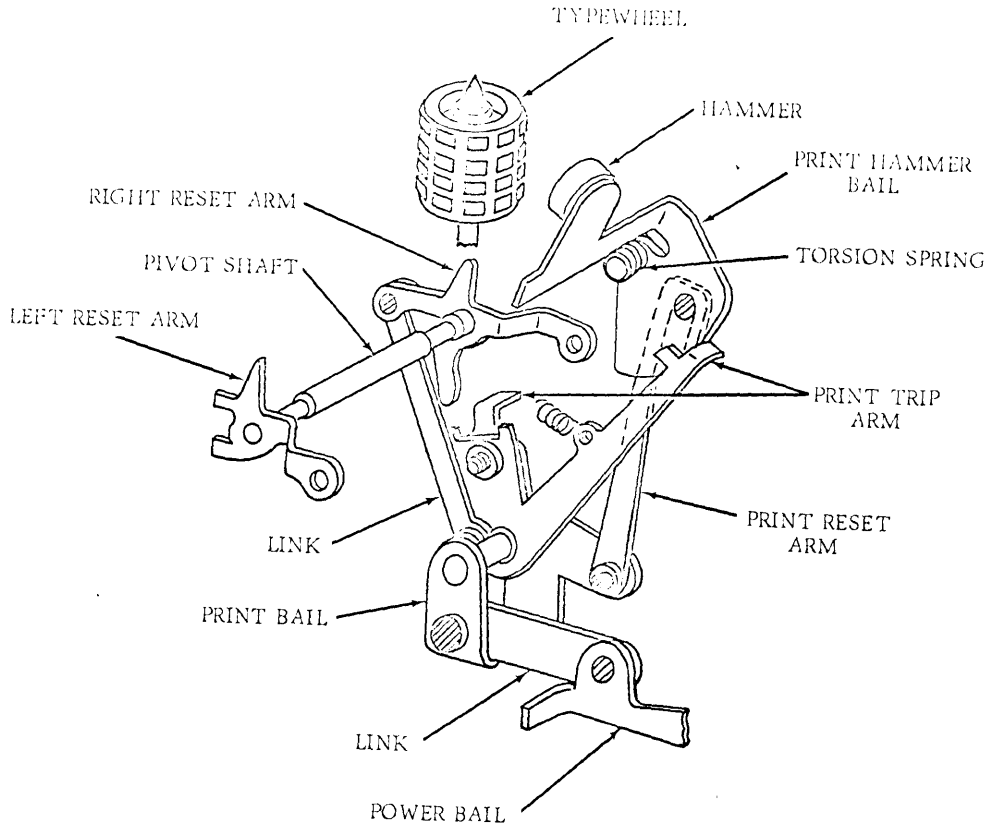


Figure 2-33

Drum Printer

When the proper character is in position, the drum movement is stopped and held in place until the hammer is fired, thus forcing the paper and carbon ribbon forward against the type.

In most present-day drum printers, the paper is held in position by a paper transport mechanism, and the type drum and hammer are moved horizontally across the paper, thus requiring no horizontal paper movement.

3) Ball Printers

Ball printer operation is similar to that of the drum printer except that the characters are formed on the surface of a ball. The character to be printed is selected by a combination of vertical and horizontal rotary movements of the ball bringing it into the selected print position. When the character is in position, the ball is driven against a carbon ribbon printing the character. Character isolation obtained through the use of a ball allows elimination of the back hammer reducing the inertia of the system and allowing faster operating speeds. It allows a front impacting system which produces a greater number of carbon copies. Like the drum printer, the ball printer requires no horizontal movement of the paper, thus contributing toward systems reliability. Ball printers are capable of operating at rates up to 20 characters per second due to their low inertia. Like the drum printer, the ball printer readily lends itself to changes in type font.

4) Matrix Printers

The matrix printer, like the ball printer and typewriter, is a front printing device. Spring loaded type is held in a rectangular matrix in front of a carbon ribbon. Characters are selected by horizontal and vertical movement of the matrix which brings the selected character in line with a hammer. When in proper position, the hammer is fired against the character, thus giving it the inertia to imprint on the paper. Like the ball printer and the drum printer, the matrix is carried horizontally across the face of the paper requiring no horizontal movement of the paper itself.

The most common application of the matrix printer is in teletype operation where it is operated in the range of five to seven characters per second.

5) Stick Printers

The stick printer is similar in concept to the drum printer. The type is held on the face of a hexagonal or octagonal type stick. This type stick is moved horizontally in front of the hammer and rotated to bring the desired character into print position. When in print position, a hammer fires against the rear of the paper bringing it into contact with the carbon ribbon and the selected character. Usually, this type of printer relies more on linear motion than rotary motion in the selection of the character.

In summary, all present electromechanical character printers depend upon selecting a character and bringing it into a fixed position in front of a carbon ribbon and paper array; then applying the necessary force to transfer an image to the paper. In all cases, the character is not in motion at the time of transfer. The result is that a clear image can be obtained from this type of printing. However, this is done at the expense of possible improvements in speed.

In summary, the characteristics of electromechanical character printers are compared in Table 2-3.

TABLE 2-3

ELECTROMECHANICAL CHARACTER PRINTERS

	Typewriter	Drum	Ball	Type Matrix	Type Stick
Pressure Source	Character Front	Hammer Back	Character Front	Character Front	Hammer Back
Changeable Type Font	No	Yes	Yes	No	No
Mechanical Conplexity	High	Medium	Low	Medium	Medium
Speed Char/Sec	12	10	20	8	10

2.4.4.3 Machine-to-Machine Interface

In current technology there are two broad classes of machines which must communicate with each other and with others of their own type. The first of these classes is the analog machine which is an operating simile or analog of the problem being studied. In an electrical analog machine the data is portrayed by a voltage level. The voltage level is continuously varied to correspond to the variations that occur in the function being represented in the real world. The digital machine works with a mathematical model of the real world and expresses all changes as changes to the magnitude of a number in an equation.

To provide communication from an analog machine to another analog machine it is necessary to convert the voltage level of the first machine into a voltage level in the second machine which would represent the same number.

To allow one digital machine to speak with another digital machine, it is necessary for the first machine to convert its digital representation into the code representing the same digit for the other machine.

To allow communication between an analog and digital machine it is necessary for the voltage level to be digitized, or for the digital representation to be converted into a voltage that can be recognized by the other machine.

Provided that two digital machines or two analog machines are designed to operate at the same degree of accuracy, it is possible for them to communicate without loss in the accuracy of the data as no rounding effect is involved. Whenever a digital machine must speak with an analog machine, or vice-versa, a conversion problem is involved and there is some potential loss of accuracy of the data.[8]

2.4.4.3.1 Analog Machines

The problem of analog-to-analog communication has not yet been investigated and will be included in this section at a later date.

2.4.4.3.2 Analog-to-Digital and Digital-to-Analog Machines

This area is currently under investigation; however, current state-of-the-art is not fully explored.

2.4.4.4 Machine-to-Machine Communication--Digital

There are two classes of digital machine-to-machine communication. Real-time transmission and stored data transmission. In real-time transmission concept, data is originated by one machine and transmitted to a second machine which has responsibility for monitoring the line and accepting data as it occurs. (See Figure 2-34). The transmission may be bit serial, character serial, or word serial. Some form of buffering is usually required either on the part of the initiating machine or on the part of the receiving machine. This may take the form of a separate buffer or a buffer that is an integral part of the process. Many problems are involved in scanning a number of such machines by one machine, that is, accepting the data in an order that will assure that no data is lost. This section will deal with a wide variety of machine-to-machine communication including console-to-computer communication, computer-to-console communication, computer-to-computer communication, radar-to-computer communication, weapon-to-computer communication and computer-to-weapon communication, etc.

2.4.4.4.1 Digital Stored Data Communication

In the concept of digital stored data communication, one machine communicates with another machine which is a storage device or "data sink". At some later point in time the same machine, or another machine, reads data from the storage device. The concept is very much like that of using an auxiliary memory, except that communication implies the ability in some manner to remove the data from the machine and place it on another data reading machine. It also implies that the data be read by the second machine in the same manner in which it was recorded by the first machine.

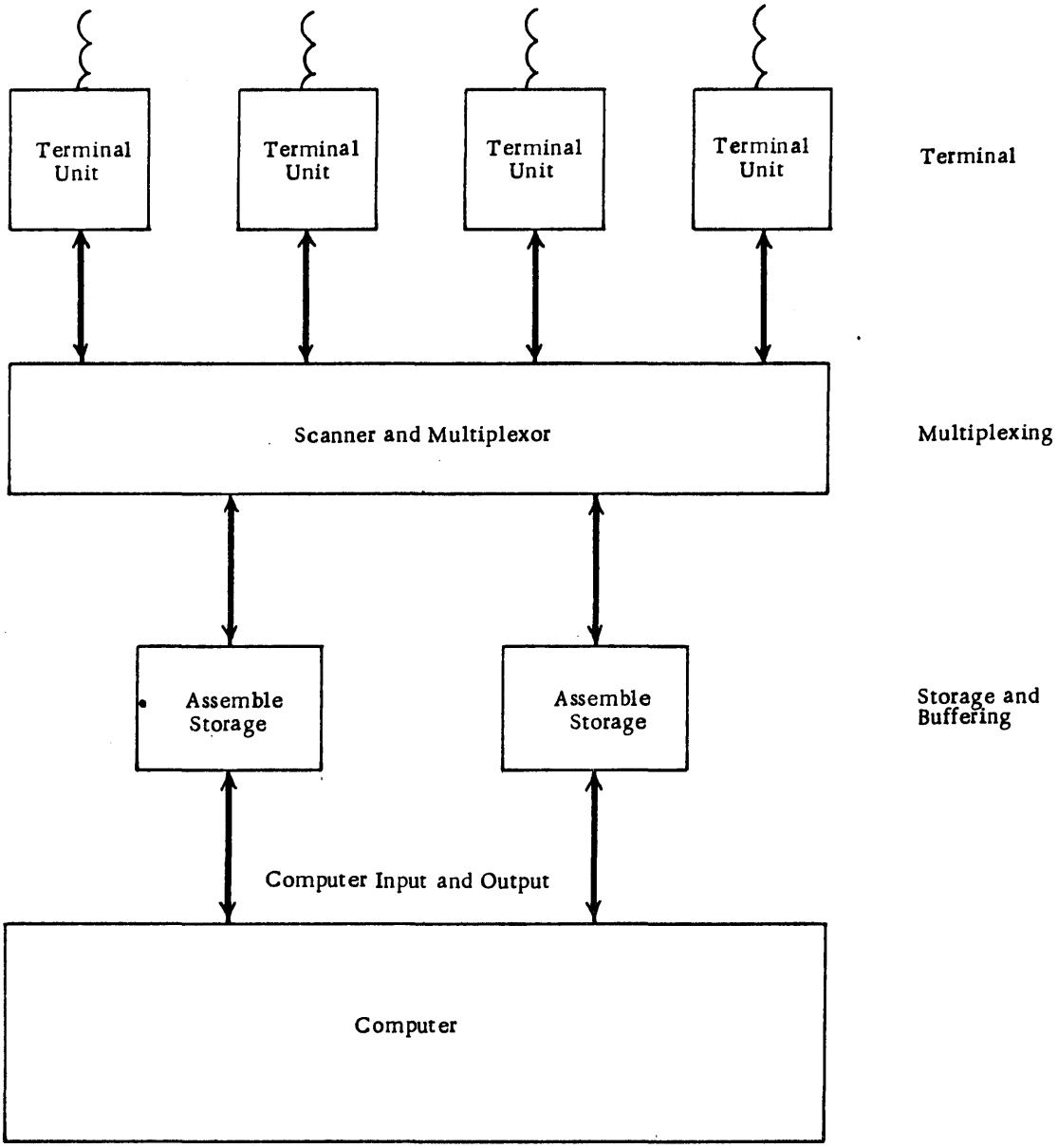


Figure 2-34 Schematic of Typical Interface Functions in Digital Machine-to-Machine Communication

This functional difference separates data storage communication devices such as magnetic tape, paper tape, and punched cards, from the random access storage devices such as core memories, disc files, and drums. This separation is a very real one in practice even though it is possible to build devices with characteristics that are suitable in both applications.

2.4.4.4.2 Punched Cards

Where a unit record storage or communication is required, punch card equipment represents the most economical and most efficient form of existing storage. Card punching equipment is available that will record at rates from one to 300 characters per second, and card reading equipment is available that will read from rates of 1 to 1000 characters per second. Although the cost per bit of storage in this media is relatively high, it can well be justified in certain types of application such as programming and document handling. As the punched card represents a unit record, it is a particular convenience where one machine must create data which must pass through human hands and later be entered into a machine system. A current contender for this field is a combination of printers and character recognition equipment. However, in most applications the punched card is more economical on a per bit handled basis.[9] Detailed examination of present state-of-the-art and developments in punched card equipment is currently underway and will be included at a later date.

2.4.4.4.3 Punched Paper Tape and Incremental Magnetic Tape

Punched paper tape and incremental magnetic tape represent the current state-of-the-art in incremental recorded continuous records. Neither is particularly suitable to the unit record concept. Neither is well suited for document recording. Both are capable of accepting or transmitting character oriented data in an asynchronous fashion without regard to block length. As a result, these devices are useful for interfacing with communications type equipment. They can accept data from a relatively high speed source and record and transmit asynchronously or continuously at a lower speed. They can accept it from an asynchronous or low speed device,

and store it for high speed reading by a faster device. Both record data in a continuous form and in a compact manner such that the data stores itself, e.g. the reel of tape can readily be transmitted from point-to-point without loss of data and without possible change in the ordering of data. The equipment involved to record or read the information is relatively inexpensive and easy to integrate in a system. Currently, a wide range of paper tape equipment is available with recording speeds varying from one to 150 characters per second, and reading speeds varying from one to several thousand characters per second. Although incremental magnetic tape equipment is currently available, it is quite new and will, therefore, be discussed in more detail under available input-output devices in the 1970-1980 period.

Detailed examination of present state-of-the-art and developments in paper tape and incremental magnetic tape is currently underway and will be included at a later date.

2.4.4.4.4 Magnetic Tape Recorders

The magnetic tape recorder as used on a modern computer, provides both a temporary storage device for the computer itself and a medium of transmission of data from one point to another as does paper tape. It can be used at a variety of speeds and can be used as a speed translation device. In its conventional form, it is unlike paper tape equipment in that it is inherently block oriented.

Although it is possible to have a block one character in length and thus turn the tape machine into a character serial device, this is not a practical piece of equipment. Equipment performance is based primarily on start time, (that is, the length of time it is necessary for the tape to achieve the necessary read/write speed) and a combination of the speed at which the tape is passed and the bit density recorded on the tape.

Detailed examination of present state-of-the-art and developments in magnetic tape equipment is currently underway and will be included at a later date.

2.4.5 Availability of Input Devices in 1970-1980

As the input-output study is still in the evaluation stage, any conclusions drawn in this section must be considered as preliminary. Further evaluation will produce much more meaningful content for this section and continuing investigation may disclose new and hitherto unknown concepts which could result in usable input-output devices in the 1970-1980 period.

2.4.5.1 Man-machine Interface

Since little can be done to expand the information output rate of the human, improvements in a man-machine interface must necessarily come from a better utilization of the data passed through this channel. This, in turn, must come about through a more sophisticated man-machine relationship in which the data flow from the man to the machine expresses concepts which are common to the man by virtue of his learning and are common to the machine by virtue of its program. In such a manner, it is possible for the man and machine to establish a "rapport" or working relationship in which, under certain circumstances, only a small amount of information need be passed between the two: the machine assuming what the man will do under certain circumstances, and the man assuming what the machine will do under certain circumstances, thus relieving the load on the interface.

2.4.5.1.1 Sound

Although there is currently much investigation under way as to means of meaningful interpreting the sound patterns produced by humans; and, in spite of the fact that there have been built a number of machines which have been capable of analyzing human originated sounds and distinguishing those sounds from a small vocabulary of words or phrases, it seems unlikely that practical working voice input equipment will be available for use in a tactical data system of the 1970-1980 era.[10]

2.4.5.1.2 Pressure or Motion

Human or language oriented keyboard devices are currently quite highly developed and it seems unlikely that any new breakthroughs will occur in this area. Such devices have, for many years, allowed the human to express himself in his own native languages in a speed in excess of his capability to do so.

2.4.5.1.2.1 Graphical Input

Within the last few years, much work has been done in the development of graphical input devices, and there now exists a number of such devices in laboratory form. From the human standpoint these devices have proved to be a rapid and convenient method of transferring graphic concepts from the man to the computer. Unfortunately, as the computer is much better at algebra than geometry, all such concepts must be handled mathematically and a great deal of software must be prepared before the data transmitted through such a graphical device can be meaningful to the computer. Much work has been done in this area, some of it quite successfully. However, the development of specialized software of this type has proved to be a complex and painful process. It is anticipated that such graphical input devices and their associated software will be available for use in a 1970-1980 system and will be a powerful adjunct to the conventional man-machine interface.

2.4.5.1.3 Human Language Interface

The ability of input equipment to sense a human language representation has been progressing slowly but steadily over the last ten years. Currently, such equipment is available, and without doubt more sophisticated forms will be available in the 1970-1980 period. The problem faced is the degree of sophistication available in this type of equipment. To date, most equipment has been built to order, with the result that there has been little requirement for versatility, and hence the cost of the equipment has been very high. If the development of a mass market occurs within the next few years, we can foresee a substantial increase in the versatility of human language interface equipment as well as a substantial decrease in its cost.[11]

2.4.5.2 Machine-Man Interface

Like the man-machine interface, the machine-man interface is limited largely by the ability of the human to accept a given data rate with a given language. Since the modes of data reception of the human are quite limited and well defined, the only hope for improvement in the machine-man interface is in the improvement of languages of communication between the machine and the man. The last ten years has seen a tremendous increase in the variety of machine-to-man languages. At one time it was necessary for the man to learn the machine language and think and speak in it. Today it is possible for the machine to use some reasonably human oriented languages for human output. It is quite likely that the next five to ten years will see an increase in language availability of considerably greater significance than that during the last five or ten years. If this occurs we can expect the man-machine interface to become as efficient as the present man-to-man interface. It is, in fact, likely that because of the machine's predictability it is possible for the machine-to-man interface to be better than that of the man-to-man interface.

2.4.5.2.1 Man-Machine Interface Visual

Current information indicates no major breakthroughs in the non-display visual interface. There is currently a wide variety of equipment available that will provide graphical presentation of spoken languages. Likewise, there are a wide variety of plotters available to produce graphical output.

The speed range of the so-called high-speed printer used by the computer industry may increase somewhat as a result of improved engineering. The type font and speeds available on photocomposing equipment will probably improve slightly, and there will probably be a substantial decrease in cost. Also, plotters will probably become somewhat faster and somewhat more versatile.

2.4.5.2.2 Auditory

In the past few years there has been a rapid rise in the development of equipment which is capable of selecting a pre-recorded audio message and presenting it upon a digital command. There has also been some work on equipment that is capable of selecting a variety of words and phrases and

combining them into a meaningful message. As yet, there has been little such equipment put "on line" with a computer system. This equipment has manifested itself as automatic airline call systems and selectable sales message systems. There appears to be no reason whatsoever why such equipment cannot be used as a machine-man interface under computer control. In civilian life, there has been a good deal of reluctance to "take orders from the machine". Use of the "open loop" concept in the military does not include the possibility of allowing the machine to present decisions to a commander and allowing him to select from those decisions which, if any, he chooses to make. Having selected a course of action, there is no reason why he cannot allow the computer to issue instructions in a vocal manner just as he might allow it to make up instructions, e.g. orders, texts, etc. in a written note.

2.4.5.3 Machine-Machine Interface

As with current equipment, two types of machine-machine interface will be available. These will be the real-time message interface and the stored message interface. The real-time message interface may occur through any media that is capable of transmitting coded energy. In all likelihood, electromagnetic data transmission will continue to be far more economical than any other means except in special applications. While the columns per disc may go down as the result of an increasing understanding for the nature of data and an improvement in the design of equipment suitable for handling data, it is unlikely that any new data transmitting technique will be found. There are, however, excellent possibilities for the improvement of existing techniques; largely through the study of the nature of data and improvement in coding techniques to allow the transmission of a much greater amount of data on a given bandwidth. Such forms of data compression are most promising under some types of application. It must be kept in mind, however, that they are of greatest usefulness where the total data received can be integrated to achieve an over-all "effect" and where no single bit of data is of vital importance.

As contrasted with data compression techniques, there will probably also be a substantial improvement in the method of coding data to include a greater amount of redundance and, therefore, allow a greater accuracy of transmission and interpretation.

2.4.6 Limitations of Present and Planned Input-Output Technology

The review of this section is not complete at this stage. It will be included in the final report.

2.4.7 Recommended Developments to Meet ANTACCS Requirements

No work has been done on this section as yet as the ANTACCS requirements have not been made available.

2.4.8 Evaluation Criteria Recommended

Evaluation criteria are being established as a part of the evaluation of technology which is currently in process. When requirements information is available, the evaluation criteria for each of the separate technologies will be presented in this section and related to the ANTACCS requirements.

2.4.9 Conclusions and Recommendations

As the input-output technology task is now only 50% complete, it is possible to classify the technologies involved list sources of information and provide limited information on current status and anticipated availability in the 1970-1980 period. However, it is premature to attempt to evaluate their limitations and suitability for the as yet incompletely stated ANTACCS requirement. It is also too early to make recommendation as to future technological developments to provide evaluation criteria or to form recommendations or conclusions.

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2.5 MEMORIES

2.5.1 Classification of Memory Types

Memories can be classified in four functional categories based upon their use and purpose in the system. Each of these categories requires different combinations of speed, capacity, cost and other characteristics. A specific memory technology may overlap two or more categories but the relative importance of different characteristics and, to some extent, the design approaches and criteria vary from one category to another. The four categories used in classifying memories in this report are:

Registers and high-speed control memories
Main high-speed internal memories
On-line auxiliary storage
Off-line auxiliary storage

The high-speed control memory and the high-speed internal memory are normally considered an integral part of the computer or central processor, while the on-line auxiliary storage and the equipment for reading and writing and the off-line auxiliary storage are frequently considered external peripheral devices. However, the techniques used in mechanizing registers and high-speed memory in the central processor are also used for control and buffering functions in special purpose peripheral devices such as communications terminals and certain types of input/output equipments. This is illustrated by the use of the magnetic core matrix memory as a small capacity high-speed control memory, as a large capacity high-speed main internal memory, as a very large capacity slow-speed on-line auxiliary storage, or as a small capacity slow-speed buffer in a display unit or a communication terminal equipment. Although a magnetic core matrix memory would be used in each of the above applications, the combination of characteristics designed into the core memory would be quite different for each of these applications.

The auxiliary storage category represents very large capacity bulk storage that is addressed by the computer in large blocks rather than by individual words. It usually has an average access time several orders of magnitude slower than that of the high-speed internal memory. The on-line auxiliary storage is directly available to the computer under computer control without manual intervention. The off-line auxiliary storage

normally requires a manual operation to place the storage media on the read/write device (e.g. a magnetic tape unit) that is controllable by the computer. In this sense, a magnetic tape unit can be considered an on-line auxiliary storage if a particular reel of tape is written, left on the tape unit, and later read back by the computer. However, if a tape reel is written by the computer, taken off the tape unit, and stored on the shelf to be later put back on a tape unit to be read into the computer again, it would be considered off-line auxiliary storage.

Most off-line storage equipments such as magnetic tape units, punched paper tape equipments, and punched card equipments are commonly classed as input/output equipment since they act as input/output devices to the central processor. Unfortunately, this tends to obscure the fact that these devices are actually serving an off-line auxiliary storage function in the overall system rather than an input/output function. They should not be confused with "true input" and "true output" devices such as keyboards, printers, analog-to-digital converters, and digital-to-analog converters. In this report, these types of off-line storage devices are listed in their conventional category as input/output equipments and have been discussed previously in Section 2.3.

Equipments such as magnetic card memories and magnetic disc files with removable disc stacks are on-line auxiliary storage devices with respect to the cards or discs actually on the device at a given time. However, they act as read/write and access mechanisms for off-line storage with respect to the cartridges of magnetic cards or the stacks of removable discs on a shelf if these have been written by the device previously and will be read by the device subsequently. In this report, these devices are discussed in the category of on-line auxiliary storage. Those that can act as read/write mechanisms for off-line storage will be identified.

In addition to four major categories discussed above, certain memories can be classed in a fifth category--"special memories." This category would include:

Read-only memories
Read-mostly memories
Associative memories
Analog memories

While some of these special memories may be mechanized with completely different techniques than those in the other categories (e.g. photographic read only memory), others may be mechanized with essentially the same basic techniques but with additional control and logical functions or, in some cases, with certain hardware omitted (e.g. thin-film read only memory).

2.5.2 Sources of Information

2.5.2.1 People and Organization

Memories have been discussed with personnel of a number of different companies and governmental agencies in the course of this study. The following list indicates the companies and governmental agencies with whom memories have been discussed and the type of memories duscussed with each:

Rome Air Development Center Rome, New York	Cryogenic Memories, Random Access Memories, Non-Rotating Mass Memories, Cryogenic Associative Memories, Magnetic Associative Memories
Control Data Corporation St. Paul, Minnesota	Magnetic Thin Film Memories
Remington Rand, Univac St. Paul, Minnesota	Coincident Current Magnetic Core Matrix Mems., Word Organized Magnetic Core Matrix Memories, Magnetic Thin Film Memories, Associative Memories
Bunker-Ramo Corporation Canoga Park, California	Woven Screen Memories, Biax Associative Memories, Thin Film Plated Wire Assoc. Memories, Transfluxor Associative Memories,
Fabritek Emery, Wisconsin	Coincident-Current Magnetic Core Matrix Memories, Magnetic Thin-Film Memories
N C R Hawthorne, California	Plated Magnetic Rod Memories Photochromic Memories
Sylvania Waltham, Massachusetts	Permanent "unit-record" magnetic card memories
Philco Research Lab. Newport Beach, California	Magnetic Thin-Film Memories, Biax read-mostly memory, Biax associative memory

RCA Laboratories Princeton, New Jersey	Cryogenic Random-Access Memories, Cryogenic Associative Memories, Laminated Ferrite Memories
Laboratory for Electronics Boston, Massachusetts	Permalloy Sheet Random-Access Memories, Bernoulli-Disc Rotating Memories, Bernoulli-Disc Mass Memories
Autonetics, Anaheim, California	Memory Systems and Hierarchies
U.S. Army Engineering Research and Development Lab., Fort Monmouth, N.J.	Block Oriented Random-Access Memories, (static ferro-acoustic storage), Memory Systems and Hierarchies, Magneto-optical and Electro-optical Memories for Displays, Glass delay-line Memories
Office of Naval Research Washington, D.C.	Magnetic Core Memories, Read only Memories, Cryogenic Memories, Associative Memories, Optical Memories
National Security Agency Fort Mead, Maryland	Thin-Film Memories Cryogenic Memories
U.S. Navy Bureau of Ships Washington, D.C.	Associative Memories, Magnetic Disc Files, Magnetic Card Memories
Hughes Ground Systems Division Fullerton, California	Associative Memories, Magnetic Domain Wall Shift Registers

Much of the information presented in subsequent parts of this section is based on discussions with memory experts in the organizations listed above. In addition to discussing memory techniques that have not been adequately described in published literature, the opinions of these experts concerning the advantages, disadvantages, limitations, and future of different memory techniques were solicited.

2.5.2.2 Literature

An extensive list of references pertinent to the study of memory technology are given in the Bibliography. Most of these references have been scanned, but only a limited number of the more important ones have been studied in detail to date. Some of the material presented in subsequent parts of this section on memory technology has been extracted from some of these references. In some cases, where noted, direct quotations have been used. During the remainder of this study, the more pertinent and important of these references will be studied in detail and new references reflecting materials published or discovered subsequent to the preparation of this Bibliography will be included.

2.5.3 Memory Characteristics for ANTACCS

The characteristics required for memories in ANTACCS cannot be fully identified at this time since the results of the requirements analysis have not been available. However, it is certain that registers and high-speed control memories, main high-speed internal memories, on-line auxiliary storage, and off-line auxiliary storage will all be required in a future Naval Tactical Data System.

It is anticipated that the results of the requirements analysis and further studies in the area of machine organization will indicate whether requirements exist for any special memories.

In the way that the study of memory technology is being handled, it will not be materially affected by the results of the requirements analysis except in some detailed areas such as environmental conditions. All of the more important and more feasible types of memories that might be applicable to 1970 systems of either the ANTACCS or AMTACCS types are being analyzed and will be evaluated and compared. Memories meeting only commercial specifications and those for aerospace requirements are not being considered, but the memory technologies being studied will cover the full range of requirements for shipboard and ground-based military environments. Types of memories required for particular functions in a computer, or in other parts of the system, can be selected based on the characteristics that will be listed

and compared. The memories to be studied, compared, and evaluated will encompass all types necessary to meet all of the functional requirements in these systems--both in the central processor and in peripheral and auxiliary equipment.

2.5.4 Applications of Memories in the Naval Environment

It is anticipated that all memory requirements for shipboard and ground based military environments will be covered by this study. Applications of memories in ANTACCS and AMTACCS systems will include high-speed control memories, high-speed internal memories for program and data storage, on-line and off-line auxiliary memories for storage of multiple alternate programs, large data files, and historical records, control registers and buffers for input/output equipment, communication terminal equipments, and display equipments and status registers. The applicability of specific types of memories to different applications will be considered in further detail in the remainder of this study.

2.5.5 Current Status Review

2.5.5.1 Specific Memory Techniques Investigated to Date

In addition to the conventional magnetic core matrix memories, magnetic surface storage memories (e.g. tapes, drums, discs, cards) and delay line memories, the following types of memories have been investigated so far during the study:

Continuous-sheet cryogenic random access memories
Cryogenic associative memories
Magnetic associative memories
Planar magnetic thin-film memories
Cylindrical magnetic thin-film memories
Woven screen memories
Permanent magnetic unit record card
The laminated ferrite memory
The flute memory
The permalloy sheet memory, and
Ferro acoustic memories

A brief description of each of these memory techniques is given, and the information collected to date is summarized in this section. However, these memories have not been analyzed, compared, and evaluated in detail at this time.

2.5.5.2 Continuous-Sheet Cryogenic Random-Access Memories

Cryogenic memories are based on the principle that at temperatures near absolute zero degrees, the resistance of certain materials (superconductors) may be either zero or some finite non-zero resistance depending upon the magnitude of the magnetic field surrounding the superconductor. In one type of continuous-sheet cryogenic memory under development by RCA Laboratories, the storage media is a superconducting tin film. This tin film, a lead sense line, and lead drive strips are fabricated by vacuum deposition techniques on a two-inch square substrate.[1] These metallic films are all insulated from one another by vacuum deposited insulating films (silicon monoxide). The sense line is beneath the storage plane and is oriented diagonally to and directly under the intersections of the two sets of drive strips which are orthogonal to one another.

Coincidence of the "X" and "Y" drive currents at an intersection of the drive strips produces a magnetic field sufficiently strong to switch the region of the storage plane beneath the intersection out of the superconducting state, thus permitting magnetic flux to link through the plane in that region. When the currents are removed, the flux linking the small region of the continuous sheet is trapped, and persistent currents are established in the storage plane to support this trapped flux. The stored information can be read by subsequently applying a coincidence of drive currents of proper polarity, and then sensing the voltage change on the sense line.

In a later refinement, a cavity sensing technique is used rather than a zigzag sense line. A second continuous tin film is located a slight distance beneath the storage plane and connected to it electrically along one edge. In this case, when the proper polarity drive currents create a magnetic field sufficient to destroy the superconducting state in the region of the intersection, a change of flux is created within the cavity beneath the intersection between the storage plane and the sense plane. This causes a sense pulse at the output tabs connected to the sense plane.

This memory is made by batch-fabrication techniques. The continuous sheet superconducting storage film and sense film and the X and Y drive strips are vacuum deposited for an entire plane. In addition, the X and Y selection matrix is mechanized by means of cryotrons that are vacuum deposited on the same plane and connected to the drive strips by the deposition process.

A 16,384 bit memory plane, including 508 cryotrons for XY selection, is fabricated in 26 vacuum deposition steps using 16 different masks. The planar density is approximately 10,000 bits per square inch. The anticipated characteristics for this memory are:

$\frac{1}{2}$ to 1 microsecond access time per word
10^6 bits in a 10-inch square plane
10^9 bits in a complete memory
production capability during 1964
300 ma selection current
100 ma drive current
10^9 bit memory will cost approximately $1,000,000

A 16,384 bit plane (128 x 128) with cryotron addressing on the same 2-inch square cryogenic plane has been in operation at this time.

RCA considers the next step to be a 256,000 bit plane with 0.0005 inch spacing between wires on a four-inch square plane. Planes of 1024 x 1024 are an eventual goal. By 1965, RCA anticipates that they will have a 10^7 bit prototype memory.

Because of the basic overhead cost in the refrigerant, the cryogenic memory is not considered a good approach to a small memory, but becomes more advantageous as the size increases. RCA believes that the cryogenic approach is the more likely way to reach capacities of 10^9 bits, but that the laminated ferrite memory will be better for capacities of 10^7 bits. The crossover between the two will occur somewhere between 10^7 and 10^8 bits. The present cryogenic memory design is limited to cycle times of 1-2 microseconds because of the cryotrons used in the selection matrix.

To date, RCA has fabricated two good arrays (128 x 128), but both of these have been damaged by repeatedly taking them in and out of the liquid helium. They are now working on ten arrays for the Air Force.

2.5.5.3 Cryogenic Associative Memories

Work on cryogenic associative memories has also been underway at several companies.[2,3] The cryogenic approach is probably worthwhile only for very large capacity associative memories. The cryogenic associative memory under development at RCA is essentially a two "core" per bit type using two parallel continuous sheet planes. The associative feature depends upon whether a corresponding spot in both planes is storing the same information. If they are not, the flux between the two planes cancels out. The RCA continuous sheet cryogenic memory uses lead for the super-conductive wiring, tin for the continuous-sheet superconductive storage planes and silicon monoxide for the insulators. These are all deposited in approximately 20 different deposition steps with different masks for each. Fabrication is currently mechanized, with a circular jig holding the 20 masks in the vacuum so that each mask can be rotated into place at the proper time.

2.5.5.4 Magnetic Associative Memory

The term associative memory is used to refer to a memory which is addressed by content rather than by a unique numeric address. An associative memory involves sufficient logical capability to permit all memory locations to be searched essentially simultaneously--i.e. within some specified memory cycle time. The search may be made on the basis of the entire contents of each location or upon the basis of selected bit positions of each location. Thus, it is possible to search for all words meeting certain criteria or for all words in which a certain tag portion of the word meets the criteria. Searches may be made on the basis of equality, greater-than-or-equal-to, less-than-or-equal-to, and between limits.

Associative memories are also referred to as content addressed memories and search memories. In a sense, all of these terms are misleading in that the unit is not an associative "memory" but rather an associative "processor" since the memory function involves a minor portion of the total hardware and costs. The major portion of the hardware and costs is that involved in the logical operations necessary to accomplish the parallel search of memory locations. For example, a magnetic associative memory frequently requires a sense amplifier for each word location, and logical capability for each word (in some cases for each bit portion) to permit the parallel search

capability. These hardware elements are not required for the memory function itself. The memory function alone might account for only 1/4 or 1/5 of the total costs based on comparing the costs of the associative memory with that of a random-access memory with equivalent capacity and access time.

An associative memory differs from most random access memories from a hardware standpoint in the following ways:

1) The sense lines are word oriented
2) The drive lines are bit oriented
3) There is a large number of sense amplifiers as a result of the word orientation of the sense line
4) The sense amplifiers have a high duty cycle which tends to make them more expensive
5) A large amount of logical circuitry is required

The costs of the sense amplifiers and logical circuitry are the main factors contributing to excessive costs of associative memories compared to those of random-access memories. An associative memory also requires a non-destructive-read-out storage element since it is not feasible to rewrite every word location for each search.

Although some magnetic associative memories use a single aperture magnetic core, it is convenient to use a multi-aperture device such as the Transfluxor or the Biax element. The Transfluxor approach requires two elements per bit and requires a greater drive signal since it is necessary to actually change the direction of saturation of the material around the interrogate hole. The Biax element requires a relatively expensive sense amplifier, but it is attractive for associative memories for three reasons:

1) A fast read capability
2) A non-destructive read-out feature
3) A bipolar sense signal

Cylindrical thin film plated wires are also being investigated for associative memory applications. The cylindrical thin film plated wire appears attractive in that it offers the possibility of a large sense signal resulting from the closed magnetic path, and requires a relatively small read write drive current.

The work at Bunker-Ramo Corporation on an associative memory under a Navy Bureau of Ships contract illustrates the Biax approach to associative memories.[4] This associative memory will store 2048 words of 36 bits each. It will have the ability to search the entire memory for an exact match, for greater than, for less than, for between limits, and for simultaneous or successive combinations of these. It will also provide for arbitrary masking to control the bit positions on which the search is based. The results of the search can indicate match or no match, a count of the number of locations upon which a match was obtained, the addresses of all positions in which a match was obtained, or the data contained in each location in which a match was obtained. Optionally, all matched words can be modified automatically after a search. The basic search rate is 100 nanoseconds per bit position for an exact match. Therefore, a search of all 26 bit positions of the entire memory would require 3.6 microseconds. For all other search modes, 300 nonoseconds per bit position are required--10.8 microseconds to search on all 36 bits. As a conventional read-write memory, the cycle time is 6 microseconds.

One hole of the Biax memory is wired as a conventional coincident current read/write memory, using the Biax element in the same way that a simple magnetic core would be used. The orthogonal hole is then used for the associative feature. In the associative mode, given bit positions of all words are interrogated simultaneously, and successive bit positions of the memory are interrogated sequentially. All bits of a given word are sensed by the same sense wire, so that a sequential signal corresponding to the sequencing through the bit positions is obtained from an individual sense amplifier for each word position. The interrogation is conducted so that a negative signal from the bipolar sense signal during the active part of the cycle indicates the absence of a match. Therefore, the indication of any negative signals from a particular sense amplifier during this active period indicates a match for equality in that word position. The determination of greater than or less than is accomplished by noting the bit position from which the first negative signal occurs for a particular word. This signal, indicating a difference in that bit position, combined with the indication of whether the control word has a one or a zero in that bit position will then indicate which is greater.

2.5.5.5 Planar Magnetic Thin Film Memories

In most of the approaches to planar magnetic thin film memories, an array of discrete elements is fabricated by vacuum deposition processes on a substrate such as glass.[5,6,7,8] Each element is about 1,000 angstroms thick and is approximately 25 x 50 mils in area. The X and Y drive lines are either vacuum deposited on the same substrate with appropriate insulation between them or, in some cases, the drive lines and sense lines are fabricated on a separate substrate which is then mechanically superimposed over the one containing the magnetic elements.

Most memories of this type depend upon a predetermined orientation of the magnetic domain based on the use of anisotropic material to provide an "easy access" in one direction. The electrical signals then attempt to rotate the direction of orientation of the magnetic domains. The fluxes resulting from the electrical signals leave the orientation of the magnetic domains in other than their normal condition. This type memory can be read non-destructively by disturbing the orientation of the magnetic domains which, when the disturbing signal is removed, return to their previous condition, due to the anisotropic material.

Since this type of magnetic memory does not use a closed flux path, very low sense signals are generated. The greatest difficulty with this type of memory has been in achieving adequate uniformity in the individual elements deposited on a plane. Uniformity is a particularly serious problem since it depends upon the magnetic orientation of the deposited material as well as upon the physical uniformity of the element. The lack of a closed flux path further contributes to the problems resulting from lack of uniformity. Because of these problems, this type of memory is usually operated in a work-oriented fashion rather than a coincident current mode. This increases the cost of the associated electronics. On the other hand, the use of domain wall rotation and the absence of a closed flux path permit higher speed operation in this type of memory than in a magnetic core matrix memory.

Many companies are working on magnetic thin-film memories. It has been predicted that within the next few years they will replace magnetic core matrix memories for those high speed applications (less than 1 microsecond cycle time) in which linear-select core memoreis are now used. However, it is considered unlikely that they will replace coincident current magnetic core matrix memoreis for large capacity, slower speed applications (cycle times of 2 microseconds or greater).

Thin-film elements can now be rotated in approximately one nanosecond, but the associated electronics cause selection to take at least 35 nanoseconds. Thin-film memories can provide non-destructive read out, require less power than core memories, and are batch fabricated. However, the low sense signal level requires a good differential amplifier; fast rise time circuits are required, and it is difficult to adequately control the magnetic variables to produce uniform elements. Memories of 4000 words capacity with 100 nanosecond cycle times, and 64,000 word memories with 500 nanosecond cycle times appear reasonable for the future.

The 400 nanosecond cycle time thin-film memory now being made by Fabritek for Johnsville Naval Air Station is typical of the current advanced work in thin-film memories. This memory is word-organized, contains 1024 words of 50 bits each, and operates in a 400 nanosecond cycle time. The array is composed of film deposits approximately 900 angstroms thick that are rectangular in shape, measuring 25 x 50 mil. A single film is used for each bit.

Both X and Y axis lines are superimposed on the same printed circuit card with a plastic deposit separating them. The digit lines are approximately 32 mil wide, each consisting of two 10-mil lines separated by a 12-mil gap. The two 10-mil lines are joined at both ends of the board and are terminated in a plated-through hole for interconnection. The drive line is approximately 23 mil wide, each consisting of two 9-mil lines divided by a five-mil gap. The drive lines are also reconnected at both ends in plated holes, which are fed through to the opposite side of the adjoining board, and fed back parallel to the first line to provide a proper termination, and to provide noise cancelling. Each memory plane consists of a total of 112 substrates which are placed on a single printed circuit board. This is done to

reduce the number of interconnections involved on the board and to decrease the total number of film spots that are deposited on a single substrate thus increasing the yield. The reverse printed circuit board is placed over the film, and the total assembly is bolted together between two holding plates. The drive and sense lines are then terminated.

Manufacturing costs of current film stacks are between 20¢ and 50¢ a bit. Fabritek's objective is to develop a film plane within the next year costing approximately 5¢ a bit. The anticipated cost breakdown would be 2¢ per bit for the deposited tested film element, 1¢ per bit for the overlay, 1¢ per bit for plane assembly and test, and 1¢ per bit for final stack assembly and final test. These costs are for the fabricated planes only and do not include electronics.

Some companies have also investigated closed flux path thin-film memories. This approach is illustrated by the work at Philco Research Laboratory in Newport Beach, California, where a closed flux path thin-film memory is fabricated by first depositing a magnetic thin-film element, depositing a conductor on top of that, and finally depositing a second thin-film element on top of the conductor to close the flux path around the conductor. Philco believes that this closed flux path approach will permit thin-film memories to be operated with approximately 1/10 of the drive current (100 milliamps) of single element planar thin films, while providing larger sense output signals due to the complete switching of the flux. Such memories should also be less critical to variations in the element characteristics because of the closed flux path.

Small capacity magnetic thin-film memories have already been used in several computers to provide a few hundred words capacity for multiple high-speed registers requiring read/write cycle times of fractions of a microsecond. In one machine, a small magnetic thin-film memory is used to mechanize multiple arithmetic control registers. In another, a magnetic thin-film memory is used to provide a small high-speed multiplexed input/output buffer that also serves as an internal scratch pad memory.

Improvements in the cost of magnetic thin-film memories are being made rapidly, so that their cost can be expected to be competitive with linear-select or word-oriented core memories in the near future. The choice between linear-select magnetic core memories and magnetic thin-film memories will be made primarily on a basis of speed vs. cost. Because of the inherent magnetic and electronic techniques involved, there is little cost saving in slowing down a magnetic thin-film memory to operate at speeds slower than one microsecond cycle time. On the other hand, there are significant cost penalties in trying to operate magnetic core memories at one microsecond or less. As a result of these considerations, magnetic thin-film memories will be in widespread use during the time scale of the planned Navy Tactical Data System.

2.5.5.6 Cylindrical Magnetic Thin-Film Memories

Cylindrical magnetic thin-film memories are fabricated by depositing a magnetic film on a wire substrate.[9] The wire substrate then serves as one of the electrical conductors in the system. A closed flux path is obtained by the magnetic film surrounding the wire in a small region. A cylindrical thin film of this type offers the advantages that the closed flux path requires smaller digit currents and produces a larger sense signal. The fact that the wire substrate is used as either the digit or word conductor reduces the mechanical registration problems in the fabrication of the memory. The major problem with this type of memory has been the difficulty of producing satisfactory cylindrical films. Recent developments in these fabrication techniques have made this type of memory appear more promising.

In a recent paper, "Plated Wire Magnetic Thin Film Memories,"[10] presented at the 1964 Intermag Conference, Danylchuk and Perneski presented the following comparison of plated wire and planar film memories.

"1. Production method and control

Comparison: Plated wire is produced and tested in a continuous, serial process. Flat films are batch produced.

Conclusion: For plated wire, small numbers of bits may be rejected if bad. For flat films entire arrays may have to be rejected due to failure of a single bit.

"Comparison: The plated wires can be expected to be subjected to strain during fabrication of a memory plane. Flat films, which are plated on rigid substrates, are relatively free of strains due to handling.

Conclusion: During production a careful control of the magnetostriction of the plated wire must be maintained in order to prevent adverse strain effects.

"2. Output signal level

Comparison: The plated wire circumferential mode can use film thicknesses of 1μ (10,000Å) and more due to the closed flux path at remanence. Flat film thicknesses, which are limited by demagnetizing fields, are normally on the order of 1000Å.

Conclusion: Output signals are considerably higher for circumferential mode plated wire memories, while bit packing densities are comparable to those achieved with flat films. The axial mode plated wire has no advantage over flat films in this category since its film thickness is also limited by demagnetizing fields.

"3. Current levels

Comparison: Optimum coupling exists between fields produced by currents in the plated wire and the magnetic film deposited on the wire. For flat films, both digit and word solenoids must be added to the film array, and the opening of these solenoids are normally from 0.003" to 0.005". Also, slotted drive lines are normally necessary to permit penetration of the field generated by the uppermost conductor to the magnetic film in the planar construction.

Conclusion: For memory organization using plated wire as the digit line (circumferential mode), small (15 ma) digit currents are required. Alternatively, an axial mode memory which uses the plated wire as a word line, requires relatively small (200 ma) word currents. On the other hand, since the plated wire diameter (0.005") sets a lower limit on the area of the solenoid enclosing the wire, word currents are 0.7 to 1 amp for the circumferential mode and digit currents are approximately 0.2 amp for the axial mode. For flat films digit currents are approximately 0.2 amp while word currents are approximately 0.3 amp. It must also be pointed out that using the plated wire as a digit or word line leads to a much higher characteristic impedance than for a corresponding flat film memory line."

In another type of cylindrical thin-film memory developed by NCR, the direction of magnetization of the cylindrical elements is parallel to the center conductor rather than circumferential to it."

In the NCR rod memory, a cylindrical thin film of magnetic material is deposited over a conductive substrate, but the axial switching mode produces an open flux path element. A multiple turn winding is placed over the plated rod for each bit position. The plating material is essentially isotropic and proper operation of the memory does not depend upon anisotropy in the material.

NCR believes that their magnetic rod memory is more advantageous than either magnetic core matrix memories or planar thin-film memories in the range of 0.5 to 1.5 microseconds. They hope to lower this range to approximately 0.3 microseconds. Magnetic core matrix memories are more advantageous at slower speeds in the range of 2 to 6 microseconds; magnetic thin-film memories are more advantageous at very fast speeds of about 0.1 to 0.25 microseconds. NCR estimates that in the range of 0.3 to 1.5 microseconds, the magnetic rod memory will have approximately the same price per bit as a two microsecond coincident current magnetic core matrix memory; approximately 25¢ per bit including electronics. The electronics are compatible with and similar to those of magnetic core memories with a sense output of 80 millivolts being provided. NCR cites two major factors as making the rod memory economically feasible.

1) Rod manufacture is a continuous process including the automatic wiring of a pair of spiral wires around the rod.

2) Tooling has been developed to permit automatic fabrication of the memory stack (including multiple turn windings into which the rods are inserted).

The lack of a closed flux path is recognized as a disadvantage, but the use of a high coercivity magnetic material, permitted by the tight coupling of the multiple turn winding, overcomes this disadvantage. As a result of the high coercivity of the material, the tight coupling, and multiple turn windings, fast switching and large output signals can be obtained.

2.5.5.7 Woven Screen Memory

The woven aperture screen memory, under development by Bunker-Ramo Corporation, represents a completely different approach to batch-fabrication of memory planes.[12] In this memory, the individual memory planes are fabricated by a weaving process on looms similar to those used for the commercial weaving of textiles. The woven cell is formed by weaving the proper combination and geometry of insulated wires and bare metallic wires to form an orthogonal matrix of drive and sense wires, threading magnetic cells. The magnetic cells are formed by plating the bare metallic wires.

An electrical deposition process is used to plate a remanent magnetic material on the square aperture cells formed by the bare metallic wires. The plating process forms a closed flux path resulting from the plating of a pair of bare metallic wires in the X direction and an intersecting pair in the Y direction. The square magnetic cell formed by these four wires had been threaded previously in the weaving process by the insulated wires representing the sense line, the inhibit line, and the X and Y drive lines.

Since the plating process affects only the uninsulated wires, it is possible to weave the entire plane prior to the plating process. When the memory cell arrays are formed by the plating process, all of the sense and drive wires are already threaded through the entire plane. The details of the fabrication and characteristics of this type of memory were described in greater detail by Davis and Wells in a paper, "Investigation of the Woven Screen Memory System," presented at the 1963 FJCC.

A 10^8 bit memory assembled from 128 x 256 bit matrix planes would provide a 10 microsecond cycle time for 36 bit words. A memory of this capacity would be broken into 22 modules of storage planes. There is some uncertainty as to whether a sense preamplifier would be required for each plane. This is a question of major significance since 6336 such preamplifiers would be needed.

If the need for these preamplifiers can be avoided, the cost of a large capacity memory of this type will be significantly reduced. This is related to the problem discussed in connection with the laminated ferrite memory--a true low-cost large-capacity memory requires batch fabrication and significant cost reductions in the memory electronics as well as in the storage planes themselves.

Bunker-Ramo expects the cost of coincident current woven planes in assembled stack modules to be about 0.1 - 1¢ per bit in production quantities. However, this does not include the cost of the electronics which could be considerable.

Bunker-Ramo Corporation is also working on a woven screen memory for internal applications--a two microsecond 8,000 word, 30 bit memory. This memory is expected to be more rugged, to have higher temperature tolerances and to offer a lower cost than equivalent magnetic core matrix memories. The anticipated operating temperature range, about 105° C should be of particular interest for military applications.

Bunker-Ramo also expects the development of integrated circuit sense amplifiers and drivers for memories to have a significant effect on the cost of large batch fabricated memory systems.

Pacific Semiconductor Inc. has developed an integrated circuit sense amplifier under Air Force contract AF33(657)-11185. This sense amplifier is capable of sensing a 400 microvolt input signal to provide a 1 volt output with a maximum delay of 30 nanoseconds and a cycle rate of 20 megacycles. The write driver amplifier represents a more difficult problem. This problem has not yet been adequately solved.

A different approach to a woven screen memory is represented by recent work in Japan. This has been reported by Maeda and Matsushita in a paper, "Woven Thin-Film Wire Memories,"[13] and by Oshima, Futami, and Kamibayashi, in a paper "The Plated Wire Memory Matrix,"[14] both presented at the 1964 Intermag Conference. In this type of memory, plates wires are used as the storage elements similar to those discussed previously under cylindrical thin-film memories. The plated wire acts as the storage media, and also as the digit drive line. In the woven array, insulated wires woven at right angles to the

plated wires act as the word drive lines. This type of woven memory differs from the Bunker-Ramo approach in that the closed flux path magnetic element is the plating around a single wire rather than that formed by the rectangular intersection of four plated wires.

2.5.5.8 Laminated Ferrite Memory

One of the more promising approaches to batch fabricated memories is the laminated ferrite memory developed at RCA Laboratories. In different versions, this type of memory is proposed for both small-capacity, high-speed, control memory applications, and for large-capacity, medium-speed, main internal memory applications. Basically, the memory consists of a matrix of X and Y wires imbedded in a solid sheet of ferrite.

In fabricating the memory plane, a pattern of parallel conductors is printed on a glass substrate by a "silk screening type process." A film of ferrite is spread over the conductor pattern on the substrate by a process called "doctor-blading." After the ferrite binder dries, the ferrite is peeled off the substrate with the conductors imbedded in the ferrite sheet. This sheet is approximately 0.0025 inches thick. A second ferrite sheet is made with the conductor pattern running at right angles to that in the first sheet. A third ferrite sheet, without imbedded conductors and only 0.0005 inches thick, is inserted between the two ferrite plates with the orthogonal conductors. This three-sheet sandwich is laminated by pressing the sheets together at moderate pressures and temperatures. Sintering the laminated sheets in a controlled temperature furnace provides a truly uniform isotropic material.

The matrix of conductors provides the necessary wires for a two wire memory system in which the wires in the word oriented direction are used for reading and writing and the wires in the perpendicular direction are used for sensing and for digit determination. The write current generates a closed flux path in a plane perpendicular to the plane of the read/write drive wire. The current through the digit wire rotates the magnetic vector slightly. The methods of reading and writing in this type of array are described in detail in a 1963 FJCC paper by Shahbender, Wentworth, Hotchkiss, and Rajchman.[15]

RCA proposes this type of memory for two different applications. The first is as a high-speed control memory with approximately a 100 nanoseconds read/write cycle. In this type of application, a 256 word memory with 64 bits per word would require approximately 350 milliamps of drive current and would give a sense signal of $\pm$ 10 millivolts. The second application is as a large-capacity medium speed internal memory with a read/write cycle time of 1 - 3 microseconds. In this type of application, a drive current of approximately 50 milliamps would be required to produce a sense signal of 1.2 millivolts.

It is necessary to operate this type of memory in a word organized manner, but RCA does not consider this a limitation. To support this, they state that although coincident current memories require less electronics, the electronics are more expensive because of problems with noise in the sense line, tolerances, and back voltage on the drive wires. On the other hand, word organized memories require more electronics but they are less expensive since less critical tolerances are placed on the material; there is less noise on the sense line, and less critical tolerances are placed on the drive wire signal. Therefore, the amount of electronics is greater for the word organized memory but the total cost of the electronics may not be significantly greater because of the lesser requirements placed on them.

RCA recognizes that significant success in reducing the cost of a memory depends upon the use of relatively cheap integrated circuits to permit the electronics associated with the memory to be made by a batch-fabrication process. In a typical memory, the wired and tested array represents only approximately 1/2 of the total cost of the memory, with the other half going for the electronics. As a result, techniques such as the laminated ferrite memory alone would reduce the total memory cost by only 50% even if they were assumed to lower the array cost to essentially zero. Hence, concentrated efforts on reducing the cost of integrated circuit electronics for such memories are required if significant improvements in memory costs are to be achieved.

Costs for the laminated ferrite memory are estimated to be less than 1¢ per bit for memories with capacities of 10^7 to 10^8 bits, speeds of 1-3 microseconds, and word sizes of 200-400 bits per word. RCA expects to be making laminated ferrite memories on a commercial basis with 10^6 bits capacity in two years, 10^7 bits capacity in four years, and 10^8 bits capacity in five years.

2.5.5.9 Flute Memory

Another approach to a batch fabricated memory array is the flute memory developed by IBM. Conceptually, this memory is very similar to the RCA laminated ferrite memory but the fabrication techniques are different. The fabrication techniques and characteristics of this memory were described in a paper by several authors in the April 1964 issue of the IBM Journal of Research and Development.[16]

The planes in the flute memory are fabricated by sandwiching a pre-prepared grid of wires between two dies, each of which has matching grooves filled with a mixture of ferrite thermosetting resin binder. The grooves containing ferrite are parallel to the word lines of the wire grid so that when the two halves of the mold are placed together, the word line is completely imbedded in the ferrite tube formed by the ferrite in the corresponding grooves of the upper and lower halves of the mold. The bit lines of the wire grid are orthogonal to the word lines and intersect each of the parallel ferrite strips encasing the word lines.

A typical memory plane consists of 50 ferrite tubes intersected by 100 bit lines to give a capacity of 5000 bits per plane. The ferrite area surrounding the intersection of a bit line and a word line defines an individual bit position. Yields of 36% have been realized in the batch-fabrication process. Cycle times of 250 nanoseconds are considered possible by IBM.

2.5.5.10 Permalloy Sheet Memory

The permalloy sheet memory under development at Laboratory For Electronics is another approach to batch fabrication of a low-cost large-capacity memory. In this technique, a permalloy sheet is bonded to a substrate. A pattern is printed on photo resist covering the sheet, and the permalloy is etched away to leave a matrix of toroidal permalloy storage elements. Three small holes in the center of each toroid are plated through to provide connections from one side of the array to the other through the toroids. Printed interconnections on both sides of the board wire the array. This design effectively combines a number of known techniques into a very interesting fabrication technique for a large memory array. A paper on this memory presented by Fuller at the 1964 Intermag Conference gives a much more detailed description of the memory and fabrication techniques than the simplified one above.[17]

This development program is "aimed at improving processing speeds by providing data processing systems with random-access memories approaching the speed of ferrite-core matrix memories, but at a cost that economically permits mass memory capacities."

The goal in this development is a large capacity memory in which coincident current selection is used to reduce the electronic costs, and in which a very large memory plane (256 x 256 bits) is used to reduce fabrication costs as well as drive, selection, and sense electronics costs. A 6.5 million bit memory module is planned in which the smallest unit that is individually handled in processing is a matrix plane of 65,000 bits. The cost objectives for this development are 0.03 - 0.3¢ per bit.

2.5.5.11 Ferroacoustic Memory

The term ferroacoustic memory is used to refer to two similar memory developments being sponsored by the U.S. Army Engineering Research and Development Laboratory at Fort Monmouth, New Jersey. These contracts are with RCA Laboratories in Princeton, N.J. and General Dynamics/Electronics in Rochester, New York.

The RCA work has been described in two quarterly reports submitted to the Army[18,19]. The General Dynamics/Electronics approach has been described in Gratian and Freytag[20] in a paper, "Ultra Sonic Approach to Data Storage," published in the May 4, 1964 issue of Electronics.

Although this is a batch-fabricated memory approach, it differs from those described previously in that it is not a random access memory. This type of memory is block oriented with random access to the beginning of a block but serial access to information within the block. A batch-fabricated solid state memory of this type would be a replacement for large magnetic drums, magnetic disc files, and possibly magnetic tape.

Previous types of delay line memories suffered from the volatility and the large amount of electronics necessitated by the requirement for regenerating and recirculating the information in each individual delay line. The necessity for recirculating the information results in the loss of stored information if power is interrupted. The requirement for electronic circuitry to be in continuous use for each individual line implies a severe cost penalty in very large capacity memories. The ferroacoustic approach permits static storage of information without continuous recirculation which, in turn, permits the electronic read and writing circuitry to be switched from one line to another as part of the addressing and selection process.

In this type of memory, data is stored on a thin magnetic film plated on an acoustic tube through which a center conductor is inserted. The actual storage is in a closed flux path around the acoustic tube similar to the storage in cylindrical thin film memories discussed previously. However, the access is not made by coincidence of two electrical signals, as in the memories discussed previously, but rather by the coincidence of an electrical signal and an acoustic signal.

The concept of this type of memory is based on the change of coercivity of magnetic materials, such as permalloy plating, when the material is placed under mechanical stress. An alternate approach is based on the fact that the anisotropic characteristics of thin permalloy films are changed by stress.

In a memory based on these principles, a mechanical shock wave is initiated in the acoustic tube by a suitable transducer (e.g. magnetostrictive or piezo electric). The mechanical shock wave travels down the tube at a speed determined by the propagation constant of the material. The coercivity of the magnetic material plated on the tube changes as the shock wave passes under it and returns to its normal condition after the shock wave has passed. As a result, a temporary change in the coercivity of the magnetic media is propagated down the line.

An electrical signal, corresponding to the serial bit pattern of 1's and 0's to be stored, is placed on the center conductor. This signal causes the magnetic cylinder to be linked by a varying flux pattern depending upon the bit pattern represented by the electrical signal. The flux pattern generated by the electrical signal corresponding to a "1" is sufficient to change the state of magnetization of the magnetic material in an area where the coercivity has been altered by the mechanical stress wave. The magnetic flux corresponding to a "0" signal will not alter the state of magnetization, even in those areas where the coercivity has been changed. As a result, a bit position is determined by the time coincidence of the electrical signal and the acoustic signal. As the acoustic signal travels down the line, a "1" or "0" corresponding to the electrical signal will be written in the position defined by the front of the shock wave.

The time required to read a complete block corresponds to the time the shock wave requires to travel from one end of the line to the other. The rate at which the stored information is read or written corresponds to the frequency of the electrical signal representing the bit pattern. This frequency is limited by the physical size of the area of magnetic material whose coercivity is altered by the shock wave at a given instant. This in turn determines the bit density and hence the capacity of a line of a given length.

It is important to note that the information is stored statically in the magnetic plane and is not carried by the acoustic wave. This is in contrast to a normal acoustic delay line in which the information is actually carried by the acoustic wave. In the ferroacoustic type memory described here, the acoustic signal acts only as an access mechanism. A single acoustic signal is required to read a complete line or write a complete line. Read-back is achieved by transmitting an acoustic signal down the line and sensing the changes in the electrical signal generated on the center conductor by the magnetostrictive effect of the shock wave traveling down the line. This signal varies, depending upon the stored pattern on the line.

If this ferroacoustic approach proves feasible, it offers the following advantages:

1) Static storage
2) Semi-serial access not requiring a physical coincidence of selection wires for each bit position.
3) Ability to switch read and write mechanisms from one line to another.
4) Large capacity semi-random access bulk storage with no mechanically moving parts.
5) Possibility of off-line storage by plugging alternate blocks of delay lines into a read/write device.
6) Low cost per bit of storage.

The goals of the Army development program are to provide a block oriented random access memory with the following characteristics:

4,000,000 characters per module
4096 blocks per module
1024 blocks per module
approximately 0.002¢ per bit
(off-line storage cost not including read/write electronics)
1 microsecond access to a block.
several megacycle read/write rate.

If this development proves feasible, it will be of great significance to future computer systems. At present, there is no economic all electronic/mechanical replacement for large capacity electro-mechanical storage devices such as magnetic disc files, magnetic card memories, and magnetic tape units.

Such a replacement will be essential to future systems if the speed, cost, reliability and size limitations of electro-mechanical input/output and auxiliary storage equipments are to be avoided for very large capacity storage functions (now handled by devices such as disc files and magnetic tapes).

A future all electronic magnetic replacement will almost certainly be a block-oriented rather than a random-access-type storage device. Although a large capacity, random access, mass memory offers certain unique advantages, it is very unlikely that such a device can compete on a cost per bit basis with semi-serial electromechanical devices. The requirement for intersection of electrical signal lines for each bit position, and the excess electronics will not provide on-line storage costs of a few millicents per bit by 1970. A semi-serial or block-oriented device providing random access to a block of information, but serial access within the block will be necessary to permit the read/write electronics to be time shared by a serial bit train.

2.5.5.12 On-Line Auxiliary Storage

On-line auxiliary storages are frequently referred to as mass memories. On-line devices of this type are used to provide a large-capacity, fast, semi-random-access storage. They should be under direct on-line control of the computer, addressable by the computer, eraseable, and reuseable. All devices of this type that are currently available are electromechanical. All electronic/magnetic on-line auxiliary storages for military applications will be available by 1970 but all of these (with the possible exception of the ferroacoustic storage discussed previously), will be significantly more expensive in terms of cost-per-bit for very large capacity storage. This results largely from the fact that the all-electronic/magnetic approaches (e.g. laminated ferrite memory, woven screen memory, flute memory, etc.) require addressing each individual word. The electromechanical devices are block oriented in the sense that access is made to a particular track on a disc, drum or card, and then all information stored in that track (or block) is read or written serially by the same electronic circuitry.

Of the all-electronic/magnetic approaches to large capacity memory that have been discussed in previous parts of this report, only the ferroacoustic approach is block oriented and hence offers some promise of competing with the electromechanical devices by 1970 on a purely economic basis.

As a result of previous studies by one member of the study team, more detailed information is available at this time on electromechanical mass memories[21,22]. The information presented here is indicative of the type of critical detailed evaluation and comparisons that will be made for the other memory areas during the remainder of the study. The characteristics of the major types of electromechanical mass memories are summarized in the table shown in Table 2-4. The values shown were chosen as typical of each type of unit but frequently they represent a wide range of possible values. In some cases, certain characteristics of an individual device may vary significantly from the values shown. The characteristics of primary interest include capacity, cost, average access time, and data transfer rate. Some of these are difficult to compare because of the different physical characteristics of the devices. For example, a large magnetic drum with a head for every track will have a continuous data transfer rate equal to the instantaneous transfer rate if the heads are switched electronically. However, the continuous data transfer rate for a disc file with moving heads will be significantly greater than the instantaneous transfer rate due to the necessity for interrupting data transfer while moving the head from one position to the next. Similar differences on a more detailed level exist between different devices of the same type.

In comparing costs, a detailed investigation is usually required to determine whether prices quoted for different units include comparable electronics (i.e., controllers, buffers, switching, amplifiers, etc.). The estimated costs shown in the table are user's costs (rather than manufacturing costs) and assume a moderate amount of associated electronics.

TYPE OF DEVICE	ON-LINE CAPACITY PER-UNIT IN CHAR.	TYPICAL ON-LINE COSTS IN ¢/CHAR.	AVERAGE ACCESS TIME	DATA TRANSFER RATE IN CH/SEC.	REMARKS
Large Fixed-Head Mag. Drums	0.2×10^6 to 5.0×10^6	2.0	15 ms	100,000 to 200,000	
Moving-Head Magnetic Drums	4.0×10^6 to 65×10^6	0.3	100 ms	50,000 to 150,000	
Fixed-Head Magnetic Disc Files	10×10^6 to 40×10^6	0.5	20 ms	100,000 to 350,000	Offers Promise for Militarization
1 Dimension Moving-Head Mag. Disc.	10×10^6 to 250×10^6	0.2	100 ms	100,000 to 400,000	Contract has been awarded for militarizing one device of this type.
2 Dimension Moving-Head Mag. Disc	10×10^6 to 150×10^6	0.15	500 ms	50,000 to 100,000	Relatively obsolete
Removable-Stack Disc Files	2.0×10^6 to 7.0×10^6	0.6 (on-line) 0.01 (off-line)	150 ms	160,000	Off-line storage capacility
Magnetic Card Files	5.5×10^6 to 340×10^6	0.03 (on-line) 0.0001 (off-line)	250	100,000	Off-line storage capability Contract has been awarded for militarizing one device of this type

TABLE 2-4 SUMMARY OF CHARACTERISTICS OF ELECTROMECHANICAL MASS MEMORIES

Access time offers another illustration of the difficulties of comparing different types of mass memories. It is difficult to compare the access times even for different devices of the same type--for example, different designs and makes of disc files. It is considerably more difficult to compare the access times for completely different types of mass memories due to differences in the methods of making mechanical access since the total mechanical access is usually made up of a number of separate components.

As a result of problems of this type, comparison tables such as the one shown in Table 2-4 present at best a gross comparison. In selecting a device for any specific application, it is necessary to go into a more detailed comparison of the specific pecularities and quirks of each of the leading contenders as they relate to that application if a proper decision is to be made.

1) Large Magnetic Drums

Until recently, the capacity of large magnetic drums ranged from approximately 200,000 to 1,000,000 characters per unit for those with fixed heads, and approximately 4 to 10 million characters for those with moving heads. However, one manufacturer recently announced a large dual drum unit with moving heads providing a capacity of 65 million alphanumeric characters. In this unit, two very long drums (over six feet) are rotated on parallel centers with the surfaces close enough to one another to permit a single access mechanism to position sets of 64 heads--32 on each drum.

The choice between these two types of drums depends largely upon whether access time or capacity is the more important consideration. The fixed-head drum also implies a higher cost per bit of storage due to the number of heads and the switching circuitry required.

2) Magnetic Disc Files

A magnetic disc file consists of a stack of disks (usually 5 to 100) rotating on a common shaft. The discs are usually between 1 1/2 and 3 feet in diameter. Magnetic disc files can be classified as those with fixed heads (one head per track on each disc), those with moving heads, and those with removable disc stacks (and moving heads). Disc files with moving heads can further be divided into those in which the heads move in one dimension only (in and out among the stack of discs) and those in which the heads move in two dimensions (up and down the stack of discs as well as in and out among the stack). The major effects that these differences have on the characteristics of the devices are indicated in the Table too.

In general, the larger the number of bits that can be accessed by a single head and selection mechanism, the lower the cost per bit and the longer the access time.

a). Fixed-Head Magnetic Disc Files

Disc file storage units with fixed heads usually involve a limited number of discs, a maximum number of bits per track, and a fixed head for each track. This type of storage permits a higher track density since the fixed heads eliminate the need for mechanical positioning of the head and the resulting allowances for mechanical tolerances. The large multiplicity of heads, and the required electronic switching between heads, results in a significantly higher cost per bit than for the moving-head type disc storage.

Although this type of disc storage is somewhat similar in functions and characteristics to fixed-head magnetic drums, the use of three dimensions instead of two permits greater volumetric efficiency--greater storage capacity in a more compact unit. There are, of course, also differences in the mechanical design problems between disc and drum units, but these are outside the scope of this paper.

b). Moving-Head Magnetic Disc Files

The first commercially available magnetic disc files involved a two-dimensional head movement. A single head mechanism was moved up and down parallel to the disc stack and shaft to select one of a number of discs, and then moved in between adjacent discs to select the desired track. In this unit, the head-mount arm straddled a disc to provide a head to read the upper surface of the disc and another head to read the lower surface.

Although some modern large capacity disc files also operate on this principle, most of the present units involve a one-dimensional movement. A head mount is inserted between each pair of adjacent discs, usually with one head reading the lower surface of the upper disc and another head on the same mount reading the upper surface of the lower disc. This type of disc file provides a much faster access by eliminating the necessity for moving the heads in the dimension parallel to the disc shaft. The penalty paid for this faster access is the increase in the cost per bit of storage due to the cost of the larger number of heads and the electronic switching between heads compared with the cost of a disc selector mechanism.

The one-dimensional movement permits two secondary advantages that are not apparent from the comparisons in the Table. Since there is at least one head for each disk, it is possible to provide a larger number of read and write amplifiers to permit reading or writing multiple tracks simultaneously with a significant increase in the effective instantaneous data transfer rate.

Even without simultaneous reading or writing from all heads, the ability to switch electronically between heads increases the information that can be transferred without moving the arm. Appropriate organization of the problem can reduce the number of arm movements required, thereby increasing the effective speed of operation.

The insertion of the set of head mounts between pairs of adjacent discs can be, and has been, accomplished in several different ways mechanically. In one design, the head mounts for all discs are moved together by a common track selection mechanism. As a result, all of the heads are moved in and out simultaneously to corresponding tracks on each disc. This can be pictured as a comb of head mounts moving in and out perpendicular to the disc shaft. For any one position, the tracks being read or written on each of the discs describes a cylinder conceptually similar to a magnetic drum with wide track spacing. Another design provides independent head positioning mechanisms for each disc. If utilized, the ability to independently access tracks on different discs can permit a significant decrease in effective access time since several accesses to different discs can be overlapped or performed simultaneously.

c). Removable-Stack Disc File

The newest addition to the disc storage family is the removable-disc-stack unit. In this device, a drive mechanism handles a small stack of discs that can be removed, replaced, and interchanged with other stacks.

This device provides a compromise between the off-line storage capability of magnetic tape, and the on-line fast access capability of larger mass memories. A series of disc stacks can be stored away on a shelf and put on the drive mechanism as required. Each disc stack has approximately one fourth the capacity of a tape reel with ten times higher cost. However, all data within a stack can be on-line and addressable by the computer to provide fast access within blocks of two million characters at a time. This is particularly well suited to the requirements of many types of business problems for large total file storage capability but on-line fast access to only a segment of this in any given processing operation.

3) Magnetic Cards

The magnetic-card type of mass memory, which preceded the removable-stack disc storage by over two years, is quite different physically and mechanically. However, from a systems and applications standpoint, the two are somewhat similar in that the magnetic card memory also provides a certain amount of on-line storage capacity and an almost limitless amount of off-line storage capacity. The magnetic-card type offers an advantage over disc files in that individual cards can be copied, inserted, removed, or replaced.

In one device of this type, oxide-coated Mylar cards, approximately 3 x 14 inches in size, are hung from rods in the magazine. These rods may be selectively turned to select the card with binary-coded notches corresponding to the rods that have been turned, thus providing the ability to select any card from the magazine at random. The selected card is then dropped to the surface of a rotating drum and accelerated to the surface speed of the drum so that it can be read or written while passing under a set of heads. The card may be held on the drum for rereading or for reading another set of tracks on the same card. When it is released from the drum, it is automatically returned to the magazine. Its location in the magazine is immaterial since the selection is by the coded notches in the card and the combination of rods that are turned rather than by physical location.

The major advantages and disadvantages of the different types of mass memories are summarized in Table 2-5.

TABLE 2-5

ADVANTAGES AND DISADVANTAGES OF DIFFERENT MASS MEMORIES

TYPE OF MASS MEMORY	ADVANTAGES	DISADVANTAGES
Fixed-Head Magnetic Drums	Fast access, no mechanical head motion, high continuous data transfer rate.	Low capacity, high cost per bit, poorer volumetric efficiency, large number of heads.
Moving-Head Magnetic Drums	Large capacity, low cost per bit, possibility of parallel reading or writing from multiple heads to greatly increase instantaneous data transfer rate.	Poorer volumetric efficiency, relatively large number of heads for medium speed access or slower access if fewer heads.
Fixed-Head Magnetic Discs	Fast access, medium capacity, no mechanical head motion, high continuous data transfer rate.	High cost per bit of storage, large electronic switching matrix, large number of heads.
Two-Dimension Moving-Head Magnetic Discs	Large capacity, minimum number of heads, low cost per bit	More complex positioning mechanism, slowest access, slow continuous data transfer rate.
One-Dimension Moving-Head Magnetic Discs	Large capacity, possibility of multiple simultaneous accesses if heads are positioned independently, low cost per bit compared to fixed head units, possibility of parallel reading or writing from multiple heads to greatly increase instantaneous data transfer rate.	Relatively large number of heads, somewhat higher cost per bit compared to two-dimension disc unit, medium speed access.
Removable-Stack Discs	Large off-line capacity, low cost per bit of off-line storage, combines on-line random-access capability with large off-line capacity.	Limited on-line capacity, higher cost per bit of on-line storage.
Magnetic Card Memory	Large off-line capacity, low cost per bit of off-line storage, combines on-line random-access capability with large off-line capacity, individual cards can be copied, replaced or inserted.	Slower access, card wear and replacement necessitates eventual rewriting of entire card.

Future improvements can be anticipated. In 1962, A. S. Hoagland pointed out that the storage density of one manufacturer's commercial disc files increased from 2000 bits per square inch in 1956 to 25,000 bits per square inch in 1961. He then predicted that storage densities of "one million bits per square inch (e.g. approximately 5000 bpi, 200 tpi) will become the state-of-the-art" within the next few years. A few months earlier, M. Jacoby predicted densities of 3000 bpi and 500 tpi (1.5 million bits per square inch) would "become common-place in a few years". He then indicated that these densities could provide storage capacities of 10 to 100 billion bits if a possible increase in the physical size is also considered. Thus, increases in capacity of tens to hundreds of times over the largest present mass memories can be anticipated.

The cost per unit can be expected to decrease even with the larger capacities as the technology is improved and more manufacturing experience is obtained. Hence, the cost per bit of storage can also be expected to decrease by one to two orders of magnitude--possibly to 0.0001 cents per bit for the mass memory itself (not including control and buffering electronics). Although the picture for the future of capacity and cost appear bright, there is little hope for significant improvements in average access times for moving-media mass memories. Due to the inherent mechanical motions involved, we cannot expect improvements of as much as an order of magnitude over available devices. For significant improvements in access time, we must turn to the non-moving-media type devices.

It is likely that continued improvements and innovations in moving-media mass memories will provide ultimate capacities, access times, data transfer rates, and costs superior to those indicated above. Just as the development of the floating head permitted densities and rates in excess of those previously anticipated for fixed heads, unforeseen developments may well serve to push the limits of these devices beyond expectations. An example of work on one such development has been described in Hoagland. This is a disc unit in which the head in positioned on a track under control of a servo system with the signal read from the track being part of the control loop to permit far greater track density and multiple access arms.

2.5.6 Memory Availability in the 1970-80 Period

A preliminary estimate of characteristics expected to be available, feasible, and competitive for use in a 1970 system are shown in Tables 2-6, 2.7, and 2.8 for registers and high-speed control memories, main high-speed internal memories, and on-line auxiliary storage. Only all-electronic/magnetic technologies are shown. There is not sufficient basis at this time of anticipate an all electronic/magnetic off-line auxiliary storage. The ferroacoustic storage discussed previously appears to be the most likely candidate, but it is too early in the development of this device to determine whether it will be feasible by 1970.

The comparisons in the three tables do not include memories that are expected to be obsolete by 1970 and memory techniques that appear promising on a longer time scale but are not expected to be operational by 1970. The characteristics shown for different types of memories are those expected to be realizable for a memory to be operational in 1970. These preliminary comparisons will be refined during the remainder of the study and additional memory technologies will be added to the comparisons.

TYPE OF STORAGE	TYPICAL CAPACITY (WORDS)	TYPE ACCESS	R/W CYCLE TIME	R/W RATE	VOLATILE	POSSIBLE DATE OF 1st PROD.	BATCH FABRICATION TECHNIQUE
Integrated Ckt. FF Registers	25	Random	125 ms	40 mc	Yes	1966	Diffusion and Vacuum Deposition
Planor Thin-Film	512	Random	100 ms	10 mc	No	1965	Multi-Layer Vacuum Deposition
Cylindrical Thin-Film (Magnetic-Rod)	512	Random	250 ms	4 mc	No	1965	Plating and Automatic Cost Winders
Laminated Ferrite	512	Randon	100 ms	10 mc	No.	1966	Silk Screening "Doctor-Blading", Lamination
Linear Select Magnetic Core Matrix	512	Random	350 ms	3 mc	No	1966	?
Tunnel Diode	512	Random	10 ms	100 mc	Yes	1965	None
Flute	512	Random	250 ms	4 mc	No	1966	Ferrite Molding

TABLE 2-6

Preliminary Estimate of Characteristics of Registers and High-Speed Control Memories in 1970

TYPE OF STORAGE	TYPICAL CAPACITY (WORDS)	TYPE ACCESS	R/W CYCLE TIME	R/W Rate (WORDS)	VOLATILE	POSSIBLE DATE OF 1st PROD.	BATCH FABRICATION TECHNIQUE
Continuous-Sheet Cryogenic	2×10^6	Random	1.0 ms	1 mc	?	1969	Multi-layer Vacuum Deposition
Laminated Ferrite	0.2×10^6	Random	2.0 ms	0.5 mc	No	1968	Silk-Screening "Doctor-Blading", Laminating
Woven-Screen	0.2×10^6	Random	2.0 ms	0.5 mc	No	1966	Weaving, Plating
Magnetic Thin-Film	0.2×10^6	Random	0.5 ms	2 mc	No.	1967	Vacuum Deposition
Permalloy-Sheet	2.0×10^6	Random	10.0 ms	0.1 mc	No	1967	Silk-Screening, Etching, Plating
Flute	0.1×10^6	Random	2.0 ms	0.5 mc	No	1968	Ferrite Molding
Linear Select Magnetic Core Matrix	0.2×10^6	Random	1.0 ms	1 mc	No	1965	?
Glass Delay Line	0.02×10^6	Serial Random	20.0 ms	1 mc	Yes	1965	Glass Rod

TABLE 2-7

Preliminary Estimate of Characteristics of Main High-Speed Internal Memories in 1970.

TYPE OF STORAGE	TYPICAL CAPACITY (WORDS)	TYPE ACCESS	ACCESS TIME	R/W CYCLE TIME	R/W RATE	VOLATILE	POSSIBLE DATE OF 1st PROD.	BATCH FABRICATION TECHNIQUE
Continuous-Sheet Cryogenic	20×10^6	Random	-	5.0 ms	0.2 mc	?	1970	Multi-Layer Vacuum Deposition
Woven-Screen	5×10^6	Random	-	10.0 ms	0.1 mc	No	1968	Weaving, Plating
Permalloy-Sheet	5×10^6	Random	-	100.0 ms	0.01 mc	No	1968	Silk-Screening, Etching, Plating
Ferro-Acoustic	20×10^6	Serial/ Random	1 ms (to block)	-	3 mc	No	1969	Plating, Acoustic Cylinder

TABLE 2-8

Preliminary Estimate of Characteristics of On-line Auxiliary Storage in 1970.

During the time from 1970 to 1980, continual improvements will be made in the characteristics of most of these memory types. Other types of memories not feasible for a 1970 system will probably be developed to a point that they can be included in an operational system prior to 1980. These may include low-cost, large-capacity random access mass memories, integrated semiconductor memories, electron spin echo storage, large-capacity low-cost magnetic film domain wall storage, and perhaps high resolution electron-beam fabricated storage systems. There will undoubtedly be some radically new memory techniques developed during the 1970-80 period, but a large part of the improvement in memory characteristics and capabilities during that time period will result from continued improvements of memories now in use or under development. This is particularly true with respect to improved batch-fabrication techniques. Although there is a possibility that some exotic new memory techniques, such as a high-speed random access read/write memory based on the use of lasers, will be developed during that time period, it is certain that new methods of fabricating magnetic memories will be developed that will have significant and dramatic effects on the cost, speed and capacity.

2.5.7 Limitations of Present and Planned Memories

It is difficult to place ultimate limits on the cost, speed, and capacity of different memory types since the violation of basic physical laws has not been the limiting factor to date and probably will not be for the foreseeable future. The comparison tables given in Section 2.5.5 indicate the characteristics anticipated for a 1970 system but these are not ultimate limitations in most cases. It is important to note that in considering the limitations, the set of characteristics must be taken as a whole. For example, for a particular type of memory, a certain combination of speed and cost may be anticipated for a 1970 system. However, if the capacity were decreased significantly, the speed could be increased and if the speed were decreased, the capacity could be increased. Therefore, the characteristics shown in the tables in Section 2.5.5 should not be considered as limitations on any individual characteristic

but rather as a reasonable expectation for characteristics for 1970.

A number of memory experts have given consideration to ultimate limitations of memory technologies. One of these is Dr. J. A. Rajchman of RCA Laboratories who prepared the diagram shown in Figure 2-35. This diagram shows Dr. Rajchman's estimate of the limitations in terms of speed vs. capacity for different memory technologies. The difficulty of placing such limitations on a rapidly developing technology is indicated by the fact that the diagram shown in the figure is the latest of a number of similar diagrams prepared by Dr. Rajchman over the past two or three years each being updated to reflect changes in the technology since the previous one.

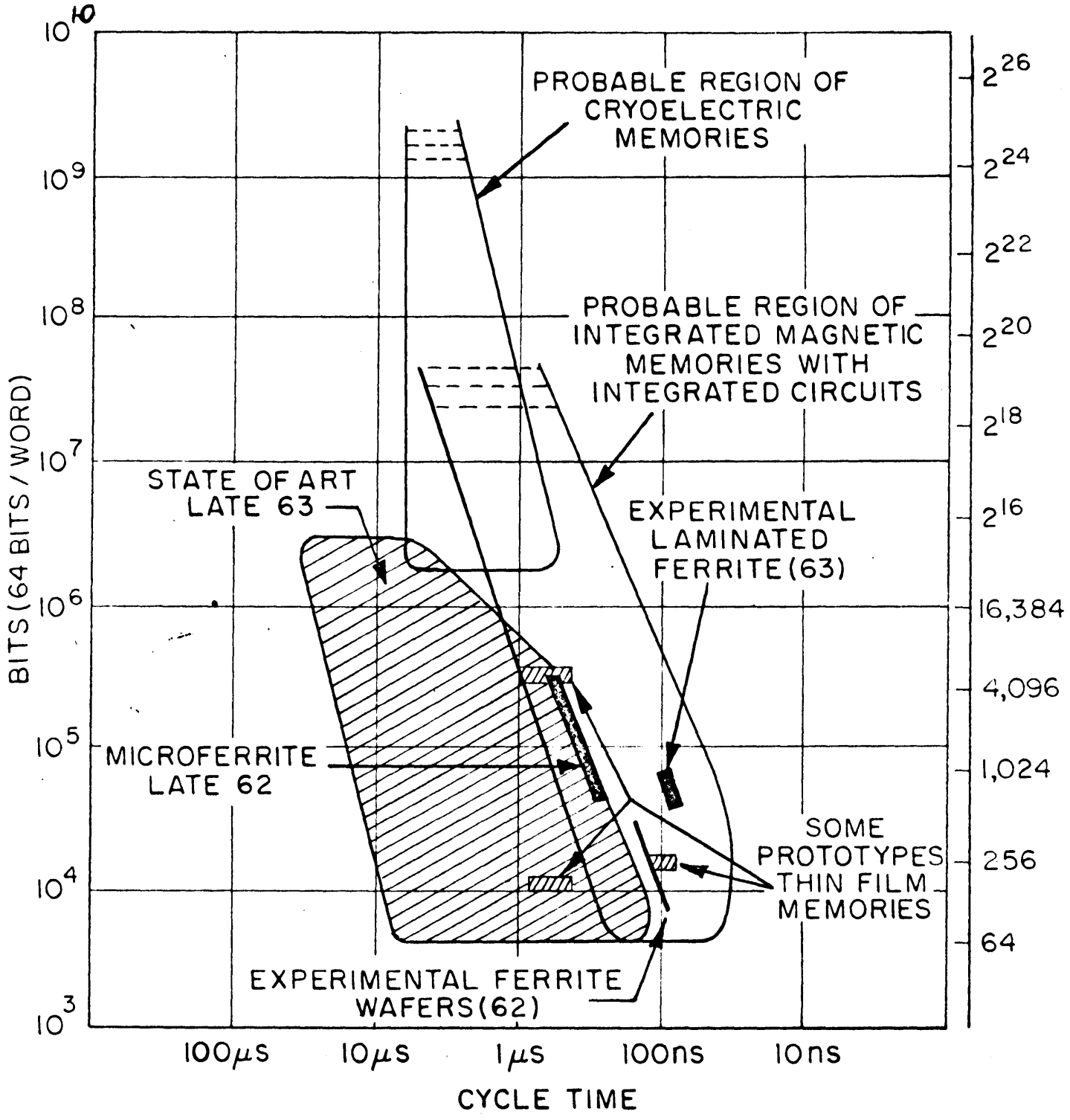

Figure 2-35 - Storage Capacity and Cycle Time of Memories
(After Rajchman)

2.5.8 Recommended Developments to Meet ANTACCS Needs

No development efforts are necessary to assure availability of memories meeting ANTACCS needs in 1970 from a performance stand-point. However, development efforts will be required to assure that certain types of these memories meet the operational requirements for temperature, shock and vibration, nuclear radiation effects, electro-magnetic interference requirements, humidity, and perhaps reliability and maintainability. It is anticipated that the solid state electronic and magnetic memories will meet ANTACCS requirements for reliability and maintainability but if electro-mechanical memories such as magnetic drums, magnetic disc files, and magnetic card memories have not been completely replaced by all electronic/magnetic memories by that time, additional development efforts will be required to further militarize these electromechanical devices. Some work in this direction is currently underway but additional work will be necessary to meet fully the requirements of a 1970 ANTACCS System. The requirements for an ANTACCS for that time period are probably more stringent and would necessitate development work directed toward reducing the size and weight of these devices as well as meeting the environmental conditions discussed above.

This is considered to be an interim effort since it is believed that electromechanical devices of this type will ultimately be replaced by all electronic or magnetic memories. However, at this time it does not appear safe to assume that this will be accomplished in all cases in time to satisfy the requirements of the 1970 ANTACCS system. Hence, it will be necessary to further improve the environmental characteristics, reliability, and maintainability of present types of electromechanical memories (particularly disc files and magnetic card memories) for these systems.

2.5.9 Evaluation Criteria Recommended

In evaluating different types of memories for use in a 1970 ANTACCS System, it will be necessary to consider a relatively large number of characteristics and parameters. However, many of these can be quickly considered for most types of memories and will not require an elaborate and detailed comparison. These characteristics will be noted for particular memories only where they significantly increase the desirability or appear to be a major deterrent to the use of a particular type of memory. The parameters and characteristics to be considered in comparing and evaluating different types of memories will include:

Type of storage media or phenomena involved
Access time
Type of access
Read/write cycle time
Read-only cycle time
Read/write rate
Device switching time
Storage capacity
Storage density
Static or dynamic
Eraseable
Non-destructive read out
Volatile or non-volatile
Addressing and selecting techniques
Size and weight
Operating temperature range
Susceptibility to shock and vibration
Susceptibility to nuclear radiation effects
Susceptibility to electromagnetic interference
Generation of electromagnetic interference
Susceptibility to humidity
Other environmental considerations
Approximate or relative cost per bit
Range of reasonable memory system costs
Reliability
Maintainability
Logistics Requirements
Batch-fabrication techniques
Fabrication and packaging problems
Stand-by power requirements
Operating power requirements
Approximate or estimated date of first production quantity applications
Special features (e.g. associative)
Functional uses in a computer or digital system
Special requirements (e.g. cooling or refrigeration)

Although all of the above characteristics should be considered, it will usually be necessary to make a detailed comparison and evaluation only on the basis of the following characteristics: type of storage media or phenomena, access time, type of access, read/write cycle time (for random access memories), read-only cycle time (for read-only memories), storage capacity, volatile or non-volatile, eraseable, relative cost per bit, adaptability to batch-fabrication techniques. The effect or implication of other characteristics will be noted where appropriate for particular memories as "remarks." For example, the operating temperature range will be noted only where it is extremely difficult for a particular type of memory to meet the temperature ranges required in the military environment.

2.5.10 Conclusions and Recommendations

Memories in all categories for use in a 1970 ANTACCS System should and can be manufactured by various batch-fabrication techniques. Such techniques for fabricating large memory arrays as units rather than by the assembly of large numbers of discrete elements, are well along at this time and are receiving considerable attention from the industry. The memory function is particularly adaptable to batch-fabrication techniques since it consists of large numbers of similar elements or circuits and hence is highly repetitive. This is true on one extreme for small high speed one word registers that might be fabricated as a single integrated circuit array, and on the other extreme for very large capacity on-line auxiliary memories such as a cryogenic memory, laminated ferrite memory, or woven screen memory. It is certain that techniques of this type will be feasible, economic, highly developed and in widespread use by 1970.

However, it is not certain that large capacity on-line auxiliary memories of this type will be competitive with electromechanical memories (e.g. magnetic disc files and magnetic card memories) on a cost-per-bit basis by that time. It may be necessary to use some electromechanical device for this mass memory function, or to recognize and accept a cost penalty for using an all electronic or magnetic approach. This is particularly true for mass memories with capacities of 10^9 bits and above. Although these

very large capacities can be achieved by using multiple banks of smaller memories, this will probably not be economically feasible. As a result, moving magnetic-media type electromechanical type memories will likely be used for these requirements.

Associative memories will be feasible and available but their use will depend upon developments in machine organization and upon significant cost reductions. Relatively small capacity associative memories will probably be used in conjunction with the main high-speed random-access internal memory for functions such as indexing and perhaps some list processing. However, it is not believed that large capacity associative memories serving as the main internal memory will be economically justifiable or feasible by 1970.

Conclusions concerning the relative advantages and disadvantages of specific types of memories will be developed during subsequent parts of this study and recommendations will be made as to specific types of memories to use in different subsystems and for different functions.

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2.6 COMPONENTS AND PACKAGING

Components and packaging techniques have been investigated and are discussed together as intimately interrelated topics. The method of packaging arrays of components cannot be considered independent of the nature of the component itself. On the other hand, the selection of specific types of components imposes unique requirements on the packaging techniques. The ultimate goal is the maximum degree of batch-fabrication possible to permit relatively large segments of a computer, or other digital equipment, to be fabricated as a unit in a single set of processing operations.

Until recently, it has been necessary to package individual discrete components (e.g., transistors, diodes, resistors, capacitors, etc.) into circuit arrays by techniques such as printed circuits or welded connections, and to further interconnect groups of these modules into subassemblies. Frequently cables and cable connectors are used to interconnect such subassemblies into units of equipment. With new types of components, such as integrated circuits, it is no longer necessary to interconnect physically discrete individual components into a circuit module. Steps are being taken toward developing techniques for fabricating combinations of circuit modules without requiring separate packaging and interconnection operations. It is believed that ultimately major subassemblies will be made as a single unit by batch-fabrication processes.

One of the largest problems facing the widespread application of integrated circuits is that of efficient packaging and finding suitable interconnection techniques. This involves questions such as the maximum size of a "throw away" unit, spares and logistics, maintenance, and flexibility. For example, is it advantageous to have a computer fabricated with a few hundred modules of packages, each of which is unique, to minimize the total amount of equipment and cost? Or, is it desirable to use five or ten times as many modules or packages, of perhaps 20 - 50 different types, to enable stocking of less spares? These types of questions have to be answered before a 1970 system is designed.

2.6.1 Classification of Components

Components discussed in this section are the logical components used in mechanizing the control, arithmetic, and other logical functions in a digital system. Memories and peripheral equipment are not considered components in the context of this discussion. Components considered here are those necessary for performing logical operations, providing temporary storage of the results of logical operations, and amplifying or shaping signals. Examples of these are diode gates, flip-flops, and transistor amplifiers respectively.

These components can be classified by whether they are active or passive, by the method of fabrication, by whether they are electronic, magnetic or optical, by what circuit or logical function they perform, and on the basis of other characteristics, such as speed or cost. The major classifications used in this discussion are: electronic, magnetic, or optical. Most of the discussion is devoted to electronic components which are classified on their method of fabrication. One method of fabrication is by the use of discrete components such as individual transistors, diodes, resistors, and capacitors. Several other methods of fabrication are classed under the general category of "integrated circuits".

Integrated circuits can be divided into four categories, again based on the method of fabrication:

1) Hybrid circuits in which passive elements are printed on a ceramic substrate, and discrete (but unpackaged) active components are connected to printed interconnections on the same substrate. This combination is then packaged as a single unit. (The "solid logic" components used in the new IBM 360 system are examples of this method of fabrication).

2) Monolithic integrated circuits in which a number of active elements (e.g. transistors and diodes) and the associated passive elements to perform a specific circuit function, or set of circuit functions, are fabricated by diffusion processes in a single silicon chip.

3) Hybrid monolithic thin-film circuits in which active elements, and possibly certain passive elements, are diffused into a silicon chip as in the preceding case but with additional thin film passive elements and interconnections fabricated on top of the same silicon chip by vacuum deposition processes.

4) Active thin-film circuits in which both the active components as well as the passive components are fabricated by vacuum deposition of thin-film elements.

All-magnetic logic components and each of the types of integrated circuits listed above are discussed in further detail in Section 2.6.5

2.6.2 Sources of Information

2.6.2.1 People and Organizations

Organizations with whom components and packaging techniques have been discussed include the following:

Motorola Semiconductor Div. Phoenix, Arizona	Integrated circuit sense amplifiers Integrated circuit storage registers Monolithic integrated circuits Hybrid integrated circuits
Remington Rand UNIVAC St. Paul, Minn.	Hybrid integrated circuits Integrated circuit reliability & failure analysis Packaging techniques
Control Data Corp. St. Paul, Minn.	Integrated circuit applications Packaging techniques

Autonetics Anaheim, Calif.	Monolithic integrated circuits Integrated field-effect-transistor circuits Integrated circuit packaging techniques
Bunker-Ramo Corp. Canoga Park, Calif.	Monolithic integrated circuits Integrated circuit sense amplifiers
RCA Laboratories Princeton, New Jersey	Integrated field-effect-transistors Metal oxide semiconductor integrated circuits Active thin film integrated circuits
Hughes Semiconductor Div. Newport Beach, Calif.	Integrated circuit packaging techniques Monolithic integrated circuits Hybrid integrated circuits Active thin film integrated circuit
Sylvania Waltham, Mass.	Tunnel diode circuits
ONR Washington, D.C.	Optical components
RADC Rome, New York	Optical components
SRI Menlo Park, Calif.	All magnetic logic Cellular logic for integrated circuits Electron beam fabrication Fluid logic
Fairchild Semiconductor Mountainview, Calif.	Monolithic integrated circuits Hybrid integrated circuits
Optics Technology Belmont, Calif.	Optical components
NASA Washington, D.C.	Active thin-film integrated circuits Monolithic integrated circuits Packaging techniques
National Security Agency Fort Mead, Va.	Optical techniques Integrated circuits

Information obtained during discussions with personnel of these organizations provided a basis for much of the information in other sections of this report. The opinions of experts in specific areas in these organizations were solicited concerning the advantages, disadvantages, limitations and future prospects for different circuit and packaging techniques.

2.6.2.2 Literature

An extensive list of references pertinent to the study of components and packaging techniques is given in the Bibliography. Many of these references have been scanned but only a limited number of the more important ones have been studied in detail to date. A study of these references has contributed to the material presented in subsequent parts of this section, and direct quotations have been used where noted. The more pertinent and important of these references will be studied in detail during the remainder of this investigation and new references will be included to reflect material published or discovered subsequent to the preparation of this Bibliography.

2.6.3 Components and Packaging Characteristics for ANTACCS

It is anticipated that relatively high-speed components with high reliability will be required for ANTACCS and AMTACCS equipments. These components and packaging techniques will have to be chosen on the basis of their ability to meet specifications for shipboard and ground-based military systems. Characteristics of applicable components and packaging techniques will be compared and evaluated but the choice of specific characteristics will depend upon the details of machine organization and the results of the requirements analysis. Components and packaging techniques investigated will include those necessary for meeting all requirements both within the central computer and in peripheral and auxiliary equipment.

2.6.4 Applications of Components in the Naval Environment

It is anticipated that all components and packaging requirements for shipboard and ground-based military environments for ANTACCS and AMTACCS type systems will be covered by this study. Emphasis will be placed on digital techniques, but certain appropriate analog techniques (e.g. memory sense amplifiers, analog-to-digital converters, digital-to-analog converters, etc.) will be considered. The specific applications of these components will be considered in further detail during the remainder of this study.

2.6.5 Current Status Review

In most available commercial and military computers, logical operations are mechanized with discrete semiconductor circuits - usually transistor flip-flops, transistor amplifiers, and transistor or diode gates. Few such discrete semiconductor circuits will be in use in 1970.

Logical components investigated so far during this study include:

Cryogenic logic
Fluid logic
Optical logic
Semiconductor logic using special elements (e.g. tunnel diodes)
All-magnetic logic
Semiconductor integrated circuits

Most of the time to date has been devoted to investigating semiconductor integrated circuit techniques for digital equipment. All of the types of components listed above are discussed briefly in this section, but the major part of the discussion is devoted to integrated circuits. Packaging techniques are also discussed in some detail. In analyzing components and packaging techniques for a 1970 system, primary consideration should be given to their adaptability to batch-fabrication techniques. Microelectronics and batch-fabrication techniques

are frequently associated and discussed as though they were synonymous However, there is a distinction in that the term "microelectronics" places emphasis on miniaturization and small size; whereas the term "batch-fabrication" places emphasis on methods of fabrication, these are methodized to permit relatively large numbers of elements to be fabricated in a "batch" without the necessity for individual handling of discrete elements.

A number of microelectronic techniques are not adaptable to batch-fabrication. On the other hand, techniques necessary to achieve batch-fabrication processes tend to lead to small sizes of individual elements and hence to microelectronics.

2.6.5.1 Fluid Logic

Fluid logic is usually mechanized by hydraulic or pneumatic systems in which small mechanical movements are used to switch the path or flow of a hydraulic or pneumatic media e.g. oil or air[1]. The major disadvantages of fluid logic are the relatively slow response time (milliseconds) and the size and weight compared to equivalent integrated semiconductor circuits. Fluid logic offers advantages in some adverse environments such as high temperature, electromagnetic fields, and nuclear radiation. Fluid logic may also offer advantages (e.g. lower cost) in applications where the initial input information is in a mechanical form and a mechanical output is required. An example of this is a desk calculator where the initial inputs are key depressions and the outputs are mechanical printing operations. Fluid logic may be applicable to some shipboard functions, such as weapon direction and ship's control. However, fluid logic will not be competitive with integrated circuits for logical functions in the central processor and auxiliary equipment for the information processing portion of a 1970 ANTACCS system.

2.6.5.2 Cryogenic Logic

Cryogenic techniques have been discussed previously in the section of this report dealing with memories. Cryogenic logic and switching devices, such as the cryotron, have been proposed for computer use for approximately ten years. During this time, they have not been proved superior to semiconductor techniques. Although there is some controversy concerning this, most workers in the field concede that logical components are the least likely application for cryogenic techniques in a computer[2]. Most of the cryogenic research and development work remaining at this time is concentrated on associative and large-capacity memories. Cryogenic logic and switching is considered primarily as an adjunct to a large-capacity or an associative cryogenic memory. The use of cryotrons for the selection tree in a large-capacity cryogenic memory is an example. It is very unlikely that cryogenic logic techniques will be competitive with semiconductor integrated circuit logic in 1970.

2.6.5.3 Optical Logic

There has been considerable interest in the possibility of using optical logic devices in computers because of the inherent speed theoretically possible when working with light. Recent developments in fiber optics and lasers have accelerated this interest[3,4,5]. Some of the characteristics of lasers that make them attractive for computer use are:

1) The output is coherent and monochromatic
2) Very high frequencies are possible
3) The beam is highly collimated
4) High-power intensity
5) Capable of either continuous or pulse operation.

Fiber optics have the capability of conducting light around curved paths, and hence they offer interconnection possibilities similar to the use of wires in carrying electrons. However, lasers and fiber optics will see use in memories and display areas before they will be successfully used as logical components. Optical logic techniques offer great promise for the long range future, but they will not be feasible for use in a 1970 system.

2.6.5.4 Special Semiconductor Elements

A number of unique or special purpose semiconductor devices have been proposed for use in computers. Of these, the most serious consideration has been given to the tunnel diode [6,7]. Tunnel diodes have been proposed for high-speed, small-capacity memories as well as high-speed logical components. Of the various approaches to "kilomegacycle circuits" tunnel diodes are considered the most practical, although the rates of approximately 200 - 500 megacycles at which they have been used do not quite fall in the kilomegacycle range. Soon after they were introduced 4 or 5 years ago, tunnel diodes were considered by many people to be an exciting solution to the high-speed computer circuit problem. However, difficulties in working with a two terminal device such as the tunnel diode have seriously dampened this enthusiasm. The problems of interconnection techniques for tunnel diode circuits operating at a frequency of several hundred megacycles have proved to be difficult. Systems become very expensive as a result of the discrete mechanical configurations required for interconnections and shielding. Although tunnel diode logic circuits are feasible, they will not be competitive with integrated circuit techniques for an ANTACCS type system in 1970.

2.6.5.5 All-magnetic Logic

Magnetic elements can be used in a digital system for logic as well as for storage functions. However, magnetic elements have not enjoyed the widespread use or success as logical elements that they have as

memory elements. This is, of course, due to the difference in the nature and requirements of memory components and logic components. A single word location in a memory is addressed at one time, and a large driving current, low sense signal, and destructive read out are acceptable. On the other hand, for a logic element it is necessary to provide some form of gain, and to sense the state of the device without changing it.

A number of applications for all-magnetic logic and a number of types of logical configurations and elements have been described in the literature[8,9,10,11]. All-magnetic logic offers several distinct advantages including:

1) High reliability
2) Radiation resistance
3) High temperature operation
4) Low stand-by power
5) Non volatile
6) Low power required at low frequencies
7) Cost (in some cases).

The major disadvantages in the use of all-magnetic logic have been the inherent slow speed and the lack of a steady state output indication. For most applications all-magnetic logic circuits have not proved themselves sufficiently advantageous with respect to either cost or performance to encourage their use in place of the simpler and more common semiconductor circuits.

The characteristics of all-magnetic logic are ideal for certain applications such as an onboard computer in a deep space probe. In this application, very low speeds are acceptable and radiation resistance, low standby power (since the spacecraft is inoperative for the long cruise periods of the mission) and high reliability are important. However, for the type of applications encountered in an ANTACCS system, all-magnetic logic is not considered competitive with semiconductor

circuits - particularly not with integrated circuit techniques for a 1970 system. The radiation resistance characteristic and the high reliability would be important if future developments prove that integrated circuits are not as reliable as magnetic logic. However, it appears that semiconductor integrated circuits will approach the reliability of all-magnetic logic, and that the cost of these elements will be less than that for the discrete elements used in magnetic logic. The speeds of all-magnetic logic are not sufficient for the central processor. The multi-apertured devices found most suitable for magnetic logic have been limited to rates of a few hundred kilocycles per second. For other shipboard functions such as peripheral equipment, weapon direction systems, and ship's control systems where high speeds are not required, magnetic logic may prove a good choice. It is possible that new developments in thin-film integrated magnetic circuits in the next few years may enhance the performance and significantly reduce the cost of all-magnetic logic.

2.6.5.6 Integrated Circuits

Integrated semiconductor circuits are by far the outstanding candidate for the logical mechanization of a 1970 ANTACCS system. Integrated circuits have been proved feasible and successful, and are currently being used in several military computers. Hybrid integrated circuits are used in the Remington Rand CP667 computer for NTDS and in the new IBM System 360 commercial computer[12,13]. Monolithic integrated circuits have been used in the Autonetics Monica Computer, and are being used by Litton in the computer for the new F-111 (TFX)[14]. Estimates of the military use of integrated circuits range from 40 to 50% of all military electronics in 1970 to approximately 75% in 1973[15,16,17]. Since digital circuitry is more adaptable to integrated circuit techniques, the estimates are even higher for computer and data processing equipment - approximately 70% by 1970. Actually, this figure will probably be closer to 90% (not including the memory) for new digital equipment designed to become operational in 1970.

Integrated circuits are not basically new components in the sense that lasers are, but rather they represent radically new methods of fabricating and packaging semiconductor circuitry. The reduction in the number of discrete components, resulting from fabricating complete circuits as a single component, offers significant advantages in terms of reliability, cost, and size. Batch-fabrication of volume quantities of integrated circuits will result in significantly lower costs than is achieved by the present printed circuit and hand wiring of basic components and circuit modules.

Mr. J. M. Bridges, of the Department of Defense, states that "a semiconductor integral circuit containing the equivalent of some 20 parts displays the same failure rate as a single conventional transistor," and he predicts failure rates of approximately 0.0001% per 1000 hours[18]. Failure rates as low as 0.001 to 0.0002% per 1000 hours are anticipated for the advanced Minuteman computer, and a number of estimates place the ultimate reliability of monolithic integrated circuits as 0.0001% failures per 1000 hours[14,19]. Dr. Noyce of Fairchild Semiconductor has described the actual reliability experienced on two specific aerospace computers as follows:[19]

> "We have data on two operating medium-sized computers that use integrated circuits. The first is the Apollo guidance computer, designed by MIT and built by Raytheon. It has accumulated 19 million operating hours on its integrated circuits, in which time two failures have occurred--an initial failure, and the other a failure, external to the package, that was caused by moving the computer. The second system, the MAGIC 1, an airborne computer built by the AC Spark Plug Computer Division, has accumulated 15 1/4 million hours with two failures. Fairchild's in-house life-test program, with 33 million total operating hours, has had a total of eight failures; of these, five accumulated during the first 6 2/3 million hours and only three occurred on more recent units during the last 26,334,982 hours. These data are not extrapolated from accelerated tests, but are actual, observed operational failure rates, and include early production units in some cases. Considering the complexity of the function performed by these circuits, the integrated circuit equipment today is ten times more reliable than its discrete component counterpart."

The higher reliability of integrated circuits results from the fact that there are fewer individual components, circuits are of smaller size, there are fewer connections of dissimilar metals, most connections are made by vacuum deposition, and there is less handling of components.

Based on considerations of reliability, cost, size, weight, and environmental conditions, it is reasonable to expect that integrated circuits will account for almost all of the logical components in a 1970 shipboard or ground-based military system.

There are four basic types of integrated circuits although these are sometimes called by different names and in some cases grouped differently. The term hybrid is particularly confusing since it is applied to thin-film passive components with discrete active components and to thin-film passive components with monolithic active components. These four types are:

1) Hybrid Discrete Thin-film (or Thick-film) Circuits[13]
   In this type of circuit, passive elements, such as resistors and capacitors, are printed on a ceramic or glass substrate by either vacuum deposition of thin-film elements, or by printing of thick-film elements in a process similar to silk screening. Discrete (but unpackaged) active components are connected to printed or deposited interconnections on the same substrate. The combination is then packaged as a single unit. This is an interim type circuit that was developed before monolithic and hybrid monolithic circuits were technically feasible for large scale production.

   This type of circuit offers the advantage that the passive components can be made cheaply with tightly controlled tolerances. Relatively large values of capacitance can be fabricated and resistance values can be maintained within a few percent. As a result, this approach is more adaptable to linear circuits, such as differential amplifiers and

analog circuitry, at present than is the monolithic integrated circuit. This type of circuit also has the advantage that there are no interactions and parasitic capacitances between the different elements as is the case for the monolithic integrated circuit. It has the disadvantage that the active elements must be handled as discrete elements. The reliability is probably not as high, due to the handling of the active elements and the soldering of these elements to the printed interconnections on the substrate. The cost will be higher and large arrays of logical circuits cannot be batch-fabricated. It is believed that this type of circuit will phase out before 1970 with preference being given to the second and third type of integrated circuits discussed below.

2) Monolithic Integrated Circuits[20]

This type of circuit is completely integrated. Active elements (e.g. transistors and diodes) and the associated passive elements (e.g. resistors and capacitors) necessary to perform a specific circuit function or set of circuit functions, are fabricated by a series of diffusion processes in a single silicon chip. This circuit has the advantage that all components in the circuit are made during the same series of operations, and that multiple circuits of this type can be batch-fabricated in a single set of operations.

This type of circuit should ultimately be cheaper to fabricate and more reliable due to the ability to make all interconnections by vacuum deposition processes. It is more adaptable to the batch-fabrication of large interconnected arrays such as a major segment of an arithmetic unit. There have been three major disadvantages with respect to monolithic integrated circuits to date:

a). The interaction between semiconductor elements diffused in the same silicon chip and the resulting parasitic capacitances.

b). Difficulty in maintaining resistor tolerances better than approximately 20%.

c). Difficulty in fabricating capacitancies of more than a few micro-microfarads.

The yield of this type circuit has not been as satisfactory since any individual bad element makes the entire circuit bad. It is difficult to get accurate information on the yield experienced by manufacturers, but estimates range from approximately 1% to 20% for present high-grade military type circuits with yields of 50 to 90% predicted for the future. Monolithic integrated circuits are well suited to digital applications where component values are not as critical, but they are not satisfactory for most types of linear circuits at present because of the interactions and the difficulty in controlling tight tolerances. Intensive research and development efforts are being expended on the problems of monolithic integrated circuits and rapid progress is being made. Both Signetics and Motorola have reported success in isolating the components in a monolithic integrated circuit to reduce the parasitic capacitance. This should increase the speed of circuits of this type and permit their application in certain types of linear circuits. It is anticipated that this type of circuit will be the major integrated circuit technique used in digital applications within the next few years.

3) Hybrid Monolithic Thin-film Circuits[21]

In this type of circuit active elements, and possibly certain passive elements, are diffused into a single silicon chip as in the preceding case. However, additional thin-film passive elements as well as interconnections are fabricated on top of the silicon chip by vacuum deposition processes.

This technique combines the advantages of the first type of hybrid circuit discussed with the advantages of the completely monolithic integrated circuit. Tight tolerances on resistors and capacitors can be maintained and relatively large values of capacitance fabricated while not handling discrete components. Batch-fabrication of arrays of elements and circuits in a single set of processes, and higher reliability resulting from vacuum deposited interconnections are achieved. With this type circuit, it is possible to obtain many of the cost and reliability advantages of the completely monolithic integrated circuit while fabricating higher quality components. The fabrication of linear integrated circuits, such as differential amplifiers and other analog type circuits, is facilitated. Several hundred thousand ohms of resistance and several hundred micromicrofarads of capacitance can be obtained on an integrated circuit using this hybrid approach. Resistor tolerances of better than 10%, and capacity tolerances of two parts per million can be obtained relatively easily. Higher resistor tolerances can be achieved by "trimming" the resistors during the test operation.

This technique will be used along with the completely monolithic integrated circuit for the next five to eight years at least. Monolithic integrated circuits will be used wherever possible, with the hybrid monolithic thin-film circuit being used to complement and supplement them where higher tolerance components or larger values of capacitance are required. Unless the isolation problem in the monolithic integrated circuit is completely overcome, the hybrid monolithic thin-film approach will also permit higher speeds.

4) Active Thin-film Element Circuits[22,23].

In this type of circuit, both the active components and the passive components are fabricated by vacuum deposition of thin-film elements.

Predictions concerning the date at which active thin-film elements will become feasible vary widely - from "almost immediately" to "not less than five years". The longer estimate is probably the more accurate one with the possible exception of a related device - the metal-oxide-semiconductor. A field effect transistor can be fabricated in this way by depositing germanium or silicon on a passive substrate, depositing an oxide insulator such as silicon monoxide, and depositing aluminum plates for connections and distributed capacitance. Cadmium-sulphide is frequently used instead of germanium or silicon.

This type of device offers excellent radiation resistance characteristics and is quite amenable to batch-fabrication of large interconnected arrays with minimum interaction. This circuit is attractive because of its simplicity. RCA reports yields of 90 - 95% compared to approximately 20% for conventional silicon integrated circuits.

Another advantage of this type of device is that it is ideally suited to a complementary symmetry type of circuit because of its bipolar nature. One field effect transistor can essentially act as the load line for another field effect transistor. As the characteristics of one transistor change due to external conditions, the characteristics of the other change also, resulting in a lesser effect of the net change.

Although the metal oxide semiconductor type of field effect transistor can perhaps be used in a 1970 system, it is doubtful that any other types of thin-film active elements, such as thin-film transistors, will be in use until later during the period between 1970 and 1980.

In considering integrated circuits for logical components, it is also necessary to consider the type of logical configuration to be used. The major types are:

1) Direct coupled transistor logic (DCTL)
2) Diode transistor logic (DTL)
3) Resistor transistor logic (RTL)
4) Resistor capacitor transistor logic (RCTL)
5) Transistor coupled transistor logic (TTL)
6) Emitter coupled transistor logic (ECTL) also referred to as current mode logic (CML, or MECL).

The choice between these different types of logical circuit depends upon the function for which the circuit is chosen and the method of fabrication of the integrated circuit itself. The relative importance of speed, cost, power, size, and reliability will vary with different applications and different circuit fabrication techniques. The major advantages and disadvantages of each type are shown in the Table 2.9 below:[24,25,26,27]

TABLE 2.9

Logic Circuits	Advantages	Disadvantages
DCTL	Low power Simplicity	Poor load distribution Noise sensitive Low fan-out
RTL	Simplicity Better load	Noise sensitivity Slower speed than DCTL
RCTL	Good load distribution Good noise rejection High fan out Low power	Slower speed More complex circuit
TTL	High speed Simplicity Low power	Low fan-out Poor noise sensitivity

Logic Circuits	Advantages	Disadvantages
DTL	Good noise immunity Good isolation Good fan-in capability Low power	Two power supplies required, Slower speed, Low fan-out
ECTL	Simplicity Good load distribution High speed operation	More critical circuit parameter More components Two power supplies Noise sensitivity

Monolithic integrated circuit application for linear circuits have not progressed as far due to the problems with interaction between components, parasitic capacitance, and the difficulty of fabricating larger values of capacitance. As a result, most of the success in integrating linear circuits has been with hybrid type integrated circuits. Differential amplifiers and other types of analog computer circuits have been difficult to mechanize with monolithic circuits for these reasons. A good deal of effort has been expended on certain types of linear circuits for computers--particularly sense amplifiers for memories[28].

It is believed that satisfactory memory sense amplifiers in monolithic form will be available within 1 - 2 years. This will have a significant effect on memory costs for large capacity memories as discussed in the memory section of this report. Other types of circuits, such as magnetic memory drive circuitry, have been difficult to mechanize in monolithic form because of the power handling requirements. The solution to this problem is not as close as the solution to the sense amplifier problem.

Ultimately, the successful widespread use of integrated circuits in computers and information processing systems will depend upon the industry's ability to find new and more effective ways of utilizing larger arrays of individual circuits. Although significant improvements can be achieved by replacing the discrete semiconductor circuits with integrated circuits in present types of logical configurations and machine organization, new approaches will be required to realize the ultimate potential of integrated circuits. It will be necessary

to fabricate groups of circuits in "functional electronic blocks" or in some kind of generalized "cellular logic" array[29,30]. The use of larger function electronic blocks depends upon techniques for making major segments of a machine more repetitive, so that a relatively large number of similar blocks can be used. This is possible now in some arithmetic parts of a parallel machine where successive stages of registers and adder circuitry are repetitive. However, it is very difficult at this time in the control parts of a machine where there is little tendency for repetitiveness. In a cellular array, a large number of similar circuits would be fabricated on a chip with appropriate means of semi-standard interconnections between them. Methods of designing computers with this type of structure need further investigation. In either case, problems of redundancy, the ability to work with a limited number of bad elements, and interconnection techniques need extensive work.

2.6.5.7 Packaging

It has been pointed out that one reason for the increased reliability of integrated circuits is that groups of elements can be interconnected by vacuum deposition processes rather than by soldering, welding, or crimping[27,31,32]. The use of vacuum deposition techniques can lead to the formation of molecular junctions at the points of interconnections rather than the interfaces that result from other methods. The vacuum deposition of interconnections also removes much of the human element. This advantage has been described by Mr. McKenzie of Electronics magazine as follows:

"Whereas welding or soldering constitute a weakening of reliability, owing to possible carelessness or ineptitute of a technician, the thin-film applied through a fixed mask would necessarily provide automatic and uniform interconnection.

Present interconnection practice involves many methods of making joints and the connecting leads themselves are of materials chosen as best suited for joining. Hand soldering may always be used for a number of larger joints or touch-up work, but as the size of units decreases the uncertainty as well as the damage sometimes caused will continue to curtail use of hand soldering.

Automatic dip soldering and flow soldering involve certain hazards such as overheating, corrosion from flux, and particles of excess solder. The joints are good only to the melting point of the solder used. Special techniques such as the use of solder preforms and hot air, are continually under investigation but the limitations of the soft-solder joints are understood and efforts are directed to better methods of joining.

Welded circuits can be successfully made and the joints hold up to temperatures of about 1,500° F. Initial problems of obtaining satisfactory welds with tinned copper, brass and nickel-iron alloy wires have been largely eliminated through the use of nickel, nickel-clad copper and stainless clad copper. Improvements in welding techniques have produced successful joints even with formerly difficult materials. Data are still lacking on the definite improvement in reliability of the welded over the soldered joint but it may be as high as 20 to 1."[31]

A large percentage of the bulk of present day computers is composed of interconnections, connectors, and cables. The use of functional electronic blocks or cellular logic permitting the batch-fabrication of interconnections for large groups of circuits will greatly alleviate this problem[29,30,33,34,35].

The inter-connection of integrated circuits is another possible application for lasers. Many of the problems of soldering and welding inter-connections can possibly be overcome by using a laser micro-welding technique[36]. The use of a laser for welding does not require high vacuum equipment as does electron beam welding equipment, no foreign materials are introduced into the joint as in soldering, and heating of the elements is not necessary. No pressure is applied to the joint, and the laser beam can reach places that are inaccessible to other welding techniques. The use of the high energy beam from the laser for welding purposes has been demonstrated and is being further investigated.

Interconnection between integrated circuit blocks has been accomplished by a number of techniques including the use of multi-layer boards, a cord wood structure, and micromodule techniques.

The multi-layer board approach seems to be the most widely acceptable at this time[34]. The choice of interconnection technique also involves a number of questions other than the actual making of interconnections-- What is the minimum size of throw-away package? What is the effect on maintenance and spares? How is layout and organization of the machine affected? How adaptable is the technique to batch-fabrication? Is adequate heat transfer provided? What is the volumetric efficiency?

Another problem in the assembly of groups of integrated circuits, as in any other type of electronics, is that of cooling. One interesting approach to this problem is to provide a completely controlled atmosphere by immersing all the components in a liquid such as Freon. The Freon can be maintained at a constant temperature by external water cooling to permit close control of the temperature around the individual components. It also keeps foreign substances such as dust and humidity away from the components. The ability to control the temperature and environment in which the components are working simplifies this basic circuit design and permits higher performance circuitry by removing the necessity for working over a large temperature range.

The problems of packaging and interconnection of basic circuit modules will be investigated further in the remainder of this study.

2.6.6 Availability of Components in the 1970-1980 Period

Completely integrated circuit components capable of fulfilling the requirements for the central processor and peripheral equipment will be available prior to 1970. All magnetic logic for slower speed application will be available but may not be competitive. It is unlikely that optical logical components will be available until at least the mid 1970's. Cryogenic logic and special semi-conductor devices such as tunnel diodes will not be competitive with integrated circuits for ANTACCS type applications.

Although there is much work to be done in the area of packaging techniques and integrated circuit components, it is believed that adequate techniques will be available for use in a 1970 system.

It is possible that two basic types of logical components will be used in an ANTACCS type system in the 1970 time period. One of these will be high-speed semiconductor integrated circuit components with large fan-in and fan-out capabilities for mechanizing the central processor and other high-speed parts of the system. For economy purposes, a second type of circuit might be used in peripheral equipment and slow-speed applications. These circuits may be either a slow-speed semi-conductor integrated circuit type component or perhaps all-magnetic logic components. If the cost differential is not significant between the two categories of components, the high-speed integrated circuit components may be used even in the slow-speed peripheral equipment to provide a higher degree of standardization and to reduce the spares and maintenance requirements.

2.6.7 Limitations of Present or Planned Components and Packaging Techniques

Limitations of cyrogenic logic, fluid logic, and special semi-conductor elements have been discussed previously. The primary limitations of all-magnetic logic is one of speed, and it is possible that this type of component will be used in slow-speed applications. No limitations on the availability or capability of semi-conductor integrated circuit components for applications in ANTACCS type equipment are foreseen for the 1970 period. Integrated circuits will be capable of meeting and exceeding all the requirements for digital type circuits with the possible exception of high powered output components.

2.6.8 Recommended Developments to Meet ANTACCS Needs

No additional developments in the area of logic components are needed to meet ANTACCS needs for the 1970 period. Adequate research and development efforts are currently underway on integrated circuits to assure the necessary components for a future NTDS system. However, additional effort is needed to develop improved packaging techniques and packing philosophy for the optimum utilization of integrated circuit techniques and batch-fabrication processes. This will require work not only in the specific area of packaging techniques, but also in the areas of machine organization to permit types of logical configurations that are readily adaptable to the batch-fabrication of large arrays of circuits.

2.6.9 Evaluation Criteria Recommended

Recommended criteria for evaluating components and packaging techniques will include the following:

Type of logic
Type of circuit elements
Type of fabrication
Number of active elements per circuit package
Number of passive elements per circuit package
Approximate cost per circuit package
Propagation delay
Power dissipation
Power requirements
Permissible levels of logic
Fan-in and fan-out ratios
Noise sensitivity
Nature of active elements
Stand-by power requirements
Operating power requirements
Susceptibility to nuclear radiation effects
Susceptibility to electromagnetic interference
Generation of electromagnetic interference
Susceptibility to shock and vibration
Susceptibility to humidity
Operating temperature range
Special requirements (e.g. cooling or refrigeration)
Approximate date of first production quantity applications
Batch-fabrication techniques

Some of these will rule out certain types of components without the necessity for detailed comparisons. Applicable components will be compared and evaluated on the basis of those characteristics that directly affect the relative value or importance of competitive components. For example, components will not be compared on the basis of their susceptibility to nuclear radiation effects, but this will be cited as an advantage of specific techniques where applicable. On the other hand, the propagation delay, or fan-in and fan-out ratios, will probably be compared in detail for different types of components or circuit configurations.

2.6.10 Conclusions and Recommendations

Most of the digital parts and a large percentage of the analog parts of an ANTACCS system for 1970 will be mechanized with semiconductor integrated circuits. Emphasis should be placed on batch-fabrication techniques, not only with respect to the circuits themselves, but with respect to machine organization approaches that permit the fabrication of large arrays of circuits in a single set of processing operations. Further consideration will be given to specific uses of hydraulic logic and all-magnetic logic during the remainder of this study, but integrated circuits are considered to be the primary candidate for mechanization of the 1970 system.

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2.7 ADVANCED USAGE TECHNIQUES

For purposes of this present definition, advanced usage techniques are construed to be those which, while they may be beyond the "experimental" stage, have as yet no wide application of a pragmatic sort. Certain of the techniques are hardware-oriented. That is, the basis for a new family of usages or for a programming philosophy or problem approach may arise because of the availability of new hardware features or departures from customary or ordinary logic design. The inclusion of interrupt logic in general purpose computers, for instance, made the whole field of real-time and on-line applications workable and practical. Similarly the stored-logic design of the computer of the BRN-3 navigation set made the use of interpretive programming practical in that application. Such programming had long been judged "impractical" on the conventional digital computer.

2.7.1 Classification of Advanced Usage Techniques

Based on preliminary investigations and searches of the literature, the following categories of investigation have been established:

2.7.1.1 Heuristics and Machine Learning

The apparent applicable advances in heuristics programming and problem formulation, as related to command and control seem to indicate that little of a generally pertinent nature is to be found in this area. The same is true of machine learning. Therefore, these two areas have been combined.

2.7.1.2 System Diagnosis

The rapidly-growing importance of this topic, particularly in complex data systems, which include one or more digital computing modules, warrants its conclusion among the advanced usage techniques, and emphasis on its study.

System self-diagnosis is, in some measure, hardware-determined. The abilities for accomplishing diagnosis under computing module control are provided, usually, by the existence of the proper kinds of communication paths, and an interrupt structure or its equivalent which permits the proper level of query and response within the system.

But a good deal of diagnosis is found in properly-designed programming.

Certain kinds of diagnosis are not fault-oriented. There may be a diagnosis in real time, as in the Quotron stock-quoting system which analyzes system traffic load and permits deferring of low priority or less-important messages.

Among the topics of interest in diagnosis are the following:

1) Preserving memory contents during power failure or other catastrophic failure.

2) Cycling through a pre-determined set of tests, either in free time or in real time.

3) Ability to recycle tests arbitrarily under operator direction.

4) The use of redundancy as a diagnosis tool, and to permit system graceful degradation.

5) The use of back-up systems of equal or less ability.

6) The use and design of background diagnostic programs in real-time systems.

All of the above apply not only to on-line diagnosis of the computational and control sub-system, but also to on-line diagnosis of communications, sensor and weapons subsystems.

2.7.1.3 Pattern Recognition

Pattern recognition work in digital computers is progressing rapidly enough to warrant its inclusion here and the attendant expenditure of time. Pattern recognition is a broader subject than character recognition. Character recognition may be thought of as an important subset of pattern recognition in which the set of patterns (font) is known and bounded. Neither of these is necessarily so in pattern recognition, since one task conceivable may be the determination of similarities in two or more patterns, none of which is previously known.

Among the techniques now used in experimental pattern recognition are the construction of Boolean matrices in which the pattern is, in essence, described as an array of ones and zeroes (blacks and whites). Various operations, such as ANDing and shifting matrices, permit pattern comparisons and alterations.

Feature extraction also is used to define categorized lines, curves, and intersections in a pattern, and to assign them to differently-chosen envelopes or regions which may aid in recognition. Contour analysis, similar to that performed in cartography, is also used as a technique in machine pattern recognition.

2.7.1.4 Associative Memories and Related Techniques

The development of associative memories of content-addressable and other types, together with their obvious applicability to many problems in command and control, makes emphasis on this area desirable in the present work. Working modules of content-addressable memories have been built at various places, notably by Goodyear. Research work has been done and prototypes have been tested at such places as the Bunker-Ramo Corporation.

Content-addressable memories, in which information is stored as adjoined words, or in which search or addressing is possible on the basis of partial words or information keys, is the usual type of design. However, most structures today preclude the finding of dual entries with certainty. Other possible structures have also beein investigated, including, for example, those in which indexing, or relative address structure, becomes a built-in part of the memory module.

Current designs do not compete in capacity/cost ratio with conventionally-organized memories, though probably this situation will change rapidly upward with increased use of associative memories.

2.7.1.5 Adaptive Systems

Development of these systems, particularly where computers and display modules work in a single system, makes inclusion of them reasonable here.

Adaptive systems are those that change their basis of action with environment or history. For example, a speed-sensing system element might have its calibration changed in real time as a result of successive observed positions. Adaptive systems have manifest applications in command and control, and will be investigated in more detail during the balance of the study.

2.7.2 Current Status of the Advanced Usage Subtask

Literature and Source Compilation is under way on this subtask. Manning of the subtask has been structured to schedule completion on or before the end of month ten.

2.8 COMPUTER SYSTEM ORGANIZATION

Computer system organization deals with the design of the larger components of a computer system and their relationship to each other with respect to capability, communication and synchronization. It is an extremely important subject in computer technology since it is the near-unanimous opinion of experts in the field that greater strides will be made in computer efficiency during the next 10 years through organization than through straight hardware improvements at the component level. Computer organization is extremely important for consideration in ANTACCS because of the stringent requirements that are placed on the system and because of the inherent complexities of these large-scale, real-time systems which will implement ANTACCS.

One of the central objectives of the work of computer system organization is to arrive at a series of recommendations on the characteristics of a possible future NTDS family of computers. This objective is motivated as follows:

Sooner or later there will need to be an upgraded family of computers for future NTDS. Within the next three or four years a basic decision will likely be made as to whether computers in the 1970's for NTDS will be upgraded, programmed compatible versions of the present systems, or a new family of computers with different modular components and different instruction repertoires will be designed to take their place. To make that decision it is instructive to examine carefully the characteristics of a future NTDS computer family should it be desirable to develop one.

The work on machine system organization is approximately 25% complete. This part of this Midway Report will consist mostly of an outline of the subject to be considered and the organization and intent of the technical efforts. Only one part of the computer system organization effort is relatively complete. This is the

section on "stored logic" or "microprogrammed" computers. However, in each section of this report on computer system organization there is a brief discussion of the subject matter to be treated in the future work.

2.8.1 Classification of Computer System Organization

For the purposes of the work thus far, this technical area has been divided into the following:

Multi computers and modular concepts
Memory and memory oriented computers
Internal organization
New computer trends
Analog/digital hybrids
Existing NTDS computers.

All of these are perhaps self-explanatory, except "new computer trends". In this area stored logic and microprogrammed computers will be covered, as well as so-called highly-parallel computers, such as those of the Solomon type.

In addition there will be a discussion of: requirements and applications of computer systems in ANTACCS, recommendations and comments on a possible future NTDS computer family, and recommendations and comments on other types of computer equipments such as specialized memories and peripheral or buffering equipments, and majority logic.

2.8.2 Sources of Information

2.8.2.1 People and Companies

At this point there has not been a comprehensive survey of people and companies with respect to this subject. Because of the great familiarity of the project team with current efforts in the country, there will not be a great deal of time spent on a thorough survey. However, it is intended that information and opinions be solicited from

a number of people close to NTDS computer development in the Navy and in industry. As a start in this connection, an extensive interview was held with Mr. Donald Ream of BuShips late in June. Similar interviews will take place in the next few months.

2.8.2.2 Literature

Since the section on stored logic and microprogrammed computers is the only section relatively complete at this time, the bibliography is limited to that technical area. Cited references are listed at the end of the section. General references are in the bibliography.

2.8.3 Multi Computers and Modularity

Since the advantages of multi computers and modularity for ANTACCS are obvious with respect to reliability and expansibility requirements, this technical area of computer organization is considered to be very important. Although this work is now well under way, for the purposes of the Midway Report the discussion here will be limited to the organization and topics to be considered.

First of all, definitions and motivations will be presented; that is, what multi computers are and why are they important. Next, existing hardware configurations will be examined. This will range from the RW-400 computers and multi-1604 systems for CINCPAC to the D825 systems for NRL. The manner in which these computers are being used will then be discussed. Operational factors of multi computers will be analyzed especially as they relate to the ANTACCS environment. Programming considerations of these larger systems are important since they represent a new challenge to the techniques. Finally, the future uses in ANTACCS will be developed.

2.8.4 Memory and Memory-Oriented Computers

Since the memory is the principal part of a computer, it is important to look at the implications of computer system organization from the point of view of the memory involved and how it is used.

In the other parts of the technology work, memories have been discussed from the standpoint of the hardware configurations and their capabilities as a component. In this section the computer system is discussed from the standpoint of the type of memory and how it fits with the total computer system.

The following topics constitute this section:

Memory types and uses
Memory hierarchies
Memory addressing
Content-addressed or associative memories
Read-only memories
Memory oriented computers

2.8.5 Internal Organization

There are some interesting and important aspects of internal organization which should be examined. Some of these internal organization factors have a big impact on the computer's efficiency and the total computer organization. Some of the topics to be discussed are:

Registers and intra-machine communication
Instruction repertoire
Input/output.

2.8.6 New Computer Trends

2.8.6.1 Stored Logic and Microprogrammed Computers

2.8.6.1.1 General

For a number of years the term stored logic has been equated through usage with microprogramming. Although the literal definitions of these terms, if they could be agreed upon, might indicate that a distinction should be made between them, it would be a minor one; perhaps, simply, a matter of the point of view.

Historically, the term microprogramming is attributed to Wilkes[1,2,3]. The greatest area of agreement concerning the definition among writers on the subject is that it is difficult. For the most part, the question is side stepped and earlier definitions cited (as here).

The difficulty is that the concept was initially seen as a radical departure from conventional design, was implemented somewhat incompletely (in terms of the original concept) and has since come to be thought of in terms of these implementations. It, therefore, takes on varying meanings and associations in different applications of the design.

An ambitious definition is given by Glantz:

"Microprogram (noun)--a program of analytic instructions which the programmer intends to construct from the basic subcommands of a digital computer; a sequence of pseudo-commands which will be translated by hardware into machine sub-commands; a means of building various analytic instructions as needed from the subcommand structure of a computer; a plan for obtaining maximum utilization of the abilities of a digital computer by efficient use of the subcommands of the machine."

"Microprogramming (verb)--to plan an analytical process in a pseudo-code which is to be reduced to the subcommands of a digital computer; to plan an analytical operation in terms of the subcommand structure of a digital computer; to plan an analysis which will utilize the subcommands of a computer in an optimum fashion."

The definition hinges on the words "subcommand" and "subcommand structure" by which is meant simply the manipulation of smaller elements of logic than is usual. The term pseudo-command, although a hackneyed term, may mean almost anything, and is used here to indicate that the code is different or at least unconventional.

Initially, Wilkes envisioned a design somewhat more specific. He conceived the possibility of dynamically alterable instruction sets incorporating the use of two control matrices, a "connection" matrix and a "sequencing" matrix. One matrix would determine a number of

control states and the other would select the specific micro-operations for a particular state. The micro-operations performed would vary then, depending on which set of control logic was in effect.

From this idea of variable logical machines which depend on the state of a control matrix, grew the notion that the programmer could determine a unique order code by combining basic building blocks of logic (variously called, micro-operations, microcommands or subcommands).

The concept is derived from the fact that the typical machine instruction consists of a sequence of basic elementary operations which are, however, fixed (or wired in), i.e. implemented by hardware. These sequences are often complicated and intricate. It was felt that a basic defect of the conventional machine was the probability of the superfluous performance of certain of these subcommands serving no useful purpose in the computation involved.

It was, therefore proposed that the basic machine operations be made available to the programmer. It was recognized that the selection of these basic elements would be of paramount importance since the combinative properties of those chosen would allow the programmer to develop a powerful logical machine. In effect, the logical design of the instruction set would be done by the programmer.

Mercer[4] defines microprogramming as "the technique of designing the control circuits of an electronic digital computer to formally interpret and execute a given set of machine operations, as an equivalent set of sequences of micro-operations, elementary operations that can be executed in one pulse time."

This would tend to place the responsibility in the hands of the logic designer and there is, perhaps, a continuing validity in this viewpoint. However, the original fascination of the concept lay in the possibility that the order code could ultimately be chosen at will by the programmer.

The "one-pulse" criterion, however, is considerably diluted in later developments, although, one of the characteristics of stored logic is the relatively small number of clock pulses per computer instruction. Furthermore, the concept of programming using individual microcommands is not perhaps strictly realized (in the sense of a one-for-one sequencial specification by the programmer). Rather, the programmer ordinarily specifies that a particular set of micro-commands occur (perhaps a dozen or so). He may specify explicitly that a particular one will operate, but usually in combination with others. He may modify in a sensitive manner his choice of micro-commands, and may combine them in many ways. In this respect, however, the stored logic computer may not be so different from the conventional computer which also may have a sensitive control of operation (with various modifiers in its instruction word). Indeed, an occasional debunker's pastime is the "explaining away" of the difference attributed to stored logic computers in conventional terms. The difference may turn out to be one of degree.

Nevertheless, we shall attempt to characterize the development by describing the successful commercial adaptations of the principle and to indicate certain directions that the development of this concept may take. For although there does not appear to be precise agreement as to what constitutes microprogramming or stored logic, and further, whether intrinsically it is a good design, the effects of the development to date are undeniable and the future implications are far-reaching.

It will be seen that certain of the early motiviations for this type of design are no longer so compelling due to other developments (mostly hardware), and that certain other trends have perhaps re-inforced the reason for its continued use.

2.8.6.1.2 Descriptions of Current Stored Logic Computers

Rather than attempt a rigorous or composite definition of stored logic, it is perhaps more instructive to consider the common characteristics of the various stored logic implementations, and to indicate those attributes that, it is generally agreed, characterize its development. For, it is more useful to describe it in terms of what it appears to be now and to derive if possible, what it might presently be, than to define it in terms of what it was originally conceived to be. Parenthetically, it might be noted that the earlier thinking in some respects is the more sophisticated and is perhaps deserving of attention as a sub-topic in the somewhat neglected field of basic computer organization.

The subject of stored logic was presented in a series of articles in the February 1964 issue of Datamation[5,6,7,8,9], and the material contained there was drawn on in preparing this report. The approach taken in these articles was that of describing the commercial machines which were currently marketed as stored logic machines; and the concept is described in terms of these machines. These computers are the TRW-130/133/530 computers, the PB-440 and the C-8401.

However, these computers in some respects are as different from each other as they are from the conventional computer (with which stored logic computers are invariably contrasted). And, perhaps, even more, they depart from the original concepts of stored logic and microprogramming as described by Wilkes. We will, however, examine the characteristics of these machines briefly, noting the common attributes and the distinctive features of each.

1) <u>TRW-130(AN/UYK-1), TRW-530, TRW-133</u>

The TRW-130 is the forerunner of this family of computers. It was initially designed under a Navy contract to serve as a militarized multi-general purpose computer to be used

primarily for shipboard use. The considerable success of this computer was probably due more to other design characteristics (small size, militarized construction, ruggedness, ability to operate with high reliability under adverse environmental conditions),--than to its stored logic design. It is claimed, however, that the stored logic method permitted a simplicity of hardware which would have been impossible to implement economically if a more standard design had been adopted.

The TRW-130 contains 8192 words of 15 bit storage with a six microsecond read-write cycle. The TRW-530 is very similarly organized but has an 18 bit word and certain additional logical options due to the longer instruction word. The TRW-133 incorporates the same design as the TRW-130 but is three times as fast with a two microsecond cycle.

Operation may be thought of as occurring on three levels in the TRW machines; the microcommand level, the machine instruction level and the interpretive level. Microcommands are not accessible individually to the programmer although he specifies them in combinations (explicitly and implicitly) at the machine code level. The machine code command is given the name Logand (Logical Command) and occupies one word of computer memory. A string of logands may be combined to form a routine called a Logram (Logical Program). These routines which are written in a closed subroutine form operate in a sequential fashion and are called into operation by the programmer specifying a list of routines to be operated (a Logram Calling Sequence). When the computer is used in this manner it is said to be operating in the interpretive mode.

The logical organization features accessible working registers which are available to the programmer* for the various machine functions to be performed, sometimes interchangeably. It is the individual transfers between these registers which are recognized as the microcommands which are defined for this machine. These registers are used for arithmetic, memory addressing, logical, and control transfer purposes, and for input/output and temporary storage. For example, the P register is used as an addressing register, as an extension of the arithmetic register, as a shifting register, contains the quotient in division, the least significant part of the product in multiplication, and also acts as an instruction counter for the interpretive level of programming. Incrementing logic is available and, therefore, indexing and program counter sequencing may be assumed by these working registers.

The instruction word format (logand format) features an address option field that provides unusual addressing flexibility. The address for the current operand is ordinarily found in one of four of the working registers mentioned earlier and is specified by the address option field. Indirect addressing is also available and the combination properties of this addressing scheme are designed to minimize addressing overhead.

* The programmer of the lower (machine code) level of coding is given the name logrammer, presumably because he is composing logrames. He programs (or logrames) using logands. The term logander, however, is not valid. The coder who uses logram calling sequences is called a programmer.

The instruction word has various formats and may contain two functional commands (operations codes) per word. These will explicitly call for the execution of particular microcommands. It also contains a control field which has to do with memory accessing (allowing or inhibiting) and address incrementation.

It is sometimes maintained that the combinative properties of this word allows a vast number of unique instructions variously estimated at 8 to 12 thousand. Only a relatively small fraction of these are meaningful, however, and fewer yet are useful. Such sales arguments miss the point since the real strength of the machine involves the way combinations of logands (the more common ones, usually) may be put together rather than the ability to call on an unusual or esoteric instruction from the large number available.

The higher order interpretive language consists of a string of logram calling sequences. The symbolic names of the lograms are arbitrary in the sense that the programmer can name and design his own. The assembly program will assign the starting addresses for the corresponding logand strings.

The logram calling sequence is specified to the computer by placing in sequencial cells the starting addresses of the corresponding machine code subroutines. Interspersed among these addresses are the addresses of any operands needed. Thus, the interpretive mode code (the logram calling sequence) consists simply of a string of addresses of subroutines and operands. It is said that these lograms correspond to the wired-in instructions of other computers, but a closer look would suggest they correspond more closely simply to closed subroutines, which, in fact, is what they are. However, a unique method of subroutine linkage is used which obviates

the necessity for an interpretive routine to sequence the routines. Each subroutine provides its own linkage to the succeeding routine by accessing the address supplied in the calling sequence and placing it in the machine program counter. To facilitate this method, the computer (program) maintains essentially two separate program counter registers which indicate the current position in the calling sequence and the program counter location within the current subroutine.

The interpretive level instruction repertoire is called the Basic Logram Package. The instructions defined by this set resemble those of a one address computer, including single and double precision commands. In addition, special logram packages are available, e.g. floating-point package, matrix arithmetic, etc. It is noted that these routines require memory space and, in general, only those routines needed in the application should be loaded. Although, initially, wide varieties of instruction repertoires were anticipated, including those which could simulate those of other machines, in practice, the Basic Logram Set is most commonly used. In some ways, the interpretive level is the more cumbersome. The most attractive alternative to those familiar enough with the machine operation is to descend to the machine code level utilizing the more efficient methods available there.

The interpretive mode overhead tends to be constant (approximately two logands per logram) which constitutes a rather high cost for the simpler lograms. For example, the logram add command costs 18 microseconds (on the TRW-133), the logand add, only 4 microseconds. Therefore, a combination of the two codes is sometimes preferred, using logands for the simpler functions (add, shift and those commands that can utilize the efficient memory addressing available on that

level, i.e. load, store, and indexing) and using lograms for the more complex such as sine, cosine, BCD to binary conversion, etc. The computer, when programmed in this way, approaches very closely the typical usage one would expect on our conventional computer using machine code and closed subroutines.

2) PB-440

The motivation for the development of the PB-440 was similar to that held by the AN UYK-1 designers-the desire to develop the capability to tailor make instructions sets specially suited to the application. An important feature was added and the claim was made that the first Dual Memory Stored Logic Computer had been developed. A homogenous memory design, it was felt, would just barely hold its own compared with conventional designs (presumably because of the interpretive mode overhead) and therefore, it would be advantageous to place the strings of microsteps in a special module of fast memory.

The PB-440, then, has two classes of memory; a main memory, which operates at a five microsecond cycle time, and Logic Memory (or "control" memory) which is a non-destructive biax memory with a one microsecond read time. The minimum configuration of the computer has 4096 and 256 24-bit words of these types of memory, respectively.

The relatively small amount of fast memory was sufficient to define certain basic instruction sets which could be modified or replaced by reading in new ones, and it was expandable in 256 word modules, if desired.

The format of the PB-440 allows two micro-orders, sometimes called micro-steps, per instruction word. Any of 64 separate micro-order codes may be specified. In addition, the format contains two modifier fields per micro-order which will ordinarily indicate one of seven working registers as operand source and/or destination. Here, as in the TRW machines, the working registers are available to program manipulation (i.e. accessible to the programmer) to an unusually large degree.

The routines stored in fast memory are called microutines. They are called into play by the "control sequence" which utilizes special instructions designed for the purpose. It was noted that the higher language level operation code for the TRW machines was, in fact, simply an address; the address in core memory of the start of the logram. In the PB-440 the operation code will ordinarily refer to a microutine by number (i.e. 1 of 64), and utilize a jump table to facilitate rapid micro-instruction interpretation*.

Special instruction sets include a systems-oriented command list, a scientific/engineering problem-oriented command list, and a FORTRAN set. These are interchangeable by computer memory loading. The instruction sets are normally stored in fast memory but are also executable from main memory. The micro orders are tailored to recognize various data formats such as floating point, or sign-magnitude numbers, and alphanumeric characters.

Program optimization involves the utilization of the time between main memory accesses, referred to as "shadow time", during which useful computing may be accomplished (as long as it does not involve further main memory access).

* From a hardware standpoint, two-level programming is a fiction, since the computer will always remain on one level (i.e. the lower). The interpretive level (which is sometimes referred to as pseudo-code) consists of a macro-instruction control sequence which simply specifies which subroutines are to operate. This is true of all the computers discussed in this report.

3) C-8401

The dual memory concept is also implemented in the Collins Computer, the C-8401 Data Processor. The microprograms are stored in the fast memory, called the instruction memory. This memory is composed of 1024 36 bit words with a read time of one microsecond. The formats of the instruction word allows either two or three transfers to occur. The transfers relate to the exchange of information between exchange registers, certain of which are associated with logical or arithmetic functions. Each of the basic operations is associated with a particular register. A large number of working registers are thus made available to the programmer.

The main memory is composed of 4096 (expandable in 4K modules) 16 bit words with a five microsecond cycle. Thus, up to 15 micro-instructions can be performed during each main memory cycle time. Notice that this assumes a micro-instruction to be a part (or field) of a computer instruction word.

Macro-instructions are stored in main memory and constitute a higher level problem-oriented language. The interpretive mode linkage is effected by an interpretive routine called RNI (Read Next Instruction). This routine maintains an address counter which is stored in one of the exchange registers. It also is able to provide branching in the instruction memory to the subsequent micro-programming to be performed.

The C-8401 was designed primarily as a communication network processor. One of the distinctive features of the machine is the ability to control I/O operations from many sources at the same time. Although this is not unique in modern computers, it is facilitated to an unusual degree by the computer design

which incorporates the external exchange registers for this purpose. Input and output is specified by separate micro-programs selected by the RNI microprogram in the same manner that other microprograms are activated. The machine was designed with a single application in mind but is suitable for other applications by software modification. This conforms to the basic rationale of the stored logic principle.

2.8.6.1.3 Characteristics

To the general observation that programming may be undertaken on a lower level of abstraction on stored logic computers, using generally smaller logical elements, we shall add certain other characteristics of the stored logic implementations to date.

1) Multi-level programming - Interpretive operation is featured on each of the computers discussed. Although complete programs may be prepared on the machine code level, the machines are specifically designed to facilitate subroutinization.

2) Accessible Working Registers - The internal registers of the machine are available for minute manipulation involving transfers, temporary storage, addressing, as well as arithmetic computation and control.

3) Adaptive instruction sets - All claim the feasibility of custom made instruction sets to suit individual applications.

4) Relatively few clock pulses per computer instruction.

It is noted that there tends to be fewer clock pulses per machine instruction. Usually, however, the clock pulse contains several micro-operations and the compounding of useful functions is considered a design advantage. This doubling up of logical operations is seen in the fact that all three computers allow at least two command functions per computer word.

The PB-440 and the C-8401 have in common the utilization of fast control memory modules for the storage of the stored logic routines. It should be noted that the development of fast (control) memory modules for special purposes is not a unique stored logic feature. It is a common characteristic in recent entries in the computer field.

And, finally, these machines have the common characteristic of admitting to being stored logic computers. The implementation of microprogramming techniques is more widespread than the number of machines which admit to being stored logic would indicate. Stored logic is now claimed only by those manufacturers who are committed to it. No longer can much benefit be derived from claiming it as an innovation. If the term stored logic does not survive, it will probably be because of semantic difficulties and the current uncertainty among computer manufacturers as to whether the designation has positive or negative sales value. The term microprogramming is somewhat more acceptable currently and probably more descriptive.

The long heralded 360 series announcement alluded to the fact that the microprogramming technique is a part of the design philosophy. In this instance the lower end of the line qualifies as being microprogrammed. However, there is no suggestion that custom made instruction sets are anticipated. On the contrary, instruction compatibility and standardization is stressed. It is interesting to note that several other manufacturers have indicated willingness to conform to this new instruction repertoire and, in at least one case, the translation will be achieved with stored logic techniques.

2.8.6.1.4 Evaluation

The advantages and disadvantages of stored logic as a design principle are difficult to weigh. It could be argued that the stored logic design has not been the most compelling reason for success or

failure of those computers which have used it; nor even the most important feature. In any case, commercial success is not a valid indicator of design excellence since the two seem to correlate only casually.

The advantages are perhaps most often summed up in the word "flexibility"; flexibility in the sense that varieties of instructions may be produced--that there is a selection of programming methods--that the instruction repertoire may be changed by reading in a new set of microsteps. Whole "logical" computers may be designed to suit particular problem requirements; other computer repertoires may be simulated to retain software investments; and special instructions can be designed as needed and added to the growing library of routines.

Stored logic appears to offer certain cost savings to the manufacturer. The less complicated control logic, the lower number and types of components, together with the opportunities for standardization of component modules make it intrinsically an attractive design.

Another advantage which was cited by early writers is that the order code may be changed late in the development of a new machine. And, of course, the interpretive language can be modified even after it is built. This reflects the early concern regarding rapidly changing instruction repertoires. Thus, stored logic was seen as a way of delaying obsolescence. Currently, however, there is a tendency to perpetuate code structures, at least among families of computers; in order to maintain compatibility.

Although the interpretive operation is considered the primary programming method, the lower level machine code is sometimes preferred. This is occasionally necessary to exact maximum efficiency for critical computations. Sometimes, it is found necessary to code on that level for competitive reasons.

The interpretive overhead cost must also be weighed in terms of storage as well as execution time. For, in the case of stored logic computers, the (interpretive) instruction repertoire must be stored. In the case of the dual memory machines this storage is quite expensive. This argument may be turned around, however. The instruction repertoire saves storage in the sense that subroutines save storage. And the dual memory machines assuredly have a compelling reason for storing the instruction set in fast memory.

The primary objection to stored logic computers is that it is difficult to program them. It is felt that the logical complications that must be dealt with are enormous; that the programmer should not only have a thorough understanding of the subcommands, but should have a knowledge of the internal logic of the computer and even the circuitry involved. It is said that microprogramming is not intended for the casual user.

It is probable that the actual difficulty of programming stored logic computers is exaggerated. Although it takes a little longer to develop facility at the lower language level, programmers experienced in microprogramming are usually enthusiastic. They consider it challenging and sometimes it takes on the characteristic of an intellectual recreation. However, what is often overlooked among those who (modestly) insist its a "snap", is that, while it may not seem more difficult to them, it will very likely take considerably longer to write a string of code using microprogramming than it would with conventional code. The apparently greater latitude to compose elegant code even when machine efficiency results, can sometimes turn out to be a false economy in terms of work accomplished per unit cost.

However, it is argued that once the software is developed to provide the desired interpretive instruction repertoire, programming is as easy as for any other computer. The theory is that a small team of microprogrammers (perhaps one) may serve to prepare all special instructions that may be required, and will generate new repertoires as the need is seen. This is a perfectly valid point of view, and the capability to tailor-make an instruction set is certainly one of the most powerful arguments for microprogramming. Unfortunately, however, this kind of software has turned out to be extremely expensive. This is due not only to the cost of the programming effort but also to the concomitant costs of library maintenance, documentation and attendant activities associated with user's groups and software development generally.

It is usually found more expedient to use combinations of instructions already available than to develop new ones that are more efficient. Private instructions make the rounds unofficially (usually to avoid the bother of getting them accepted as a part of the library), and standard usages become difficult to maintain. The concept of private order codes for variable machines does present some procedural problems. Too much flexibility may be a disadvantage.

The consensus among those who are familiar with the cost trade-offs involved tends to suggest (reluctantly) that stored logic as practiced by the programmer is not paying its way. A partial solution is not to allow the applications programmer the discretion of instruction repertoire alteration. He is presented with a "logical" machine that is unalterable. This unfortunately tends to negate the basic advantage of microprogramming, i.e., flexibility. Another approach is to fix the stored logic (a contradiction in terms?) in the machine. At least one manufacturer is using this approach, and has, in effect, a plugboard type of stored logic modularity.

The stored logic design should be evaluated in the context of various other developments affecting its utility. One important consideration has been the changing size both logical and physical, of hardware components. Initially stored logic received considerable impetus from the fact that hardware replacement of large component modules was expensive and sometimes difficult. Use of smaller logical elements was found to be more economical. Lower component count, standardization of pluggable replacements, and savings in control logic; these factors were all felt to be especially compatible with the stored logic design.

A counter trend seems now in effect which suggests that larger and more complex logical components may be produced now at a fraction of earlier costs. This, together with the tendency towards miniaturization, may limit the degree of divisibility that is economical. As the cost of hardware components decreases, the motivation for small micro-logics may be expected to diminish. In this connection, it is noted that the ratio between hardware and software costs is changing. There is little evidence that the latter may be reduced in the same dramatic fashion as the former.

With the increasing cost of software, utilization of existing software inventories becomes very important. One approach to this problem is the development of translators to allow programs written in the language of one computer to be executable on another. Stored logic machines are very amenable to this type of implementation and, as the "host" computer, will not pay so severe an execution time penalty ordinarily as would one with a conventional design.

Perhaps in the larger view, it is not too significant if the stored logic concept is maintained as an entity (although the term microprogramming is almost certain to continue to be applied to whatever it seems convenient and appropriate). The advances associated with this development; language flexibility by sensitive manipulation of small logical elements, standardization of hardware components, dual or multiple memories to suit varying computational demands, and translations of language repertoires to utilize software inventories, are likely to be of an enduring nature in computer technology.

The concept has diverged in development and has been diluted in implementation. It has turned out to be a variation rather than a radical departure from conventional design. Investigation in this direction is incomplete, however, and the techniques involved are certainly worthy of continuing study in consideration of the larger topic of computer organization. Perhaps the development will go full circle with a new look at Wilkes control matrices.

2.8.6.2 Highly Parallel Computers

A new area in computer organization which represents an almost complete departure from conventional computer design is "highly parallel computers". In these computers the arithmetic and control logic is essentially decentralized to the extent that they exist at nodes of a network. All of the arithmetic and control units at the nodes then work in parallel to provide, in theory, a high speed operation. These computers are best represented by the Solomon computer developed at Westinghouse under contract with RADC.

There is an important question of whether these highly parallel computers have any place at all in future ANTACCS. This question will be examined.

2.8.7 Analog/Digital Hybrids

It is intended here to discuss briefly the subject of analog/digital hybrid computers. More specifically, the current uses and possible future uses in ANTACCS of these systems will be analyzed. Although this work will not be a thorough examination of this type of computer system it will nevertheless present useful information and some opinions about future ANTACCS uses.

2.8.8 Existing NTDS Computers

To best understand what the characteristics might be of future NTDS computers it is necessary to understand and develop a critique of existing NTDS computers. This will be done in this section of Technology.

The following computers will be discussed by the completion of the study effort: Q-20, Q-20B, 1218, AN/UYK-1, CP-667, MTDS and ATDS computers. Rather than a thorough and exhaustive presentation or summary of the characteristics of these computers, there will be a short critique stating the more and less desirable aspects of each of them.

2.8.8.1 Introduction

The current and widespread employment of the Q-20 computers by the Navy for many critical tasks makes them a vital component of the Navy's data processing capability. With this proportion of the Navy computing effort centered in Q-20 computers, and with the Q-20 compatibility being built into the CP 667, it is necessary for the ANTACCS study to investigate in some detail the capabilities and limitations of the Q-20A and Q-20B. The effort is approximately 50% completed at this time and a technical report will be published as the effort continues.

The requirement of the armed forces to meet the exigencies of modern warfare has led to the development of computers especially designed for military environments. These computers are the chief processing elements in systems designed to have very rapid response time and sufficient reliability for both defense and attack situations. The best-known computer in this class is the NTDS unit computer Q-20. All the military computers, in addition to having the obvious capability of being operational in severe physical environments, must have the additional qualities of high reliability, low maintenance requirements and complete engineering documentation.

To increase their capability for field employment, the NTDS computer (and the Army Fieldata computers) have adopted standard strobe philosophy for interfacing peripheral equipment. The Navy version is labeled the "NTDS Interface" and is included in all equipment that is intended for Navy employment. It is the signature of NTDS. The use of the NTDS Interface permits peripheral equipment to be added or removed from a computer system in the field by simply plugging or unplugging them.

These military characteristics, when combined with their general computer characteristics, have made these computers candidates for use in other military systems; and (in their commercial counterparts) candidates for use in some non-military applications.

The list of military computers with the above characteristics has become relatively large. The Army Fieldata program included IBM's IMPAC, Sylvania's MOBIDIC, Philco's BASICPAC and COMPAC, and RCA's MICROPAC (the FADAC computer used by the artillery was not a member of this family). Of these computers, only the MOBIDIC and BASICPAC were produced in significant numbers.

The Navy computers have been produced chiefly by UNIVAC, and include the military computers Q-17 ("Countess"), CP 642A/USQ-20(V), CP 642B/USQ-20(V), and the CP 667. In addition, two smaller computers have been built with "NTDS Interfaces": the TRW AN/UYK-1 and UNIVAC's model 1218.

The only computer having the official NTDS designation is the CP 642A/USQ-20(V) which is the unit computer of NTDS. UNIVAC model 1212 or CP 642B/USQ-20(V) is a current, up-dated version that is, from the standpoint of instructions, almost completely identical to the Q-20A. The CP 667 is a new computer that is equivalent to the Q-20B, in one mode, and is a new, more powerful computer in another mode. For the purpose of the evaluations to be published, the Q-20 will be used as a basis for comparison.

2.8.9 Requirements and Applications of Computers in the ANTACCS Environment

In this section the needs of ANTACCS with respect to computers will be discussed. Emphasis will be placed on the kinds of capability necessary, the locations of the computers and the organization of the shipboard equipments from a total systems point of view. Some of the topics to be considered are as follows: computer location, inter-computer communication, computer functions, computer system expansibility, and shipboard vulnerability.

2.8.10 Recommendations and Comments for ANTACCS Computers

One of the principal outputs of this section will be a description of a possible future family of NTDS computers. Items to be covered are memory, speed, organization, circuitry and packaging, and compatibility of these systems. This description will constitute additional input in arriving at the decision as to whether a totally new family of NTDS equipments should be developed or whether there should be a continual upgrading of present NTDS computers on a program-compatible basis.

As well as the description of a possible future NTDS family of computers and the motivations for such a family, there will be a discussion of possible other computer-like equipments which might find application in ANTACCS. This will include systems such as highly-parallel computers of the Solomon type, analog/digital hybrid, and digital modules.

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2.9 PROGRAMMING

Much work remains to be done in the programming area, however, an outline has been developed, and a comparison of the effectiveness of compilers for the ANTACCS application has been undertaken. The following is an outline of the document which is being prepared.

2.9.1 Classification of Programming

The meaning of the phrases computer program, computer programmer and computer programming is slowly changing. This section will present a definition of the words and list the factors causing the changes.

2.9.1.1 Definition

A historical definition of computer programs, computer programmer, and computer programming.

2.9.1.2 Factors

Factors causing a change in what constitutes a program, how a program is generated, and who generates it.

2.9.1.2.1 Hardware

A discussion of the programming implications of the development of inexpensive mass memories and display devices, the extensive use of communications media, the effect of novel organizations of computer hardware.

2.9.1.2.2 Systems

Developments in both ANTACCS oriented and non-ANTACCS oriented computer systems - a discussion of the implications of the development of communication-based data processing, information retrieval, process control, management systems.

2.9.1.2.3 Education

A discussion of the changes in education, training and function of programmers.

2.9.2 Sources of Information

2.9.2.1 People and Companies

A visit will be made to NEL to get a fix on their procedures.

2.9.2.2 Literature

There are many treatises on computer applications and program results, but relatively few on programming itself. References will be listed.

2.9.3 Programming Characteristics for ANTACCS

In this section are defined programming techniques and concepts which have an application to ANTACCS, together with their application. The subjects covered will be those named in section 2.9.5

2.9.4 Status

A definition of the state-of-the-art for the techniques of program generation, program checkout, program maintenance, and the integration of programs into systems.

2.9.4.1 Programming Tools - Off-Line Systems

2.9.4.1.1 Assemblers and Compilers

An evaluation, description, and/or comparison of assemblers and compilers and their application to ANTACCS, namely,

1) Assemblers
2) ALGOL
3) COBOL
4) FORTRAN
5) CS-1

6) NELIAC
7) JOVIAL
8) TABSOL

2.9.4.1.2 Systems Packages - Off-Line Executives

A description of the functions, usage, and application for the ANTACCS of:

1) Monitors
2) Data and Report Generators
3) Diagnostics
4) Debugging Packages
5) Simulations

2.9.4.2 Executive Programs - On-Line Systems

A comparison of the capabilities of the executive programs of the following systems:

1) SAGE STC
2) NTDS D-825
3) MAC
4) SABRE

in terms of:

2.9.4.2.1 Executive Programs

The programs required to coordinate the events which must be processed by the system.

2.9.4.2.2 Time Sharing - (The Executive Only)

A comparison of the techniques of achieving a more optimum utilization of the computing modules. To be included are discussions of control by:

1) Highly parallel computers
2) Multiprocessing
3) Multiprogramming

2.9.4.2.3 Intersystem Control and Communication Programs

A comparison of the system components which control the operation of and flow of data through a system. To be included are a discussion of the requirements and techniques for:

1) Scheduling
2) Buffering
3) Switching
4) Intermodule communication

2.9.4.2.4 Reliability, Malfunction, and System Readiness

A comparison of the programs and programming techniques which can influence system reliability, system malfunction detection and correction, and the determination of system status. Included will be discussions of:

1) Component Diagnostics
2) Component Utilization in Programs
3) FIX
4) Graceful Degradation
5) System Readiness

2.9.4.3 System Performance

A comparison of the ways in which systems which include programmed computers can be used to provide performance data during operation.

2.9.4.4 Program Documentation

2.9.4.4.1 Types of Program Documentation

A description of the various ways in which programs have been documented in the past. The description will cover for each type of documentation, the format, the content, the relationship to other tasks, the timing, and the distribution. The classifications are defined to be:

1) Task description - the types of documentation which relate programs to systems.

2) Function descriptions - the types of documentation which relate programs to system functions.

3) Flow Charts - the types of documentation which relate programs to hardware.

4) Comments - the ways in which documentation has been made an integral part of program preparation.

2.9.4.4.2 Uses of Program Documentation

A description by type of documentation of their use in the various phases of system implementation. To be included is a discussion of the requirements for documentation and the purposes the types of documentation were meant to serve, served, or could serve. The classifications to be used are:

1) System Design
2) System Installation and Checkout
3) System Operation and Maintenance
4) System Modification or Improvement

2.9.4.4.3 Techniques of Program Documentation

A description of some machine processes, aside from compilation and assembly, which may be used to produce program documentation explicitly or implicitly. To be covered are:

1) Simulation
2) Documentation Retrieval
3) Flow Charting by Computer

2.9.5 Programming Availability in the 1970-1980 Period

The section will include a prediction by subject of 2.9.4 of status in the 1970-1980 period. In addition, it will include a discussion of some techniques, trends, and concepts which will become important

to the programmer:

1) Logical languages - the development of pseudolanguages based on symbolic logic and language analysis.

2) Procedural languages - the development of Algol-like languages.

3) Non-Procedural languages - the TABSOL-like languages.

4) Implicit programming - techniques which replace the programming function.

5) List Processing - techniques for information distillation and manipulation.

6) Man-machine symbiosis - techniques of integrating procedures and processes.

7) System Analysis - the integration of programming and the disiplines associated with system implementation.

2.9.6 Limitations of Present and Planned Programming

A documentation of the differences between the anticipated status of programming in the 1970-1980 period and the status of programming now.

2.9.7 Recommended Developments to Meet ANTACCS Needs

A documentation of procedures for eliminating the deficiencies found in 2.9.6.

2.9.8 Evaluation Criteria Recommended

2.9.8.1 Program Development

A discussion of the techniques which have been used to control the scheduling, cost, required effort, and quality of programming for large systems. To be included are a discussion of:

1) The Milestone System
2) PERT
3) Approaches to Cost Analysis
4) Methods of Obtaining Execution Efficiency

2.9.8.2 Program Design

A discussion of ways in which programs are designed and of the factors which have an influence on their design. To be included is a discussion of the factors which preclude optimum design. The following subjects are to be discussed.

1) System Analysis
2) Program and System Documentation
3) Computer Languages
4) Subroutines and Segmentation
5) Macro and Micro Program Development
6) Program Packages

2.9.9 Conclusions and Recommendations

This section will be completed after a thorough analysis of ANTACCS programming operations.

3. METHODOLOGY

3.1 INTRODUCTION

This section of the mid-term report presents the material developed thus far in the Methodology part of the study. The material presented is preliminary in that it will be supplemented and amplified as appropriate during the balance of the study. As in all technical studies, final documentation lags somewhat behind the completion of the work. One must also consider that although this is mid-point in the study calendar, one half of the hours budgeted for Methodology have not yet been applied. For these two reasons, the following material is less than half of that ultimately to be provided by Methodology.

This section of the mid-term report is organized into three sub-sections:

1) General Methodology

2) Implementation Methodology

3) Specific Methodology

Bibliographical material is included in a common bibliography section at the end of the report.

In general, the work in Methodology is abreast or ahead of schedule.

3.2 GENERAL METHODOLOGY

3.2.1 General

This area of the study is concerned with the investigation of a few of the most important tools available for Naval Systems Planners. These tools are called "General" since they are not directed toward the solution of specific problems. Rather, they are tools which may be used in any phase of system planning, and are in that sense "general" methods. The effort, according to plan, is divided among four areas:

1) Simulation Languages
2) Techniques of Simulation
3) Mathematical Modeling
4) Critique of General Methodology

In this report, material is presented from areas 1 and 2.

3.2.2 Simulation Languages

3.2.2.1 Introduction

Simulation languages are those higher order programming languages which are especially designed to facilitate the programming, coding and checkout of digital computer simulations.

Simulation languages (or sim languages) allow the simulator to proceed at a greater speed in the design and construction of a simulation since they provide for the creation of routine procedures control, and the recording of data. Most sim languages were created for a specific purpose and have since been expanded to treat a larger class of problems.

Simulations and models have been coded for digital computers from the very beginning of the computer era.

The earliest of these simulations were coded using octal and even binary absolute techniques, and fine simulations may still be produced using machine language or combinations of machine language and Fortran, or Algol. The use of a simulation language is in no sense required for the

production of a good simulation program. However, the use of a proper sim language facilitates the production of the sim program and makes the designer's task an easier one, as well as improving the speed of his progress.

3.2.2.2 How Sim Languages Work

The construction of simulations involves the creation of lists of things, people or events. These lists present one person (thing or event) at a time to be served or operated upon by the logic of one of the central models of the simulation.

Consider, for instance, an application of simulation of supermarket operations. People waiting in line to pay at a supermarket would be in a list, the head of the list to be served next by the simulation's model of what the cash register operator does. The lists and operations may be cascaded to show how the customer must wait at the meat counter, and in the parking lot, or how he is served in succession by the cash register operator and then the bag boy.

In some simulations, the lists may be few and very long. In others, many short lists or mixtures of long and short lists are required.

In each simulation, there is at least one operation which serves the items waiting in the lists. In complex simulations it is often necessary to model many operations which are used to serve lists and in turn add the just-served items to one or more other lists which will, in their turn, be served.

The construction of these complicated models is simplified by the use of sim languages since they provide conventions (or regularized shorthand) for specifying the creation of lists, the operation of the serving models, the inter-dependencies of serving models, the influence of time or other environmental circumstances (such as tide), etc., Each one of the various sim languages uses different conventions and they vary in their simplicity, power, and general applicability. This is due primarily to the fact that

they were all created for specific purposes. Most of them have been expanded in scope since their inception, but the prospective user of sim languages stands to benefit if he picks a language which was originally designed for a problem similar to the one he currently faces.

The advantage of using a sim language tailored for an application similar to the one at hand must be weighed against the difficulties of learning a new sim language or having a computer available for which the language was written. But in general, one should stay as close to the original area as possible to avoid encountering too many of the inherent limitations which are present in all sim languages. The more complex and complete languages may be used to simulate simple relationships and occurrances, but they are often much too ponderous for such use.

The use of a sim language is a multi-step operation and will be explained here simply:

1) Develop the rules for processing the lists. These may be mathematical models or stochastic models (models based upon probabilities) or combinations of these.

2) Develop the rules for the creation of the lists and for items entering and leaving the lists other than by being served by the primary models.

3) Develop the relationships and linkages which relate the lists and models to each other.

4) Develop the timing and operational considerations for the execution of the simulation.

The user now begins to write the simulation using the conventions of the language chosen. When this step is completed, the computer and the simulation assembly program process the sim conventions. The output of this step is a program (or deck) in computer language. This deck may be in machine code such as FAP, but more often the result of the first pass is a compiler language such as Fortran. This, in turn, must be compiled into

machine code and then converted into the binary deck which is finally operated. This operation is the simulation being cycled. The answers and statistical data are recorded and printed out during and following this third pass.

Some sim languages permit the use of machine code and compiler or assembly language in the original writing of the simulation. This process is called "enrichment" and enhances the basic capability of the sim language. Enrichment permits the simulation designer to code certain intricate portions of his simulation in machine or assembly language and bypass various shortcomings of the sim language. Since all possible simulation requirements cannot be provided for in a sim language, enrichment capability is a highly desirable characteristic, although one good language (GPSS) does not posess it.

The easier the sim language is to learn and use, the more stylized it tends to be and the more limited it tends to be in terms of the flexibility of what it can describe. The more capable a sim language is, the more complex its rules are and the more difficult it is to use properly.

3.2.2.3 Some Simulation Languages

This section discusses several of the better known sim languages as well as three which are of considerable interest to simulators at the present time. This material will be added to substantially during the next portion of the study. Only a brief glimpse is provided of the languages, but it should serve to show the primary capability and application of each.

1) GPSS II

This program is an IBM product and an outgrowth of the "Gordon Simulator" which first appeared as an AIEE conference paper in August 1960. GPSS I followed and the current GPSS II is an enhanced and more flexible version of its model I

Predecessor. GPSS is designed to handle simulations of communications systems and computer systems, where there may be many lists of varying lengths, but where the central model(s) of the simulation are relatively simple logically. All of the relationships and types of operations are rigidly specified, and GPSS cannot be enriched with any assembly or machine code. GPSS II is available for the IBM 7090-7094.

2) GASP

GASP was developed by the U.S. Steel Corporation to simulate the operations in various shops of steel mills. In these simulations, the lists may be somewhat shorter than with communications simulations. At the same time, the models of the simulation can be very complicated. GASP is one of the earliest of the powerful, flexible sim languages. GASP permits the use of Fortran for enrichment and is compatible with Fortran diagnostic tools. It is available for the IBM 1620, 7070-7074, 7090-7094, and CDC G-20.

3) CLP

The Cornell List Processor, or CLP, was developed by the Industrial Engineering Department of Cornell University. Its purpose was to provide engineering students with a general purpose simulation language that could be learned and used well in one semester. CLP is simple in its syntactic construction and, therefore, easy to learn. It is not completely stylized and so, has fair flexibility. CLP may be enriched by employing CORC statements. (CORC is a compiler language written by Cornell with an eye toward ease of use). CLP combines simplicity with flexibility and enrichment. It is availably only for the CDC 1604.

4) DYNAMO

DYNAMO is a capable sim language but one designed expressly for the construction of simulations employing differential equation models. It was developed at the Massachusetts Institute of Technology for the IBM 7090-7094. It is an interesting and valuable engineering tool but one which has rather limited scope of application.

5) CSL

Control and Simulation Language (CSL) was developed by IBM (UK) in conjunction with Esso (UK) for the purpose of simulating corporate operational problems of large scope. These are problems such as the operation of a port-tank form--refinery complex receiving crude oil by tanker and shipping output by rail, truck and barge. The real capability of CSL lies not in the creation of long lists, but in the ability to create and manipulate many complex operational models and to cascade these models in tremendously complex ways.

As might be expected, CSL has a difficult syntax and many formidable construction rules. It may be enriched with Fortran. It is a "three-pass" language which would ordinarily be of little concern. For CSL, however, the first pass is made on the IBM 1401 (U.K. Model) and the last two passes on the IBM 7090-7094. It is not now available in the U.S. nor outside of IBM (U.K.), but it is supposed to be available generally in Britain in late 1964.

6) SIMPAC

SIMPAC was developed by the System Development Corporation as a research tool and is one of the more powerful of the simulation languages. Almost by definition, this makes it one of the most difficult to learn. SIMPAC is run on a 7090-7094, and while other sim languages for the 7090-7094 operate under Fortran control, SIMPAC normally uses SOS control and this requires 14

tape drives. SIMPAC could be run on a large Fortran 7090 but it would be cumbersome to do so. SIMPAC can be enriched, but not with compiler language. Its only enrichment is with a machine mnemonic code (SCAT).

Many of these limitations are of little importance to the skilled programmer with a very large 7090-7094 installation at his disposal. Still, they represent substantial barriers to many potential users.

7) SIMSCRIPT

SIMSCRIPT was developed at Rand to provide more efficient preparation of simulations being used in various Rand projects. It operates on an IBM 7090-7094 under Fortran control. It may be enriched by Fortran statements and by code written in FAP (a Fortran compatible mnemonic machine code). This FAP enrichment feature gives it great capability, at the same time allowing for enrichment by the easier-to-use Fortran.

SIMSCRIPT is complex in its syntax and rules, and is difficult to learn and use well. Some of this is compensated for by its excellent documentation which includes a pamphlet on how to cheat the sim language grammar rules to provide even more capability.

SIMSCRIPT is the most popularly used of the powerful simulation languages and will probably remain so for some time to come.

8) MILITRAN

MILITRAN is a military simulation language developed under contract to the Office of Naval Research by Systems Research Group, Incorporated. It is designed to run on the IBM 7090-7094, and is primarily designed for the simulation of military operations,

rather than the simulation of system operations. The first available comprehensive technical output of the MILITRAN Project arrived during the preparation of this report and could not be reviewed in time for inclusion. It will be covered in a later report.

3.2.2.4 The Application of Simulation Languages

The simulation programs which sim languages prepare are not quite as efficiently coded as those a very skilled programmer could write, but they are available in a small portion of the time that programmer would require. In simulation programming, as in other programming, understanding the problem and deciding what to do take impressive amounts of time. But, once that is done, simulations may be prepared much more easily , accurately and speedily using a sim language.

The system engineer has two major uses for a sim language. In the process of design, he often wants to check the performance of portions of the system or simple sets of interactions. For this purpose he wants a quickly used, simple sim language. For this purpose CPL would be ideal, but it is not generally used, although it could probably be made available. He must use GPSS II or something more complex than he needs like GASP or SIMSCRIPT. With these limitations, most system engineers do not simulate quick and dirty problems as they would be more prone to do if CLP or a similar simple language were available.

The second simulation requirement of the system engineer is the one of simulating large portions of the system and finally the entire system. This type of simulation is normally not prepared on a short term basis and the more powerful languages SIMPAC or SIMSCRIPT can appropriately be used. CSL, when it becomes available, will be highly desirable for these large scale simulations.

3.2.2.5 Current Developments

More than one computer manufacturer is known to be or reported to be preparing simulation languages. These seem to be at the most powerful end of the capability spectrum. SOL has been developed by a group of system engineers at Burroughs, Pasadena. It runs on the B-5000 and is extremely powerful, reportedly as capable as SIMSCRIPT or SIMPAC. In addition, SOL may be enriched with ALGOL statements, and runs under B-5000 ALGOL control. It is also constructed in a completely different manner from the balance of the sim languages. It is "syntax oriented" which means that the compiler and its conventions more closely parallel our natural language in operation and, therefore, the grammar and construction are much easier to learn to use.

SOL was not mentioned in the previous section since it must be released to the public through Burroughs, Detroit, and at last report they seem to have little interest in doing so.

There are no reports of smaller scale languages in development.

3.2.2.6 Comment

This leaves the language spectrum available to the system engineer looking like this:

GPSS II CLP GASP SIMPAC SIMSCRIPT CSL SOL

with DYNAMO and MILITRAN each off in its own specialized but useful dimension. GPSS II is capable but completely unchangable since it cannot be enriched. CLP could probably be made available by private treaty, but it is not well known and only runs on the 1604. GASP is old, but capable and runs on several machines including the G-20. SIMPAC has great power but severe limitations. CSL is not available yet, and SOL may never be.

The choice is really GPSS II, GASP or SIMSCRIPT and with these three languages, the simulation requirements of all phases of system engineering may be met satisfactorily. But special applications make CLP, SOL and CSL continue to look very promising to those who follow simulation closely.

3.2.3 Techniques of Simulation

Several papers concerning various aspects of simulation have been planned. They are:

1) Simulation and Modeling Techniques for System Design.

2) Simulation for Command Control System Checkout.

3) Simulation for Training Purposes.

4) Simulation for Command Control System Development.

5) Simulation: A General Discussion and Survey.

6) The Role of Simulation in Test and Evaluation of Navy Command Control Systems at Point Mugu.

7) Simulation in Real-Time for the Line Commander.

8) Design of Simulations of Real-Time Systems.

9) Mathematical and Physical Modeling Techniques.

Of this series, 1, 2, 4, and 6 are included in this report. The balance of the material will be presented in subsequent reports.

3.2.3.1 Simulation and Modeling Techniques for System Design.

3.2.3.1.1 Introductory

Why does a system designer use simulation techniques? "Simulation" and "modeling" imply imitation while "design" implies creation. Actually, the system designer does not simulate and model for the purpose of creating system designs but for the purpose of testing system designs. The system designer can test and examine the early forms of his design with simple diagrams and hand calculations. His intuition and experience tell him that one equipment configuration is more functional than another. However, as the design becomes more advanced, he finds it increasingly difficult to evaluate the design trade-offs. Finally, the design is too

complex. He can no longer visualize the dynamics and interrelationships of the myriad of components in his creation.

How can he be sure his design will perform as he hopes or expects when it is subjected to the stresses which the real world will impose? One method would be to build a prototype system and subject it to a simulated real-world environment. There are obvious reasons why this is an unrealistic approach, especially for military command and control systems:

1) Simulated environments, such as military maneuvers, are expensive in terms of time, manpower, and money.

2) It is difficult to reproduce real-world environments for repetitive tests of system prototypes.

3) System prototypes are expensive and may require years of development.

Computer simulation is a relatively fast and inexpensive alternative method of testing system designs. Simulation, however, is limited by the ability of the simulation designer in creating an accurate model of the system components and their interaction. The system components may be computer programs, human controllers, information channels, sensors, weapon systems, etc. Each component and its dynamic relationship with the other system components must be represented accurately to achieve a valid system simulation.

Here lies the "fly in the ointment." The fly is the human component. The actions of human components are relatively unpredictable, especially when they involve evaluation and decision processes.

There are two general classifications of system simulations: Man-machine simulation and all-computer simulation. The following sections will discuss the application of these two types of simulation to the design of command and control systems.

3.2.3.1.2 Man-Machine Simulation

This section discusses operations simulation. Operations simulation is used to simulate the operation of a command and control system at the interface between management personnel and display devices. Figure 3-1 illustrates a command and control environment and the man-machine interface which is simulated with an operations simulation.

An operations simulation presents simulated information to management personnel and modifies the information appropriately depending on their response to the information. In other words, an operations simulation consists of:

1) Management personnel

2) Communication equipment, and

3) Information exchange

The method of controlling the information exchange between the management personnel and the communication equipment depends on the information rate and quantity. If only a small amount of information is communicated, the information exchange might be implemented manually with switches and/or grease pencil displays. However, since the information rates and quantities are high for command and control systems, operations simulations generally employ computers to control the information exchange. The computer is also used to simulate other components of the command and control environment, i.e., sensing devices, controlling devices and the external world activities.

Figure 3-2 illustrates an air-traffic-control (ATC) simulation which is an excellent example of an operations simulation. The computer is used to simulate a portion of the external world activity (the movement of the aircraft) and part of the command and control system (the radar tracking inputs). [1]

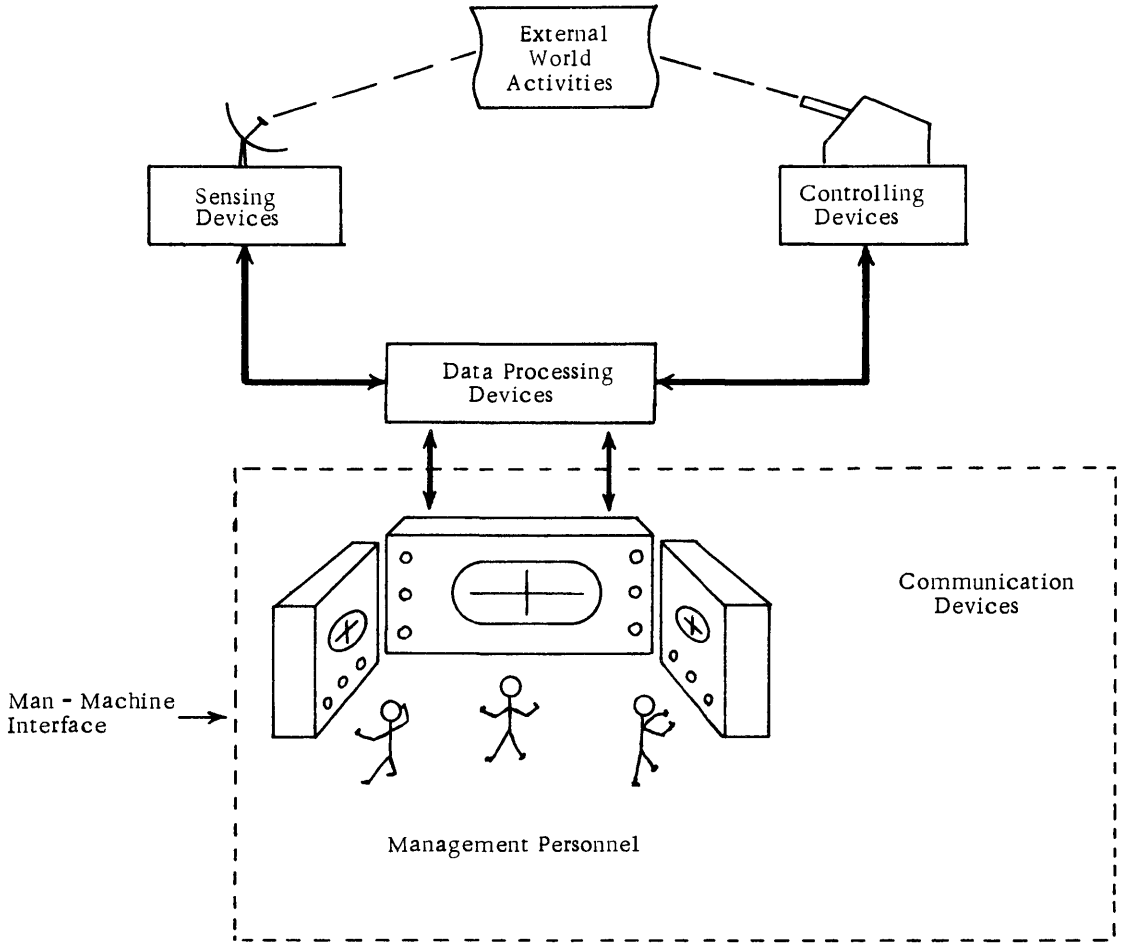

Figure 3-1.

COMMAND AND CONTROL ENVIRONMENT

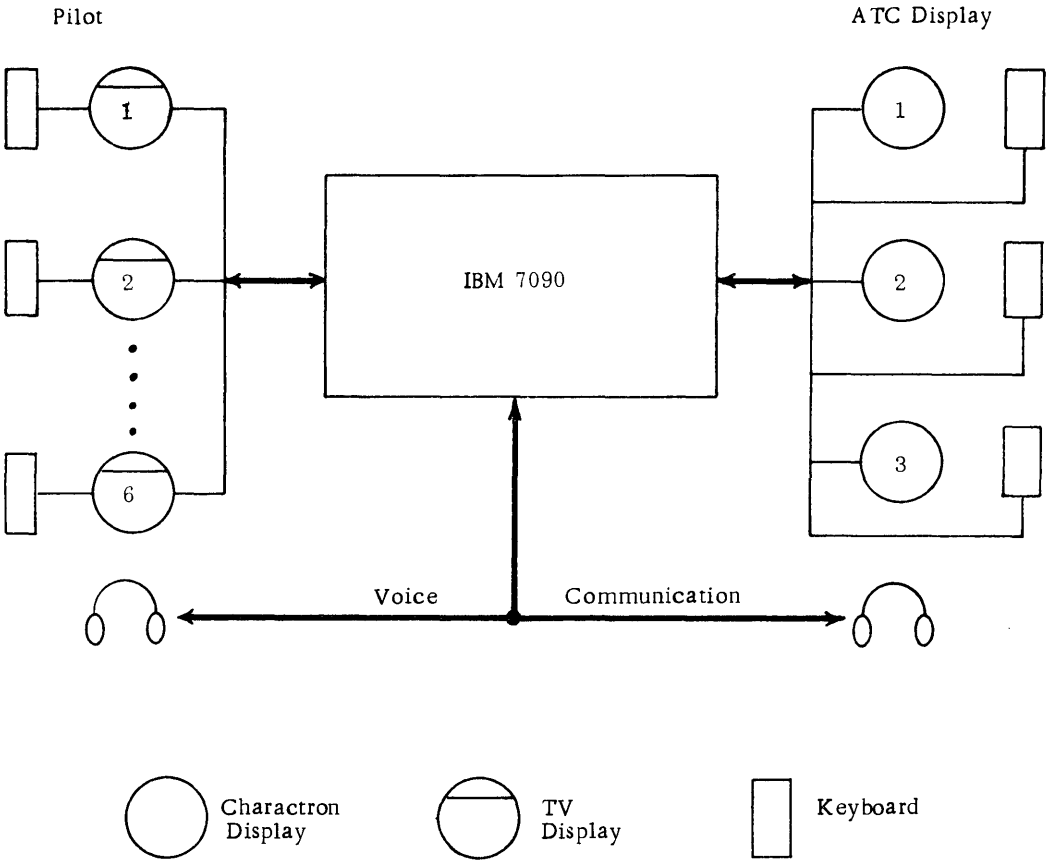

Figure 3-2.

FUNCTIONAL DIAGRAM OF AIR-TRAFFIC-CONTROL SIMULATION

Ultimately, the objectives of system designers are to increase the effectiveness and functionality of the system design and at the same time, reduce the time and cost of implementation. Operations simulation is a tool which can be used by system designers in achieving these objectives. However, these objectives are too general to be used in planning specific simulation runs. Each simulation run or series of runs is designed to produce data which will be used to form specific conclusions about the system design.

The system design is mutually determined between the system users and the system designers. The design is arrived at by using past

experience, imagination, projection, intuition, etc. However, many system parameters are difficult to evaluate: the type of information displayed, the frequency of information updating, the number of operators required, the performance of the operators under peak loading, the reaction time of the operators, the types of operator errors, the consequences of operator errors, unnecessary control options, necessary automatic modes of operation, etc. These parameters affect the system design considerably. They affect the quantity of communication links, the size of computer memory, the speed of the selected computer, the computer software, etc.

The model of the system may contain hundreds of parameters which must be examined. Sometimes it may be necessary to examine only one parameter with a series of simulation runs. For instance, the effect of aggregate or lumped radar returns during peak loading on the commander's actions could be tested with a series of simulation runs.

Operations simulations have been used to determine these types of parameters at the System Development Corporation. The following paragraph is an excerpt which describes the results of an operations simulation of a Manual Air Defense Master Direction Center.

"By means of the bioscopic simulation technique described, it was possible (1) to obtain measures of the rate of information processing throughout the system, the number and kind of errors which were made, and a measure of the performance variability of all the operators; (2) to obtain a clear picture of the job requirements at each of the positions throughout the entire complex in terms of the information requirements of the position;(3) to observe performance degradation under various conditions of stress; (4) to determine how centralized supervision from the MDC could be effectively maintained and how restricted communication lines should be used to maximize information flow; and (5) to provide an overall estimate of system efficiency in terms of the primary operational

mission of the MDC complex - namely, how much threat warning time could be expected under various kinds of stress conditions, both in peace and war situations." [2]

Sometimes a system design contains latent parameters as requirements which are illuminated during an operations simulation. In a sense, the simulation is used as a stimulus for ideas which will improve the system design. This point is expressed in Item (2) of the preceding citation.

Hopefully, operations simulation will provide feedback to the system designers for the improvement of the system design. This will reduce the time and cost of implementation by reducing the modifications to the production model of the system. This point is well illustrated by the cost of computer software changes compared to the original software in the SAGE System. In the opening address of the 1963 Fall Joint Computer Conference, it was stated by Major General Terhune that the cost of each computer instruction for the original SAGE software was approximately $32, and the cost of each computer instruction for modifications to the original software was estimated between $100 and $1,000.

It is concluded that an operations simulation should not be implemented unless a definite need is identified. In addition, a simulation technique should be developed which will satisfy that need. After the simulation is implemented, each simulation run should be planned to yield results which can be used to form specific conclusions.

"The most common pitfall in simulation is the failure to anticipate how simulation results will be used. Simulations can produce literally mountains of data. Selection from these data, reduction into summaries, and analyses of significance must be anticipated and, in fact, preplanned. Perfectly good simulations have been known to fail for lack of this planning." [3]

This section describes the simulation laboratory and equipment which is necessary to conduct operations simulation. The simulation laboratory is the enclosure which houses the equipment and personnel. The equipment consists of computer hardware, computer software and communication devices.

1) Simulation Laboratory

The laboratory consists of many rooms, depending on the amount of hardware required to support the simulation and the type of environment which must be simulated. If a decentralized command and control system must be simulated, a room or compartment may be required for each group of management personnel. The Command Research Laboratory at SDC has a modular construction so it can be easily partitioned into various sized compartments. The ceiling of the laboratory is constructed of interchangeable squares which contain lighting, power and communication outlets.

SDC is also conducting several man-machine simulation studies in the System Simulation Research Laboratory. Each study is supported by the adjacent computing facility which is used primarily for general data processing functions, with occasionally scheduled simulation runs.

In addition to the data collected by the computing facility during simulations, a large amount of information is gathered by observation. The observers are separated from the participants by one-way glass. Each study has an observation area where the simulation controllers can study the simulation participants. The Systems Logistics Laboratory at the Rand Corp. consists of a similar arrangement.

Simulation laboratories should be built adjacent to existing computing facilities to take advantage of their data-processing

support. This can reduce the equipment costs, which are high in man-machine simulation, by making efficient use of computer time.

The laboratories should have a modular construction which can be easily modified to suit varied group configurations. This type of construction is expensive, however, and may not be warranted if an extended simulation activity is not foreseen.

One of the fringe benefits of an operations simulation is its system checkout capability. If the laboratory is large enough, actual system hardware can be incorporated into the simulation as it is developed. The actual system computer can be used in the simulation when ready and the general computing facility could be relegated to furnishing system inputs.

"In support of its design and development responsibilities in the Strategic Air Command Control System (SACCS) project, SDC established a Simulation Facility (SIMFAC) in Paramus, New Jersey. The SIMFAC is a physical model of the SAC Underground Command Post complete with Command/Control personnel stations, capabilities to produce simulated SACCS hardware printouts and wall displays. There is a soundproof observation deck in which SIMFAC personnel perform actions necessary to simulate all external occurrences starting from an Intelligence buildup to changes in threat responses. It is in this manner that many of the operational design concepts for Command/Control function have been derived and validated." [3]

2) Computer Hardware

Large general purpose digutal computers are generally used to control operations simulations because:

a) They have software which facilitates the development and modification of complex simulation programs.

b) They have speed and capacity for processing the simulation tasks in real-time, and

c) Many organizations already use a large general purpose digital computer for their data processing work.

The Systems Simulation Research Laboratory at SDC uses a Philco 2010 to control several man-machine simulations. The computer is normally used for general data processing tasks with an occasionally scheduled simulation support function. The computer can also operate in a pseudo multi-programming mode in which a data processing program can be interrupted and saved for later completion while a simulation program is executed.

An air-traffic-control simulation used an IBM 7090 which was equipped with interrupt features, a real-time clock and special interface equipment .

"Based on early experience it was decided that a large high-speed digital computer would be required to properly conduct these simulation experiments. At that time the IBM 709 was installed at the National Aviation Facilities Experimental Center and was, therefore, recommended for use with this Computer Driven Simulation Environment (CDSE). Subsequently, the IBM 709 was replaced by an IBM 7090. The 7090 computer was equipped with two data channels, a Direct Data Connection, and a real-time digital clock. The simultaneous read-write-compute feature of this computer made possible the transfer of large blocks of data without excessively increasing program

execution times. The Direct Data Connection provided high-speed data transfer to the Display Buffer system and from the Keyboard Data Entry System." [1]

The computer was used to simulate terminal air traffic in this simulation which illustrates one of the advantages of using a digital computer, i.e., the capability of easily simulating other system or real-world components.

"A digital computer can be used to generate these targets within this framework of requirements. It permits the inclusion of controlled navigation and speed error distributions so the effect of errors on the simulated system can be studied. The versatility of digital computer generated targets also allows additional functions to be programmed in the aircraft simulation that were unavailable in previous analog simulation equipment, e.g., the ability to realistically navigate the aircraft using the instrument landing system (ILS), or realistic simulation of take-off acceleration, etc."

"Simulation of Sub-Systems. A digital computer can be used to simulate a large variety of complex sub-systems that might occur in present or future air traffic control systems. Simulation of these sub-systems avoids the necessity of developing these often complex equipment until their value has been reasonably well determined. Some examples of these sub-systems might be the radar or other form of position acquisition system, the radar or beacon tracking system, or a beacon attitude receiving and display system." [1]

In the last five or six years, computer speeds have increased to the point where they can be used much more extensively for real-time operations simulation. The most effective type of

computer is a large scale general purpose digital machine with interrupt features, real-time clock and standard display interface equipment.

Multi-programming techniques can be used to reduce the cost of operations simulation by using computer time more efficiently. Cost can also be reduced by making use of an already existing computing facility.

3) Computer Software

To date, there are no software packages specifically tailored for the implementation of real-time man-machine simulation programs. This is probably due to the limited use or novelty of the technology. There are compiler languages which can be used for real-time programming, but generally real-time programs are seldom coded in a compiler language because the generated code is not efficient and real-time compiler languages are not available for most computers. However, if computer time is not an issue, some efficiency could be sacrificed for the advantages of a compiler language.

The computer software required to support a large simulation effort will be an expensive investment. It will be modified more than any of the other equipment which make up the total facilities. A real-time simulation programming system should be established before any simulations are attempted. The programming system will aid in the planning and coordination of the simulation development. It will also facilitate program modifications and documentation by establishing standard procedures. In addition, new personnel will become familiar with a well-organized and documented system with the least effort.

Once a flexible programming framework is established, the development of the many programming segments which compose the simulation can begin. Some of the program segments will contain actual system software logic, the other program segments will be simulations of real-world elements.

The actual system software logic will undergo an evolution as the system requirements solidify through use of the operations simulation. The outgrowth of the evolution will be a set of program specifications which fit the needs of the final system with a minimum of modification. In a sense, the computer program specifications are written before the hardware is selected. These specifications will be helpful in selecting proper computer and auxiliary memory units.

The simulated environment software will provide substitutes for the real-world elements which are absent in the simulation. The software will be the implementation of mathematical (including logical) models which represent radar inputs, weapon effectiveness, threat dynamics, system errors, etc. The speed of the computer must be adequate enough to process the actual system software logic and the real-world models in real-time. Consequently, time is the limiting factor when designing the mathematical models. For example, it may be necessary to compute radar detection on a probability basis using a stochastic process rather than modeling the radar search pattern and testing to determine when the radar beam intercepts an aircraft.

4) Communication Devices

Communication devices consist of displays and consoles required for communication between the computer and the

management personnel. The equipment depends on the type of information which must be communicated. Cathode ray tubes, TV tubes, slide projectors, keyboards, buttons and switches are commonly used devices. The Systems Simulation Research Laboratory at SDC uses all these equipments in their man-machine simulation studies. Manual display devices, such as weather status and equipment status boards, are economical displays which are frequently used in the early stages of operations simulation.

"The displays chosen were of the Charactron type (19" diameter) and had ability to display alphabetic and numeric information (fixed character size), special symbols (for aircrafts, fixes, etc.) as well as lines. Since the display format was under program control, flexibility existed for simulation on these displays for any desired situation. Initially, there were four displays connected to the computer through the Display Buffer system. Three of these are presently used for air traffic controller consoles and one provides data for the simulator pilots by means of a closed circuit TV system. Four high resolution cameras transmit the data from the Charactron to six simulator pilots' TV monitor displays."

"A set of input keyboards are required to allow controllers and pilots to communicate with the computer. Six keyboards are used for simulator-pilot input functions and three for the air traffic controller positions." [1]

General purpose display equipment should be used for operations simulation during the design phase of system development. This will enable the equipment to be reconfigured in order to test a variety of operating modes and display configurations.

"Previous experience has shown that buffered general purpose displays are needed for controller and pilot situation displays. These units should also be capable of displaying tables and other alphanumeric information to the controller. By building the simulation around a general purpose digital computer the flexibility of a programmed display system with no "built in" format restriction can be readily obtained." [1]

After firm communication requirements have been determined, more elaborate consoles and displays may be constructed in order to refine the system design.

5) Additional Hardware Equipment

Additional equipment may be warranted to achieve more realism. It might be necessary to make models or photographs of terrain which are scanned by closed circuit TV cameras to realistically display military developments.

The computer which is used for the simulation must process the actual system software and also simulation models. If the system software becomes elaborate, the computer may not be able to compute both in real-time. In this case, it may be necessary to use another computer to process the simulation models. This computer could supply all the inputs to and receive all the outputs from the computer which executes the system software logic.

Hybrid simulation techniques can also be used to relieve the digital computer of burdensome equation solving. An analog computer might be employed to simulate an entire air battle involving many interceptors and threats.

Imagination is the only limit to the degree in which realism may be achieved in operations simulation. Some man-machine simulations no doubt employ sound effects to increase the realism of the simulation.

Operations simulations are conducted using a "gaming" approach. A threat model is designed which will present a situation to the management personnel through their communication devices. The simulation will respond to the actions of the management personnel by displaying to them the consequences of their actions. The goal of the management personnel is to "defeat" the threat model.

An extension of this technique induces a note of competition into the simulation by using two teams:

A "red" team which is completely familiar with the system and simulation, and "blue" team which is composed of system designers and system operators.

The red team designs threat models and tactics which it feels can best challenge the system. The simulation should be designed to provide the red team with as much flexibility as possible. This could be achieved by allowing them to write software models which would be included in the simulation. These models could include elaborate tactics which could be changed dynamically depending on the response of the system.

Of course, this technique must use referees to monitor the red team's threat design to insure it does not violate any rules of the game. The referees also test the simulation to see if it operates correctly prior to the simulation run.

After the simulation is checked out, the blue team is briefed and they "man the consoles" and do their best against the threat model. The object of this approach is to test the total capability of the system and locate any weak points.

The following two paragraphs are from a paper which describes the use of an Air Defense Master Direction Center Simulation.[2]

"Four test crews were used at each of the experimental sites in the MDC complex. All four crews were exercised once each day for six days in each of the eight test conditions for a total of 192 exercises. The test situations included three wartime and five peacetime STP problems. All were high load problems designed specifically to stress weak points in the complex."

"Data were collected regarding the time required for the air picture to be displayed on the MDC vertical board. Measures of timeliness, accuracy, and completeness of information were used as criteria for the evaluation of the efficiency of the system under the eight test configurations."

3.2.3.1.3 All-Computer Simulation

This part of the paper will use a hypothetical system design to illustrate how all-computer simulation can be used as a system design tool. The discussion presents a brief description of the system design, a system model and a simulation technique.

The mission of the system is to defend a circular area against attack from approximately 25 ballistic missiles with an 80% probability of destroying 25 missiles, and at 95% probability of destroying 20 missiles.

The system design consists of five interceptor complexes equally spaced on the perimeter of the defended area. Each complex has a computer, command personnel, interceptors, detection equipment and tracking equipment. All of the five perimeter complexes are connected through a master control center which monitors the entire system. Figure 3-3 is a simple illustration of the system deployment and communication links.

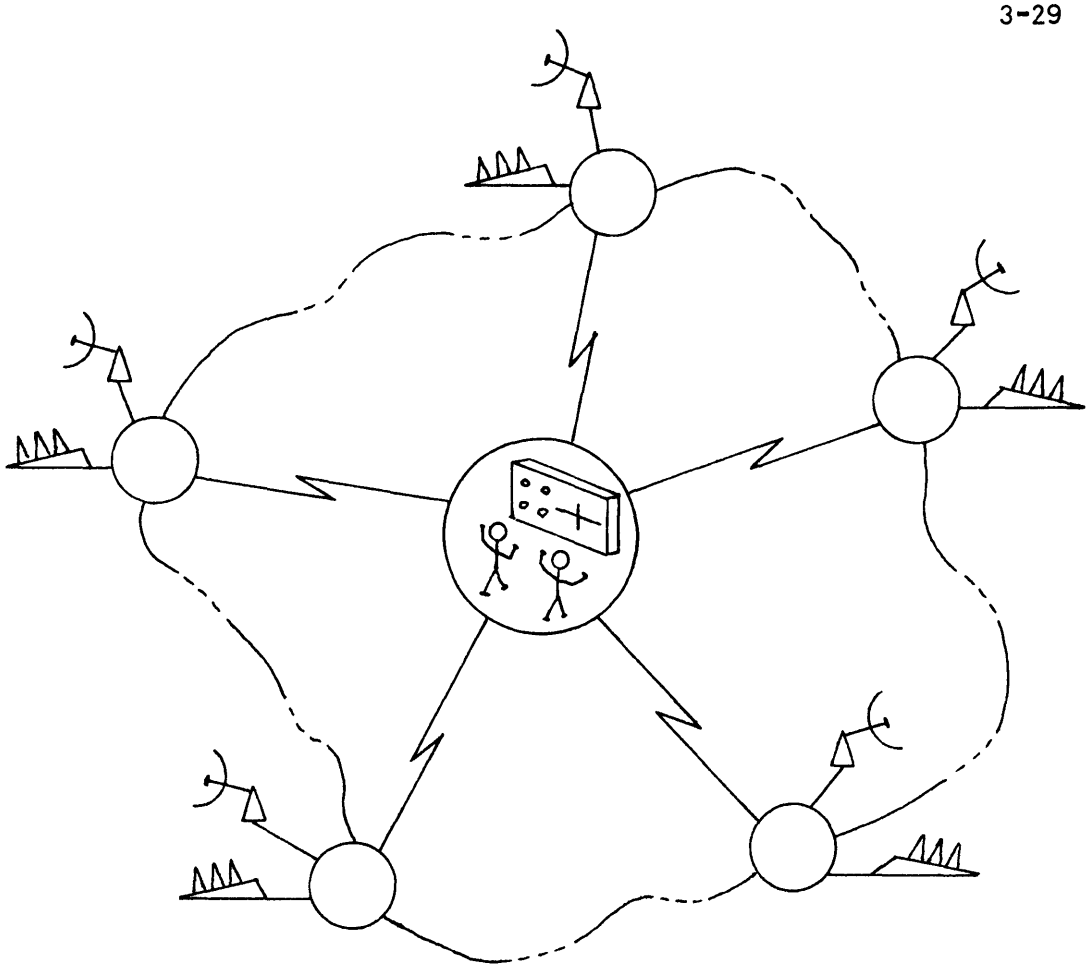

Figure 3-3.

HYPOTHETICAL SYSTEM DESIGN

The following list describes some parameters of the system design which affect the capability of the system. The task of the system designer is to determine a set of parameters which will permit the system to fulfill its mission. At the same time he must consider the system cost involved with each eelection of parameters.

1) The detection ranges of the missiles are uniformly distributed between P_1 and P_2 yards.

2) Each complex has P_3 interceptors which can be launched at a maximum rate of one interceptor every P_4 seconds.

3) The probability, P_5, of one interceptor destroying one missile is a known function of the position and velocity of the missile at the launch time of the interceptor.

4) The time required for the master control center to assign a BM to another complex is normally distributed about P_7 seconds with a known variance; the assignments are processed in order, one at a time.

5) A peripheral complex is destroyed if a missile impacts within P_8 miles of the complex.

In addition to these types of parameters, decision rules must be established which govern the use of the system, i.e.:

1) How many interceptors are launched at each missile?

2) How are weapon assignment conflicts resolved?

3) How much control is exercised by the master control center?

Can the system designers determine a set of parameters and operating procedures which they feel will maximize performance and economy, using their intuition and experience? If they determine a set of parameters, how can they demonstrate the performance of their design for final approval? For example, how can they show the economics of hardened complexes vs. more destructive interceptors?

Although simulation is not by any means a panacea, it is being used successfully to shed light on these types of questions. Some of the evidence of this are the number of simulation languages now being used to study the "machine-shop" class of problems. The block diagrams or flow diagrams which describe this class of problems are very similar to the block diagram which would be used to model the hypothetical missile-interceptor system. The jobs in the machine shop simulation would be analogous to the missiles, and the machines would be analogous to the peripheral complexes.

Figure 3-4 is a simplified block diagram of the missile-interceptor model. Even with this simple problem, however, it would be difficult to determine the capability of the model using pure intuition.

A computer program must be written to exercize the block diagram model of the system design. If a simulation language is not used, a tailored computer program must be written.

Many simulation runs are required to obtain results from a stochastic system model. The approach to the missile-interceptor model would be a Monte-Carlo technique:

1) Design a variety of attack configurations which span the spectrum of expected threats.

2) Select a desirable set of model parameters and decision rules.

3) Run the simulation many times, possibly a thousand times, for each attack configuration.

The effectiveness of the model against an attack configuration will be proved if 25 missiles are destroyed in 80% of the runs and 20 missiles are destroyed in 95% of the runs. If the effectiveness of the model is inadequate, another set of parameters must be tested in an effort to improve the performance. In any case, the model parameters should be varied to study the sensitivity of the model's capability to critical parameters, the number of interceptors launched at each missile for example.

The following paragraph describes a general system simulation program, essentially a simulation language, which is used at the System Development Corporation:

"A major contribution to the tools available for data processing system analysis has been developed in the form of a Data Processing System Simulator (DPSS). The DPSS is an extremely flexible general purpose computer program that provides system performance data on a

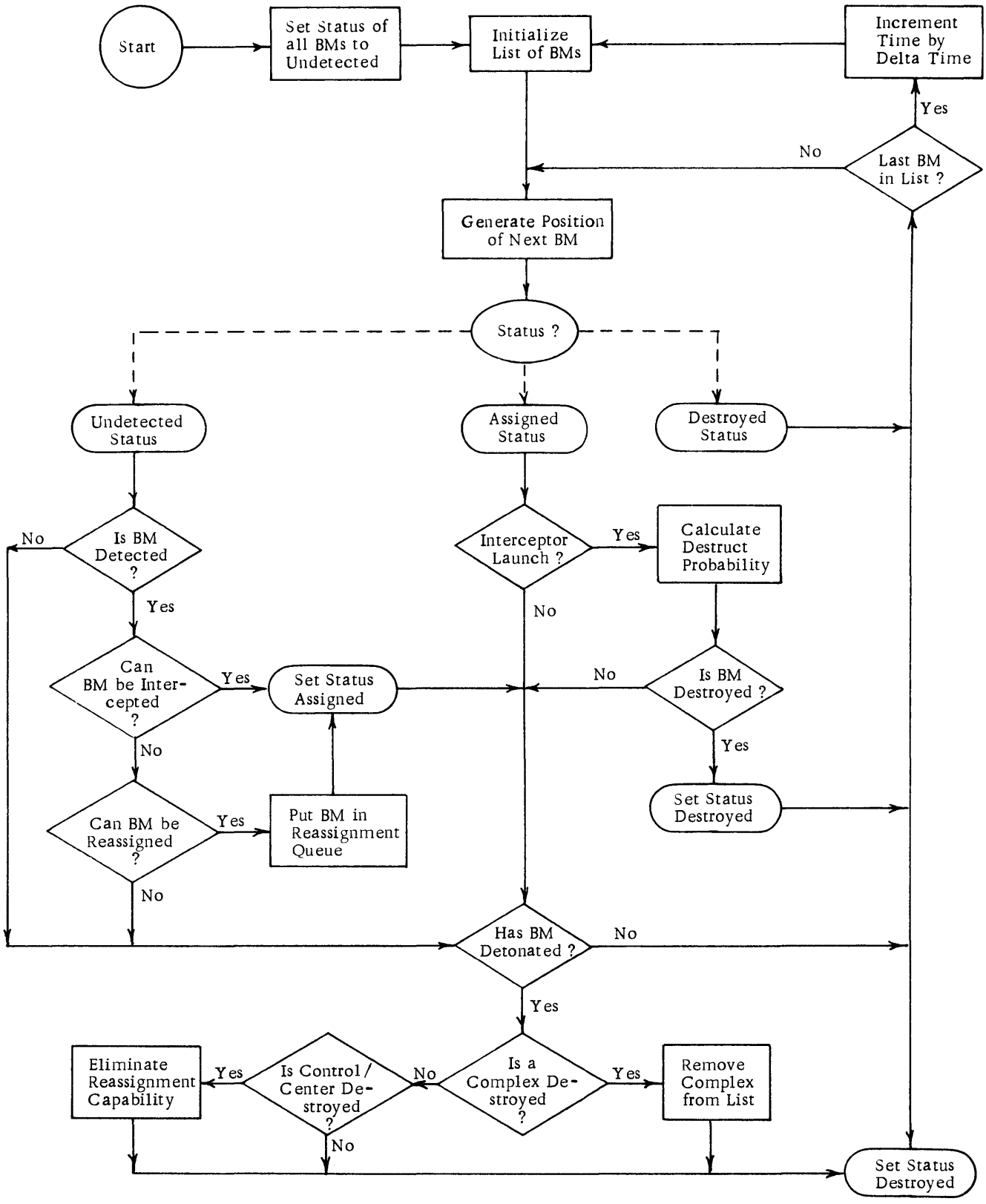

Figure 3-4.

MISSILE-INTERCEPTOR MODEL

proposed new design or modification to an existing design prior to making equipment selections and commitments or performing any significant computer program design. The total system design including the software and equipment portions can be subjected to a rigorous analysis and evaluation early in the design process so that key decisions can be made in the areas of:

1) The kind of equipment to be used.

2) The number of each type of equipment.

3) The kind of data processing discipline and strategy required.

4) The projected performance of the system under varying loads.

5) The system's maximum capacity.

6) The system's ability to respond as a function of loading capacity, and environment."

The degree of validity of the simulation results is dependent on the degree of accuracy of the system model. If one component of the system is modeled inaccurately, the system is sensitive to that component, the results of the simulation will be misleading.

If the system contains an active human component, it will be difficult to develop an accurate model of the system. However, if acceptable models can be developed for human elements, all-computer simulations can be used to save time and money. Models of human elements can be developed using man-machine simulations. This can be done by recording the reaction of many elements in response to a specific display configuration. The recorded data can be used to establish "typical" operator decisions, errors, etc. Unfortunately, models developed in this manner can only be used for the simulation of one situation (one attack configuration).

The performance of the missile-interceptor model is supported by human components which never make mistakes when assigning missiles to complexes. A more realistic model might occasionally cause missiles to be assigned to complexes which have all destruction probability. In either case, it would be difficult to determine the performance of the operators without the aid of a man-machine simulation.

However, even with erroneous components in the system, simulation results can be valuable in determining the relative importance of different components in the system. Suppose that the operators in the BM-interceptor system made errors frequently which affected the total performance of the system by 25 percent. Even with this error in the model, the simulation might still be used to evaluate the trade-offs between "hardened" complexes and more accurate interceptors.

3.2.3.1.4 Conclusions

Operations simulation and all-computer simulation both can be used to answer system design questions. Both types of simulation have advantages and disadvantages which will be presented in the following discussion.

Operations simulation is a valuable tool for determining the operational requirements of a command and control system. This is accomplished by entering actual operating personnel into the simulation so they can uncover functional difficulties of the system design before the system is produced and used in the field. This point is emphasized in the following paragraph.[4]

"The problem described in this paper is probably characteristic of many large system-design problems. Certainly the need for such operational control systems is expanding in the military, and in both civilian and military the need for improved management systems has been ever present. Simulation techniques can prove of much help in these

problems by providing a means of pooling and integrating knowledge from many sources and by providing the opportunity to integrate and vary the many variables and parameters that compose such systems. Although most published simulation experiences have involved all-machine models, we have found much value in man-machine simulation when the problems have involved organizational interactions, the design of information systems, and conflicting or interacting decision rules, since these undergo considerable development during the simulation process."

The main disadvantages of operations simulation are:

1) They require elaborate hardware equipment, i.e., displays, special interface equipment, larger facilities, etc.

2) They require more time to implement,

3) They require more time to run, i.e., they normally run in real-time and require the briefing and debriefing of operating personnel and

4) They require the use of a trained experienced operational crew.

The advantages and disadvantages of operations simulation are reversed for all-computer simulation. All-computer simulation requires no elaborate equipment or facilities (other than a three million dollar computer), it is relatively fast to implement (especially when written in a simulation language) and it can run faster than real-time (if it is not too large). However, it generally cannot be used to uncover any functional difficulties of the operating personnel.

Consequently, all-computer simulation is normally used in conjunction with Monte-Carlo techniques. These require a great number of simulation runs or for the evaluation of large numbers of design alternatives. An all-computer simulation written in SIMSCRIPT was used at the RAND Corporation in a logistics study to evaluate a large number

of scheduling procedures.[5] The two most optimum procedures were then evaluated in an operations simulation of the same system.

In this way, operations simulation and all-computer simulation can be used in conjunction with each other to solve system design questions rapidly and economically.

3.2.3.1.5 A Recommendation

It is recommended that operations simulation and all-computer simulation be employed at the earliest possible stage of ANTACCS design. Actual Navy operating personnel should be used in an operations simulation so they may evaluate the functionality of the operating procedures and total system concept.

"Operations simulation can deal with hardware, command decisions, Human interaction, operating procedures, situational change - in fact, all the important factors operating in and about a system - in such a way that inputs are identified, performance is observed and measured, and outputs are recorded. Here, then, is a significant extension of the simulation technology that provides powerful means of assisting in the design, development, evaluation, and improvement of total systems."[3]

A simulation facility has just been completed at the Naval Missile Center, Point Mugu, California. It is a 1-1/2 million dollar building containing 48,000 square feet of floor space which will be used primarily for weapon system development. This facility would be well suited for an operation simulation effort.

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3.2.4 Simulation for Command and Control System Checkout

3.2.4.1 Introductory

Simulation has become a very popular scientific term. It has been applied to a wide variety of unrelated activities: the numerical integration of equations of motion, management and war games, pilot trainers, sociological and psychological experiments. It seems that the term "simulation" is used whenever any activity is represented by something else. Simulation is also applied to the activity of system checkout. The operation of a system is often initially checked out with test inputs which are not received from the normal or "real" environment. This mode of operation is popularly referred to as a simulation mode.

Electronic circuits are commonly checked with signal generators and oscilloscopes. The signal generator is used to supply an input signal to the circuit while the oscilloscope displays the way in which the circuit transforms the signal. In simulation jargon, the signal generator would be termed a signal simulator.

A similar approach is used to check out command and control systems. This paper describes the simulation checkout of three command and control systems: the Range Safety System, the Real-Time Data Handling System and MTDS.

3.2.4.2 Range Safety System

The range safety system of the Pacific Missile Range is a complex of radars, communication links, computers, command and control devices, etc. Part of the mission of the Range Safety System is to provide range safety support during missile and space launches from Pt. Arguello or Vandenberg AFB. The range safety function is controlled from the Range Safety Control Center at Pt. Arguello, California. Here radar tracking data is collected from many radar sites.

The data is processed in real-time by an IBM 7090 and displayed in the Range Safety Control Center. The displayed information is used to evaluate the performance of missiles. If the missile violates any predetermined limits, it may be destroyed.

A set of computer program parameters must be prepared for each launch. These parameters are the characteristics of the missile, local weather data, program control parameters, etc. Before each launch, a simulation is run which tests the parameters and the equipment in the Range Safety Control Center.

The simulation is controlled by the computer program. When the computer program is in the simulation mode, it reads simulated radar data from magnetic tape instead of reading data from the radar input buffer. The simulated data is actual raw radar data which is recorded from a previous similar launch. The simulated data is processed by the computer program in the normal fashion. The program output exercises most of the equipment in the Range Safety Control Center. This equipment includes digital-to-analog converters, plugboard switches, plotting boards, control consoles, etc.

The simulation checks the operation of the program and terminal hardware but not the radars or communication links. At present the radars are checked out manually by the radar operators at each site.

The Range Safety System has been built up and modified over a period of years. It is a patchwork of many smaller systems. The checkout of all the component systems is a laborious task which must be performed for each launch. This procedure is coordinated by voice communication.

If the computer could monitor or control this routine checkout operation, the operation of the Range Safety System would be more efficient. At present only a few launches can be made each day because of the time-consuming preparations.

The checkout of the Range Safety Center is a relatively simple procedure because it is under computer control. Routine procedures such as system checkout should be controlled by computers whenever possible.

3.2.4.3 The Real-Time Data Handling System

The Real-Time Data Handling System (RTDHS) being implemented at Pt. Mugu, California, is a multi-computer system consisting of peripheral computers and primary computers. The peripheral computers receive and process radar data at each radar site and transmit the processed data to a primary computer. The primary computer processes the data, presents displays and performs control functions. A typical control function would be the transmission of aircraft vectoring commands.

The simulation checkout of RTDHS is similar to that of the Range Safety System. Simulated radar data can be read from magnetic tape and used to check out the computer program and associated equipment. However, the RTDHS simulation can be more comprehensive than the Range Safety System simulation. This can be accomplished by transmitting the simulated radar data to the peripheral computers for processing. After processing by the peripheral computers, the data can be transmitted back to the primary computers. In this way, the hardware and programs at each radar site and the transmission system can be checked out in addition to the operation of the primary site.

Multi-computer systems, such as RTDHS, are readily adaptable to simulation checkout because of the flexibility of program control at many places in the system. RTDHS simulation modes can be expanded simply by modifying the computer programs. For example, each peripheral computer could read simulated radar data from tape and transmit the data to the primary computer. The radars could also be included in the simulation because they can be controlled by the computer program through digital-to-synchro converters.

3.2.4.4 MTDS

Simulation is used in similar fashion in MTDS. The MTDS configuration resembles that of RTDHS. It consists of a central or primary computer which receives the data from a number of satellite computers. The central computer, a Q-20, is used to support the Tactical Air Command Center (TACC) which monitors the entire "battle". The Q-20 is used primarily to control the various displays in the TACC. A satellite computer supports the operations at a Tactical Air Operation Center (TAOC). The TAOC's identify, classify and assign weapons to airborne targets and transmit their actions to the TACC.

The MTDS simulation checks almost the entire system. Targets are generated by the Q-20 and transmitted to the TAOC's where they are processed in the normal fashion. The TAOC's transmit their results to the TACC for display and command/control action.

MTDS also employs several other smaller simulations for checking out system components. The operation of the TAOC's can be checked out individually without involving other parts of MTDS. This is done by supplying simulated targets to the TAOC with a target simulator, the SPS-T2A. The SPS-T2A is a built-in piece of hardware which generates controllable targets.

The best director of MTDS simulation, Major Barnard, made a comment on MTDS simulation: "Simulations should be designed so they may be set up and operated completely by military operations personnel. SDC prepared film which was used for the MTDS simulation runs and the time required for the film preparation was too long."

The simulation checkout in MTDS is quite extensive. The simulations which are used to checkout system components are valuable trouble shooting and maintenance aids. These component simulations can be used prior to a total system simulation to avoid using the entire system to locate a malfunction in one component.

In conclusion:

1) Simulation is an effective method of checking out a command and control system.

2) Simulation can be much more comprehensively in a multi-computer system because more equipment can be included in the simulation.

3) System components should have built-in simulation capability so they may be checked out individually.

3.2.5 Simulation for Command Control System Development

3.2.5.1 Introduction

The preceding paper on simulation discussed the use of simulation for the design of command and control systems. This paper will discuss the use of simulation in the development of command and control systems.

When does the design phase end and the development phase begin? The time of departure is not well defined. The development of some system components may begin before the design phase is finished. However, in order to form a basis for the organization of the paper, an arbitrary time of departure will be defined.

A command and control system (or total system) is composed of a number of subsystems: communication systems, detection systems, weapon systems, transportation systems, data processing systems, programming systems, etc.

The task of total system design involves integrating various subsystems into an optimum geometrical and functional configuration. Part of this task is determining the general characteristics of each of the subsystems. For a detection subsystem, for example, such characteristics could be range, track capacity, accuracy, watts, size, weight, etc. After the general characteristics have been determined for each subsystem, the development of the total system can begin, i.e., the design and development of the various subsystems. This shall be our defined time of departure.

3.2.5.2 General Considerations

The problems involved in designing and developing subsystems are in general the same as those involved in designing and developing total systems, i.e. integrating a large number of components into an optimum configuration. Consequently, much of the general discussion contained in the first paper will also apply here. In order to avoid repetition, only a brief summary of analysis applications is given in this paper.

3.2.5.2.1 Analysis

Simulation plays a major role in the analysis phase of system design. Most of the published material on simulation is classified by ASTIA under "Research." As this indicates, simulation is an important research tool. As such, it is used in the analysis phase of system design. One of the first tasks in the analysis phase is to evaluate a large number of alternative designs. Many times, simulation is used for this purpose because analytical methods are too difficult to apply. For example, the design may contain many non-linear relationships which would eliminate the value of a linear programming solution.

One of the largest applications of simulation is in the field of dynamics. The differential equations or mathematical models of moving vehicles are often too complex for analytical solution. Sometimes the models contain empirical tables, such as atmospheric density functions, which must be represented analytically with series approximations. Consequently, an accurate solution can only be obtained by numerical integration. Although numerical integration solutions bear little resemblence to man-machine or "machine shop" simulation techniques, they are popularly referred to as simulations.

3.2.5.2.2 Optimization

Many of the references cited in this paper state that simulation was used to optimize a system design. System designs which contain only a few parameters can be optimized by evaluating all possible designs. Suppose a system design contains only two parameters and each parameter can assume ten values. All possible cases for a design of this type can be evaluated with one hundred simulation runs.

Unfortunately, the performance of few system designs are dependent on only two parameters. The optimization of multi-parameter systems is much more difficult. The gradient or "hill-climbing" method is generally applied to multi-parameter optimization problems.

The gradient method begins with an estimate of the set of parameters which will optimize the design. This set of parameters is gradually adjusted by small steps until it is no longer possible to optimize the design by further adjustment of the parameters' values. In other words, the top of the "hill" is reached and movement in any direction would be downhill.

The inherent power of the gradient method is the technique by which the parameter adjustment is controlled. The amount by which each parameter is adjusted varies with every step. However, at each step, the vector sum of all the adjustments is constant. The amount by which a parameter is adjusted is proportional to the sensitivity of the optimization function to that parameter. Parameters which affect the optimization function the most are modified by a greater amount. This method follows the steepest path up the hill.

Figure 3-5 is a graphical representation of the gradient method.[6,7]

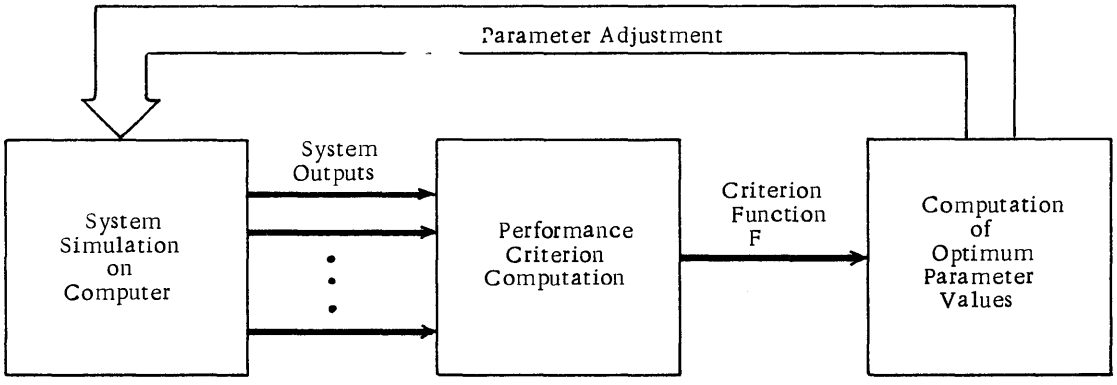

Figure 3-5, Block Diagram of Design Optimization Problem

The gradient method is frequently implemented on hybrid computers. The analog portion of the computer is used to simulate the system design. The digital portion is used to evaluate the performance of the simulated system and to control the adjustment of parameters. The optimization of automatic control systems is one of the largest applications of hybrid computer optimization.

3.2.5.3 Subsystems

The examples presented have shown where simulation has been used in the development of various subsystems of command and control systems. They are intended as an indication of simulation applications and not as a comprehensive treatment.

3.2.5.3.1 Communication Systems

Communication or transmission systems can become quite complex, especially in a decentralized command and control system. Figure 3- illustrates a complex transmission system which could be analyzed with simulation techniques.[8]

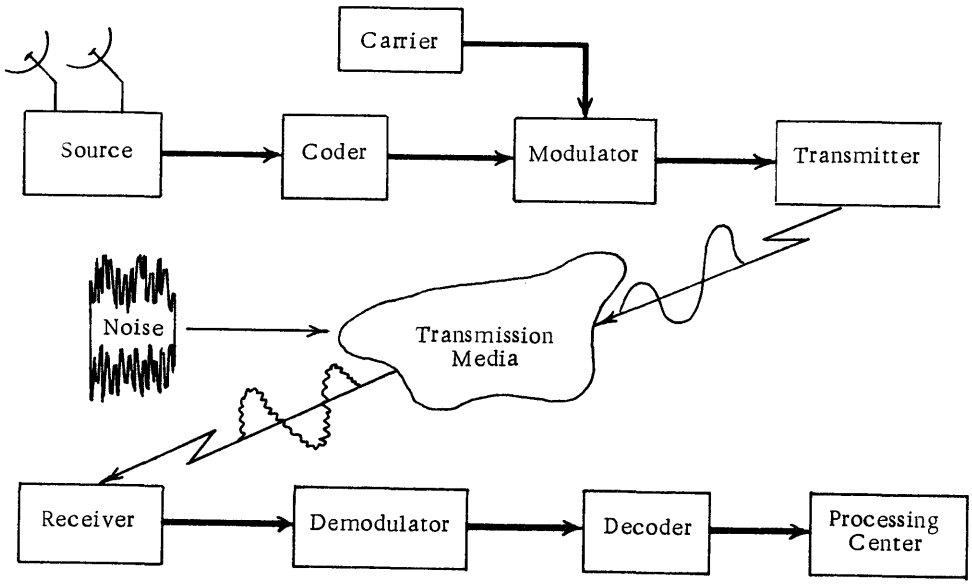

Figure 3-6, Carrier Transmission System

Analog simulation has been used at General Electric to analyze a secure communications system design.[9] The simulation was used to evaluate system feasibility, to determine optimum system parameters and to evaluate system performance in various signal environments. The simulation results saved time and expense by eliminating the construction of hardware equipment. Simulation can be used to analyze the performance of filter methods for reducing the effect of transmission noise or ECM.

3.2.5.3.2 Detection Systems

Radar, sonar and infrared detection systems have been studied with simulation techniques.[10] Simulation can be used to study the system performance as a function of the system errors, for optimization and improvement of system parameters and for analysis of measurement accuracy and track ability.[11]

Analog simulation has been used at General Electric to improve radar system design concepts. Potential areas of difficulty were illuminated by the simulation early in the design phase.[12]

An article published in Russia describes how digital simulation is used as a research tool for studying electromagnetic fields around disturbing objects, i.e., plates, discs, cylinders and spheres.[13]

3.2.5.3.3 Weapon Systems

The complete assortment of simulation tools can be used in the design and development of weapon systems.

Digital computer simulation can be used for the solutions which require great accuracy. Digital simulation is used for determining guidance parameters of ICBM's and space vehicles. The successes of missile launches demonstrate the accuracy of these simulations. Unfortunately, accurate digital simulations require a large amount of computer time. Many times the calculations must be performed in double precision arithmetic.

On the other hand, analog simulations require relatively little computer time but are not highly accurate. Consequently, analog simulation is used when many solutions are required. For example, analog simulation can be used for analysis of guidance techniques or the calculation of kill probabilities of air-to-air missiles.[14]

Man-machine simulation can be used to study the performance of human components in weapon systems. The ability of pilots to navigate from vectoring commands is being studied with man-machine simulation at the Naval Missile Center, Pt. Mugu, California. The pilot sits in a mock-up of a cockpit and responds to the vectoring commands by manipulating conventional controls. The position of the aircraft is calculated with analog simulation.

TV missile systems have been analyzed with man-machine simulation in order to determine the ability of pilots to guide missiles. The pilot is supplied with a TV picture of a target and stick for guiding the missile. The missile is simulated with a TV camera that is mounted on a platform which moves towards a model target. The motion of the platform (the missile) is controlled by an analog computer which simulates the motion of the missile in response to the pilot's commands.

Sometimes actual system hardware is studied by simulating the environment of the hardware component. Infrared seeker components have been studied by supplying a moving target to the seeker through an arrangement of lenses and mirrors. The motion of the seeker platform (the missile) and the target are controlled with an analog computer.[15]

3.2.5.3.4 Transportation Systems

Analog and digital simulations are used to study damped spring mass systems (suspension systems) of transport vehicles.[16] Analog simulation is used more extensively because it is better suited for the solution of differential equations.[17] These simulations are valuable for determining the shock and stresses on delicate components which must be transported: computers, communications equipment, guidance equipment, etc.

General Motors has written a simulation language, DYANA, which is used to simulate complex damped spring mass systems. The input to DYANA is a description of the physical system, i.e. geometry, spring constants, damping coefficients, forcing functions, etc. DYANA translates the input into a set of differential equations which represent the system. A Fortran program is punched by DYANA which will solve the equations and print out the responses of system components.

3.2.5.3.5 Data Processing Systems

Simulation is used at the micro and macro level of the development of data processing systems. One of the largest applications of simulation at the micro level is for the checkout of logical circuit designs. Since computer logic is essentially boolean algebra, it can be represented with boolean expressions. This type of simulation operates at the bit-time level for the checkout of logical circuits.[18]

The application of simulation at the micro level is not limited to computer circuits. A paper presented at the Western Joint Computer Conference 1957, describes how other computer components can be simulated, i.e. drum memory, word structure, information channels, etc.[19] Simulation has also been used to study error patterns in computer information channels.[20]

Simulation at the macro level is used at SDC for the design of data processing systems. The following excerpt describes a simulation program which is used for this purpose.[21]

> "A major contribution to the tools available for data processing system analysis has been developed in the form of a Data Processing System Simulator (DPSS). The DPSS is an extremely flexible general purpose computer program that provides system performance data on a proposed new design or modification to an existing design prior to making equipment selections and commitments or performing any significant computer program design. The total system design including the software and equipment portions can be subjected to a rigorous analysis and evaluation early in the design process so that key decisions can be made in the areas of:

"1) The kind of equipment to be used.

2) The number of each type of equipment.

3) The kind of data processing discipline and strategy required.

4) The projected performance of the system under varying loads.

5) The system's maximum capacity.

6) The system's ability to respond as a function of loading, capacity, and environment."

IBM has written a simulation language, GPSS, which can be used to study data processing system designs. The following example is taken from the GPSS reference manual.[22]

"EXAMPLE 3 - RAMAINDER DIVISION: A DISK FILE APPLICATION

In a disk file, the disks revolve at the rate of one revolution per 50 milliseconds. Each disk comprises 100 tracks, and each track is subdivided into five sectors.

Assume that an access arm has been positioned to the desired track and that the following sequence of operations is to take place:

OPERATION	Time, Ms.	Equipment
1. Wait for desired sector	25±25	Channel
2. Read record	10	"
3. Update record	30±5	" + CPU
4. Wait for desired sector	?	"
5. Write and write-check record	60	"

The beginning of operation 5 must follow the beginning of operation 2 by an integral multiple of 50 milliseconds. If the CPU is timeshared, operation 3 may cause a delay of unknown magnitude.

3.2.5.3.6 Programming Systems

The programming system which controls the real-time processing in a command and control system is generally under a continual modification. The modifications result from improvements or expansion of the system. Simulation can be used to check out these modifications. This is accomplished by simulating input data to the system which will test the program's functions.

The programming system designed by Informatics for the Real-Time Data Handling System at Pt. Mugu, California, operates in a variety of simulation modes.[23] One mode uses simulated radar data from magnetic tape to check the operation of the programming system. Another simulation mode is used to check out the system hardware prior to an operation.

3.2.6 The Role of Simulation for Test and Evaluation of Navy Command Control Systems at Pt. Mugu.

3.2.6.1 Introduction

An example of the role of simulation is the testing and evaluation of new and complex systems is presented by this description of the simulation facilities which are operated by the Navy at the Naval Missile Center, Pt. Mugu, California, Facilities similar to those described can be extremely valuable to electronic system designers. Not only are they of value in the examination of tactical and attack parameters, such as range at time of firing, but also similar, less sophisticated facilities, can be of great value of the system designer in the evaluation of alternative design concepts during early phases of design.

3.2.6.2 Mission of Naval Missile Center

The purpose of this section is to show the organizational composition, functions and responsibilities of the Naval Missile Center.

3.2.6.2.1 Organization

The U.S. Naval Missile Center is a tenant activity of the Pacific Missile Range. Its management control coordination is provided for the Bureau of Naval Weapons by the Assistant Chief for Research, Development Test and Evaluation.

The Naval Missile Center is, therefore, under the military command of the Commander, Pacific Missile Range, and under the Management Control of the Bureau of Naval Weapons. Under the Commander of the Naval Missile Center, the major technical branches are inter-related as shown in Figure 3-7.

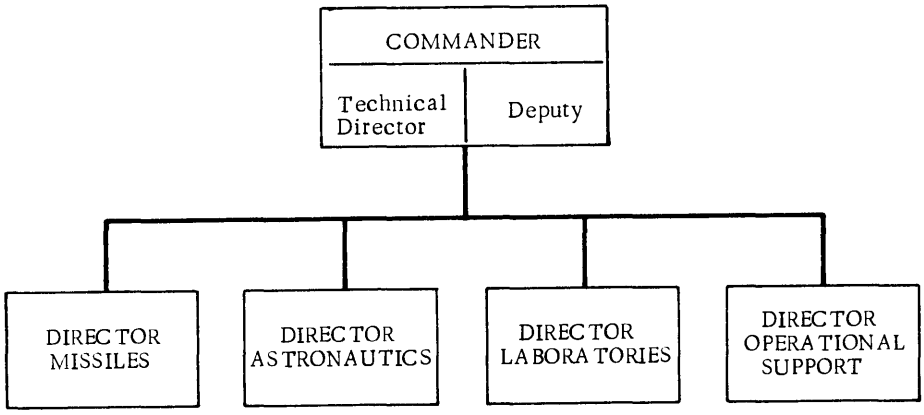

Figure 3-7

3.2.6.2.2 Functions and Responsibilities

The mission of the Naval Missile Center is, in accordance with SecNav Notice 5450: To conduct tests and evaluation of Naval guided missiles, their components and weapons systems; to provide services and support to the Pacific Missile Range; to provide supporting services pertaining to planning, development, evaluation and training in the field of astronautics and bio-science.

1) Conduct test and evaluation of Naval airborne tactical data systems and components.
2) Perform Board of Inspection and Survey Trials for integrated naval weapons systems in accordance with Board of Inspection and Survey Directives.
3) Perform research and development for advanced simulation, instrumentation, environmental test techniques, and improved serviceability and reliability characteristics of missile weapon systems.

To accomplish these task assignments and the total mission, the basic line functions of NMC are divided into four basic directorates. These directorates have the following responsibilities:

1) Director Missiles

The Director of Missiles has the responsibility to provide technical plans and direction for the test and evaluation of missile systems subsystems and components. Under this directorate are the project offices which coordinate the following projects:

Sparrow III
Bullpup/Shrike
ATDS
PHOENIX

2) Director Astronautics

The director of astronautics has the responsibility of planning, prosecuting and managing the astronautics and advanced weapons programs assigned to the Naval Missile Center.

3) Director Laboratories

The director of laboratories has the responsibility for planning, prosecuting and managing the laboratory activities surrounding the development, test and evaluation of weapon systems/subsystems and the life science aspects of the missile and astronautics programs assigned to the command.

4) Director of Operational Support

The director of Operational Support is required to provide operational support to the Pacific Missile Range (PMR), Naval Missile Center (NMC), and as directed to the Fleet and visiting and tenant units in the areas of aircraft maintenance, target support and photographic services.

3.2.6.3 The Simulation Laboratory

Construction is being completed on a new simulation and vectoring facility for the Naval Missile Center. The laboratory will contain analog computers and other special purpose electronic equipment, and will study a large class of problems with prime emphasis on simulation testing of Navy weapons systems.

3.2.6.3.1 Role and Function of the Simulation Laboratory

The use of simulation in the development and test of missile weapon systems is not new at the Naval Missile Center. Analog computers have been used for this purpose since 1950.

The original computers were housed in a single room in one of the large quonset buildings in the old technical area on the beach. Simulation activities have grown over the years until now all of three temporary frame buildings and partsof two others are being used for this purpose.

The most general role and function of the simulation laboratory is to use simulation studies for all those problem areas which can be effectively studied by this method. The tremendous new physical plant and equipment being allocated to this effort speaks for its success in the role of simulation as a tool for test and evaluation.

3.2.6.3.2 Physical Plant and Equipment

The new simulation laboratory (a $1,500,000 structure) is located at Point Mugu on the beach south of 20th Street. It will rise on a 300 foot front and contain 48,000 square feet of floor space.

There will be 40,000 square feet of laboratory and office space on the ground floor. A tower will house aircraft mockups on the second floor and missile system evaluation laboratories on the third floor.

The facility will be used by NMC for simulation of all parts of weapons systems by electronic analog computers and for vectoring missile-carrying aircraft into correct positions for launching missiles against airborne targets.

Simulation activities will account for most of the laboratory areas in the building. Space has been planned not only for the computers and special devices to simulate parts of weapon systems, but also for shops and laboratories.

The shops will be used to maintain and modify the computers, and the laboratories to design and build other simulation equipment.

The analog computers currently in use and to be moved to the new facility are of several varieties. The REAC (Reeves Electronic Analog Computer) has five consoles, each of which contains approximately 60 amplifiers; and two of which have a bank of six coefficient function generators. The newest of the laboratories' computers is the Beckman EASE 2133. This is a $200,000 class analog computer and has many important features including all electronic multiplication, 20 cycle bandwidth, and considerable capability for presentation of digital information to the operator, both dynamic and printed. This computer has 120 amplifiers, 6 electron resolvers, 40 multipliers, 180 potentiameters and 120 trunk lines for communicating with external devices.

The oldest of the large analog computers is the Bendix three-dimensional flight simulator which is approximately eight years old. This computer has 88 amplifiers.

The PACE computer built by EAI is used for small problem analysis such as checking the roll control device on PHOENIX. This analog computer is classed at 100 amplifiers.

In each of the above computers, the number of amplifiers has been referenced, thus providing a reasonable index to the amount of inherent computational capability provided by each analog computer. There is also some current discussion centering around the acquisition of a digital computer. This will probably come to exist in what is currently called a "Hybrid" configuration.

3.2.6.3.3 Current Applications

Prominent among the simulation projects being carried on now and to continue in the new building is a cockpit mockup of the F4B (Phantom II) airplane. This was designed and built in the present simulation laboratories to study the problems involved in attacking an enemy airplane when the pilot of the missile-carrying interceptor never actually sees his target. The laboratory studies using the initial capability of the F4B cockpit were initially concerned with two basic problems:

1) How does a ground or shipboard controller, using a long range search radar, vector the interceptor airplane into a position where its own airborne radar can "see" the target?

2) How can the airplane be flown close enough to the target to successfully launch a missile?

The pilot must depend entirely on information obtained from his radar system to do this. Hence, with this "vectoring" problem to study, the most important part of the F4B cockpit simulator is the radar display. Every effort has been made to have the pilot and his radar observer see the same displays that would appear in a combat situation.

Closely associated with the intercept evaluation is the test and evaluation program for the Airborne Tactical Data System (ATDS). This is a computer-automated fleet-oriented system with similar objectives.

The cockpit simulator requires three large analog computers to realistically represent:

1) The response of the airplane to the flight controls.
2) The geometry (or geography) of the problem, sometimes extending over several hundred miles.
3) Simulation of the electronic equipment aboard the airplane which transforms the raw radar information to meaningful displays.

The ATDS is typical of a complete weapon system which must be located in a laboratory where it can be studied in a simulated environment. This system consists of a high-powered search radar and a number of digital computers which automatically interpret what the radar sees, display the information and automatically direct a number of fighter aircraft to intercept enemy aircraft.

The equipment is all carried aboard the twin-engine E-2A (Hawkeye) airplane.

A set of operational ATDS radar-computer-display equipments, as found in the Hawkeye, is installed and operating at the Naval Missile Center in laboratory spaces near the analog computers.

The laboratory ATDS is able to "talk to" and automatically exchange information with any operational ATDS aircraft while flying in this area. The laboratory ATDS will be an important occupant of the new Simulation and Vectoring Facility.

By locating the laboratory ATDS near the analog computers, many tests of the automatic detection tracking and reporting functions of the ATDS computers can be performed without actually having airplanes in the air.

It is possible to know how accurately the ATDS can do its job without actually putting an airplane in the air.

3.2.6.4 A Cockpit Simulator

An intercept simulator was constructed at the Naval Missile Center to aid in evaluation of the F-4B/SPARROW III and Airborne Tactical Data System weapons systems. The simulator combines an analog computer with a mock-up of an F-4B cockpit and accessory equipment to simulate, in the laboratory, the flight of a single F-4B fighter from combat air patrol to breakaway maneuver in the interception of an enemy aircraft.

Simulation of the intercept flight is achieved by solving, on an analog computer, mathematical equations representing the fighter-target intercept dynamics, and by duplicating with operating hardware the cockpit portions of the F-4B airplane. This duplication includes the airborne-intercept-radar controls and displays for both the clear and countermeasures environment.

The cockpit itself provides simulation only through the navigational instrumentation. No attempt is made to provide such effects as optical (landscape), thermal or gravitational effects as is common in simulations used in preparation for lunar landings.

It has been found, however, that for this particular intercept problem, the adjustment period for pilots to fly smoothly and effectively without "feel" is a few days and that this lack of "feel" does not affect the general validity of the system tests.

3.2.6.4.1 General Statement of Test Objectives

By combining an analog computer with a mockup of an F-4B cockpit and accessory equipment, the intercept simulator duplicates many of the flight conditions found in Naval airborne intercept tactics. Such tactics, as used in current fleet defense strategy, deploy early warning (EW) aircraft around a fleet perimeter, with F-4B interceptors on combat air patrol (CAP) 100 to 150 nautical miles distant. The early warning radars contact and track approaching aircraft; the information is processed by a Combat Information Center (CIC) and, if the aircraft is determined to be hostile, a CIC air controller dispatches one or more of the patrolling F-4B's to intercept the enemy. Radio communications from the CIC to the F-4B pilot guide or "vector" him until he can detect the hostile target with his own airborne intercept (AI) radar. After detection, the target is automatically tracked by the AI radar until the pilot has launched his missile and maneuvers away from the collision area.

Future fleet defense operations are similar in broad outline, but will involve the Airborne Tactical Data System (ATDS) and the Naval Tactical Data System (NTDS). In these systems, discussed in the following sections, information is processed automatically by digital computers, and once the interceptor pilot is assigned to a mission, vectoring information is automatically transmitted, received and presented to him by electronic means.

The F-4B intercept simulator consists, physically, of the following major units:

- Electronic Analog Computer
- Pilot's Cockpit
- Radar Intercept Officer's Cockpit
- CIC Station
- AN/ASW-13 Digital Data Communications Set

With these interconnected units, the flight, or any portion of the flight, of a single F-4B fighter can be simulated from CAP position to breakaway maneuver. Although no actual motion of the cockpits is involved, the pilot and radar operator "fly" the F-4B within its designed aerodynamic limits, receive vectoring commands from the CIC, operate the AI radar in finding and tracking a target, and respond to radar scope displays and instrument indications duplicating those in actual aircraft. Countermeasures (CM) effects, such as voice jamming, chaff, decoys and range jamming, can be included in the simulation. The intercept simulator allows technical areas of interest, such as vectoring accuracy of the effects of engineering changes, to be readily investigated; the results are combined with other ground tests and with flight tests in an overall weapons-system evaluation.

3.2.6.4.2 Simulation of Intercept Problems

The simulation of the intercept problem is achieved by solving, on the electronic analog computer, mathematical equations representing the fighter-

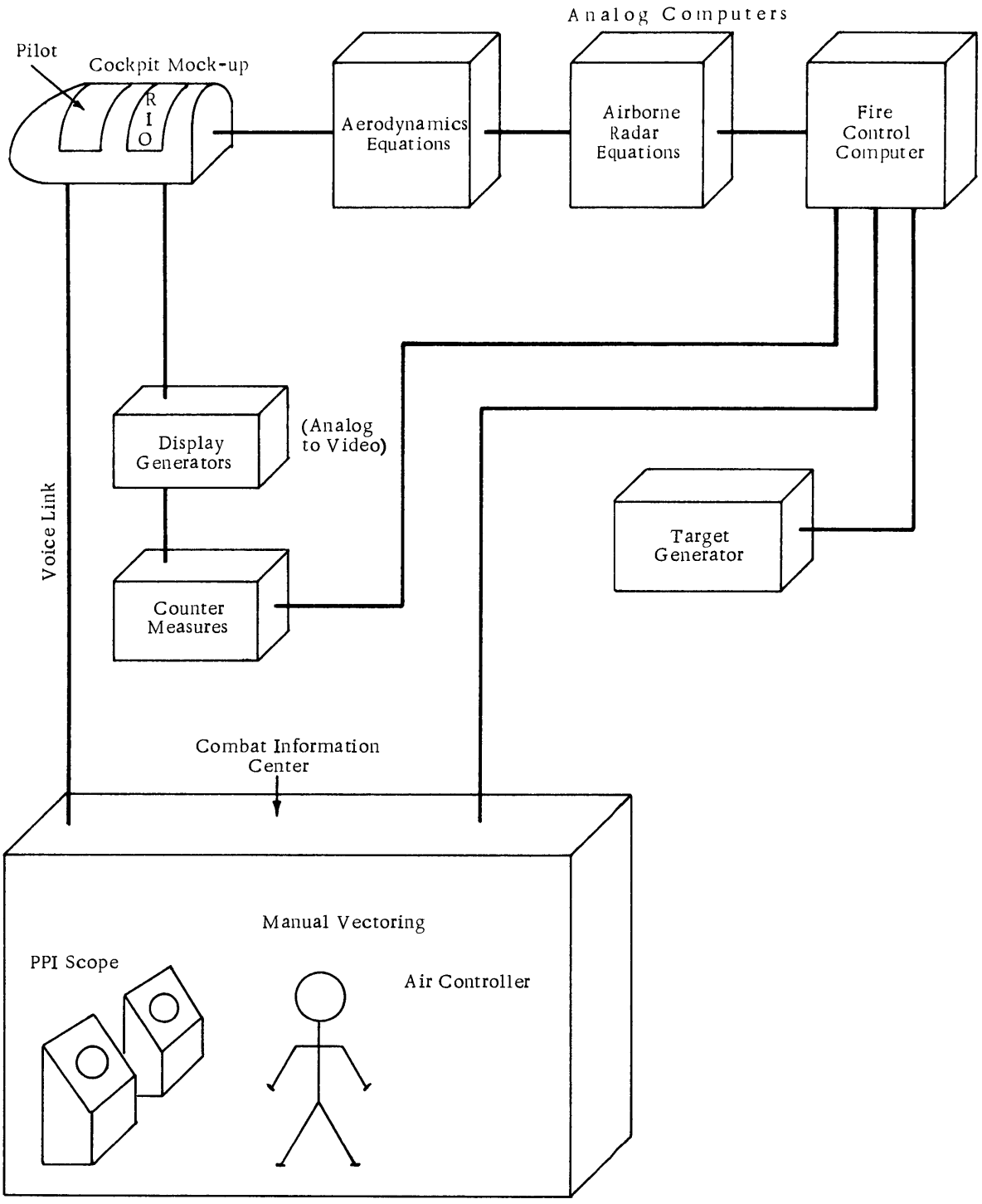

Figure 3-8

MANUAL VECTORING SCHEMATIC

target intercept dynamics, and by duplicating with operating hardware the cockpit portions of the F-4B airplane, the CIC station and countermeasure effects. The computer and hardware occupy separate rooms, but are cabled together and function as a single unit to simulate a typical intercept situation or problem.

The electronic analog computer (EAC) is an assembly of electronic and electro-mechanical units in which DC voltages are used to correspond to mathematical quantities or variables. Each of the units in the computer is capable of performing one or more mathematical operations on the voltages (and, therefore, on the mathematical quantities) fed into it. By interconnecting the units to perform all the operations called for by any given set of equations, an electronic scale model of the mathematical equations is thereby produced, and the computer can then be operated to give a solution. The equations are typically those of engineering or physical systems, in which mathematical operations produce changes in the variables with time; variables such as position in space, velocity and heading are examples. In the analog computer, the voltages vary continuously with respect to time in a corresponding manner.

The equations necessary to simulate the typical intercept problem can be divided into four main groups. The equations are interrelated in actual use and the quantities obtained are instantaneous.

1) Aerodynamic Equations
   These represent the flight characteristics of the F-4B aircraft. Quantities such as its acceleration, turn rate and climb rate are obtained.
2) Kinematic Equations
   These represent the position and attitude of the fighter and target as viewed from the early warning (EW) reference point. Quantities such as distances north and east from the EW station are obtained.

3) AI Radar Equations

These represent the basic geometry between fighter and target. Quantities such as the elevation and azimuth angles of the target with respect to the fighter are obtained.

4) Fire Control Computer Equations

These represent identical equations which are mechanized in the Airborne Missile Control System (AMCS) of the F-4B, and which produce visual indication on the radarscopes of favorable conditions for firing a missile. Quantities such as the maximum error in heading that the missile can tolerate and the distance, or range, to missile are obtained.

The quantities -- In the form of voltages -- obtained from the continuous solution of the above equations are connected to the various units of operating hardware via cables from a group of external terminals in the analog computer. Likewise, quantities obtained from the operating hardware can be entered into the equations via these terminals.

Full dimensioned hooded cockpits of wood and sheet-metal construction are provided for a pilot and a radar intercept officer (RIO). The pilot's cockpit is equipped as essentially with a control stick, rudder pedals, throttle, instrument panel, AI radarscope and a communications set; the RIO cockpit is equipped with an AI radar control set, AI radarscope, cummunications set and an instrument panel. External to the cockpit and supplementing the AI radar is a rack of electronic circuitry which performs several functions:

1) Converts analog-computer outputs to video for radarscope displays.
2) Provides realistic AI radar switching sequences and modes of operation.

3) Produces the simulation of enemy countermeasures effects such as chaff drop, angle and range deception, noise jamming and voice jamming.

The rack is of modular design so that changes can be made readily.

The CIC station is located in a separate room approximately 50 feet from the cockpits. The station's main simulation equipment consists of a plan position indicator (PPI) and a communications set. Supplementing the PPI scope display, it also provides for the simulation of countermeasures such as chaff drop, range jamming, multiple targets and decoys.

A fully operating prototype of the ATDS weapons system, is being evaluated in another section of the Computer Division laboratory. The evaluation plan calls for a tie-in with the F-4B Intercept Simulator. Anticipating this requirement, the cockpits were prewired for installation of the tie-in unit, an AN/ASW-13 digital data communications set. Now installed, it displays vectoring information automatically from inputs received from the ATDS system. When the simulator is used in ATDS operations, the CIC station is normally disconnected.

Suppose a hostile aircraft has been detected at a range of 350 nautical miles at point due north of CIC station. The target has been determined to be 40,000 feet above mean sea level and to be proceeding south at a speed of Mach 0.9. An F-4B fighter on CAP has been assigned to intercept the enemy. The CAP station is angularly removed 40 degrees east of a line extended northward from fleet center; the F-4B is initially flying at a speed of Mach 0.9.

The conditions just discussed are initial conditions which must be specified and set into the simulator before actual operations begin. Each such condition may be prescribed over a wide range of values, enabling the simulation of a variety of intercept situations. The target and fighter appear as blips on the PPI at the CIC station. When the simulator is turned on, air controller notes movements of the blip and calculates the heading and speed the F-4B should take; he then radios this information to the pilot (communications jamming, if present, will interfere). The pilot manipulates the control stick, rudder pedals and throttle as he would in an actual flight.

These motions produce changes in the EAC equations and such changes are instantly reflected in the cockpits as instrument movements and AI radarscope displays, and in the CIC as a scope display, hence giving the effect of continuous flight.

The intercept can be divided into two phases--search and attack. In the former phase, the pilot continues to be vectored by the air controller, while the RIO manipulates the radar control and searches for the target on his radarscope. Upon detecting the target, the RIO acquires lock-on, at which time the atuomatic tracking mode of the radar is simulated and the scope display channels are switched to receive fire-control computer inputs; the attack phase has begun. The pilot now has on the scope a visual indication of how to maneuver the airplane to a favorable missile-launch position, when to fire a missile (the missile itself is not simulated), and when to break away from the impact area. At any time during such a flight, the various CM effects can be switched in or out.

Figure 3-9 is a functional block diagram of the simulator.

3.2.6.5 ATDS Test and Evaluation

The modern tactical environment places increasing demands on the mobility, flexibility and dispersion of the Carrier Task Force. The task of gathering, transmitting and processing tactical information into decision making form for the Fleet Commander and his staff has grown proportionately. The Airborne Tactical Data System (ATDS) has been developed to satisfy this need for improved data acquisition and cross-tell to permit rapid command appraisal of the overall tactical situation, as well as rapid solution of a mass of detailed problems required for the precise control of the elements of the Task Force.

The ATDS is, therefore, an airborne system which is designed to provide both intercept control and early warning to the fleet.

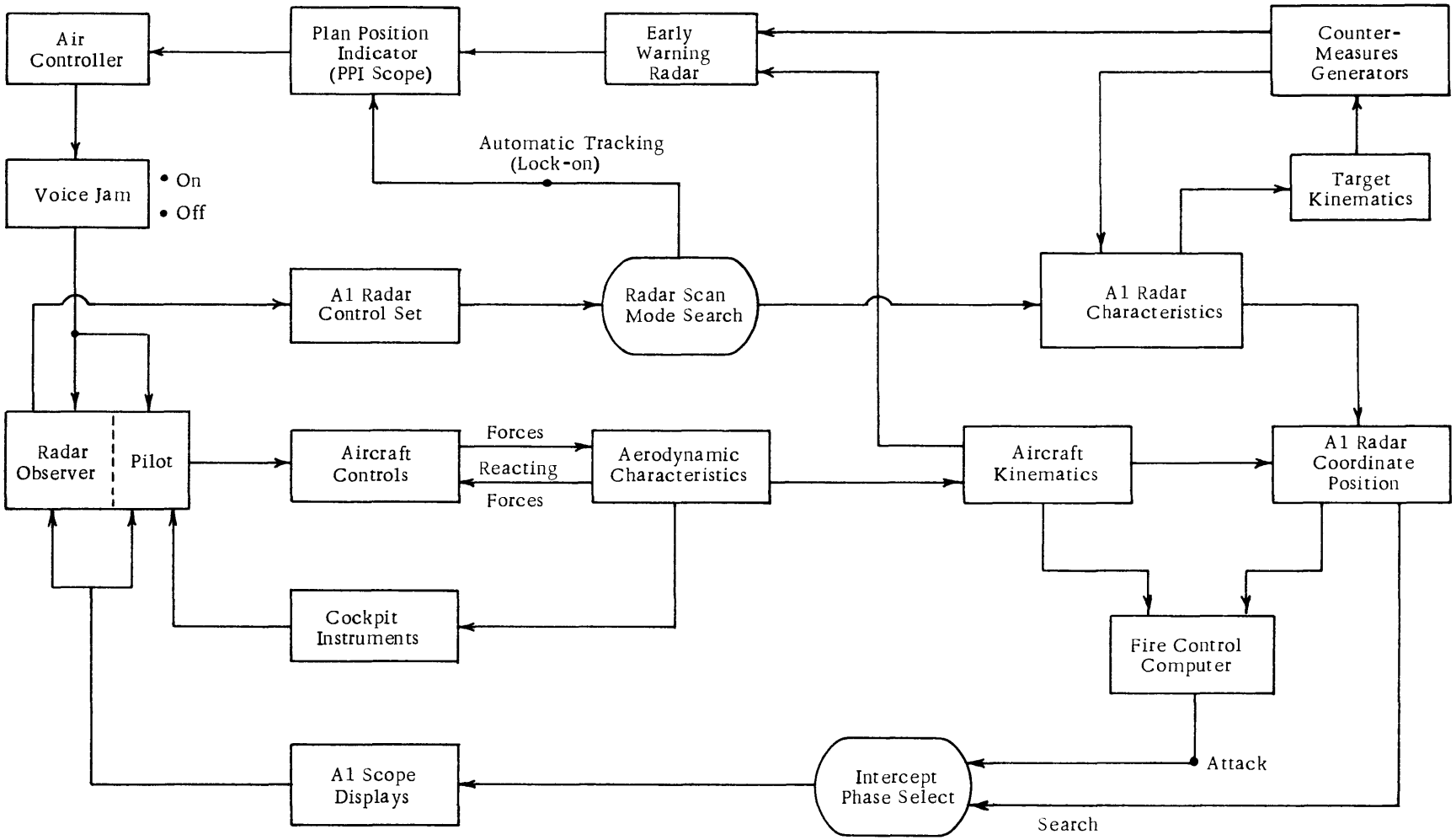

Figure 3-9

FUNCTIONAL BLOCK DIAGRAM OF F-4B INTERCEPT SIMULATOR

3.2.6.5.1 Evolution and Function of ATDS

A basic role of the Naval Missile Center is to conduct engineering test and evaluation of Navy Weapons System. From this point of view, the ATDS is considered to be an experimental system, and the purpose of the current test and evaluation activities at MNC is to determine the feasibility of this concept.

The Bureau of Aeronautics started the development program for ATDS in 1955 and evaluation work began at the Naval Missile Center in 1958. The original AEW aircraft consisted of a radar, PPI scopes and an operator with a grease pencil and a voice communication link. He would visually detect and track the "bogies" and report them over the communication net.

As a result of some considerable experience with this technique, system designers came to believe that this approach to the AEW function would be inadequate both because of target saturation and because of the excessive reaction time required to classify the target and assign weapons to the threat.

The ATDS evolved, therefore, to provide automated processing of many functions such as; automatically processing the radar data and detecting the presence of a target, automatically tracking the target and automatically reporting this target to some surface activity such as the Naval Tactical Data System (NTDS), automatically vectoring an interceptor to a point where its own system can take over control of the intercept.

Thus, the modern ATDS system has evolved. This carrier based system utilizes the Grumman E-2A (W2F-1) and has an extensive complement of associated electronic equipments including: Display Equipment, Communication and Data Transmission Equipment, Radars, Identification Equipment and Data Processing Equipment.

This complex array of electronics is required to implement the wide class of functions assigned to these airborne picket ships. The required system command and control functions of the ATDS include:

1) Detection
2) Acquisition
3) Identification of Target
4) Evaluation of Threat Potential
5) Weapon Assignment
6) Transmission of Control Data to Interceptors
7) Transmission of Tactical Data among the various Elements of the Fleet
8) Provide Accurate Navigation Computations

These system functions are to be accomplished automatically, semi-automatically, and manually as required by the particular mission objectives.

The ATDS command and control functions indicated above are implemented by the following subsystems and principal components:

1) Detection Subsystems
2) Navigation Subsystem
3) Communication Subsystem
4) Data Processing Subsystem
5) In-Flight Performance Monitoring

3.2.6.5.2 Test and Evaluation Methods

The purpose, again, of these MNC activities is to test and evaluate the ATDS. To perform this function adequately, an effort was made to acquire the prime avionics equipment. These equipments were received and installed in the laboratory.

To exercise these equipments, a complex of analog computers and other support devices such as inertial subsystems and the air data computer were built by MNC so that the system would function in the laboratory as a complete system. Tests of the ATDS systems were run both with the laboratory set and with conventional ATDS craft. Of particular interest here, of course, is the laboratory-based tests. The test series of the laboratory ATDS was conducted in the following modes:

1) Test runs using simulated inputs.
2) Test runs in the laboratory using live inputs from radars scaning targets in the sea test range.
3) Combination of live and simulated inputs.

In addition to these test modes, computer programs for the IBM 7090 were written to do computer simulation of some of the computer functions such as detection, tracking and vectoring. In these cases, the 7090 programs are written in such a manner as to duplicate, identically, the computations performed in the computer equipments of the ATDS craft. Using this technique, one can exercise the logics of the system with the widest possible choices of circumstances to verify conditions and tests that would rarely happen in live testing.

3.2.6.5.3 Simulated Environments for ATDS

One of the important aspects of the test and evaluation effort is the series of controlled laboratory tests. These tests runs in the laboratory facilitate data gathering and recording and, through the use of simulated inputs, provide a very large data base for subsequent evaluation.

To contrast the simulated inputs with the equipments being exercised (see Figure 3-10), these functional subsystems are described:

The Detection Subsystem has three principal components:

1) Search Radar Set
2) Radar Recognition Set (IFF)
3) Computer Detector

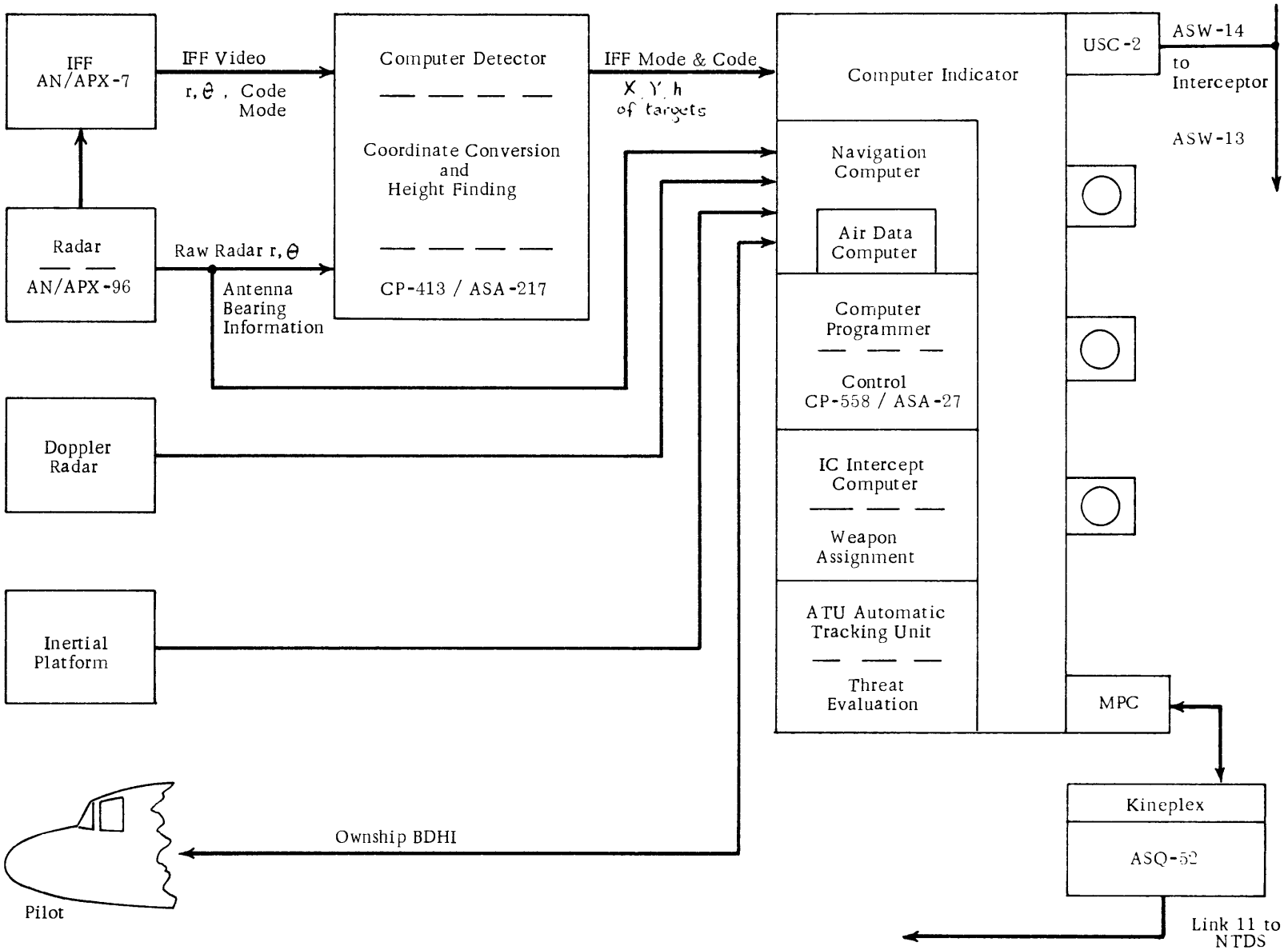

Figure 3-10

ATDS Prime Avionics Equipment Configuration

These components are designed to perform the following functions:

1) Detection

The Search Radar supplies raw video to the Computer-Detector and to the AN/ASA-27 Computer-Indicator Group (CRT) displays.

Detection probability for weak radar and IFF legitimate target returns is enhanced by correlating received signals on a sweep-to-sweep basis, thereby permitting lower thresholds than would otherwise be possible. Acquisition of false or meaningless targets by the Computer-Detector is controlled by sensing the azimuthal and range duration of radar and IFF returns (high density target areas), thereby moderating the effects of ECM, sea clutter or other sources of noise that would otherwise tend to reduce the target handling capacity of the system.

2) Identification

The Radar Recognition Set transmits and receives IFF data, compares received IFF data with previously stored data and transmits "verification" signals, as well as raw IFF video for display, to the AN/ASA-27 Computer-Indicator Group via the Computer-Detector. IFF data transmitted to the AN/ASA-27 Computer-Indicator Group consist of:

a) An IFF security check bit generated by the Computer-Detector to indicate a successful bracket decode of IFF by the Radar Recognition Set.

b) The numerics of IFF replies received by the Radar Recognition Set.

c) An IFF validity bit to indicate successful decode and comparison of IFF with previously stored IFF code information.

3) Height Finding and Coordinate Conversion

Target height is determined by special processing of search radar video. Target position data is converted from polar (R-θ) to rectangular (X - Y) coordinates and, together with target height data, is transmitted to the Computer-Indicator Group for further processing and display.

The Inertial Navigation System supplies ownship horizontal velocity, attitude (pitch and roll) and heading (true and magnetic). This information, together with barometric altitude for vertical displacement, a reference doppler-derived velocity for accelerometer correction and true air speed, is processed in the Navigation Computer of the Computer-Indicator Group to produce, among other things, ownship present position, ground speed and ground track angle, range and bearing to destination, wind speed and direction and platform correction signals.

The Communication Subsystem has two principal aspects:

1) Communications between fleet elements.
2) Command Data link to and from the interceptors.

The multi-purpose Communications System (AN/ASQ-52 or MPC data link) provides two-way digital transmission of target data between surface units and other AEW aircraft. Transmitted target data consists of such items as:

1) Originator's identity and position.
2) 3-D target position and velocity.
3) Target Identifier
4) Target type, threat and engagement status.
5) Track quality and handover status.

The Digital Data Communications System (AN/USC-2 data link) is used to transmit guidance to all interceptors and to receive status data from interceptors capable of reply. Transmitted guidance data consists of such items as:

1) Controlled Interceptor Identifier.
2) Target slant range and target ground velocity.
3) Interceptor/target range and bearing, attack heading and time-to-go.
4) Command heading, speed and altitude, target altitude and action to be taken.

Received interceptor status data consists of such items as:

1) True Air Speed
2) Altitude
3) Heading
4) Fuel Status
5) Armament Status

The Data Processing Subsystem is a complex of computer equipment which has, as one of its principals, the Computer Indicator Group.

Target data received from the Computer-Detector is correlated (associated) with target track data stored in the Computer-Programmer to update existing tracks and to initiate new tracks.

Automatic tracking of maneuvering targets is by linear filters and unique three-dimensional adaptive gating techniques utilized in the automatic tracking unit, the special purpose digital computer of the Computer-Programmer. In addition, since both IFF and search radar video are available for tracking, friendly aircraft are tracked by IFF and beacon returns for greater positional accuracy as well as greater blip/scan ratios than are usually attainable from skin-track. To associate discrete target reports with established friend tracks, the numerics of Mode II and Mode III IFF returns are compared with the IFF code data stored in the

Computer-Programmer for friendly elements previously entered into the system. It is also determined whether tracks are friendly or unknown, and surface or airborne. Tracks are cancelled after "n" radar misses where "n" is a function of track status; i.e., whether the track is tentative or established. Tracks are also updated on the basis of reports via the AN/ASQ-52 data link. Operators monitor the automatic detection, acquisition and tracking processes and supply supplementary position data to the automatic tracking unit as required.

The Computer-Programmer continually extrapolates the position of all airborne unknown and hostile targets to determine threat potential to a previously manually-entered defended point, and to assign an appropriate threat priority index; i.e., ranks targets in order of threat. Upon establishment of the automatic threat evaluation mode, the target representing the greatest unassigned threat is made available for automatic weapon assignment and is also displayed to the operators. Manually-designated threats automatically receive the highest priority, whether in the manual or automatic threat evaluation mode.

In this operator selected mode, the greatest unassigned threat is submitted to the intercept computer for Interceptor assignment. Stored data on the available controlled interceptors is then automatically examined, and, on the basis of aerodynamic capability, fuel status, AI radar/weapon capability and time-to-go, the Computer-Programmer assigns and computes and transmits intercept instructions to the interceptor that can best counter the threat. This assignment process continues until all available interceptors have been paired with threats. Weapon assignments may be accomplished manually by the operators as an alternative procedure, in which case the operators pair available interceptors one-by-one with a selected threat and, based on the appearance of the display, manually assign one of the interceptors. This procedure is continued until all available interceptors have been assigned.

Guidance instructions are automatically and continually computed for simultaneous control of engaged interceptors. These instructions are based on an intercept computer program derived from the characteristics of weapons expected in the operational inventory. In addition, the terminal approach path is automatically computed on the basis of weapon requirements and AI radar characteristics to ensure maximum kill probability. Automatic transmission of guidance instructions to the interceptors is accomplished via the AN/USC-2 data link as well as automatic receipt of interceptor status reports from those interceptors capable of replying via AN/USC-2. Progress of each engagement may be observed on the Control-Indicator CRT displays.

Reports consisting of positional data, velocity and category, etc., on targets selected by the operators for general reporting (or handover to other AEW aircraft or to surface elements) are automatically organized by the Computer-Programmer and transmitted via the AN/ASQ-52 data link. Similarly, the system is capable of receiving target data via the AN/ASQ-52 from other elements, of correlating such reports with stored target tracks, and of tracking and displaying such targets to the operators. Status and order messages (e.g., hand-over) are also automatically received, processed and answered.

System performance is automatically monitored in flight by pre-programmed self-check routines in the Computer Programmer. These routines are performed continually, periodically or on manual initiation. Self-checking includes the automatic assessment of adequacy of performance as well as system status, as displayed on the IFPM test set for operator monitoring and decisions relating to operation in a degraded mode as required. Test targets are carried in the system (in addition to live targets) to provide continual verification of system performance. The IFPM system also provides a practical means of expediting fault isolation using only the permanently installed aircraft equipment.

Simulation of input data is of several forms. The input of simulated radar data is shown in Figure 3-11 and consists basically of range and azimuth voltages entered into the system at the point where the true aircraft sensors would pass on this same information. To simulate these inputs, two characteristics of the sensor data must be closely imitated:

1) Shape of the pulse
2) Time of arrival

The pulse shape is manufactured in either the IFF simulator and the video simulator. The time of arrival at the Computer Detector is controlled by the target generator computer. A computer of some capability is required for this function to produce a correct equivalent of the three radar returns which are normally received from a single target. The first return is direct and allows the distance computation, the second two are bounce returns. The bounce return allows the computation for target height, knowing the time lapse between returns and height of the E-2A aircraft.

The other simulated inputs are also analog computer derived and provide for inputs that would normally come from the inertial platform and from the doppler radar.

The ATDS laboratory set is capable of operating with both live and simulated interceptors being directed against either live or simulated targets. To use the cockpit simulator the flight characteristics of the type of interceptor it is "pretending" to be are programmed into the analog computers. The cockpit simulator then relates to the ATDS laboratory equipment set as indicated in Figure 3-12. The cockpit communicates with the ATDS system through the ASW-14 and the ASW-13 data link which would normally be found in an operational fleet interceptor.

Two simulation sources are associated with the Communication Subsystem and provide for two types of capability:

1) Playback of previously recorded live inputs.
2) Simulation of messages normally generated by other sources; e.g., NTDS.

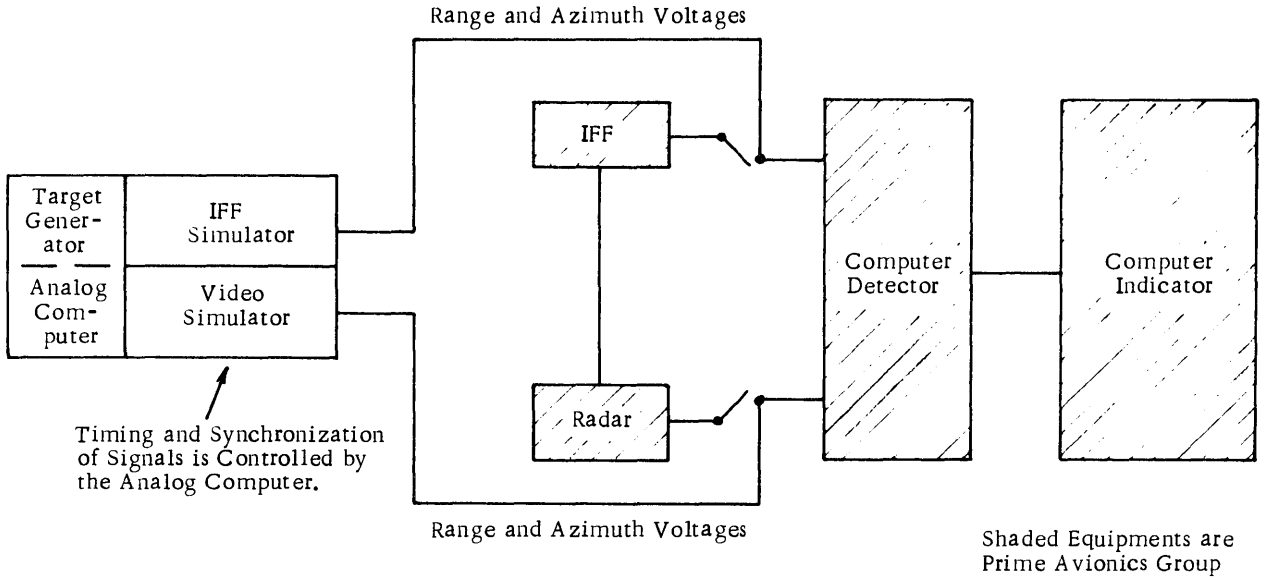

Figure 3-11

Radar Data Input Simulation

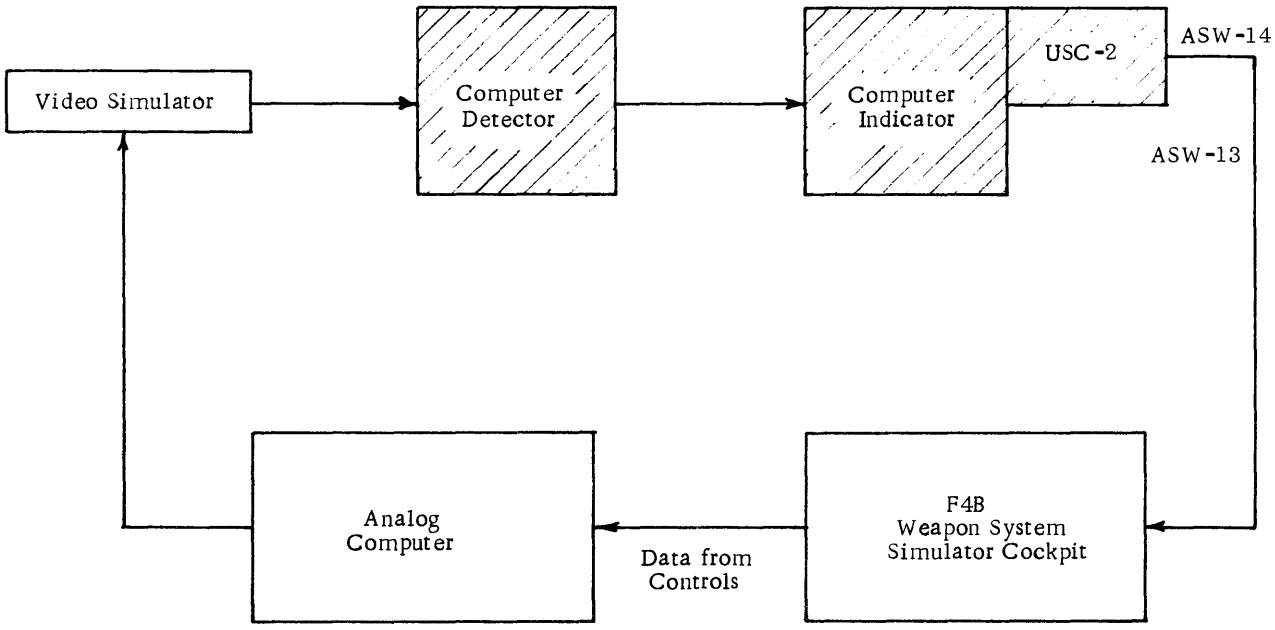

Figure 3-12

Using the Cockpit Simulator

The laboratory is able to "monitor" any sea test range operation and record any data items of value to its test series. These sets of real world data may be played back repeatedly into the system for isolation of system errors or verification of corrections made to the laboratory model of the ATDS.

3.2.6.6. Integration Tests with Companion Systems

The ATDS System is normally considered to provide a far-ranging extension to the fleet-centered NTDS. It is also possible, however, for the ATDS and MTDS (marine Tactical Data System) to communicate with one another and exchange information about tracking and other target reports. In this case, the ATDS is said to provide a seaward extension of the MTDS.

3.2.6.6.1 General Integration Effort

The Naval Missile Center has been made supervisor for conduction ground technical tests of tactical data systems. In this role, joint tests are made involving interaction with ATDS located at Point Mugu, NTDS located at Point Loma and MTDS located at Santa Ana. (See Figure 3-14).

The primary integration concern is with conducting compatibility tests between ATDS, NTDS, and MTDS to investigate interface in the following areas:

1) Language Basis
2) Language Interpretation

In the first area, the interest is syntactic and centers around the allowable symbols used by the system and the rules concerning the various symbol strings of transmission. Second, an effort is made to investigate the relative interpretations of these symbol strings. Particular emphasis is placed on investigation of possible sources of intra-system error in such as:

1) Track correlation
2) Navigation
3) Track quality measures
4) Target category assignment algorithms
5) Mathematical transforms

Verification of compatibility is made by performing joint tests with communication in pairs between the three installations. And, of course, the ultimate objective is to achieve an effectively integrated tactical data system complex.

3.2.6.6.2 Communications

The target reporting function, that is, the air-to-surface link for communication with the various tactical data systems, makes use of the Collins Kineplex ASQ-52. This unit (known as link 11) uses the Kineplex principle for parallel transfer of data. Its relation with the NTDS and MTDS is shown in Figure 3-13. This data link provides the basic intra-system communication.

An example of the usage of this link is in providing the MTDS with inputs from ATDS. In many cases, the ATDS outputs required are elementary and can be provided by an ATDS simulator. For example: to send one or two slowly changing targets to assist the MTDS in program de-bug operations does not require the ATDS, itself, to be tied up.

In particular, the ATDS/NTDS interface problem is investigated by tracking common targets and then looking at track correlation and other error sources.

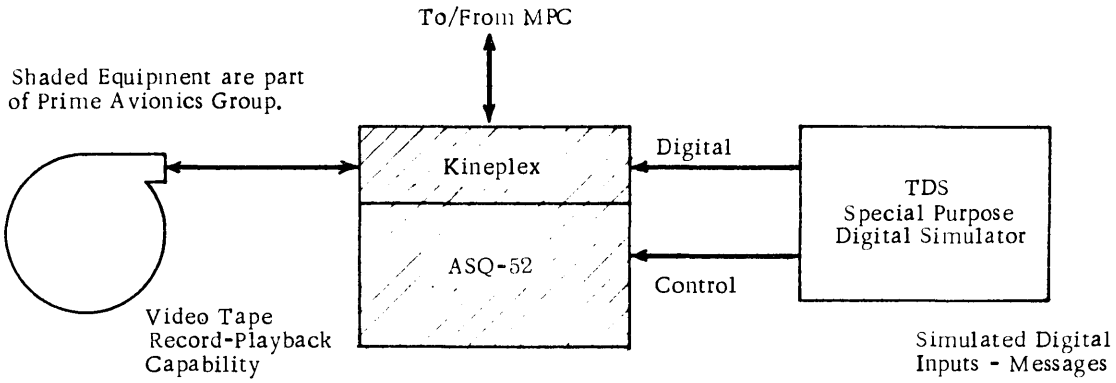

Figure 3-13

Communication Subsystem Simulation

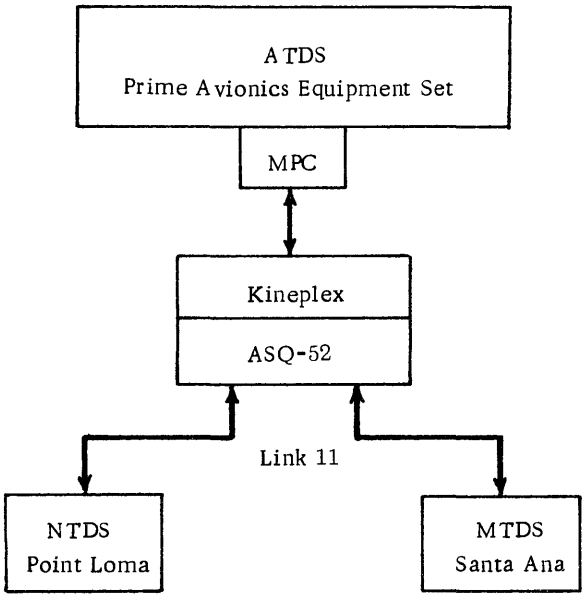

Figure 3-14

3.3 IMPLEMENTATION METHODOLOGY

3.3.1 General

This area of the study investigates some of the aspects of electronic system implementation and change of greatest interest to Naval System Planners. For convenience, the work is separated into the slightly more abstract subject of "System Change" and the slightly more concrete subject of "System Implementation." This is done with the realization that the two subjects are in practice indistinguishably intertwined.

The effort is divided as follows:

1) System Implementation Process

   a) System Design

   b) System Implementation

   c) System Specification and Documentation

   d) Naval System Implementation

      i) Who are the Naval System Planners?

      ii) What is the Naval System Planning Envisioned?

      iii) What is the Naval System Design Channel?

      iv) When and how should Fleet and USMC operational inputs be included in planning and design?

      v) What are ANTACCS' test cell requirements?

In this report material is presented from areas a) and b).

2) System Implementation Process

   a) Planning For the Evolutionary Introduction of EDP

   b) Design Change Control

c) The Naval Design Change Control Channel

d) Testing Design Changes

In this report material is presented from area a).

3.3.2 System Design

3.3.2.1 Introduction

This material is presented as a series of very short sections, each addressing an important concept in System Design, System Engineering or System Analysis. There has been no attempt made to be exhaustive in each section nor all-encompassing in the selection of subjects to be mentioned. Rather, the purpose is to touch upon many of the most important concepts in System Design, provide a general understanding of each point, and direct the reader to some little-known but very substantial references.

The subjects touched upon in this report are:

1) Systems Engineering and System Analysis
2) Engineering as Art
3) Solving the Entire Problem
4) Practice Versus Theory

Subsequent short papers will address the topics of:

1) The System Design Process
2) The Design Process for EDP Systems
3) The System Cost Concept
4) Difficulties in Evaluating Large Systems
5) The Role of Analysis in Design

3.3.2.2 System Engineering and System Analysis

System Engineering is that portion of the engineering art* which has to do with the design, production, installation, analysis and operation of those accumulations of men, procedures and equipment popularly known as systems.

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* A discussion of the "art" of engineering will follow in the next section.

It is important to fix clearly upon the concept that System Engineering treats of four main types of problems (design, production, installation, operation) and in the treatment of portions of these problems uses certain analytical techniques. In this respect it is no different from any of the older fields of the engineering art such as Mechanical, Electrical, Civil or Industrial Engineering.

The topical literature of System Engineering at times emphasizes System Analysis to the extent that it begins to seem a subject of its own, rather than an extremely valuable tool for use by system engineers. This emphasis is quite natural since analysis and analytical techniques may be thought of and taught in a stylized and orderly fashion and are therefore more easily discussed in many circles.

Analytical techniques are used by engineers in all phases of their work to evaluate as precisely as possible the complex interactions of various parts of systems, proposed systems, and changes to systems. A more thorough discussion of the role of system analysis in design will be presented in a subsequent paper.

This particular set of papers will discuss primarily the more non-numerical aspects of System Design. An over-all view of System Design, System Production (to include procurement), and System Installation will be covered in a similar set of papers entitled "System Implementation".

3.3.2.3 Engineering as an Art

This is a concept which flies in the face of much of our culture, nourished as it is by the popular press. That the concept of engineering as an art is not widely understood nor, upon occasion, even popular, has no bearing upon its truth. An understanding of the design process requires an appreciation of this concept.

It is quite likely that any confusion as to the "scientific" nature of engineering results from the popular misapprehension as to the role of mathematics and science in engineering. Much engineering practice is based upon the use of mathematics, and engineering (as an art) uses any available means to accomplish its ends, including scientific procedure or data. This tends to obscure the fact that engineering is essentially synthetic, that, although engineers use many mathematical and analytical tools, most of them spend their professional lives putting things together to make their work. How they do this is a matter of touch, style, instinct and training. For the good engineer it is also an art*.

The artistic requirements of all phases of engineering are high, but perhaps the highest requirement exists in the design phase. In this phase the engineer operates almost exclusively with concept, ideas, and relationships until most of the critical decisions are made. Only then can he see the tin being bent and the wire pulled. By the time people can "see" the product, it is usually too late to rectify mistakes by anything other than patching. Occasionally, blunders are made which cannot be fixed at all.

3.3.2.4 Solving the Entire Problem

It is self-evident that any engineering project, design or installation should solve the entire problem, but we only have to look around us to see that they do not always do so. The gantry that will not fit over its missile; the spacecraft that does not send back its TV picture, and the tactical system that can't be assembled in the dark, are all examples of a failure to solve the entire problem.

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* For an excellent discussion of the philosophy of engineering the reader should read the collected papers of Professor Hardy Cross. Engineering and Ivory Towers, Goodpasture, R. C., ed., McGraw Hill, New York, 1952.

In almost every instance these failures belong to one of the three following classes:

1) Failure to meet mission requirements
2) Failure to stay within design parameters
3) Failure to provide adequately for human contact with the system

Any of these failures may result for one of three reasons. In the first instance the customer does not know or refuses to tell (as hard as that may be to believe) adequate information about the mission, design parameters and human engineering requirements. If the engineer must guess about data he must use, then the customer must abide by the results of this guesswork. The system engineer cannot design effectively if he must work at arm's length from the customer. When the customer needs additional information about his requirements, the money invested in investigation and study is well-spent to prevent having to cope with an inadequate system.

The second reason for failure is that the customer and the system engineer do not always have the same implicit meaning to their vocabulary. "Reliability" means one thing to the system engineer in his laboratory. It means something else entirely to the electronic technician working in close quarters behind some rotating machinery. The customer and his designer must make sure that they have a firm mutual understanding of their vocabularies. Words like light-weight, flexible, expansible, reliable, etc. must have understood meanings before the designer can hope to succeed. The responsibility lies in both directions.

The third reason for failure is poor performance on the part of the system engineer, and failure of the customer to reject this poor performance. Unfortunately, not all engineers are equally good, and not all engineering errors can be found by inspection. A bridge may be a thing of beauty and structurally perfect, but if it doesn't clear the next generation of warships at high tide it is a failure as a well-done project. This type of blunder cannot often be found

by inspection. The prevention of such errors can only come from a combination of painstaking study, talented designers and an alert interested customer.

A number of expensive errors in systems may be traced to the lack of competent operational input early in the design stage by the eventual user of the system. There is some danger of this in an environment where one organization designs and buys, while another organization uses the end product. As competent as the designer and buyer may be, he cannot feel like the user does.

The system designer, the procurement agency and the actual operational user must establish a qualified informal design committee early in the design effort to ensure that the mission, the design parameters and the human engineering requirements are approximately stated and fulfilled.

3.3.2.5 Practice Versus Theory

In the practice of engineering (particularly design), there is a constant necessity to integrate various standard practices, fundamental theory, "horse-sense", and ingenuity to the end of producing the most appropriate system, structure or product for an appropriate price in an appropriate time.

The proper balance, obviously, lies between the two extremes of all theory or all field practice. We used field men with their muddy shoes and their test gear. We also require the numerical analysts. But good design is not an "either-or" proposition. We must have our designs created, not by theoreticians, nor by pragmatists, but by men with a good appreciation of both the theoretical and the practical.

As obvious as this point is, it has been overlooked in the design and implementation of many military systems. Some systems which are theoretically acceptable cannot be taken down, moved and reassembled with any degree of convenience, although they are supposed to be

mobile. The striking of this proper balance, which includes both theory and practice, is not as simple as it may seem*.

Analysis goes hand-in-hand with design, and the process of analysis must ultimately provide the designer with data of some practical impact upon the design problem at hand. The designer is not interested in the small differences between various methods, but in the calculation of a result which will be meaningful in operation in the field. The theoretical human limit of the number of interceptors one air controller can handle by voice is of little real interest if it far exceeds the radio channel capacity of the station he mans, or if all intercepts in this time period will be controlled by data link. The intellectual challenge of developing new tools or theories is thrilling, but the customer in a design contract is paying for a workable design.

During the operation of any system temporary conditions will develop such that components will operate close to or in excess of their theoretical limitation. This is particularly true of the man-machine interface. Much of the art in good system design lies in determining where these overloads can be tolerated and where we must spend the money to eliminate them. The reverse of this lies in recognizing those field conditions which reduce theoretically allowable operational loads upon equipment, operators or communication.

Another facet of system stress is that which deals with how systems are handled in the field. They are over-heated, over-cooled, dusted, moistened, bumped, jolted, etc., often far in excess of what the requirements anticipate. A good designer will allow for as much of

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* An excellent discussion of this problem is found as Chapter 1 of Design of Modern Steel Structures, Grintner, L. F., Macmillan Co., New York, 1941.

this treatment as possible and often will reduce the physical load of a certain part, slip in an extra gasket or an extra spring to protect the critical part or assembly.

Tactical systems' operating environments probably cannot be predicted with any high accuracy, and the concientious system designer will do what he can to anticipate field abuse and abnormal conditions.

Certain theoretical practices must be tempered by a great deal of judgment when designing field systems. Very large and very small parts, such as Cannon Plugs are difficult to assemble at night or with very cold hands. Certain types of patented huts or shelters may be erected only twice before critical parts fail, though theoretically (and in the sales brochures) they are satisfactory. These types of limitations upon the application of design theory to actual practice must be carefully considered by the system designer.

The extension of these remarks seems clear. Tactical Mobile Command Control Systems should be judged partially (but critically) by their susceptibility to being assembled at night in a rainstorm under blackout conditions. For exercise, one should apply this test conceptually to MTDS or ARTOC and use hungry, tired men who have been shot at seriously that same day.

3.3.3 System Implementation

3.3.3.1 General

Implementation is a very broad and ill-defined subject which deals with the problems and processes of designing, producing, testing, and installing systems. A general description of the process is applicable to the implementation of weapons systems, electronic systems, and EDP systems. However, the subject matter of the ANTACCS effort in this area is the implementation of EDP systems, and particularly those for tactical command-control systems.

Detailed preliminary analysis defined some 150 steps, decisions, processes and products involved in the implementation of command control EDP systems. The complex linkages and relationships between these steps made study and analysis quite difficult. In addition, any sort of graphic representation was unwieldy in the extreme. To discuss the area properly and build concepts correctly these 150 items were abstracted and combined into 80 major steps. These concepts are presented only graphically in this report.

Implementation is divided into seven phases according to Air Force System Command Terminology, and this terminology is used in this report. The use of this terminology is not a final choice, but some substantial portion of industry and the military is acquainted with its meaning.

Very considerable work remains to be done in the implementation area to develop and correlate concepts of particular interest to ANTACCS. It would be a simple thing to adopt AFSC-ESD-Mitre-SDC terminology en masse, but that is not the purpose of the implementation area's effort. Substantial changes will be made to this data, although it does approximately represent what must occur in the implementation of EDP systems for command control.

3.3.3.2 Discussion

The figures which follow show the implementation cycle divided into the following seven phases:

a) System Definition

b) System Design

c) Program Design

d) Program Production

e) Program Test

f) System Test

g) System Operation

The definition of these phases has long been established by custom and usage, but our only concern here is to follow the general concept of each phase and its place in the overall scheme of implementation.

An open style of notation has been used to portray the contents of each phase. This was used for two reasons which deserve mention here:

a) In nearly every phase most activities have inputs for all activities that follow in time. This makes for too much ink - that transmits too little meaning. In every system all parts are closely inter-related in many different respects. This holds true in implementation of systems.

b) Arrows and lines convey the impression that the data shown is accurate or final or that it <u>should</u> be related in the manner demonstrated. This is not the case here.

Events progress in time from left to right. Events stacked top to bottom take place about the same time, although one or more blocks can move right or left in any phase - and in actuality do so when real systems are implemented.

System Definition Phase (Figure 3-15):

This activity is concerned with finding out what the problem is and what the resources are that may be applied to its solution. This is not the same phase as Mr. McNamara's Program Definition Phase. After requirements are defined, a System Manager is appointed and he sees that the overall system requirements are further defined according to the various subsystems to be used.

System Design Phase (Figure 3-16):

This phase begins with selection of sources. It defines schedules and quality criteria. During this phase, the Operational System Description is prepared, evaluated and concurred upon. Changes to the OSD are reflected by changes to the System Requirements.

Program Design Phase (Figures 3-17, 3-18):

This phase is shown on two figures. The phase begins with comprehensive agreement upon computer, hardware and software design constants and details. Work is commenced on the overhead computer facility. The program system design is set, and comprehensive plans are begun for over-all system testing. Whatever work required on program conventions and standards is done, and the data base is designed.

As the phase continues, the EAM support facility is begun, the program system design is evaluated, and the collection of data base information is begun. At about the half-way point of the phase, EAM operating procedures are set, and the procedures for processing program design changes are established.

The planning for system testing has been continuing and now matures into defined system tests and schedules for their performance. At about this point, program design activity is initiated for operational, utility, data base, and system exercise production programs.

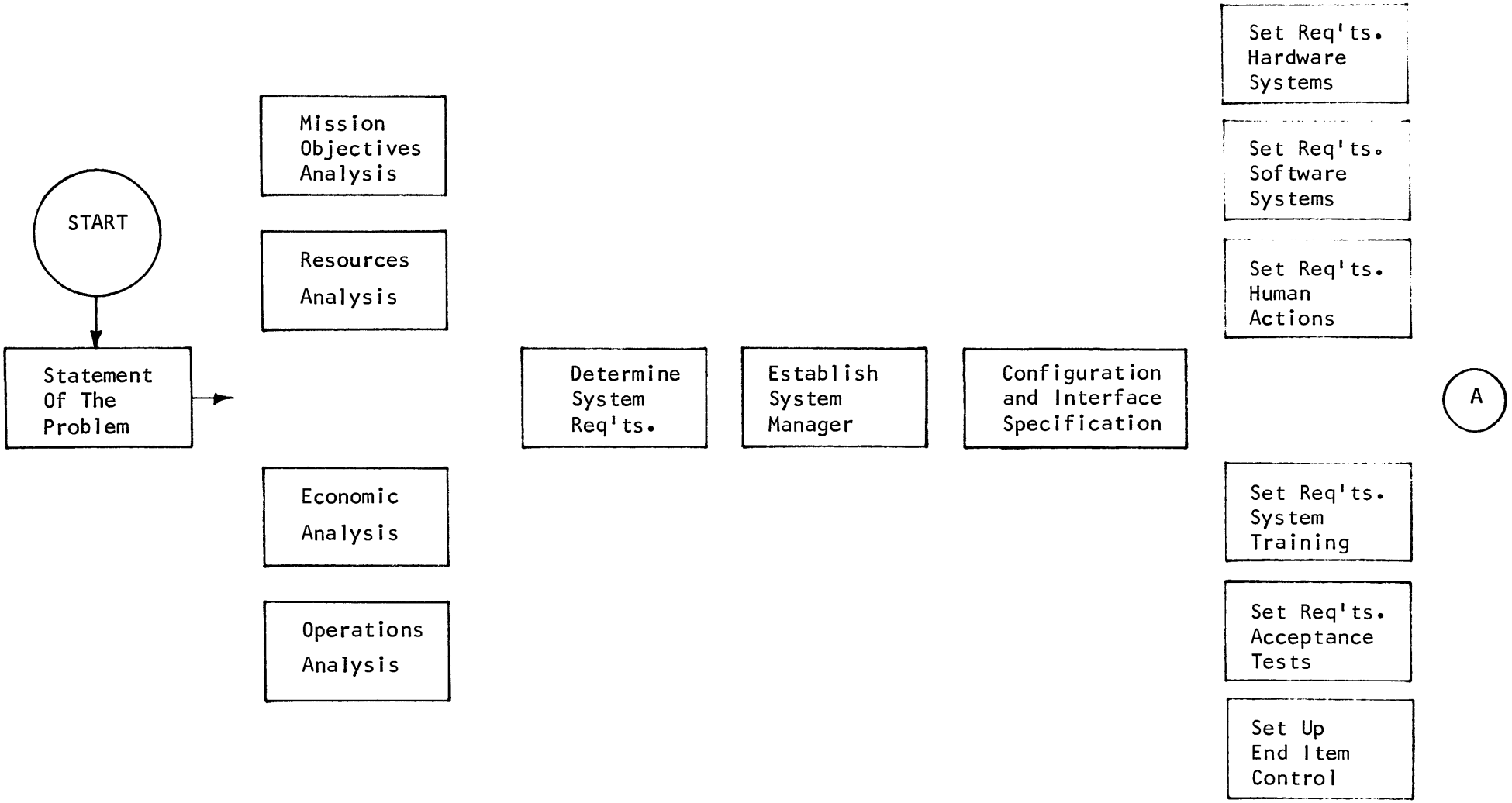


Figure 3-15

SYSTEM DEFINITION PHASE

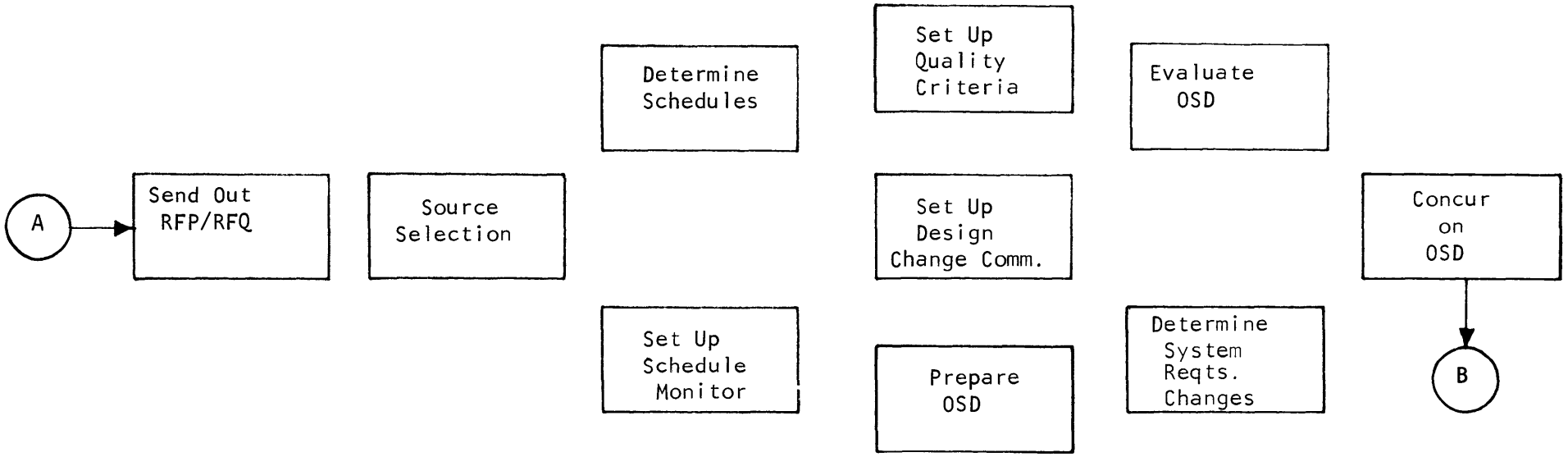


Figure 3-16 - System Design Phase

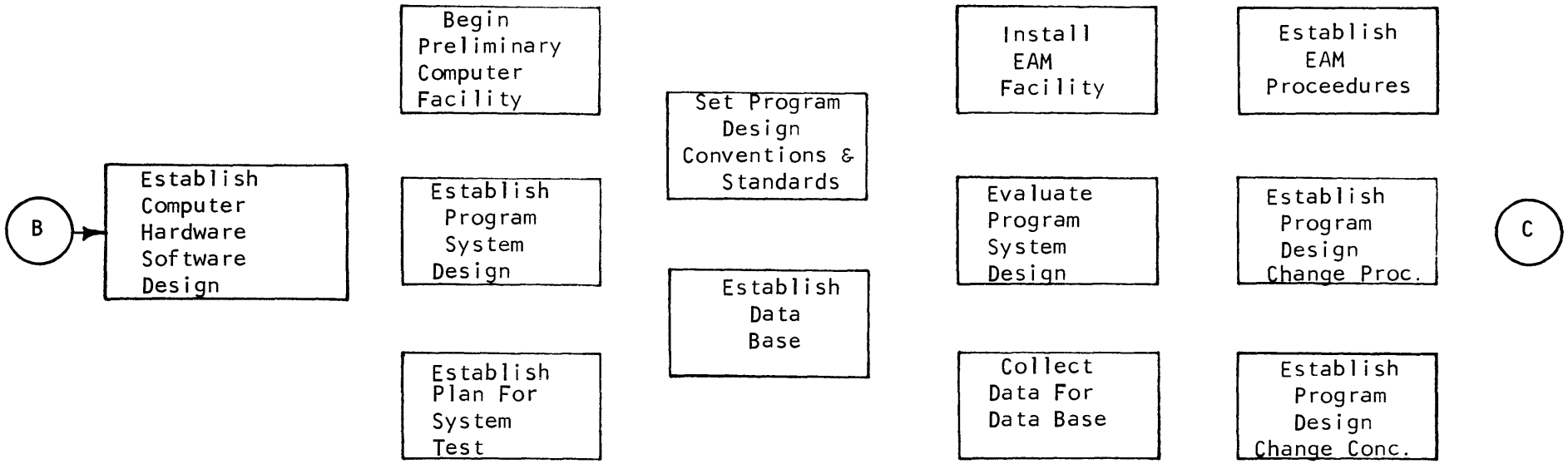


Figure 3-17 - Program Design Phase (I)

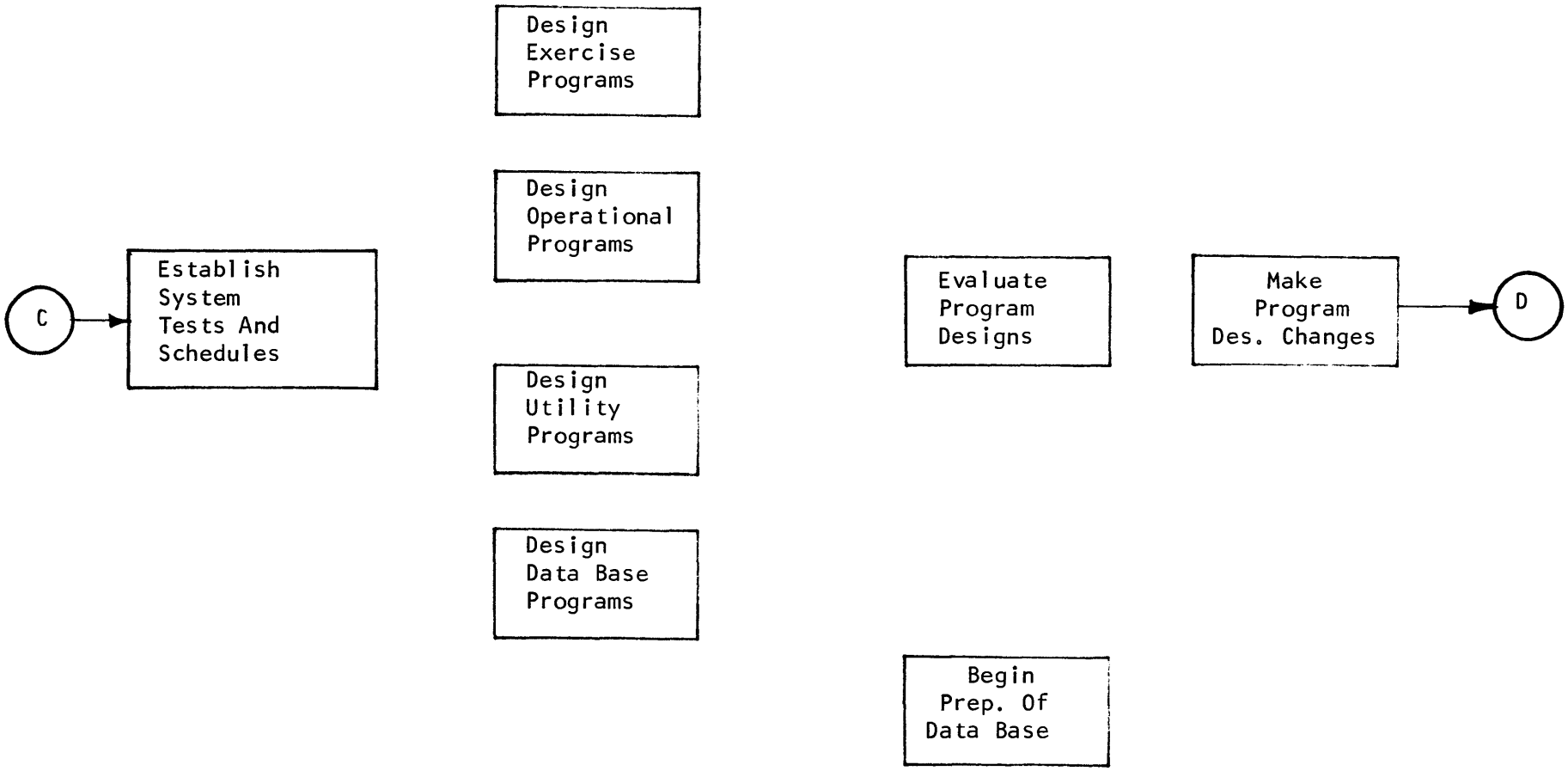


Fig. 3-18 Program Design Phase (II)

As the program design phase closes, program designs are evaluated and changed, and data base preparation begins.

Program Production Phase (Figure 3-19):

The purpose of this phase is to actually bring into being the coded computer programs. During this phase utility programs, exercise programs, data base programs, facility programs, and operational programs are all coded. The computer is delivered shortly after the beginning of this phase and is made available as soon as possible. Standardized assembly tests are designed in preparation for the next phase, and system test design is begun.

Program Test Phase (Figure 3-20):

In this phase all five families of programs are parameter, assembly and system tested. Operational system test materials are prepared.

System Test Phase (Figure 3-21):

In this phase the data base is loaded and the exercise generation program is system tested. The entire operational system (including procedures and hardware) is tested. Following operational system testing, the customer (either the purchaser, the user, or both) performs acceptance tests.

System Operation Phase (Figure 3-22):

After acceptance testing, the user puts the system "on-line" and begins to accumulate the experience and data which will enable him to plan for changes to his system.

Comment:

This approach to EDP system implementation is quite complex (in its detail) and organizationally has been made quite monolithic. There has been some question as to its slow reaction time and high cost. Still,

it has produced large-scale working EDP systems on time for AFSC. While most of these functions must be accomplished in some manner, this discussion should not be considered a recommendation for precisely this approach for all new systems, particularly those for ANTACCS.

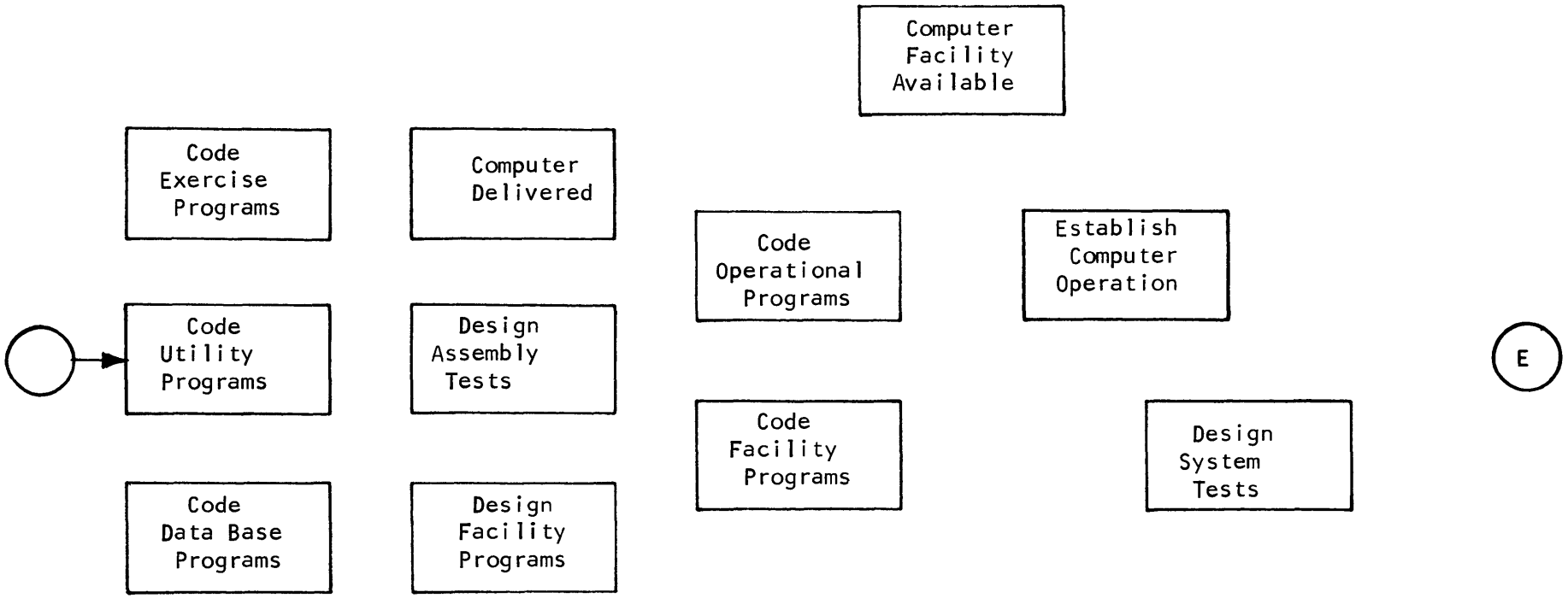


Figure 3-19 - Program Production Phase

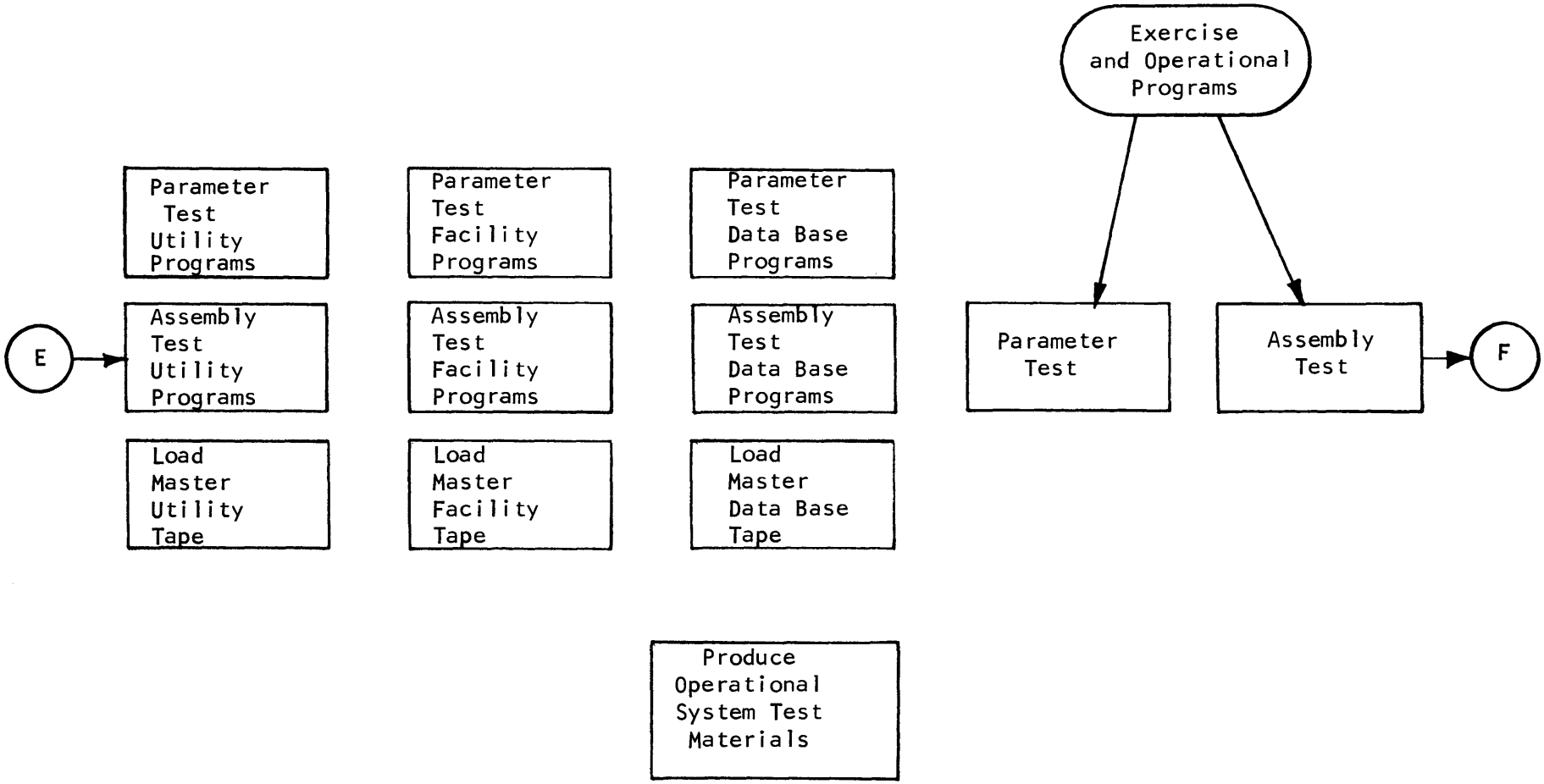


Figure 3.20 - Program Test Phase

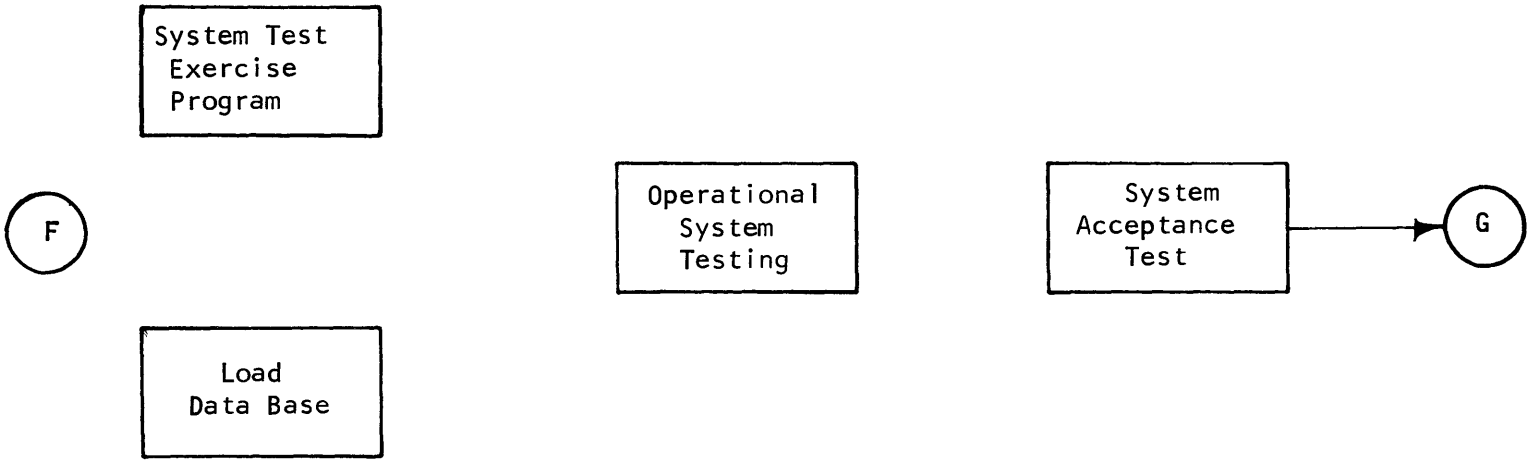
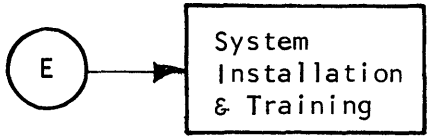
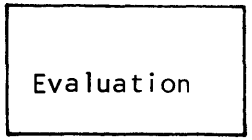


Figure 3-21

System Test Phase





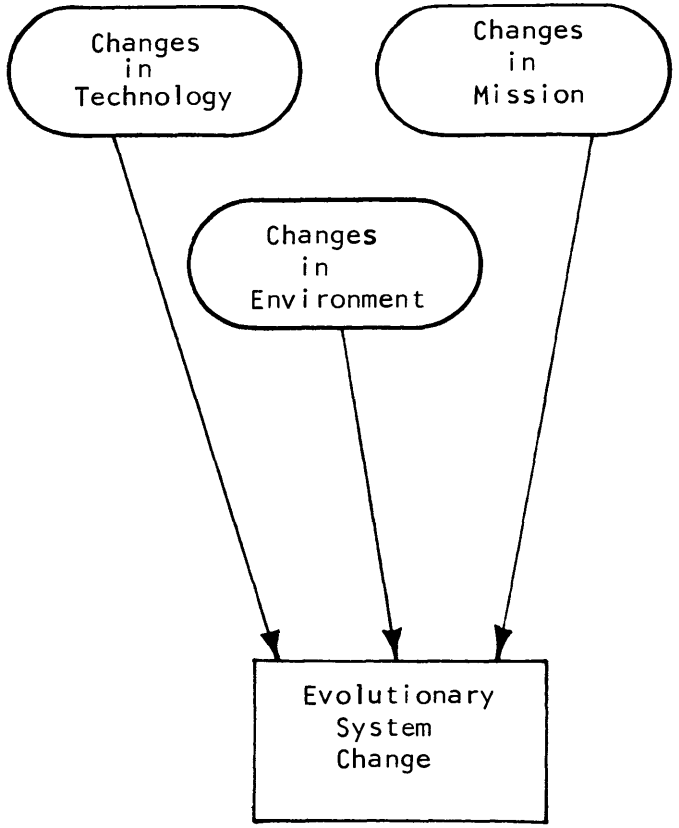


Figure 3-22

System Operation Phase

3.3.4 Planning For the Evolutionary Introduction of EDP

3.3.4.1 General

The general trend of system planning has become one of evolution in the past few years. This is particularly true for those systems which lend EDP support of any sort to the commander while he executes his command task. This is primarily true since command tasks are so complex that it is hard to define completely what help the commander really needs, and it is then often difficult to develop those EDP tools and facilities which provide that command assistance.

Not only is the evolutionary approach appropriate for the initial design and installation of systems, it is also most appropriate for the introduction of improvements to existing systems. Both the SAGE system which was abruptly revolutionarily installed, and the NMCSSC which was very evolutionarily developed now incorporate changes by an evolutionary process similar to the one described below.

This section presents a relatively complete description of the evolutionary process and how any command or headquarters may begin to plan for the evolutionary introduction of EDP assistance for command function. The same evolutionary planning may be applied to the entire system for those systems with large non-EDP sub-systems.

3.3.4.2 Description

The planning of an evolutionary process for introducting EDP into a command organization is unique. For identifying the process as evolutionary emphasizes that EDP development will be dominated by uncertainty. We cannot anticipate sufficiently how the problems will change, how commanders and their staffs will profit or suffer from automated assistance, how the organization will be restructured or gain new tasks, or modify its scope. These are a few of the unknowns.

On the other hand, when we demand planning, we commit ourselves to some understanding of the future, to identification of a range of plausible and implausible goals, and to the need to decide early on long lead-time items such as facility space, hardware funding and procurement, and areas for further research. Accordingly, planning for evolution is a process of attempting to ensure an appropriate capability for growth without disrupting current capabilities; but also without foreclosing on future capabilities (either by being too specific too early or, equally dangerous, by not undertaking some specific activities early enough.)

Accordingly, an EDP evolutionary plan handles different problems in different ways. In some cases it establishes an organization for attacking the problems without anticipating what the specific solutions will be. In these cases, the key questions are the size and nature of the supporting organizations, their interrelationships, and the procedures for applying and evaluating their efforts. In other cases, the planning process must recognize long lead-time implementation choices. Although it attempts to delay, as much as possible, the time when these decisions are made, excessive delay will impede future progress; accordingly, the time selected for making these decisions must consider trade-offs between uncertainty and delay. Finally, the initial plan must anticipate the continual need for replanning. It can only do this if it projects assumptions, milestones, and expected measures of performance. Over time, these assumptions prove valid or invalid, schedules are bettered or missed, progress is greater or less. A good plan will suggest when replanning is called for and, possibly, even the nature of the corrective action.

Probably the most difficult problems which will need to be faced in the initial EDP planning is the first area discussed above, that is, the organizational arrangements for evolving EDP. Before discussing a possible outline for an EDP Plan, it might be useful to mention some

of the issues that must be considered in organizing for the EDP support of an operating command. It is more illuminating to do this in the context of a specific arrangement.

Evolutionary implementation involves a three-stage development process. In the first stage, short range improvements are made to current operational capability and to exercising and evaluation capability. The lead-time from identification of a needed improvement to its incorporation in current capabilities is less than six months. (By incorporation in current capabilities we mean that the indicated improvement has at least reached the stage of development and testing that it can be run in parallel with current operational capabilities.)

In the second stage, medium range improvements are developed and evaluated where these improvements are expected to need a three month to two year lead-time before they become operational. An "experimental operations" capability and associated experimental exercise and evaluation capabilities are maintained to stimulate ideas for medium range improvements and to provide a test-bed for evaluating these improvements.

In the third stage, an analytic and experimental center is operated whose concerns and tools are at a much more abstract level than those used in the centers in the first two stages. The outputs of this third center assist all agencies in planning and analyzing requirements and designs. Certain major EDP techniques may be shown to be tentatively feasible and ready for further development and experimentation in the second stage. Also, a development program in EDP technical tools is conducted as a part of this stage. The third stage looks as much as five years into the future and none of its developments would likely be operational in less than a year (and then only if they were expedited with highest priority through the second and first stages). In support of these three stages, EDP functional design, program design and

implementation activities specify and develop the short and medium range improvements, and the experimental models.

In planning the allocation of resources to these various activities, it is essential to remember that this organization is intended to provide an almost continuous flow of products and data. For example, the activity "experimental operations" receives EDP programs and procedures from two sources; by operating on these it rejects some products, modifies others, passes them on to current operations, and develops data for evaluation and further design.

If resources are not properly allocated among the various stages and activities, serious bottlenecks or gaps can occur. For example, if relatively inadequate resources are provided to experimental operations, then it will not have the capability to develop and evaluate the medium range improvements and inputs from analytic operations. Something will have to give. The rate of absorbing new techniques from analytic operations may be sharply curtailed so that this latter activity is providing only marginal improvements to the system. The analysis and verification of medium range improvements may not be adequately performed so that a higher than appropriate flow of unvalidated techniques is passed on to current operations. Finally, such high standards for validation may be maintained that the flow of products to current operations becomes very small, and as a result, the entire developmental effort is providing few operational improvements. Fortunately, such a multi-stage development process is partially self-adapting so that a somewhat balanced flow of products and design data is achieved. A major role of EDP planning is to monitor the flow of products through these diverse activities and to adjust the allocation of resources and the interrelationship between the activities so that a reasonably efficient and appropriate development organization is achieved.

Accordingly, an initial plan for this development organization would have to consider such questions as:

1) What resources should be allocated to each stage?

2) What relative emphasis should be placed on design and development versus exercising and evaluation?

3) Can some of the same facilities be used for both current operations and experimental operations?

4) What types of experience are required to perform each of the activities: user, user representatives, analyst, data processing designers, etc? In managing them? In planning for them? In monitoring them?

5) How can operational needs be made to guide the development of technical tools? To what extent are these tools operationally substantive (e.g., planning models) versus general (e.g., executive systems), versus operational (e.g., artillery fire support systems.)

6) What documents are required to describe plans, needs, products, evaluations and tools?

Although these questions have been posed with respect to the three stage development mechanism depicted in the attached figure, they will also have to be addressed in the EDP Plan. The plan must also consider these additional (and possibly more difficult questions):

1) How many stages does the user need in the development process?

2) What is the lead-time for the various stages?

3) What is the role of present agencies in the proposed mechanism?

4) New documents will have to be designed, and responsibility for producing these documents assigned. What is the relationship of present documents such as Technical Development Plans and Fiscal Year Functional Requirements to these new documents?

3.3.4.3 Contents of the Plan

The EDP Plan should address the following areas:

1) Goals and phasing objectives for EDP.

2) Organization and activities for EDP Development.

3) Measures for Change, Allocation and Planning.

4) Current and Imminent Progress.

5) Software Development.

6) Hardware Planning and Procurement.

7) Problem Areas.

8) Proposed Activities.

9) Plan Modification.

A brief discussion of the contents of each area follows:

1) Goals and Phasing for EDP. To what extent, over time, will EDP support be required in ANTACCS to serve operations, intelligence, logistics, communications, gaming, and planning? To what extent, over time, can the data bases and processing routines in support of these functions be integrated? What other developments will be taking place during the coming five or so years which will have a major effect on the role of EDP support? What functional needs should guide early development activities? Given significant alternate long range configurations, what intermediate milestones would

would have to be achieved to attain each long range goal? What critical decision points exist over time in selecting between alternate configurations?

2) Organization and Activities for EDP Development. How many stages should be planned, over time, for developing ANTACCS EDP? What is the relationship between these various stages? What documents and other products must be generated in performing each of these functions? What agencies are responsible for originating, reviewing, coordinating and approving the various documents?

3) Measures for Change, Allocation and Planning. What quantitative measures can be applied in planning or reviewing the growth or change of EDP support? What are present planning factors for supporting resources (including various types of personnel) needed to achieve the above measures? What guidelines exist for allocating resources devoted to current operations, current exercises and evaluation, analyses of potential improvements, operational specification of EDP functions, computer program design and implementation, development of exercise and evaluation support and tools, maintenance of EDP systems (including minor modification), and development of utility systems?

4) Current and Imminent Progress. What is the current manning, experience and history of the various units using tactical EDP in the Navy? What EDP capabilities are currently operational? What EDP developments are scheduled for early operation? What are the current relationships between the various services using and developing tactical EDP? How do present accomplishments compare with past plans and why?

5) Software Development. How much and what research and development in software tools should be sponsored by the Navy? How would these research and development activities be related to non-Navy R&D in this area? What developments can be undertaken which are not operationally specific; for example, executive programs, time sharing systems, query languages, data base management systems, modeling ideas, etc? What user or operational guidance is required in initiating such efforts and in subsequently monitoring their development? When might significant new developments be ready for incorporation in experimental or operational EDP systems? What steps must be undertaken to ensure that such new capabilities can be introduced into experimental or operational systems with minimum disruption?

6) Hardware Planning and Procurement. How should the procurement of improved data processing, display, communications and input devices be programmed? What constraints does the normal programming cycle impose on procurement of these improved capabilities? Should the programming cycle be somewhat modified to facilitate the timely procurement of both major and minor hardware improvements? At the time of initial installation, how much processing capability should be reserved to facilitate growth over time?

7) Problem Areas. In preparing any plan, the planning process generally illuminates problem areas or uncertainties which fall outside the scope of the planning group or which cannot be resolved during the planning cycle. What are these areas? What specific issues and alternatives are involved? How does the plan cope with these problems? (How soon does it assume they will be resolved? Does it inhibit certain specific resolutions?) Can the EDP planning activity propose a means of resolving some of these problems?

8) Proposed Activities. In light of the above, what changes are recommended to present plans including changes in organizational relationships, procurement specifications and schedules, and level of supporting resources?

9) Plan Modification. How should the initial plan be revised? By whom? With what coordination and concurrence procedures? How often?

A number of these planning questions are within the scope of the current ANTACCS and MTACCS efforts. Others remain to be answered as the Navy develops more information about its future operations, the threat and the technology. It is interesting to note, and sometimes a little confusing to be faced with the similarity between the Total System Algorithm and the EDP System Algorithm. They are quite similar in most respects. Subsequent reports will show in detail how these two processes are related.

3.4 SPECIFIC METHODOLOGY

This area is concerned with the investigation of a few pressing design problems, primarily those in which the designer is faced with making choices among alternatives. Very little effort has been expended in this area so far. The effort is scheduled to be directed as follows:

1) Storage and Transmission of Data

2) The Assignment of Tasks - Man or Machine

3) Special Purpose vs General Purpose Displays

4) The Organization of Information Processing

5) Quantitative Design Tools

One paper is presented here on Quantitative Design Tools.

3.4.1 Quantitative Design Tools

This section will eventually consist of a few papers, not necessarily closely related to each other, but each relating to subject matter of high interest to the System Planner or System Manager. This particular paper shows one technique which is of value to system planners in evaluating the capability of various computing central processes at early stages of design or planning.

3.4.2 The Calculation of Figures of Merit For The Comparison of Digital Computers

3.4.2.1 Abstract and Summary

This paper discusses the theory, construction and application of the Figure of Merit technique for the evaluation of contemporary computer system's central computers and high speed memories. Four currently available methods are presented and analyzed (Class Method, Information Channel Capacity Method, Efficiency Index, and Babbage Method). A new method is presented (Highland Method) which avoids many of the shortcomings of previously used Figure of Merit Methods.

3.4.2.2 Introductory

This paper discusses several approaches to determining arbitrary numerical measures for comparing the "computing capability" of electronic

digital computers. Measures of this nature are often called "Figures of Merit". The measures discussed here, and others like them, consider only the "main frame" and high speed memory capability of the computer being examined. That is, they consider only the size of high-speed memory, the speed with which data is transferred into the computer from memory, and the speed of computation.

Since one of the crucial limitations of modern data processing equipment is often input-output capability, these "Figures of Merit" approaches clearly leave much to be desired. However, we must bear in mind that normally the purpose of computer installations is not to perform input-output functions but to manipulate data. Regardless of I/O (input-output) limitations, this work is done by the central computer, and figures of merit have real value in the comparison of central computer capability without regard to type of computer or the application for which the computer is used.

To complete any worthwhile analysis, considerations such as instruction repertoire, I/O capability, amount and type of low speed storage, mean time between failures, mean time to repair, etc. must be studied analytically. Nevertheless, figures of merit offer substantial advantage to the system analyst who understands their rationale and limitations, and who confines their use to "rough-cut" first approximations.*

3.4.2.3 Rationale

There are two distinct general approaches to measuring the capabilities of computing machinery. Only one of these (the figure of merit) is discussed in this paper. To understand this one technique fully it is necessary to understand the other (the "bench-mark" technique) to a limited degree.

* An unpublished paper by Mr. Ronald W. Rector is acknowledged. In this paper (Measuring the "Capability" of Computing Equipment) he cites a number of figure of merit techniques. A part of this paper draws upon these.

1) The Bench Mark Technique

This approach to measuring computer capability is problem oriented. That is, machines are evaluated on their ability to perform certain problems or selected parts of the total task proposed. These problems may be entire real problems, parts of real problems or synthetic problems made to resemble real problems closely. This technique is called the "bench-mark" method since it compares machines by examining their differential capability (normally speed) to perform the same "benchmark" problem.

The bench-mark technique (if carefully executed) can be quite accurate, but it is very costly in talent and time, and requires an accurate and precise definition of the total task to be performed. In addition, any bench mark problem which is not the complete task ultimately to be demanded of the computer takes on certain aspects of simulation and is subject to many of the limitations of simulation.

2) The Figure of Merit

This approach attempts to evaluate the capability of an individual machine without regard to how that capability will be used. This is much the same thing as a power station being given a kilowatt rating without regard to how much electricity is used or how it is used. At first, this may seem a little foolish since the only reasonable purpose of computers is to solve real problems. However, system planners find it very useful to be able to think of and measure main frame and memory capability in the abstract. Figures of merit permit them to do this.

Figures of merit may be used to provide preliminary answers to a number of problems without the need to prepare a bench mark analysis. Among these problems are questions such as:

1) I am now processing data at rate R. My work load will increase to about 7R. What various machines should I consider acquiring?

2) My old machine needs to be replaced. What will I have to pay for a new machine, and how much capability could I have left for expansion? This is really a new statement of question #1.

3) Company A charges $5,000 per month for machine 1. Company B charges $7,500 for machine 2. Is the difference worthwhile in terms of data processing?

4) The new system I am planning should have the computing load of about half that of System X, which uses a CDC 6600 at about full capacity. Allowing for 20% expansion what machines should I think of for my system? I plan to split the computing load among four computers, A, B, C, and D.
$B = \frac{A}{2}$ and $C = \frac{A}{3}$

These and other important questions of a preliminary planning and design nature can be answered by using some figure of merit technique.

The entire figure of merit approach is based upon the premise that "more" is "better". The question "Is 10% more also 10% better?" will be discussed later. The more fundamental question "More what?" is answered (depending upon what figure of merit we consider) by "more internal speed", "more high speed memory" or some combination of both. How these qualities are juggled or combined differs from case to case and is discussed by individual case.

In general, we can say that more speed is better in direct proportion to the increase. That is, a four-fold increase in speed is four times "better", and a six-fold increase is six times "better". Another way of looking at this is, a machine which can do work in four hours that was previously done in eight is twice as beneficial to the user. This is particularly true of machines used "on-line".

Considering the usefulness of high speed memory to a user, we can say that more is better, but <u>not</u> in direct proportion to the increase.

That is, to go from a size of 500,000 bits to 1,000,000 bits is more beneficial to the user than to go from 1,000,000 bits to 2,000,000 bits - even though the increase is by the same factor.

There is however some difference in opinion as to how much the worth of memory changes as size of memory grows larger. The manner in which the incremental utility of larger memories decreases is generally felt to be logarithmic (or some function so close to logarithmic that the difference is not worth worrying about). Remember we are searching for some numerical way to express professional opinion, so accuracy is greatly to be preferred to precision. Accuracy is faithfulness of conceptual replication, while precision refers to the degree of refinement of the measurement. It is easy to have one without the other, but precision without accuracy is misleading, at best, while accuracy without precision is often very useful.

For some applications, perhaps one such as message switching, memory requirements may be thought of as absolute. That is, the high-speed memory must be big enough to do the job - but size increments beyond that point are of little use. For these applications, and those where time constraints are severe, more attention should be paid to the efficiency of the computation process than is normally done.

With this introduction to the rationale of figure of merit, we may proceed to the technical discussion of several types of figures or merit, their applications and shortcomings.

3.4.2.4 The "Classic Method"

Rector [1] has applied the name to this method, and while it may not be "classic" in the most pristine sense of the word, the method has been applied in much of the literature. The calculation is a simple one:

$$\text{Class Figure of Merit (CFM)} = \log_{10} \frac{M}{T}$$

Where M = High speed memory capacity in bits
and T = Access time is seconds

Various forms of memory arrangement must be converted to give a total reading in bits. Sign bits and parity bits should not be included.

Access time is the time required to fetch a word (or character or set of characters) from memory. In destructive-readout memory machines the data cannot be operated upon until that small portion of memory is restored with the data just read out destructively. This takes one more memory access time. The two times together are called a memory cycle. Most data are given in cycle time and must be divided by two. However, in non-destructive memory machines operations begin immediately after access time.

Since most tabular data presents the time in microseconds (The Adams Chart, for instance) it is most convenient to use, and subsequent calculations in this paper will use, microseconds. Since there is no standard, we can use what we wish, but microseconds are more widely used and more convenient.

By using this method, we can calculate the CFM for many storage and access cevices, not just computers alone. Some values calculated in this manner are shown in Table 3-1.

TABLE 3-1 CLASSIC FIGURE OF MERIT

	Max. Wds.	Bits/Wd	Total Bits	Storage Cycle Time (in musecs)	$\frac{\text{Cycle Time}}{2}$	$\frac{\text{Bits}}{\text{Access}}$	$\text{Log}_{10} \frac{\text{Bits}}{\text{Access}}$
CDC 6600	262 K	60	15,720,000	0.7	0.35	44,910,000	7.6523
IBM 7030	262K	64	16,768,000	2.2	1.10	15,240,000	7.1829
Hughes H-330	181K	48	6,288,000	1.8	0.90	6,969,000	6.8432
Philco 212	65K	48	3,120,000	1.8	0.75	4,160,000	6.6191
RCA 601	32K	56	1,792,000	1.5	0.75	2,389,000	6.3783
Univac 1107	65K	36	3,340,000	4.0	2.00	1,170,000	6.0682
SDS 9300	32K	24	768,000	1.75	0.87	882,800	5.9459
CDC G-20	32K	32	1,024,000	6	3.00	341,300	5.5332
Packard 8.440	23K	24	672,000	5	2.50	269,900	5.4313
CDC 160A	32K	12	384,000	6.4	3.20	120,000	5.0792
SDS 910	16K	24	384,000	8	4.00	96,000	4.9823

Basic Data From Adams (Nov., 1963)

Several points must be completely understood by the system planner contemplating the use of measures such as this one. These are:

1) The logarithmic nature of the CFM number.
2) The equal treatment of memory and speed increases.
3) The implicit relationship of computation speed and access time.

The CFM is, by definition, the logarithm of a decimal number. Its being logarithmic has several implications for a user.

The human mind apparently thinks in linear terms as a normal course of events. Even when presented with a table and the certain knowledge that the CFM is a logarithm, it somehow seems more real to think of terms varying from 100,000 to 45,000,000 than from 4.9 to 7.6. Our world of experience is linear, and dealing with logarithms can be quite illusory for those not on guard.

Therefore, when we look at Table 3-1 we may note casually that the 910 is 4.9+ and the 6600 is 7.6+. This would mean to many persons that two 910's are a little better than one 6600. Of course this is not true, and the error comes from treating logarithms as decimal numbers. In reality, the table tells us that the capability of the 6600 is three decimal places greather than the capability of the 910. And that says that the 6600 is between 100 and 1,000 times as powerful as a 910.

This is useful information, but it cannot be said that it is intuitively obvious, as good as the 6600 is. It would have to be worked out very carefully and for a particular example. We find, then, that direct comparisons between the very high and very low ratings on the scale may be open to some question. It is also open to question as to how meaningful this 1,000 to 1 ratio could be even if it were quite accurate.

The illusory nature of logarithms and the seeming abnormal compression of the scale should be looked at again. This time look at three computers clumped at the center:

Hughes 330	CFM = 6.8432
RCA 601	CFM = 6.3783
Univac 1107	CFM = 6.0682

These machines appear to be very close together in capability, particularly since they have the same first digit in their CFM. One might imagine that they are indistinguishably close. By reference to column A we see that the quotients prior to the taking of the logarithm lie in the relationship of 6.9: 2.4: 1.2. This is a considerable difference, indeed, and it is in adjacent areas of this long table that comparisons of CFM's have a great deal of usefulness and reasonable credibility.

We have just backed into three fundamentals of logarithmic tables which must be thoroughly understood by any system planner who uses the CFM technique.

1) Logarithmic representations must be used to place extremely large numbers and very small ones in the same table conveniently, and to allow these numbers to be manipulated pleasantly.

2) The use of logarithms obscures the true linear relationships of many types of data, and can simulate logical errors by all but the most cautious users of these types of tabular data.

3) Arithmetic operations must be performed upon the Antilog of the CFM <u>not</u> the CFM itself, that is, the quotient before the $\log_{10}$ is obtained.

Using the data in Table 3-1 we will solve problem 4 in Section 3.4.2.3. This will crystallize the points discussed so far.

The proposed system will have a load of about one half of System X which uses a CDC 6600 to about full capacity. Allow for 20% expansion. Use four machines A, B, C, and C, with $B = \frac{A}{2}$ and $C = \frac{A}{3}$. We will confine ourselves to machines from Table 3-1.

CDC 6600	CFM = 7.6523	(1)
Antilog_{10}	7.6523 = 44,910,000	(2)
$\frac{44,910,000}{2}$	= 22,455,000	(3)
120% x 22,455,000	= 26,946,000	(4)

We intend to split the load derived in (4) among four machines. The load must be allocated 6/13 to A, 3/13 to B, 2/13 to C and 2/13 to C.

$$\frac{26,946,000}{13} = 2,072,769 \quad (5)$$

$$A = 6 \times 2,027,769 = 12,166,614 \quad (6)$$

$$B = 3 \times 2,027,769 = 6,083,307 \quad (7)$$

$$C = 2 \times 2,027,769 = 4,055,538 \quad (8)$$

$$\log_{10} 12,166,614 = 7.0853 = CFM_A \quad (9)$$

$$\log_{10} 6,083,307 = 6.7841 = CFM_B \quad (10)$$

$$\log_{10} 4,055,538 = 6.6580 = CFM_C \quad (11)$$

From (9) we see that a smaller than maximum size 7030 will do well for machine A. From (10) we see that an H-330 is close to exactly right for machine B, and from (11) we see that the 212 should be used for machine C.

The outstanding shortcoming of the Classic Figure of Merit is that it treats increments in storage as being equally beneficial.

Let us state the CFM equation again:

$$CFM = \log_{10} \frac{(\text{High speed storage in Bits})}{(\text{Access Time in Microsecs.})}$$

The logarithm_{10} does not apply to either the numerator or the denominator, but to the quotient, and therefore treats increases in speed and increases in memory as equally beneficial. For speed this is desirable. For memory size this is not really acceptable.

The worth of machines is often estimated by specialists to look something like

$$\text{Merit} = \frac{\log_x (\text{high speed storage in bits})}{\text{access time in microseconds}}$$

This expression satisfies much of the discussion here and something like it will be treated later.

In the Classic Figure of Merit and in some others, the only computer speed considered is cycle or access time. In destructive readout machines, cycle time equals two access times. Most instructions also require integral numbers of access times for their execution. This is because internal speeds are governed by a clock (in synchronous machines) and hence by how fast that clock will permit instructions to be executed.

Normally, the fastest tasks of logical testing or shifting control unconditionally will occupy one access time, and more complex instructions more integral units of access time. Thus, a reasonable approximation of the internal processing speed may be had by looking at access time. However, for a really accurate estimate of the internal computational speed of any machine, reference must be made to instruction time. This is treated in a subsequent section.

In asynchronous machines, front parts of each instruction may be thought of as overlapping with the final parts of preceding instructions, and therefore access time is not as reliable a measure of computation speed. Still, computation is wedded to the speed with which numbers can be shifted into and out of memory, and access time is a reasonable indicator of that speed.

When these techniques are used with non-destructive readout machines, extreme care must be taken to use access time for non-destructive machines and cycle time for destructive machines. This is because in non-destructive machines computation can begin as soon as the number is brought in, while in destructive machines one additional access time is required to restore the number to its original memory location.

In figure of merit computations, considerations other than those of the main frame, memory and some approximation of computation speed are entirely ignored. The capabilities of input/output peripheral equipment for each system must be studied in detail according to the requirements

of each system, and they are not amenable to approximation before the requirements of a system are reasonably well known. It must be remembered that some relatively slower machines have fine input/output and peripheral equipment and, thus, more than make up for their so-called "speed deficiencies".

3.4.2.5 Information Channel Capacity

Data processing machines that are used primarily for switching purposes and have memories which meet the absolute minimum required by the problem, may be compared by the use of a slightly more involed technique which treats only the internal speed of the computer.*

$$\text{Channel Capacity or } C = \frac{L}{\frac{N}{P} + T} \cdot Q$$

Where L = Word length in bits

N = Number of bits required for the execution of an operation

P = Clock rate in bits per second

T = Average wait time

Q = Number of simultaneous operations performed.

This approach does yield a good measure for the internal effectiveness of a computer used solely as an information switch. Its shortcoming is primarily that, since the approach does not consider memory requirements as other than absolute, the approach has little general application.

This method also has the disadvantage of considering word length (longer = better) without considering memory size. The result of this is two-fold. First, machines with long words come out better than machines with short words - even if they have the same number of bits in memory, which is hardly reasonable. Second, it is quite possible for a machine with the longer word to be <u>less</u> efficient (even given an equal-sized memory) than a short worded machine, for the following reasons.

* This technique was developed by Amelco, Inc. in a study performed for Douglas Aircraft as a part of the Army/Navy Instrumentation Program. <u>Data Processing, ANIP Research</u>, June 1961, Amelco, Inc.

Most command control processing, indeed much business processing, consists of setting and testing items (parts of words) not of making arithmetic computations using full words.[2,3,4] To do this, a word with many bits must be shifted or cycled a larger average number of bit positions than a word with fewer bits. This takes more time. There are machines having special logical circuitry which allows the testing and setting of a few bits without manipulating the entire word. In other than those machines, it is misleading to say "the longer the word, the better". Often this may be completely incorrect. This argument assumes the same number of bits in memory, of course.

However, the reason for including this number (L) in the computation here is: The more bits in the word, the more data can be transferred in from memory in parallel, and this is an advantage - though somewhat diluted sometimes by an increase in shifting time.

As with other figures of merit, this one does not evaluate input/output or peripheral equipment. It is included here primarily to show a good method for evaluating internal timing.

3.4.2.6 Efficiency Index

The general concept of indices of efficiency is that they measure the ability of the device examined to produce output equal to the input provided. A steam engine's efficiency is the ratio of the BTU per hour output to the BTU per hour input in fuel.

When we compute the "efficiency index" of digital computers, dollar cost is used as input in the place of BTU/hr input, and the efficiency measure is supposed to show how much "computational ability" per dollar cost is delivered by various machines.

One of the many possible manners of computing an index such as this is shown below.[5]

$$\text{Efficiency (E)} = \frac{n}{t\ Ca}$$

Where n = Number of bits per word

t = Add time + 0.01 Multiply time

Ca = Cost of arithmetic and control units

This measure has several shortcomings. Nearly any measure using the same terms will have the same disabilities, regardless of how the terms are accumulated arithmetically.

1) Using the word length alone in the numerator has the same weaknesses it had in Channel Capacity measurement.

2) Using cost in the computation of the index itself has three serious disadvantages

   a) It is very difficult to obtain the bare cost of the arithmetic unit and of the control unit by themselves for a large array of computers. Granted that it can be done for any particular computer at will - it is still a formidable task for the 75 odd computers now available in the U.S. The G.S.A. electronic supply catalog will have the prices of the pieces, but customer engineers will have to be questioned to make sure the correct set of prices is added up to produce the total cost.

   b) The total cost of the various systems is not any constant function of the arithmetic and control unit. Some computers have low priced units, others high, and any system must <u>all</u> be bought and installed to obtain whatever efficiency is inherent in the two units discussed here. It is only the whole cost of the whole system that is of any importance to us.

   c) Regardless of what cost is used, it is subject to considerable fluctuation, irrespective of what is published by G.S.A. This is true since costs are not physical constants of the machine itself, but are derived by management fiat. By using rather vague and fluctuating data in the computation, particularly in multiplication or division, the entire result is open to the most serious question. Of course, prices should be considered, but they should be considered separately from the physical constants of the machine itself.

3) The most serious consideration in this type of measurement is the use of

t = Add time + 0.01 Multiply time

Naturally, internal computational speed should be considered in evaluating any computer. The Classic Figure of Merit does this indirectly as stated earlier. In this instance, the construction of the factor t implicitly states that the programs, yet to be designed and coded, will call for two times access time instructions (like add) 100 times as often as they will call for 8, 10, 12 or more times access time instructions (such as multiply and divide). We must not interpret the construction of "t" to mean that add and multiply themselves will be most popularly used or will occur with this relative frequency, only that instructions requiring that number of access times will occur with that frequency. The consideration is this. By constructing "t" in this way we are, in effect, simulating (or guessing at) the future use of the computer. If we are close to correct in our guess, our answers will be very good indeed (barring other flaws in the computation of these indices). If we are not close to correct, our answer will be terrible.

It is desirable, however, to get a better reading of internal computational speed than is done indirectly by the CFM and this is a very reasonable way to do so. Analysts using this technique should be aware of its possible shortcomings. That there is some possibility of error should not prevent the consideration of the technique.

4) This figure of merit cannot evaluate the efficiency of the entire computational system since it cannot estimate the input/output and peripheral equipment accurately (indeed, at all) before the system is planned. This shortcoming is not peculiar to the efficiency index alone, but is shared by all figures of merit.

3.4.2.7 Babbages

C. J. Shaw of SDC has developed, but not documented, a figure of merit which avoids many of the shortcomings of those discussed previously. The numerical answer is in terms of "Babbages", a unit of measure he originated.

The Babbage rating of a computer is obtained by using the following equation:

$$B = \frac{L \log_2 M}{T}$$

Where: L = Length of word (in bits) transferred to/from memory during the access time, T

M = Total number of bits in high speed memory

T = Access time in microseconds for transferring in L bits in parallel

The introduction of the term L in the numerator as a multiplier gives a much higher rating to those machines which transfer more bits per access time. This does not mean that, all other things being equal, longer words mean better computers. It means simply that the more bits that are transferred in at each access, then the more information reaches the computer each accesss. In this respect more is better. As was stated earlier, there is a possible shortcoming here. Machines with proportionally longer words consume more time cycling and shifting data into the correct position (once it is transferred in) if they do not have some character and/or partial word logic, as well as full word logic. The consideration of this term, then, while highly desirable, is capable of producing some error if the analyst does not guard against it.

The $\log_2 M$ term in the numerator states that each successive bit of storage added to memory is 1/2 the benefit to the user of the immediately previous bit of storage. This is probably too severe a judgment upon the marginal value of increments of storage. In most discussions with programmers and systems analysts, the author has found that the feeling is:

"Each bit is almost as valuable as the preceding bit. Almost - but not quite". In all fairness to Shaw, he has admitted that incremental bits of memory were probably more valuable than 0.5 of the preceding bit, but that he chose $\log_2$ for ease of calculation. There is a mathematical way around the difficulty of using logarithms to other than the base 10 or 2. This will be shown in detail later.

There is, however, one real difficulty in the construction of Shaw's "Babbage". It is an obscure mathematical shortcoming, but one which has a tremendous effect upon the resultant rating. In the Babbage computation, the principle is applied inadvertently and is, therefore, a severe shortcoming. This will now be explained.

When the logarithm of a number is multiplied by another number, the product is the logarithm of the original number, but to a <u>new</u> base. What this new base is is determined by the number used as the multiplier. A different number - a different base. The equation governing this relationship is:

$$\log_X Y = \frac{1}{\log_{10} X} \cdot \log_{10} Y \qquad (12)$$

This means that we can handily find the logarithm of any number to any base we desire, given the presence of a table of common logarithms ($\log_{10}$). But it also means that in the Babbage computation the logarithmic base used to evaluate the size of memory varies inversely as the size of the word transferred from memory during the access time.

Stated another way, the error says that as the number of bits transferred from memory gets larger, the more valuable to the user is each succeeding bit of memory. How valuable is dependent upon what size the word is; but here are three examples:

<u>If the multiplier is:</u>	The percentage value to the user of each <u>new bit in terms of the preceding bits is</u>:
6.8	71%
12.6	83%
24.1	90%

Now it is very likely that each succeeding bit is something from 0.7 to 0.9 as valuable as the preceding bit, as discussed before. However, it is poor technique to have this value function fluctuate between computers - depending upon something else entirely. There is a method to consider word length transferred without encountering this difficulty, which is discussed later.

An interesting point is that since the log of the numerator is operated on arithmetically by the formula, the resultant Babbage reading can be manipulated arithmetically without the logarithmic difficulties mentioned in the discussion of the CFM.

The Babbage Method goes far toward providing a very useful measurement. It has produced reasonable comparisons when the result was tempered by some professional judgment. It is clearly the best Figure of Merit method developed to date. It is worthwhile, however, to examine one more attempt to provide a Figure of Merit measurement.

3.4.2.8 The Highland Method

The Highland Method of computing figures of merit has been developed by E. K. Campbell over the past two years. It represents an attempt to produce a Figure of Merit method which obviates the internal logical and mathematical difficulties which appear in those approaches mentioned previously. This method was developed in an intermittent and evolutionary fashion. It does not suffer from most of the logical and mathematical difficulties of other techniques, but is still subject to the inherent limitations of Figure of Merit.

$$HM = \frac{K \ (\log_{10} M)}{A \cdot \frac{T}{B}}$$

Where: K = Conversion Constant (see below)

M = Total Bits in High Speed Memory

A = Add Time (in microseconds)

T = Memory Access Time (in microseconds)

B = Bits Transferred in parallel during one access time

K is the constant required to change the $\log_{10} M$ to the log of M to another base depending upon what value is selected for K. Table 3-2 which follows, shows some values to use for K, depending upon what value is selected for the marginal utility of additional memory.

TABLE 3-2 VALUES OF THE MULTIPLIER 'K'

Incremental Value of Additional Bits of Memory	Value of Multiplier "K"
0.40	2.5
0.50	3.3
0.71	6.8
0.77	8.7
0.83	12.6
0.90	24.1

The use of K allows the analyst to adjust the evaluation to reflect his professional judgment as to the incremental value of memory for the application at hand. It is reasonable to believe that for most applications the value of K is somewhere in the vicinity of 0.7 to 0.9, though for some it could be much higher (or lower). The method of computing new values for K is as follows:

$$\log_X Y = \frac{1}{\log_{10} X} \cdot \log_{10} Y$$

The incremental value is $\frac{1}{X}$.

Therefore: if the incremental value of bits added to memory is to be 0.4,

Then,

$$\frac{1}{X} = 0.40$$

$$X = 2.5$$

and, from the first equation,

$$\log_{2.5} Y = \frac{1}{\log_{10} 2.5}$$

$$\log_{10} 2.5 = 0.39794$$

$$K = \frac{1}{\log_{10} 2.5} = \frac{1}{0.39794} = 2.5$$

M is the total number of data bits in memory. That is, the total number of bits excluding sign and parity bits. Log_{10} is used since tables of this function are easily obtained, and multiplier K changes $\log_{10}$ to whatever base we wish to use.

A is the add time of the machine. It is necessary to use some direct measure of instruction time since it is possible for a machine to have a fast access time and a much slower instruction time than comparable machines. Add time is used since the type of circuit logic which makes add slower or faster also makes most other instructions slower or faster. In addition, two access-time instructions are very frequently used, and add time by itself is not an unreasonable representation of computational speed.

The term $\frac{T}{B}$ is used to allow consideration of the number of bits transferred in parallel (B) in the denominator and thus avoid the difficulties involved in multiplying logarithms. T is in the denominator since a smaller time is better and this increases the size of the answer. As T is divided by B, the result grows even smaller as B increases.

$\frac{T}{B}$ is multiplied by A to remove any undue advantage which might accrue to very cheaply built machines having a very fast transfer rate and something slow like a ripple-shift add logic. In addition, any slight advantages in computational speed by one machine over another should be fairly portrayed, since it is computation and not transfer rate that gets the task accomplished.

Table 3-3 shows the machines evaluated by the Highland Method.

In the Highland method there are a number of improvements over the other methods. An examination of Table 3-3 may rock some of our preconceptions, but reference to columns M, T, A and B will show why machines are ranked as they are.

As with the Babbage, the resulting Highland number may be operated upon arithmetically for purposes of solving analytical problems. This may be done since the rating number scale, after having been both multiplied and divided, is now linear (or very close to it) instead of logarithmic.

The Highland Method measures what we wish to consider in a logical and mathematically consistent manner. The resultant ratings may be manipulated analytically. Finally, the analyst has a method for adjusting the marginal value of incremental memory to the potential user for the task at hand.

3.4.2.9 Conclusion

It must be understood that Figures of Merit have severe limitations both in their field of application and in the scope of factors which they consider. However, they are of great value to the analyst who understands them thoroughly. They can be at the same time, professionally threatening to the executive or administrator who uses them casually - - without an understanding of what they mean or measure.

There is no satisfactory way at this time to bridge the gap between having a data processing requirement and selecting the appropriate machine for it, except to perform a detailed analysis of the task at hand. This analysis will necessarily include a bench-mark analysis unless the requirements are well-known in relation to the capability of a particular computer. Only then will a Figure of Merit comparison yield any meaningful results directly. Even so, the next step is often a benchmark analysis.

The next limitation of Figures of Merit is that they necessarily cannot evaluate input/output capability or peripheral equipment configuration since these are system (or problem) oriented and cannot be adequately determined in advance of problem definition.

	Total Bits Mem. (M)	Access Time (T) Microsecs.	Bits Transferred in Parallel (B)	Add Time (A) Microsecs.	$\log_{10}M$	$K \log_{10}M$ (K = 12)	$A\frac{T}{B}$	$\frac{K \log_{10}M}{A\frac{T}{B}}$ (The Highland Rating)
CDC 6600	15,720,000	.35	60	.7	7.19645	86.3574	.00408	21,166
Philco 212	3,120,000	.75	48	.6	6.49415	77.8298	.00936	8,315
IBM 7030	16,768,000	1.10	64	1.5	7.22453	86.6944	.0256	3,386
Hughes H-330	6,288,000	.90	48	1.8	6.79851	81.5821	.0337	2,420
SDS 9300	768,000	.87	24	1.75	5.88536	70.6243	.0633	1,115
RCA 601	1,792,000	.75	56	5.7	6.25334	75.0401	.0752	997
P-B 440	672,000	2.50	24	1.0	5.82737	69.9284	.104	762
Univac 1107	2,340,000	2.00	36	4.0	6.36922	76.4306	.222	344
Univac 490	960,000	3.00	30	4.8	5.98227	71.7872	.480	149
CDC G-20	1,024,000	3.00	32	15.0	6.01030	72.1236	1.40	51.5
SDS 910	384,000	4.00	24	16.0	5.54158	66.4990	2.67	24.9
CDC 160-A	384,000	3.20	12	12.8	5.54158	66.4990	3.42	19.4

HIGHLAND METHOD FIGURE OF MERIT (With K for ~.8 Value)

TABLE 3-3

Some additional key factors which are not considered by Figure of Merit methods are; instruction repertoire, amount and type of low speed storage, mean time between failure, mean time to restore, and amount of memory cycle overlap. These factors must all be carefully weighed in any complete analysis.

Figures of Merit may be used quite well to evaluate the relative power of various central computers and their high speed memories independent of their application to a specific problem. Not only can they be used to solve the analytical problems posed earlier and other problems closely related, but also they can be used very effectively to evaluate, from a cost-effectiveness point of view, proposed changes to data processing systems.

When memory size is considered, parity bits and sign bits should be excluded from the total since they store little or no information. Some are required but others may be superfluous for the task at hand. The number (M) to be used is the largest memory size that the particular machine can be expanded to.

The illusory potential of logarithmic scales was more than completely covered in a previous section. This quality must always be kept in mind by the analyst. It begins to fade as linearity is restored by operating on the log arithmetically. Unintentional changing of the base of the logarithm will result, however, if care is not exercised with these manipulations.

Access Time and Cycle Time must be used carefully in evaluating destructive and non-destructive readout machines.

Another effect must be guarded against. In some machines memory banks may be arranged so that access time may be reduced by referring to these banks in rotation. This is called "overlapping". Some machines have this capability - others do not. The amount of overlapping allowable varies among models and as a function of how many blocks of memory are purchased. Since the number of memory blocks to be required cannot often

(if ever) be accurately determined at this stage of analysis, overlapping should be considered by the analyst; but not in the figure of merit computation.

One of the very low access times quoted by one manufacturer results from maximum overlapping (which cannot be used unless all possible memory banks are acquired), while a very low access time quoted by another manufacturer can still be reduced to about 2/5 of that quoted by the use of his maximum overlapping capability. So much for the technical content of descriptive literature. The competent analyst must be certain where each of his numbers came from and why.

Add time is probably as good an indicator of internal computational speed as can be found, and using it alone does not inject the tincture of simulation mentioned earlier. In certain situations where the internal speed of the machine is quite critical, the Information Channel Capacity technique should be considered. Often, however, the technique used in the Highland Method should be adequate.

The concepts concerning word size have been treated adequately in previous sections, but it is important to remember that big words are not tantamount to better machines in all instances.

Since cost cannot accurately be predicted early in the analysis, and since costs are subject to change due to the pressures of competition, costs must remain outside the computation. This is true even though they must be considered in any worthwhile analysis.

When only a very small proportion of the high speed memory of a particular machine is of a very much higher speed than the balance, such as 128 registers of thin film vs. 32 K registers of core, then the thin film speed may be neglected entirely for the Figure of Merit computation. However, if we begin to postulate machines which have 5-10% or more of main memory operating ultra-high speed, then this clearly must be considered in the computation. Just how to do this best is open to discussion at the moment. In the Highland Method this factor would likely appear as some sort of multiplier in the denominator.

References - Calculation of Figures of Merit - Section 3.4

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4. STUDY INTEGRATION TASK

4.1 SCOPE AND OBJECTIVES OF STUDY INTEGRATION TASK

4.1.1 Merge Outputs of Requirements, Technology, and Methodology

The ANTACCS Study Integration Task merges the outputs from the Requirements, Methodology, and Technology tasks; and develops and demonstrates a set of approaches to ANTACCS system design. The integration task examines the outputs from the other tasks with the purpose of system synthesis, and evaluating and comparing alternatives. Among the major parameters to be considered are:

1) Missions
2) Command Levels
3) Timeliness
4) Operational Tasks
5) Information Processing Tasks
6) Data Flow
7) Standard Operating Procedures

The inputs to Integration may be classified as follows:

1) From Requirements:

   a) All mission requirements for Naval Tactical Command Control systems for the 1970 - 1980 time period.

   b) A substantial documentation of the interrelationships of these mision requirements.

   c) Projections of tactical concepts and procedures for the missions and time period stated.

   d) Projections of the naval forces available to carry out these missions, their formations, numbers, etc.

2) From Technology:

   a) Current and Projected Hardware and Software Technology as it applies to information processing systems.

   b) The implications of this technology to the design and operation of Naval Tactical Command Control Systems.

3) From Methodology:

   a) The methods for properly planning and designing an information processing system for command control. This will include explanations of or references to appropriate numerical or analytical tools.

   b) The methods and techniques which may be used to plan and control the implementation of information processing systems - and possibly by extrapolation - command control systems.

   c) Examinations of a few external areas of interest (such as simulation, modeling, and simulation languages) which, though not an integral part of design or implementation, are of interest to command control personnel.

The aim of integration is not to develop a preliminary design of ANTACCS but to illustrate the procedures and analytic techniques which can be applied by Naval system planners who will be synthesizing and evaluating alternate approaches to ANTACCS.

4.1.2 Comparison of Implications of Alternate System Operating Concepts for ANTACCS

On the basis of the ANTACCS system requirements which characterize the various system operating concepts, the Integration task describes hardware/software implications and puts together a system configuration for each operating concept. These alternate configurations will be compared by applying the techniques and procedures developed and specified by the Methodology task. The following comparison parameters will be used:

1) Data processing equipment requirements
2) Software requirements
3) Manpower requirements including calibre of personnel required and training requirements
4) System Costs (using the Total Force Cost Concept)
5) Intership Communication Requirements
6) Vulnerability to Natural Interference
7) Vulnerability to Man-made interference
    a) Unintentional
    b) Intentional
        i) Active
        ii) Passive
        iii) Spoofing

4.1.3 Demonstration of Application of Techniques and Procedures to the Synthesis and Evaluation of a System Node

Part of the Integration effort is to demonstrate the application of Methodology (techniques and procedures) to the synthesis and evaluation of a system node. In the process, the information needs and level of detail required for anlaysis becomes apparent. Because the level of detail required for a complete analysis of a system node is greater than for a system comparison, and this level of detail cannot be provided for every node, the node to be analyzed will be selected jointly by the Requirements and Integration tasks on the basis of availability of detailed data to adequately describe a node, completeness of nodal description and appropriateness of the node to ANTACCS.

Procedures to estimate system performance will be selected from the methodology outputs, and applicable constants will be determined by the Integration Task. Boundary conditions describing the nodal requirements, inclusive of concurrency of missions, will be established and used subsequently to estimate hardware/software/procedures configurations which satisfy the ANTACCS operation requirements. Each hardware/software/procedures configuration will be used as a basis for estimating

the intra-node system implications and communication requirements. System boundary conditions will be isolated from the system requirements by analyzing system stress conditions; timeliness, traffic volume, processing routines, etc., and will be used to synthesize alternate configurations. The trade-off parameters for estimating system performance will be selected from the point of view of critical system performance, and measurability. Parameters that cannot be measured or observed are useless in system design or evaluation. The system performance characteristics will then be estimated by considering the hardware/software/procedures configuration, the system boundary conditions, and estimated value or range of values on the system trade-off parameters. Estimated system performance characteristics will be tabulated for quick comparison, and used to compare one system against another.

4.1.4 Discussion of System Planning Items

The integration task will also examine the items covered in a TDP and will isolate the information developed by the ANTACCS study that specifically applies to the development of an ANTACCS/ACDS TDP. Topics to be included in this discussion are:

1) Management of the program
2) System design and specification
3) System test and evaluation

4.1.5 Summary of Study Integration Tasks

In summary, the Study Integration task will:

1) Merge the outputs from the Requirements, Technology, and Methodology tasks.
2) Demonstrate the application of these outputs to the synthesis and comparison of the attributes of various system configurations resulting from the system operating concepts as hypothesized and described by the Requirements task.

3) Demonstrate the application of the outputs from the Requirements, Technology, and Methodology tasks to the synthesis and evaluation of an ANTACCS system node.
4) Isolate and discuss the items developed by the ANTACCS study which are directly applicable to the preparation and specification of an ANTACCS/ACDS TDP.

4.2 COMPARISON OF IMPLICATIONS OF ALTERNATE SYSTEM OPERATING CONCEPTS

4.2.1 General

A candidate system is a complex of men, hardware, and software that functions in concept according to prescribed procedures to accomplish given objectives. The prescribed procedures and objectives are embodied in the descriptions of the input data, output data, data base, data processing functions, decision points, and data displays. The requirements of a candidate system are completely defined by specifying the parameter details within the above categories. However, the hardware-software-human relationships (HSHR) are not determined. Indeed, only the boundary conditions are delineated. The HSHR are functions of the state-of-the-art in hardware and software, space and power limitations, personnel limitations, economics, etc. It should be noted also, that the candidate systems as defined apply equally well to a data display, a ship, a level of command, or even a complete task force. Different system operating concepts are reflected in the detail definition of system parameters.

In this manner the Requirement task will define the command structure for alternate system operating concepts by specifying the levels of command, command activities and the interconnecting information flow lines. Direction of flow, type of traffic, volume of traffic, and timeliness of each type of traffic would be associated with each information flow line.

The command structure will serve as a framework for developing the mission descriptions and candidate systems. Each mission, its objectives, functions, etc., will be defined by the Requirements task for each command level, from the top command level which interfaces with the strategic command net to the lowest level of command which interfaces with the sensor and weapons systems.

4.2.2 ANTACCS Structure and Organization

4.2.2.1 Objectives of Structuring and Organizing

The first step in the comparison of alternate system operating concepts is the structuring of the ANTACCS information which characterizes these operating concepts. The areas to be covered in the structuring process are:

1) Structuring of the operational elements making up ANTACCS with respect to command, mission, platforms, and operational concepts.

2) Identifying concepts of system operation.

3) Identifying the information sets needed by Integration to perform the design function which brings together technology and requirements.

4) Presenting a structure and procedure for developing an information model for command and control which will assist in formulating alternate system configurations, and will facilitate performing trade-off analyses.

This process will show the direction to be taken and the information requirements that will be needed to fulfill the basic project objective of identifying and evaluating alternate approaches to system design of ANTACCS. These alternate designs will be approached from the point of view of:

1) Postulating an operating concept (e.g., centralized, decentralized).

2) Representing the requirements of ANTACCS command levels.

3) Hypothesizing hardware/software/man configurations for elements or nodes of the ANTACCS system.

4) Evaluating each alternate configuration in terms of criteria such as cost, capacity, capability, flexibility, etc.

Specifically, the nodes that would be included are those of the four command levels of ANTACCS: Task Force Commander, Task Group Commander, Task Unit Commander, and Task Element Commander.

4.2.2.2 Platforms - Missions - Command

At any point in time, the U.S. Navy has an aggregate of platforms to perform the many missions within a current Naval command organization. The platforms represent at least a twenty-year span of marine engineering construction techniques and weapon technology. The missions include the traditional Navy missions (of which AWS, AAW, STRIKE, and AMPHIB will be the objects of ANTACCS study) along with the requirements of responding to the threat of new technological weapon developments. The naval command structure remains essentially the same, but the information needs and response time requirements for different levels of command vary widely with mission, weapons, and threat.

Responding to any and every threat is a formidable task that requires experienced personnel, exercising timely and effective control over the U. S. Navy units participating in assigned operations.

4.2.2.3 Platforms

The ANTACCS structure will be consistent with and conform to the limitations of the existing and anticipated U. S. Naval platforms. The primary classes of platforms to be considered in the development of alternate configurations of command and control systems for the ANTACCS study are:

Aircraft Carriers: CVA, CVAN and CVS
Command Ships: AGMR
Cruisers: CA, CAG, CG, CGN, CGL
Destroyers: DD, DDE, DDG, DDR, DL DLG, DLGN
Submarines: SS, SSG, SSGN
Aircraft: Airborne Command and Control Centers

Supporting platforms will be included in the alternate system descriptions whenever necessary for completeness in the analysis and evaluation. Classes of platform information desired are: weapons, sensors, communications, mission performance capabilities, command level associations, etc.

4.2.2.4 Missions

The ANTACCS study is directed to the analysis and evaluation of an amphibious operation which includes a detailed analysis of the following missions (and to others as they are determined to be appropriate).

Anti Air Warfare (AAW)
Anti Submarine (ASW)
STRIKE
AMPHIB

The information requirements for each mission will be described by BAARINC for every level of command within the purview of ANTACCS to provide a basis for effectively integrating the existing and proposed Naval subsystems (NTDS, ATDS, etc.) into an integrated command and control structure.

4.2.2.5 Command Structure

The U.S. Naval command structure has traditionally been superimposed on the platform oriented elements of the Navy which occurs naturally because each ship can be considered as a single entity. Because of the platform orientation, and the need for flexibility within a naval organization, each ship must be capable of performing multiple missions, both sequentially and concurrently. Sequentially, whenever a

primary mission is changed, and concurrently whenever multiple missions are assigned. The multiple mission-multiple command level capability of the ships provide great flexibility for making up a Task Force, for mission assignment and re-assignment and for utilizing a Task Force for new missions other than the ones for which it was initially formed. The thread which coordinates and unites these diverse, mission-oriented complexes of ships and men is the Naval command and control structure.

The basic command structure which will be used by the Integration Task in synthesizing and evaluating candidate systems for ANTACCS is illustrated in Figure 4.1 Naval Operational Chain of Command for ANTACCS.

This structure illustrates six levels of command which extend from the Fleet Commander in Chief down to the Element Commander. The lower four levels of command represent the command span covered by ANTACCS. ANTACCS will interface with the Numbered Fleet Commander above, and will extend to the Element's Combat Information Center at the lower end of the command structure.

ANTACCS will integrate the existing and proposed Naval weapon, sensor, and command systems such as NTDS, MTDS, ATDS, SEAHAWK, CAPE, FRISCO, IOIS, etc. into a unified Naval command structure within which the future navy will operate. These systems will have a unique interface within ANTACCS at each level in the command structure. Each interface will be defined by data transfer and timeliness response required for effective inter-system operation. Intuitively, one is led to believe that each of these weapon and sensor systems will interface within ANTACCS at several levels of command. For instance, the NTDS system will interface with ANTACCS on the element commander level by providing raw and/or processed sensor data which reflects dynamic environmental conditions, and by receiving weapon and sensor assignments from the element commander.

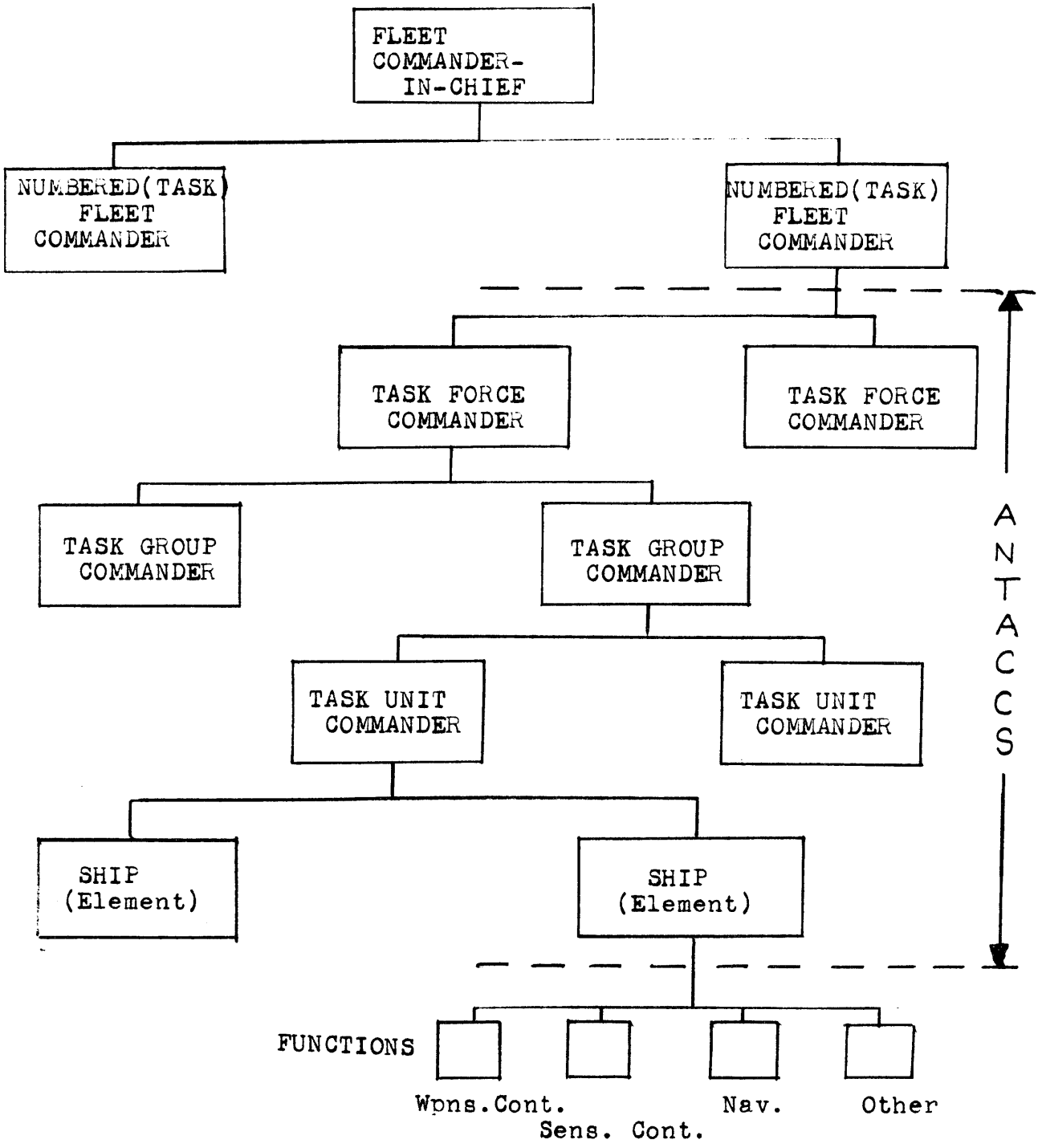

Fig. 4-1: NAVAL OPERATIONAL CHAIN OF COMMAND FOR ANTACCS

NTDS will also interface on a higher command level where decisions affecting area of coverage and target responsibility between NTDS and ATDS are to be made. The information necessary to support area of coverage assignments certainly will not be raw sensor outputs, but processed environmental summaries which reflect magnitude and direction of raid instead of individual aircraft location. Changes in area of coverage will probably be based upon a number of factors, some of which might be: size of raid, threat axis, probable enemy reserves, etc. In conclusion, each level of command will have its unique interface with the weapon and sensor systems, and will have its unique problems associated with control and utilization of the weapon and sensor systems.

The information requirements will be delineated by the breadth of command responsibilities within each level of command, and by the extent of direct control exercized over sensors and weapons. Breadth of command is a function of the number and type of missions assigned, and of the mission objectives. As a general rule, the greater the breadth of command, the greater becomes the probability that only summary data will be provided as a routine basis, with detailed supporting data to be made available on short notice. Also, the larger the number of simultaneously assigned missions, the more diverse and less detailed becomes the information needed to support the commander in the execution of the missions. In the development and evaluation of the alternate system for ANTACCS, the information requirements for each level of command and mission will be determined and compared with the requirements for other missions. The flexibility of the ANTACCS alternate systems and operational efficiency for multiple mission performance will be estimated through the techniques of comparing information, personnel, and equipment requirements for each level of command.

4.2.3 Concepts of System Operation

4.2.3.1 General

Initially two philosophies of system control, centralized and decentralized, will be analyzed and evaluated. While centralized and decentralized control represent extremes in system control, a modified and perhaps more realistic interpretation of each concept will be used in the ANTACCS Analysis.

4.2.3.2 Centralized Control

The centralized system control concept is illustrated by Figure 4.2, Centralized System Control. This figure is grossly simplified, however, the concept of centralized control is clearly depicted. First, it is assumed that each ship in the task force is capable of performing the control function of each assigned mission, and that each ship can satisfactorily perform the target detection and weapon control operations associated with the assigned mission. In the figure, Ship number 3 has been designated Force Anti Air Warfare Commander (FAAWC) for the task force. In this capacity, FAAWC would receive processed and semiprocessed outputs from the AAW sensors throughout the task force, evaluate the environmental data, and initiate management directives for the assignments of AAW weapons to targets. Actual control of the weapons would be exercised by Combat Direction Centers located on each ship. Since each ship would be equipped to perform the AAW control function of the Task Force, this function could be immediately transferred from one ship to another, if necessary.

A similar situation prevails for the Force Anti Submarine Commander (FASWC). The FASWC would receive processed and semiprocessed outputs from the ASW sensors throughout the Task Force, evaluate the ASW environment and initiate management directives for the assignment of the ASW weapons to the targets. The FASWC would exercise management control over the Task Force ASW sensors and weapons, but active control would be exercised by the Combat Direction Centers on each ship.

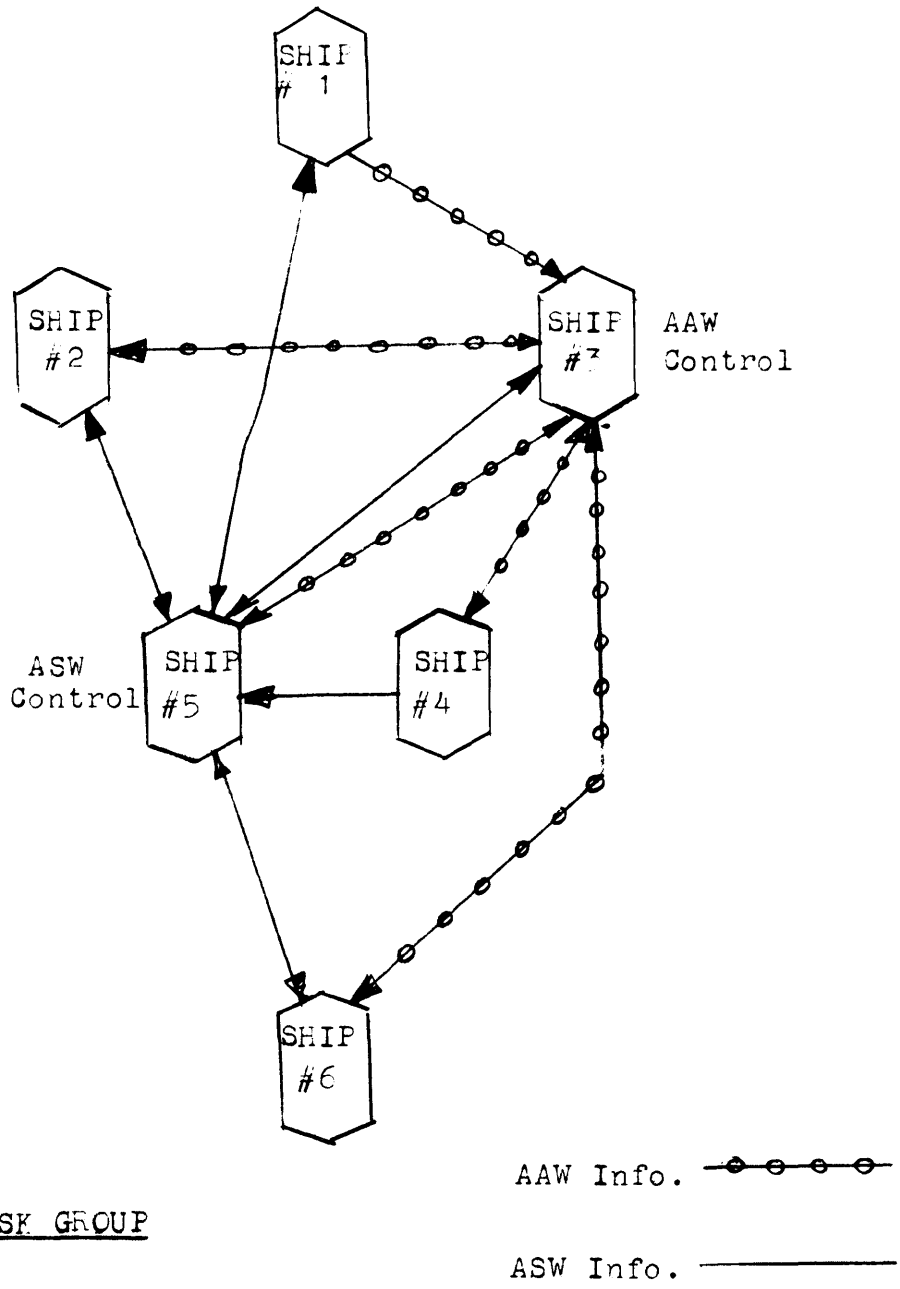

Figure 4-2; **CENTRALIZED SYSTEM CONTROL**

While each ship would be capable of assuming the Force mission control function of each mission, this does not mean that the mission control would be performed equally well by each ship. Differences in available space, equipment, and personnel, would affect the efficiency of mission control from one ship to another. Another factor which would also influence the efficiency of mission performance would be the number of concurrent missions which would be performed on a single ship. Larger ships could and would probably perform more than one concurrent mission. However, each ship would have a saturation point, which is a function of the equipment, personnel, and data volume and beyond which the system performance would begin to deteriorate rapidly. The saturation point would probably differ for each ship because of the normal variation in equipment and personnel, but the variations in saturation point conditions should be small and should lie within a yet undetermined but small range of parameter values.

4.2.3.3 Decentralized Control

The decentralized system control cpncept is illustrated by Figure 4.3 Decentralized System Control. It is assumed that each ship would be capable of performing the control functions for all missions simultaneously, and one ship within each sector would be assigned total responsibility for the section. Within the sector, Sector Warfare Commander (SWC) would perform the management control function for all missions and would initiate directives for assigning sensors and weapons to targets. Each SWC would inform other SWC of the current environmental conditions on a timely basis through a routine interchange of information and through special messages for handover of target assignment and weapon control. The area of responsibility for a damaged or inoperable SWC would be reallocated among the remaining SWC's to maintain total area coverage. Enlarging the area of control might result in degradation of system performance. Incremental increases in area of coverage and number of targets would result in incremental degradation of the system until a saturation point was reached. Beyond the system saturation

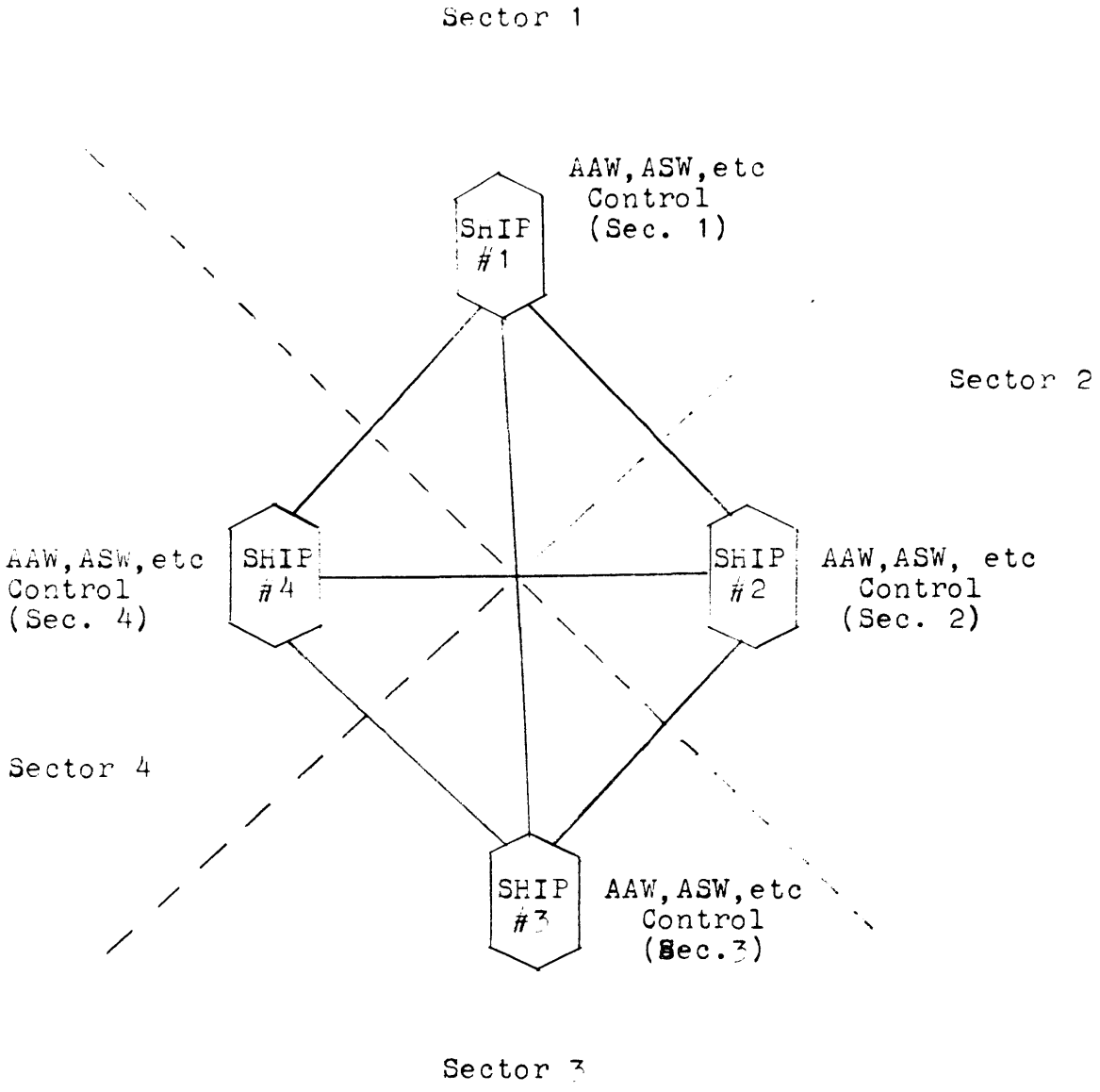

Fig. 4-3; **DECENTRALIZED SYSTEM CONTROL**

point, system performance degrades much more rapidly than the incremental increase in system load. The saturation point will probably differ for each environmental condition and force configuration, but the variations in the saturation point conditions should be small and should lie within a yet undetermined but small range of parameter values.

4.2.3.4 Implications of Centralized/Decentralized Philosophy

There are several implications of the Centralized/Decentralized control concepts which will be enumerated, but not evaluated at this time.

1) Both concepts imply that a trade-off between computer facilities and communication facilities will be effected. That is, the input data to each level of command will be summarized and edited before data will be transferred to the next level of command, and the amount of data transferred will be influenced by command level needs, communications facilities, and data processing facilities.

2) Control and Applications

   a) Centralized control concept permits application of ships, equipment, and personnel to missions for which they are best suited.

   b) Decentralized control concept requires a jack-of-all-trades ability for each command level.

3) Area of Responsibility

   a) Area of responsibility is greater for each mission in the centralized control concept which might introduce problems with long range, high volume communications especially under ECM.

   b) Area of responsibility is smaller for each mission in the decentralized control concept which implies shorter range, high volume traffic.

4) Centralized control concepts would probably require fewer computers and displays per ship because fewer missions would be simultaneously assigned to a single ship.

5) Decentralized control concepts would be more flexible because each command level ship would be capable of assuming and discharging the responsibilities of sector control, which would include command and control of multiple missions.

4.2.4 Basis for Comparison of Alternate System Operating Concepts

4.2.4.1 Attributes of Each System Operating Concept

The initial step in comparing the alternate system operating concepts is to assemble and organize the information which characterizes these concepts. The assembly of this information will be by:

1) Inter-node information flow characteristics which will relate mission, data quantity, direction of flow, timeliness criteria, inter-ship distance, communication facilities, etc.

2) Command level and procedures which will relate mission, operational tasks, data needs, decisions, timeliness criteria, information processing tasks, etc.

3) Task force complement and disposition which will relate ship type, command level, intership distances, communications facilities, etc.

Another purpose of the analysis associated with this task, other than organizing the data, is to isolate similarities and dissimilarities among the various information characteristics of the various system operating concepts. The similarities are representative of the invariant attributes among the system operating concepts, and system design solutions based upon these attributes should show a degree of consistency. The dissimilarities are representative of the variant attributes among

the system operating concepts, and system design solutions based upon these attributes should be examined to determine their impact on the systems. Variations in system performance and operation should be primarily reflected in design solutions which satisfy the variant system attributes.

This effort was not completed for this report. It will be fully discussed in the ANTACCS Study final Report.

4.2.4.2 Estimate Hardware/Software Implications

The variant and invariant attributes of the system operating concepts will be translated into their hardware/software implications. The analysis steps included in this subtask are briefly discussed below, and will be fully discussed in the final report.

1) Estimate quantity of data to be stored on each command level which would include: classes of data, quantity of data, data base update cycle, data retrieval cycle, mission, and command level.

2) Estimate information processing functions to be performed on the various classes of data which would include; processing functions, classes of data, quantity of data, processing time, concurrence of processing, mission, and command level.

3) Develop general system hardware/software configurations for each system operating concept.

4.2.4.3 Comparison of Alternate System Operating Concepts

The analysis steps to be included in this sub-task are briefly discussed below and will be fully discussed in the final report.

1) Define the basis for comparison of alternate system operating concepts.

   a) Hardware/software/procedures/personnel

   b) Cost

c) Intership communications

d) Vulnerability to natural and man-made interference

2) Compare the alternate system operating concepts

This comparison will be made against the hardware/software configuration developed in task 4.2.4.2(4) and comparison parameters defined above.

3) Document the results of comparison of alternate system operating concepts

These results will be discussed in the ANTACCS Study final report.

4.3 DEMONSTRATION OF THE SYNTHESIS AND EVALUATION OF A SYSTEM NODE

4.3.1 Nodal Development

A node is an element of ANTACCS which can be described relative to its position in the command structure, the communication system, the platform which carries it and a set of special command and control functions. A node is completely defined by characterizing its inter- and intra-nodal parameters. Inter nodal parameters include: information movement between nodes, relationships among nodes, nodal inputs, and nodal outputs. Intra-nodal parameters include: mission, platform, operating concept, command level, technical functions, command elements, and operational tasks. The structure for organizing these parameters will be a multidimensional array as described in paragraph 4.3.2. Multidimensional arrays will be used to organize the background information into a suitable structure for analysis of alternate system configurations. Examples of these arrays to organize background information are: platforms vs command levels, platforms vs primary missions, platforms vs weapons and sensors, command levels vs information requirements, command levels vs operational tasks, etc. In addition to the background information, the multidimensional arrays will also be used to organize the mission requirements information for each level of command. The structured information will then be used as a basis for synthesis and evaluation of the alternate configurations for ANTACCS.

The methods of information structuring will be amenable to analysis, within limits, by applying set theory. Such concepts as null sets, congruence, and intersection can be usefully employed to isolate related and non-related technical operations and data bases. The applications and limitations of set theory to information structuring will be investigated and used wherever set theory techniques are found to be applicable.

4.3.2 Information Structuring

Past experience in planning and implementing on-line, real time information processing systems has led to various information structuring tools to guide the transition from broad requirements to specific implementations

of hardware, software and user procedures. Continuing work in this field will undoubtedly produce more techniques in the future, however, no universal techniques or methodology exist in this problem area at this time. These considerations, however, do not mean that the analyst/planner should not attempt to use the most objective techniques available. In recognition of the current state of information structuring methodology and technology, Informatics has selected a structuring technique as a starting point which has been used successfully in a recent on-line information processing system analysis and design. The basis of this technique is a structure which depicts the information movement and processing in the system under analysis in a framework consistent with the particular problem, yet independent of particular configurations, echelons or geographic divisions of the system in the real world.

In ANTACCS this means that the structure should depict the current (seconds, minutes) and historical (hours and longer) environmental information movement and processing, and the command information movement and processing within the system in a framework which is consistent with, yet independent of, four variables: particular command level, mission, platform, or operational concept.

A structure thus developed is applicable as an analytical tool for integration of intra-nodal requirements under differing combinations of the four variables and for isolating the necessary data processing and display operations after successful integration.

A structure which meets this criterion is a multidimensional framework which details system operational tasks on one axis, elements of command and control on the second axis and a series of definable and, to the extent possible, logically separable information processing functions on the third axis. Each of the information processing functions is defined by its inputs, outputs, historical data banks or criteria, and internal processes. The functions thus defined are linked by information flow from function to function, feedback among functions and recycling of some or all functions. This linking allows the structure to depict

the dynamics of the decisions and information flow for each operational task. Figure 4-4 is an example of the structure. One axis represents some elements of command and control: estimate of the situation, development of plan preparation and issuance of directives, and monitoring planned actions. Another axis shows some examples of system operational tasks; surveillance, weapons assignment, weapon employment and movement of forces. The third axis shows the information processing functions as:

1) Data Collection and Classification:
   a) Monitoring static and dynamic parameters which define the enemies, political objectives, and military capabilities and actions.
   b) Monitoring static and dynamic parameters which define our own political objectives, military capabilities, and actions.
   c) Monitoring static and dynamic parameters which define the neutrals' political objectives and military capabilities.
   d) Monitoring static and dynamic parameters which define the weather, and other physical phenomena.
   e) Segmenting the data collected into various definable classes.

2) Data Conversion and Selection:
   a) Converting like data to common base (all time to Z-time, locations to common, etc.).
   b) Separating pertinent mission data from the total input data.

3) Information Correlation and Significance Determination which is:
   a) Combining information from within a source or from various sources to structure a partial or complete description of events or situations.
   b) Determining possible event or situation outcomes by comparing current partial description of events and situations with past events and situations (prediction).
   c) Determine the relative worth, redundance, conflict, and/or importance of various information.
   d) Feedback to data collection and selection to make a change in emphasis or input needs.

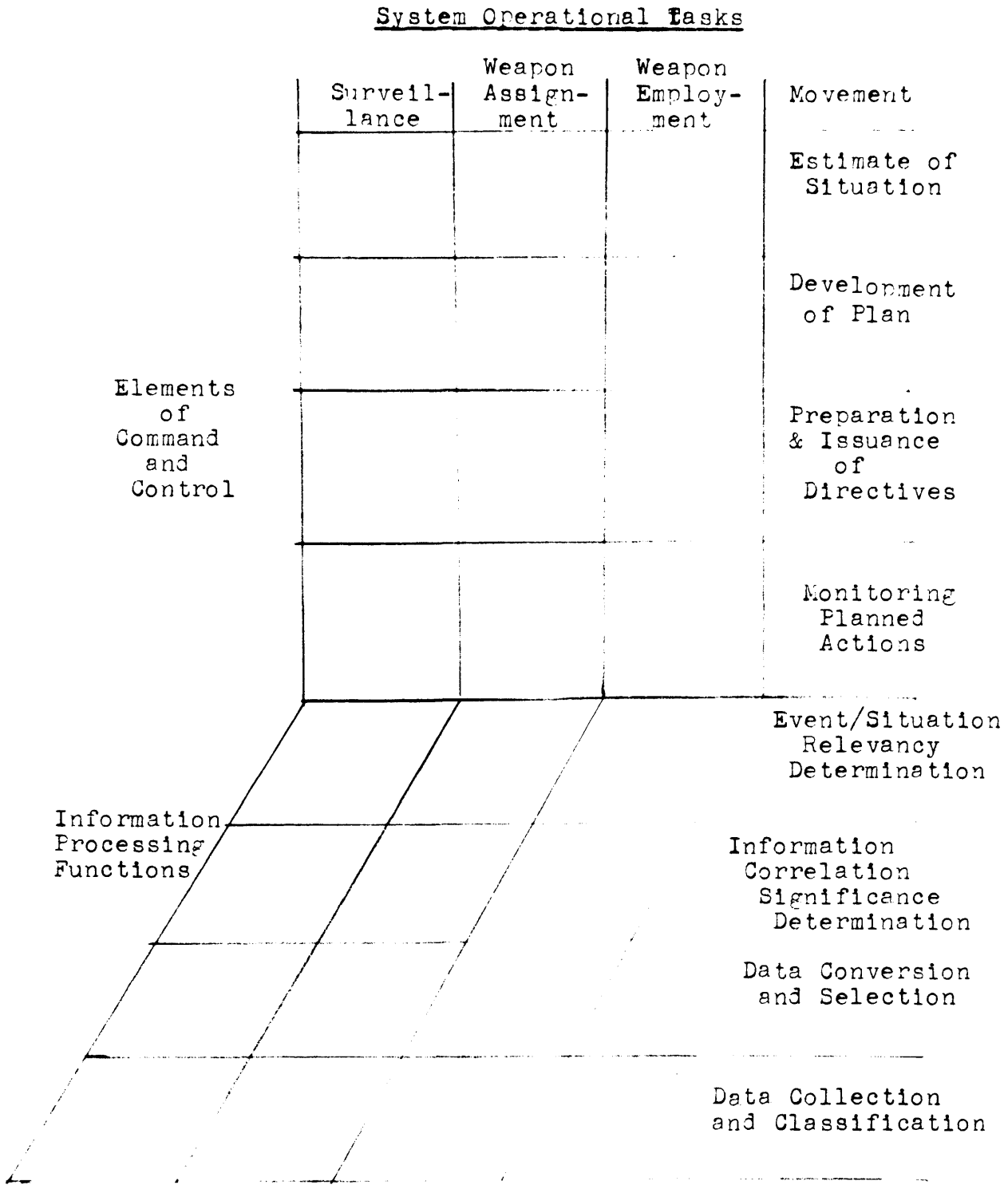

Fig. 4-4; INTRA NODE DEFINITION; GIVEN MISSION, PLATFORM, COMMAND LEVEL, OPERATIONAL CONCEPT

4) Event/Situation Relevancy Determination which is:

   a) Relating events/situations within the environment to particular task, etc.

The Complete Description for Each Function Should Include:

1) Technical Function Title including expected level of analysis

2) Input to Function

   a) Qualitative

      i) types of input
      (class definition down to specific formats, etc.)

      ii) source of input
      (forward from previous function, feedback from other functions, etc.)

   b) Quantitative

      i) frequency or occurence rate of inputs

      ii) timeliness of input
      (related to origination of data)

      iii) concurrence of multiple sources

3) Historical and/or Criteria Files of Function

   a) Qualitative (data type description)

   b) Quantitative

      i) amount of data

      ii) update frequencies

   c) Retrieval or use times/frequencies

4) Logical Processes within Function

   a) Qualitative

      i) information/data relationships
      (derivable or inferable classes)

ii) logical algorithms

iii) use of historical data, criteria, or thresholds

iv) decision results

b) Quantitative

i) frequencies

ii) concurrences

iii) time delays

5) Outputs

a) Qualitative

i) types

ii) formats

iii) routing

b) Quantitative

i) lengths of messages, information groups, etc.

ii) frequencies by types, etc.

iii) timeliness required and/or timeliness achievable by types

4.3.3 Structure Use

Structures developed in the pattern described above can be used to illustrate the basic qualitative and quantitative aspects of information flow and processing at many levels of detail within a node and many levels of abstractness, depending on the stage of problem requirements definition. For instance, functions should be defined for a complete task force engaged in every mission at a general level to establish a point of reference for starting a detailed analysis, as well as completely detailing the flow and processing that should occur for a node at a particular command level (Task Group) performing a particular mission (decentralized AAW) using particular platforms (DLG's and DDR's). Once an intra-node structure has been defined, the data processing operations can be defined. Some typical operations are:

1) input
   - on line from machine
   - manual entries
2) output
   - on line displays
   - printouts
   - alarms
   - to another machine on line
3) computing
   - arithmetic
   - logic
4) filing and collecting
5) sorting
6) file purging
7) file searching

This statement of the data processing operations which must be performed, along with all the various file sizes and an indication of the complexity of the logic, allows an estimate of the equipment characteristics (dp and display and comm.), program specifications, and procedures necessary to meet the node requirements. Alternate projected hardware, software, and procedure descriptions can now be assembled and evaluated.

4.3.4 Example of Integration Approach

A preliminary illustration of the structuring technique described in section 4.3.2 has been constructed using the BARRINC TFC nodal description. It is presented below under the two primary headings of intra-nodal parameters and inter-nodal parameters.

4.3.4.1 Intra-Nodal Parameters

1) Node to be Described

Command Level	- TFC
Platform	- Not Given
Mission	- AAW (limited war)
Concept of Operation	- Centralized Control

2) Elements of Command and Control

Estimate of the Situation
Development of the Plan
Preparation and Issuance of Directives
Supervision of Planned Action

3) System Operational Tasks

Allocation of Support Units
Relative Disposition of Forces (Position, Time, Movement)
Determination of Threat Axis, Magnitude
Surveillance of Current Force and Threat Status

4) Information Processing Functions

a) Estimate of the Situation, Relative Disposition of Forces, Threat

i) Data Collection and Classification

Inputs	- Intelligence Report, Movement Report, Own Forces
Outputs	- Not Given
Processes	- Not Given
Historical Banks or Criteria	- Not Given

ii) Data Conversion and Selection

Inputs - Not Given
Outputs - Not Given
Processes - Not Given
Historical - Not Given
Banks,Criteria

iii) Information Correlation and Significance Determination

Inputs - Not Given

iv) Outputs -
Printout - Enemy Forces Information
Printout - Friendly Forces Information
Plot - Enemy Forces Time and Position Plot
Plot - Friendly Supporting Forces Time and Position Plot
Printout - Relative Combat Power
Printout - Opposing Characteristics

v) Processes - Sort, Search

vi) Historical Banks, Criteria

Enemy Forces in Area of Operation
Friendly Supporting Forces in Area of Operations
Area of Operations Data
Area Communications Facilities

vii) Event/Situation Relevancy Determination

Inputs - Not Given
Outputs - Not Given
Processes - Not Given
Historical - Not Given
Banks

b) Development of the Plan, Allocation of Supporting Units, Determination of Threat, Relative Disposition of Forces

i) Data Collection and Classification

Inputs - Component Operations, action statements, threat axis, schedule, coordination instruction

Outputs - Not Given

Processes - Not Given

Historical - Not Given

Banks

ii) Data Conversion and Selection

Inputs - Not Given

Outputs - Not Given

Processes - Not Given

Historical - Not Given

Banks

iii) Information Correlation and Significance Determination

Inputs - Not Given

Outputs - Not Given

Processes - Not Given

Historical - Not Given

Banks

iv) Event/Situation Relevancy

Inputs - Not Given

Outputs - Events by operation, forces, formation, tactical net plan

v) Processes - Search

vi) Historical Banks -

Own Forces and Status

Own Forces Characteristics

Enemy Forces

Formations

Current Disposition

Future Events

c) Preparation and Issuance of Directives

Not Given

d) Supervision of the Planned Action, Surveillance

i) Data Collection and Classification

Inputs - Own Forces Status Position
Enemy Forces Status Position
Outputs - Not Given
Processes - Not Given
Historical - Not Given
Banks

ii) Data Conversion and Selection

Inputs - Not Given
Outputs - Not Given
Processes - Not Given
Historical - Not Given
Banks

iii) Information Correlation and Significance Determination

Inputs - Not Given
Outputs - Not Given
Processes - Not Given
Historical - Not Given
Banks

iv) Event/Situation Relevancy Determination

Inputs - Threshold Ps
Outputs - Time of Threat Onset
Significant forces change
Time Required to Change Disposition
Maximum Weapon Release Range and Time
Ps at Maximum weapon release and threshold test
Alerts
Processes - Not Given
Historical - Own Forces

Banks	Current disposition
	Enemy Forces
	Relative Combat Power
	Formations

4.3.4.2 Inter Nodal Parameters

1) Inputs - Not Given
2) Outputs - Not Given
3) Relationships Among Nodes - Not Given

NOTE: A node has not been selected for complete analysis to date, however, the selection will be made soon and an analysis presented in the final report.

4.3.5 Boundary Conditions

1) Statement of Bounds for each Node in the System
2) Technology Limits
3) Requirements Limits

NOTE: To be accomplished in final report to a detailed level for one node as indicated and to a general level for all nodes.

4.3.6 Trade-Off Parameters

4.3.6.1 Operation Parameters

1) Level of Capability Achieved
2) Comprehensiveness of Node Solution
3) System Operation under Degradation Conditions
4) Time, Volume Capacities
5) Saturation Points

4.3.6.2 Implementation Parameters

1) Time to Implement and obtain operational capability
2) Complexity of implementation
3) Cost of subsystem and total
4) Cost of operating system (maintenance and supplies peculiar to alternative)

NOTE: The Trade Off Parameter definition will be improved and figures provided in the final report for the node selected for intensive study.

4.3.7 Description of Hardware/Software/Procedures Alternatives

1) Configuration Descriptions

2) Measures of Performance for Alternatives

3) Configuration Capabilities

Methods for analytically evaluating alternates of the complexity of ANTACCS are yet to be fully developed, but will fall in the class of techniques which assign relative values to the various criteria levels achieved by alternates and form resultants for each candidate. The resultants will then be compared using an appropriate numerical scale to arrive at a best choice.

4.4 DISCUSSION OF SYSTEM PLANNING ITEMS

The present work by Informatics is intended to demonstrate, by example for one node, the application of methodology and analytical techniques to system design as a guide for the system planners who will be responsible for complete system design and preparation of the Technical Development Plan (TDP) for ANTACCS. With this view in mind, Informatics has provided a discussion of several system planning items which form part of a TDP. Items of particular interest are:

1) Narrative of Requirements and Brief of the Development Plan
2) Management Plan
3) Block Diagram of System
4) Subsystem Characteristics
5) Associated System Characteristics
6) Test and Evaluation Plan

Most of the work in the study integration task must necessarily be done in the final months of the study effort. Accordingly the discussion of this task in this midway report is of an introductory nature only.

5. BIBLIOGRAPHY

5.1 INTRODUCTION

Bibliography is organized generally in the sequence of the technical section of the report. This section thus collects the bibliographical references under the following main headings.

1) Technology

   a) Displays
   b) Input/Output Devices
   c) Memories
   d) Components and Packaging
   e) Advance Usage Technique
   f) Machine System Organization
   g) Programming

2) Methodology

   a) Computers and Hard Science
   b) Simulation

At this point in the ANTACCS study, the bibliographical data has not been completely cross-checked and merged. This will be done for the final report.

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5.3.1 Computers and Hard Science

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