NOTE: The polling address is determined by the setting of the two HEX rotary switches positioned below the baud switch. The least significant Hex digit is determined by the upper of the two switches.

The Model 302 CRT terminals are designed for operation in a polled, daisy chain or multidrop method of operation. The polling sequence is extremely simple, consisting of a 2-character interrogation sequence.

To Select a Terminal (Poll):

COMPUTER SENDS:	TERMINAL RESPONDS:	CONDITION:
1/ ENQ (Hex 05) C_E		------
2a/ Normal Address (any ASCII character)	EOT (Hex 04) (OR) STX (Hex 02) (OR) 512 ASCII character block	If "SEND" key has not been depressed. If "SEND" key has been depressed. If "SEND" key depressed and unit is factory strapped for "ALL DATA".
2b/ Fast Select Address (See Note 2)	No signal returned	Terminal ready to receive data (See programming notes)

After Terminal Selected:

The desired HEX can be generated from a keyboard using the CONTROL key and a letter

COMPUTER SENDS:	CONTROL	TERMINAL RESPONDS:
1/ STX (Hex 02)	C_B	Sends all data from cursor position to end of screen.
2a/ DC1 (Hex 11) (AND)	C_Q	Shifts to cursor address mode. No transmission.
2b/ ASCII character (AND)		Cursor moves to character position on line. (See Table)
2c/ ASCII character		Cursor moves to line on screen.
3/ BS (Hex 08)	C_H	Cursor backspaces.

COMPUTER SENDS:		TERMINAL RESPONDS:
4/ LF (Hex 0A)	C_J	Cursor steps to next line.
5/ CR (Hex 0D)	C_M	Carriage return.
6/ DC2 (Hex 12)	C_R	Home cursor.
7/ DC3 (Hex 13)	C_S	Cursor up one line.
8/ DC4 (Hex 14)	C_T	Cursor advance.
9/ BEL (Hex 07)	C_G	Bell rings.
10/ HT (Hex 09)	C_I	Tab.
11/ EM (Hex 19)	C_Y	All following characters will be protected against operator action and displayed at lower intensity.
12/ US (Hex 1F)	C_{SH_O}	All following characters will be unprotected and displayed at normal intensity.
13a/ CAN (Hex 18) (AND)	C_X	All unprotected characters cleared from cursor position to end of screen and cursor goes home. (See programming notes)
14a/ FS (Hex 1C)	C_{SH_L}	All characters cleared from cursor position to end of screen and cursor goes home. (See programming notes)
15a/ SYN (Hex 16) (OR)	C_V	Disconnects from line - Operator still locked out - "SEND" key still depressed.
15b/ ETB (Hex 17)	C_W	Disconnects from line. Operator free to use terminal.

Programming Notes:

Failure to release a previously selected terminal will cause it to respond to computer instructions, causing the input to the computer to be "garbage". Previously selected terminals are released by the

TABLE OF CURSOR POSITIONING

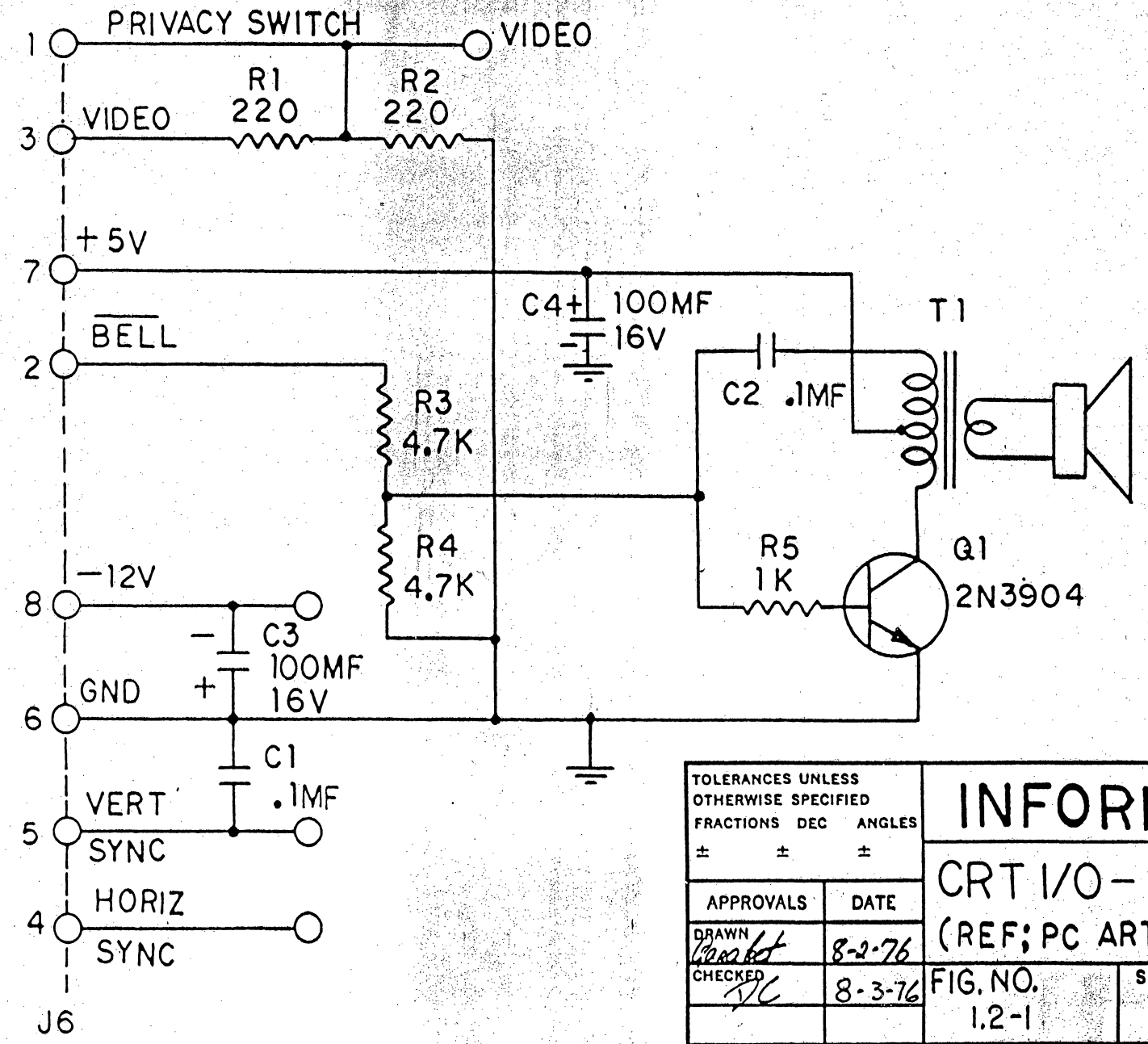
"X" POSITION - This is the character position on the line:

Computer Sends (Hex):	Cursor Moves to Character Position:	Computer Sends (Hex):	Cursor Moves to Character Position:
00	1	10	17
01	2	11	18
02	3	12	19
03	4	13	20
04	5	14	21
05	6	15	22
06	7	16	23
07	8	17	24
08	9	18	25
09	10	19	26
0A	11	1A	27
0B	12	1B	28
0C	13	1C	29
0D	14	1D	30
0E	15	1E	31
0F	16	1F	32

"Y" POSITION - This is the line of the screen:

00	1
01	2
02	3
03	4
04	5
05	6
06	7
07	8
08	9
09	10
0A	11
0B	12
0C	13
0D	14
0E	15
0F	16

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	CHANGE C1 FROM .01 TO .1	8-2-76	



TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

APPROVALS	DATE
DRAWN	8-2-76
CHECKED	8-3-76

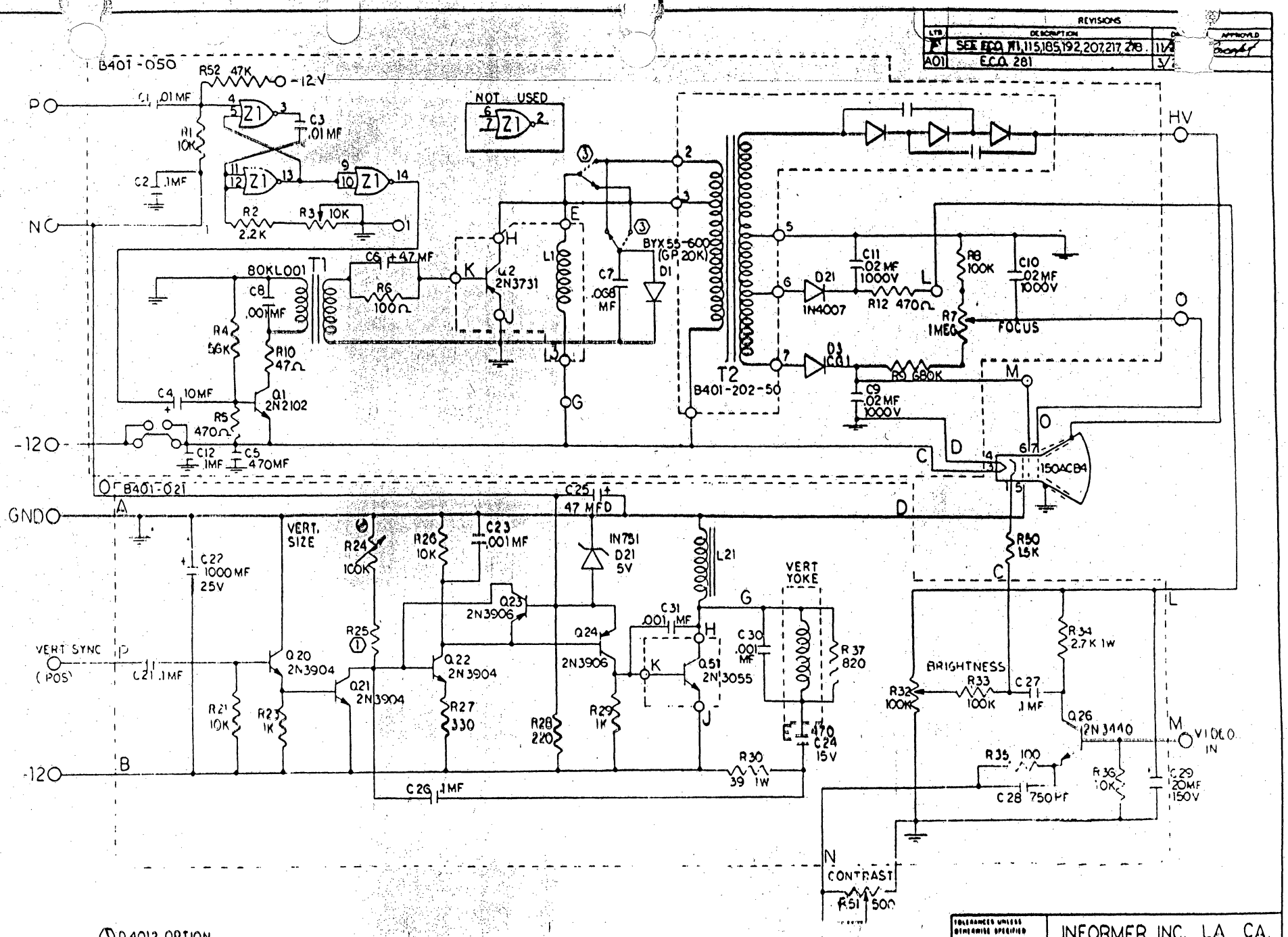
INFORMER INC.

CRT I/O - D301-204

(REF; PC ARTWORK D301-002)

FIG. NO.	SIZE	DRAWING NO.
1.2-1		85068

DO NOT SCALE DRAWING — SHEET



REVISIONS		
LTR	DESCRIPTION	DATE
	SEE ECO #1,115,185,192,207,217,218	11/4
A01	E.C.O. 281	3/

APPROVED

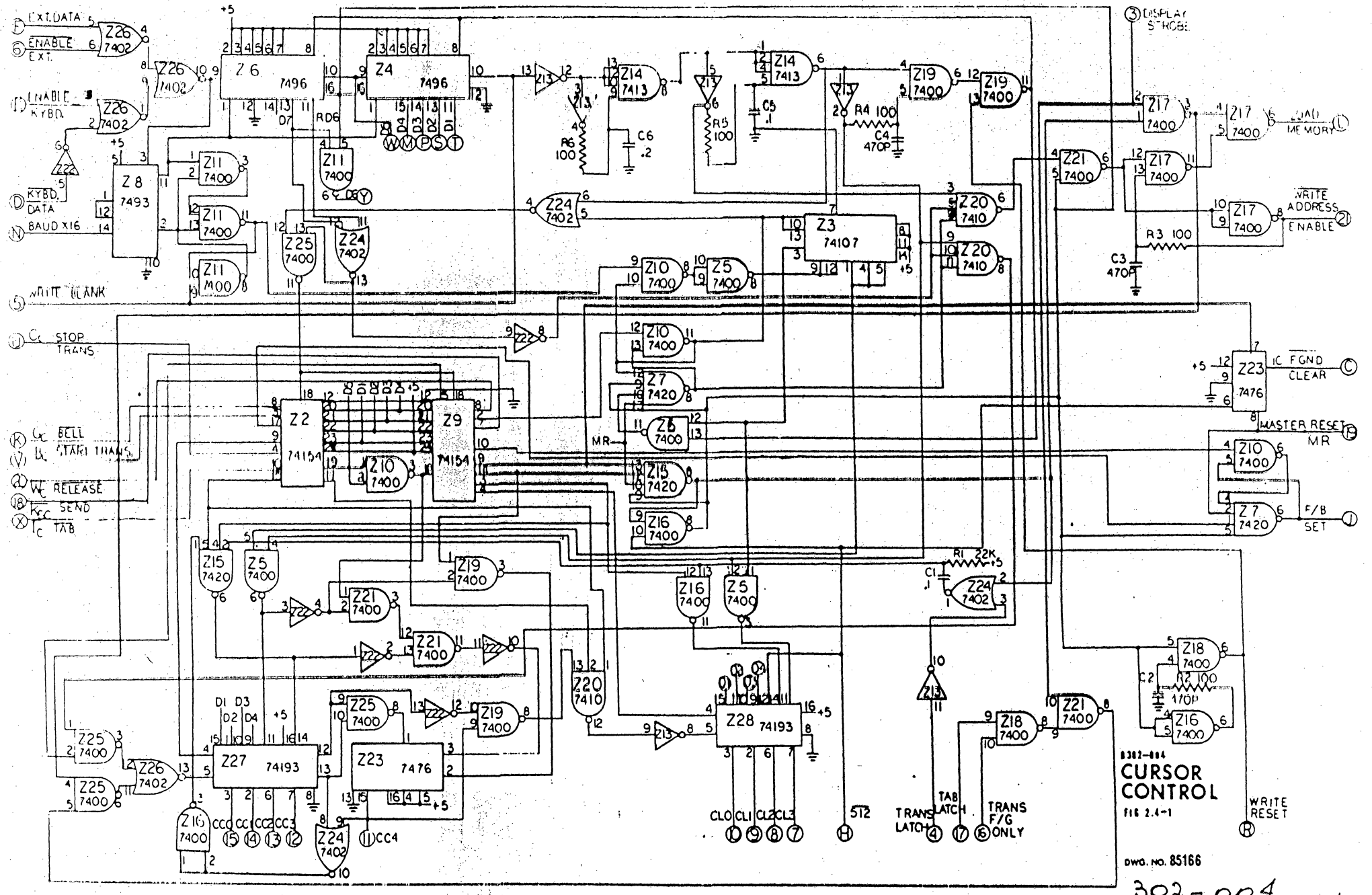
(J) D4012 OPTION

2) Z1 IS SP 380

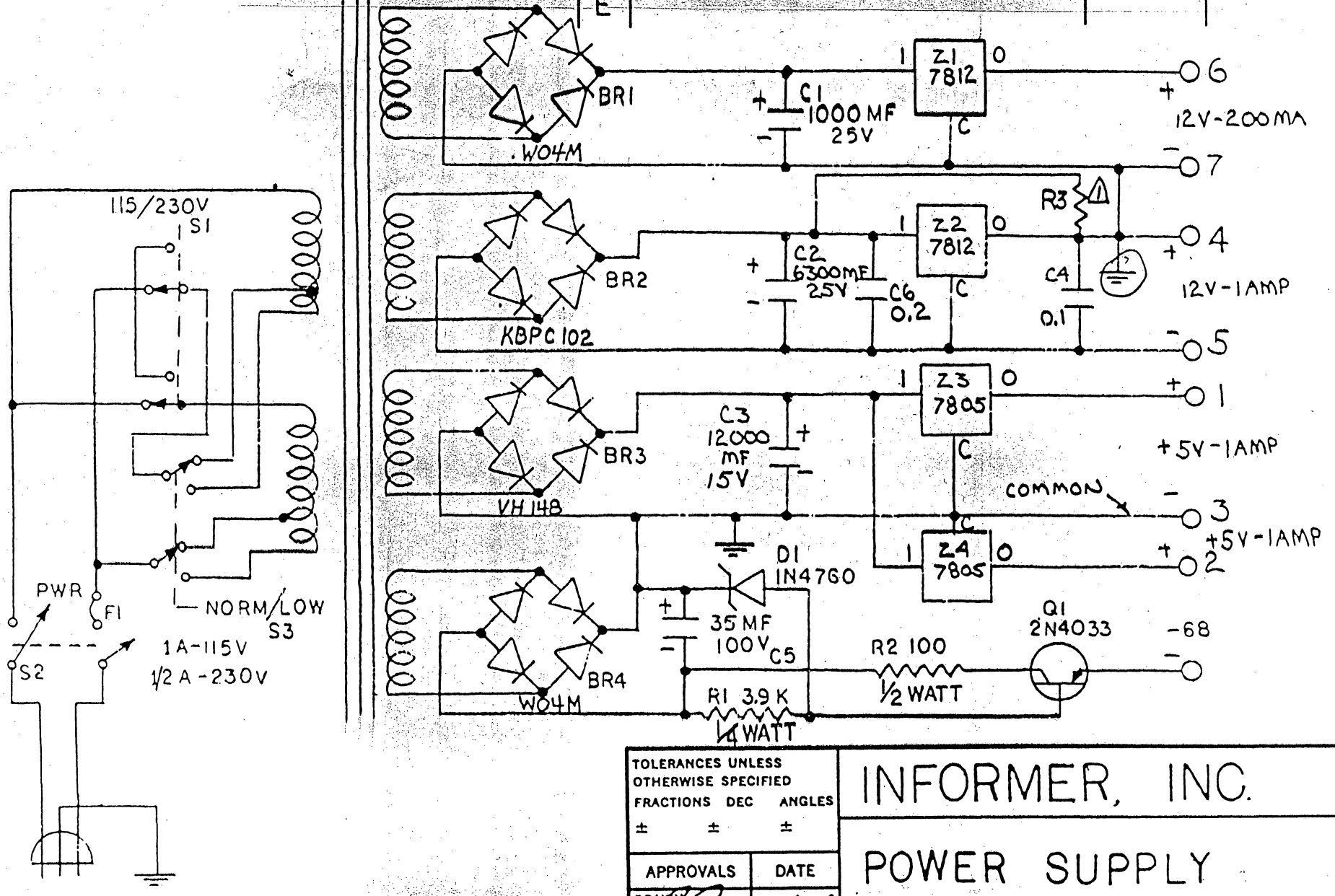
(1) R25 IS 100K FOR D4012; FOR OTHER MODELS SELECT IN TEST, 100K OR 150K

NOTES:

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES	INFORMER INC. LA. CA.	
APPROVALS / DATE	HORIZONTAL & VERTICAL VIDEO -12V	
DRAWN 10/9/72	FIG. NO 1.2-3	SIZE C
CHECKED 11/14/72		DRAWING NO 85003
ENG 3/2/73	DO NOT SCALE DRAWING	SHEET 1


EXT. DATA
ENABLE EXT.
ENABLE KYBD.
KYBD. DATA
BAUD X16
WRITE BLANK
STOP TRANS
BELL
START TRANS
RELEASE
SEND
TAB
DISPLAY STROBE
LOAD MEMORY
WRITE ADDRESS ENABLE
IC FGND CLEAR
MASTER RESET
MR
F/B SET
WRITE RESET
CURSOR CONTROL
FIG 2.4-1
8302-004
DWG. NO. 85166
302-004

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
E			



⚠ R3 IS 20 OHM 15W AND IS USED ONLY WITH B401 006 MEMORY BOARD

NOTE:

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

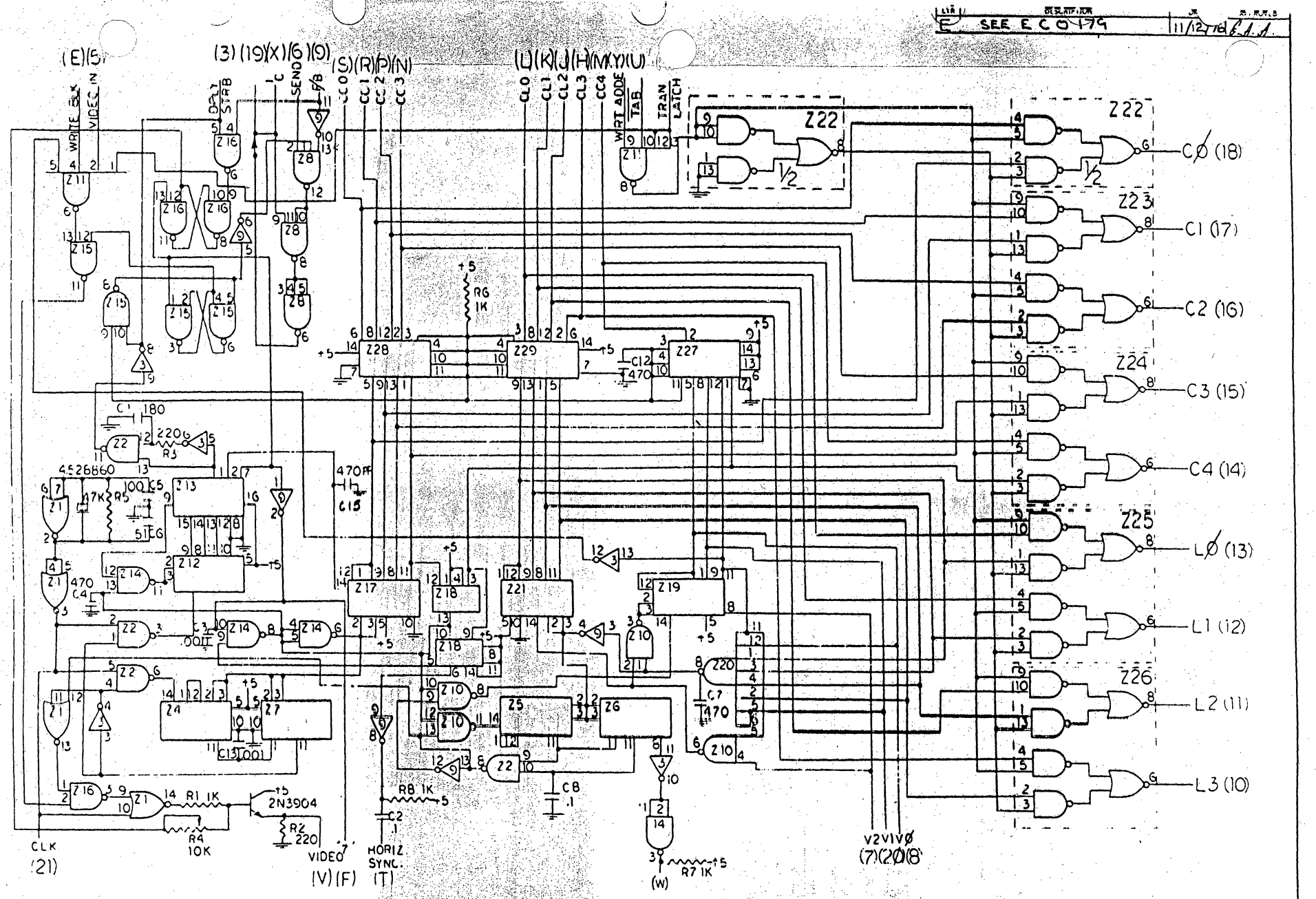
APPROVALS	DATE
DRAWN	10/28/76
CHECKED	11/23/76

INFORMER, INC.

POWER SUPPLY

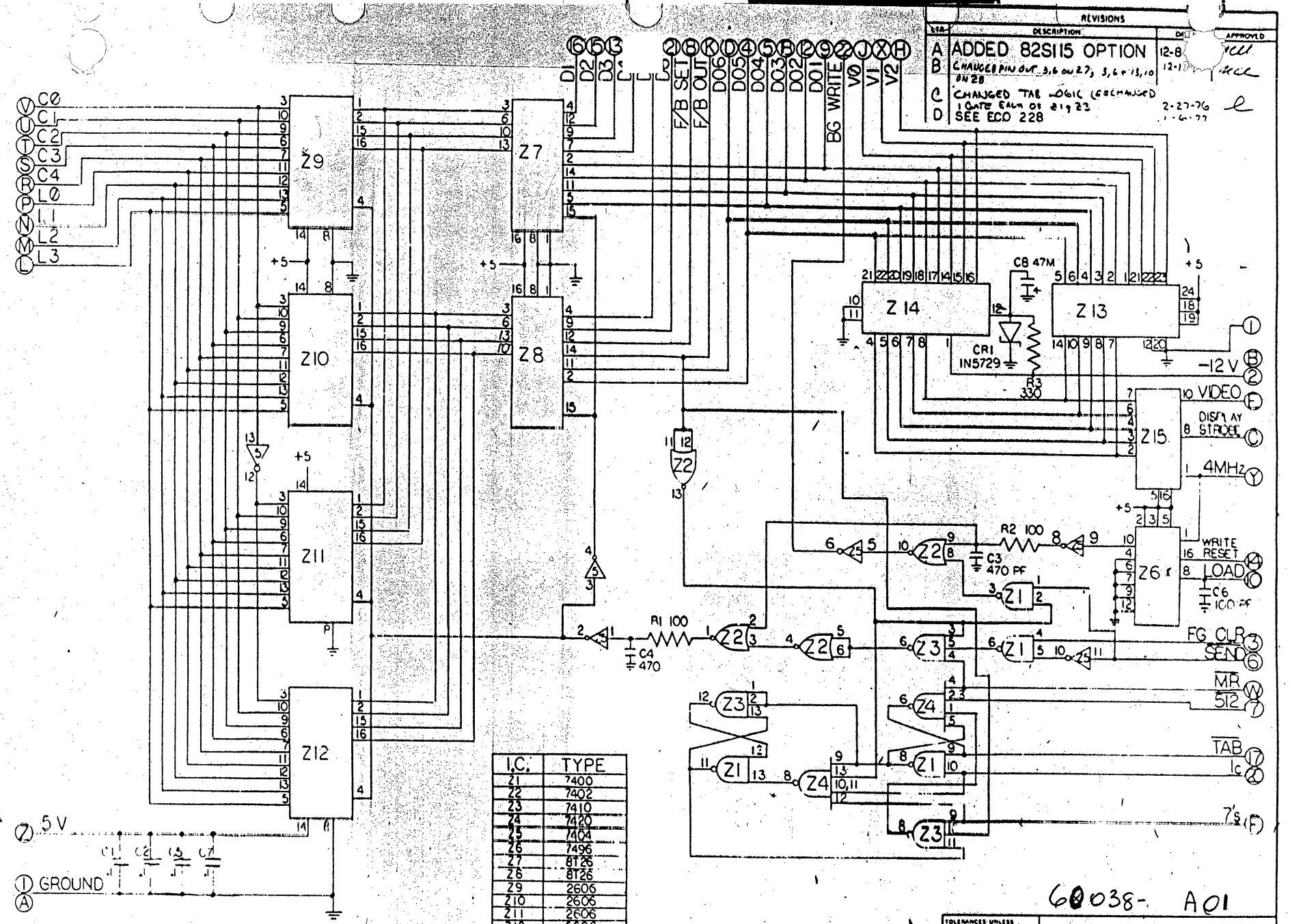
FIG. NO.	SIZE	DRAWING NO.
2.1-2	A	85008

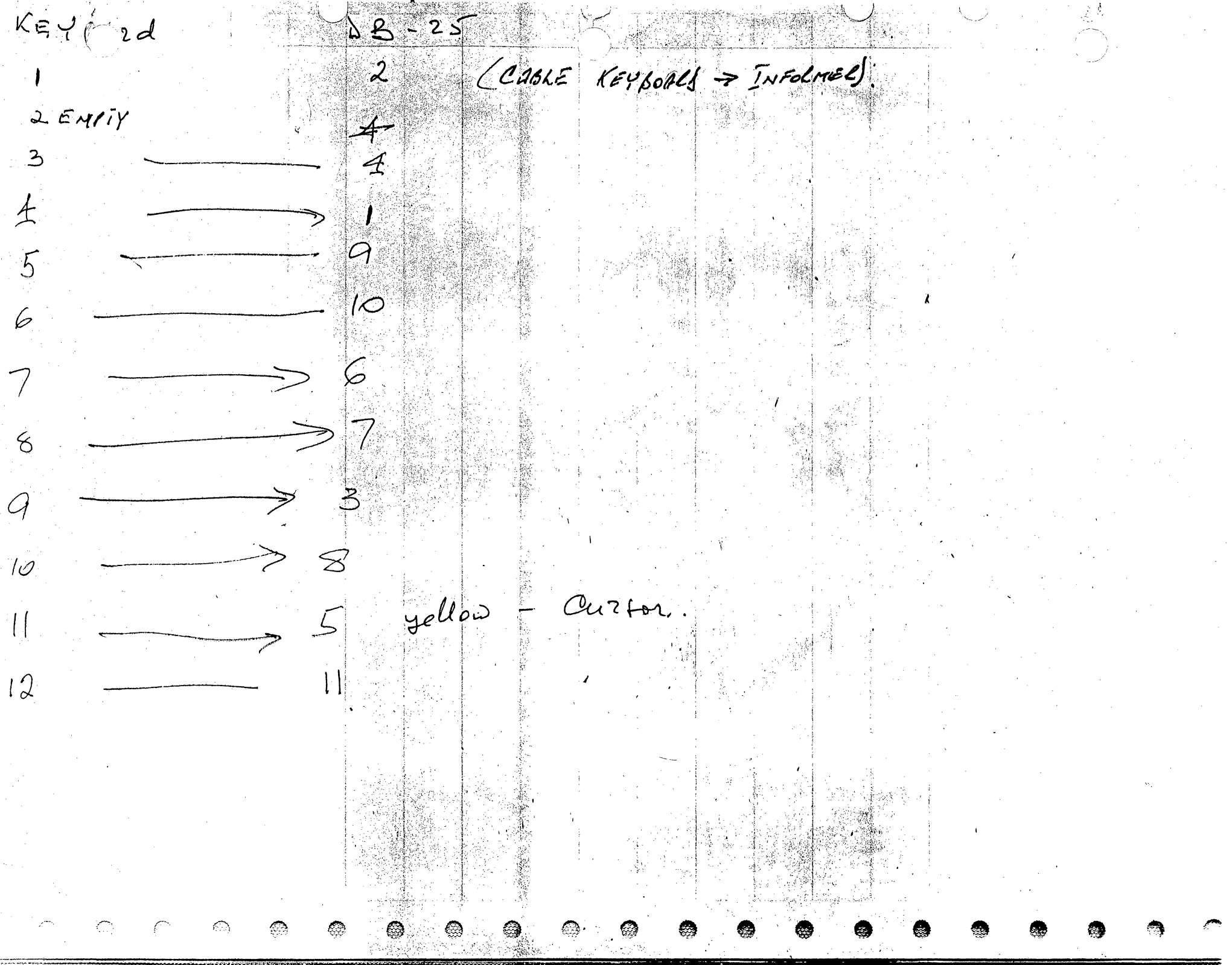
DO NOT SCALE DRAWING | SHEET 1 of 1



Z1 - SP381	Z6 - 74LS93	Z11 - 74LS20	Z16 - 74LS00	Z21 - 74LS93	Z26 - 74LS51
Z2 - 74LS00	Z7 - 74LS93	Z12 - 74LS93	Z17 - 74LS93	Z22 - 74LS51	Z27 - 8242
Z3 - 74LS04	Z8 - 74LS10	Z13 - 74LS42	Z18 - 74LS107	Z23 - 74LS51	Z28 - 8242
Z4 - 74LS93	Z9 - 74LS04	Z14 - 74LS00	Z19 - 74LS93	Z24 - 74LS51	Z29 - 8242
Z5 - 74LS93	Z10 - 74LS00	Z15 - 74LS00	Z20 - 74LS30	Z25 - 74LS51	

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES		INFORMER INC LA.CA.	
APPROVALS	DATE	TIMING AND CONTROL LOGIC D302-015	
DR BB	11/12/76	FIG. NO. 23-1	SIZE C
CHECKED		DRAWING NO 85165	
		DO NOT SCALE DRAWING	SHEET

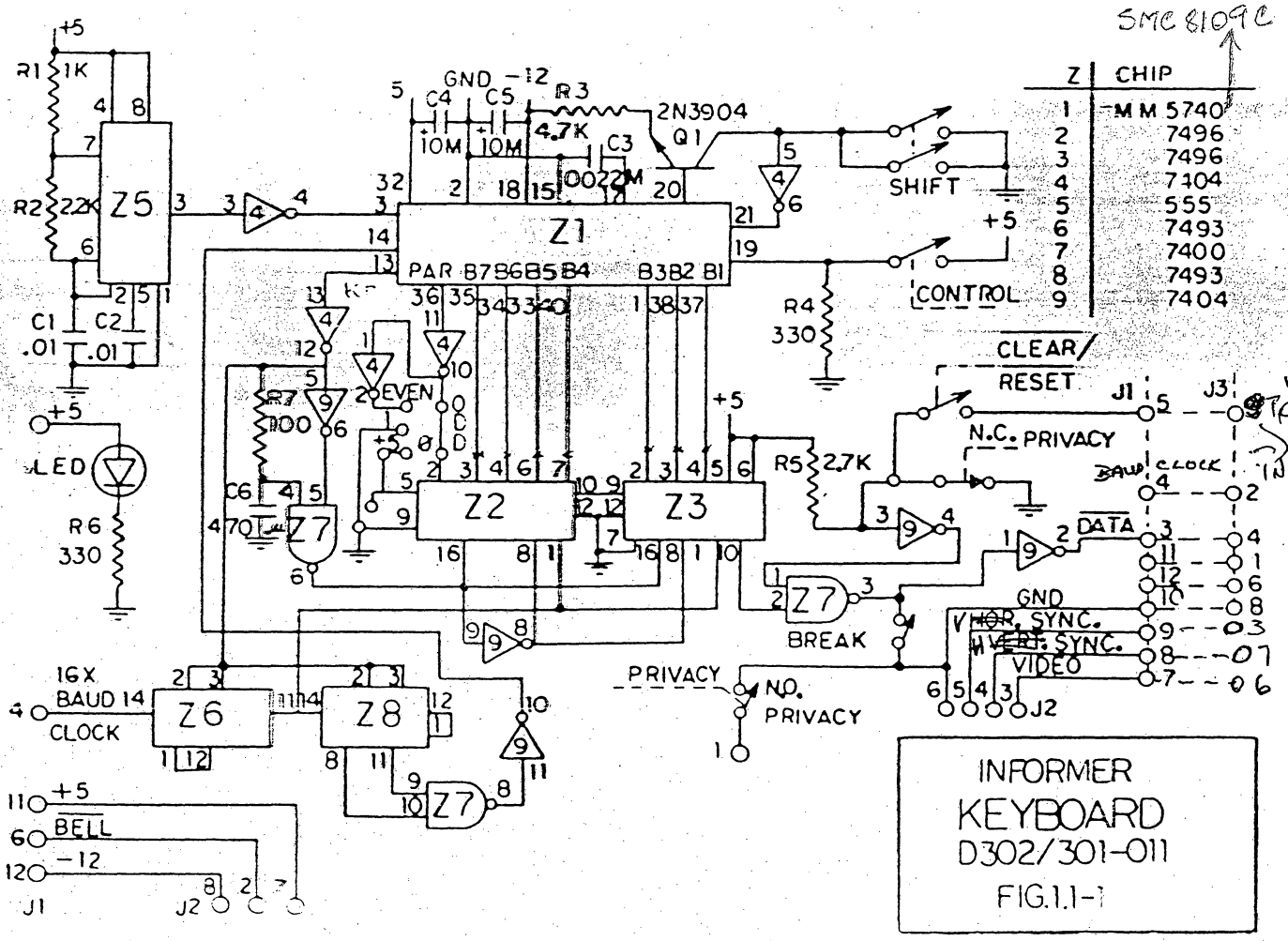

REVISIONS
A ADDED 82S115 OPTION 12-8
B CHANGED PIN OUT 3,6 ON Z7, 3,6 + 13,10 ON Z8 12-10
C CHANGED TAB LOGIC (EACH CHANGED 1 GATE EACH OF Z1, Z3) 2-27-76
D SEE ECO 228 1-6-77
D1 D2 D3 C4 C5 C6 F/B SET F/B OUT D06 D05 D04 D03 D02 D01 BG WRITE V0 V1 V2
C0 C1 C2 C3 C4 L0 L1 L2 L3
Z9 Z7 Z10 Z8 Z11 Z12
Z14 Z13 Z15 Z6 Z2 Z1 Z3 Z4 Z5
C8 47M
CR1 IN5729
R3 330
R1 100
R2 100
C3 470 PF
C4 470
C6 100 PF
+5
-12 V
VIDEO
DISPLAY STROBE
4MHz
WRITE RESET
LOAD
FG CLR
SEND
MR
512
TAB
Ic
7's
5 V
GROUND
C1 C2 C3 C4
I.C. TYPE
Z1 7400
Z2 7402
Z3 7410
Z4 7420
Z5 7404
Z6 7496
Z7 8T26
Z8 8T26
Z9 2606
Z10 2606
Z11 2606
Z12 2606
Z13 82S115
Z14 2513
Z15 7496
OR D302-006 (CAN BE SUBST.)
60038-A01
INFORMER INC.
MEMORY
D302-016
FIG. NO. 2.5-1
SIZE C
DRAWING NO 05037
DO NOT SCALE DRAWING
SHEET 1 OF 1


KEY (2d
DB-25
(CABLE KEYBOARD → INFORMER).
1
2
2 EMPTY
4
3
4
4
1
5
9
6
10
7
6
8
7
9
3
10
8
11
5
yellow - cursor.
12
11

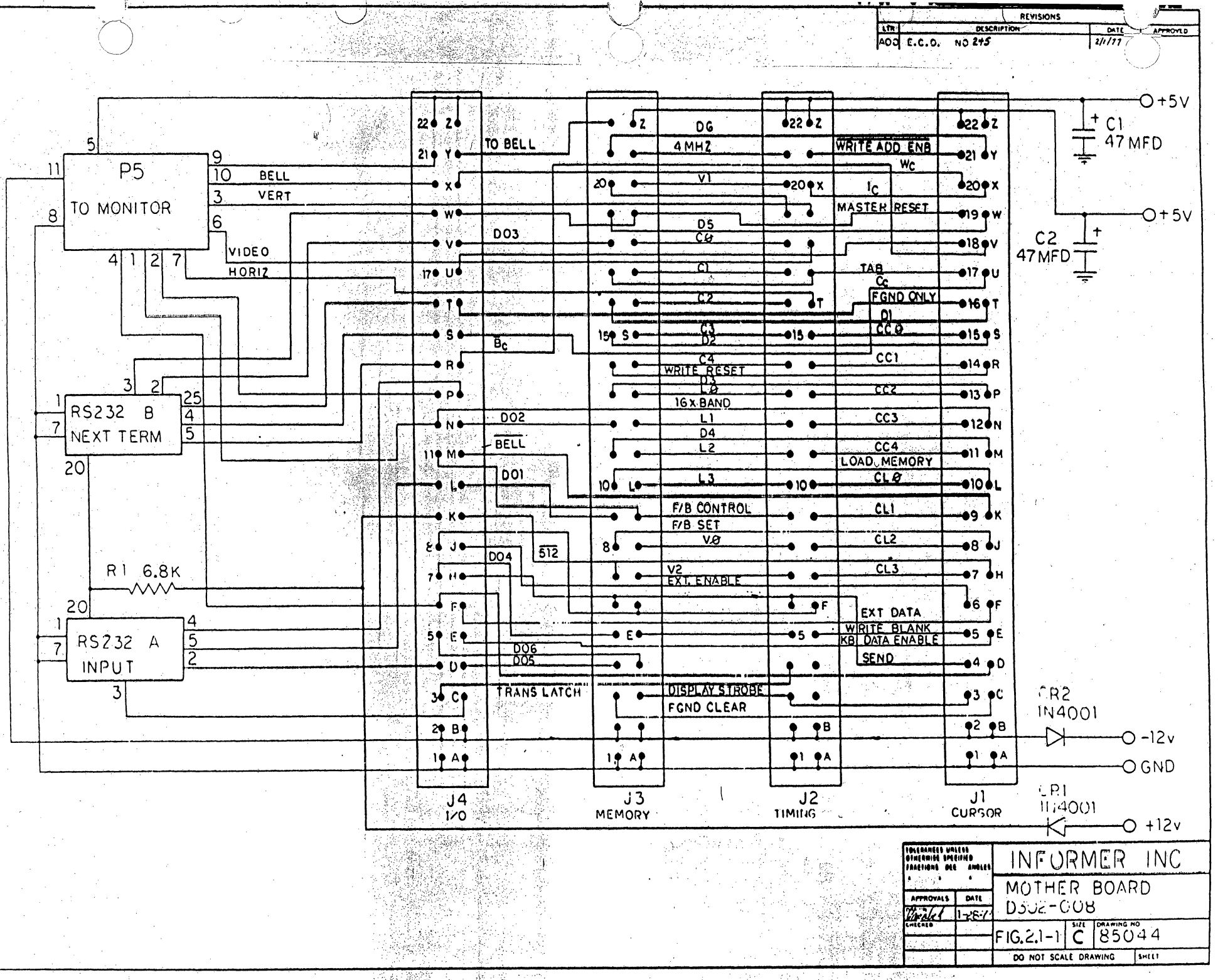
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D	SEE ECO 174	10/75	

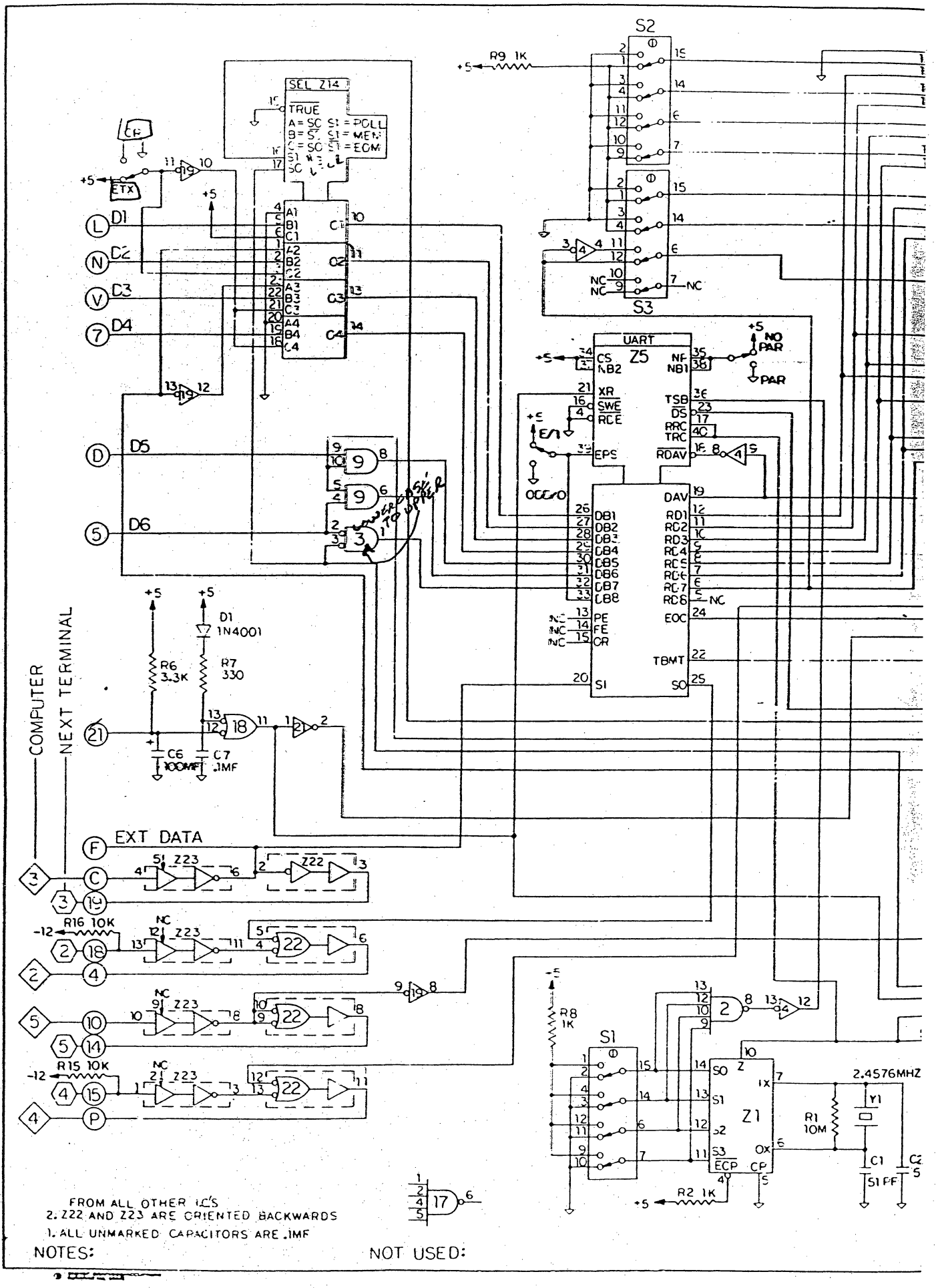
KEY CAPTION ROW 1	RESET/VLR	HOME	: -	" 2	# 3	$ 4	% 5	& 6	' 7	(8	) 9	0	+/- :/-	= -		7	8	9
JUMPS Z1 FROM PIN	J1-5	6	4	5	6	7	7	8	8	9	9	10	10/11	11		12	12	12
TO PIN	R5	23	22	22	22	22	23	23	22	22	23	23	22/22	22		22	23	31
KEY CAPTION ROW 2	END JOB	→	Q	W	E	R	T	Y	U	I	← O	P	LF/CR	CR/SEND		4	5	6
JUMPS Z1 FROM PIN	4	6	4	5	6	7	7	8	8	9	9	10	10/11	11/6		12	12	12
TO PIN	25	27	24	24	24	24	25	25	24	24	25	25	24/24	24/30		24	25	30
KEY CAPTION ROW 3	FG CLR CTL	←	CTL [:	A	S	D	F	G	H	J	K	L	+ ;	RUB OUT	BRK TAB	1	2	3
JUMPS Z1 FROM PIN	7/45	12	+5/10	4	5	6	7	7	8	8	9	9	13	10	GND/11	12	12	12
TO PIN	30/19	28	19/22	26	26	26	26	27	27	26	26	27	27	26	Z9-1/10	26	27	28
KEY CAPTION ROW 4	OPT/TAB	↑	SFT	Z	X	C	V	B	↑ N	M	< ,	> .	? /	SHIFT		0		.
JUMPS Z1 FROM PIN	6/11	6	GND	4	5	6	7	7	8	8	9	9	10	GND		12		10
TO PIN	29/30	25	Z4-5 Q1-C	28	28	28	28	29	29	28	28	29	29	Z4-5 Q1-C		29		28
KEY CAPTION ROW 5	OP2/SND	↓																
PIN	6	10						11										
TO PIN	30	24						29										

NOTE
* TYP. 7 PLACES FOR HALF OF KEYCAP FOR D301 AND BOTTOM FOR D302

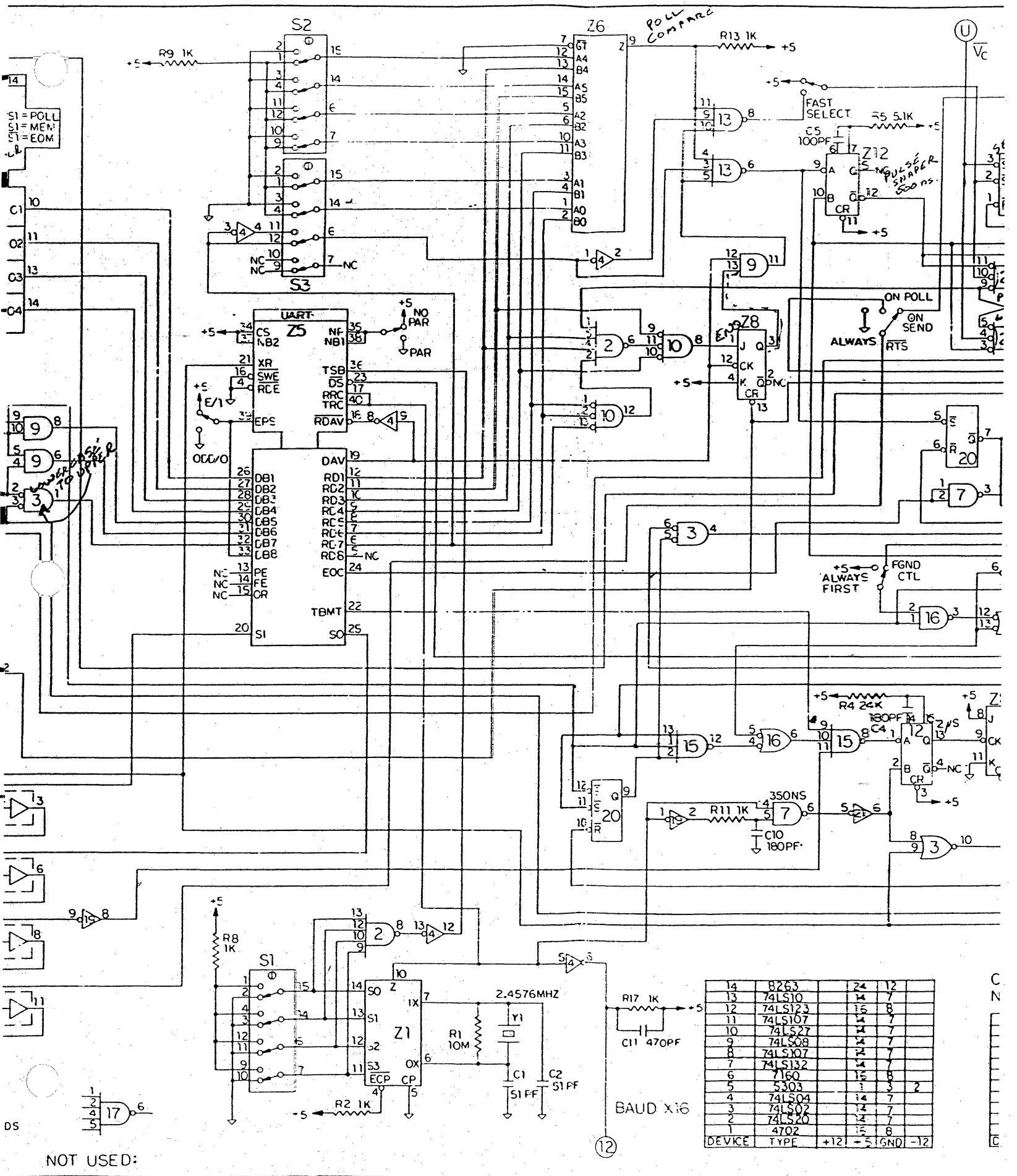


INFORMER
KEYBOARD
D302/301-011
FIG. 1.1-1


REVISIONS
LTR DESCRIPTION DATE APPROVED
A00 E.C.O. NO 245 2/1/77
P5
TO MONITOR
BELL
VERT
VIDEO
HORIZ
RS232 B
NEXT TERM
RS232 A
INPUT
R1 6.8K
TO BELL
DO3
Bc
DO2
BELL
DO1
DO4
512
DO6
DO5
TRANS LATCH
DG
4MHZ
V1
D5
C0
C1
C2
C3
D2
C4
WRITE RESET
D3
L0
16X BAND
L1
D4
L2
L3
F/B CONTROL
F/B SET
V0
V2
EXT. ENABLE
DISPLAY STROBE
FGND CLEAR
WRITE ADD ENB
Wc
Ic
MASTER RESET
TAB
Cc
FGND ONLY
D1
CC0
CC1
CC2
CC3
CC4
LOAD MEMORY
CL0
CL1
CL2
CL3
EXT DATA
WRITE BLANK
KB DATA ENABLE
SEND
+5V
C1
47 MFD
+5V
C2
47MFD
CR2
IN4001
-12v
GND
CR1
IN4001
+12v
J4
I/O
J3
MEMORY
J2
TIMING
J1
CURSOR
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
APPROVALS DATE
CHECKED
INFORMER INC
MOTHER BOARD
D502-008
FIG. 2.1-1
SIZE C
DRAWING NO 85044
DO NOT SCALE DRAWING
SHEET

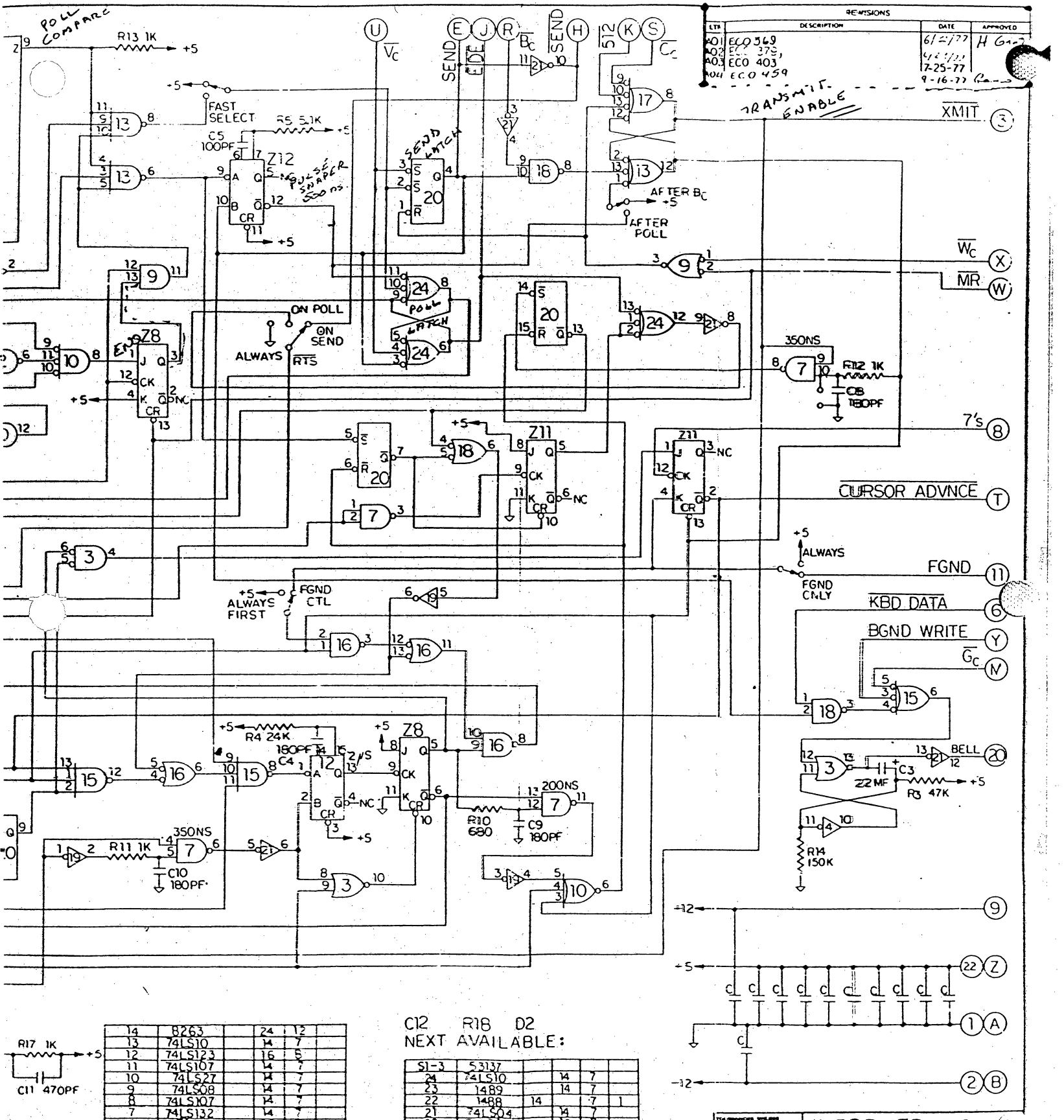

S2
R9 1K
SEL Z14
TRUE
A = SC S1 = POLL
B = S S1 = MEM
C = SC S1 = EOM
ETX
D1
D2
D3
D4
D5
D6
S3
UART
Z5
NO PAR
PAR
TBMT
EOC
DAV
RDAV
D1
1N4001
R6
3.3K
R7
330
C6
100MF
C7
.1MF
COMPUTER
NEXT TERMINAL
EXT DATA
R16 10K
R15 10K
R8
1K
S1
Z1
2.4576MHZ
R1
10M
Y1
C1
51 PF
R2 1K
FROM ALL OTHER I.C'S
2. Z22 AND Z23 ARE ORIENTED BACKWARDS
1. ALL UNMARKED CAPACITORS ARE .1MF
NOTES:
NOT USED:

60100



DEVICE	TYPE	+12	+5	GND	-12
14	8263		24	12	
13	74LS10		14	7	
12	74LS123		16	8	
11	74LS107		14	7	
10	74LS27		14	7	
9	74LS08		14	7	
8	74LS107		14	7	
7	74LS132		14	7	
6	7160		16	8	
5	5303		3	2	
4	74LS04		14	7	
3	74LS02		14	7	
2	74LS20		14	7	
1	4702		16	8	

60100-A03



DEVICE	TYPE	+12	+5	GND	-12
14	8263		24	12	
13	74LS10		14	7	
12	74LS123		16	5	
11	74LS107		14	7	
10	74LS27		14	7	
9	74LS08		14	7	
8	74LS107		14	7	
7	74LS132		14	7	
6	7160		16	5	
5	5303		1	3	2
4	74LS04		14	7	
3	74LS02		14	7	
2	74LS20		14	7	
1	4702		16	5	

C12 R18 D2
NEXT AVAILABLE:

DEVICE	TYPE	+12	+5	GND	-12
S1-3	53137				
24	74LS10		14	7	
23	1489		14	7	
22	1488	14		7	1
21	74LS04		14	7	
20	74LS279		16	8	
19	74LS04		14	7	
18	74LS00		14	7	
17	74LS20		14	7	
16	74LS00		14	7	
15	74LS10		14	7	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
601	ECO 369	6/21/77	H Gray
602	ECO 378,	6/21/77	
603	ECO 403	7-25-77	
604	ECO 459	9-16-77	

INFORMER INC.
D302 UNIVERSAL I/O
60100 A03
FIG 2.2-7
SIZE D
85168
DO NOT SCALE DRAWING
SHEET

MODIFICATION OF THE INFORMER TERMINAL FOR A STAND ALONE RS232 SYSTEM

PART 1 : Bypassing the Polling and Send circuitry

Use the included schematics and partial board layouts to aid in making the modifications.

Modifying the UNIVERSAL I/O BOARD

STEP 1: Disconnect the serial output of the UART from the RS232 output by cutting the designated traces. Jumper the RS232 converter (pin 5 of Z22) to the serial KBRD DATA (pin 3 of Z18).

STEP 2: Disconnect the SEND Enable from $\overline{\text{KBRD DATA}}$ gate so that keyboard data will always be available at the RS232 output (remove pin 2 of Z18 from the PC board by desoldering or by cutting it).

Modifying the CURSOR CONTROL BOARD

STEP 3: Enable serial $\overline{\text{EXTERNAL DATA}}$ "OR" $\overline{\text{KEYBOARD DATA}}$ to the video display memory all the time (independent of SEND) by cutting the $\overline{\text{ENABLE EXT.}}$ and the $\overline{\text{ENABLE KBRD}}$ lines and grounding pins 3 and 6 of Z26.

The terminal should now function with an RS232 device connected to the female EIA connector as shown in FIGURE 1. Set the Baud Switch on the end of the I/O BOARD (shown in FIGURE 2) to the desired setting according to the chart in the APPENDIX of the Manual. Parity is a function of the jumper on the Keyboard Printed Circuit.

PART 2 : Adding a Scrolling Circuit

The following additional circuitry and modifications are not totally effective. Because the display memory is wrap-around, the line that is scrolled off the screen at the top is not erased but appears at the bottom of the screen . This isn't a great problem if the sending device writes new information on each line, but if it skips a line the old unerased line appears sandwiched between the new information.

If used with a small computer, a software approach to scolling might be simpler. 512 bytes of computer memory could be set aside for a duplicate display memory which could be manipulated easily by changing the address offset and then rewriting it into the terminal's display memory. The last line could be erased before rewriting. This would also allow more than one page of memory to exist if more computer memory is available. Don't overlook the extensive cursor control codes that could also be used by the computer to manipulate the terminal's display memory. (see the APPENDIX of the Manual). If you choose the hardware approach carefully follow the next steps using the included schematics and partial board layouts as a guide.

Cursor Control Board Modification

STEP 4: Cut the trace that feeds the downcount input of the Cursor Line Counter (pin 4 of Z28) to allow insertion of the Scrolling Circuit"B". Connect 2 jumpers to the edge-connector terminals 'E' and '6' to allow the added circuitry to be connected via the Mother Board.(These 2 terminals were formerly used by the now-disconnected ENABLE EXT and ENABLE KYBD lines.)

Mother Board Modification

STEP 5: Cut the traces to terminals 'E' and '6' of J1 (CURSOR) and connect 'E', '6' and 'H' to the appropriate points on the Scrolling Circuit "B". (note that the trace for terminal '6' is on the backside of the Mother Board which can be reached if all the boards are removed)

STEP 6: Cut the traces (labelled LØ, L1, L2, and L3 on the Mother Board schematic) on both sides of the Mother Board and connect the Scrolling Circuit "A" to the designated terminals. This effectively inserts the scroll count plus the line count as the effective line address to the display memory.

Description of scrolling circuits

The screen is effectively scrolled by adding a one-line offset to the line counter address each time the cursor exceeds the last character position on the screen (the 512th character position). This is accomplished by a 4-bit counter which is incremented by the 512 character detection circuitry and a 4-bit parallel adder.

The character line address lines LØ, L1, L2, and L3 are active low so must be inverted before and after the parallel adder. This is accomplished by the 7404 hex inverter and half of the 7400 quad Nand gate.

Since the 512th character detect also resets the cursor line counter to zero, the cursor would always appear in the HOME position after a line is scrolled. This is prevented by delaying the $\overline{512}$ pulse and applying it to the down-count input of the cursor line counter bringing the counter back to 15 and placing the cursor at the beginning of the last line on the screen after each scroll. This is accomplished by the One-shot and OR'd with the normal cursor down-count control.

The original scrolling circuit was constructed on a piece of Vector Board 1.5" x 4" and attached to the terminal circuits via the Mother Board terminals following the modifications outlined above.

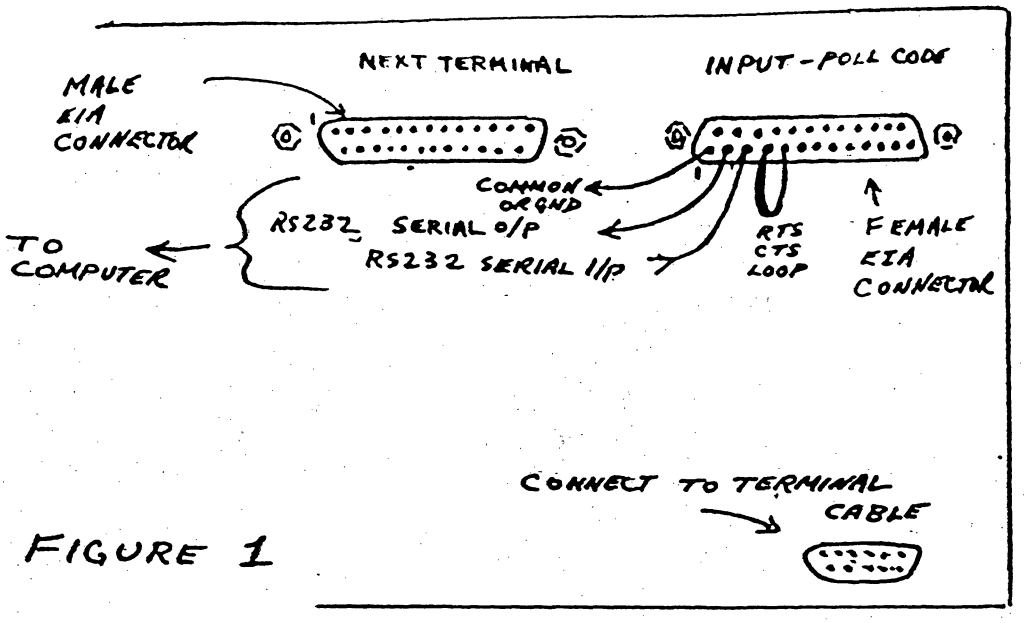


FIGURE 1

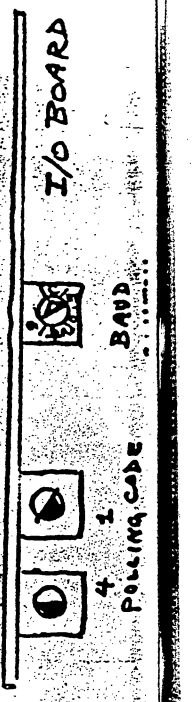
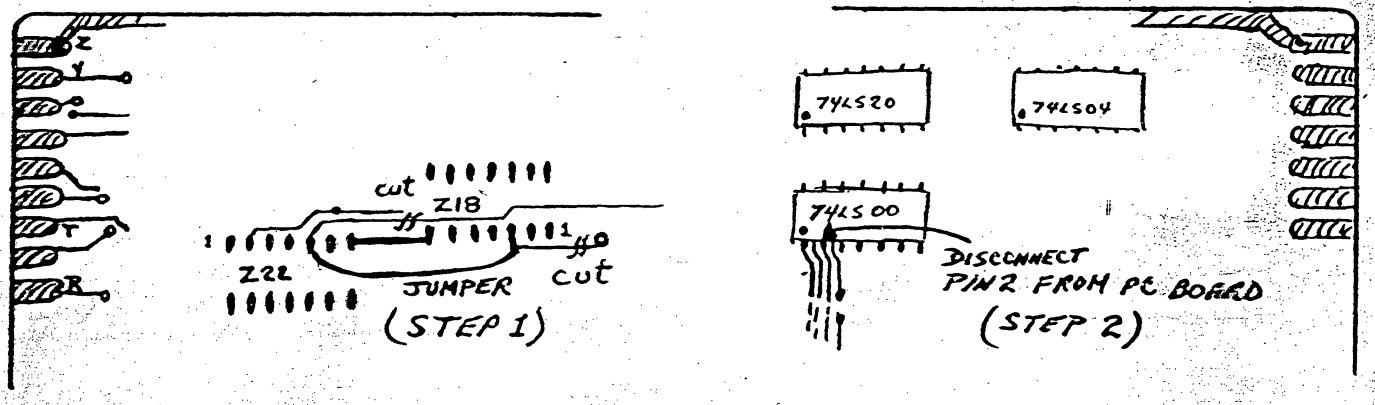


FIGURE 2

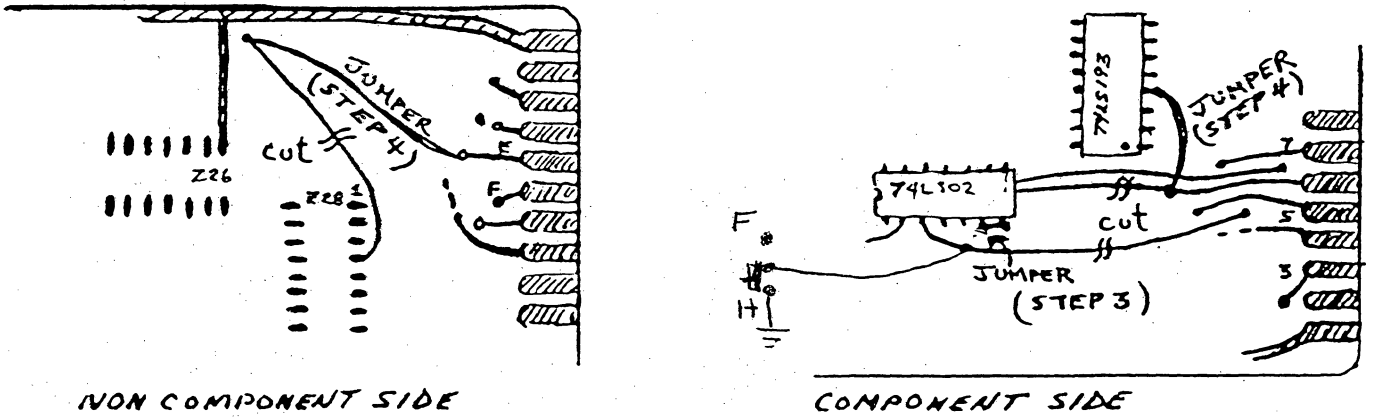
FIGURE 3 PARTIAL LAYOUT OF UNIVERSAL I/O BOARD



NON COMPONENT SIDE

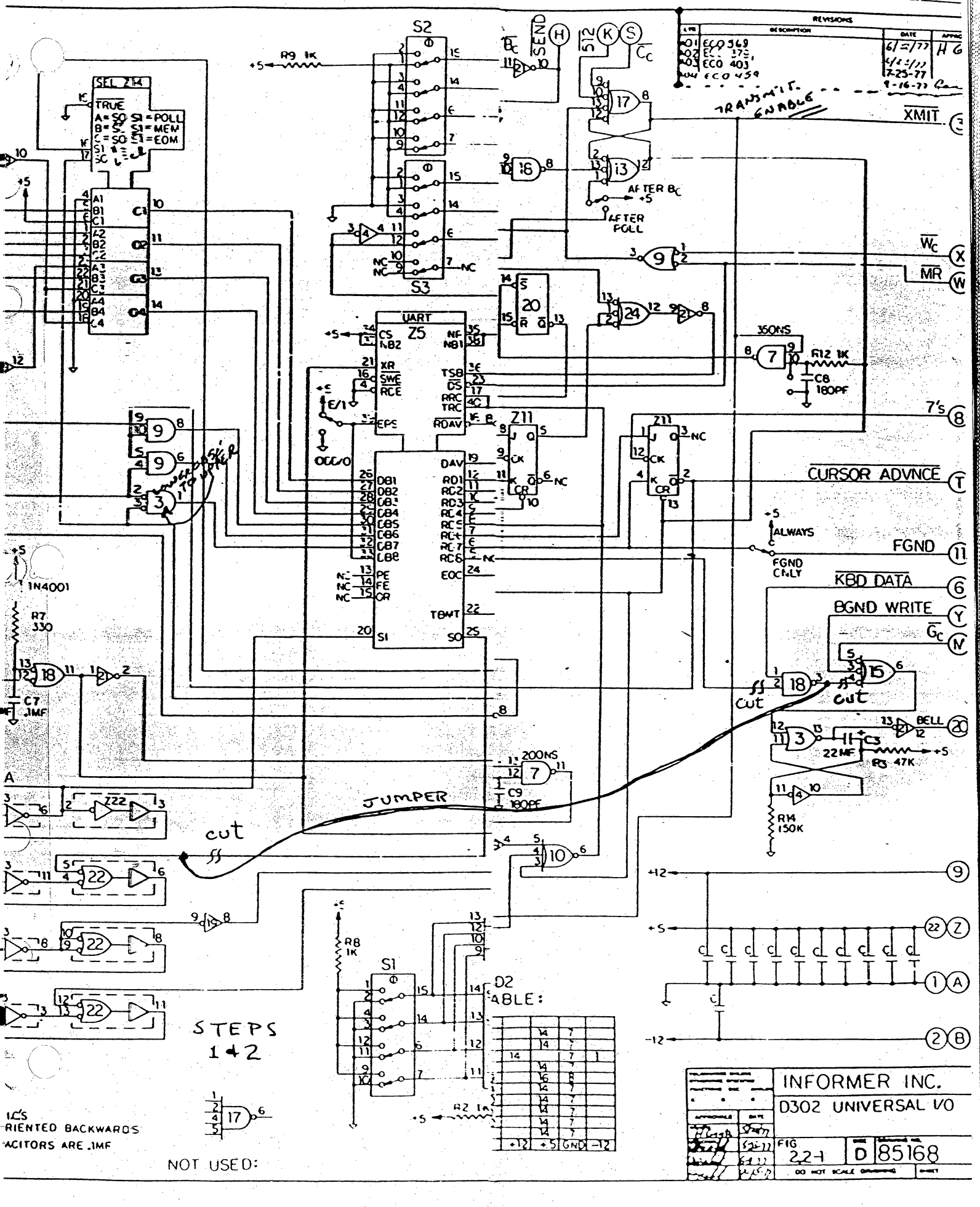
COMPONENT SIDE

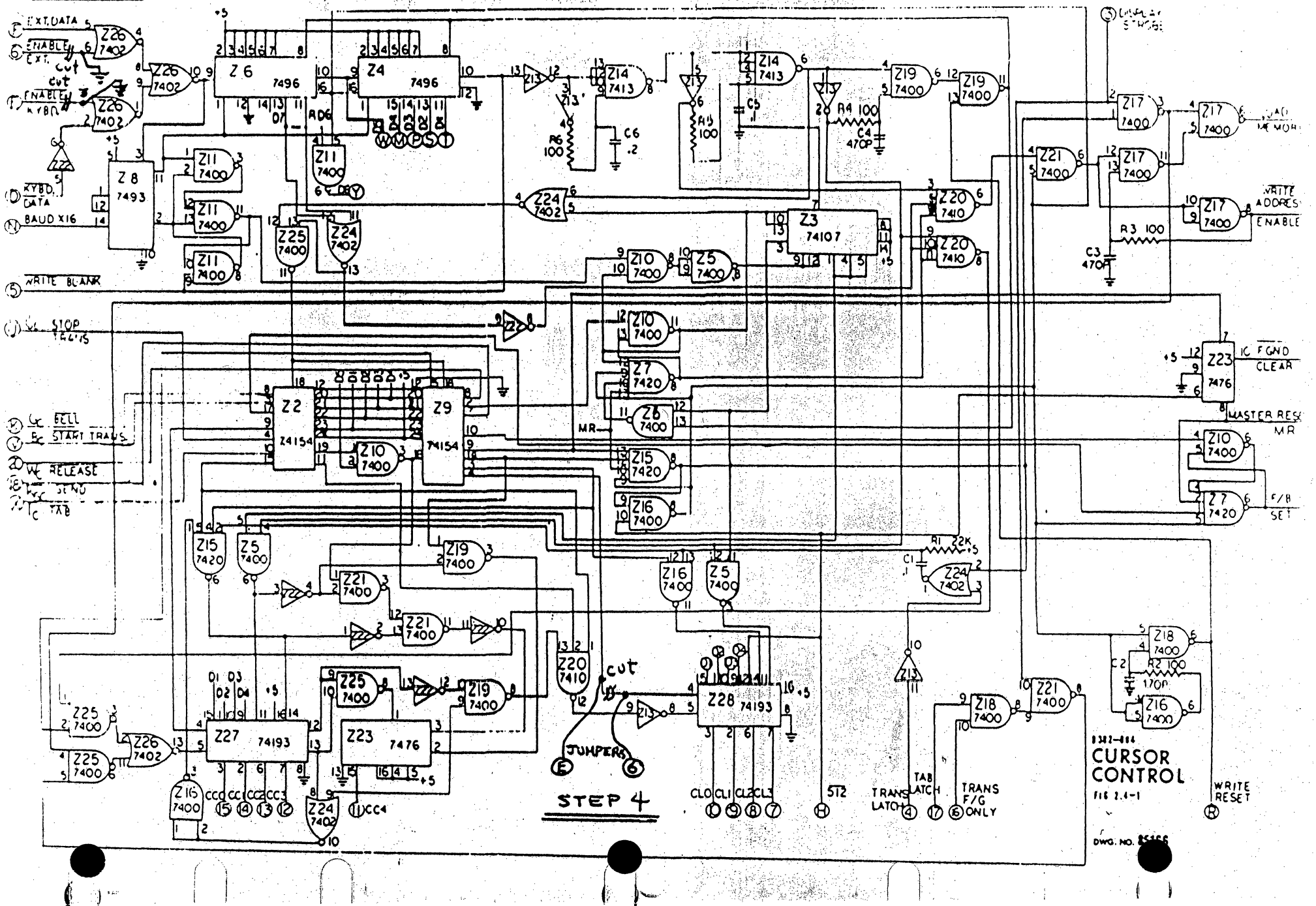
FIGURE 4 PARTIAL LAYOUT OF CURSOR CONTROL BOARD



NON COMPONENT SIDE

COMPONENT SIDE


REVISIONS
ECO 369
ECO 403
ECO 459
6/1/77
4/25/77
7-25-77
9-16-77
TRANSMIT ENABLE
XMIT
SEL 2M
TRUE
A=SO S1=POLL
B=S1 S1=MEM
C=SO S1=EOM
S2
S3
SEND
AFTER BC
AFTER POLL
UART
Z5
Z11
Z22
WC
MR
350NS
R12 1K
C8 180PF
7's
CURSOR ADVNCE
ALWAYS
FGND
FGND ONLY
KBD DATA
BGND WRITE
GC
cut
BELL
22MF
R13 47K
R14 150K
200NS
C9 180PF
JUMPER
1N4001
R7 330
C7 .1MF
R8 1K
S1
D2
CABLE:
R2 1K
+12
+5
GND
-12
STEPS 1+2
NOT USED:
ICS ORIENTED BACKWARDS
CAPACITORS ARE .1MF
INFORMER INC.
D302 UNIVERSAL I/O
FIG 2.2-1
D
85168
DO NOT SCALE DRAWING


5
STEP 3
EXT. DATA
ENABLE EXT.
cut
cut
ENABLE KYBD
KYBD. DATA
BAUD X16
WRITE BLANK
STOP BITS
BELL
START TRANS
RELEASE
STND
TXB
Z26 7402
Z8 7493
Z6 7496
Z4 7496
Z11 7400
Z25 7400
Z24 7402
Z10 7400
Z5 7400
Z3 74107
Z14 7413
Z19 7400
Z20 7410
Z21 7400
Z17 7400
Z18 7400
Z16 7400
Z15 7420
Z7 7420
Z2 74154
Z9 74154
Z23 7476
Z27 74193
Z28 74193
Z13
R1 22K
C1
R2 100
C2 170P
R3 100
C3 470P
R4 100
C4 470P
R5 100
C5
C6 .2
MR
IC FGND CLEAR
MASTER RES MR
F/B SET
WRITE ADDRES ENABLE
JUMPER
STEP 4
CLO CL1 CL2 CL3
512
TRANS LATCH
TAB LATCH
TRANS F/G ONLY
WRITE RESET
CURSOR CONTROL
FIG 2.4-1
DWG. NO. 85466

1.0 Monitor Assembly

The Data Entry Informer is composed of several major assemblies. The desk top Monitor consists of a display unit and a keyboard.

The connecting cable between the Monitor and the Control Unit supplies +5 volts, -12 volts, and ground to operate the Monitor display unit and provide power for the keyboard encoder and the conversion logic. In addition, horizontal, vertical and video signals are brought to the display unit. A multiple of the baud rate clock and power for the bell are also provided from the Control Unit. The Monitor generates the ASCII coded data, using the keyboard and baud rate clock, and sends this to the Control Unit. One key has its contacts on the Monitor carried to the Control Unit on a separate wire for various options such as local clear, reset, etc.

1.1 Keyboard

The Keyboard Assembly (Figure 1.1-1) consists of a group of single pole, single throw, cross bar contact switches, one corresponding to each character. Each switch, when depressed, provides a jumper path between two pins on a MOS encoder circuit.

The encoder circuit uses a dynamic scanning technique to detect and pinpoint keyswitch activity on the keyboard. In this method, two ring counters are employed. A 9-bit x counter monitors the rows of the switch matrix while the columns are monitored by a 10-bit Y counter. Since there are 9 x 10 possible counter states, ninety data switches may be defined by their X-Y coordinates.

Every scan time (90-bit times), all keys are interrogated in turn to determine their status. Each particular key is interrogated every 90-bits or once each keyboard scan cycle. This is implemented by employing the X counter as drivers to drive the sensing of each column of the switch matrix. Therefore, if a switch is closed it will be detected when its row (X coordinate) is driven and its column (Y coordinate) is sensed. This corresponds to the particular X-Y time (one of 90 time slots in the scan) defining the closed switch. A key detect pulse at the X-Y time in question is issued and this is used to define the status of that particular key and generates a coded bit pattern.

In addition to scanning the key switch matrix, the X and Y counters are used to scan the contents of a Read Only Memory which contains the bit pattern for each key switch. For example, when switch X_1, Y_1 is being interrogated (at X_1-Y_1 time) the counters are addressing the memory location in the ROM which contains the code for switch X_1Y_1. If the key is closed, a key detect pulse will be issued. At this time, the ROM contents are strobed into latches which then hold the code pattern for key X_1, Y_1. It should be noted that the scanning of the switch matrix and ROM occur simultaneously and repetitively. The clocks are never stopped; information is obtained dynamically.

1.1 Keyboard (Continued)

For each keyswitch it is possible to have four modes. These are determined by the status of the SHIFT and CONTROL keys. There are four possible code patterns for each key as determined by the mode switches. These code patterns are related in that, for any key, in any of its modes, only four of its 9-bits may vary. All code patterns are programmed at the time of manufacturing, using a single mask variation.

The keyboard encoder chip may be either an N-key rollover type or a two key lockout type. N-key rollover is defined as the ability to issue a code each time a new key is depressed, regardless of the status of all other keys. This means that each time a new key is depressed, a code for that key would be issued even if other keys are still depressed. This type of rollover is ideal for fast typing applications, since no training is required to release the currently depressed key before a new one is depressed. Even in slower typing applications, burst typing of typical trigrams such as "THE" and "ERE" can be a problem if N-key rollover is not employed.

N-key rollover is accomplished by remembering the status of each key on the previous scan cycle. This is achieved by using a 90-bit shift register whose input is the key detect signal. If the input and output of the shift register are monitored, it is possible to compare the status of each key on the past scan (output of shift register) with its status on the current scan (input of shift register). A valid key closure is present only if the input of the shift register is true and its output false. A release is present when the input is false and the output is true. The other two cases (00 and 11) correspond to no change in status; either released or depressed. The ROM word is strobed into the output latches only when a valid key closure is detected.

Once a previously closed key is released it then becomes possible to accept it as a valid closure if it is depressed again. To preclude generation of erroneous codes through sneak paths when multiple keys are depressed, isolation diodes

are used with the "N" key rollover chips. When the keyboard is operated with the two key lockout encoder chip, output code generation is inhibited after the first key is depressed. An output code change from the next key will occur only after the first depressed key is released.

Since the codes are the same when generated by the same closures with either encoder, "N" key rollover units may be converted to two key rollover units by simply changing the encoder chip but not vice versa (because of the isolation diodes needed to prevent erroneous codes when using the N key rollover chip).

Keyswitches exhibit a bounce characteristic upon both depression and release. In normal operation, many keyboard scans could occur during the time of switch bounce. It is then necessary to make sure that this bounce is not recognized as multiple depressions and/or releases. As soon as the scanner detects a change in key status, an internal time delay is activated which instructs the encoder to ignore keyboard activity. At the end of the time out (usually several milliseconds) when switch bounce has subsided, the encoder resumes interrogating the switch matrix. The time delay is continuously variable with an external capacitance connected to Pin 17 of the encoder.

Before a soldering iron is used on the keyboard circuit board, the integrated circuit keyboard encoder should be protected against voltage transients by placing a conductive pad across the socket pins. The encoder chip is plugged into a socket so that it may be removed and replaced. Keys may be removed by removing the mounting screws and unsoldering pins as required.

A key-locked switch is provided which enables the keyboard transmission in one position and disables the keyboard while blanking the video in the other position. A BREAK key is normally provided to shift the output transmission from a mark to a space condition. Individual keys are provided as a convenience to generate specialized control (CONTROL and character) codes without requiring depression of two keys simultaneously.

1.1 Keyboard (Continued)

The keyboard schematic, Figure 1.1-1, indicates the encoder circuit, Z-1; pin connections corresponding to each key are shown. The cable from the control unit connects to J-1 and the cable to the Display Unit connects to J-2. The sampling clock required by the encoder is generated by Z-5, a free running multivibrator. When a key is selected, the encoder bits are strobed into shift registers A-2 and Z-3. The incoming Baud Clock (at 16 times frequency) is counted down by Z-6 before clocking the data out on Pin 3 of J-1.

1.2 Display Unit

The Display Unit is a compact plug-in package containing the cathode ray tube with its power supplies, the vertical deflection amplifier, the horizontal deflection amplifier, and the video amplifier. The DC power for the Display Unit is supplied by the Control Unit through the interconnecting cable. The Display Unit assembly also includes the CRT I/O board which contains the conversion circuitry* from the parallel keyboard data to serial data (where used), as well as the bell speaker (where used).

The three separate hardwired circuit boards used in the Display Unit are described individually below.

The horizontal deflection system is triggered by a timing pulse from the timing board. The pulse sets a one shot (Z1) whose on-time is determined by the horizontal drive (an internally adjusted) control. The one shot output is isolated by an inverter and used to turn on the horizontal driver transistor, Q1. This in turn provides sufficient power to turn on the horizontal transistor during the right hand side of the sweep. The lefthand portion of the sweep is supplied by stored energy controlled by the damper diode, D1. During horizontal flyback, high voltages are generated in the horizontal transformer, T2. Taps on the transformer provide pulses which are rectified to supply 550 volts for the cathode ray tube screen electrode, as well as high voltage, and 100 volts for the video amplifier.

The vertical deflection system utilizes a feedback amplifier triggered by the vertical sync pulse. When vertical sync arrives, it turns on transistors Q20 and Q21 which pull the base of Q22 to the -11 volt supply. The vertical pulse is differentiated to provide momentary pull down. The capacitor C26 then charges through the vertical size control to generate a sawtooth ramp. This is amplified and used to drive the vertical deflection yoke. A small feedback resistor, R30, samples the current in the yoke and provides feedback to the input to maintain vertical linearity. A

*On some models this circuitry is part of the keyboard assembly.

5 volt zener diode (D21) serves the dual purpose of setting the correct voltage levels and providing power for the horizontal driver one shot, Z1.

The video amplifier consists of a single transistor which is driven directly by the emitter follower on the timing board. Since the basic crystal clock provides a chopped signal, only high frequencies (4 megahertz) are presented to the amplifier. A peaking capacitor is placed in the emitter of the amplifier to boost the high frequencies. The output signal is applied to the cathode of the cathode ray tube. The gain of the video stage (contrast) is adjusted by a potentiometer in the emitter of the amplifier. The brightness control is normally set to keep the CRT beyond cutoff and the tube is illiminated only by the peaks of the video. As a result, the screen can be blanked by shorting the video signal to ground. During maintenance, it is possible to turn up the brightness and examine the deflection and CRT system independently of the video signals.

The CRT I/O board, which is permanently fastened to the Display Unit assembly, has contact fingers for a connector and cable supplying power, synch signals and video from the control unit via the keyboard.

2.0 Control Unit

The Control Unit contains all of the electronic circuitry with the exception of the cathode ray tube, deflection and video systems, and the keyboard encoding system. The circuitry, or logic, is contained on four plug-in printed circuit boards. A "mother board" contains the connectors and necessary interconnecting wiring. Two connectors with slide lock fasteners are provided -- one providing power and signals between the Control Unit and the desk top Monitor, and the other being a standard RS 232B connector for connection to a computer, data set, or teletype line. Wiring to the pins is shown in Figure 2.1-1.

2.1 Chassis

Approximately forty per-cent of the Control Unit is devoted to the system power supply shown on the schematic, Figure 2.1-2. A hidden switch, located under the unit, permits operation on 115 volt or 230 volt power lines. The installer may set this switch with a screwdriver prior to mounting the Control Unit on its mounting plate. The transformer and filter systems are designed to operate on either 50 or 60 Hz power lines. In order to operate the unit at minimum temperature under widely varying line voltages, a separate Normal/Low line switch is located in the plug-in logic board compartment. In the Low line position, the unit will operate down to 95 volts (190 volts if 230 volts nominal supply). In the normal position, the unit is designed to operate over a 105-125 volt range (215-250 for 230 volt nominal supply).

Up to five separate voltage supplies are built into a single circuit board. Each supply consists of bridge rectifier, input filter capacitor, and (where required) an integrated circuit regulator. Two of the supplies provide 5 volts at 1 ampere for logic circuitry with the regulators running off a common raw d.c. supply. All voltages on the power supply board are strapped with short wires to the mother board for distribution. A 1.0 ampere fuse is mounted just inside the dust cover. Each integrated circuit regulator is "short circuit proof."

The complex electronic functions are located on four plug-in circuit boards. All input/output functions are located on a single circuit board (Input/Output Logic Board, Figure 2.2-1).

Of the remaining three logic boards, one contains the internal "memory" and its associated control functions (Section 2.5). The second board (Section 2.3) provides timing and the selection matrix required to separate the display and storage functions of the memory board. This board also generates the cursor display and provides low impedance video drive and synch signals to the display unit. The third logic board (Section 2.4) contains the cursor position counter, input data serial parallel conversion and decoding, and other functions such as clear, foreground/background, cursor addressing, etc.

2.2 Input/Output Logic Board

The diamond shaped boxes on the bottom left of Figure 2.2-1 identify signals from the computer. Hex boxes identify the next terminal connector.

The modem used to couple terminal data to the computer requires a Request To Send (RTS) signal on pin 4. This signal is generated by conditions determined by a strap on the I/O board. Condition 1 (Always) causes the Request To Send line to be high at all times. For condition 2 (Poll), the Request To Send line goes high after a correct poll code has been received. For condition 3 (Send), the Request To Send signal goes high immediately after the operator has depressed the SEND key. On receipt of the Request To Send high level, the modem typically puts tones on the telephone line.

Modems are normally set to raise the Clear To Send line upon receipt of a Request To Send level (pin 4, RS232 connector). In order for terminals to send data, their Clear To Send line (pin 5, RS232C connector) must be high. In systems where data may be sent as soon as available, the Clear To Send line must be strapped high. This may be accomplished either by supplying a voltage or by strapping the RS232C pins 4 and 5 together to raise the Clear To Send line automatically when Request To Send goes high.

Data from the computer is received on RS232C pin 3 and is coupled to pin C on the I/O board through the mother board. The signal is converted from RS232 levels to TTL levels by Z23. In addition to utilizing the TTL data internally, the I/O board uses an RS232 driver, Z22, to reamplify and resend the signal to the next terminal. The external data received, now at TTL levels, is sent via pin F to the cursor unit to decode control codes. In addition, the data is coupled into the serial input of a Universal Asynchronous Receiver Transmitter (UART), Z5, on pin 20. Data is clocked into Z5 from a crystal oscillator controlled divider system generating a sequence of baud clocks for all usable baud rates. The output of this clock system appears on pin 10 of Z1 and is coupled directly into pins 17 and 40 of the UART, Z5. When a serial stream of data comprising a single byte has been received, the data information sits on lines labeled RD1 through RD8 as received data bits. The Data Available line, (pin 19)

also goes positive to indicate that the data has been received and is stabilized. The parity bit is ignored (note that RD8 (pin 5) has no connection). The positive Data Available level is coupled through an inverter to the Reset Data Available (pin 18). The negative going transition of the Data Available pulse on pin 19 is utilized for poll code detection and either acceptance or rejection.

The polling code system consists of a two byte sequence, of which the first byte is ENQ (hex 05). The data on the output bus of the UART is coupled to chips Z2 and Z10 where the ENQ is decoded. If ENQ is present, pin 1 of Z8 goes high enabling the flip flop when the Data Enable pulse goes low (the trailing edge of the signal as described above). Since Z8 toggles on receipt of the first ENQ, if two ENQs are received in a row, Z8 will reset. When the first ENQ is received, pin 3 of Z8 goes high enabling Z9. Pin 12 of Z9 is directly connected to the Data Available line. The character following the ENQ code will enable both inputs of Z9, and pin 11 of Z9 will go high enabling gates Z13.

The data on the byte received following ENQ is coupled into comparator Z6. Z6 compares this data with the switch settings on S2 and S3 (the address code) and, if they are the same, puts a positive signal on pin 9 which is also coupled to gates Z13. Z13 will have a low output on either pin 8 or pin 6 depending upon the value of bit 7 in the byte. If bit 6 is a normal poll code, pin 6 of Z13 will go low. In cases where the computer wishes to bypass the operator and select a terminal even though SEND has not been depressed (force poll), the computer merely inverts the value of bit 7, taking pin 8 of Z 13 low instead of pin 6. The fast select (force poll) strap must be connected to pin 8 of Z13 for this to operate.

Z12 is a pulse shaper which is actuated by the inputs on pins 9 and 10. If the SEND key has been depressed, pin 10 will be high. If pin 6 of Z13 goes low at the same time, Z12 will be triggered and will generate a pulse of approximately 500 nanoseconds. This negative output is used to set the poll latch Z24 (pins 8 and 6). If the terminal is strapped to transmit data immediately after it is polled, the strap will set flip flop Z13 (pin 12) and Z17 (pin 8) and enable immediate transmission.

When the poll latch Z24 is set, pin 8 goes high and pin 6 goes low. This causes: (1) the signal to be coupled back to the ENQ decode to prevent further decoding action even if ENQs are received; (2) a Data Enable command to go to the cursor board, enabling display and acceptance of data since a correct poll has been performed; (3) generation of a Request To Send level (if the strap is set) by coupling pin 6 of Z24 pin 12 and Z21 pin 8. Z24 pin 1 and pin 13 represent an OR gate. The Request To Send level can be raised either by the polled flip flop Z24 or by flip flop Z11 which provides a poll response if the SEND key has not been depressed (typically EOT). Every time a correct poll has been received, the output of Z29 pin 7 is used to reset Z11, causing the Q output (pin 5) to go low and raising the Request To Send line. After transmission of the poll response (EOT) character the EOC output (pin 24 of Z5) goes high. This is inverted by Z7 pins 1, 2, 3 and used to set Z11, causing pin 5 to go high and removing the Request To Send input.

If the unit is strapped to transmit after STX (E_C) is received, STX is decoded in the cursor board, brought in through pin R, inverted in Z21 and coupled through Z18 to set the transmit latch Z13/Z17. The transmit latch Z13/Z17 can be reset by: the control C character received via pin S; the end of screen command (512 characters transmitted) on pin K; the control W signal from the computer; or the keyboard's master reset key (pin W). When the transmit latch Z13/Z17 is reset as indicated above, the trailing edge is spiked by Z7 and used to set flip flop Z20. Pin 10 of Z7 may optionally be strapped to ground (shorting C8). In this case, no end of message character is generated since pin 8 of Z7 will not have a signal.

Z20 controls the transmission of the end of message character. When it is set, $\overline{Q}$ (pin 13) goes low. This low command is coupled to Z14 (character select status select) and is used to select the desired character bits. Since the signal on S1 is now low and the signal S0 is still high on Z14 (because the transmit latch is still set), the output of Z14 will be either ETX or CR depending upon the strap on the input of Z19 pin 11. The negative signal at pin 13 of Z20 is also coupled through OR gate Z18 and inverter Z19 to OR gates Z16. Pin 11 of Z16 enables pin 10 of Z16, permitting the UART clocking signal (present on pin 5 of Z8) to clock the Data Strobe and load the characters to be transmitted into the UART register. Another section of Z16 (pin 6) enables the counter to generate the load pulse.

Transmission to the computer is handled by the UART, Z5. Data is strobed into the UART bus (pins 26-33, DB1-DB8) by Data Strobe (pin 23) going low. The UART then converts the parallel data to a serial stream at pin 25 (SO). This is coupled to pin 5 of Z22, converting to RS232 level. When the UART is available to be loaded with the next byte of data, the TBMT line (pin 22) goes high. After the UART transmits the stored data, it internally transfers the next data byte to the transmission section. The TBMT signal is applied to pin 9 of Z15, an AND gate. Pin 11 of Z15 is held high by the Clear To Send command from the modem. When pin 10 goes high, pin 8 is low. The baud clock on pin 10 of Z1 going positive causes a narrow (350 nanosecond pulse) negative pulse to be present on pin 6 of Z7. This is inverted through Z21 and used to clock Z12 (if pin 1 is low). The output of Z12 is a 2 microsecond positive pulse appearing on pin 13. The trailing edge is used to set Z8 and generate the Data Strobe input for the UART. This in turn permits the next character on the data bus to be strobed into the UART (since the buffer memory is now available).

Z16, pins 4, 5, 6, is used as an OR gate with pin 6 going high to enable the Data Strobe. Pin 4 goes low when all three inputs on Z15 go high: pin 13 goes high when the cursor has completed its positioning, is stable, and is located under the next transmittable character; pin 1 is held high whenever the transmit latch is "on" indicating that a transmission can be performed; pin 2 goes high when Z20 is set (pin 9 of Z20 is normally held high during rest periods by the transmit latch Z13/Z17 holding pin 12 low when not transmitting).

When transmission is started by latch Z13/Z17 being set, pin 12 is released and pin 11 controls the "on" time of Z20. After the first load pulse is sent and after the transmit latch is set, the Data Strobe pulse is coupled back to pin 10 of Z20 causing it to reset. When the cursor again stops at a transmittable character, pin 11 goes low causing Z20 to again set. As a result, Z20 toggles "on" when either the cursor has stopped or transmission has started and is reset with each Data Strobe. When "on", it couples into pin 2 of Z15 and enables transmission by strobing data into the UART. The output of Z20 pin 9 is also coupled via Z3 pins 4, 5, 6 to the cursor advance latch Z11. The Data Strobe coupled to pin 6 of Z3 prevents changing the cursor advance latch when a Data Strobe is present since this

could cause an error in the data appearing on the UART data bus. The Data Strobe output on pin 6 of Z8 is also used to reset the poll and end of message latches (2 sections of Z20). Z7 generates a 200 nanosecond negative spike on pin 11 which is inverted and applied to Z10. Z10 is used as an OR gate (master reset and data strobe) but is inhibited from operation if the transmit latch Z13/Z17 is off.

If the send latch is set and the operator hits a key, the bell rings. This is accomplished by bringing the keyboard data line in on pin 6 of the connector to pin 1 of Z18. This is mixed with the send latch data on pin 2 of Z18 to actuate the bell circuit. The bell also rings if the bell command arrives on pin M of the connector or if the operator tries to write on background data (pin Y of the input connector). The output on pin 20 of the connector exists for approximately one half second and is used to turn on the bell.

Selection of response coding data to be transmitted is handled by selector chip Z14 and gates Z9 and Z3. In normal operation, when the transmit latch is on, bit D5 is coupled directly through Z9 pins 8, 9, 10 to DB5 on the UART. Data bit D6 is similarly coupled right into the UART. If the transmit latch is not set and a response is being sent to the computer (such as EOT or ETX), bits 5, 6 and 7 are all zero. Z3 is used to convert lower case code characters generated by the keyboard into upper case. Since lower case has both bits 6 and 7 present, Z3/Z9 supplies bit 6 directly into the bit 6 input of the UART while inhibiting bit 7. The inverse also occurs, D6 low causes D7 to be high when input bit 6 is low. Z14 selects either data bits 1, 2, 3 and 4 or the appropriate preset bits corresponding to the end of message character or the poll response.

2.3 Timing and Control Board

The timing and control logic board schematic is shown in Figure 2.3-1. Starting with a crystal oscillator, this basic clock is used to control the intensity at each spot along each horizontal line. The clock drives a horizontal counter consisting of Z12, Z17 and Z18. The four bit outputs of Z12 are decoded by Z13 to provide timing during the character display time. One output, properly timed, is shaped into a narrow pulse and used as the display strobe. This strobe pulse is supplied to the memory board and transfers the information stored in the memory into a shift register that generates the actual video information. The remaining counters provide the 32 character position addresses to both the memory and the cursor coincidence network. Z27, Z28 and Z29 are digital comparators, which compare the cursor position counter with the display counter. When coincident (defining the position of the cursor on the screen) flip-flop Z15 is set to provide the cursor underline bar. This flip-flop is reset at the end of the character by Pin 7 of Z13.

At the end of each horizontal displayed line, the clock signal to the line counter is stopped and the clock applied to a retrace counter consisting of Z4 and Z7. During this count, the video on the screen is blanked and, at an appropriate count, a horizontal synchronization signal is sent to the television set. When the retrace count is completed, the clock is again applied to the line counter and the next line generated.

At the end of each horizontal line, a signal is applied to the vertical position counters Z19 and Z21. Z19 determines the T.V. line being displayed and Z21 selects the character being displayed. As in the case of the horizontal counters, when the screen display is complete, the input signal is transferred from the line counter to the vertical retrace counter. Again, as in the case of the horizontal, a vertical synchronization signal is taken from the vertical retrace counter Z5 and Z6.

The video signal, which had been strobed into the shift register on the memory board, is clocked out by the basic crystal clock to the video gating chain. The video is blanked when a character is being written on memory and during the retrace portions of the video display. In order to improve character appearance, each character is transmitted as a series of dots

2.3 Timing and Control Board (Continued)

at the basic clock frequency. This is accomplished by gating the clock into the video output path. When a character is to be displayed in background mode, a memory board signal sets flip-flop Z16, which shunts the output video, reducing its amplitude and providing a lower intensity signal. The ratio of intensity (background to foreground) is a function of the cathode ray tube characteristic, the amplifier, characteristics, the settings of the brightness and contrast controls, and adjustable resistor R4 which has been selected to provide an appropriate ratio. If its value is reduced, the background intensity will also be reduced compared to the foreground intensity. The output of the video chain utilizes a low impedance emitter-follower drive.

The timing board also provides addresses for the random access memories used on the memory board. Gates Z22 through Z26 select either the display counter or cursor counter address for application to the random access memories. The cursor address is selected when input data has been received and must be written in the memory at the then cursor location. At all other times, the display counter address is used to request the next character to be displayed from the memory.

2.4 Cursor Control Board

The cursor control and input decoder logic board, Figure 2.4-1, contains several separate functions. On a selected terminal, input data is received at TTL levels via Z26 from the RS232 connector to Pin 5 of Z26. Before SEND is depressed, this gate is disabled and the data appearing on Pin 2 of Z26 (looped around from the keyboard) is carried to the input path. Data appearing on Pin 10 of Z26 is directly coupled to the serial input of shift register Z26. No action occurs while the input line is "marking". When the "start" signal appears on the data line, Pin 3 of Z28 is taken low, enabling Z8 to count the incoming baud rate clock on its Pin 14. If the "start" signal is present for eight full clock pulse times, a signal appears on the counter output, Pin 11 of Z8. This loads the "start" signal into the shift register and, at the same time, sets data latch Z11. This output is applied to Pin 2 of Z8, enabling the counter to continue running after the "start" pulse disappears and data is present on the data line. Every 16 clock pulses into Z8 generates a shift command to the registers, Z6 and Z4, loading the serial stream data into the registers with the data value at the time midpoint of the signal. Input noise on the data lines does not persist for a sufficiently long time to set the data latch to clock data into the shift registers.

When the start pulse reaches the end of the shift registers (all data is now stored in the registers) it resets the data latch to prevent further clocking, blanks the screen (since data will be written in a different place in the memory) and starts the generation of the basic time signals required to load the data into the memory. The timing chain consists of three pulse delay circuits in series (Z14, Z14B and Z19). The output of the first delay network activates the control decoders, Z2 and Z9, if the data in the shift registers represents a control code (i.e., no six or seven bit is present). If the signal is not a control code, the delayed pulse is used to transfer the memory address from the display counters to the cursor counters. In this case, an additional delay circuit (Z17) provides the load memory command after the new address has had time to stabilize. When the initial pulse ends (after approximately 2 microseconds) the second pulse delay generates a strobe to step the cursor counter.

2.4 Cursor Control Board (Continued)

A wide variety of control codes can be strapped into the cursor board to perform any particular function. The schematic shows a typical set for illustrative purposes. If the control code, "Cursor XY Position" shown as Qc on the schematic, is received from the computer, the cursor counter inputs are inhibited by Z20 under control of the X-Y latch Z7/Z10 and the X-Y sequencer Z3. If this command has been received, the next data word sets the data latch and steps Z3 to gate the first five bits of the data word into the cursor character position counter, Z27 and Z23, by activating the preset line (Pin 11) from Z5. The next data word received steps Z3 to its next data word received steps Z3 to its next position and loads the first four bits of the data into the cursor line counter, Z28. After this sequence is complete, the final pulse delay network, Z19, is used to preset the shift registers, Z6 and Z4, to the condition corresponding to a "marking" data line and to reset the X-Y position latch.

A number of special operations are selected by input computer data. When "Backspace" (hexadecimal 88, Hc) is received, it is decoded by Z2 and Z9. These generate a negative pulse on Pin 9 of Z2, which is used to step cursor character counter (Z27 and Z23) backwards. When "Carriage Return" (Mc) is received, it generates a negative pulse on Pin 15 of Z2. This is applied to Z15 and inverted to clear the cursor character counter, Z27 and Z23.

If the ASCII Delete character (Hex FE) is received, it is inhibited by Z1 and ignored. When the "Home Cursor" command, shown as Rc on the schematic, is received, it generates a negative pulse at Pin 3 of Z9 and, through gates Z15 and Z16, resets both cursor character and line counters, Z27, Z23 and Z28. The "Ring Bell" command (Gc) causes a signal to appear on Pin 8 of Z2. This is transmitted to the I/O logic board, where a wide pulse is generated to ring the bell for approximately one-half second. The computer command "Set Foreground" shown as Oc on the schematic, is used to set flip-flop Z7/Z10 by generating a signal at Pin 17 of Z2. When this has been set each character received will also cause a foreground bit to be written in the foreground/background memory. The flip-flop may be set to the background mode by receipt of the "Set

Background" code, shown as Yc on the schematic, which is decoded on Pin 10 of Z9. In this mode, characters are displayed with lighter (background) intensity than normal characters.

When a "Clear Screen" command, shown as Lcs on the schematic, is received, all characters are removed from the screen (by writing spaces into each memory location) and the cursor is returned to its home position at the upper left hand corner of the display. Since the ASCII character for space consists only of bit six, the clear function actually involves placing a six bit in each memory location and removing any other bits present. This means that the cursor counters must step through every character, and the space code must be loaded into the memory at the character position.

When the "Clear Screen" command is received, an output pulse appears on Pin 14 of Z9 and is used to set the clear flip-flop Z15/Z16. The flip-flop output is used to reset the X-Y position latch, the foreground/background latch, and the input data registers. It also forces a bit 6 on the data line (via Z11) even though the shift register itself does not have this bit present.

In order to minimize the time required to clear the screen, the cursor counters are reset to "0" and then stepped through the entire 512 character positions in just over one millisecond, writing a space code into each position. The counters are cleared by a differentiated pulse derived from the leading edge of the clear flip-flop output. The differentiated pulse is applied to Pin 2 of Z15 and Pin 13 of Z16, whose outputs drives the reset lines on the cursor counters. In order to step the cursor counters rapidly and write spaces in every memory position, the clear flip-flop output is used to enable gate Z17, Pin 1, allowing the display strobe, generated on the timing board, to load the memory rapidly. The clear flip-flop also transfers the write address source from the display counters to the cursor counters.

2.4 Cursor Control Board (Continued)

When the cursor counters have completed their count at the 512th position, Z28 overflows, and its carry pulse is used to reset the clear flip-flop. The resetting of this flip-flop causes the generation of a termination pulse, which presets the data input shift registers, Z6 and Z4, to correspond to input data "marking". This same pulse is applied to the memory board load cycle circuit to prevent loading any other data.

When a "Clear Foreground" character, shown as Xc on the schematic, is received from the computer, any foreground characters on the screen are removed and the cursor returned home. This character is decoded and generates a negative pulse on Pin 9 of Z9 to set the clear flip-flop, as described above, and also set the clear foreground flip-flop, Z23. When this flip-flop is set, it controls a gate on the memory board, Z17, to prevent writing space characters in memory locations where a background bit has previously been stored. All other steps of the clear function occur as described above.

2.5 Memory Board

The internal memory used to store data and refresh the CRT display is contained on the memory board, Figure 2.5-1. Since each memory chip contains 256 bits, and the display has 512 characters, two chips are required for each of the six data bits comprising the ASCII code. The need to remember foreground/background information for each character requires an additional bit. As a result, there are seven pairs of memory chips, one for each bit and one pair for foreground/background. Because of timing requirements, alternate characters on a line use different chips. Character counter bit "0" is used to select the group of seven chips which is to be active for a particular character. The memory chips are addressed continually, either by the display counters or by the cursor counter (when data is to be written on the memory). The resulting six data bits are applied in parallel to the character generator, Z16, which provides the intensity bit information for the particular character line to the shift register, Z15. After the address and data has stabilized, a display strobe generated on the timing logic board is used to transfer the data to the shift register. As each subsequent clock pulse is received, the appropriate video information appears on the output of the shift register and is used to drive the display tube.

The static memory chips require clocking in the correct sequence in order to store data. Z19, a shift register, is wired to preload the sequence when strobed. The signal on connector Pin 10 is used to preset data into Z19. The output of Z19 clocked by the four MHZ clock, provides the necessary timing sequence.

If the SEND button has not been depressed, writing on background characters is inhibited so that the operator may not write over protected fields. This is accomplished by Z21 preventing the write cycle from being applied to the memories unless its Pin 2 is low. This occurs if any input on Z18 is held low -- by the presence of a foreground bit in memory on Pin 11, or Z17 Pin 8 bing low. This can only occur if Pin 9 and Pin 10 are high. This corresponds to the SEND latch being

in the SEND position and the CLEAR FOREGROUND latch on the cursor board not being set. This gating prevents the operator from writing over background fields until the SEND button is depressed, at which time the operator has lost control and the computer can write on the background fields.

The operator may tab to the next foreground field by depressing a key. This key causes the generation of a negative pulse which is applied to connector Pin 20 and set flip-flop Z17/Z22. One output of the flip-flop connects to Pin 17 and is used to enable high-speed stepping of the cursor control counters.

When the operator depresses the tab key, the cursor will go to the next foreground field following a background field. Tab flip-flop Z17/Z22 is set (Z17-6 goes high) when the operator sends the tab command. The output of flip-flop Z17/Z18 (Pin 3) is applied to Pin 13 of Z18 to prevent resetting of the tab flip-flop if foreground characters are in position over the cursor when the tab is depressed. The next background character that comes up is applied to Pin 2 of Z22 and used to reset Z17/Z18. The first foreground field following this is applied to Pin 2 of Z18, resetting the tab flip-flop Z17/Z22.

This board also contains voltage dropping diodes and a zener regulated supply for the RAM memories.