UNIVERSAL PROM PROGRAMMER REFERENCE MANUAL

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Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051

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CHAPTER 1

INTRODUCTION

The Universal PROM Programmer (UPP) is a peripheral device, designed to simplify the programming of Intel's family of electrically programmable read only memories (PROMs). Because it is a "peripheral" device, the PROM Programmer must be interfaced to a "control computer", such as one of Intel's INTELLEC microcomputer development systems. The control computer transfers commands, memory addresses, control information and data to the PROM Programmer, enabling it to program a particular PROM or to read the contents of a previously programmed PROM. The PROM Programmer also includes provisions that allow the control computer to read the internal status of the PROM Programmer peripheral.

On the front panel of the Universal PROM Programmer are mounted two zero-insertion-force sockets; one 16-pin, the other 24-pin (UPP-101). As an option two 24-pin sockets can be mounted instead (UPP-102). Each socket is driven by a printed circuit board within the PROM Programmer that contains the electronic circuits required to program a particular class of PROMs. These printed circuit boards with the device-related circuitry are referred to as "personality cards". The Universal PROM Programmer can contain two different types of personality cards at any given time (one associated with each socket) The personality cards are easily exchanged to allow users to reconfigure their UPP, as required to program the PROM devices. There are several different personality cards and adaptors that are used for programming the various PROM devices listed in Table 1-1.

The Universal PROM Programmer comes in a 17"x6"x7" cabinet that houses all of the peripheral's printed circuit boards, as well as the power supply.

Table 1-1

Personality Card Selection[1]

PROM	PERSONALITY CARD	ADAPTER	NO. OF PINS	NO. OF PINS	ORGANIZATION	ACCESS TIME
1602A 1702A	UPP-872 (Chapter 7)	-	24	2048	256 x 8	1.0 µs
2704 2708	UPP-878 (Chapter 4)	-	24	4096 8192	512 x 8 1024 x 8	500 ns
2716 2758 2758 S-1865	UPP-816 (Chapter 10)	- UPP-555[2] UPP-555	24	16,384 8192 8192	2048 x 8 1024 x 8 1024 x 8	450 ns
3601 M3601	UPP-361 (Chapter 6)	-	16	1024	256 x 4	70 ns 90 ns
3602 3602A	UPP-865 (Chapter 12)	UPP-562	16	2048	512 x 4	70 ns
3604 3604A		-	24	4096	512 x 8	70 ns
3604L-6 3604 AL		UPP-555	24	4096	512 x 8	90 ns
3605		UPP-565	18	4096	1024 x 4	70 ns
3608		UPP-555	24	8192	1024 x 8	80 ns
3621		UPP-562	16	1024	256 x 4	70 ns
3622 3622A		UPP-562	16	2048	512 x 4	70 ns
3624 3624A		-	24	4096	512 x 8	70 ns
3625 3628	UPP-865 (Chapter 12)	UPP-565 UPP-555	18 24	4096 8192	1024 x 4 1024 x 8	70 ns 80 ns
8748	UPP-848 (Chapter 8)	supplied	40	8192	1024 x 8	not applicable
8755	UPP-855 (Chapter 9)	supplied	40	16,384	2048 x 8	400 ns
8755A	UPP-955 (Chapter 9)	supplied				

NOTES:

1. Preliminary Notice: This is not a final specification and is subject to change.
2. optional

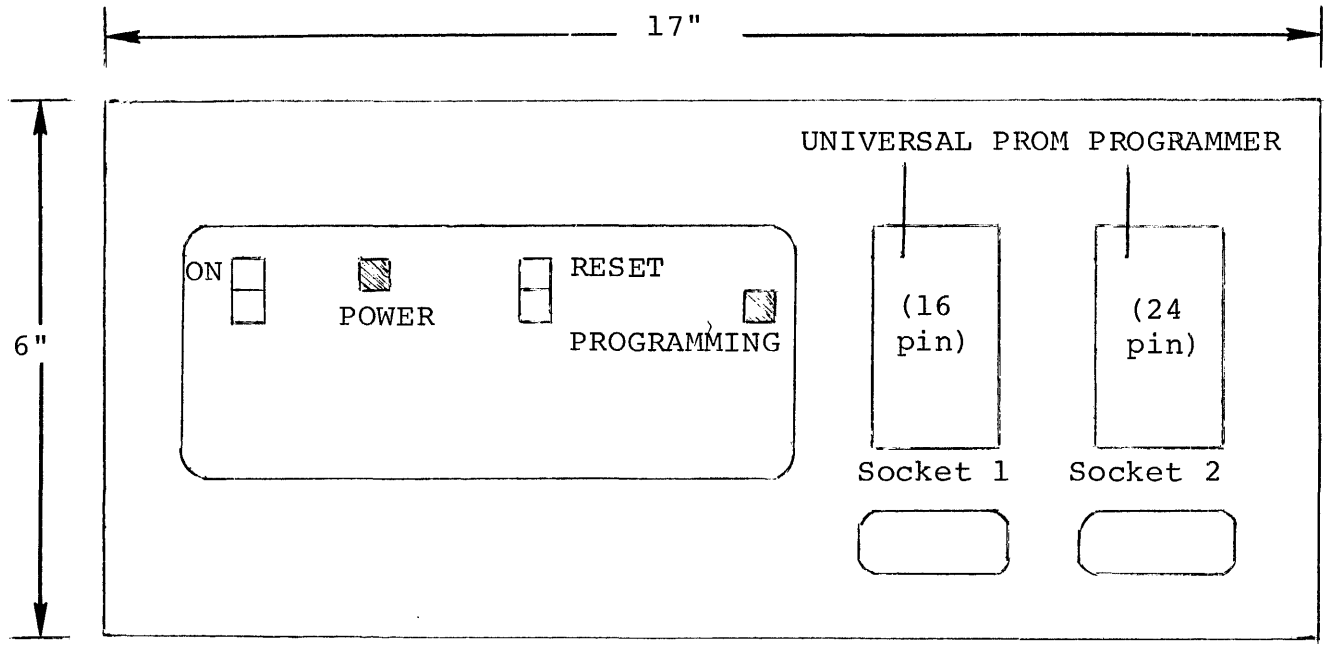
1.1 SYSTEM OVERVIEW

The Universal PROM Programmer consists of a Front Panel, a Control Board, two personality card slots and the power supply, as shown in Figure 1-1.

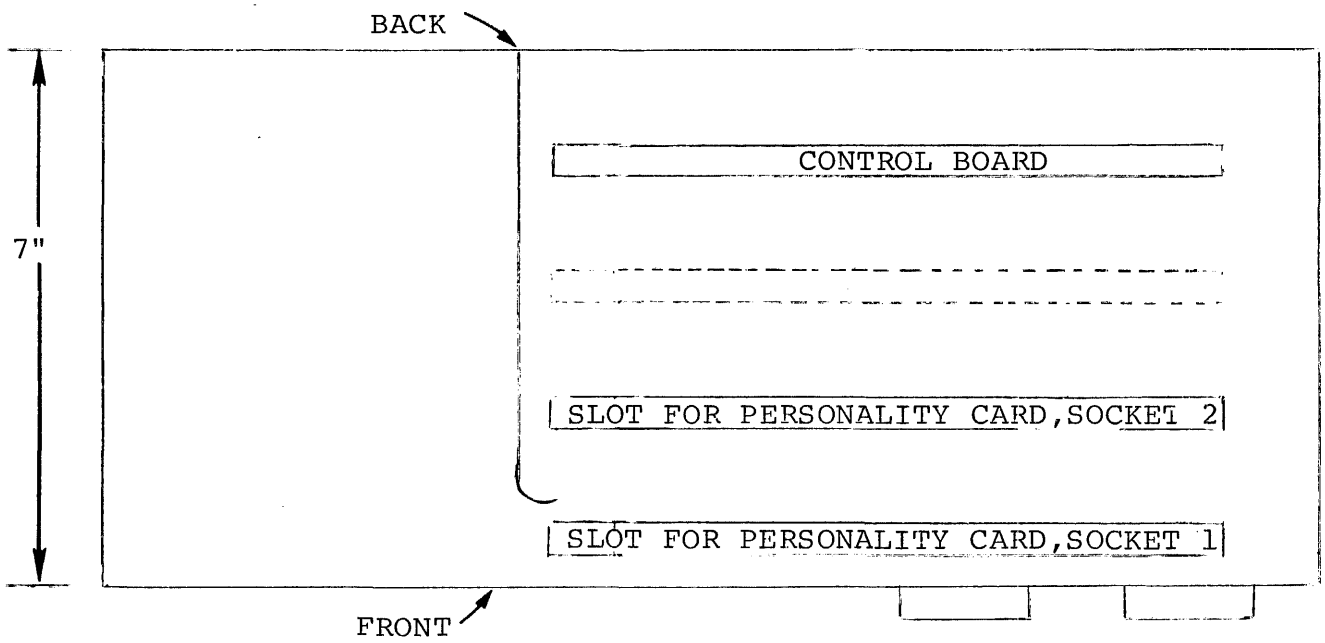
The Front Panel includes a POWER ON switch and indicator (5VDC power), a RESET switch which will initialize the peripheral when pressed (The RESET function should be used only if the control computer can't communicate with the U.P.P. because the 4040 did not initialize correctly. RESET should not be used when the control computer is reading or programming a PROM.), a PROGRAMMING indicator that lights when a PROM is being programmed, and two zero-insertion-force sockets. Each socket is connected to one of the two personality card slots in the card rack. There are two socket configurations available. One configuration provides a 16-pin socket on the left (socket #1) and a 24-pin socket on the right (socket #2)(UPP-101); the other configuration provides two 24-pin sockets (UPP-102).

> --WARNING--
>
> Caution must be taken to insert the PROM in the front panel socket correctly (pin 1 in the upper left side). Damage to the PROM and/or personality card is possible if a program attempt is made when the PROM is inserted upside down.

Each personality card contains ROM memory (that stores the program/read routines), as well as all of the electronics (e.g., voltage regulators and level shifters), required to program a particular class of PROMs. There are two slots in the peripheral for personality cards, one associated with each Front Panel socket. The different types of personality cards (see Table 1-1) can be easily exchanged to reconfigure the peripheral's programming capability. A complete list of PROMs programmed by a personality card is found in the chapter describing that card.



FRONT VIEW (UPP-101)



TOP VIEW

FIGURE 1-1

PROM PROGRAMMER: FRONT PANEL AND CABINET

--CAUTION--

When inserting a personality card, make sure that the power is off and that the card is placed in the card slot associated with the socket that will hold the PROM being programmed.

The Control Board, as its name implies, is the controlling module within the PROM Programmer. The Control Board accepts commands from the control computer, and, in turn, directs the appropriate personality card to perform the specified operation. The Control Board can cause a personality card to read or program a particular PROM location. The Control Board also maintains a status word that can be read by the control computer. In addition to supervising the execution of commands, the Control Board is responsible for receiving and storing the 12-bit PROM address, the 8-bit write data byte and four control bits from the control computer. The PROM address and write data are, in turn, passed onto the personality cards. During read operations, the Control Board accepts the read data byte from the personality card and transfers it to the control computer. Figure 1-2 illustrates the primary data paths between the control computer, the Control Board and the personality cards.

The power supply transforms standard 115/230 VAC power into the following DC levels for use by the Universal PROM Programmer:

+5.85 VDC, regulated (VCCH)
-10 VDC, regulated
+40 VDC, unregulated
-40 VDC, unregulated
+70 VDC, unregulated

(protected by 1 Amp fuses)

NOTE: Do not use slow blow type fuses.

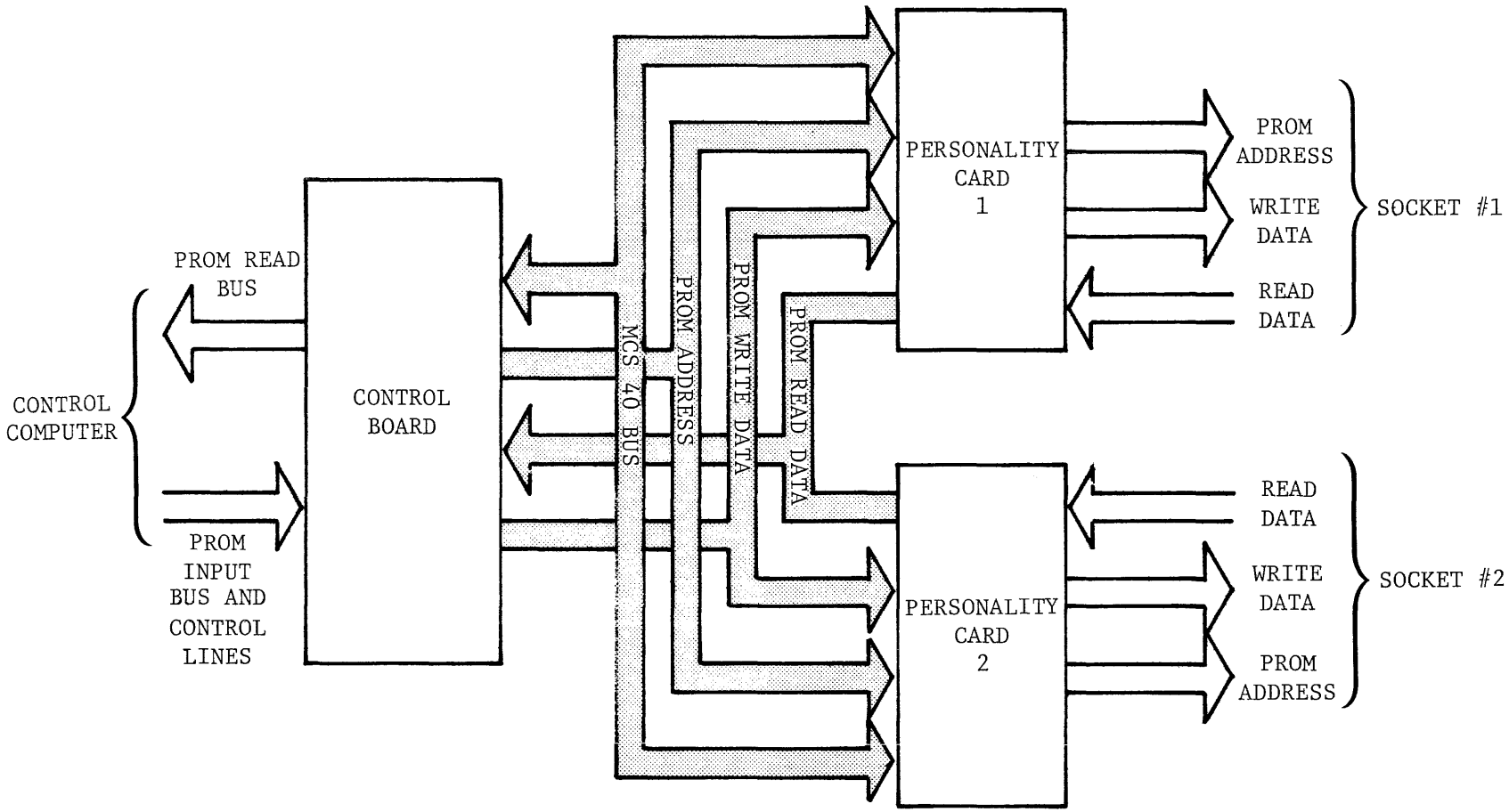


FIGURE 1-2

PROM PROGRAMMER: DATA FLOW

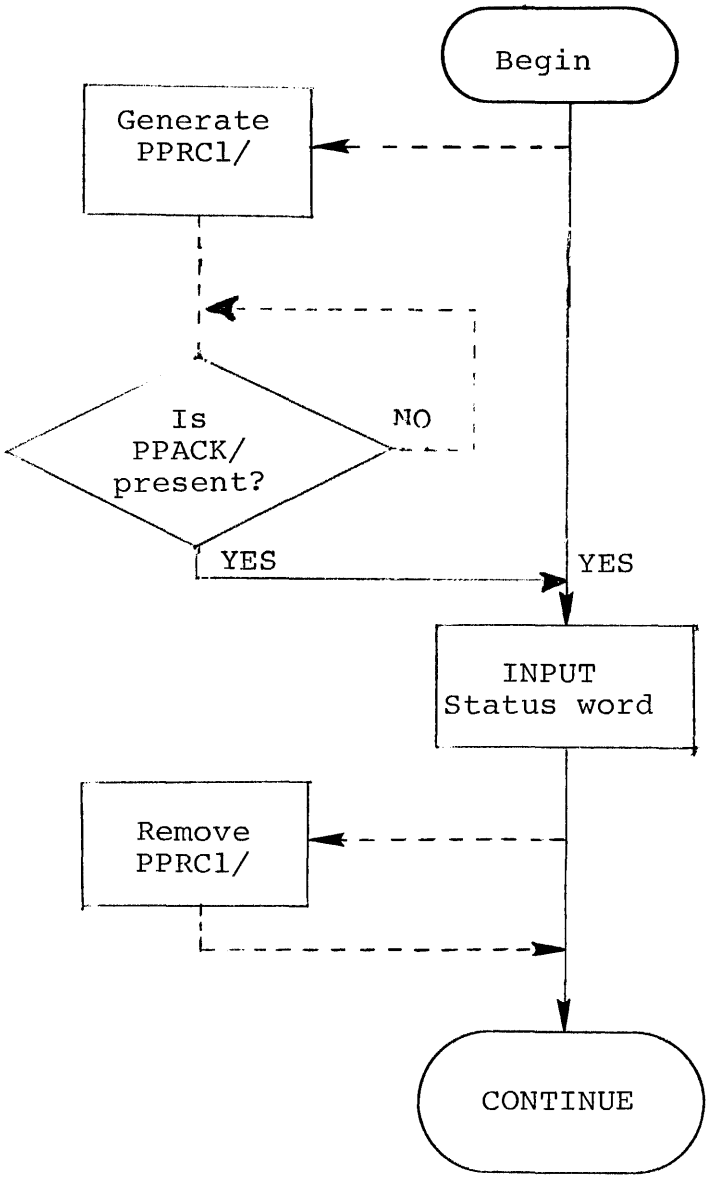
NOTE: In the remaining chapters of this manual we will be describing the circuitry on the Control Board and the various personality cards. Both active-high (positive true) and active-low (negative true) signals appear on these PCB's. The following convention should eliminate any confusion when reading subsequent chapters or when referring to the schematics in Appendix B: whenever a signal is active-low, its mnemonic is followed by a slash; for example, RESET/ means that the level on that line will be low when the peripheral is being cleared. When the slash is omitted from the signal mnemonic, it specifies that the signal is active-high; that is, the level on the RESET line will be high when the peripheral is being cleared.

1.2 CONTROL COMPUTER SOFTWARE REQUIREMENT

All operations that are performed by the Universal PROM Programmer are initiated by commands from the control computer. The control computer should:

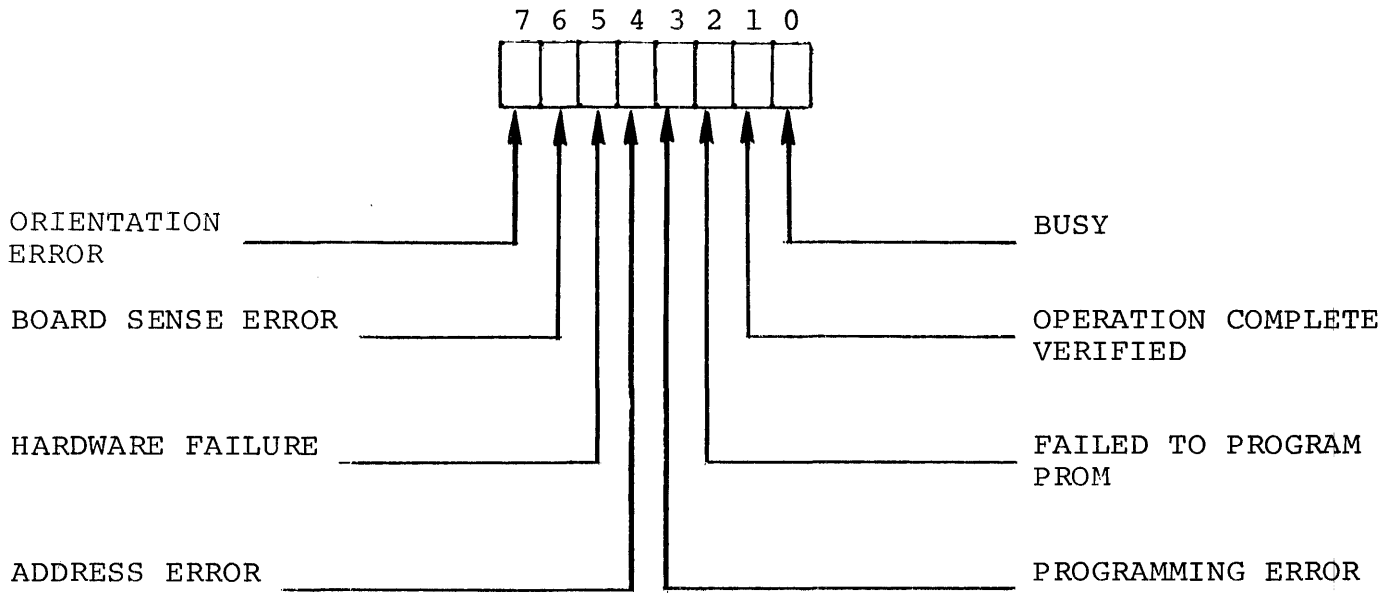
- Read the internal status of the PROM Programmer
- Cause the PROM Programmer to read data at a particular PROM location
- Cause the PROM Programmer to program data into a particular PROM location

The control computer would normally read the PROM Programmer's 8-bit status word to determine if it is busy, before beginning a read or program sequence (see Figure 1-3). If bit 0 of the status word is true, the peripheral is busy. The status word is always available on the PROM read bus, except during read data cycles. If the control computer does not require that its read status cycles be acknowledged, it can merely examine the contents of the PROM read bus. If the control computer does require a read acknowledge (as does the INTELLEC®MDS system), the control computer should send a read status pulse (PPRC1/) to the peripheral. PPRC1/ will cause the PROM Programmer to generate an acknowledge signal (PPACK/) and return it to the control computer. Bit definitions for the status word are shown in Figure 1-4.



Note: Dotted line indicates action required by control computer systems other than the INTELLEC® MDS which automatically generates the necessary strobes.

Figure 1-3. Read Status (Flow chart)



Where:

BIT 0 = BUSY indicates that a program data operation is in progress.

BIT 1 = OPERATION COMPLETE/VERIFIED indicates that a data read or program operation has been successfully completed.

BIT 2 = FAILED TO PROGRAM PROM indicates that the PROM Programmer was unable to successfully program the PROM.

BIT 3 = PROGRAMMING ERROR indicates that a program data word called for a fused bit position to be reprogrammed which is impossible on Bipolar PROMs.

BIT 4 = ADDRESS ERROR indicates that the PROM address was out of bounds.

BIT 5 = HARDWARE FAILURE (e.g., the high voltage from the power supply was not present, or the PROM programmed incorrectly).

BIT 6 = BOARD SENSE ERROR indicates that a personality card was not present when the Control Board tried to access it.

BIT 7 = Orientation error indicates that the PROM is in upside down.

NOTE: All bits are mutually exclusive. Bits 1-7 are invalid, unless bit Ø, BUSY, is false.

FIGURE 1-4

STATUS WORD

Having determined that the PROM Programmer is not busy, the control computer can then begin passing the PROM Programmer the parameters it will require to perform a data read or program operation. The control computer must output an 8-bit control/high address nibble and an 8-bit low address byte as shown in Figure 1-5.

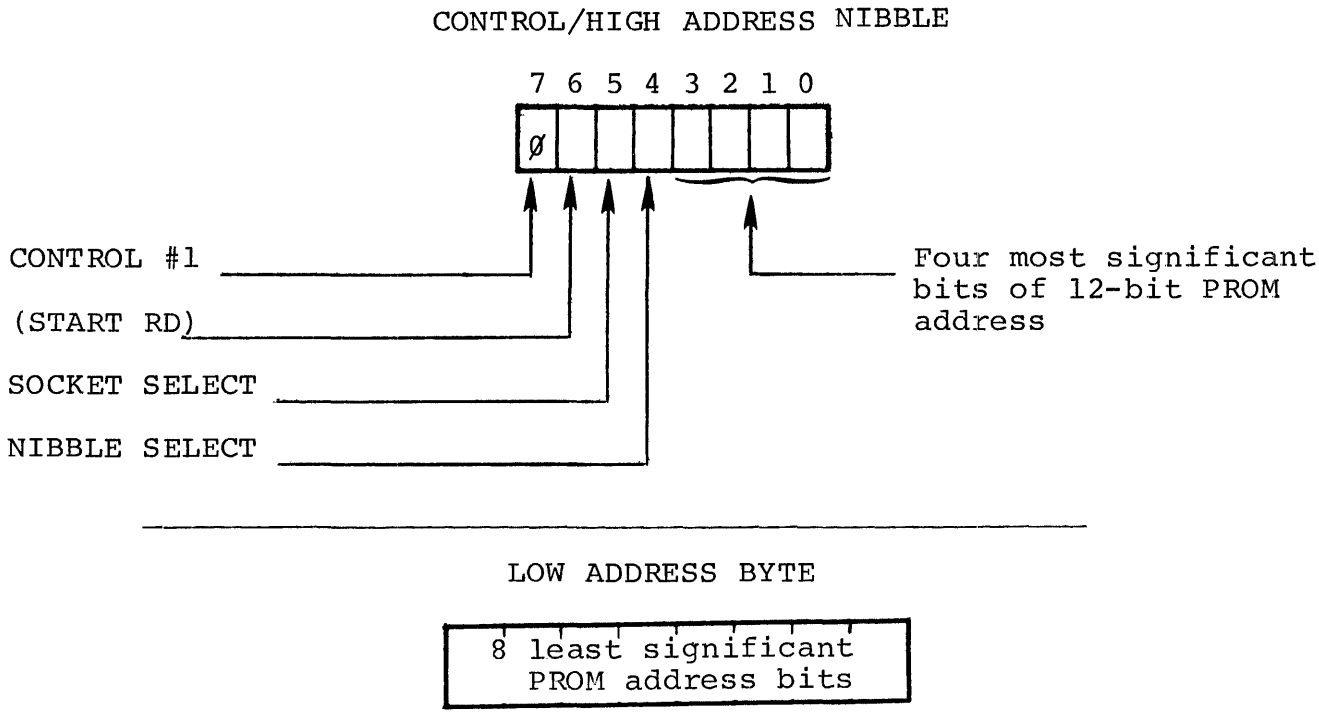


FIGURE 1-5
CONTROL AND ADDRESS PARAMETERS

The control computer must output the control/high address byte with the PPWC1/ strobe. The most significant bit is an undefined control bit (CONTROL #1); it must be false (logical 0). (START RD) will, if set (logical 1), initiate a read data operation. SOCKET SELECT (bit 5) identifies one of the two sockets on the Front Panel (if SOCKET SELECT = logical 1, socket #1 is selected; if SOCKET SELECT = logical 0, socket #2 is selected). When programming a PROM that is organized into 4-bit words, NIBBLE SELECT (bit 4) specifies whether the upper or lower four bits of the 8-bit write data byte are to be used (if NIBBLE SELECT = logical 1, the most significant 4 bits of the write data byte are programmed into the addressed PROM location; if NIBBLE SELECT = logical 0, the least significant 4 bits are used). When programming an

8-bit word, NIBBLE SELECT is ignored.

The control computer must output the low address byte with the PPWC2/ strobe. The contents of the low address byte, together with the four least significant bits (0-3) of the control/high address nibble, form the 12-bit PROM address that uniquely identifies the particular location to be accessed within the selected PROM.

After the control/high address and low address parameter bytes have been output to the PROM Programmer, the control computer can initiate the actual data read or program operation.

DATA PROGRAM OPERATION:
A data program operation is initiated when the control computer outputs an eight-bit write data word with the program strobe signal (PPWC0/). The write data word is the data that will be written into the addressed location within the selected PROM. As we mentioned above, the NIBBLE SELECT control bit can select either half of the write data byte when programming a PROM with 4-bit words (e.g., the 3601 PROM). The PPWC0/ strobe latches the write data byte and sets the WRITE PROM-BUSY/ command latch in the PROM Programmer. Because WRITE PROM is latched, it is not necessary for the control computer to maintain PPWC0/ throughout the data program cycle. The PROGRAMMING indicator on the Front Panel is lit while the data is being written into the addressed PROM location. After the PROM location is successfully programmed or when an error is detected, the internal status word is updated and the WRITE PROM-BUSY/ latch is reset.

To determine when a data program cycle has been completed, the control computer should periodically read the status word from the Universal PROM Programmer, checking for <u>not</u> busy. When the status word does indicate not busy, the control computer should read the status word again to determine if an error occurred or if the operation was completed successfully.

Figure 1-6 provides a flow chart for the data program operation.

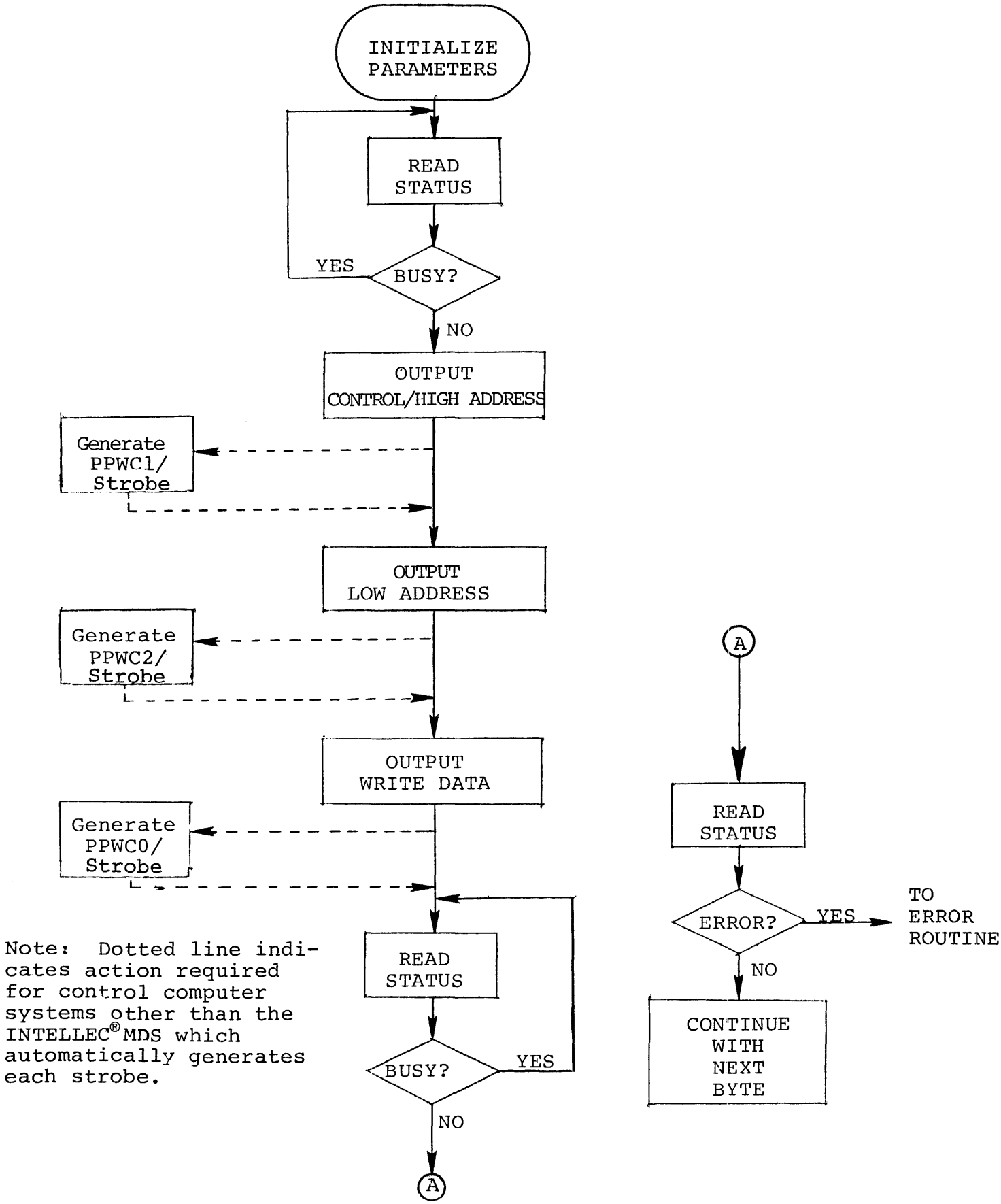


Figure 1-6. Programming One Byte (Flow chart)

DATA READ OPERATIONS:

There are two methods for reading data from the Universal PROM Programmer.

A data read operation can be initiated when the control computer sends the read data command (PPRC0/) to the PROM Programmer. The PROM Programmer will read the contents of the PROM location specified by the 12-bit PROM address (previously output by the control computer), and return the data to the control computer, with a read acknowledge signal, PPACK/. PPACK/ informs the control computer that valid data is on the input bus. It is the responsibility of the control computer to remove its PPRC0/ signal when it receives PPACK/. After removing PPRC0/, the control computer must read the status word from the Universal PROM Programmer to determine whether the data is valid, or invalid due to an address out of bounds error or a board sense error. Refer to Figure 1-7.

The other method for reading data which avoids the acknowledge delay mentioned above is a status check approach. The control computer outputs (with PPWC1/) the control/high address byte to the Universal PROM Programmer with bit 6 (START RD) true. The control computer then reads the status word, waiting for busy (bit Ø) to go false. When busy does go false, the control computer should input the data byte by issuing the read data command (PPRC0/). The data and the read acknowledge (PPACK/) will be returned in less than 1 μsec. Then the control computer should read the status word again to determine if the read data is valid. The control computer need not be occupied for an extended period of time when reading data with this method. Refer to Figure 1-8.

NOTE: When reading a 4-bit PROM, the 4-bit data is in lower four bits of the 8-bit word sent to the control computer.

In Appendix A we have summarized the PROM Programmer commands which have been coded in the INTELLEC®MDS Monitor program and which are available to users when the Universal PROM Programmer is being controlled by an INTELLEC®MDS system.

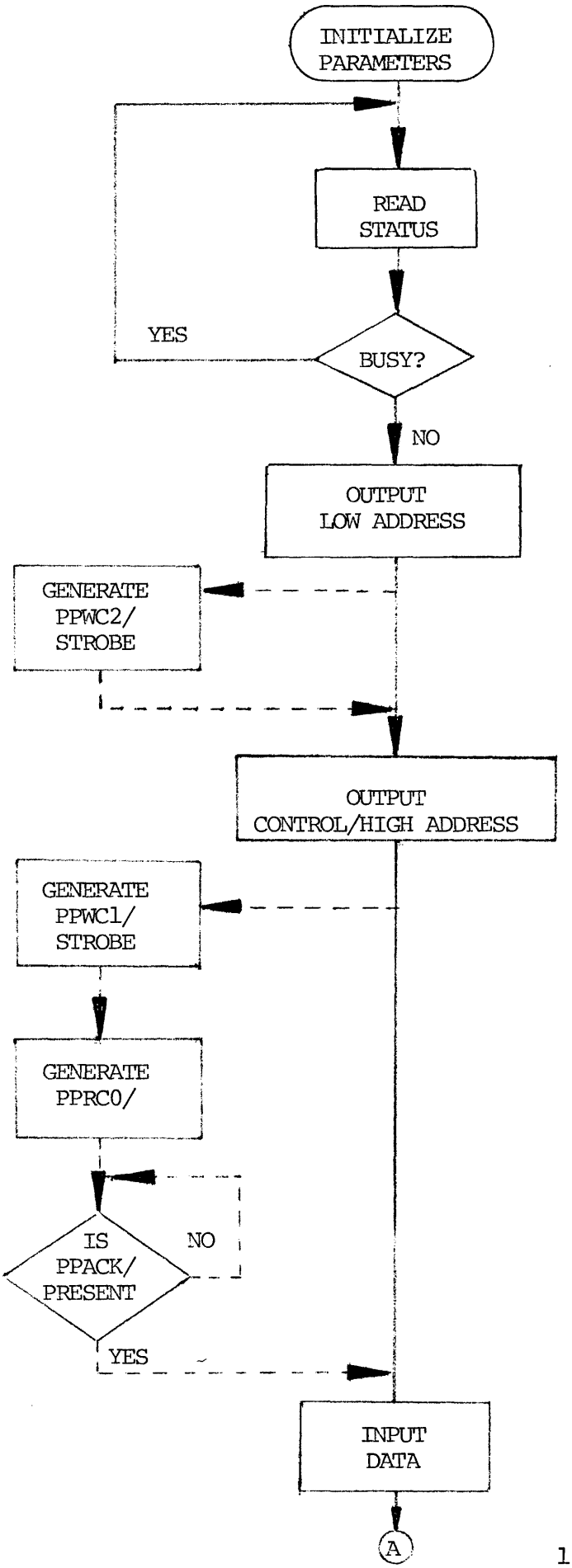
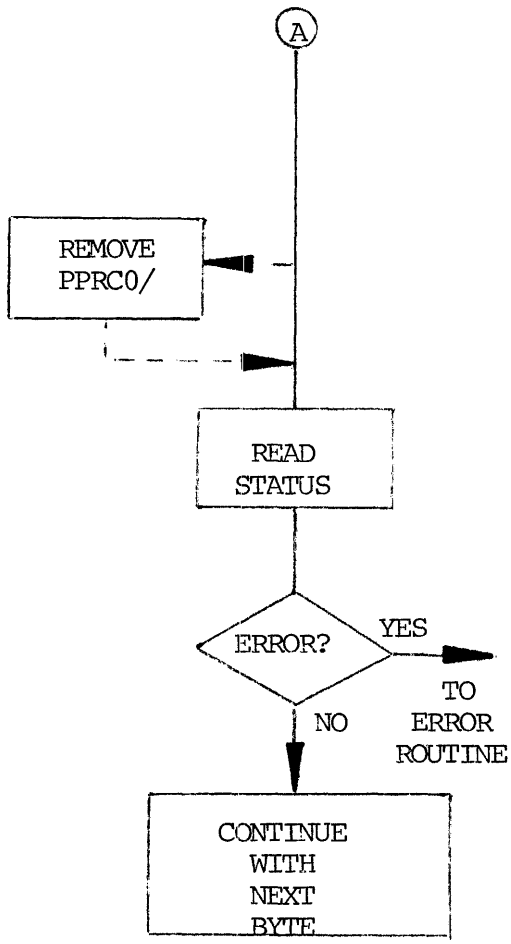
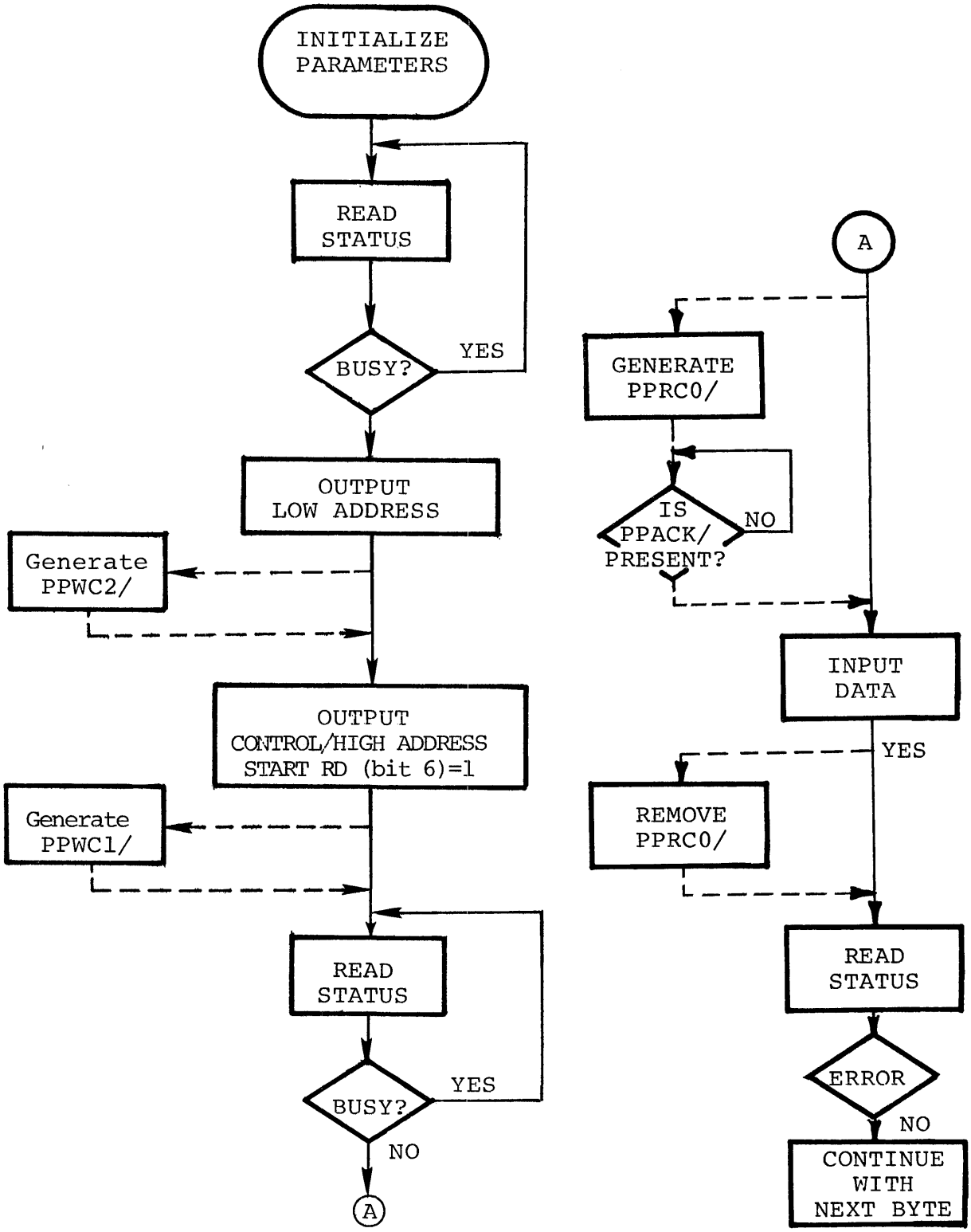


Figure 1-7. Read Data - Method 1 (Flow Chart)

Note: Dotted line indicates action required by control computer systems other than the INTELLEC®MDS which automatically generates the necessary strobes.





Note: Dotted line indicates action required by control computer systems other than the INTELLEC® MDS which automatically generates the necessary strobes.

Figure 1-8. Read Data-Method 2 (Flow chart)

CHAPTER 2
THE CONTROL BOARD

The Control Board coordinates all operations performed by the Universal PROM Programmer. The Control Board receives commands from the control computer, and, in turn, directs the appropriate personality card in the performance of the particular operation specified by the control computer's command. The Control Board can cause a personality card to read a particular location in a PROM, or the Control Board can cause a personality card to program a particular location in PROM. The Control Board also maintains a status word that can be read by the control computer.

In addition to supervising the execution of commands from the control computer, the Control Board is responsible for receiving and storing:

- the 12-bit address that identifies the PROM location to be accessed during read or program operations,
- the 8-bit data word that is to be written into the addressed PROM location during program operations, and
- the four control bits that specify the socket and nibble to be used during read or program operations.

Section 2.1 identifies the various functional blocks within the Control Board. The next section, 2.2, explains how these functional blocks interact to execute each of the PROM Programmer operations. The final section in this chapter provides a pin list for the Control Board.

2.1 FUNCTIONAL DESCRIPTION: CONTROL BOARD

For descriptive purposes, the Control Board can be viewed as consisting of ten functional blocks:

1) MCS™-40 chip set
2) Reset logic
3) Clock generator
4) Mode control register (4 bits)
5) High address register (4 bits)
6) Low address register (8 bits)
7) PROM write data register (8 bits)
8) Status decoder
9) PROM read logic
10) Comparator

as shown in Figure 2-1.

At the heart of the Control Board is the Intel® 4040 microprocessor. Instructions for the microprocessor are stored in ROM chips (Intel® 4001). Three chips are located on the Control Board with the 4040 itself; they contain instructions for operations which are independent of the characteristics of a particular PROM. Two additional ROM chips are located on each personality card; they contain instructions which are dependent on the characteristics of the PROM for which the personality card is designed. There is also one chip of RAM (Intel® 4002) for the microprocessor; it is located on the Control Board. The 4001 ROM chips each provide four input or output lines, while the 4002 RAM chip provides four output lines that allow the 4040 microprocessor to communicate with circuitry outside of the MCS™-40 chip set. The 4040 communicates with the 4002 RAM and 4001 ROM chips via the MCS™-40 bus that consists of:

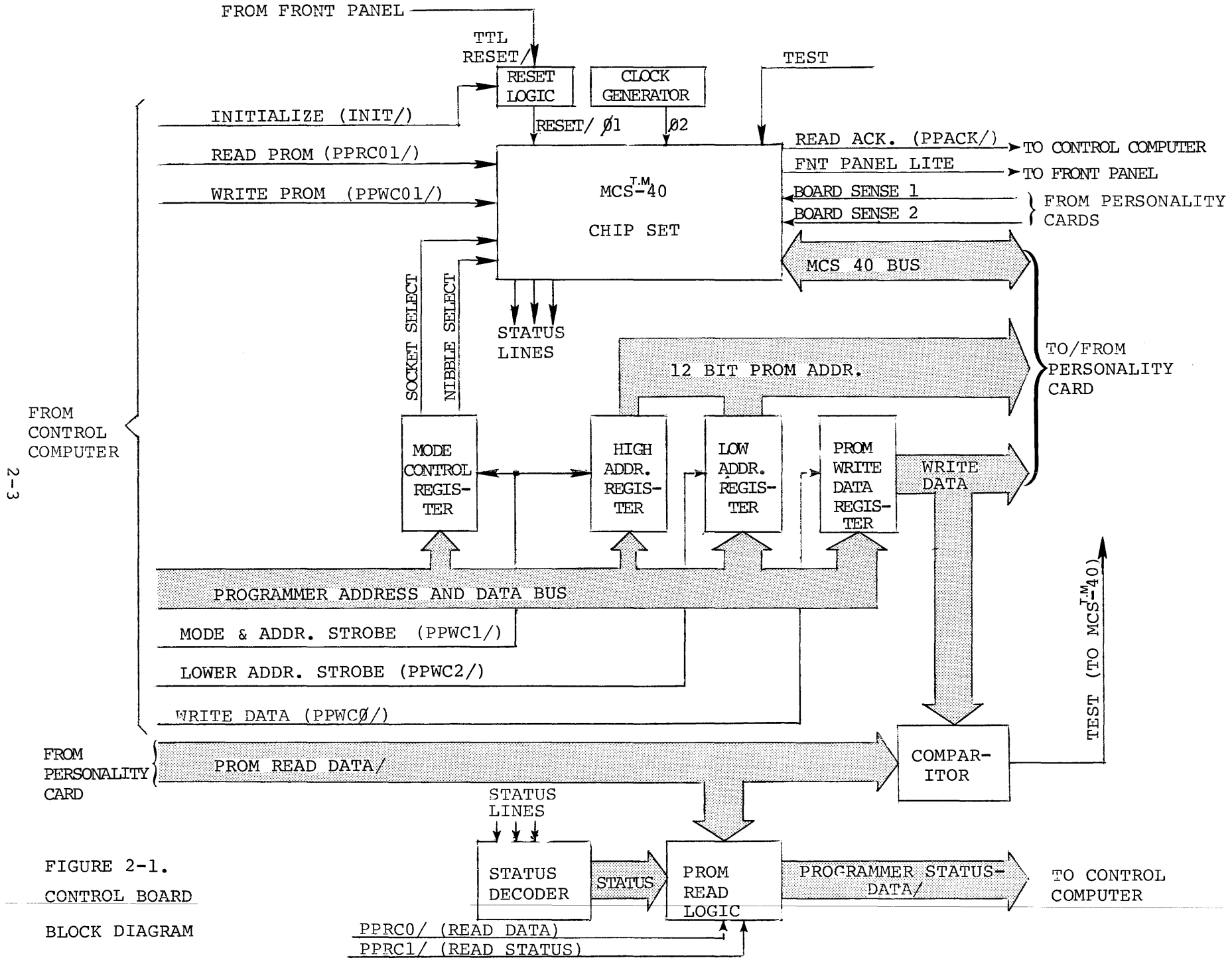


FIGURE 2-1.
CONTROL BOARD
BLOCK DIAGRAM

- 4 data lines (D0-D3),
- a SYNC line,
- the two clock signals (Ø1 and Ø2), and
- four memory control lines (CM-ROM0, CM-ROM1, CM-RAM0, and CM-RAM1).

In the following paragraphs, we will use the term "MCS™-40" to refer to the chip set that includes the 4040 microprocessor the 4001 ROM's and the 4002 RAM.

There are two circuit blocks included on the Control Board that are necessary for the operation of the MCS™-40, the reset logic and the clock generator.

The reset logic supplies a reset signal (RESET/) to the MCS™-40. When this signal is true (active low) all of the MCS™-40's internal registers are cleared and the program counter is set to location zero. The effect of this is that the PROM Programmer will be properly initialized to accept a command from the control computer. The reset signal will be supplied whenever one of the following occurs:

1) the power switch on the front panel is switched from OFF to ON,
2) the reset switch on the front panel is pressed,
3) the initialize line (INT/) is pulsed by the control computer.

The clock generator supplies the two clock inputs, Ø1 and Ø2, that provide a timing reference for the MCS™-40. The clock generator is driven by a 5.185 MHz crystal oscillator. Timing for Ø1 and Ø2 is illustrated in Figure 2-2.

The mode control register stores the four control bits that are output by the control computer with the four high order PROM address bits:

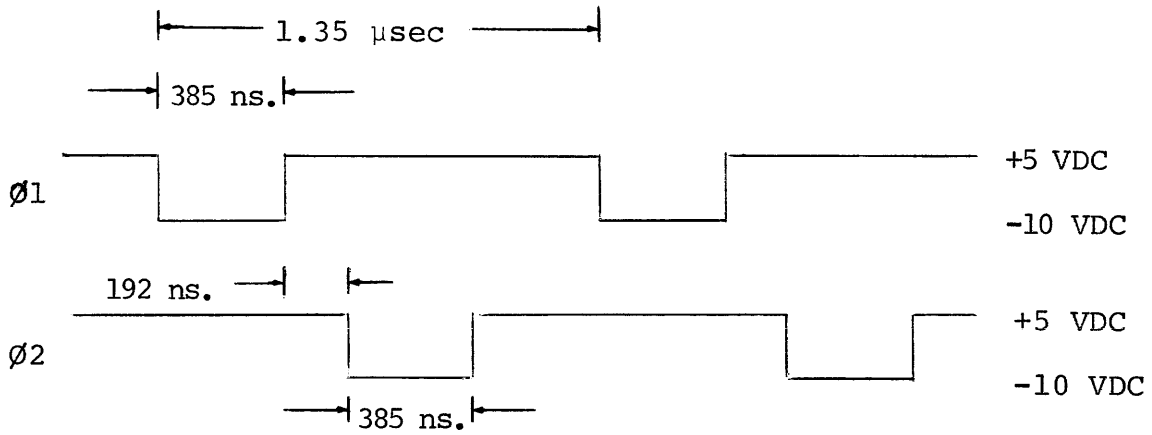
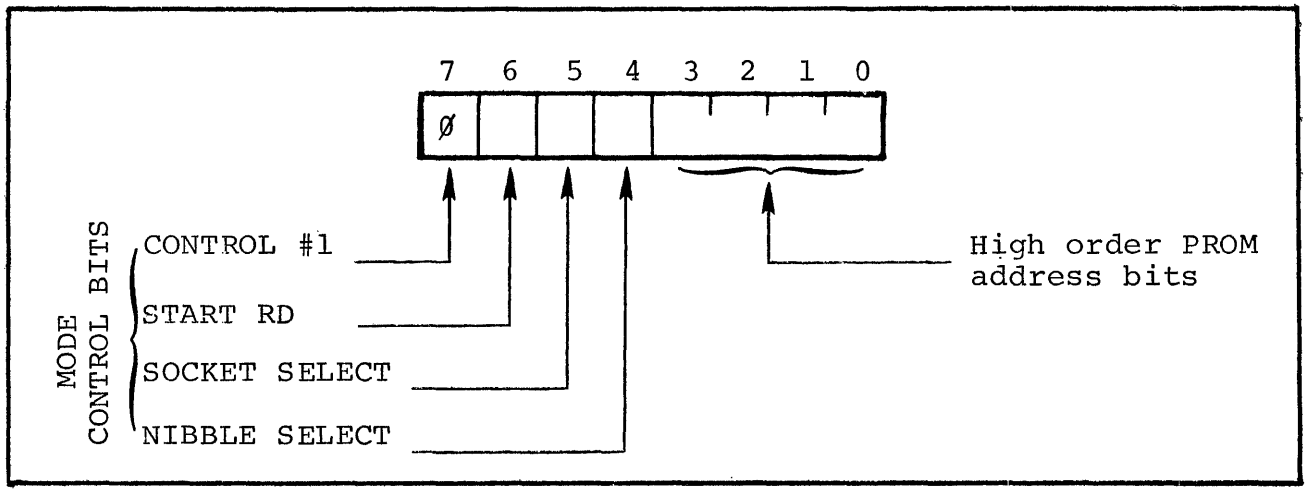


FIGURE 2-2. Ø1 and Ø2 TIMING



CONTROL/HIGH ADDRESS BYTE, OUTPUT BY CONTROL COMPUTER

The most significant mode control bit, CONTROL #1, is not used on the Control Board but must be false (logical Ø) because it is latched and made available at the board's edge connector. Bit 6 (START RD) will, when set (logical 1), initiate a read data operation in the Universal PROM Programmer. The other two mode control bits, SOCKET SELECT and NIBBLE SELECT, are latched then made available to the MCS™-40 through input port 0, bits 0 and 1 of the 4001 ROM at A20. SOCKET SELECT specifies which of the two sockets on the front panel is to be read or programmed. NIBBLE SELECT specifies which nibble is to be programmed when programming a 4-bit device. NIBBLE SELECT is ignored when programming or reading PROMs that are organized into 8-bit words.

The control computer generates the PPWC1/ strobe when the Control/ High Address nibble is on the data lines (PPD0/-PPD7). PPWC1/ latches the four control bits into the mode control register, and, at the same time, latches the four address bits into the high address register. The contents of the high address register constitute the four most significant bits of the 12-bit PROM address, and are made available to the personality cards via lines, PROM ADDRESS 8 through PROM ADDRESS 11.

The low address register stores the eight low order PROM address bits that are output (via lines PPD0/-PPD7/) by the control computer along with the PPWC2/ strobe. PPWC2/ latches the address bits into the low address register. The address bits are made available to the personality cards via lines, PROM ADDRESS 0 through PROM ADDRESS 7. The twelve PROM ADDRESS bits uniquely identify the PROM location to be accessed (bit 0 is the least significant bit).

When the control computer issues a program command, it places the data to be written into the PROM on data lines, PPD0/-PPD7/, and issues the PPWC0/ strobe. PPWC0/ latches the data byte into the PROM write data register, and starts the program data operation. The contents of this register are made available to the personality cards via lines WRITE DATA 0 through WRITE DATA 7 (bit 0 is the least significant bit).

The Control Board provides a status word that can be read by the control computer. The MCS™-40 maintains this status word by periodically updating the contents of the three status lines (STATUS 0, STATUS 1 and STATUS 2) through an output port on the 4002 RAM chip (All). These three status lines specify one of eight possible conditions. STATUS 0, STATUS 1 and STATUS 2 are applied to the status decoder which activates one of eight outputs. The eight outputs of the status decoder constitute the PROM Programmer status word.

The status word is fed to the PROM read logic. The PROM read logic enables the status word onto the PROM read bus (PRD0/-PRD7/) at all times, except during PROM read data operations. When the control computer issues the read status command, PPRC1/, the PROM read logic merely acknowledges the command by generating PPACK/; the status word is already available on the bus.

When the control computer issues a PROM read data command, PPRC0/, the PROM read logic disables the status word and gates the data word read from the PROM (via the appropriate personality card) onto the PROM read bus lines. After the MCS™-40 determines that the

data word has been read and placed on the bus, it causes the PROM read logic to acknowledge the command by generating PPACK/. When the control computer removes its read data command (i.e., when PPRC0/ goes false), the status word is again enabled through the read status logic.

The comparator provides a means of comparing the 8-bit PROM write data from the control computer and the PROM data read from a personality card. The TEST line from the comparator is applied directly to the 4040 microprocessor, indicating the outcome of the comparison.

2.2 THEORY OF OPERATION: CONTROL BOARD

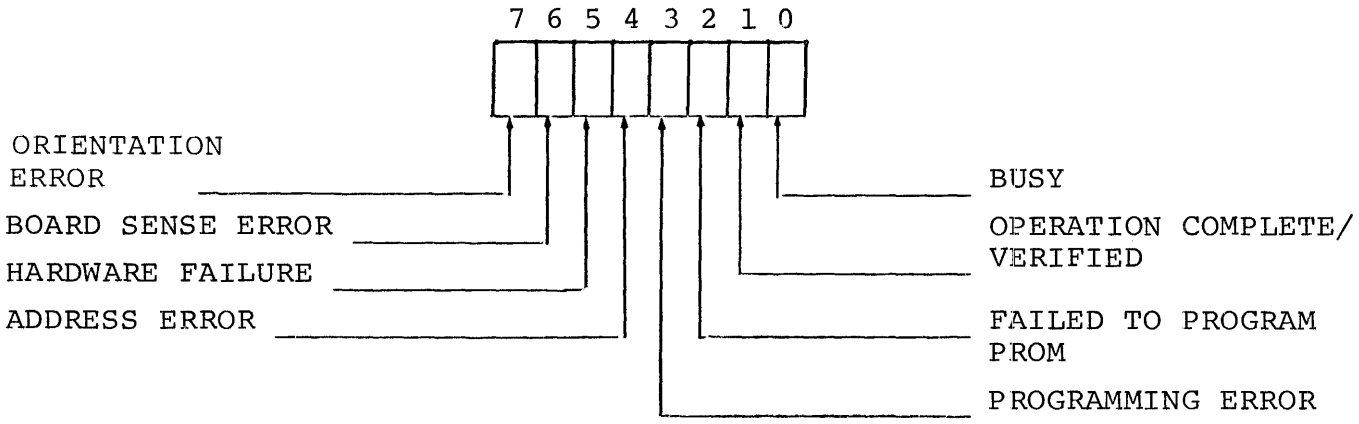
In this section we will describe how the functional blocks on the Control Board interact to execute each of the possible operations. We will begin by describing the read status operation, because it is the operation that would normally be executed first, to determine whether or not the PROM Programmer was busy. We will then discuss the sequences in which the control computer outputs control and address information. This would usually be done immediately prior to actually executing a PROM read data or PROM program data operation. Finally, we will describe the read data and program data operations.

2.2.1 READ STATUS SEQUENCES

As we mentioned in Section 2.1, the MCS™-40 maintains an eight-bit status word by updating three status lines (STATUS 0-STATUS 2) whenever internal status changes. These three status lines are output from three bits on the 4002 RAM (A11) Port, and applied to the status decoder logic which activates one of its eight outputs as determined by the levels on the three status lines. The eight-bit status word is gated through the PROM read logic and driven over the PROM read bus (pins 62-69) by eight 7406 open-collector inverting driver circuits.

The control computer can read the status word by issuing the read status command, PPRC1/ (pin 71). PPRC1/ directly enables the acknowledge signal PPACK/ (pin 72) which can be used to strobe the status word into the control computer and/or reset the read status command.

The PROM status word is illustrated in Figure 2-3. Read status timing is shown in Figure 2-4.



NOTE: Bits 1-7 in the status word are only valid if bit 0 is false (i.e., if the PROM Programmer is not busy). All of the status bits are mutually exclusive (i.e., only one can be true at any given time).

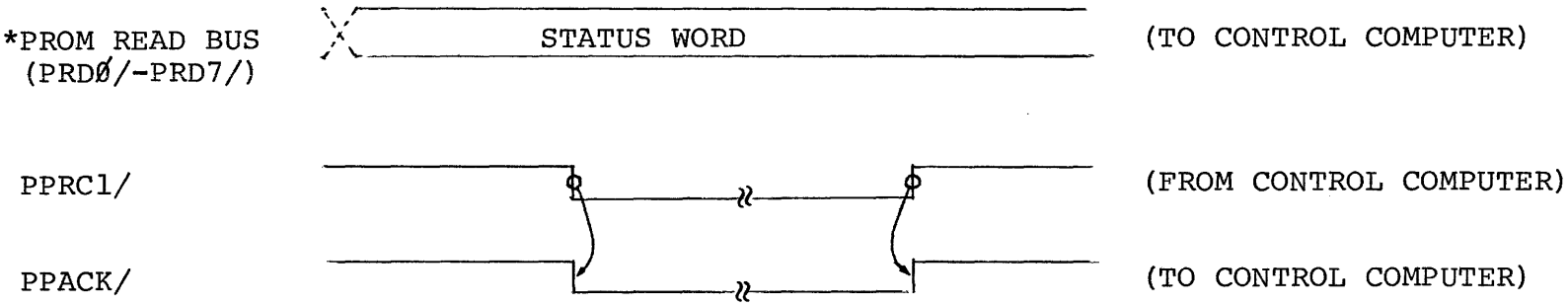
FIGURE 2-3

PROM PROGRAMMER STATUS WORD

2.2.2 CONTROL/ADDRESS OUTPUT SEQUENCES

Before actually beginning a read data or program data operation, the control computer must provide the PROM Programmer with certain control information, as well as a 12-bit address that specifies the PROM location to be accessed. This information is output in two sequences.

The first byte consists of four control bits and the four most significant bits of the 12-bit address. As we mentioned earlier, the control bit portion includes one bit (CONTROL #1) which is buffered and passed to the Control Board's edge connector. The control bit is reserved for future use and must be maintained in a Ø state. The START RD bit can be used to initiate a read data operation. Another control bit, SOCKET SELECT, specifies which of the two sockets on the front panel are to be accessed (SOCKET SELECT - logical 1 for socket #1 and SOCKET SELECT - logical 0 for socket #2). The other control bit is referred to as NIBBLE SELECT. Because some PROM's are organized in 4-bit words (e.g., 3601), there must be a means of specifying which 4 bits of the 8-bit write data byte are to be written into the PROM during program sequences. When NIBBLE SELECT = logical 1



*The status word is on the PROM read bus at all times except during the execution of PROM read data commands (see Section 2.2.3).

FIGURE 2-4. READ STATUS TIMING

the four most significant bits of the write data register are used; when NIBBLE SELECT = logical 0, the least significant bits are used. When 4-bit PROM words are read, the 4 bits are duplicated on bits 0-3 and 4-7 at the PROM read bus. NIBBLE SELECT is ignored when programming or reading PROMs organized into 8-bit words.

The control/high address strobe, PPWC1/ (received at pin 75) latches the four control bits into the mode control register and the four address bits into the high address register.

The other byte that must be output by the control computer prior to a read or program data operation is the low order address byte. This byte is strobed into the eight-bit low address register by the low address signal, PPWC2/ (pin 76). These bits constitute the eight least significant bits of the 12-bit PROM address. All twelve address lines (PROM ADDRESS 0-11) are made available to the personality cards (via pins 29-40).

2.2.3 PROM READ DATA SEQUENCE

There are two methods of reading data from the PROM Programmer. The first method is when the control computer can initiate a PROM data operation by issuing the read data command, PPRC0/ (received at pin 70). PPRC0/ disables the read logic gates that had allowed the PROM status word onto the PROM read bus, and enables the PROM RD DATA lines from the personality cards (pins 52-59) through the read logic and onto the PROM read bus (PRD0/-PRD7).

PPRC0/ is inverted and applied to input port 0, bit 2 of the 4001 ROM at A20, under the mnemonic, RD PROM. When not busy, the MCS-40 stays in a program loop that alternately examines the RD PROM and WRITE PROM input ports on the 4001 ROM. If the MCS-40 finds a true level on RD PROM, it will then examine the SOCKET SELECT input at port 0, bit 1 on the same 4001 ROM. Having determined which socket,

and consequently which PROM and personality card, are to be accessed, the MCS™-40 then examines the board sense input for the personality card associated with the selected socket, BD SENSE #1 (input port 1, bit 2 on the 4001 ROM at A29) or BD SENSE #2 (input port 1, bit 0 on the 4001 ROM at A29). If the appropriate board is not present, an error condition is indicated in the status word, an acknowledge (PPACK/) is generated and the operation is terminated.

Having determined the socket to be accessed, the MCS™-40 transfers program control to the proper read routine stored in the 4001 ROM's on the appropriate personality card. Using the I/O ports on the personality card ROM's, the MCS™-40 can, by executing the read routine stored in these ROM's, cause the personality card to read the addressed PROM location (refer to Chapters 3-6), and send the data to the Control Board on the PROM RD DATA 0-7 lines (pins 52-59). Recall that these lines are enabled through the PROM read logic and out onto the PROM read bus, PRD0/-PRD7/ (pins 62-69).

When the addressed PROM location has been successfully read and the data is on the PROM read bus, the MCS™-40 sets the COMPLETE/VERIFIED bit in the status word and issues the PROM PROG RD ACK signal from the output port, bit 3, on the 4002 RAM (A11). PROM PROG RD ACK, in turn, generates PPACK/ which is made available to the control computer via pin 72. PPACK/ indicates that data is on the PROM read bus (PRD0/-PRD7/). The control computer can strobe the data in with PPACK/. The control computer must reset the PPRC0/ command <u>after</u> it has accepted the data from the PROM read bus. When PPRC0/ goes false, PPACK/ also goes false. The eight-bit PROM status word is again enabled through the PROM read logic and out onto the PROM read bus. The control computer should read the status word to verify that the data is valid and that no error occurred.

Figure 2-5 illustrates PROM read data timing for this method.

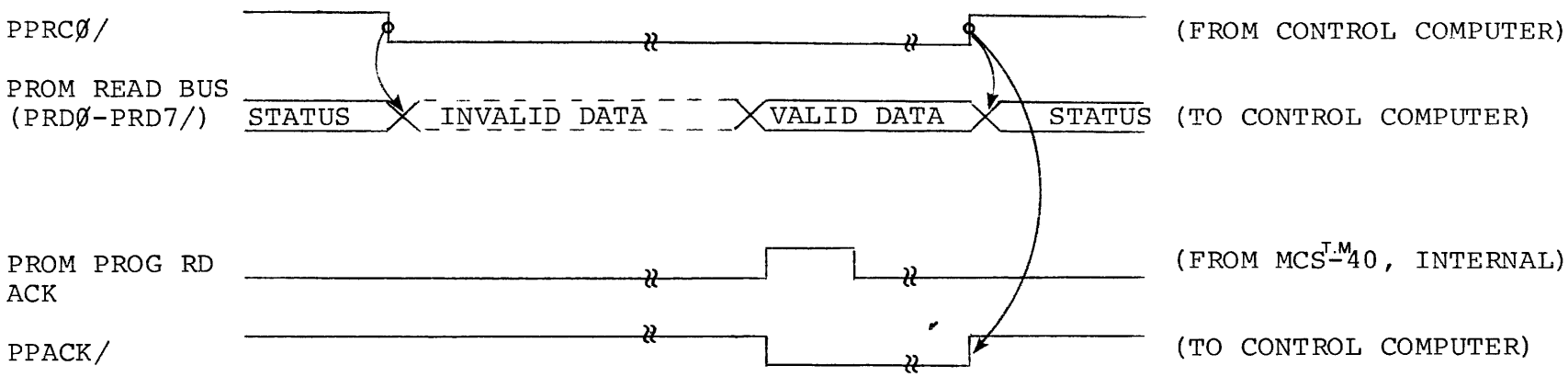


FIGURE 2-5

PROM READ DATA TIMING

The other method for reading is a status check approach. The control computer outputs a Control/high address byte with bit 6 (START RD) set (logical 1). The accompanying strobe (PPWC1/), in conjunction with the START RD bit, sets BUSY (bit 0) in the status register and generates the READ PROM signal which is applied to input port 0, bit 2 of the 4001 ROM at A20. The MCS-40 will interrogate the input port and cause the appropriate personality card to read the addressed PROM location and make it available to the Control Board, as described above for the first method.

When the data is read (or an error occurs), the MCS-40™ outputs PROM PROG RD ACK from the output port, bit 3, on the 4002 RAM at A11. PROM PROG RD ACK, in turn, clears the READ PROM Signal to the MCS-40™ and the BUSY bit in the status word. When the control computer reads the status word and determines that BUSY is false, the control computer should then issue the PROM read data command (PPRC0/). PPRC0/ will cause the read acknowledge signal (PPACK/) to be generated with 1 μsec. PPRC0/ also enables the data byte through the PROM read logic and onto the PROM read bus, PRD0/-PRD7/ (pins 62-69). The control computer should read the status word again to verify that valid data is available and that no errors occurred. This method of reading data from the Universal PROM Programmer prevents the control computer from being occupied for an extended period of time.

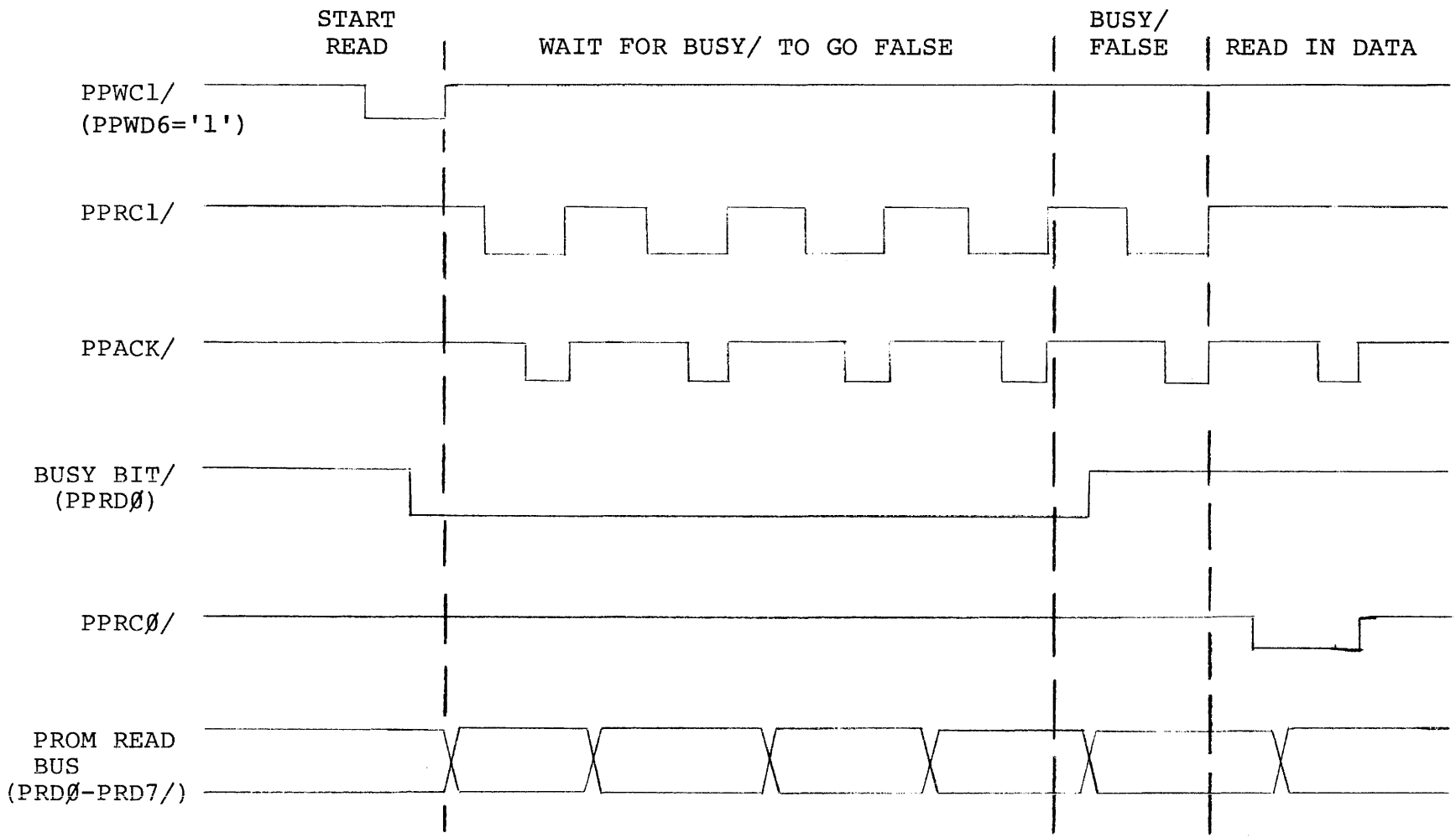


FIGURE 2-6

USING START RD BIT OF CONTROL BYTE

2.2.4 PROM PROGRAM DATA SEQUENCE

The control computer initiates a PROM program data operation by outputting eight-bits of write data to the PROM Programmer, and by issuing the program data strobe, PPWCO/ (received at pin 74).

The eight write data bits are received on lines PPD0/-PPD7/ (pins 77-84), and latched into the write data register by PPWCO/. The contents of the write data register are available to the personality cards on lines WRITE DATA 0-7 (pins 21-28). If the particular PROM to be programmed is organized into 4-bit words, the NIBBLE SELECT bit of the mode control register (see Section 2.2.2) will dictate which 4-bits of the 8-bit write data byte are actually to be written into the addressed PROM location.

PPWCO/ also sets the busy latch (A6-10) in the status logic. The low $\overline{Q}$ output of this latch (BUSY/) is gated through the PROM read logic onto line PRD0/, and constitutes bit 0 of the PROM status word. Thus, the busy status is indicated immediately instead of waiting to be software set by the MCS™-40. The high Q output of the busy latch is labeled WRITE PROM, and is applied to input port 0, bit 3, on the 4001 ROM at A20.

As we mentioned in the previous section, the MCS™-40 stays in a program loop that alternately examines the RD PROM and WRITE PROM inputs on the 4001 ROM. If the MCS™-40 finds a true level on WRITE PROM, it will then examine the SOCKET SELECT input at port 1 on the same 4001 ROM. Having determined which socket, and consequently which PROM and personality card, are to be accessed, the MCS™-40 then examines the board sense input for the personality card associated with the selected socket, BD SENSE #2 (input port 1, bit 0, on the 4001 ROM at A29). If the appropriate board is not present, an error condition is indicated in the status word and the operation is terminated.

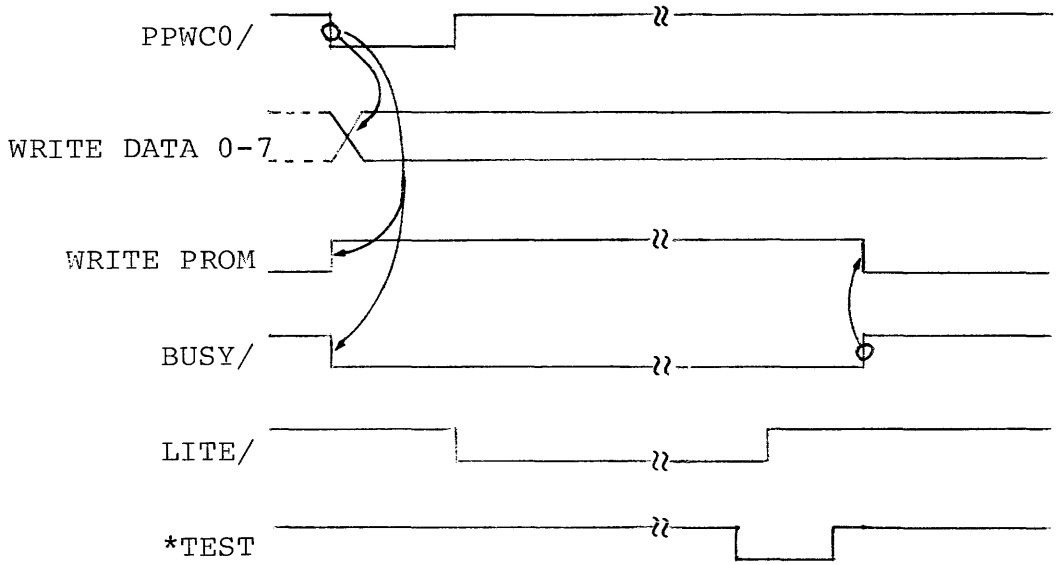
If the PROM to be programmed is organized into 4-bit words, the NIBBLE SELECT input (port 0, bit 0, on the 4001 ROM at A20) is examined to determine which 4-bits from the PROM write data register are to be used.

Having determined the socket and nibble to be accessed, the MCS-40™ updates the three status lines, (STATUS 0-2) to indicate an internal busy state, and outputs an active-low pulse on the LITE/ line (bank 1, port 0, bit 3, on the 4001 ROM at A10) to illuminate the PROGRAMMING indicator on the front panel of the Universal PROM Programmer (FNT PNL LITE signal at pin 86). The MCS-40™, then, transfers program control to the proper program routine stored in the 4001 ROM's on the appropriate personality card. Using the I/O ports on the personality card ROM's, the MCS-40™ can, by executing the program routine stored in these ROM's, cause the personality card to write the proper data bits into the addressed PROM location (refer to Chapters 3-6 for specific descriptions of the personality cards).

When the addressed PROM location has been successfully programmed, the MCS-40™ turns off the PROGRAMMING indicator on the front panel, sets the COMPLETE/VERIFIED bit in the status word, and clears the busy latch (BUSY/ and WRITE PROM both go false).

Note that the PROM Programmer does not return an acknowledgement signal to the control computer during Write command sequences (PPWC0/, PPWC1/, and PPWC2/).

Figure 2-7 illustrates timing for a program data sequence.



* When low, TEST indicates that the PROM location was successfully programmed. (8-bit operation only)

FIGURE 2-7
PROM PROGRAM WRITE TIMING

2.3 PIN LIST: CONTROL BOARD

The Control Board communicates with control computer, the personality cards and the PROM Programmer front panel through a 100-pin double-sided PC edge connector. Pin allocations and designated signal function for the 100-pin connector are listed in Table 2-1.

TABLE 2-1. CONTROL BOARD PIN LIST

PIN	MNEMONIC	FUNCTION	*SOURCE	*DESTINATION(S)
1	GND	Ground		
2	GND			
3				
4				
5	VCCH	Power inputs (5.85 VDC)	PS	
6	VCCH		PS	
7	VCCH		PS	
8	VCCH		PS	
9	GND	Ground		
10	GND			
11	-10V	Power inputs	PS	
12	-10V		PS	
13	GND	Ground		
14	GND			
15				
16	BD SENSE #2	Board Sense #2	PC#2	CB
17				
18	BD SENSE #1	Board Sense #1	PC#1	CB
19	CONTROL #2	Control bits	CB	
20	CONTROL #1			
21	WRITE DATA 0	Write data bus to personality cards	CB	PC's
22	WRITE DATA 1			
23	WRITE DATA 2			
24	WRITE DATA 3			
25	WRITE DATA 4			
26	WRITE DATA 5			
27	WRITE DATA 6			
28	WRITE DATA 7			
29	PROM ADDRESS 0	PROM address bus to personality cards	CB	PC's
30	PROM ADDRESS 1			
31	PROM ADDRESS 2			
32	PROM ADDRESS 3			
33	PROM ADDRESS 4			
34	PROM ADDRESS 5			
35	PROM ADDRESS 6			
36	PROM ADDRESS 7			
37	PROM ADDRESS 8			
38	PROM ADDRESS 9			
39	PROM ADDRESS 10			
40	PROM ADDRESS 11			
41	D0	MCS™-40 data bus (bi-directional)	CB←→PC's	PC's←→CB
42	D1			
43	D2			
44	D3			
45	Φ2	MCS™-40 clock signals	CB	PC's
46	Φ1			
47	CM-ROM0	Enable ROM bank 0	CB	PC
48	CM-ROM1	Enable ROM bank 1	CB	PC
49	CM-RAM1	Enable RAM bank 1	CB	PC
50	SYNC	MCS™-40 Synchronization	CB	PC's

*PS=power supply *CB=Control Board *PC=personality card *FP=front panel

TABLE 2-1. (CONTINUED)

PIN	MNEMONIC	FUNCTION	*SOURCE	*DESTINATION(S)
51	RESET/	System reset	CB	PC's
52	PROM RD DATA 0/	Data read from PROM	PC	CB
53	PROM RD DATA 1/			
54	PROM RD DATA 2/			
55	PROM RD DATA 3/			
56	PROM RD DATA 4/			
57	PROM RD DATA 5/			
58	PROM RD DATA 6/			
59	PROM RD DATA 7/			
60				
61	GND	ground		
62	PRD0/	Data read bus to control computer	CB	CC
63	PRD1/			
64	PRD2/			
65	PRD3/			
66	PRD4/			
67	PRD5/			
68	PRD6/			
69	PRD7/			
70	PPRC0/	Read data command	CC	CB
71	PPRC1/	Read status command	CC	CB
72	PPACK/	Acknowledgement	CB	CC
73	GND	ground		
74	PPWC0/	Program data command	CC	CB
75	PPWC1/	Control/high address strobe	CC	CB
76	PPWC2/	Low-address strobe	CC	CB
77	PPD0/	Data output bus from control computer	CC	CB
78	PPD1/			
79	PPD2/			
80	PPD3/			
81	PPD4/			
82	PPD5/			
83	PPD6/			
84	PPD7/			
85	INT/	Initialization signal	CC	CB
86	FNT PNL LITE	PROGRAMMING light driver	CB	FP
87				
88				
89				
90				
91	TTL RESET/	RESET switch	FP	CB
92				
93				
94				
95				
96				
97				
98				
99				
100	LOCAL ON LINE/	Not used at present		

*CB=Control Board *PC=personality card *CC=control computer *FP=front panel

CHAPTER 3
SYSTEM UTILIZATION

The Universal PROM Programmer was designed to simplify the task of programming Intel's family of PROMs. The operation is basically one of just inserting the PROM in a socket on the front panel and then directing the control computer to issue the appropriate commands to the PROM Programmer.

In the typical case where the control computer is one of Intel's INTELLEC® microcomputer development systems, the use of the PROM Programmer is particularly easy. Section 3.1 provides the information necessary for the physical installation of the PROM Programmer and for PROM devices. Refer to Appendix A for the details of the keyboard operator commands accepted by the INTELLEC® MDS Monitor for use with the PROM Programmer.

Section 3.2 contains the detailed interfacing requirements of the PROM Programmer. This information is provided for those applications where the PROM Programmer is controlled by a computer other than the INTELLEC® MDS system.

3.1 INSTALLATION

Installation procedures for the PROM Programmer are quick and easy to perform. However, to prevent possible electrical shock or damage to the components of the PROM Programmer, it is important that the instructions provided in this section be carefully followed.

Section 3.1.1 specifies the cabling requirements of the PROM Programmer. Section 3.1.2 contains step-by-step instructions for the removal and installation of personality cards. Section 3.1.4 contains the procedure for replacing the socket board assembly. Section 3.1.5 lists I/O port assignments when using the Universal PROM Programmer with an INTELLEC®MDS, INTELLEC®8/MOD 8 or INTELLEC®8/MOD 80 system.

3.1.1 CABLING

The Universal PROM Programmer connects to the control computer via a 22 gauge, multi-strand wire cable. Seven lines on the cable require twisted pair wire; one wire is grounded (see Table 3-1). Standard cables provided by Intel are 5 feet, the maximum length of the cable is 10 feet.

One end of the cable, with a 25-pin connector (AMP 205261-6 or 205201-7) plugs into a 25-pin socket connector ITT cannon DBC-25P-AA, in the Universal PROM Programmer. All lines are terminated in this 25-pin socket connector.

The other end of the cable is attached to the control computer:

INTELLEC® MDS

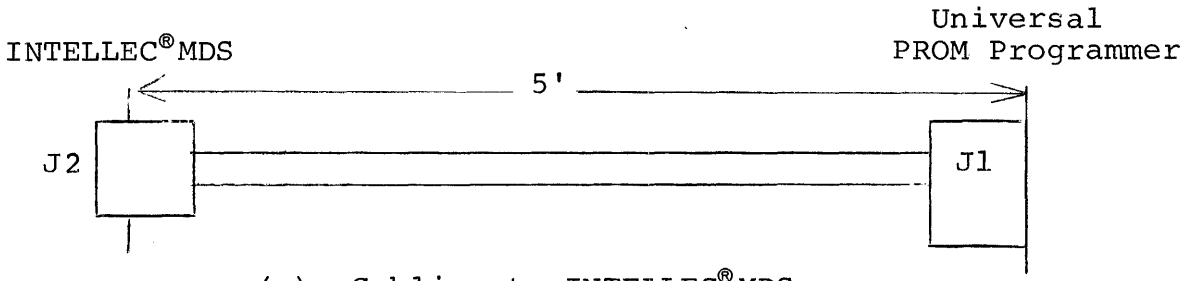
When the Universal PROM Programmer is used with an INTELLEC® MDS system, the cable (MDS-UPP-900) is attached to the back panel of the INTELLEC® MDS system via a 25-pin connector plug (AMP 205208-1) and pin assembly (AMP 205202-6 or AMP 205202-7) as shown in Figures 3-1 (a) and Appendix B-27.

TABLE 3-1

CONNECTOR PIN ASSIGNMENTS

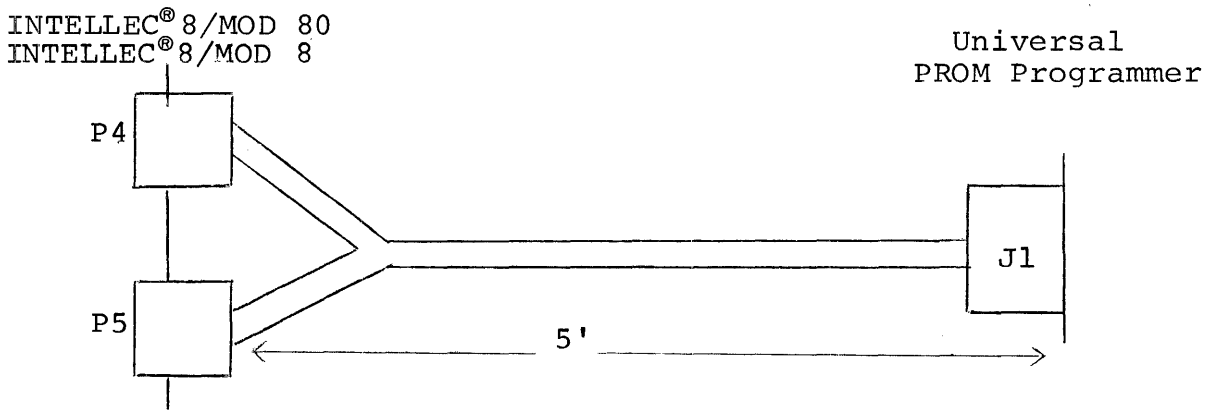
**SIGNAL	Universal PROM Programmer Connector Pin	INTELLEC® MDS Connector Pin	INTELLEC® 8/MOD 80 INTELLEC 8/MOD 8
GND	J1-1	J2-1	P4-1
PPACK/	J1-2*	J2-2*	P4-14*
PPRC1/	J1-3*	J2-3*	P5-7*
PPRC0/	J1-4	J2-4	P5-6
PRD7/	J1-5	J2-5	P4-32
PRD6/	J1-6	J2-6	P4-31
PRD5/	J1-7	J2-7	P4-13
PRD4/	J1-8	J2-8	P4-12
PRD3/	J1-9	J2-9	P4-30
PRD2/	J1-10	J2-10	P4-29
PRD1/	J1-11	J2-11	P4-11
PRD0/	J1-12	J2-12	P4-10
GND	J1-13	J2-13	P5-1
INT/	J1-14*	J2-14*	P5-28*
PPWD7/	J1-15	J2-15	P5-32
PPWD6/	J1-16	J2-16	P5-31
PPWD5/	J1-17	J2-17	P5-13
PPWD4/	J1-18	J2-18	P5-12
PPWD3/	J1-19	J2-19	P5-30
PPWD2/	J1-20	J2-20	P5-29
PPWD1/	J1-21*	J2-21*	P5-11*
PPWD0/	J1-22*	J2-22*	P5-10*
PPWC2/	J1-23*	J2-23*	P5-27*
PPWC1/	J1-24*	J2-24*	P5-9*
PPWC0/	J1-25	J2-25	P5-8

* Twisted pair wiring
** Refer to Section 3.2 for signal summary



(a) Cabling to INTELLEC® MDS

MDS-925



(c) Cabling to INTELLEC® 8/MOD 80, INTELLEC® 8/MOD 8

IMM 6-90

FIGURE 3-1

CABLING

INTELLEC®8/MOD 80, INTELLEC®8/MOD 8

When the Universal PROM Programmer is used with an INTELLEC® 8/MOD 80, or INTELLEC®8/MOD 8 system, the cable is attached to the back panel of the INTELLEC®8/MOD 80 or INTELLEC® 8/MOD 8 system via two 37-pin connector plugs (AMP 205310-0) and pin assemblies (AMP 205310-0) as shown in Figures 3-1 (c) and Appendix B-28.

Table 3-1 correlates pin assignments on the Universal PROM Programmer connector with pin assignments on the connectors used with INTELLEC®MDS and INTELLEC®8/MOD 80 INTELLEC®8/MOD 8 systems.

3.1.2 PERSONALITY CARD INSTALLATION

Since some applications require the ability to program a variety of PROM devices, the personality cards of the Universal PROM Programmer have been designed so that they may be easily exchanged by the operator. This feature gives the PROM Programmer the capability to program any Intel® PROM.

Figure 3-2 shows the PROM Programmer as viewed from the top, with the cover removed. Notice there are slots for three printed circuit cards. The Control Board is located near the rear of the PROM Programmer; it is not normally removed. The two slots near the front are for the personality cards. The slot nearest the front holds the personality card that controls Socket 1 (16-pin socket on MDS-UPP-501; 24-pin socket on MDS-UPP-502). The other slot holds the personality card that controls Socket 2 (the 24-pin socket). The step-by-step procedure for exchanging personality cards is given below.

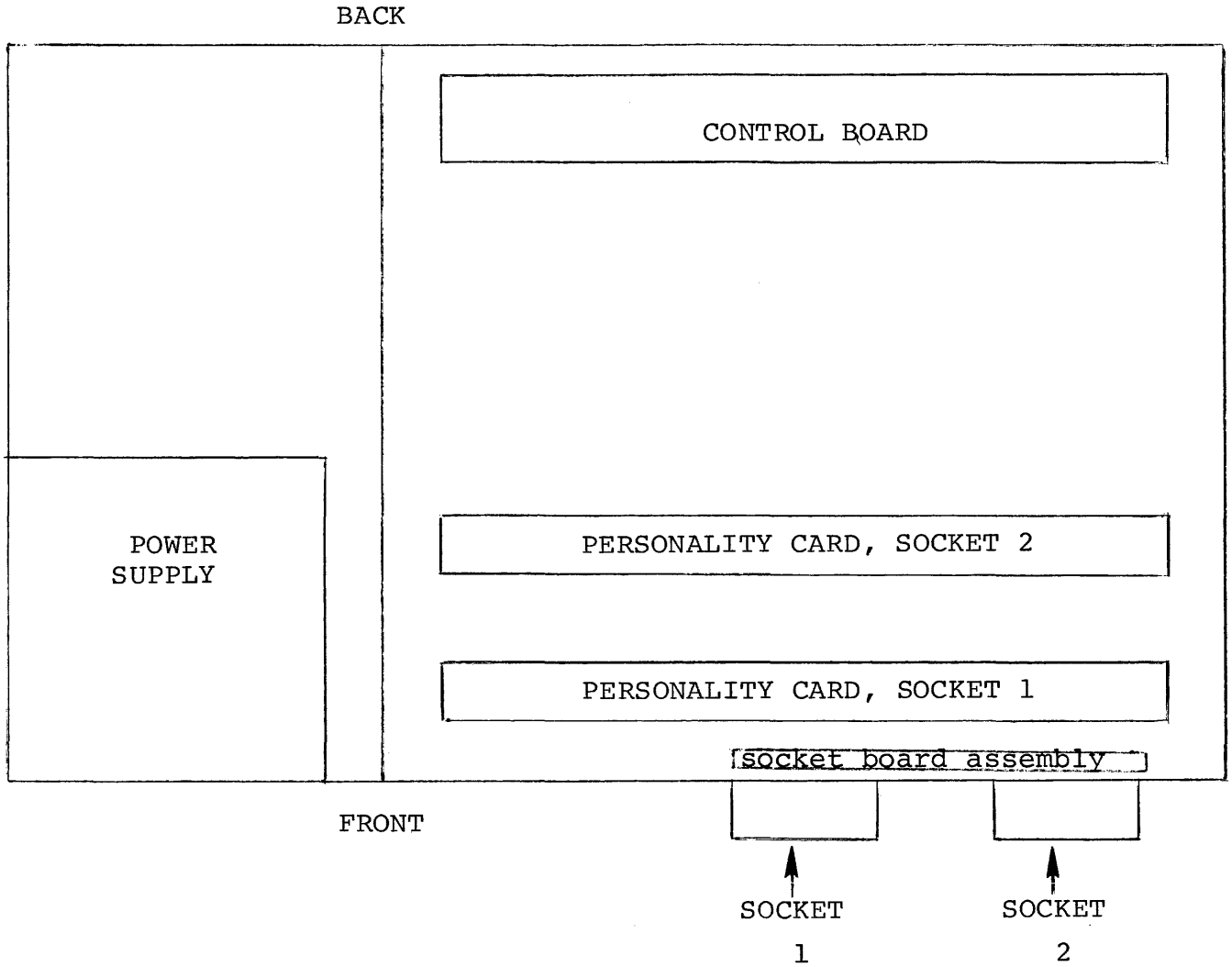


FIGURE 3-2
TOP VIEW OF PROM PROGRAMMER
(COVER REMOVED)

--WARNING--

Turn the ON/OFF switch on the front panel OFF and remove the AC power cord from the power source before removing the cover of the PROM Programmer. This will prevent electrical shock as well as protect the components of the PROM Programmer.

1) Remove the cover of the PROM Programmer by twisting each of the four screws on the cover approximately 1/4 turn counterclockwise to unlock them, and lift the cover off.

--WARNING--

The system power must be off for at least 60 seconds before the personality card is removed or inserted. This time is needed so the power supply can discharge. If this is not done, damage may occur to the personality cards.

2) If necessary, remove the previously installed personality card by first lifting up the two plastic locking tabs (one at each corner). Then grasp the edge of the personality card and pull it straight up and out of the cabinent.

3) Select the personality card to be installed. Note the card number designation (e.g., "UPP-878 Personality Module") printed on one side of the card. This side must face toward the front of the PROM Programmer when it is installed. The 100-pin edge connector on the personality card mates with the slot in the PROM Programmer.

4) Carefully slide the selected personality card into the card slot. Press down on the two plastic locking tabs to secure the card in place.

5) Double check to be sure you placed the right card in the correct socket (see Figure 3-2). Mark the identification panel located under the socket on the front panel with the designation of the personality card you have just installed.

6) Place the cover back on top of the PROM Programmer and fasten it by turning the four screws clockwise.

> CAUTION
>
> Never operate the Universal PROM Programmer with the cover off, as it will impede required air flow.

3.1.3 PROM DEVICE INSERTION

The correct insertion of the PROM in the socket on the front panel is very important. There are two things you must avoid doing:

- DON'T insert the PROM in the socket unless it is compatible with the personality card indicated below the socket on the identification panel.
- DON'T insert the PROM upside down.

Check the markings on the top of the PROM and on the identification panel to be sure they match. Using a mismatched personality card and PROM could possibly destroy the PROM, cause damage to the personality card, or both.

When inserting the PROM be sure the semi-circular notch on one end of the PROM is at the top of the socket. An upside down PROM could harm the PROM and perhaps the personality card too.

> CAUTION
>
> A PROM should not be in one of the sockets when power is turned on or when the Universal PROM Programmer or control computer is RESET, as it may result in the accidental programming of a PROM location.

3.1.4 SOCKET BOARD REPLACEMENT

> --WARNING--
>
> Turn the ON/OFF switch on the front panel OFF and remove the AC power cord from the power source before removing the cover of the PROM Programmer. This will prevent electrical shock as well as protect the components of the PROM Programmer.

1) Remove the cover of the PROM Programmer by twisting each of the four screws on the cover approximately 1/4 turn counterclockwise to unlock them, and lift the cover off.

2) If necessary, remove the installed personality cards by first lifting up the two plastic locking tabs (one at each corner). Then grasp the edge of the personality card and pull it straight up and out of the cabinet.

3) Carefully remove the front Bezel by removing 2 Hex nuts at the top corner of the UPP. Then pull the Bezel forward from the bottom to release 2 quick disconnect fasteners located at the lower left and right sides of the Bezel. Internal cables will restrict travel to approximately 4". Lay the Bezel in front of the UPP.

4) Remove the 4 cable assemblies from the front panel socket board.

5) Remove the 5 screws and lift out the socket board.

6) Place the dress cover on the front of the new socket board. (This cover provides electrical isolation between the chassis and the socket board.)

7) Install the new socket board and replace the 5 screws.

8) Replace the 4 cable assemblies as shown in Figure 3-3.

9) Replace the Bezel by fastening the quick disconnect fasteners and Hex nuts.

10) Replace the personality cards. Double check to be sure you placed the right card in the correct socket (see Figure 3-2).

11) Place the cover on top of the PROM Programmer and fasten it by turning the four screws clockwise.

> CAUTION
>
> A PROM should not be in one of the sockets when power is turned on or when the Universal PROM Programmer or Control Computer is RESET, as it may result in the accidental programming of a PROM location.

3.1.5 I/O PORT ASSIGNMENTS

Table 3-2 lists those INTELLEC®MDS I/O port addresses that are dedicated for use with Universal PROM Programmer. Table 3-3 provides the dedicated port addresses on the INTELLEC®8/MOD 8 and INTELLEC®8/MOD 80 systems.

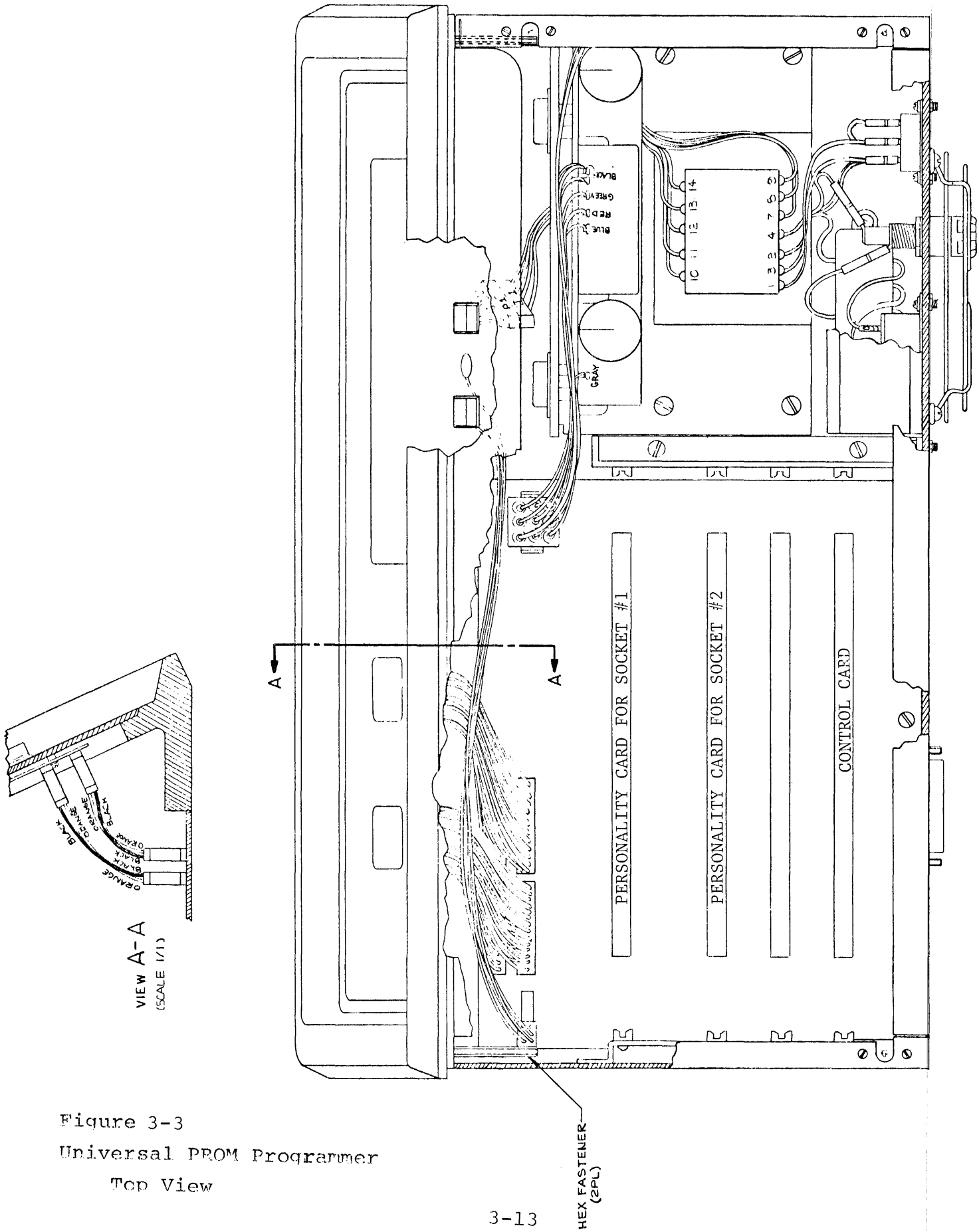


Figure 3-3
Universal PROM Programmer
Top View

TABLE 3-2

I/O PORT ADDRESSES: INTELLEC® MDS

DIRECTION	I/O PORT ADDRESS	FUNCTION
INPUT	ØØFØ	Read PROM data (LSB=DØ)
	ØØF1	Read PROM status DØ=BUSY D1=COMPLETE/VERIFIED D2=FAILED TO PROGRAM D3-D7=OTHER ERRORS*
OUTPUT	ØØFØ	Write PROM data (LSB=DØ)
	ØØF1	Output Control/High Address byte DØ-D3=most significant four bits of PROM address D4=NIBBLE SELECT D5=SOCKET SELECT D6=START RD D7=CONTROL #1 (must be Ø)
	ØØF2	Output eight least significant bits of 12-bit PROM address (LSB=DØ)

*See Section 1.2 for complete list of errors.

TABLE 3-3

I/O PORT ADDRESSES: INTELLEC® 8/8, INTELLEC® 8/80

DESCRIPTION	I/O	INTELLEC® 8/8	INTELLEC® 8/80
		PORT - BIT	PORT - BIT
PPACK/	INPUT	7 - Ø	7 - 0
PPRC1/	OUTPUT	D - 1	5 - 1
PPRCØ/	OUTPUT	D - Ø	5 - Ø
PPRD7/	INPUT	6 - 7	6 - 7
PPRD6/	INPUT	6 - 6	6 - 6
PPRD5/	INPUT	6 - 5	6 - 5
PPRD4/	INPUT	6 - 4	6 - 4
PPRD3/	INPUT	6 - 3	6 - 3
PPRD2/	INPUT	6 - 2	6 - 2
PPRD1/	INPUT	6 - 1	6 - 1
PPRDØ/	INPUT	6 - Ø	6 - 0
INT/	OUTPUT	D - 7	5 - 7
PPWD7/	OUTPUT	E - 7	6 - 7
PPWD6/	OUTPUT	E - 6	6 - 6
PPWD5/	OUTPUT	E - 5	6 - 5
PPWD4/	OUTPUT	E - 4	6 - 4
PPWD3/	OUTPUT	E - 3	6 - 3
PPWD2/	OUTPUT	E - 2	6 - 2
PPWD1/	OUTPUT	E - 1	6 - 1
PPWDØ/	OUTPUT	E - Ø	6 - Ø
PPWC2/	OUTPUT	D - 6	5 - 6
PPWC1/	OUTPUT	D - 5	5 - 5
PPWCØ/	OUTPUT	D - 4	5 - 4

3.2 INTERFACING

A parallel interface is used between the PROM Programmer and the control computer. The interface consists of two 8-bit unidirectional buses, three write command lines, two read command lines, an acknowledge line, and an initialize line. Section 3.2.1 contains a functional description of each of the interface signals. Section 3.2.2 lists their operating characteristics.

3.2.1 INTERFACE SIGNAL DESCRIPTION

This section defines each of the signal lines that comprise the interface between the PROM Programmer and the control computer. Table 3-4 correlates the Control Board edge connector pin assignments with the corresponding pins on the back-panel-mounted connector, for each of the interface signals. The interface is a negative true bus (a TTL 'Ø' is the active state).

PPRC0/ — Read Data Command; issued by the control computer to initiate a read of a PROM location. Signals the MCS™-40 (through RD PROM) to start a read, and gates the PROM RD DATA/ lines (from the PROM) through to PRD0/-PRD7/.

PPRC1/ — Read Status Command; when issued by the control computer it directly enables the acknowledge signal, PPACK/. (Status is always available on PRD0/-PRD7/ unless PPRC0/ is active.)

PRD0/-PRD7/ — Read Data Lines; used to transmit either data or status (as requested by PPRC0/ or PPRC1/) to the control computer. PRD0/ is the least significant bit.

PPWC0/ — Write Data Command; issued by the control computer to initiate the programming of a PROM location. Signals the MCS™-40 (through Write PROM) to start a program operation, and causes the data currently on PPD0/-PPD7/ to be latched in the Write Data Register.

TABLE 3-4

BACK PANEL CONNECTOR PIN LIST

Control Board Edge Connector Pin	Universal PROM Programmer Back Panel Connector Pin	SIGNAL	DESCRIPTION
61	1	GND	Ground (signal return)
62 63 64 65 66 67 68 69	12 11 10 9 8 7 6 5	PRD0/ PRD1/ PRD2/ PRD3/ PRD4/ PRD5/ PRD6/ PRD7/	Read data or status word is input to control computer on these lines. PRD0/ = LSB (logic 1 = 0VDC)
70	4	PPRC0/	PROM Read data command PPRC0/ initiates a data read.
71	3	PPRC1/	Read status command PPRC1/ initiates a status read. The status word is input on lines PRD0/-PRD7/: PRD0/ = BUSY (logic 1 = BUSY) PRD1/ = COMPLETE/VERIFIED PRD2/ = FAILED TO PROGRAM PRD3/ = CANNOT PROGRAM PRD4/ = ADDRESS ERROR PRD5/ = HARDWARE FAILURE PRD6/ = NO PERSONALITY CARD PRD7/ = NOT USED } Valid Only If BUSY = Logic 0

TABLE 3-4. (Continued)

Control Board Edge Connector Pin	Universal PROM Programmer Back Panel Connector Pin	SIGNAL	DESCRIPTION
72	2	PPACK/	Read acknowledge When PPACK/ is true (0 VDC) status of read data is available on lines PRDØ-PRD7/.
73	13	GND	Ground (signal return)
74	25	PPWCØ/	Write data strobe PPWCØ/ initiates a program sequence and strobes write data into the universal PROM Programmer on lines PPDØ/-PPD7/ When programming 4-bit words NIBBLE SELECT bit of Control/High address word specifies whether most or least significant 4 bits are used.
76	24	PPWC1/	Control/High address strobe PPWCØ/ strobes Control/High address byte into Universal PROM Programmer on lines PPDØ/-PPD7/: PPDØ/-PPD3/ = Four most significant bits of 12-bit PROM address (PWD3/=MSB) PPD4/ = NIBBLE SELECT (logic 1→ bits 0-3 used) (logic Ø→ bits 4-7 used) PPD5/ = SOCKET SELECT (logic 1→ 16 pin, socket #1) (logic 0→ 24 pin, socket #2)

TABLE 3-4. (Continued)

Control Board Edge Connector Pin	Universal PROM Programmer Back Panel Connector Pin	SIGNAL	DESCRIPTION
76 (Cont'd)	24 (Cont'd)	PPWC1/ (Cont'd)	PPD6/ = START READ (logic 1 → start read) (logic 0 → do not start read) PPD7/ = CONTROL #1 (must be logic 0)
75	23	PPWC2/	Low address strobe PPWC2/ strobes the eight least significant bits of the 12-bit PROM address into the Universal PROM Programmer on lines PPDØ/-PPD7/. (PPDØ/ = LSB of address)
77 78 79 80 81 82 83 84	22 21 20 19 18 17 16 15	PPDØ/ PPD1/ PPD2/ PPD3/ PPD4/ PPD5/ PPD6/ PPD7/	Write data, control/high address and low address bytes are output to Universal PROM Programmer on these lines (PPDØ/=LSB) (logic 1 = 0 VDC)
85	14	INT/	System reset (minimum duration = 500 µsec.)

PPWC1/ — Mode Control and Address Strobe; when issued by the control computer PPD4/-PPD7/ are latched in the Mode Control Register, and PPD0/-PPD3/ are latched in the High Address Register.

PPWC2/ — Low Address Strobe; when issued by the control computer PPD0/-PPD7/ are latched in the Low Address Register.

PPD0/-PPD7/ — Write Data Lines; used to transmit data, address, or mode control information (as indicated by PPWC0/, PPWC1/, or PPWC2/) to the various registers in the PROM Programmer. PPD0/ is the least significant bit.

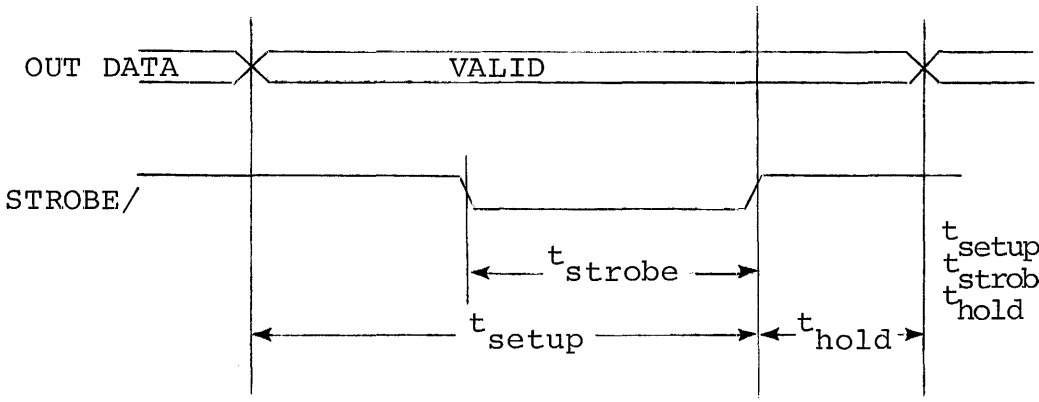
PPACK/ — Read Acknowledge Signal; indicates to the control computer that the data or status (requested by PPRC0/ or PPRC1/) is available on PRD0/-PRD7/.

INT/ — System Initialization Signal; when issued by the control computer causes the MCS-40™ to stop anything in progress, initialize itself, and wait for either a PPRC0/ or a PPWC0/ command.

3.2.2 OPERATING CHARACTERISTICS

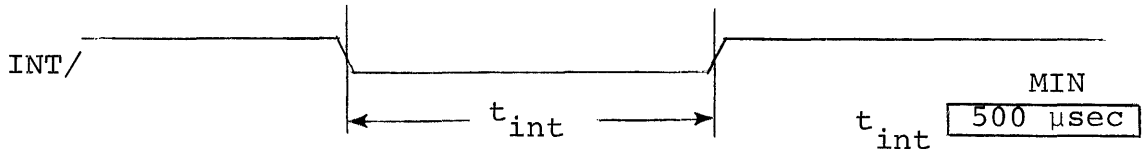
AC characteristics for the Universal PROM Programmer are summarized in Figure 3-4. DC characteristics are listed in Table 3-5.

WRITE DATA TIMING:



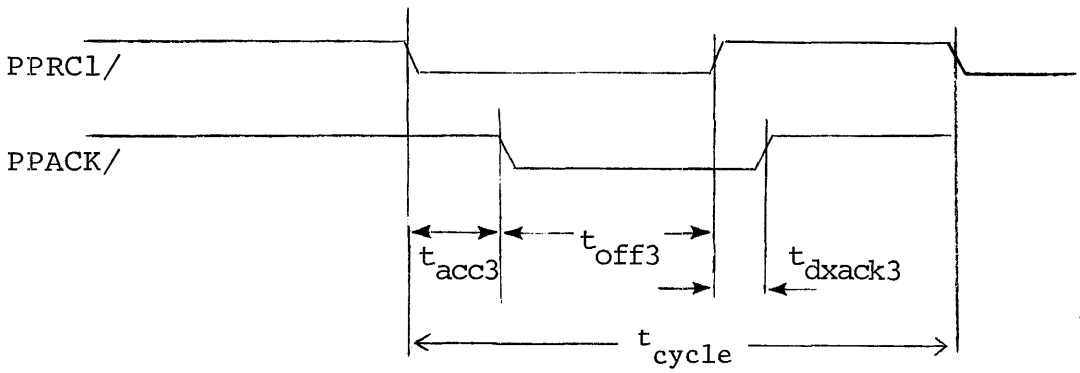
	MIN	MAX
t_{setup}	1500 ns	-
t_{strobe}	700 ns	-
t_{hold}	675 ns	-

INITIALIZE TIMING:



	MIN
t_{int}	500 µsec

READ STATUS TIMING:



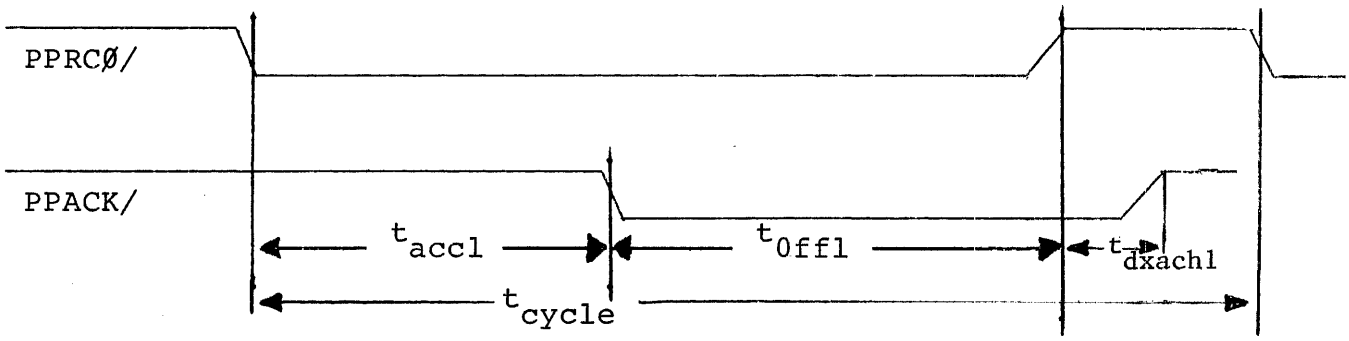
	MIN	TYP	MAX
t_{acc3}	0	25 ns	50 ns
t_{off3}	0	-	-
t_{dxack3}	0	25 ns	50 ns

$$t_{cycle} \geq t_{acc3} + t_{0ff3} + t_{dxach3}$$

FIGURE 3-4

AC CHARACTERISTICS

READ DATA TIMING (Command Initiated):



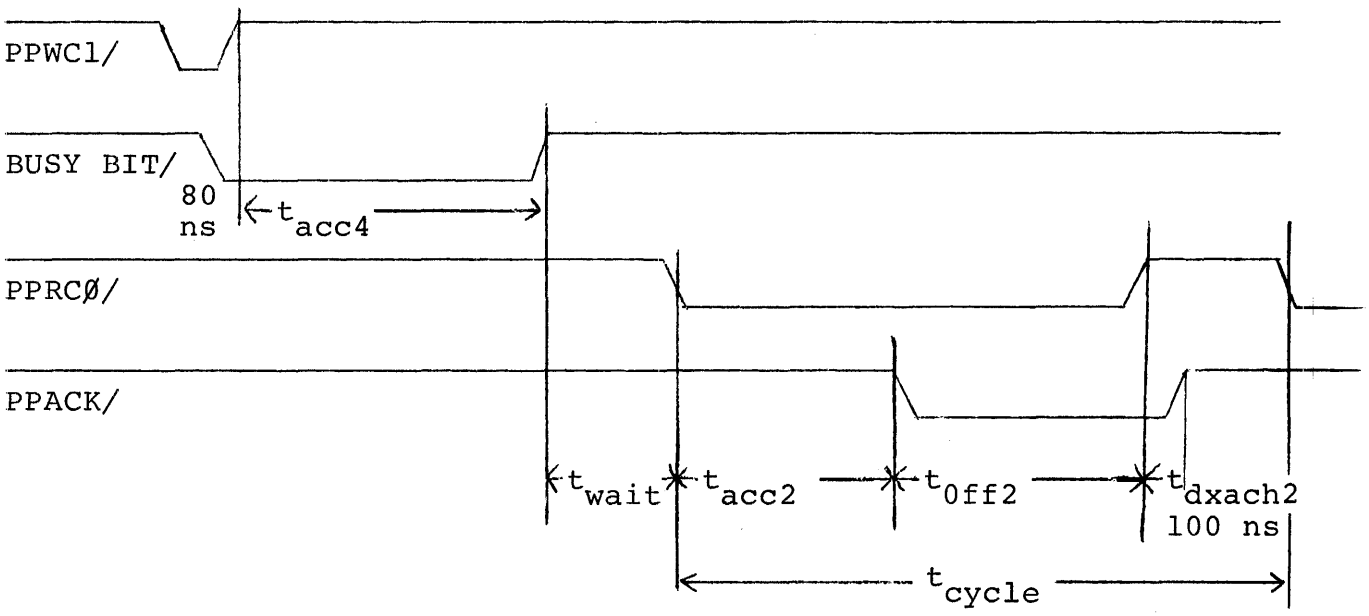
	MIN	TYP	MAX
t_{accl}	-	1.6 ms	2.0 ms
t_{0ffl}	-	-	600 µs
t_{dxachl}	-	100 ns	150 ns

$$t_{cycle} \geq t_{accl} + t_{0ffl} + t_{dxachl}$$

FIGURE 3-4 (continued)

AC CHARACTERISTICS

READ DATA TIMING METHOD #2 (Using START RD bit of control byte):



	MIN	TYP	MAX
t_{acc4}	-	1.6 ms	-
t_{wait}	0	-	-
t_{acc2}	200 ns	1000 ns	2000 ns
t_{0ff2}	0	-	-
t_{dxach2}	-	100 ns	150 ns

$$t_{cycle} \geq t_{acc2} + t_{0ff2} + t_{dxach2}$$

FIGURE 3-4 (Continued)

AC CHARACTERISTICS

TABLE 3-5

DC CHARACTERISTICS

SIGNAL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
PPRCØ/	V_{IL} Input low voltage		0.7	V	VCC = 5.0
	V_{IH} Input high voltage	2.0		V	VCC = 5.0V
	I_R Input leakage current		-2.8	mA	VCC = 5.25V, V_R = 5.25
	I_F Input load current		-8.0	mA	VCC = 5.0 VIL = 0.3V
PPRC1/	V_{IL}		0.8	V	
	V_{IH}	2.0		V	
	I_R		-40	µA	
	I_F		-1.6	mA	
PRDØ/- PRD7/, INT/ PPWCØ/- PPWC2/	V_{IL}		0.8	V	VCC = 4.5V
	V_{IH}	2.0		V	VCC = 4.5V
	I_R		1	mA	VCC = 5.5V
	I_F		-1.6	mA	VCC = 5.5V
PRDØ/-	V_{OL} Output low voltage		0.7	V	VCC = 4.5 I_{sink} = 20 mA
PRD7/	V_{OH} Output high voltage			V	open collector 250Ω
	I_{OL} Output sink current		20	mA	VCC = 4.5V
	I_{OH} Output source current		12	mA	VCC = 5.0 VOUT = 2.0
PPACK/	V_{OL}		0.8	V	VCC = 4.5V
	V_{IH}	2.4		V	VCC = 4.5 VIN = 0.8 VOUT = 400 µA
	I_{OL}		-1.6	mA	VIN = 0.4 VCC = 5.5
	I_{OH}		1	mA	VIN = 5.5, VCC = 5.5V

CHAPTER 4
THE UPP-878 PERSONALITY CARD

The UPP-878 Personality Card contains the logic that is needed to both program and read the contents of a 2708 PROM location. The 2708 is an erasable PROM and is organized as a 1024 word by 8-bit memory. Access time for the 2708 PROM is 500 nanoseconds. Intel also manufactures a 2704 PROM. Both types of PROMs are identical except for the size of their memories:

The 2708 contains 1024 8-bit words.
The 2704 contains 512 8-bit words.

The UPP-878 Personality Card is designed to handle these PROMs in addition to PROMs of similar characteristics but different speeds. Table 4-1 lists the available selections. Detailed specifications for the 2708 and 2704 are contained in Section 4.1.

Section 4.2 discusses the major components of the UPP-878 Personality Card. It also discusses the sequence and the timing of events for both the read and the program operations.

Section 4.3 provides a pin list for the UPP-878 Personality Card. This list includes the allocation and the function of each of the signals that appear on the pins of the Personality Card edge connector.

Appendix C discusses the 2708 auxiliary software package. This package is needed to program Intel's 2708 and 2704 PROMs when using the UPP attached to an Intellec® MDS. This auxiliary software is required due to unique programming algorithm of the 2708 family of PROMs. (See Intel's 2708 specification sheet).

TABLE 4-1

THE UPP-878 PERSONALITY CARD DEVICE SELECTION

PROM	PINS	NUMBER OF BITS	ORGANIZATION	ACCESS TIME
2704	24	4096	512 X 8	500 ns
2704-5	24	4096	512 X 8	1.0 µs
2708	24	8192	1024 X 8	500 ns
8704	24	4096	512 X 8	450 ns
8704-4	24	4096	512 X 8	850 ns
8708	24	8192	1024 X 8	450 ns
8708-4	24	8192	1024 X 8	850 ns
8708-5	24	8192	1024 X 8	1.0 µs

4.1 2708/2704

The 2708 is a 1024 word by 8-bit electrically programmable read only memory, designed for use in limited quantities and when fast turn-around and pattern experimentation are important. The PROM Programmer can program all 1024 words of the PROM in less than five minutes. The 2708 can be erased by controlled exposure to high intensity ultraviolet light. After it is cleared, the 2708 can be reprogrammed by the PROM programmer. The 2708 may be erased and reprogrammed as often as desired.

The 2708 is operated by standard power supply voltages: +12 volts and $\pm$5 volts. The data outputs of the 2708 are tri-state. Both inputs and outputs to the 2708 are TTL compatible during both read and program operations. The 2708 is shipped to the customer in an erased condition; that is, with ones (output high) in all memory locations. During programming, zeros (output low) are loaded selectively into the chip's memory locations. All eight bits of one word are programmed simultaneously by setting the desired bit pattern on the eight data terminals of the 2708. The address of the word to be programmed is placed on the ten address terminals of the 2708. The selected memory location is then programmed by two pulsed signals applied to the chip's PROGRAM and CHIP SELECT pins. Section 4.2 includes detailed specifications of the signals used to program the 2708.

The 2708 is packaged in a 24-pin dual in-line package with a transparent quartz lid. A silicon die is located under the transparent lid. Erasure of the PROM is accomplished by exposing the silicon die to ultraviolet light at a wavelength of 2537 Angstroms. The recommended integrated dose (the product of intensity and exposure time) is 10 W-sec/cm^2. Examples of ultraviolet sources which can be used are the Model UV5 and the Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc., (4115 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. Fifteen to twenty minutes exposure to

the lamp, at a distance of one inch, will clear the PROM completely. Avoid unnecessary or prolonged exposures, which are potentially damaging to the PROM.

--WARNING--

High intensity ultraviolet light can cause serious burns. Ultraviolet radiation can also generate potentially hazardous amounts of ozone. Observe the following precautions when using an ultraviolet source to erase a PROM:

1) Never expose skin or eyes to the source directly.
2) Do not stare at an object which is under ultraviolet illumination. The light is invisible, but is nevertheless injurious to eye tissue.
3) Use the source only in a well-ventilated area.

The 2704 is identical to the 2708 in every respect except for the total number of words of memory. The 2708 has 1024 words of memory, while the 2704 has 512 words of memory; as a consequence the 2704 has only 9 address input pins instead of the 10 address input pins of the 2708.

4.2 FUNCTIONAL DESCRIPTION: UPP-878 PERSONALITY CARD

The UPP-878 Personality Card contains all of the logic needed to either program or read a word (8-bits) of a 2708 PROM. The Personality Card operates under the supervision of the Control Board (see Chapter 2). The PROM itself is plugged into the 24-pin socket on the front panel of the PROM Programmer. This socket is wired directly to the Personality Card.

The Control Board is responsible for supplying address and data information, and requesting that the Personality Card perform either a program or a read operation. The Personality Card, in turn, attempts to perform the requested operation, returns data to the Control Board, and notifies the Control Board of the success or failure of the operation.

Figure 4-1 is a functional block diagram of the UPP-878 Personality Card. It may be helpful to frequently refer to this diagram during the following discussion of the Personality Card. The names of the signals that appear in Figure 4-1 generally correspond to the names used on the schematic of the UPP-878 Personality Card (see Appendix B).

Communications between the Personality Card and the Control Board are handled by four parallel buses:

A) The MCS-40™ Bus includes the control, timing and data paths that are necessary for the operation of the 4040 processor on the Control Board and the two 4001 ROMs on the Personality Card.

B) The PROM Address bus provides the Personality Card with the 12-bit PROM address from the Control Board.

C) The PROM Write Data bus from the Control Board provides the 8-bit data word to be programmed into the PROM by the Personality Card.

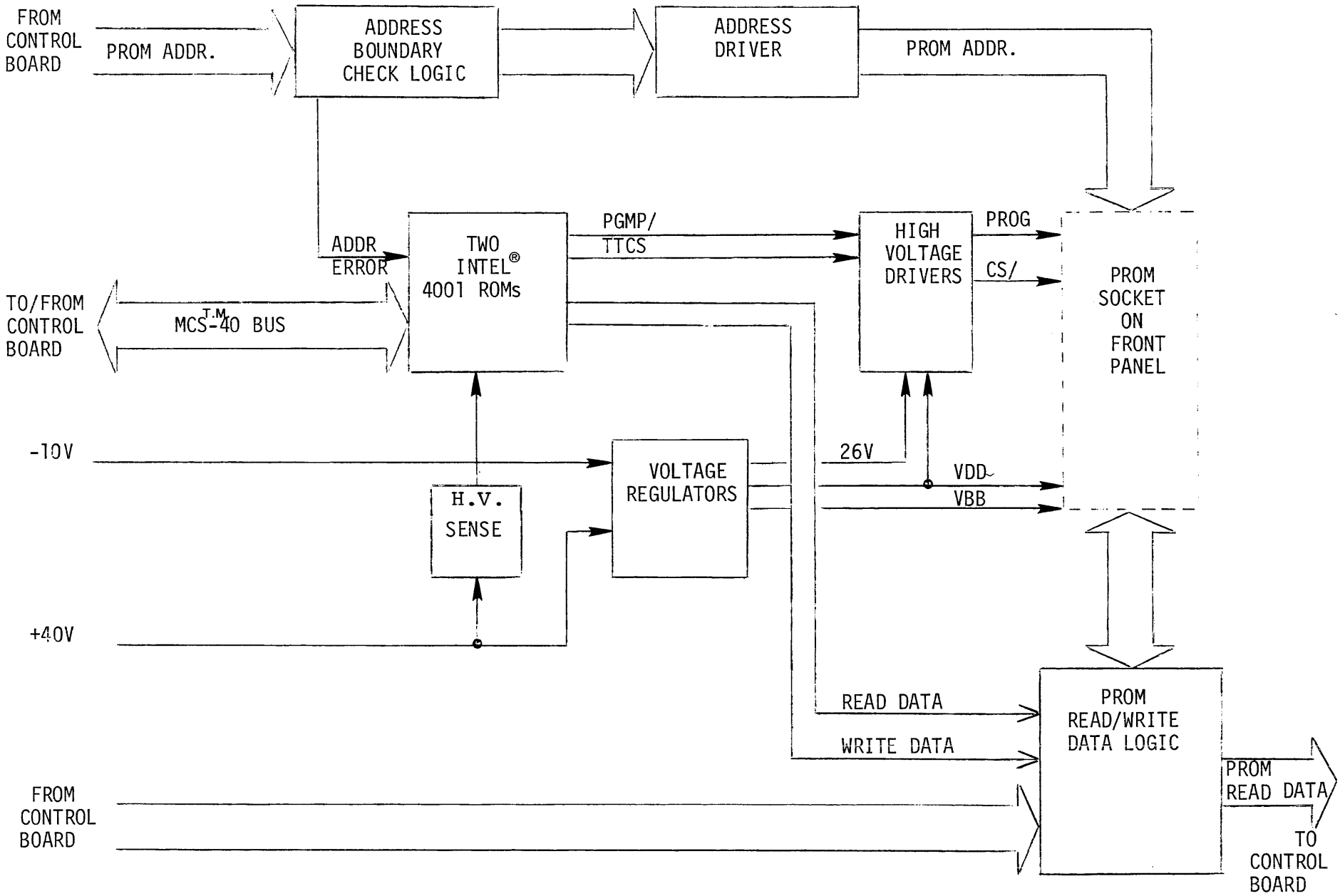


FIGURE 4-1

UPP-878 PERSONALITY CARD BLOCK DIAGRAM

D) The PROM Read Data bus returns the 8-bit data word in the selected PROM location to the Control Board.

There are six major components of the UPP-878 Personality Card as shown in Figure 4-1:

1) The PROM address logic examines the 12-bit address from the Control Board. A bank of switches (S1) is incorporated in the PROM address logic. The state of these switches should reflect the type of PROM (2708 or 2704) being programmed. See Figure 4-2 for the location and switch settings of S1. The PROM Programmer operator may change the setting of S1 if necessary. (Refer to Section 7.2 for instructions for the removal and installation of Personality Cards.) Based on the state of S1 the PROM Address logic can determine if the 12-bit address exceeds the bounds of the selected PROM. If it does, the logic will activate the address out of bounds line (A00B/) to port 1 of a 4001 ROM (A11).

2) The two Intel® 4001 ROMs are a part of the MCS™-40 (the processor itself is located on the Control Board). The ROMs contain instructions for the MCS™-40 that will effect the reading or programming of a 2708 PROM. The MCS™-40 interacts with the Personality Card through the I/O ports on the two ROM chips.

3) The Voltage Regulators supply the operating voltages +12V, +26V and -5V to the PROM at VDD (pin 83), PROG driver (pin 82) and VBB (pin 85), respectively. The +5V for VCC (pin 88) is supplied directly from VCCH through a dropping diode. The +26V regulator has two protective circuits. One is a current limit of 300 mA (set by R16 and R17) to protect the regulator and the PROG driver against shorts at the PROM socket. The other is a crow-bar circuit that will short out the +40V supply, should the regulator fail.

--CAUTION--

It is possible to damage the regulator if the personality card is removed when the +40 volt line is not totally discharged. For this reason, a user must wait 60 seconds after system power is off before removing this personality card.

4) The Write Data Gate allows the PROM Write Data from the Control Board to move on to the PROM during a program operation. The gate is closed except during a program operation. It is controlled by the Write Data Enable line from port Ø of a 4001 ROM (A5).

5) The PROM Data Logic handles the flow of data to and from the PROM. During a program operation the PROM Write Data is passed on to the PROM through open collector drivers. During a read operation, the Read Data Enable line from port 3 of a 4001 ROM (A11) will signal the PROM Data Logic. This will allow the PROM Read Data to be passed back to the Control Board (in complemented form).

6) The High Voltage Drivers perform the actual PROM programming. The CS/ driver is a high voltage open collector gate which when deactivated by TTCS allows CS/ to rise to programming level (12V). The program pulse (PROG) is generated by a 3-state transistor driver circuit. The PROG line (pin 82) is driven to 26V during the programming operation. During read operations, the PROG line is grounded (see Figure 4-3). (For compatibility with future devices that will also be programmed by the UPP-878 Personality Card, the "float" during read" function can be enabled with the switch at S1-3.)

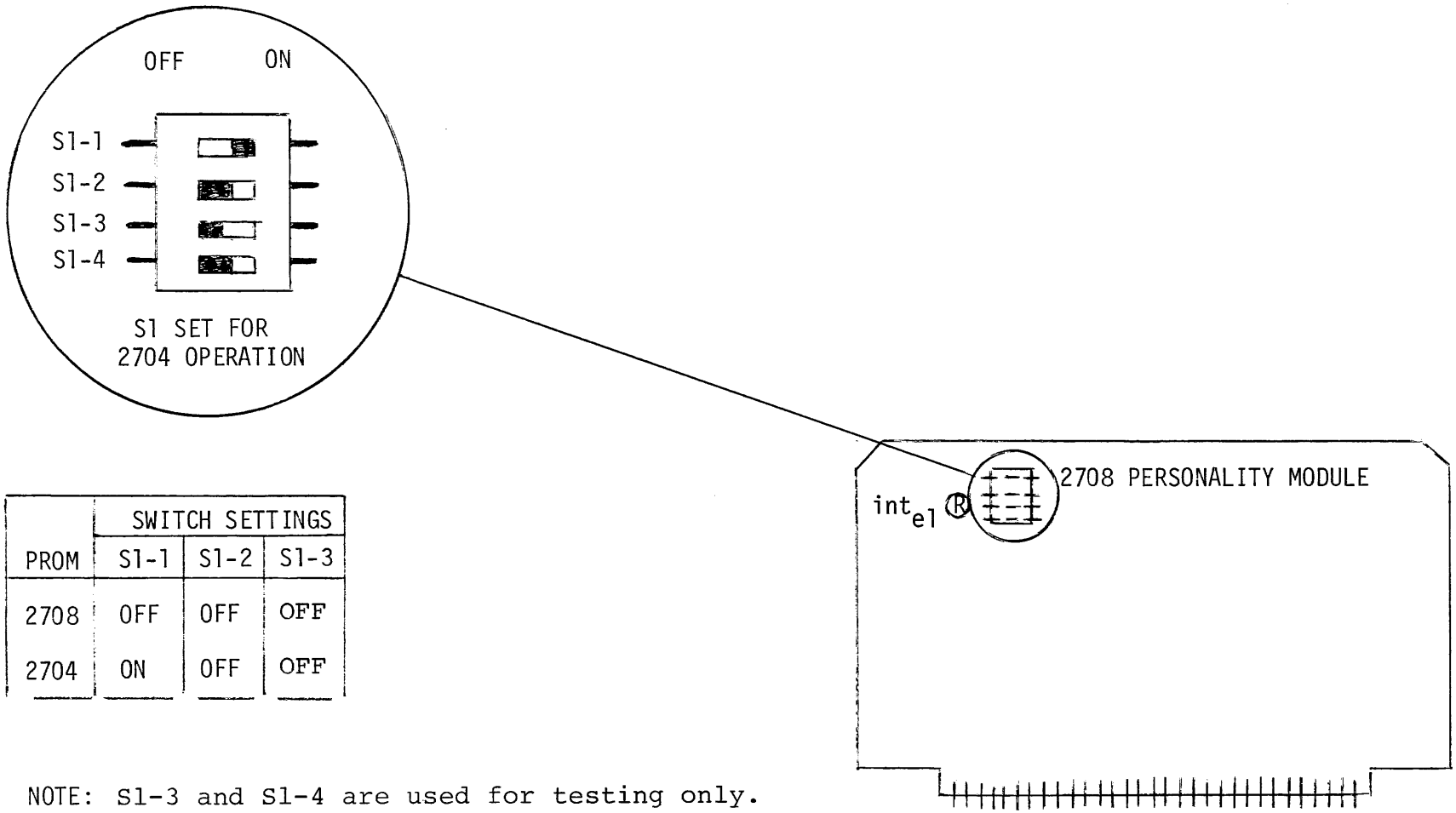
The remainder of this section will describe how the above functional blocks interact to perform the two operations: program and read. There are two distinct locations in the ROM on the UPP-878 Personality Card that are the entry points to which the MCS™-40 branches: one entry point for a program operation and one for a read. When the Personality Card receives control it assumes the PROM Address is available on the address bus. In the case of a program operation it also assumes the PROM Write Data is on the data bus. In either case the first step is to check for an address error.

The address check is a matter of testing the Address Out Of Bounds signal (AOOB/). If the signal indicates an address error the Personality Card aborts the operation and returns control to the Control Board. If the address is valid, the operation continues.

PROM READ DATA:
In the case of a read operation there is little left that needs to be done, since the static conditions of the Personality Card present the selected PROM data word to the PROM Data Logic. All the MCS™-40 needs to do is turn on the Read Data Enable line from the 4001 ROM (All) output port 3. When this is done the PROM Read Data is returned to the Control Board. The Personality Card has then completed the read operation.

PROM PROGRAM DATA:
The program operation is only slightly more involved. After the address has been checked the program operation begins. The sequence of events is as follows:

1) The MCS™-40 checks to see that the Voltage Regulator is receiving +40 volts from the Power Supply. If the signal HV Sense from the Voltage Regulator to ROM (All) port 2 is true, then the +40 volts is available. If not, the program operation is aborted, and control returns to the Control Board.



PROM	SWITCH SETTINGS		
	S1-1	S1-2	S1-3
2708	OFF	OFF	OFF
2704	ON	OFF	OFF

NOTE: S1-3 and S1-4 are used for testing only.

FIGURE 4-2
LOCATION AND OPERATION OF SWITCH S1

2) The signal TTCS is switched from high (which indicates read) to low (indicating program). This transition causes CS/ to be pulsed as shown on the timing diagram, Figure 4-3.

3) The signal Write Data Enable is switched from low to high allowing the PROM Write Data to be presented to the PROM.

4) The signal PGMP/ is switched from high (its read level) to low, causing the high voltage driver to allow the programming pulse PROG to rise.

5) The Personality Card now holds these conditions constant for 1 msec., while the data is electrically programmed into the PROM.

6) When the 1 msec. has elapsed, the signal PGMP/ is switched back to high, removing the programming pulse PROG from the PROM.

7) The signal Write Data Enable is switched back to low, removing the PROM Write Data from the PROM.

8) The signal TTCS is switched back to high, causing CS/ to return to the read level.

9) Control is then returned to the Control Board.

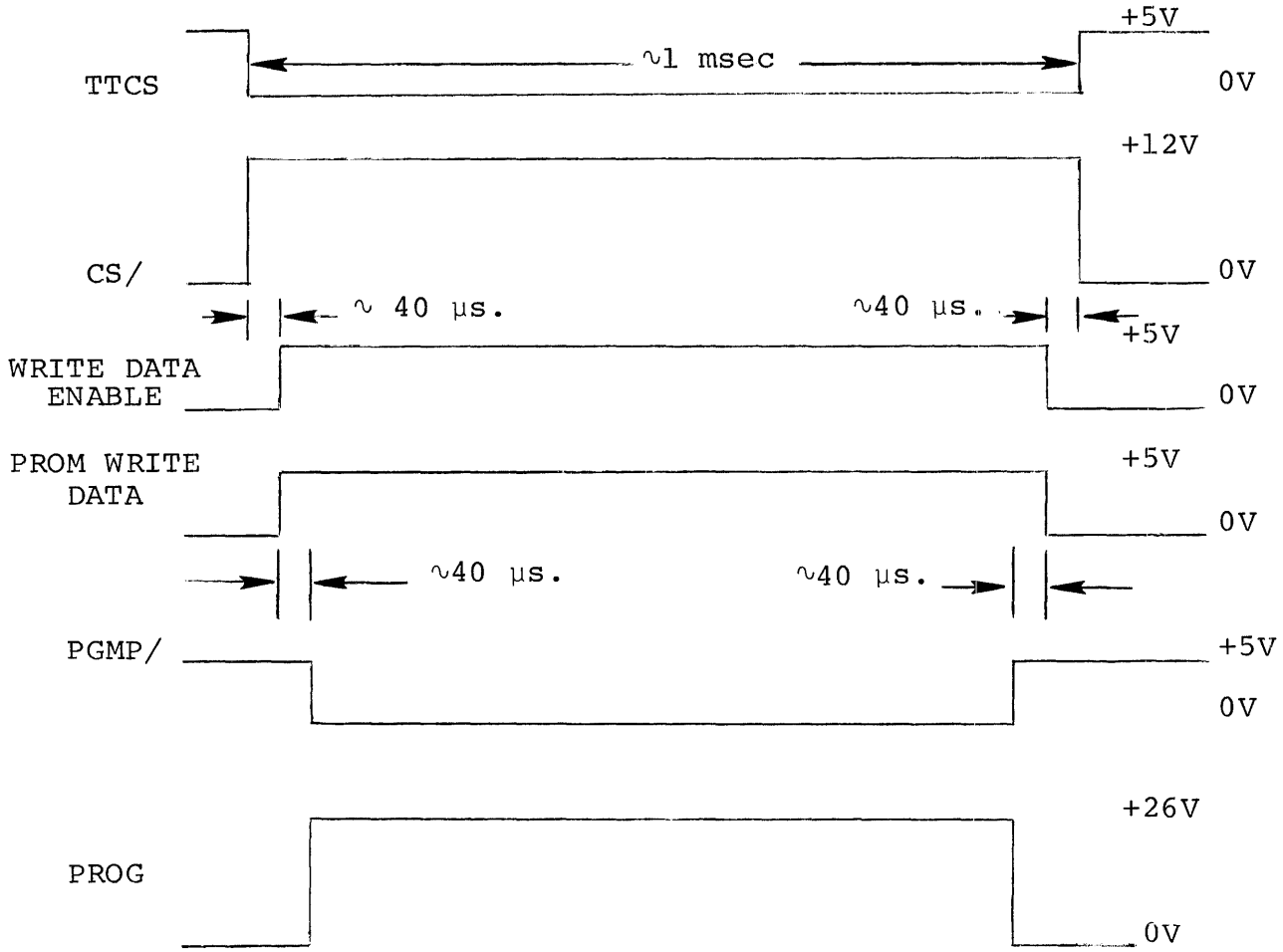


FIGURE 4-3

UPP-878 PERSONALITY CARD PROGRAM TIMING

4.2.1 SYSTEM SOFTWARE REQUIREMENTS

The 2708 family of PROM requires that the programming operation start at location Ø and go through the entire PROM sequentially. One pass through all addresses is defined as one program loop. The total number of loops required is 100. Thus 102,400 program operations are required to program a 2708 (51,200 for 2704).

Figure 4-4 shows a system flow diagram to perform a transfer function and a program function.

4.3 PIN LIST: UPP-878 PERSONALITY CARD

The UPP-878 Personality Card communicates with the Control Board and the PROM socket on the front panel through a 100-pin double-sided PC edge connector. Pin allocations and designated signal functions for this 100-pin connector are given in Table 4-2.

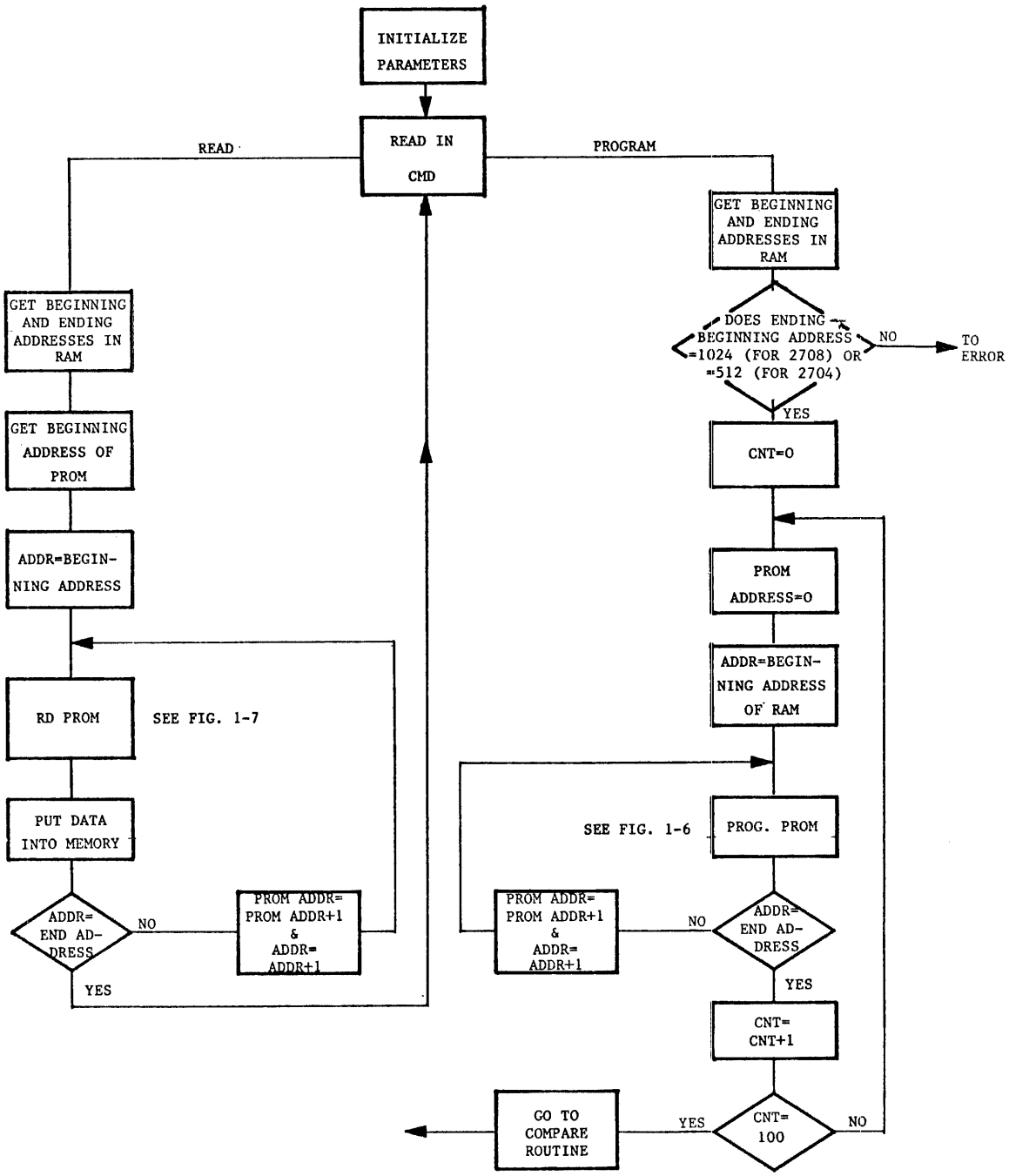


FIGURE 4-4

UPP-878 SYSTEM SOFTWARE (FLOW CHART)

TABLE 4-2

UPP-878 PERSONALITY CARD PIN LIST

PIN	MNEMONIC	FUNCTION	SOURCE*	DESTINATION*
1	GND	Ground		
2	GND			
3				
4				
5	VCCH	Power inputs (5.85 VDC)	PS	PC
6	VCCH			
7	VCCH			
8	VCCH			
9	GND	Ground		
10	GND			
11	-10	Power inputs	PS	PC
12	-10			
13	GND	Ground		
14	GND			
15				
16	BD SEN/	Board sense	PC	CB
17				
18				
19	CONTROL	Control bit		
20				
21	WRITE DATA 0	Write data bus from Control Board	CB	PC
22	WRITE DATA 1			
23	WRITE DATA 2			
24	WRITE DATA 3			
25	WRITE DATA 4			
26	WRITE DATA 5			
27	WRITE DATA 6			
28	WRITE DATA 7			
29	PROM ADDRESS 0	PROM address bus from Control Board	CB	PC
30	PROM ADDRESS 1			
31	PROM ADDRESS 2			
32	PROM ADDRESS 3			
33	PROM ADDRESS 4			
34	PROM ADDRESS 5			
35	PROM ADDRESS 6			
36	PROM ADDRESS 7			
37	PROM ADDRESS 8			
38	PROM ADDRESS 9			
39	PROM ADDRESS 10			
40	PROM ADDRESS 11			
41	D0	MCS-40™ data bus (bi-directional)	CB/PC	PC/CB
42	D1			
43	D2			
44	D3			
45	Ø2	MCS-40™ clock signals	CB	PC
46	Ø1			
47	CM-ROM	ROM bank enable	CB	PC
48				
49				
50	SYNC	MCS-40™ synchronization	CB	PC

*PS=power supply CB=Control Board PC=UPP-878 Personality Card FP=Front Panel (PROM socket)

TABLE 4-2. (Continued)

PIN	MNEMONIC	FUNCTION	SOURCE*	DESTINATION*
51	RESET	MCS-40™ reset	CB	PC
52	PROM RD DATA 0/			
53	PROM RD DATA 1/			
54	PROM RD DATA 2/			
55	PROM RD DATA 3/	Data read	PC	CB
56	PROM RD DATA 4/	from PROM		
57	PROM RD DATA 5/			
58	PROM RD DATA 6/			
59	PROM RD DATA 7/			
60				
61	A7			
62	A6			
63	A5			
64	A4	Address to PROM	PC	FP
65	A3			
66	A2			
67	A1			
68	A0			
69	O1	PROM data	PC/FP	FP/PC
70	O2	(bi-directional)		
71	O3		PC	FP
72	VSS	Power to PROM		
73				
74				
75				
76				
77	O4			
78	O5	PROM data	PC/FP	FP/PC
79	O6	(bi-directional)		
80	O7			
81	O8			
82				
83	VDD	Power to PROM	PC	FP
84				
85	VBB	Power to PROM	PC	FP
86	A9	Address to PROM	PC	FP
87	A8			
88	VCC	Power to PROM	PC	FP
89				
90				
91	GND	Ground		
92	GND			
93				
94				
95	+40V	Power to Voltage	PS	PC
96	+40V	Regulator		
97				
98				
99	GND	Ground		
100	GND			

* PS = Power Supply CB = Control Board PC = UPP-878 Personality Card
FP = Front Panel (PROM socket)

CHAPTER 5

THE UPP-864 PERSONALITY CARD*

The UPP-864 Personality Card contains the logic that is needed to both program and read the PROMs listed in Table 5-1. This list of PROMs will be referred to as the 3604 PROM family. The 3604 PROM family is programmed using the same technique, but each member of this family may have different word lengths, access times, amount of storage, and package sizes (e.g., 24 and 16 pin dip). Detailed specifications of the 3604 PROM family are contained in Section 5.1. The 3604 PROM family can be divided into two sub-families: devices with word lengths of 4 bits and those with word lengths of 8 bits. The UPP-864 Personality Card can accommodate both sub-families, the 8 bit family directly through the socket on the front panel, and the 4 bit family by insertion of an adaptor in the socket on the front panel. The adaptor converts the 24 pin socket into a 16 pin socket.

Section 5.2 discusses the major components of the UPP-864 Personality Card. It also discusses the sequence and the timing of events for both the read and program operations.

Section 5.3 provides a pin list for the UPP-864 Personality Card. This list includes the allocation and the function of each of the signals that appear on the pins of the Personality Card edge connector.

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*NOTE: The UPP-864 has been replaced by the UPP-865, which programs all PROMs previously programmed by the UPP-864. This chapter is retained for reference only; refer to Chapter 12 for data on the UPP-865.

TABLE 5-1

UPP-864 PERSONALITY CARD DEVICE SELECTION

PROM	PINS	NUMBER OF BITS	ORGANIZATION	ACCESS TIME
3604	24	4096	512 X 8	70 ns
3604-4	24	4096	512 X 8	90 ns
M3604	24	4096	512 X 8	90 ns
M3604-6	24	4096	512 X 8	120 ns
3624	24	4096	512 X 8	70 ns
3624-4	24	4096	512 X 8	90 ns
M3624-6	24	4096	512 X 8	90 ns
3602*	16	2048	512 X 4	70 ns
3602-4*	16	2048	512 X 4	90 ns
3602L-6*	16	2048	512 X 4	90 ns
3622*	16	2048	512 X 4	70 ns
3622-4*	16	2048	512 X 4	90 ns
3622L-6*	16	2048	512 X 4	90 ns

* An adaptor must be installed into the 24 pin socket on the front panel. MDS monitor software will not program the device. Auxiliary software is needed. (See Section 5.2.)

5.1 3604/3624/3602/3622/3621 PROM

The 3604 and 3624 families are monolithic, high speed, Schottky clamped TTL memory arrays with polycrystalline silicon fuses. They are high density 4096 bit (512 words by 8-bits) PROMs designed for use in limited quantities and when fast turn-around is important.

The PROMs are manufactured with all outputs high. Logic low levels are electrically programmed in selected bit locations by the application of a programming pulse that blows the polysilicon fuse. Each output that is to be changed from high to low (logic 1 to 0) is programmed individually. The programming current (approximately 5 milliamps) is forced into the output to be programmed while the other 7 outputs are allowed to float. A series of pulses are applied, with the pulse width increasing in duration (from 1 µs up to 8 µs) until the fuse is blown. After the fuse is blown, the pulses continue for another 100 µs to insure the complete oxidation of the fuse material. Section 5.2 includes detailed specifications of the signals used to program the PROMs.

The 3604 PROM family programmable with the UPP-864 Personality Card consists of 5 basic types. The 3621 is packaged in a 16 pin dip (dual-in line package). It provides 1024 bits of storage (256 x 4) with 3-state outputs. The access time is 70 ns; a 50 ns version (3621-1) is also available. The 3602 and 3622 are packaged in 16 pin dip and provide 2048 bits storage (512 x 4) with 3-state outputs (3622) or open-collector outputs (3602). The access time is 70 ns; a 90 ns access time is also available. The 3604 and 3624 are packaged in 24 pin dips and provide 4096 bits of storage (1024 x 8) with 3-state outputs (3624) or open-collector outputs (3604). The access time is 90 ns; a 120 ns version is also available.

5.2 FUNCTIONAL DESCRIPTION: UPP-864 PERSONALITY CARD

The UPP-864 Personality Card contains all of the logic needed to either program or read a word (8-bits) of any 3604 or 3624 PROM. The Personality Card operates under the supervision of the Control Board (see Chapter 2). The PROM itself is plugged into the 24-pin socket on the front panel of the PROM Programmer. This socket is wired directly to the Personality Card.

The Control Board is responsible for supplying address and data information, and requesting that the Personality Card perform either a program or a read operation. The Personality Card, in turn, attempts to perform the requested operation, returns data to the Control Board, and notifies the Control Board of the success or failure of the operation.

Figure 5-1 is a functional block diagram of the UPP-864 Personality Card. It may be helpful to frequently refer to this diagram during the following discussion of the Personality Card. The names of the signals that appear in Figure 5-1 generally correspond to the names used on the schematic of the UPP-864 Personality Card (see Appendix B).

Communications between the Personality Card and the Control Board are handled by four parallel buses:

A) The MCS™-40 Bus includes the control, timing and data paths that are necessary for the operation of the 4040 processor on the Control Board and the two 4001 ROMs on the Personality Card.

B) The PROM Address bus provides the Personality Card with the 12-bit PROM address from the Control Board.

C) The PROM Write Data bus from the Control Board provides the 8-bit data word to be programmed into the PROM by the Personality Card.

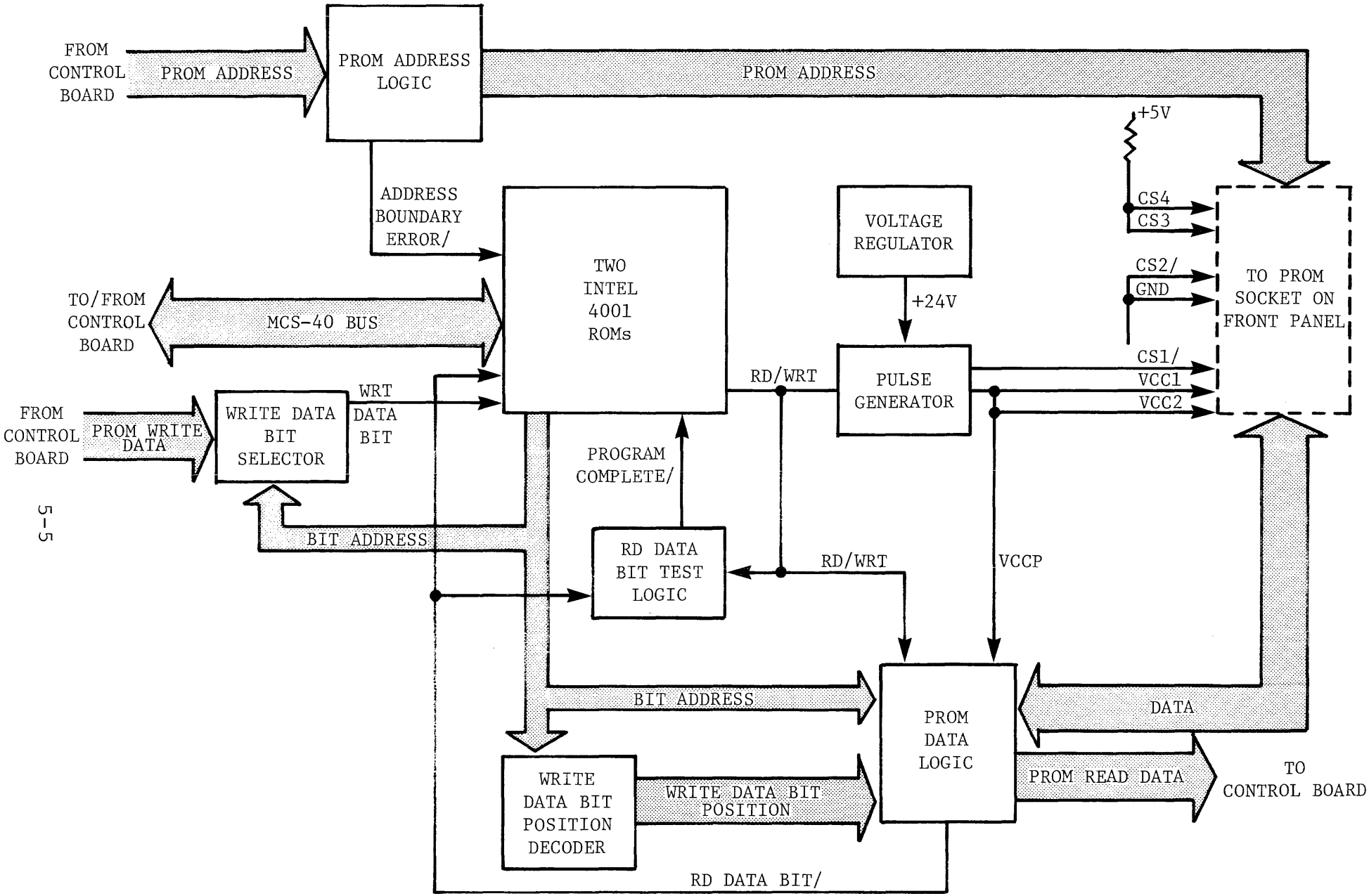


FIGURE 5-1: UPP-864 PERSONALITY CARD FUNCTIONAL BLOCK DIAGRAM

D) The PROM Read Data bus returns the 8-bit data word in the selected PROM location to the Control Board.

There are eight major components of the UPP-864 Personality Card as shown in Figure 5-1:

1) The PROM Address Logic examines the 12-bit PROM Address from the Control Board. Since the 3604 PROM is organized into 512 words, the address must be within the range of 0 to 511 (i.e., the three most significant bits must be zero). If the address is out of this range the logic will signal the address error on the Address Boundary Error/ line. The PROM Address is sent to the PROM through 7407 open-collector drivers.
2) The Two Intel® 4001 ROMs are a part of the MCS™-40 (the processor itself is located on the Control Board). The ROMs contain instructions for the MCS™-40 that will effect the reading or programming of a 3604 PROM. The MCS™-40 interacts with the Personality Card through the I/O ports on the two ROM chips.
3) The Voltage Regulator takes an unregulated +40 volts from the power supply and provides a regulated +24 volts to the Pulse Generator. The +24 volt regulator (a series pass) includes two protection provisions, a current limit and a crow-bar circuit. The current limit is set at 0.6 amp. The crow-bar provides over-voltage protection. If VCCP exceeds 33V, an SCR will fire and ground the +40V through a 5Ω resistor. This causes the 1 amp fuse on the UPP power supply to blow. A hardware error will be indicated if a program operation is attempted and the +40V is not present.

--CAUTION--

It is possible to damage the regulator if the Personality Card is removed when the +40V line is not totally discharged. For this reason, a user must wait 60 seconds after system power is off before removing this Personality Card.

4) The Pulse Generator provides the programming pulses that blow a fuse (thereby programming a bit from 1 to 0) in the PROM. The pulses are delivered to the PROM at CS1/ (pin 85), VCC1 (pin 86), VCC2 (pin 88) and (via the PROM Data Logic) to the output to be programmed. The MCS$^{T.M.}_{-}$40 signals the Pulse Generator to start the programming pulse trains when it switches the RD/WRT line from low to high. When the MCS$^{T.M.}_{-}$40 returns RD/WRT to low the outputs of the Pulse Generator return to levels that allow the PROM to be read: CS1/ goes to 0 volts and VCC goes to +5 volts.

5) The Write Data Bit Selector provides the MCS$^{T.M.}_{-}$40 with one of the eight bits of the PROM Write Data. The bit to be selected is determined by the three-line Bit Address bus from the MCS$^{T.M.}_{-}$40. (Recall that each bit of the 3604 that is to be changed from 1 to 0 must be individually programmed. The MCS$^{T.M.}_{-}$40 uses the Bit Address bus to select each bit of data in turn, and then checks to see if it must be programmed.)

6) The Write Data Bit Position Decoder translates the Bit Address bus into the eight-line Write Data Bit Position bus: the one line (out of the eight) corresponding to the Bit Address is switched from a floating state to an active state. The other seven remain in the floating state.

7) The RD Data Bit Test Logic consists of a 9602 one-shot multivibrator and its associated RC circuits. When RD/WRT is high (a program cycle is in progress) and RD Data Bit/ makes a significant transition from low to high (when the PROM's fuse blows) the one-shot fires, Program Complete/ drops from high to low signalling the MCS$^{T.M.}_{-}$40 that the bit has been programmed.

8) The PROM Data Logic can be in one of two states depending upon RD/WRT. When RD/WRT is low (a read operation) the PROM Data Logic uses Bit Address to select one of the eight data bits from the PROM, and places that bit on RD Data Bit/ in complemented form. Additionally, the

PROM Data Logic will allow the full eight bits of data to be returned to the Control Board over the PROM Read Data bus (again in complemented form). When RD/WRT is high (a program operation) the PROM Data Logic uses the Write Data Bit Position lines and the pulses from the Pulse Generator (VCCP) to force the programming current into the output to be programmed. RD Data Bit/ will reflect the potential at the selected output (inverted); when it switches from low to high, the fuse has blown.

The remainder of this section will describe how these functional blocks interact to perform the two operations: program and read. There are two distinct locations in the ROM on the UPP-864 Personality Card that are the entry points to which the MCS-40™ branches: one entry point for a program operation and one for a read. When the Personality Card receives control it assumes that the PROM Address is available on the address bus. In the case of a program operation it also assumes that the PROM Write Data is on the data bus. In either case the first step is to check for an address error.

The address check is simply a matter of testing the Address Boundary Error/ at the ROM input port. If this signal is true the selected address exceeds 511. If this occurs the Personality Card aborts the operation and returns control to the Control Board. If the address is valid, the operation continues.

PROM READ DATA:

In the case of a read operation there is little left that needs to be done, since the static conditions of the Personality Card present the selected PROM data word to the PROM Data Logic. All the MCS-40™ needs to do is signal the PROM Data Logic (over Bit Address line 2) and the PROM Read Data is returned to the Control Board. The Personality Card has then completed the read operation.

In the case of a 4 bit read operation, the same Personality Card operations occur as in the 8 bit read. That is, the Personality Card reads 8 bits of data. The adaptor card, in this case, generates logic Ø on the upper 4 bits of PROM data and PROM device generates the lower 4 bits of data. As an example, the Personality Card is going to read location 1ØH (Hex) of a 3602 PROM (512 x 4) and location 1ØH contains a 9H (1ØØ1), the Personality Card will send 8 bits of data Ø9H (ØØØØ1ØØ1) to the control card.

NOTE: The UPP-864 Personality Card does not check for the presence of the +40V supply during read operations. If the +40V is not present, however, the data will be invalid.

PROM PROGRAM DATA:

The program operation is somewhat more involved. Since only one bit can be programmed at a time the MCS-40™ has to handle each bit as a separate operation. The Bit Address bus is used to indicate the bit currently being programmed.

The MCS-40™ starts with bit 0 and continues through bit 7 processing them each in turn. For each bit position the MCS-40™ compares the WRT Data Bit to the RD Data Bit/. The outcome of the comparison will indicate one of three possibilities:

- The bit to be programmed and the contents of the PROM are the same. In this case the MCS-40™ simply moves on to the next bit.

- The bit to be programmed is a 1 while the PROM (having been previously programmed) holds a 0. Since a fuse, once blown, cannot be restored, this results in an error: the operation is terminated and control returns to the Control Board.

- The bit to be programmed is a 0 and the PROM holds a 1. In this case the MCS-40™ will program the PROM as described below.

When the MCS™-40 finds a bit that needs to be programmed from a 1 to a 0 it switches the RD/WRT line from low to high. This initiates the series of pulses from the Pulse Generator that will cause the fuse in the selected PROM location to be blown. The amount of time required to actually blow the fuse can vary widely. Typically a fuse will blow within 1 millisecond, but occasionally a fuse may take up to 400 milliseconds. The MCS™-40 is prepared for either eventuality.

The Pulse Generator has two outputs: CS1/ and VCCP. (VCCP supplies VCC1, VCC2 and the PROM Data Logic which, in turn, supplies the pulse to the output to be programmed). Figure 5-2 shows the timing of these signals. Note that the pulses maintain a duty cycle of approximately 50%. The pulse width (t_{pw}) starts at 1 μs and increases linearly over a period of approximately 100 ms to a maximum of 8 μs. The pulse rise and fall times are between 100-300 ns. Chip disable hold time (t_{cd}) is a minimum of 100 ns. The programming current (from the PROM Data Logic) applied to the output being programmed is clamped to VCC by a silicon diode and is limited to 5 mA.

The bit is programmed (i.e., the fuse is blown) when the sensed output of the PROM falls to 0 volts between the programming pulses, as shown in Figure 5-2. When this happens the PROM Data Logic will cause RD Data Bit/ to rise. This, in turn, fires the one-shot multivibrator in the RD Data Bit Test Logic, signalling the MCS™-40 that the bit is programmed.

After the MCS™-40 receives the Program Complete/ signal it maintains the pulse trains for another 100 μs to insure the complete oxidation of the fuse material. The MCS™-40 then switches RD/WRT back to low completing the program cycle for that bit, and allowing the MCS™-40 to move on to the next bit.

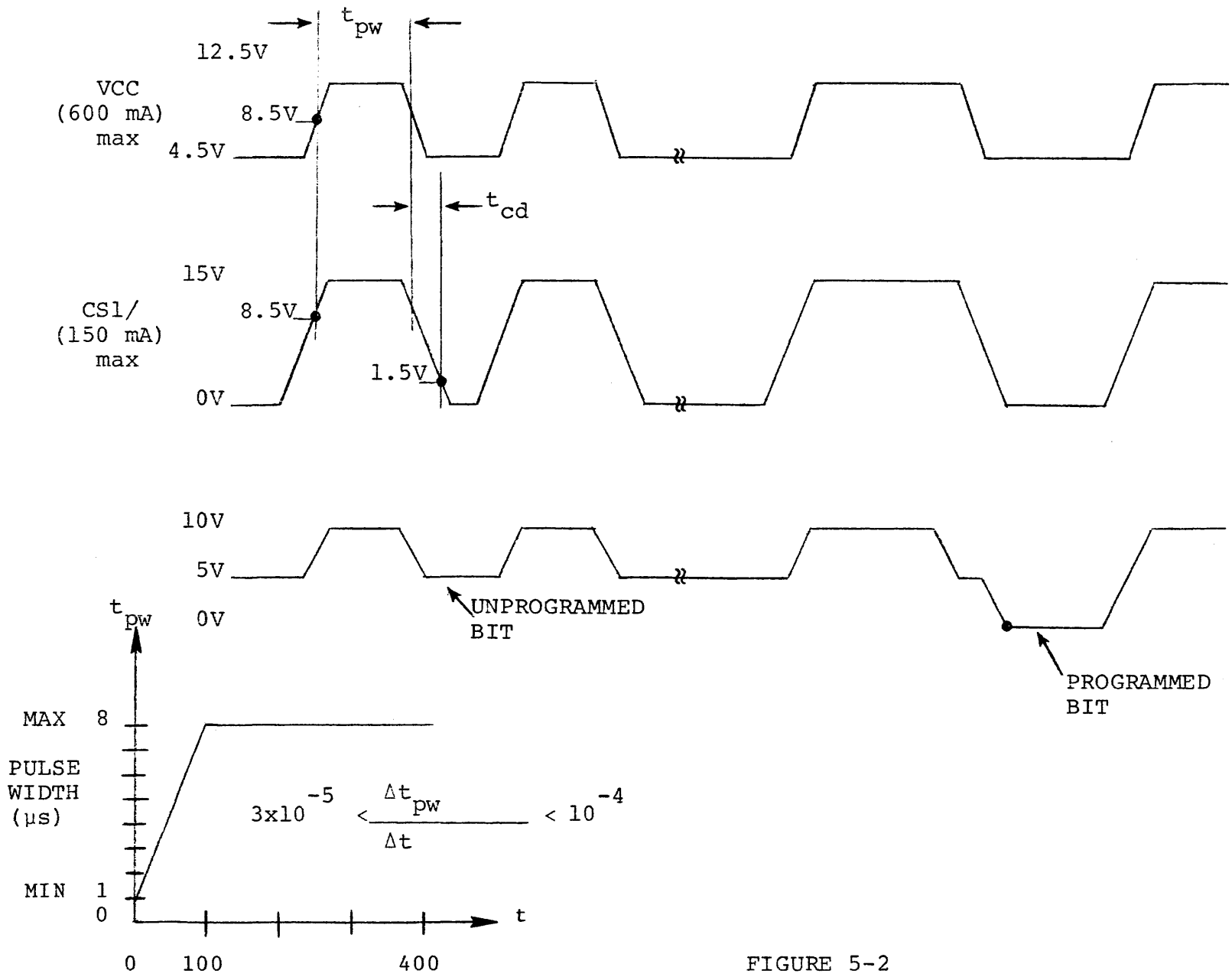

t_{pw}
12.5V
VCC
(600 mA)
max
8.5V
4.5V
t_{cd}
15V
CS1/
(150 mA)
max
8.5V
1.5V
0V
10V
5V
0V
UNPROGRAMMED
BIT
PROGRAMMED
BIT
t_{pw}
MAX 8
PULSE
WIDTH
(μs)
MIN 1
0
$3x10^{-5} < \frac{\Delta t_{pw}}{\Delta t} < 10^{-4}$
t
0
100
400

FIGURE 5-2

If the MCS™-40 does not receive the Program Complete/ signal within 400 ms of the start of the pulse trains it switches RD/WRT back to low anyway. The MCS™-40 pauses for up to 15 ms to allow the timing capacitor in the Pulse Generator to discharge, and then retries the same program cycle. If after eight complete programming cycles the fuse still hasn't blown, control returns to the Control Board with a failure to program error.

In the case of a 4 bit program operation the same operations occur as in the 8 bit program sequence, the Personality Card programs 8 bits of data. Recall in the PROM read data section, that the adapter card forces a logic Ø on the upper 4 bits of the PROM data (as seen by the UPP-864 Personality Card). Therefore, if the PROM data to be programmed is zero's in the upper 4 bits, the UPP-864 Personality Card will "think" that the upper 4 bits are already programmed and will continue to the next operation. The lower 4 bits of data are connected to the PROM so that the Personality Card can program the device. Notice that if the user wanted to program location 1ØH (Hex) of a 3622 with a 5 (0101), the Personality Card input data must be Ø5 (ØØØØ Ø1Ø1). This requirement must be satisfied by the program used by the host computer (e.g., the MDS) to control the UPP. The MDS resident monitor will not automatically mask off the upper 4 bits of a data word before sending it to the UPP, nor will it rotate the upper 4 bits of an 8-bit byte into the proper format for programming. Auxiliary software, such as the Universal PROM Mapper is necessary.

NOTE: A hardware error can be caused by many different things. It can be caused by the failure of logic in the Universal PROM Programmer or it can be caused by failure of the PROM device, itself. For example, a hardware error will be indicated if a programming attempt fails to actually program a bit or if the bit being programmed is not completely fused and instead is in an intermediate state between logical 1 and 0. A hardware error can also be indicated if the PROM data logic or a one-shot in the Universal PROM Programmer is not functioning properly.

5.3 PROGRAMMING PROCEDURE

First, the UPP-864 Personality Card is installed in the UPP. See Chapter 3.1.2 for installation instruction. These instructions are very important as they point out potential mistakes that could be made and provide cautions for the user in order to prevent damage to the PROM and/or the Personality Card.

Now, the user must determine which, if any, adapter is needed. Table 5-2 lists the required adapter requirements. The selected adapter should be installed as follows:

1) Insert the adapter in the 24 pin socket connected to the UPP-864 Personality Card previously installed (see Figure 5-3).

> --CAUTION--
>
> DO NOT insert the adapter in a socket connected to any other Personality Card, as it may damage it.

TABLE 5-2

ADAPTER REQUIRED TO PROGRAM UPP-864 FAMILY PROM

FAMILY	PINS	MARKING ON ADAPTER	NUMBER
3621	16	Adapter I	UPP 562*
3602	16	Adapter I	UPP 562*
3622	16	Adapter I	UPP 562*
3604	24	None Used	-
3624	24	None Used	-

*Out of address range error will not be detected.

2) Insert the adapter such that the lever on the adapter is on top (see Figure 5-3).

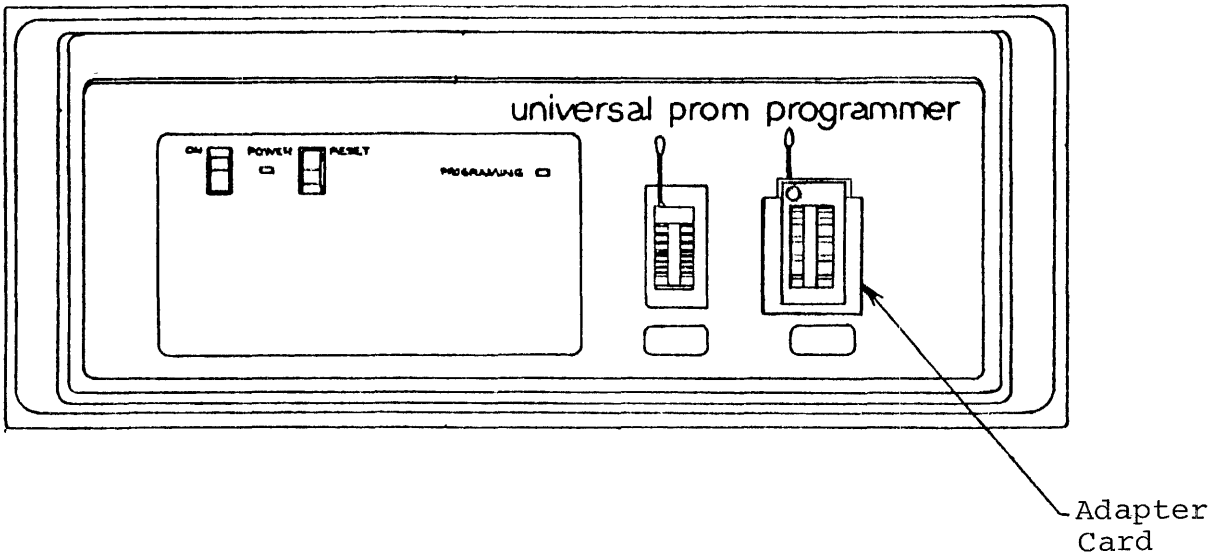


FIGURE 5-3

FRONT VIEW OF UPP WITH ADAPTER

The final step is to load appropriate software, if 3604 or 3624 type PROMs are to be programmed, standard MDS monitor software will perform the necessary operations. 4 bit members of the 3604 PROM family require auxiliary software to perform the data packing as described in Section 5.2.

5.4 PIN LIST: UPP-864 PERSONALITY CARD

The UPP-864 Personality Card communicates with the Control Board and the PROM socket on the front panel through a 100-pin double-sided PC edge connector. Pin allocations and designated signal functions for this 100-pin connector are given in Table 5-3.

TABLE 5-3
UPP-864 PERSONALITY CARD PIN LIST

PIN	MNEMONIC	FUNCTION	SOURCE*	DESTINATION*
1	GND	Ground		
2	GND			
3				
4				
5	VCCH	Power inputs (5.85V)		
6	VCCH			
7	VCCH			
8	VCCH			
9	GND	Ground		
10	GND			
11	-10VDC	Power inputs		
12	-10VDC		PS	PC
13	GND	Ground		
14	GND			
15				
16	BD SENSE/	BOARD SENSE	PC	CB
17			PS	PC
18				
19	CONTROL	Control bit		
20				
21	WRITE DATA 0	Write data bus from Control Board	CB	PC
22	WRITE DATA 1			
23	WRITE DATA 2			
24	WRITE DATA 3			
25	WRITE DATA 4			
26	WRITE DATA 5			
27	WRITE DATA 6			
28	WRITE DATA 7			
29	PROM ADDRESS 0	PROM address bus from Control Board	CB	PC
30	PROM ADDRESS 1			
31	PROM ADDRESS 2			
32	PROM ADDRESS 3			
33	PROM ADDRESS 4			
34	PROM ADDRESS 5			
35	PROM ADDRESS 6			
36	PROM ADDRESS 7			
37	PROM ADDRESS 8			
38	PROM ADDRESS 9			
39	PROM ADDRESS 10			
40	PROM ADDRESS 11			
41	D0	MCS-40™ data bus (bi-directional)	CB/PC	PC/CB
42	D1			
43	D2			
44	D3			
45	Φ2	MCS-40™ clock (bi-directional)	CB	PC
46	Φ1			
47	CM-ROM	ROM bank enable	CB	PC
48				
49				
50	SYNC	MCS-40™ synchronization		

*PS = Power Supply CB = Control Board PC = UPP-864 Personality Card
FP = Front Panel (PROM socket)

TABLE 5-3 (Continued)

PIN	MNEMONIC	FUNCTION	SOURCE*	DESTINATION*
51	RESET/	MCS-40™ Reset	CB	PC
52	PROM RD DATA 0/	Data read from PROM	PC	CB
53	PROM RD DATA 1/			
54	PROM RD DATA 2/			
55	PROM RD DATA 3/			
56	PROM RD DATA 4/			
57	PROM RD DATA 5/			
58	PROM RD DATA 6/			
59	PROM RD DATA 7/			
60				
61	A7	PROM address	PC	FP
62	A6			
63	A5			
64	A4			
65	A3			
66	A2			
67	A1			
68	A0			
69	D0	PROM data (bi-directional)	PC/FP	FP/PC
70	D1			
71	D2			
72	GND	Ground		
73				
74				
75				
76				
77	D3	PROM data (bi-directional)	PC/FP	FP/PC
78	D4			
79	D5			
80	D6			
81	D7			
82	CS4	Power to PROM	PC	FP
83	CS3			
84	CS2/			
85	CS1/			
86	VCC2			
87	A8	PROM address	PC	FP
88	VCC1	Power to PROM	PC	FP
89				
90				
91	GND	Ground		
92	GND			
93				
94				
95	+40V	Power inputs	PS	PC
96	+40V			
97				
98				
99	GND	Ground		
100	GND			

* PS = Power Supply CB = Control Board PC = UPP-864 Personality Card
FP = Front Panel (PROM socket)

CHAPTER 6

THE UPP-361 PERSONALITY CARD

The UPP-361 Personality Card contains the logic that is needed to both program and read the contents of a 3601 PROM location. The 3601 PROM is organized as 256 4-bit words. Section 6-1 discusses 3601 family specifications and Table 6-1 lists PROMS that may be programmed by this card.

Section 6.2 discusses the major components of the UPP-361 Personality Card. It also discusses the sequence and the timing of events for both the read and the program operations.

Section 6.3 provides a pin list for the UPP-361 Personality Card. This list includes the allocation and the function of each of the signals that appear on the pins of the Personality Card edge connector.

TABLE 6-1

UPP-361 PERSONALITY CARD DEVICE SELECTION

PROM	PINS	NUMBER OF BITS	ORGANIZATION	ACCESS TIME
3601	16	1024	256 X 4	70 ns
3601-1	16	1024	256 X 4	50 ns
M3601	16	1024	256 X 4	90 ns

6.1 3601 PROM

The 3601 and 3601-1 are high speed PROMs organized as 256 4-bit words. The only distinction between the 3601 and the 3601-1 is their access times: for the 3601 it is 70 nanoseconds; for the 3601-1 it is 50 nanoseconds. The M3601 is the military temperature (-55 to +125^{o}C) version of the 3601 family with an access time of 90 nsec. (Unless otherwise indicated, all references to the 3601 apply also to the 3601-1 and M3601). The PROMs are manufactured with the highly reliable polycrystalline silicon fuse and the fast switching Schottky barrier diode technology. They are designed for use in limited quantities and when fast turn-around is important. They are packaged in a standard 16-pin dual in-line lead configuration.

The 3601 PROM is manufactured with all outputs low (0). Logic high (1) output levels can be electrically programmed in selected bit locations by the application of a programming pulse that blows the polysilicon fuse. Each output that is to be changed from low to high (logic 0 to 1) is programmed individually. The programming current (approximately 5 milliamps) is forced into the output to be programmed while the other three outputs are grounded. A series of pulses are applied, with the pulse width increasing in duration (from 1 μs up to 8 μs) until the fuse is blown. After the fuse is blown, the pulses are continued for another 100 μs to insure the complete oxidation of the fuse material. Section 6.2 includes detailed specifications for the signals used to program the PROMs.

6.2 FUNCTIONAL DESCRIPTION: UPP-361 PERSONALITY CARD

The UPP-361 Personality Card contains all of the logic needed to either program or read a word (4-bits) of a 3601 PROM. The Personality Card operates under the supervision of the Control Board (see Chapter 2). The PROM itself is plugged into the 16-pin socket on the front panel of the PROM Programmer. This socket is wired directly to the Personality Card.

The Control Board is responsible for supplying address and data information, and requesting that the Personality Card perform either a program or a read operation. The Personality Card, in turn, attempts to perform the requested operation, returns data to the Control Board, and notifies the Control Board of the success or failure of the operation.

Figure 6-1 is a functional block diagram of the UPP-361 Personality Card. It may be helpful to frequently refer to this diagram during the following discussion of the Personality Card. The names of the signals that appear in Figure 6-1 generally correspond to the names used on the schematic of the UPP-361 Personality Card (see Appendix B).

Communications between the Personality Card and the Control Board are handled by four parallel buses:

A) The MCS™-40 Bus includes the control, timing, and data paths that are necessary for the operation of the 4040 processor on the Control Board and the two 4001 ROMs on the Personality Card.
B) The PROM Address bus provides the Personality Card with the 12-bit PROM address from the Control Board.
C) The PROM Write Data bus from the Control Board provides the 4-bit data word to be programmed into the PROM by the Personality Card.
D) The PROM Read Data bus returns the 4-bit data word read from the selected PROM location to the Control Board.

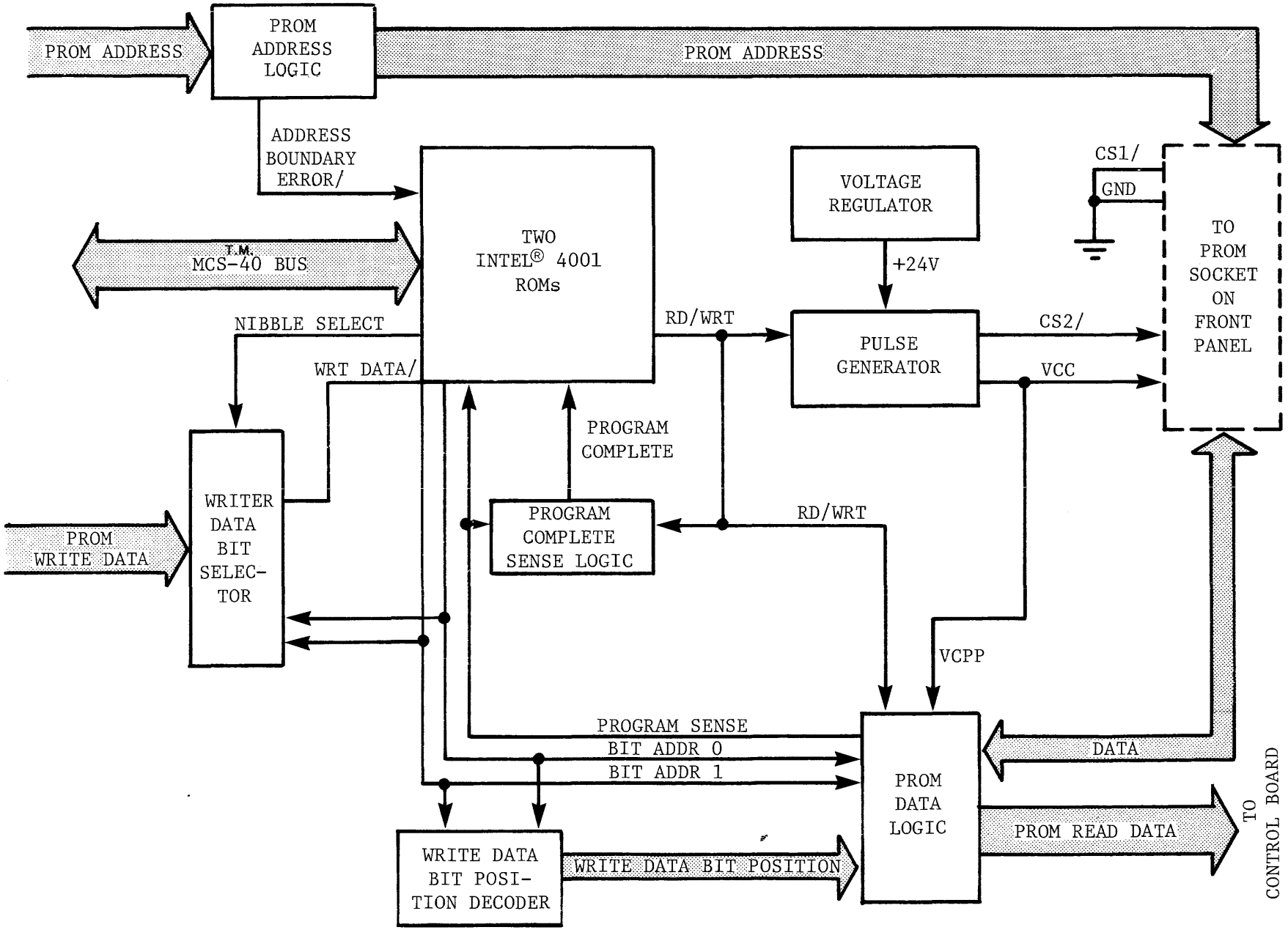


FIGURE 6-1: UPP-361 PERSONALITY CARD FUNCTIONAL DIAGRAM

There are eight major components of the UPP-361 Personality Card in Figure 6-1:

1) The PROM Address Logic examines the 12-bit PROM Address from the Control Board. Since the 3601 PROM is organized into 256 words, the address must be within the range of 0 to 255 (i.e., the four most significant bits must be zero). If the address is out of this range the logic will signal the address error on the Address Boundary Error/ line. The PROM Address is sent to the PROM through 7407 open-collector drivers.
2) The Two Intel® 4001 ROMs are a part of the MCS™-40 (the processor itself is located on the Control Board). The ROMs contain instructions for the MCS™-40 that will effect the reading or programming of a 3601 PROM. The MCS™-40 interacts with the Personality Card through the I/O ports on the two ROM chips.
3) The Voltage Regulator takes an unregulated +40 volts from the power supply and provides a regulated +24 volts to the Pulse Generator. The +24 Volt regulator (a series pass) includes two protection provisions, a current limit and a crow-bar circuit. The current limit is set at 0.6 amp. The crow-bar provides over-voltage protection. If VCCR exceeds 33V, an SCR will fire and ground the +40V through a 5Ω resistor. This causes the 1 amp fuse on the VPP power supply to blow. A hardware error will be indicated if a program operation is attempted and the +40V is not present.
4) The Pulse Generator provides the programming pulses that blow a fuse (thereby programming a bit from 0 to 1) in the PROM. The pulses are delivered to the PROM at CS2/ (pin 86), VCC (pin 88) and (via the PROM Data Logic) to the output to be programmed. The MCS™-40 signals the Pulse Generator to start the programming

pulse trains when it switches the RD/WRT line from low to high. When the MCS™-40 returns RD/WRT to low the outputs of the Pulse Generator return to levels that allow the PROM to be read: CS2/ goes to 0 volts and VCC goes to +5 volts.

5) The Write Data Bit Selector provides the MCS™-40 with one bit of data at a time via the WRT Data/ line. The bit that is selected depends upon the three inputs to the Selector: Nibble Select, Bit Addr 0, and Bit Addr 1. Nibble Select determines whether the most significant nibble or the least significant nibble of the 8-bit PROM Write Data bus will be used. If Nibble Select is high the most significant nibble (bits 4-7) is used. Bit Addr 0 and Bit Addr 1 are, in turn, used to select each of the four bits of the nibble.

6) The Write Data Bit Position Decoder translates Bit Addr 0 and Bit Addr 1 into the four-line Write Data Bit Position bus: the one line (out of the four) corresponding to the Bit Address is switched from low to high. The other three remain grounded.

7) The Program Complete Sense Logic consists of a 9602 one-shot multivibrator and its associated RC circuits. When RD/WRT is high (a program cycle is in progress) and Program Sense makes a significant transition from low to high the one-shot is re-triggered. The Program Sense signal remains low after the PROM's fuse blows. When the one-shot times out, 100 μsecs later (over programming time), the Program Complete signal goes low, informing the MCS™-40 that the bit has been programmed.

8) The PROM Data Logic can be in one of two states depending upon RD/WRT. When RD/WRT is low (a read operation) the PROM Data Logic uses Bit Addr 0 and Bit Addr 1 to select one of the four data bits from the PROM, and places that bit on Program Sense. Additionally the PROM Data Logic will allow the full four bits of data to be returned to the Control Board over the PROM Read Data bus (in

complemented form). When RD/WRT is high (a program operation) the PROM Data Logic uses the Write Data Bit Position lines and the pulses from the Pulse Generator (VCCP) to force the programming current into the output to be programmed. Program Sense will reflect the status of the selected output, when it remains low for more than 100 μsec. It indicates that the PROM's fuse has blown.

The remainder of this section will describe how these functional blocks interact to perform the two operations: program and read. There are three distinct locations in the ROM on the UPP-361 Personality Card that are the entry points to which the MCS™-40 branches: one entry point for a read operation, one for a program using the high order nibble data, and one for a program using the low order nibble data. When the Personality Card receives control it assumes that the PROM Address is available on the address bus. In the case of a program operation it also assumes that the PROM Write Data is on the data bus. In either case the first step is to check for an address error.

The address check is simply a matter of testing the Address Boundary Error/ at the ROM input port. If this signal is true the selected address exceeds 255. If this occurs the Personality Card aborts the operation and returns control to the Control Board. If the address is valid, the operation continues.

PROM READ DATA:
In the case of a read operation there is little left that needs to be done, since the static conditions of the Personality Card present the selected PROM data word to the PROM Data Logic. All the MCS™-40 needs to do is signal the PROM Data Logic to enable the PROM Read Data. Since the PROM has only four bits of data, the PROM Data Logic duplicates the four bits, placing them in both the upper and lower nibble of the 8-bit PROM Read Data bus. When this is done the PROM Read Data is returned to the Control Board. The Personality Card has then completed the read operation.

PROM PROGRAM DATA:

The program operation is somewhat more involved. Since only one bit can be programmed at a time the MCS$^{T.M}$-40 has to handle each bit as a separate operation. Bit Addr 0 and Bit Addr 1 are used to indicate the bit currently being programmed.

The MCS$^{T.M}$-40 starts with bit 0 of the selected nibble and continues through bit 3, processing them each in turn. For each bit position the MCS$^{T.M}$-40 compares the WRT Data/ bit to the Program Sense Bit. The outcome of the comparison will indicate one of three possibilities:

- The bit to be programmed and the contents of the PROM are the same. In this case the MCS$^{T.M}$-40 simply moves on to the next bit.

- The bit to be programmed is a 0 while the PROM (having been previously programmed) holds a 1. Since a fuse, once blown, cannot be restored, this results in an error: the operation is terminated and control returns to the Control Board.

- The bit to be programmed is a 1 and the PROM holds a 0. In this case the MCS$^{T.M}$-40 will program the PROM as described below.

When the MCS$^{T.M}$-40 finds a bit that needs to be programmed from a 0 to a 1 it switches the RD/WRT line from low to high. This initiates the series of pulses from the Pulse Generator that will cause the fuse in the selected PROM location to be blown. The amount of time required to actually blow the fuse can vary widely. Typically a fuse will blow within 1 millisecond, but occasionally a fuse may take up to 400 milliseconds. The MCS$^{T.M}$-40 is prepared for either eventuality.

The Pulse Generator has two outputs: CS2/ and VCC. (VCC supplies VCCP to the PROM Data Logic which, in turn, supplies the pulse to the output to be programmed.) Figure 6-2 shows the timing of these signals. Note that the pulses maintain a duty cycle of approximately 50%. The pulse width (t_{pw}) starts at 1 µs and increases linearly over a period of approximately 100 ms to a maximum of 8 µs. The pulse rise and fall times are between 100-300 ns. Chip disable hold time (t_{cd}) is a minimum of 100 ns. The programming current (from the PROM Data Logic) applied to the output being programmed is connected to VCC through a 300 ohm resistor. This will force the proper programming current (3 - 6 mA) into the output when VCC is raised to 10 V.

The bit is programmed (i.e., the fuse is blown) when the sensed output of the PROM no longer falls to 0 volts between the programming pulses, as shown in Figure 6-2. When this happens, the PROM Data Logic will cause Program Sense to remain low. This, in turn, prevents the one-shot multivibrator from being subsequently re-triggered. When this one-shot times out (100 µsecs later), the Program Complete Sense logic signals the MCS$^{T.M.}$40 that the bit has been programmed.

The MCS$^{T.M.}$40 then switches RD/WRT back to low completing the program cycle for that bit, and allowing the MCS$^{T.M.}$40 to move on to the next bit.

If the MCS$^{T.M.}$40 does not receive the Program Complete signal within 400 ms of the start of the pulse trains it switches RD/WRT back to low anyway. The MCS$^{T.M.}$40 pauses for up to 4 ms to allow the timing capacitor in the Pulse Generator to discharge, and then retries the same program cycle. If after eight complete programming cycles the fuse still hasn't blown control returns to the Control Board with a failure to program error.

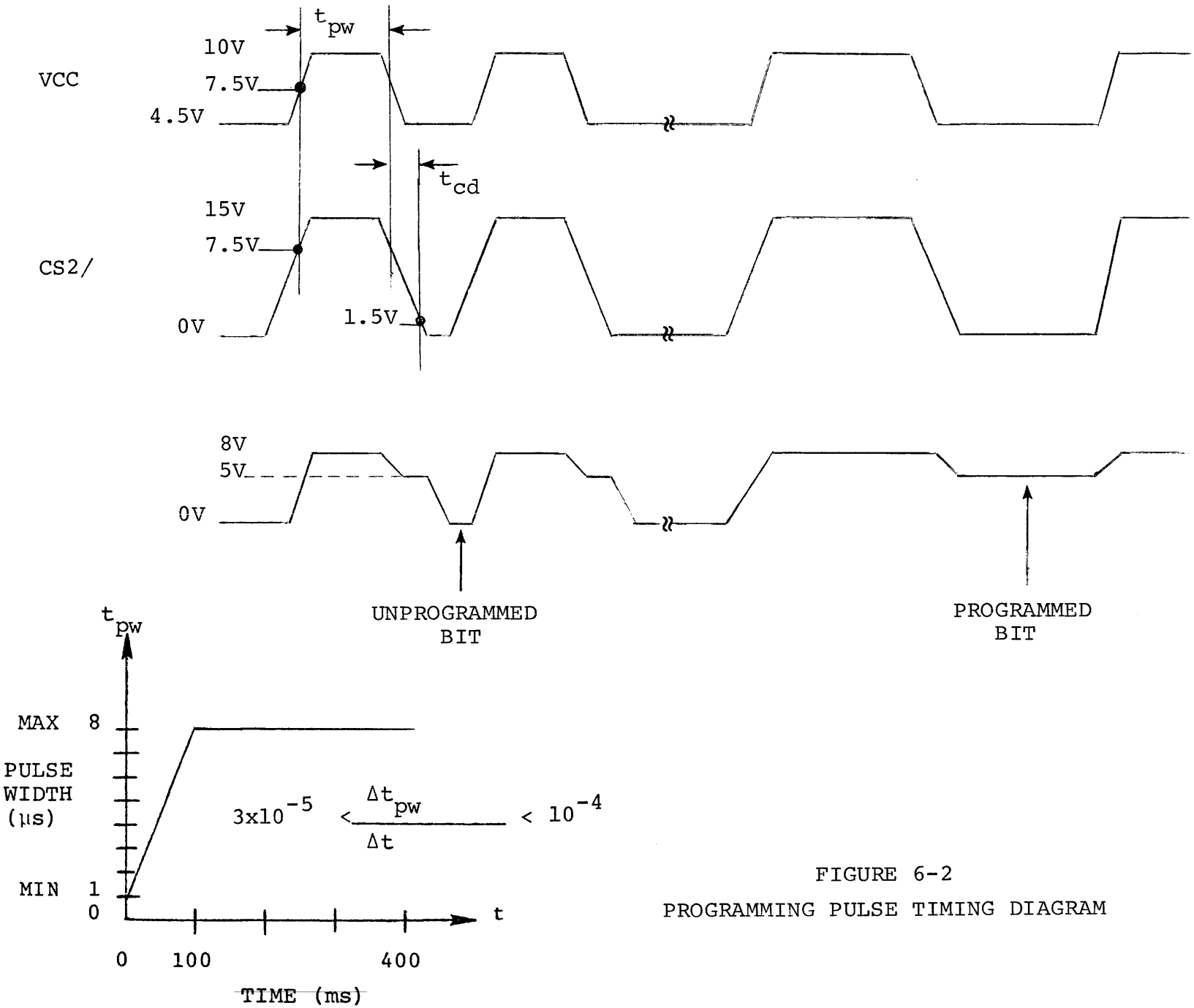


FIGURE 6-2

PROGRAMMING PULSE TIMING DIAGRAM

NOTE: A hardware error can be caused by many different things. It can be caused by the failure of logic in the Universal PROM Programmer or it can be caused by failure of the PROM device, itself. For example, a hardware error will be indicated if a programming attempt fails to actually program a bit or if the bit being programmed is not completely fused and instead is in an intermediate state between logical 1 and 0. A hardware error can also be indicated if the PROM data logic or a one-shot in the Universal PROM Programmer is not functioning properly.

6.3 PIN LIST: UPP-361 PERSONALITY CARD

The UPP-361 Personality Card communicates with the Control Board and the PROM socket on the front panel through a 100-pin double-sided PC edge connector. Pin allocations and designated signal functions for this 100-pin connector are given in Table 6-2.

TABLE 6-2.

UPP-361 PERSONALITY CARD PIN LIST

PIN	MNEMONIC	FUNCTION	SOURCE*	DESTINATION*
1	GND	Ground		
2	GND			
3				
4				
5	VCCH	Power inputs (5.85 VDC)	PS	PC
6	VCCH			
7	VCCH			
8	VCCH			
9	GND	Ground	PS	PC
10	GND			
11	-10	Power inputs		
12	-10			
13	GND	Ground		
14	GND			
15				
16	BD SEN/	Board Sense	PC	CB
17				
18				
19				
20				
21	WRITE DATA 0	Write data bus from Control Board	CB	PC
22	WRITE DATA 1			
23	WRITE DATA 2			
24	WRITE DATA 3			
25	WRITE DATA 4			
26	WRITE DATA 5			
27	WRITE DATA 6			
28	WRITE DATA 7			
29	PROM ADDRESS 0	PROM address bus from Control Board	CB	PC
30	PROM ADDRESS 1			
31	PROM ADDRESS 2			
32	PROM ADDRESS 3			
33	PROM ADDRESS 4			
34	PROM ADDRESS 5			
35	PROM ADDRESS 6			
36	PROM ADDRESS 7			
37	PROM ADDRESS 8			
38	PROM ADDRESS 9			
39	PROM ADDRESS 10			
40	PROM ADDRESS 11			
41	D0	MCS-40™ data bus (bi-directional)	CB/PC	PC/CB
42	D1			
43	D2			
44	D3			
45	Φ2	MCS-40™ clock signals	CB	PC
46	Φ1			
47	CM-ROM	ROM bank enable	CB	PC
48				
49				
50	SYNC	MCS-40™ synchronization	CB	PC

*PS = Power supply CB = Control Board PC = UPP-361 Personality Card
FP = Front Panel (PROM socket)

TABLE 6-2. (Continued)

PIN	MNEMONIC	FUNCTION	SOURCE*	DESTINATION*
51	RESET/	MCS™-40 Reset	CB	PC
52	PROM RD DATA 0/	Data read from PROM	PC	CB
53	PROM RD DATA 1/			
54	PROM RD DATA 2/			
55	PROM RD DATA 3/			
56	PROM RD DATA 4/			
57	PROM RD DATA 5/			
58	PROM RD DATA 6/			
59	PROM RD DATA 7/			
60				
61	A6	Address to PROM	PC	FP
62	A5			
63	A4			
64	A3			
65	A0			
66	A1			
67	A2			
68	GND	Ground		
69				
70				
71				
72				
73				
74				
75				
76				
77				
78				
79				
80				
81	D3	PROM Data (bi-directional)	PC/FP	FP/PC
82	D2			
83	D1			
84	D0			
85	CS1/	Power to PROM	PC	FP
86	CS2/			
87	A7	Address to PROM	PC	FP
88	VCC	Power to PROM		
89				
90				
91				
92				
93				
94				
95	+40V	Power inputs	PS	PC
96	+40V			
97				
98				
99				
100				

*PS = Power Supply CB = Control Board PC = UPP-361 Personality Card
FP = Front Panel (PROM socket)

Chapter 7

THE UPP-872 PERSONALITY CARD

The UPP-872 Personality Card contains the logic that is needed to both program and read the contents of a 1702A PROM location. The 1702A is an erasable PROM and is organized as a 256 word by 8-bit memory. Access time for the 1702A PROM is 1 μs. Listed in table 7-1 are several versions of the 1702A PROM that may be programmed by this card. Detailed specifications for the 1702A and other compatible Intel® PROMs are contained in Section 7.1.

Section 7.2 discusses the major components of the UPP-872 Personality Card. It also discusses the sequence and the timing of events for both the read and the program operations.

Section 7.3 provides a pin list for the UPP-872 Personality Card. This list includes the allocation and the function of each of the signals that appear on the pins of the personality card edge connector.

TABLE 7-1

UPP-872 PERSONALITY CARD DEVICE SELECTION

PROM	PINS	NUMBER OF BITS	ORGANIZATION	ACCESS TIME
1602A	24	2048	256 x 8	1.0 µs
1702A	24	2048	256 X 8	1.0 µs
1702A-2	24	2048	256 x 8	0.65 µs
1702A-6	24	2048	256 x 8	1.5 µs
1702AL	24	2048	256 x 8	1.0 µs
1702AL-2	24	2048	256 x 8	0.65 µs
4702A	24	2048	256 x 8	1.7 µs
8702A-4	24	2048	256 x 8	2.3 µs
8702A	24	2048	256 x 8	1.3 µs

7.1 1702A/1602A PROM

The 1702A is a 256 word by 8-bit electrically programmable read only memory, designed for use in limited quantities, when fast turn-around and pattern experimentation are important. The PROM Programmer can program all 256 words of the PROM in approximately two minutes. The 1702A can be erased by controlled exposure to high intensity ultraviolet light. After it is cleared, the 1702A can be reprogrammed by the PROM Programmer. The 1702A may be erased and reprogrammed as often as desired.

The 1702A is shipped to the customer in a cleared condition; that is, with zeros (output low) in all memory locations. During programming, ones (output high) are loaded selectively into the chip's memory locations. All eight bits of one word are programmed simultaneously by setting the desired bit pattern on the eight data terminals of the 1702A. The address of the word to be programmed is placed on the eight address terminals of the 1702A. The selected memory location is then programmed by a carefully controlled sequence of pulsed signals applied to the chip's pins. Section 7.2 includes detailed specifications of the signals used to program the 1702A.

The 1702A is packaged in a 24 pin dual in-line package with a transparent quartz lid. A silicon die is located under the transparent lid. Erasure of the PROM is accomplished by exposing the silicon die to ultraviolet light at a wavelength of 2537 Angstroms. The recommended integrated dose (the product of intensity and exposure time) is 6 W-sec/cm^2. Examples of ultraviolet sources which can be used are the Model UVS-54 and the Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc., (4115 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. Ten to twenty minutes exposure to the lamp, at a distance of one inch, will clear the PROM completely. Avoid unneccessary or prolonged exposures, which are potentially damaging to the PROM.

--WARNING--

High intensity ultraviolet light can cause serious burns. Ultraviolet radiation can also generate potentially hazardous amounts of ozone. Observe the following precautions when using an ultraviolet source to erase a PROM:

1) Never expose skin or eyes to the source directly.
2) Do not stare at an object which is under ultraviolet illumination. The light is invisible, but is nevertheless injurious to eye tissue.
3) Use the source only in a well-ventilated area.

The 1702A PROM is available in a non-erasable version: the 1602A. The 1602A is packaged with a metal lid (instead of a transparent quartz lid). The metal lid effectively prevents exposure of the PROM's silicon die to ultraviolet light, thereby making the 1602A non-erasable. The 1602A is otherwise identical to the 1702A and may, therefore, be programmed by the PROM Programmer using the UPP-872 Personality Card. Whenever we refer to the 1702A PROM, the same applies to the 1602A PROM, unless otherwise noted.

--WARNING--

Caution must be taken to insert the PROM in the front panel socket correctly (pin 1 in the upper left side). Damage to the PROM and/or personality card is possible if a program attempt is made when the PROM is inserted upside down.

7.2 FUNCTIONAL DESCRIPTION: UPP-872 PERSONALITY CARD

The UPP-872 Personality Card contains all of the logic needed to either program or read a word (8-bits) on a 1702A PROM. The Personality Card operates under the supervision of the Control Board (see Chapter 2). The PROM itself is plugged into the 24-pin socket on the front panel of the PROM Programmer. This socket is wired directly to the Personality Card.

The Control Board is responsible for supplying address and data information, and requesting that the Personality Card perform either a program or a read operation. The Personality Card, in turn, attempts to perform the requested operation, returns data to the Control Board, and notifies the Control Board of the success or failure of the operation.

Figure 7-1 is a functional block diagram of the UPP-872 Personality Card. It may be helpful to frequently refer to this diagram during the following discussion of the Personality Card. The names of the signals that appear in Figure 7-1 generally correspond to the names used on the schematic of the UPP-872 Personality Card (see Appendix B).

Communications between the Personality Card and the Control Board are handled by four parallel buses:

A) The MCS™-40 Bus includes the control, timing, and data paths that are necessary for the operation of the 4040 processor on the Control Board and the two 4001 ROMs on the Personality Card.
B) The PROM Address bus provides the Personality Card with the 12-bit PROM address from the Control Board.
C) The PROM Write Data bus from the Control Board provides the 8-bit data word to be programmed into the PROM by the Personality Card.
D) The PROM Read Data bus returns the 8-bit data word read from the selected PROM location to the Control Board.

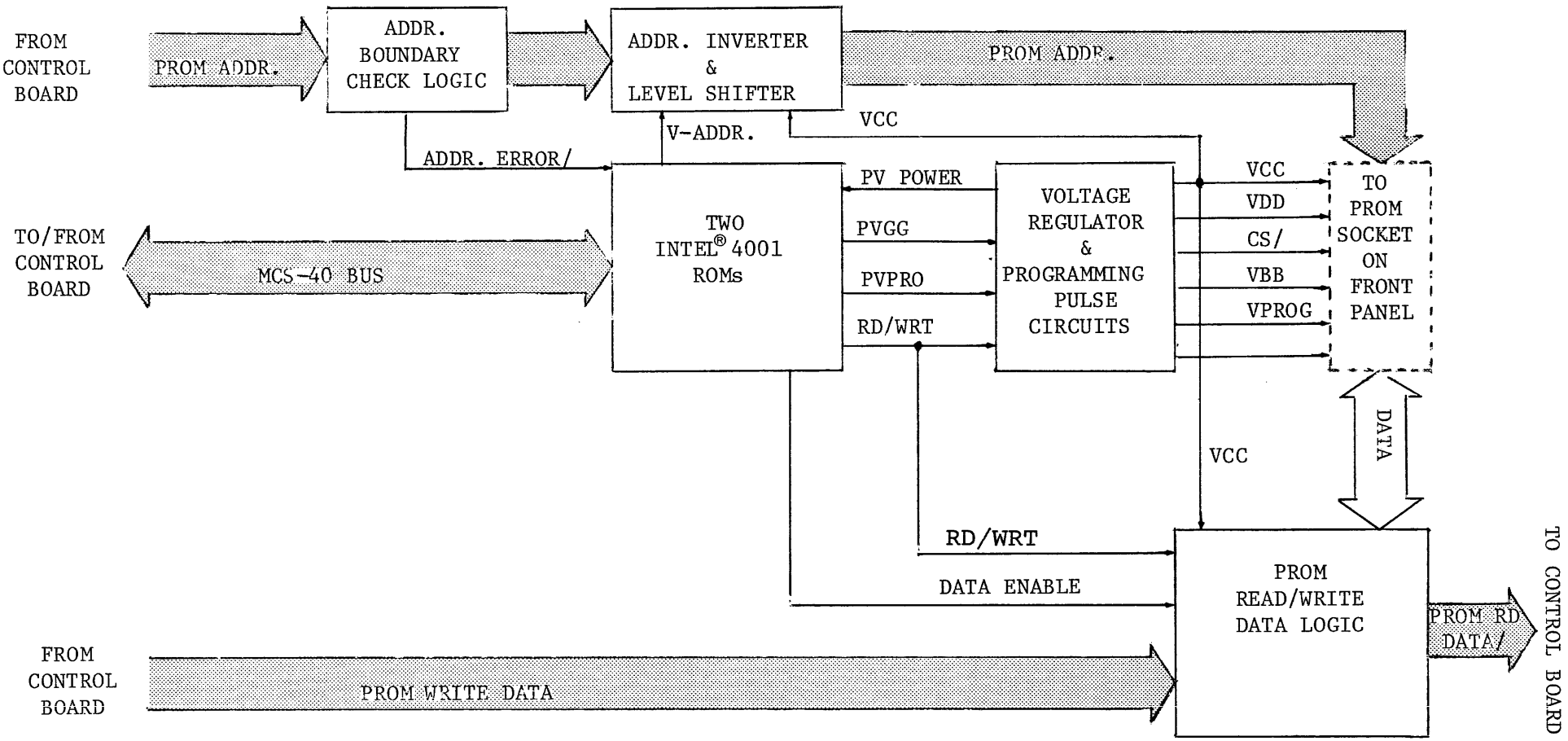


FIGURE 7-1

UPP-872 PERSONALITY CARD BLOCK DIAGRAM

There are five major components of the UPP-872 Personality Card shown in Figure 7-1:

1) The Address Boundary Check Logic examines the 12-bit PROM Address from the Control Board. Since the 1702A PROM is organized into 256 words, the address must be within the range of 0 to 255 (i.e., the four most significant bits must be zero). If the address is out of this range the logic will signal the address error at port 9, bit 1, of a 4001 ROM (A14).
2) The Address Inverter and Level Shifter receives the PROM Address from the Address Boundary Check Logic and transforms it into the type of signal required at the address pins of the PROM. The input V-Address determines whether the address is inverted (complemented) or not. The input VCC determines the voltage level of the PROM address.
3) The Two Intel® 4001 ROMs are a part of the MCS™-40 (the processor itself is located on the Control Board). The ROMs contain instructions for the MCS™-40 that will effect the reading or programming of a 1702A PROM. The MCS™-40 interacts with the Personality Card through the I/O ports on the two ROM chips.
4) The Voltage Regulator and Programming Pulse Circuits develop the pulses that are required to program the PROM. These circuits receive commands from the ROM I/O ports and supply the appropriate voltages to the PROM. The major source of power for the UPP-872 Personality Card is the VCCP power line. In the read mode, VCCP = 5 VDC, which is generated from VCCH through a dropping diode. In the program mode, VCCP = 48 VDC. There are two protection provisions in the program mode. One is a current limit which is set at approximately 700 mA. The other is a crow-bar which will fire if VCCP is greater than 56 VDC. If the crow-bar fires, the +70 VDC power is grounded through a 5Ω, 5 watt resistor which will cause the 1 Amp fuse, associated with the +70 VDC, to blow. The Personality Card will return a hardware error if a program operation is attempted & the +70 VDC is not present.

CAUTION - It is possible to damage the regulator if the Personality Card is removed when the +70 volt line is not totally discharged. For this reason, a user must wait 60 seconds after system power is off before removing this Personality Card.

5) The PROM Read/Write Data Logic performs one of two functions. During a program operation it accepts data from the PROM Write Data bus, and supplies it to the PROM at the appropriate voltage level. During a read operation it accepts data from the PROM and, if Data Enable is true, it returns the data to the Control Board.

The remainder of this section will describe how these functional blocks interact to perform the two operations: program and read. There are two distinct locations in the ROM on the UPP-872 Personality Card that are the entry points to which the MCS™-40 branches: one entry point for a program operation and one for a read. When the Personality Card receives control it assumes that the PROM Address is available on the address bus. In the case of a program operation it also assumes that the PROM Write Data is on the data bus. In either case the first step is to check for an address error.

The address check is simply a matter of testing the Address Error at the ROM input port. If this signal is true the selected address exceeds 255. If this occurs the Personality Card aborts the operation and returns control to the Control Board. If the address is valid, the operation continues.

PROM READ DATA:
In the case of a read operation there is little left that needs to be done, since the static conditions of the Personality Card present the selected PROM data word to the PROM Read/Write Data Logic. All the MCS™-40 needs to do is turn on the Data Enable line from the 4001 ROM (A14) output port 9, bit 3. When this is done the PROM

Read Data is returned to the Control Board. The Personality Card has then completed the read operation. Program control, then returns to the Control Board.

PROM PROGRAM DATA:

The Program operation is a bit more involved. After the address has been checked, the program operation begins. The sequence of events is as follows:

1) The MCS™-40 checks to see that the Voltage Regulator is receiving +70 volts from the Power Supply. If the signal PV Power from the Voltage Regulator to ROM (A14) port 9, bit 2 is true, then the +70 volts is available. If not, the program operation is aborted, and control returned to the Control Board. (Hardware Error)
2) The signal RD/WRT is switched from low (which indicates read) to high (indicating program). This transition causes the following:
    a) All six Voltage Regulator outputs are changed as shown in Figure 7-2.
    b) The PROM Read/Write Data Logic inverts the Write Data and presents it to the PROM as shown in Figure 7-2.
3) The signal V-Address is switched from low to high. This causes the Address Inverter to complement each address bit. The complemented address is presented to the PROM as shown in Figure 7-2.
4) Approximately 110 μs later, PVGG is switched from low to high. This causes VDD (pin 88) and VGG (pin 80) to drop as shown in Figure 7-2.
5) Approximately 72 μs after that, V-Address is switched back to low causing the address to be presented to the PROM in true (non-inverted) form.
6) After approximately 72 μs, PVPRO switches from low to high causing VPROG (pin 77) to dip as shown in Figure 7-2.

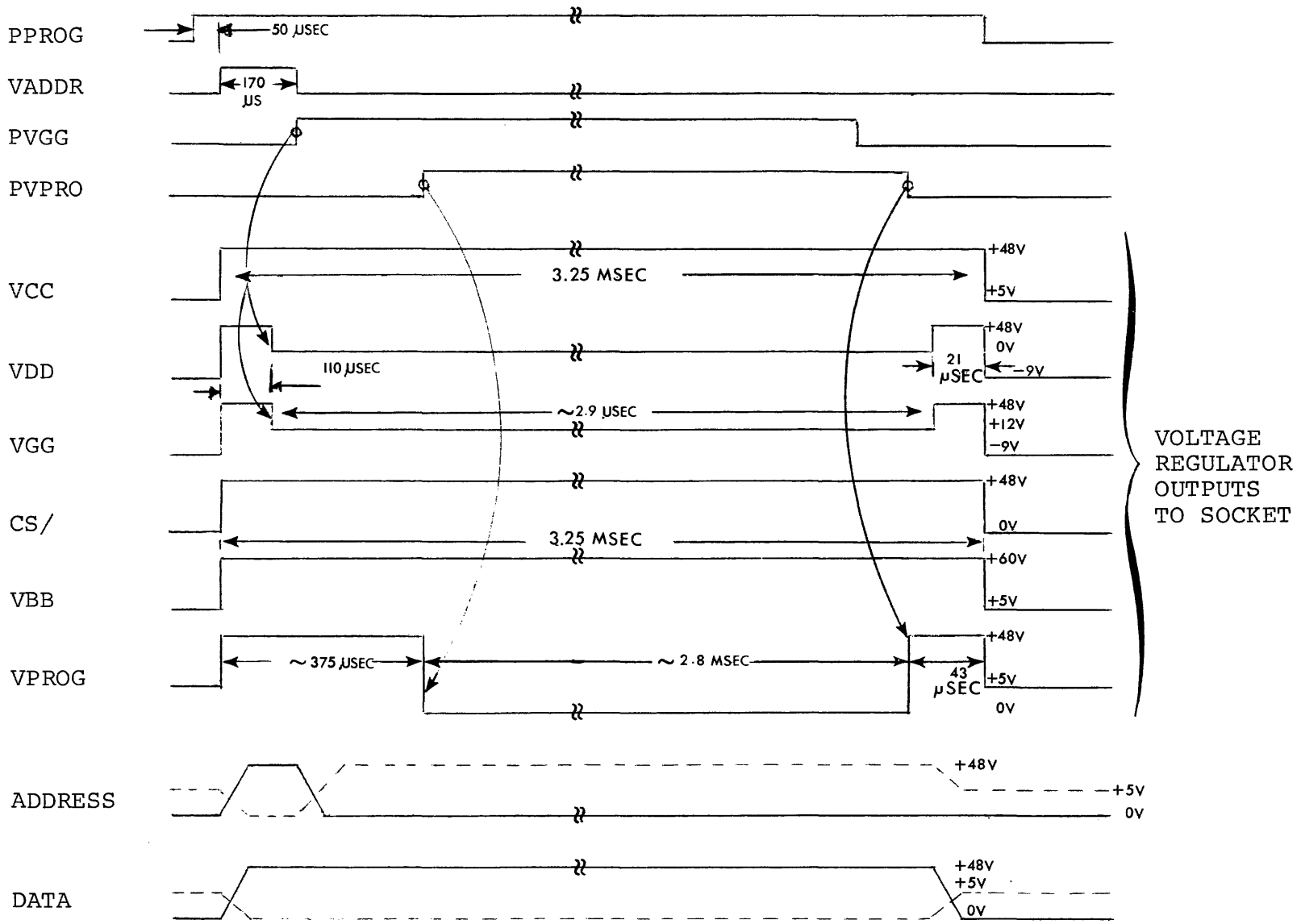


FIGURE 7-2

UPP-872 PERSONALITY CARD: PROGRAM TIMING (ALL TIMES ARE APPROXIMATE)

7) The Personality Card now holds this condition constant for approximately 2.8 msec. Then PVPRO is switched back to low causing VPROG to rise.

8) After a delay of about 21 µs PVGG is switched back to low, causing VGG and VDD to rise.

9) After another delay of 21 µs RD/WRT is switched back to low causing all six Voltage Regulator outputs to drop back to their normal levels (these levels allow a read operation to be performed).

10) The Personality Card now allows the PROM to "rest" for approximately 12.5 msec. (Since a single program cycle requires about 3 msec., the duty cycle is approximately 20%.)

11) After each program cycle the MCS™-40 performs a "read-after-write" compare using the comparitor logic on the Control Board. The Personality Card will attempt a maximum of 49 program cycles before returning control to the Control Board with a failure to program error.

After the Personality Card successfully programs a location it will continue to program that same location for a number of cycles to insure against a marginally programmed word. If N attempts are required before the first successful program, an additional 4N+5 repetitions will be performed. Upon conclusion of these repetitions, the PROM location is considered completely programmed and control returns to the Control Board.

7.3 PIN LIST: UPP-872 PERSONALITY CARD

The UPP-872 Personality Card communicates with the Control Board and the PROM socket on the front panel through a 100-pin double-sided PC edge connector. Pin allocations and designated signal functions for this 100-pin connector are listed in Table 7-1.

TABLE 7-2
UPP-872 PERSONALITY CARD PIN LIST

PIN	MNEMONIC	FUNCTION	SOURCE*	DESTINATION*
1	GND	Ground		
2	GND			
3				
4				
5	VCCH	Power inputs 5.85 VDC		
6	VCCH			
7	VCCH			
8	VCCH			
9				
10				
11	-10VDC	Power inputs		
12	-10VDC		PS	PC
13	GND	Ground		
14	GND			
15				
16	BD SENSE	Board sense	PC	CB
17			PS	PC
18				
19	CONTROL	Control bit		
20				
21	WRITE DATA 0	Write data bus from Control Board	CB	PC
22	WRITE DATA 1			
23	WRITE DATA 2			
24	WRITE DATA 3			
25	WRITE DATA 4			
26	WRITE DATA 5			
27	WRITE DATA 6			
28	WRITE DATA 7			
29	PROM ADDRESS 0	PROM address bus from Control Board	CB	PC
30	PROM ADDRESS 1			
31	PROM ADDRESS 2			
32	PROM ADDRESS 3			
33	PROM ADDRESS 4			
34	PROM ADDRESS 5			
35	PROM ADDRESS 6			
36	PROM ADDRESS 7			
37	PROM ADDRESS 8			
38	PROM ADDRESS 9			
39	PROM ADDRESS 10			
40	PROM ADDRESS 11			
41	D0	MCS-40™ data bus (bi-directional)	CB/PC	PC/CB
42	D1			
43	D2			
44	D3			
45	Φ2	MCS-40™ clock (bi-directional)	CB	PC
46	Φ1			
47	CM-ROM	ROM bank enable	CB	PC
48				
49				
50	SYNC	MCS-40™ synchronization	CB	PC

* PS = Power Supply CB = Control Board PC = UPP-872 Personality Card
FP = Front Panel (PROM socket)

TABLE 7-2 (Continued)

PIN	MNEMONIC	FUNCTION	SOURCE*	DESTINATION*
51	RESET	MCS-40™ Reset	CB	PC
52	PROM RD DATA 0/	Data read from PROM	PC	CB
53	PROM RD DATA 1/			
54	PROM RD DATA 2/			
55	PROM RD DATA 3/			
56	PROM RD DATA 4/			
57	PROM RD DATA 5/			
58	PROM RD DATA 6/			
59	PROM RD DATA 7/			
60				
61	PROM ADDRESS 2	Address to PROM	PC	FP
62	PROM ADDRESS 1			
63	PROM ADDRESS 0			
64	D0	PROM Data (bi-directional)	PC/FP	FP/PC
65	D1			
66	D2			
67	D3			
68	D4			
69	D5			
70	D6			
71	D7			
72	VCC	Power to PROM	PC	FP
73				
74				
75				
76				
77	VPROG			
78	CS/	Power to PROM	PC	FP
79	VBB			
80	VGG			
81	PROM ADDRESS 7	Address to PROM	PC	FP
82	PROM ADDRESS 6			
83	PROM ADDRESS 5			
84	PROM ADDRESS 4			
85	PROM ADDRESS 3			
86	VCC	Power to PROM	PC	FP
87	VCC			
88	VDD			
89				
90				
91	GND	Ground		
92	GND			
93				
94				
95				
96				
97	+70	Power inputs	PS	PC
98	+70			
99	GND	Ground		
100	GND			

* PS = Power Supply CB = Control Board PC = UPP-872 Personality Card
FP = Front Panel (PROM socket)

CHAPTER 8

THE UPP-848 PERSONALITY CARD

The UPP-848 Personality Card contains the logic that is needed to both program and read the contents of a PROM location in an 8748 single chip Microcomputer. The EPROM of the 8748 is an erasable, reprogrammable 1024 by 8-bit memory. Access time for the external verification of the 8748 EPROM is approximately 10 micro-seconds.

8.1 8748 PROM MICROCOMPUTER

The 8748 is an N-channel, 8-bit highly integrated microprocessor, with all of the basic building blocks of a microprocessor system incorporated on a single chip. The 8748 single chip Microcomputer includes 1024 x 8-bits of electrically programmable, erasable read-only-memory, for storing program instructions. The Universal PROM Programmer (UPP) can program all 1024 words of the PROM in less than two minutes. The 8748 PROM can be erased by controlled exposure to high intensity ultraviolet light. After it is cleared, the 8748 EPROM can be reprogrammed by the PROM Programmer. The 8748 EPROM may be erased and reprogrammed as often as desired.

The 8748 is shipped to the customer in an erased condition; that is, with zeros (output low) in all memory locations. During programming, ones (output high) are programmed selectively into the EPROM memory locations. All eight bits of one word are programmed simultaneously. After resetting the 8748 and raising its external address input, the low 8 address bits of the word to be programmed are placed on BUS 0-7 and the high 2 address bits are placed on the Port 20 and 21 inputs. A

pulse from the Personality Card causes the address to be latched in the 8748. The data to be programmed is then input on BUS 0-7. The selected memory location is programmed by applying high-voltage signals to the 8748's VDD, EA and PROG pins.

The 8748 is contained in a standard 40-pin dual-in-line package with a transparent quartz lid. A silicon die is located under the transparent lid. Erasure of the EPROM is accomplished by exposing the silicon die to ultraviolet light at a wavelength of 2537 Angstroms. The recommended dose (the product of intensity and exposure time) is 1ØW-sec/cm^2. Examples of ultraviolet sources which can be used are the Model UV5 and the Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (4115 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. Fifteen to twenty minutes exposure to the lamp, at a distance of one inch, will clear the EPROM completely. Avoid unnecessary or prolonged exposures, which are potentially damaging to the PROM.

-- WARNING --

High intensity ultraviolet light can cause serious burns. Ultraviolet radiation can also generate potentially hazardous amounts of ozone. Observe the following precautions when using an ultraviolet source to erase a EPROM:

1) Never expose skin or eyes to the source directly.

2) Do not stare at an object that is under ultraviolet illumination. The light is invisible, but in nevertheless injurious to eye tissue.

3) Use the source only in a well-ventilated area.

8.2 8748 ADAPTER FOR 24-PIN SOCKETS

Because the 8748 is packaged in a 40-pin DIP, an adapter is required to allow insertion into the 24-pin socket on the front panel of the Universal PROM Programmer. The 8748 Adapter fulfills this requirement. The 8748 Adapter must be inserted into the front panel socket with pin 1 in the upper left hand side. The 8748 should be inserted into the 8748 Adapter also with pin 1 in the upper left hand side. If the Adapter or the 8748 are not properly inserted or if an 8748 is not present when an operation is attempted, the EPROM Programmer will indicate an orientation error.

Figure 8-1 shows the pin relationships between the Adapter's connectors to the 8748 (connector J1) and to the UPP front panel (connector P1).

8.3 FUNCTIONAL DESCRIPTION: UPP-848

The UPP-848 Personality Card contains all of the logic needed to program or read the EPROM program memory of an 8748 single chip Microcomputer. The Personality card operates under the supervision of the Control Board (see Chapter 2). The 40-pin 8748 plugs into an adapter that, in turn, plugs into the 24-pin socket on the front panel of the Universal PROM Programmer. This socket is wired directly to the Personality Card.

The Control Board is responsible for supplying address and data information, and requesting that the Personality Card perform either a program or a read operation. The Personality Card, in turn, attempts

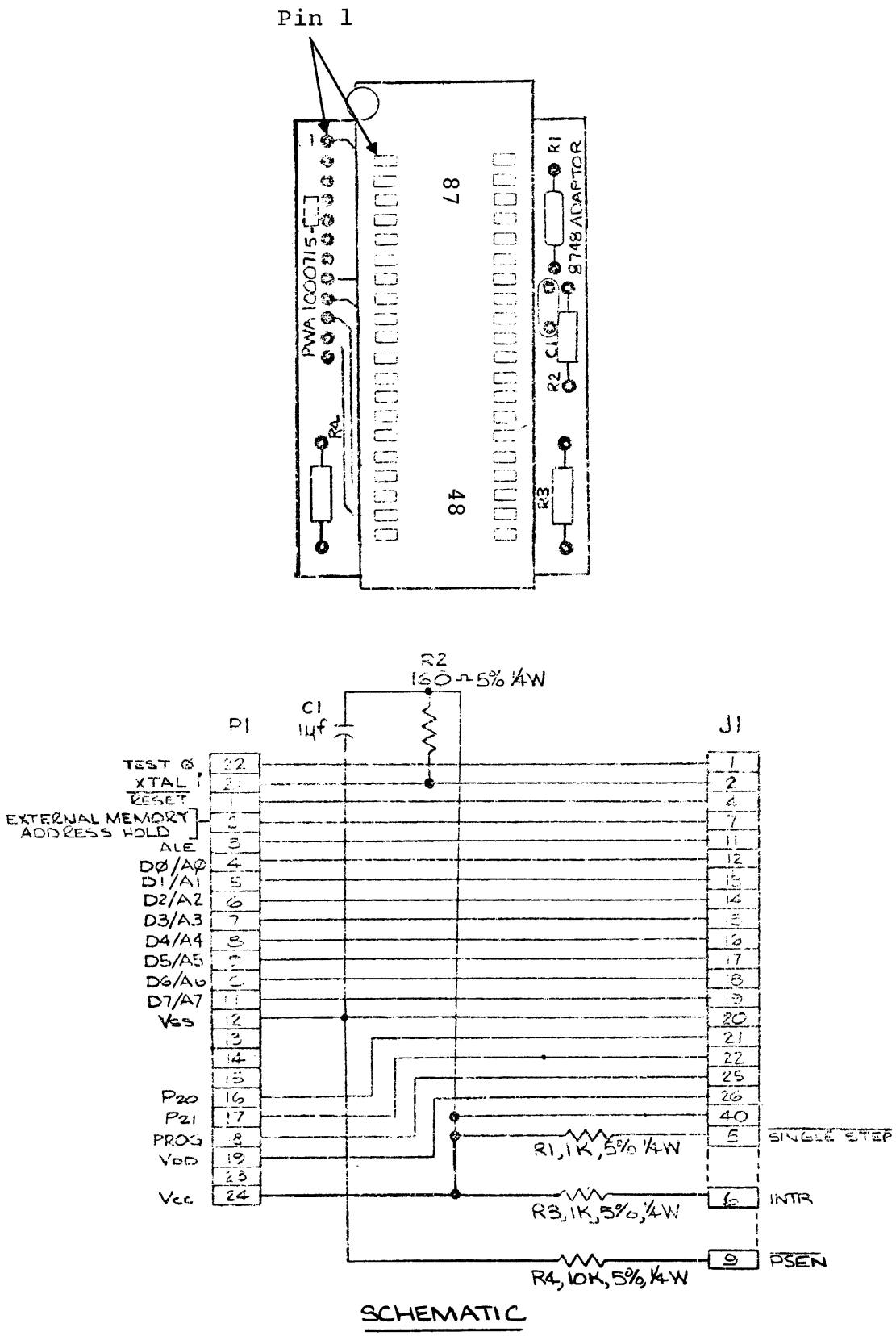


FIGURE 8-1. 8748 ADAPTER PIN ASSIGNMENTS*

(*Reference use only.)

to perform the requested operation, returns data to the Control Board (from the read or verify-after-program operation), and notifies the Control Board of the success or failure of the operation.

Figure 8-2 is a functional block diagram of the UPP-848 Personality Card. It may be helpful to frequently refer to this diagram during the following discussion of the Personality Card. The signal mnemonics that appear in Figure 8-2 generally correspond to the mnemonics used on the schematic of the UPP-848 Personality Card (see Appendix B).

Communications between the Personality Card and Control Board are handled by four parallel busses:

1) The MCS-40 Bus includes the control, timing and data paths that allow the 4040 processor on the Control Board to communicate with the two 4001 ROM's and the 4002-1 RAM on the Personality Card.

2) The PROM Address bus provides the Personality Card with the 12-bit PROM address from the Control Board.

3) The PROM Write Data bus from the Control Board provides the 8-bit data word to be programmed into the PROM by the Personality Card.

4) The PROM Read Data bus returns the 8-bit data word from the selected PROM location to the Control Board.

The UPP-848 Personality Card can be divided into six major functional blocks, as shown in Figure 8-2:

1) The PROM Address/Data logic includes two 74L157 multiplexers (at A14 and A15) that route the PROM address or the PROM write data to the 8748 device. When the Address Selection (ADDR SEL/) output from I/O port 2 on the 4001 ROM at A17 is low (true) and the TEST Ø CTL/ output from I/O port 0

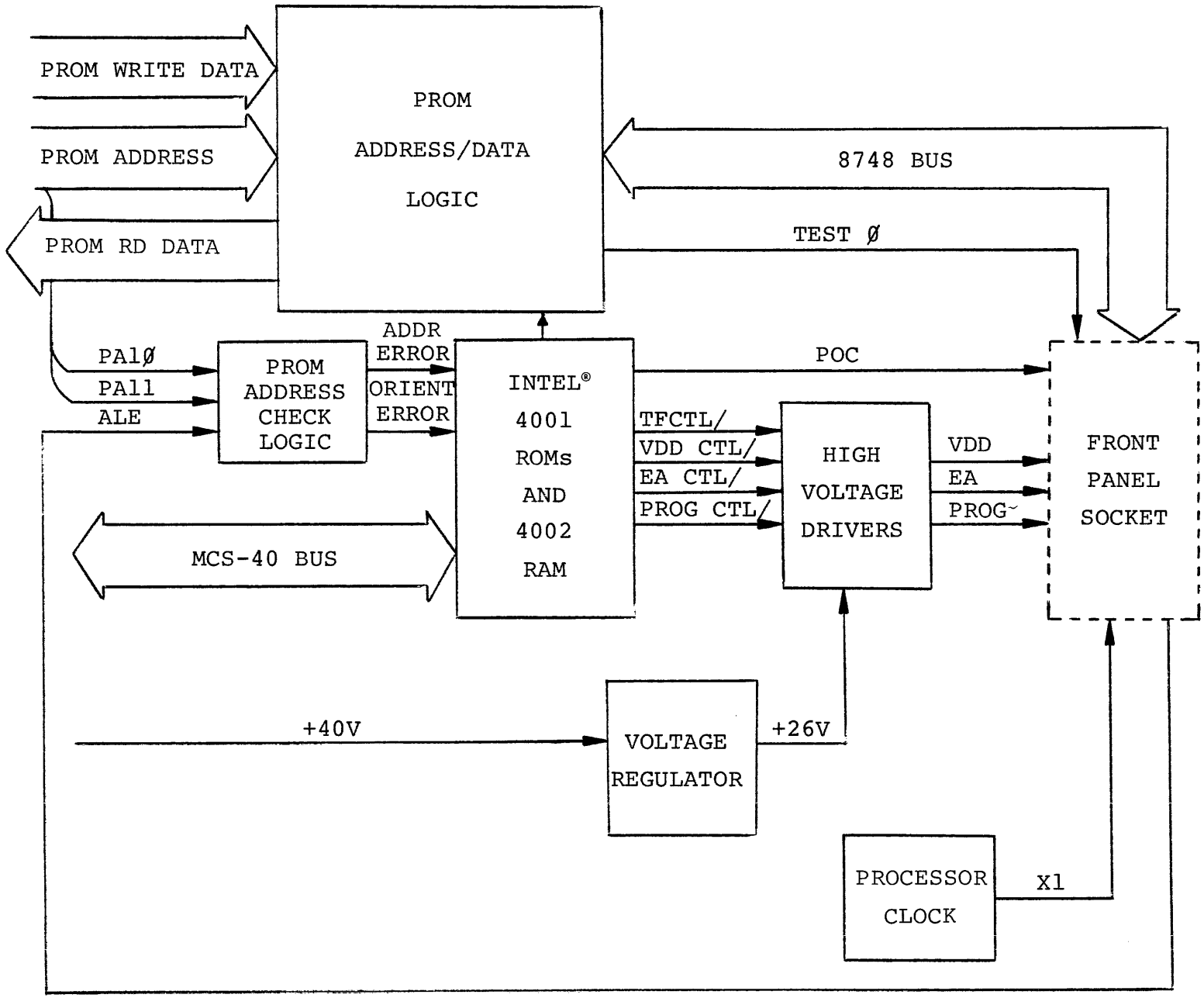


FIGURE 8-2. UPP-848 PERSONALITY CARD FUNCTIONAL BLOCK DIAGRAM

on the same 4001 is high, the eight low-order PROM address bits (PROM ADR Ø-7) are gated through to the data inputs on the 8748 (DØ-D7). Address bits 8 and 9 (PROM ADDR 8-9) are made available to the Port 20 and 21 inputs on the 8748 (P20-21). The two most significant address bits (PROM ADR 10 and 11) are available to the Address Check logic (see below).

If the Address Selection line (ADDR SEL/) is false (high), the two multiplexers gate the eight PROM Write Data bits (WR DATA 0-7) through to the 8748 data inputs (DO-7). In both cases the low level on the TEST Ø line informs the 8748 that it is to accept the data at its DO-D7 pins. Figure 8-3 illustrates address and data timing.

During PROM read operations or during the verification cycle in a program sequence, the TEST Ø line is high allowing the 8748 to send a data byte to the Personality Card. The data on lines DØ-D7 is inverted and applied to an 8212 Bus Driver in the Personality Card's PROM Address/Data section (at A19). When the MCS-40 activates the Bus Enable (BUS EN) output from I/O Port 3 on the 4001 ROM at A16, the data is enabled through the 8212 device and onto the PROM RD DATA 0-7 lines to the Control Board.

2) The PROM Address Check logic performs two functions. This logic examines the two high-order PROM Address bits, PA10 and PA11, to check for a boundary error. PA10 and PA11 are inverted and applied to switch S1. Because switch settings

6-3 and 5-4 must be closed, a high on either PA10 or PA11 (indicating an address greater than 1023) will activate the ADDR BOUNDARY ERROR/ line which is read by the 4040 processor through I/O Port 1 on the 4001 ROM at A16.

The Address Check logic also detects orientation errors. Before a program operation, the 8748 is reset by a pulse on the Power On Clear (POC) line. The MCS-40 also clears the Orientation Error counter (at A6 on the Personality Card) by pulsing the Enable Address Line (EN ALE). After the 8748 pulse is reset, it accesses all locations in its erased program memory (executing a NOP in each location). The 8748 pulses its Address Enable (ALE) output as it accesses each location. The Orientation Error counter counts each pulse on the ALE line. If the 8748 device or its adapter is improperly inserted in the front panel of the PROM Programmer or if an 8748 is not present, the output from the counter will be low, activating the ORIENTATION ERROR line which is read by the 4040 processor through I/O Port Ø on the 4001 ROM at A16.

3) The two Intel 4001 ROMs (at A16 and A17) and one 4002 RAM (at A18) are part of the MCS-40 chip set (the 4040 processor is located on the Control Board). The ROMs contain instructions for the MCS-40 that will effect the reading or programming of the 8748 PROM. The MCS-40 interacts with the Personality Card through the I/O ports on the two ROM chips and the RAM chip.

4) The Voltage Regulator (At A9) supplies the +26V (approximate) operating voltage to the high-voltage drivers at VDD (pin P1-S3), and + 24.5V (approx.) to EA (pin P1-62) and PROG (pin P1-82). The regulator logic has two protective circuits. One is a current limit of 300 mA (set by R73 and R51) to protect the regulator and the high-voltage drivers against shorts at the PROM socket. The other is a crowbar circuit that will short out the +40V supply, should the regulator fail.

5) The High Voltage Drivers perform the actual PROM Programming. Three different circuits drive the EA, VDD and PROG lines.

When the MCS-40 outputs a low level on the EA CTL/ line (port 2 on the 4002 RAM), transistor Q3 drives the External Address (EA) line (pin P1-62) to +24.5V (approx.)

If the Fall Time Control (TFCTL/) line is high, transistor Q5 will drive the VDD line (Pin P1-83) to +26V (approx.) when the MCS-40 outputs a low level on the VDD CTL/ line (port 1 on the 4002 RAM). When the MCS-40 outputs a low level on TFCTL/ (port Ø on the RAM), transistor Q4 is turned on dropping VDD to approximately +5V.

Prior to the beginning of a program operation, both transistors Q1 and Q2 are off thus maintaining a "floating" condition on the PROG line. When a program operation begins (TEST Ø goes low), transistor Q1 is activated thus grounding the PROG line. When the MCS-40 outputs a low level on the PROG CTL/ line (port 3 on the 4002 RAM), transistor Q1 goes

off and transistor Q2 goes on, driving PROG to approximately 24.5V. This programming pulse is maintained for approximately 50 milleseconds, as shown in Figure 8-3.

6) The Processor Clock logic includes a crystal oscillator that provides a stable 5.185 MHz timing reference for the 8748 single chip Microcomputer via the X1 line (pin P1-85).

The remainder of this section will describe how the functional blocks interact to perform the two operations: program and read. There are two distinct locations in the ROM on the UPP-848 Personality Card that are the entry points to which the MCS-40 branches: one entry point for a program operation and one for a read. When the Personality Card receives control, it assumes that the PROM Address is available on the address bus. In the case of a program operation, it also assumes that the PROM Write Data is on the data bus. In either case, the first step is to check for an orientation error or an address boundary error. If no 8748 is present or if it is improperly inserted in the UPP front panel, an orientation error is indicated. If the 12-bit PROM Address is greater than 1023, and address boundary error is indicated. If either error is detected, the Personality Card aborts the operation and returns control to the Control Board. If no errors are detected, the operation continues.

PROM READ DATA:

After the address has been checked, the sequence of events is as follows:

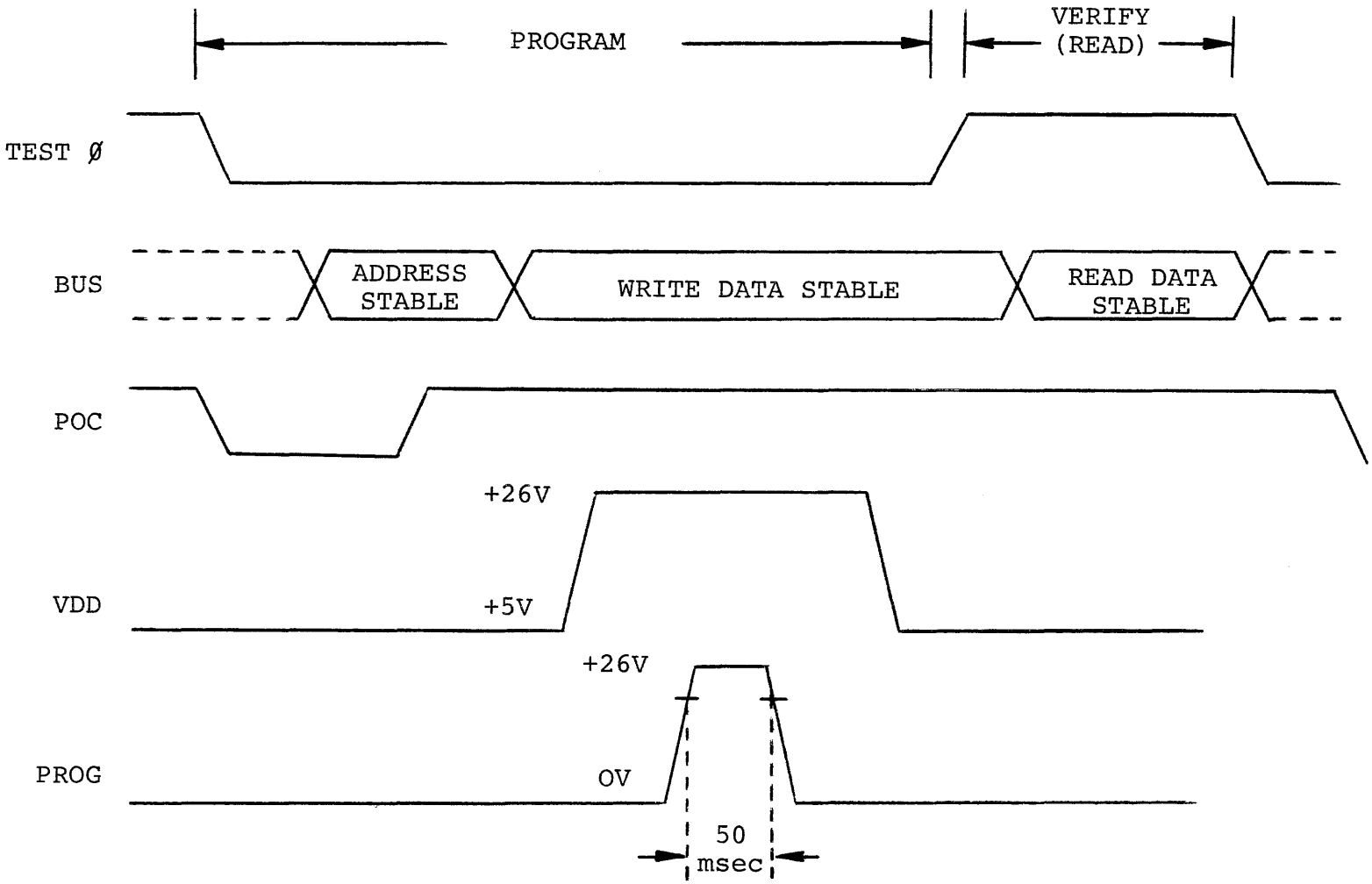


FIGURE 8-3. UPP-848 PERSONALITY CARD (WITH 8748 ADAPTER) TIMING FOR THE 8748

A. Power on clear, POC (ROM port 1 at A17), switched to low then released; this resets the 8748.

B. EA CTL/ (RAM port 2) output goes low, driving the External Address line (EA) to 24.5 (approx.)

C. MCS-40 switches ADDR SEL/ (ROM port 2 at A17) low, allowing the eight low-order address bits to be gated out to the 8748's data pins. Address bits 8 and 9 are available to the 8748 at the P20 and P21 pins. POC is momentarily grounded to latch the address in the 8748.

D. MCS-40 switches TST Ø CTL (ROM port Ø at A17) to high. TEST Ø (pin P1-86) informs 8748 that read is to occur.

E. After POC is raised, data appears on the data lines (DO-D7). The MCS-40 outputs a high level on BUS EN (ROM port 3 at A16). BUS EN enables the data to be gated onto the PROM RD DATA lines to the Control Board, thus completing the read operation.

PROM PROGRAM DATA:

The program operation is similar to the read. The sequence of events is as follows.

A. The MCS-40 checks to see that the Voltage Regulator is receiving +40 volts from the power supply; MCS-40 reads HIGH VOLTAGE PRESENT at ROM (A16) port 2. If +40V is not present, the program operation is aborted, and control returns to the Control Board.

B. POC is grounded then released, resetting the 8748.

C. TEST Ø is grounded indicating a program operation. TEST Ø also allows PROG line to be grounded.

D. EA is driven to +24.5V (approx.), as described above.

E. PROM Address bits 0-9 are gated through to the 8748 as described above. POC is momentarily grounded to latch the address in the 8748.

F. The MCS-40 switches ADDR SEL/ (ROM port 2 at A17) high allowing the Write Data to be gated out to the 8748's data pins.

G. MCS-40 switches VDD CTL/ (RAM port 1) low, driving VDD to approximately +26V.

H. MCS-40 switches PROG CTL/ (RAM port 3) low, driving PROG to +24.5 (approx.). This programming pulse is maintained for approximately 50 msec.

I. MCS-40 switches TFCTL/ (RAM port Ø) low, causing VDD to return to +5V.

J. MCS-40 verifies the programming operation by reading the programmed PROM location (as described above) and comparing it to the expected value. If the programming was not successful, the program and verification sequences are repeated once. If the PROM location is still not correctly programmed, an error is indicated and control is returned to the Control Board.

Figure 8-3 illustrates timing for both program and read sequences.

8.4 PIN LIST: UPP-848 PERSONALITY CARD

The UPP-848 Personality Card communicates with the Control Board and the PROM socket on the front panel through a 100-pin double-sided PC edge connector (P1). Pin allocations and designated signal functions for this 100-pin connector are given in Table 8-1.

TABLE 8-1. UPP-848 PERSONALITY CARD PIN LIST

PIN	MNEMONIC	FUNCTION	SOURCE	DESTINATION
1	GND	Ground		
2	GND			
3				
4				
5	VCCH	Power inputs (5.85 VDC)	PS	PC
6	VCCH			
7	VCCH			
8	VCCH			
9	GND	Ground		
10	GND			
11	-10V	Power Inputs	PS	PC
12	-10V			
13	GND	Ground		
14	GND			
15				
16				
17				
18				
19				
20				
21	WR DATA 0	PROM Write Data bus from Control Board	CB	PC
22	WR DATA 1			
23	WR DATA 2			
24	WR DATA 3			
25	WR DATA 4			
26	WR DATA 5			
27	WR DATA 6			
28	WR DATA 7			
29	PROM ADR 0	PROM Address bus from Control Board	CB	PC
30	PROM ADR 1			
31	PROM ADR 2			
32	PROM ADR 3			
33	PROM ADR 4			
34	PROM ADR 5			
35	PROM ADR 6			
36	PROM ADR 7			
37	PROM ADR 8			
38	PROM ADR 9			
39	PROM ADR 10			
40	PROM ADR 11			
41	D0	T.M. MCS-40 DATA BUS (Bidirectional)	CB/PC	PC/CB
42	D1			
43	D2			
44	D3			

*PS = Power Supply, CB = Control Board,
PC = UPP-848 Personality Card, FP = Front Panel PROM socket.

TABLE 8-1. UPP-848 PERSONALITY CARD PIN LIST (Continued)

PIN	MNEMONIC	FUNCTION	SOURCE	DESTINATION
45	Ø2	MCS-40 Clock Signals	CB	PC
46	Ø1			
47	CM-ROM	ROM Bank Enable	CB	PC
48				
49	CM-RAM	RAM Bank Enable	CB	PC
50	SYNC	MCS-40 Synchronization	CB	PC
51	RESET	MCS-40 Reset	CB	PC
52	PROM RD DATA 0	PROM RD Data Bus to Control Board	PC	CB
53	PROM RD DATA 1			
54	PROM RD DATA 2			
55	PROM RD DATA 3			
56	PROM RD DATA 4			
57	PROM RD DATA 5			
58	PROM RD DATA 6			
59	PROM RD DATA 7			
60				
61	POC	Power on Clear	PC	FP
62	EA	External Address	PC	FP
63	ALE	Address Line Enable	FP	PC
64	DO/.A0	Data/Address bus to 8748 Bidirectional)	PC/FP	FP/PC
65	D1/ A1			
66	D2/ A2			
67	D3/ A3			
68	D4/ A4			
69	D5/ A5			
70	D6/ A6			
71	D7/A7			
72	GND	Signal GND		
73	GND			
74	GND			
75	GND			
76	GND			
77	RD/	Read/Comm	PC	FP
78	ALE55	Address Line Enable 55	PC	FP
79	A10	Address bit 10	PC	FP
80	P20	Port 2Ø (8748)	PC	FP
81	P21	Port 21 (8748)		
82	PROG	Program Pulse	PC	FP
83	VDD	Power to PROM	PC	FP
84	A11	Address bit 11	PC	FP
85	X1	Processor Clock	PC	FP
86	TEST Ø	Test Ø line	PC	FP
87	PROG/Ce/	Program Ø and Chip Enable	PC	FP
88	VCC	+5	PC	FP

*PS = Power Supply, CB = Control Board,
PC = UPP-848 Personality Card, FP = Front Panel PROM Socket.

TABLE 8-1. UPP-848 PERSONALITY CARD PIN LIST (Continued)

PIN	MNEMONIC	FUNCTION	SOURCE	DESTINATION
89				
90				
91	GND	Ground		
92	GND			
93				
94				
95	+40V	Power to Voltage reg.	PS	PC
96	+40V			
97				
98				
99	GND	Ground		
100	GND			

*PS = Power Supply, CB = Control Board,
PC = UPP-848 Personality Card, FP = Front Panel PROM Socket

CHAPTER 9

THE UPP-855 AND UPP-955 PERSONALITY CARDS

The UPP-855 contains the Personality Card and Adapter for programming and reading the EPROM memory on the Intel 8755. Similarly, the UPP-955 contains the Personality Card and Adapter for programming and reading the EPROM on the 8755A, which is a new version of the 8755 chip.

The Personality Cards in both the UPP-855 and the UPP-955 are identical; however, they require two different adapters to interface the 40-pin chips to the 24-pin front panel socket on the UPP-101 or the UPP-102. The UPP-UP1 adapter interfaces the 8755, and the UPP-UP2 interfaces the 8755A. These adapters are shown in Figures 9-1 and 9-2, respectively. Each adapter is marked with the appropriate chip number for identification. Note that the only requirement for updating the UPP-855 to program the 8755A is to replace the adapter. To replace the adapter, contact:

Intel Technical Services
Dept. 472
3065 Bowers Avenue
Santa Clara, CA 95051
Telephone: (408) 987-7189

Since the installation and the operation of the UPP-855 is the same as the UPP-955, the following text refers to both units as the "Personality Card". Similarly, the text refers to both the 8755 and the 8755A as the "Device".

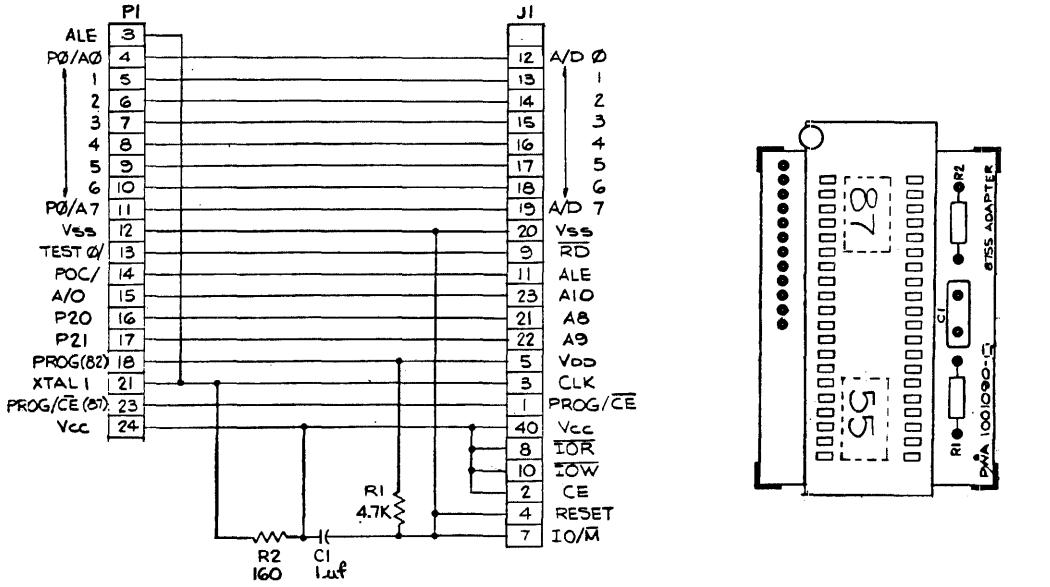


Figure 9-1. 8755 Adapter (UPP-UP1) Pin Assignments
(Reference use only)

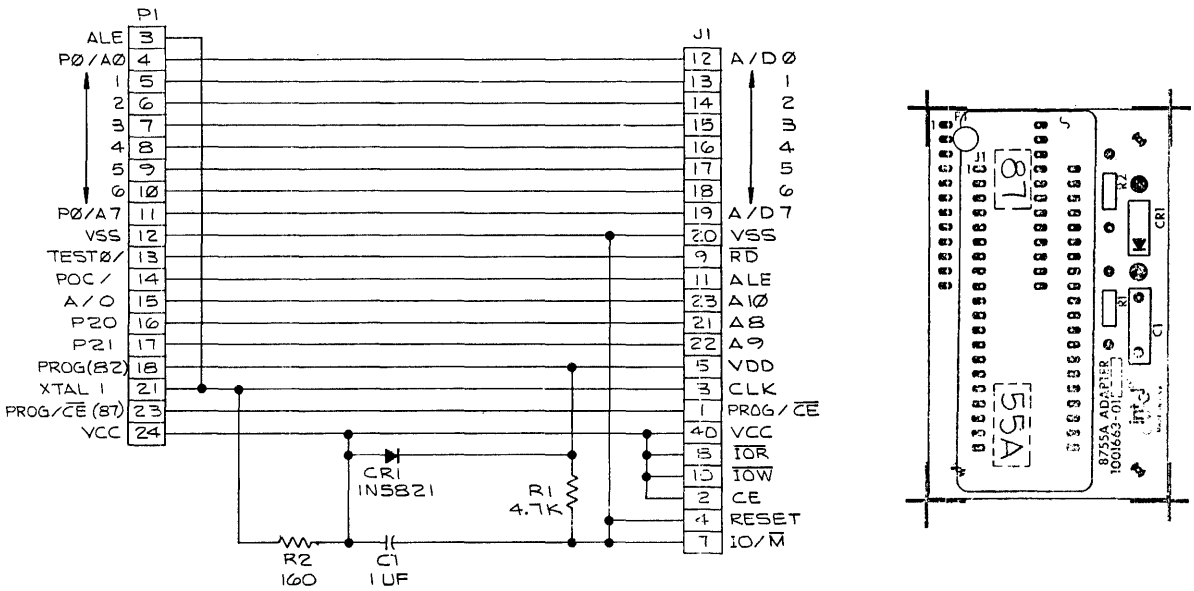


Figure 9-2. 8755A Adapter (UPP-UP2) Pin Assignments
(Reference use only)

9.1 8755 AND 8755A PROM-I/O DEVICES

The 8755 is a dual-function chip that has 16K of electrically programmable and erasable ROM (EPROM), and two general-purpose I/O ports. The memory organization is 2048 x 8 bits. The 8755A is a new version of the device.

Both devices are mounted in standard 40-pin dual-in-line packages with transparent quartz lids. A silicon die is located under the transparent lid, which allows the EPROM to be erased by exposure to high-intensity ultraviolet light.

The devices are shipped in an erased condition; that is, with ones (output high) in all memory locations. During programming, zeros (output low) are programmed selectively into EPROM memory locations. All eight bits of one word are programmed simultaneously. The programming procedure is as follows:

1. The low eight address bits of the word to be programmed are placed on A/D 0-7, and the high order address bits and chip selects are placed on the device. A pulse from the Personality Card causes the address to be latched.

2. The data to be programmed is input on pins A/D 0-7.

3. The selected memory location is programmed by one high-voltage signal applied to the VDD pin.

The EPROM is erased by exposing the silicon die to ultraviolet light with a wavelength of 2537 Angstroms. The recommended dose (the product of intensity and exposure time) is 10W-sec/cm^2. Examples of ultraviolet sources which can be used are the Model UV5 and the Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc. (4115 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. Fifteen to twenty minutes exposure to the lamp, at a distance of one inch, will

clear the EPROM completely. Avoid unnecessary or prolonged exposures, which are potentially damaging to the PROM.

-- WARNING --

High intensity ultraviolet light can cause serious burns. Ultraviolet radiation can also generate potentially hazardous amounts of ozone. Observe the following precautions when using an ultraviolet source to erase an EPROM:

1) Never expose skin or eyes to the source directly.

2) Do not stare at an object that is under ultraviolet illumination. The light is invisible, but is nevertheless injurious to eye tissue.

3) Use the source only in a well-ventilated area.

9.2 8755 and 8755A ADAPTERS

Both devices require adapters to interface the 40-pin device package to the 24-pin front panel socket on the Universal PROM Programmer. Adapters are identified by the number of the appropriate chip. The adapter must be inserted into the front panel socket of the UPP with pin 1 in the upper left corner. Similarly, the device being programmed must be inserted with pin 1 in the upper left corner. If the device or the adapter is not inserted properly, the PROM Programmer will indicate an orientation error when an operation is attempted.

Figure 9-1 shows the connections between the 8755 chip socket (J1) and the UPP front panel connector (P1). Similarly, Figure 9-2 shows the connections between the 8755A and the front panel connector.

9.3 FUNCTIONAL DESCRIPTION: UPP-855 AND UPP-955

The UPP-855 and UPP-955 Personality Cards and adapters contain the logic for programming or reading the EPROM program memory of associated devices. The Personality Card operates under the supervision of the Control Board (see Chapter 2). The devices plug into adapters that, in turn, plug into a 24-pin socket on the front panel of the Universal PROM Programmer. This socket is wired directly to the Personality Card.

The Control Board is responsible for supplying address and data information, and requesting that the Personality Card perform either a program or a read operation. The Personality Card, in turn, attempts to perform the requested operation, returns data to the Control Board (from the read or verify-after-program operation), and notifies the Control Board of the success or failure of the operation.

Figure 9-3 is a functional block diagram of the Personality Card. It may be helpful to refer to this diagram during the following discussion. The signal mnemonics that appear in Figure 9-3 generally correspond to the mnemonics used on the Personality Card schematic diagram.

Communications between the Personality Card and Control Board are handled by four parallel buses:

1) The MDS-40 Bus includes the control, timing and data paths that allow the 4040 processor on the Control Board to communicate with the two 4001 ROM's and the 4002-1 RAM on the Personality Card.

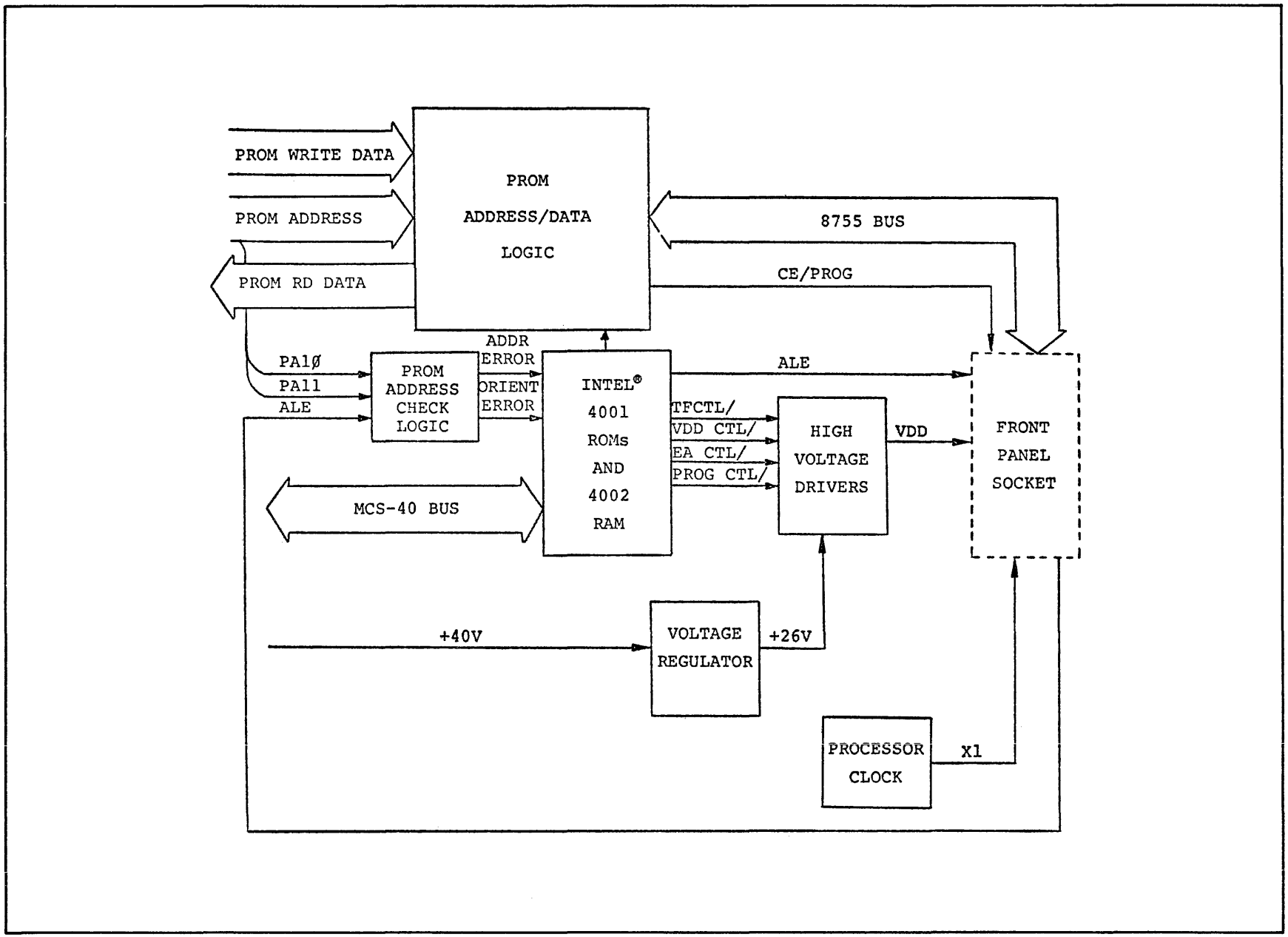


FIGURE 9-3. PERSONALITY CARD FUNCTIONAL BLOCK DIAGRAM

2) The PROM Address bus provides the Personality Card with the 12-bit PROM address from the Control Board.

3) The PROM Write Data bus from the Control Board provides the 8-bit data word to be programmed into the PROM by the Personality Card.

4) The PROM Read Data bus returns the 8-bit data word from the selected PROM location to the Control Board.

The Personality Card can be divided into six major functional blocks, as shown in Figure 9-3.

1) The PROM Address/Data Logic includes two 74L157 multiplexers (at A14 and A15) that route the PROM address or the PROM write data to the device. When the Address Selection (ADDR SEL/) output from I/O port 2 on the 4001 ROM at A17 is low (true) and the TEST 0 CTL/ output from I/O port 0 on the same 4001 is high, the eight low-order PROM address bits (PROM ADR 0-7) are gated through to the data inputs on the Device (D0-D7). The high order Address bits are made available to the Adapter card. The most significant address bit is available to the Address Check logic (see below).

   If the Address Selection line (ADDR SEL/) is false (high), the two multiplexers gate the eight PROM Write Data bits (WR DATA 0-7) through to the Device data inputs (D0-7). In both cases the low level on the TEST 0 line informs the Device that it is to accept the data at its D0-D7 pins. Figure 9-4 shows the address and data timing.

   During PROM read operations or during the verification cycle in a program sequence, the TEST 0 line is high, allowing the Device to send a data byte to the Personality Card. The data on lines D0-D7 are inverted and applied to an 8212 Bus Driver in the Personality Card's PROM Address/Data section (at A19). When the MCS-40 activates the Bus Enable (BUS EN)

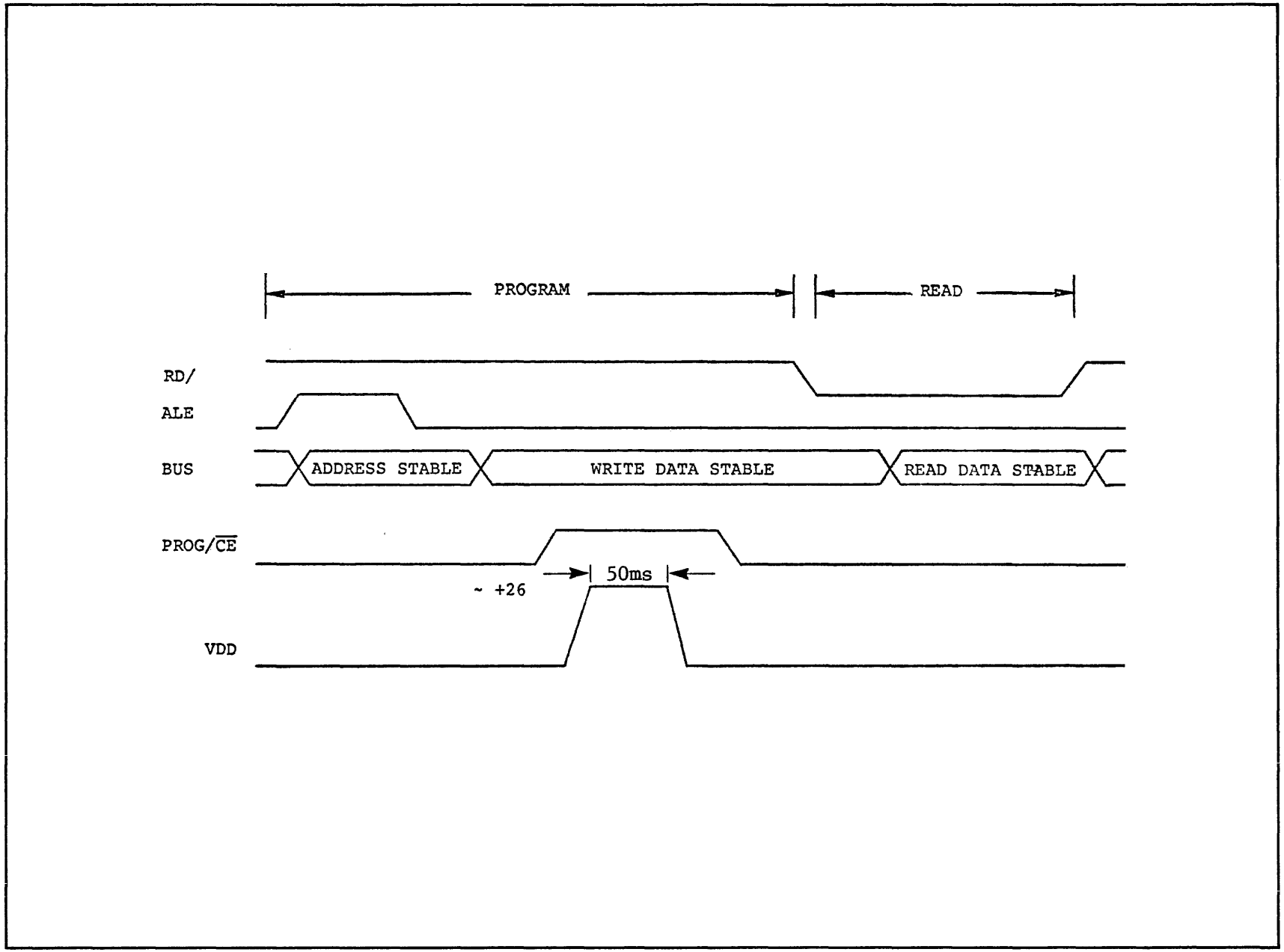


FIGURE 9-4. PERSONALITY CARD (WITH ADAPTER) TIMING

output from I/O Port 3 on the 4001 ROM at A16, the data is enabled through the 8212 device and onto the PROM RD DATA 0-7 lines to the Control Board.

2) The PROM Address Check logic examines the high-order PROM Address bit, PA11, to check for a boundary error. A high on PA11 (indicating an address greater than 2048) activates the ADDR BOUNDARY ERROR/ line, which is read by the 4040 processor through I/O Port 1 on the 4001 ROM at A16.

3) The two Intel 4001 ROMs (at A16 and A17) and one 4002 RAM (at A18) are part of the MCS-40 chip set (the 4040 processor is located on the Control Board). The ROMs contain instructions for the MCS-40 that will affect the reading or programming of the PROM. The MCS-40 interacts with the Personality Card through the I/O ports on the two ROM chips and the RAM chip.

4) The Voltage Regulator (at A9) supplies the +26V (approximate) operating voltage to the high-voltage drivers. The regulator logic has two protective circuits. One is a current limit of 300 mA (sensed by R73 and R51) to protect the regulator and the high-voltage drivers against shorts at the PROM socket. The other is a crowbar circuit that will short out the +40V supply, should the regulator fail.

5) The High Voltage Drivers perform the actual PROM Programming; VDD is the only high voltage required. Prior to the beginning of a program operation, both transistors Q1 and Q2 are off, thus maintaining a "floating" condition on the VDD line. A pulldown resistor on the adapter card provides a TTL "0" on the VDD pin during read operations. When a program operation begins transistor Q1 is activated, thus grounding the VDD line. When the MCS-40 outputs a low level on the VDD line (port 3 on the 4002 RAM), transistor Q1 goes off and

transistor Q2 goes on, driving VDD to approximately +25V. This programming pulse is maintained for approximately 50 milliseconds, as shown in Figure 9-4.

6) The Processor Clock logic includes a crystal oscillator that provides a stable 5.185 MHz timing reference for the device being programmed, via clock line (pin P1-85).

The remainder of this section will describe how the functional blocks interact to perform the two operations: program and read. There are two distinct locations in the ROM on the Personality Card that are the entry points to which the MCS-40 branches: one entry point for a program operation and one for a read. When the Personality Card receives control, it assumes that the PROM Address is available on the address bus. In the case of a program operation, it also assumes that the PROM Write Data is on the data bus. In either case, the first step is to check for an orientation error or an address boundary error. If no Adapter is present an orientation error is indicated. If the 12-bit PROM Address is greater than 2048 an address boundary error is indicated. If either error is detected, the Personality Card aborts the operation and returns control to the Control Board. If no errors are detected, the operation continues.

PROM READ DATA:

After the address has been checked, the sequence of events is as follows:

A. MCS-40 switches ADDR SEL/ (ROM port 2 at A17) low, allowing the eight low-order address bits to be gated out to the device's bus pins. Higher order address bits are made available to the device. ALE is momentarily pulsed to latch the address in the device.

B. MCS-40 switches RD/ to low. This informs the device that a read is to occur.

C. Then data appears on the data lines (D0-D7). The MCS-40 outputs a high level on BUS EN (ROM port 3 at A16). BUS EN enables the data to be gated onto the PROM RD DATA lines to the Control Board, thus completing the read operation.

PROM PROGRAM DATA

The program operation is similar to the read. The sequence of events is as follows:

A. The MCS-40 checks to see that the Voltage Regulator is receiving +40 volts from the power supply; MCS-40 reads HIGH VOLTAGE PRESENT at ROM (A16) port 2. If +4V is not present, the program operation is aborted, and control returns to the Control Board.

B. PROM Address bits 0-10 are gated through to the Device, as described above. ALE is momentarily inverted to latch the address in the Device.

C. The MCS-40 switches ADDR SEL/ (ROM port 2 at A17) high allowing the Write Data to be gated out to the data pins on the device.

D. MCS-40 switches VDD CTL/ (RAM port 1) low, which causes PROG/CE to go high.

E. MCS-40 switches PROG CTL/ (RAM port 3) low, driving VDD to +26V (approx.). This programming pulse is maintained for approximately 50 msec.

F. MCS-40 verifies the programming operation by reading the programmed PROM location (as described above) and comparing it to the expected value. If the programming was not successful, the program and verification sequences are repeated once. If the PROM location is still not correctly programmed, an error is indicated and control is returned to the Control Board.

Figure 9-4 illustrates timing for both program and read sequences.

9.4 SYSTEM SOFTWARE REQUIREMENTS

The devices can be programmed using standard PROM programming software commands provided in the Intellec MCS Monitor or by using the Universal PROM Mapper Program (UPM). The usage of these programs can be obtained in the MDS-800 Intellec MDS Operator's Manual (Monitor commands) or the Universal PROM Mapper Manual.

9.5 PERSONALITY CARD PIN LIST

The Personality Card communicates with the Control Board and the PROM socket on the front panel through a 100-pin double-sided PC edge connector (P1). Pin allocations and designated signal functions for this 100-pin connector are given in Table 9-1.

TABLE 9-1. PERSONALITY CARD PIN LIST

PIN	MNEMONIC	FUNCTION	SOURCE	DESTINATION
1	GND	Ground		
2	GND			
3				
4				
5	VCCH	Power inputs (5.85 VDC)	PS	PC
6	VCCH			
7	VCCH			
8	VCCH			
9	GND	Ground		
10	GND			
11	-10V	Power Inputs	PS	PC
12	-10V			
13	GND	Ground		
14	GND			
15				
16				
17				
18				
19				
20				
21	WR DATA 0	PROM Write Data bus from Control Board	CB	PC
22	WR DATA 1			
23	WR DATA 2			
24	WR DATA 3			
25	WR DATA 4			
26	WR DATA 5			
27	WR DATA 6			
28	WR DATA 7			
29	PROM ADR 0	PROM Address bus from Control Board	CB	PC
30	PROM ADR 1			
31	PROM ADR 2			
32	PROM ADR 3			
33	PROM ADR 4			
34	PROM ADR 5			
35	PROM ADR 6			
36	PROM ADR 7			
37	PROM ADR 8			
38	PROM ADR 9			
39	PROM ADR 10			
40	PROM ADR 11			
41	D0	MCS-40 DATA BUS	CB/PC	PC/CB
42	D1			
43	D2			
44	D3			

*PS = Power Supply, CB = Control Board,
PC = Personality Card, FP = Front Panel PROM socket.

TABLE 9-1. PERSONALITY CARD PIN LIST (Continued)

PIN	MNEMONIC	FUNCTION	SOURCE	DESTINATION
45	02	MCS-40 Clock Signals	CB	PC
46	01			
47	CM-ROM	ROM Bank Enable	CB	PC
48				
49	CM-RAM	RAM Bank Enable	CB	PC
50	SYNC	MCS-40 Synchronization	CB	PC
51	RESET	MCS-40 Reset	CB	PC
52	PROM RD DATA 0	PROM RD Data Bus to Control Board	PC	CB
53	PROM RD DATA 1			
54	PROM RD DATA 2			
55	PROM RD DATA 3			
56	PROM RD DATA 4			
57	PROM RD DATA 5			
58	PROM RD DATA 6			
59	PROM RD DATA 7			
60				
61	POC	Power on Clear	PC	FP
62	EA	External Address	PC	FP
63	ALE	Address Line Enable	FP	PC
64	D0/A0	Bidirectional Data/Address bus to Device	PC/FP	FP/PC
65	D1/A1			
66	D2/A2			
67	D3/A3			
68	D4/A4			
69	D5/A5			
70	D6/A6			
71	D7/A7			
72	GND	Signal GND		
73	GND			
74	GND			
75	GND			
76	GND			
77	RD/	Read/Comm	PC	FP
78	ALE55	Address Line Enable 55	PC	FP
79	A10	Address bit 10	PC	FP
80	P20	Address bit 8	PC	FP
81	P21	Address bit 9		
82	PROG	Program Pulse	PC	FP
83	VDD	Power to PROM	PC	FP
84	A11	Address bit 11	PC	FP
85	X1	Processor Clock	PC	FP
86	TEST 0	Test 0 line	PC	FP
87	PROG/Ce/	Program 0 and Chip Enable	PC	FP
88	VCC	+5	PC	FP

*PS = Power Supply, CB = Control Board,

PC = Personality Card, FP = Front Panel PROM Socket.

TABLE 9-1. PERSONALITY CARD PIN LIST (Continued)

PIN	MNEMONIC	FUNCTION	SOURCE	DESTINATION
89				
90				
91	GND	Ground		
92	GND			
93				
94				
95	+40V	Power to Voltage reg.	PS	PC
96	+40V			
97				
98				
99	GND	Ground		
100	GND			

*PS = Power Supply, CB = Control Board,

PC = Personality Card, FP = Front Panel PROM Socket

CHAPTER 10

THE UPP-816 PERSONALITY CARD

The UPP-816 Personality Card contains the logic for programming and reading the contents of the following PROMs:

2716
2758
2758 S-1865.

The 2716 is an erasable PROM and is organized as a 2048 x 8 bit memory. The 2758 and the 2758 S-1865 are similar, except for the memory organization, which is 1024 x 8 bits.

Descriptions of the PROMs and appropriate programming and erasing information are contained in section 10.1. Section 10.2 discusses the major components of the UPP-816 Personality Card. It also discusses the sequence and the timing of events for both the read and the program operations. Section 10.3 provides a pin list for the UPP-816 Personality Card. This list includes the allocation and the function of each of the signals that appear on the pins of the Personality Card edge connector.

10.1 PROM CHARACTERISTICS

10.1.1 2716 PROM

The 2716 is a 2048 x 8-bit electrically programmable read only memory, designed for use in limited quantities and when fast turn-around and pattern experimentation are important. The PROM Programmer can program all 2048 words of the PROM in less than ten minutes. The 2716 can be erased by controlled exposure to high intensity ultraviolet light. After it is cleared, the 2716 can be programmed by the PROM programmer. The 2716 may be erased and reprogrammed as often as desired.

The 2716 is operated by standard power supply voltage of +5 volts. The data outputs of the 2716 are tri-state. Both inputs and outputs to the 2716 are TTL compatible during both read and program operations. The 2716 is shipped to the customer in an erased condition; that is, with ones (output high) in all memory locations. During programming, zeros (output low) are loaded selectively into the chip's memory locations. All eight bits of one word are programmed simultaneously by setting the desired bit pattern on the eight data pins of the 2716. The address of the word to be programmed is placed on the eleven address (pins) of the 2716. The selected memory location is then programmed by two pulsed signals applied to the chip's PROG (TTL-level) and VPP (+26V) pins. Section 10.2 includes detailed specifications of the signals used to program the PROMs.

10.1.2 2758 PROM

The 2758 PROM is similar to the 2716 except for the memory organization, which is 1 k x 8 bits. Pin 19 of the 2758 must be at logical low level (less than 0.8 V) for a normal read or program operation.

10.1.3 2758 S-1865 PROM

The 2758 S-1865 is similar to the 2716 except for the memory organization, which is 1 k x 8 bits. Pin 19 of the 2758 S-1865 must be at a logical high level (greater than 2.2 V) for normal read or program operations.

10.1.4 Programming

Use the following procedures to install the adapter (if one is used) and the PROM in the front panel socket of the PROM Programmer.

1. Install the UPP-816 in socket J2 on the mother board of the UPP-101, and either J1 or J2 of the UPP-102. See section 3.1.2 for installation instructions. These instructions are important because they point out potential errors,

and provide user cautions to prevent damage to the PROM and/or the Personality Card.

> CAUTION
>
> The regulator of the Personality Card may be damaged if the Personality Card is removed while power is on, or prior to discharging the 40 Volt input line. Consequently, it is mandatory to wait 60 seconds after system power off before removing the Personality Card.

2. For programming the 2758 S-1865, install the UPP-555 adapter. This adapter may also be used (optionally) for programming the 2758. See Chapter 11 for additional information on the UPP-555.

> CAUTION
>
> To prevent damage to the Personality Card observe the following precautions:
>
> - DO NOT insert the UPP-555 adapter in a socket that is driven by any personality card other than the UPP-816 or the UPP-865.
>
> - Be sure to insert the adapter so that the level on the adapter is at the top.

3. Insert the PROM to be programmed in the 24-pin socket, or the UPP-555 adapter, as appropriate.

> CAUTION
>
> Be sure to insert the PROM so that pin 1 is in the upper left corner of the socket, or the adapter, as appropriate.

5. Load the appropriate software for the PROM to be programmed. Refer to the applicable documentation list in section 11.1.

6. When using the UPP-555 to program the 2758 or the 2758 S-1856, take the following additional steps:

   a. Install the 16-pin shorting plug in the appropriate socket in the UPP-555. The type number of the PROM being programmed is marked below the appropriate socket.

   b. The UPP-555 has a shorting jumper that connects to two pins at the lower edge of the UPP-555 PC assembly, at the left of the 16-pin socket where the shorting plug is placed for the 2758 and 2758 S-1865 PROMs.

      - When programming the 2758, the two-pin jumper MUST BE INSTALLED.

      - When programming the 2758 S-1865, the two-pin jumper MUST BE REMOVED.

      The function of the two-pin jumper is to hold pin 19 of the 2758 at a logical low level during programming. When the jumper is removed for programming the 2758 S-1865, pin 19 is held at a logical high level.

10.1.5 ADDRESS BOUNDARIES

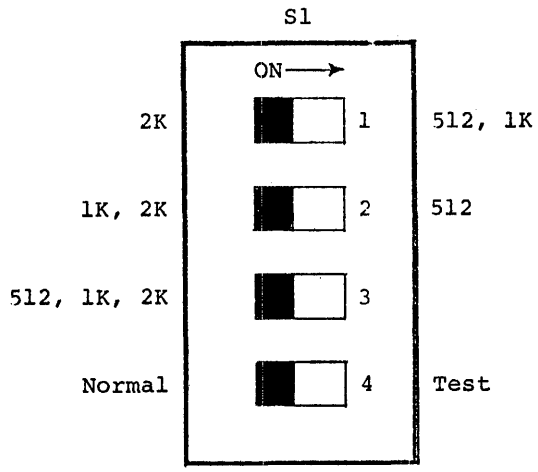
The address boundary limit of the UPP-816 Personality Card is normally set at 2047, which is the highest address of the 2716 PROM. When programming the 2758 or the 2758 S-1865, all addresses must be between 0 and 1023 (inclusive). If the boundary is exceeded (1024), no boundary error will be issued, and certain addresses may be over-written with erroneous data.

To set the address boundary on the UPP-816 for 1K boundary, slide switch S1-1 to the right (to the ON position), and switches S1-2 through S1-4 to the left (to the OFF position). Table 10-1 shows the switch settings for each address boundary, and Figure 10-1 shows the function of the switches on S1.

TABLE 10-1

PROM ADDRESS BOUNDARY SWITCH SETTINGS

PROM SIZE	S1 SWITCH NUMBER			
	1	2	3	4
2k	OFF	OFF	OFF	OFF
1k	ON	OFF	OFF	OFF
512	ON	ON	OFF	OFF



Note: The dark area on each switch denotes the position of the slide. Switch numbers are shown inside the switch area.

Figure 10-1. Switch Functions for S1. The Switch settings are shown for the 2716 PROM (2k boundary).

10.1.6 ERASING PROMS

The PROMs are packaged in a 24-pin dual in-line package with a transparent quartz lid. A silicon die is located under the transparent lid. Erasure of the PROM is accomplished by exposing the silicon die to ultraviolet light at a wavelength of 2537 Angstroms. The recommended integrated dose (the product of intensity and exposure time) is 10 W-sec/cm^2. Examples of the ultraviolet sources which can be used are the Model UV5 and the Model S-52 short-wave ultraviolet lamps manufactured by Ultra-Violet Products, Inc., (4115 Walnut Grove Avenue, San Gabriel, California). The lamps should be used without short-wave filters. Fifteen to twenty minutes exposure to the lamp, at a distance of one inch, will clear the PROM completely. Avoid unnecessary or prolonged exposures, which are potentially damaging to the PROM.

-- WARNING --

High intensity ultraviolet light can cause serious burns. Ultraviolet radiation can also generate potentially hazardous amounts of ozone. Observe the following precautions when using ultraviolet source to erase a PROM:

1) Never expose skin or eyes to the source directly.

2) Do not stare at an object which is under ultraviolet illumination. The light is invisible, but is nevertheless injurious to eye tissue.

3) Use the source only in a well-ventilated area.

10.2 FUNCTIONAL DESCRIPTION: UPP-816 PERSONALITY CARD

The UPP-816 Personality Card contains all of the logic needed to either program or read a word (8-bits) of a 2716 PROM. The Personality Card operates under the supervision of the Control Board (see Chapter 2). The PROM itself is plugged into the 24-pin socket on the front panel of the PROM Programmer. This socket is wired directly to the Personality Card.

The Control Board is responsible for supplying address and data information, and requesting that the Personality Card perform either a program or a read operation. The Personality Card, in turn, attempts to perform the requested operation, returns data to the Control Board, and notifies the Control Board of the success or failure of the operation.

Figure 10-2 is a functional block diagram of the UPP-816 Personality Card. It may be helpful to frequently refer to this diagram during the following discussion of the Personality Card. The names of the signals that appear in Figure 10-2 generally correspond to the names used on the schematic of the UPP-816 Personality Card (see Appendix B).

Communications between the Personality Card and the Control Board are handled by four parallel buses:

A) The MCS - 40 Bus includes the control, timing and data paths that are necessary for the operation of the 4040 processor on the Control Board and the two 4001 ROMs on the Personality Card.

B) The PROM Address bus provides the Personality Card with the 12-bit PROM address from the Control Board.

C) The PROM Write Data bus from the Control Board provides 8-bit data word to be programmed into the PROM by the Personality Card.

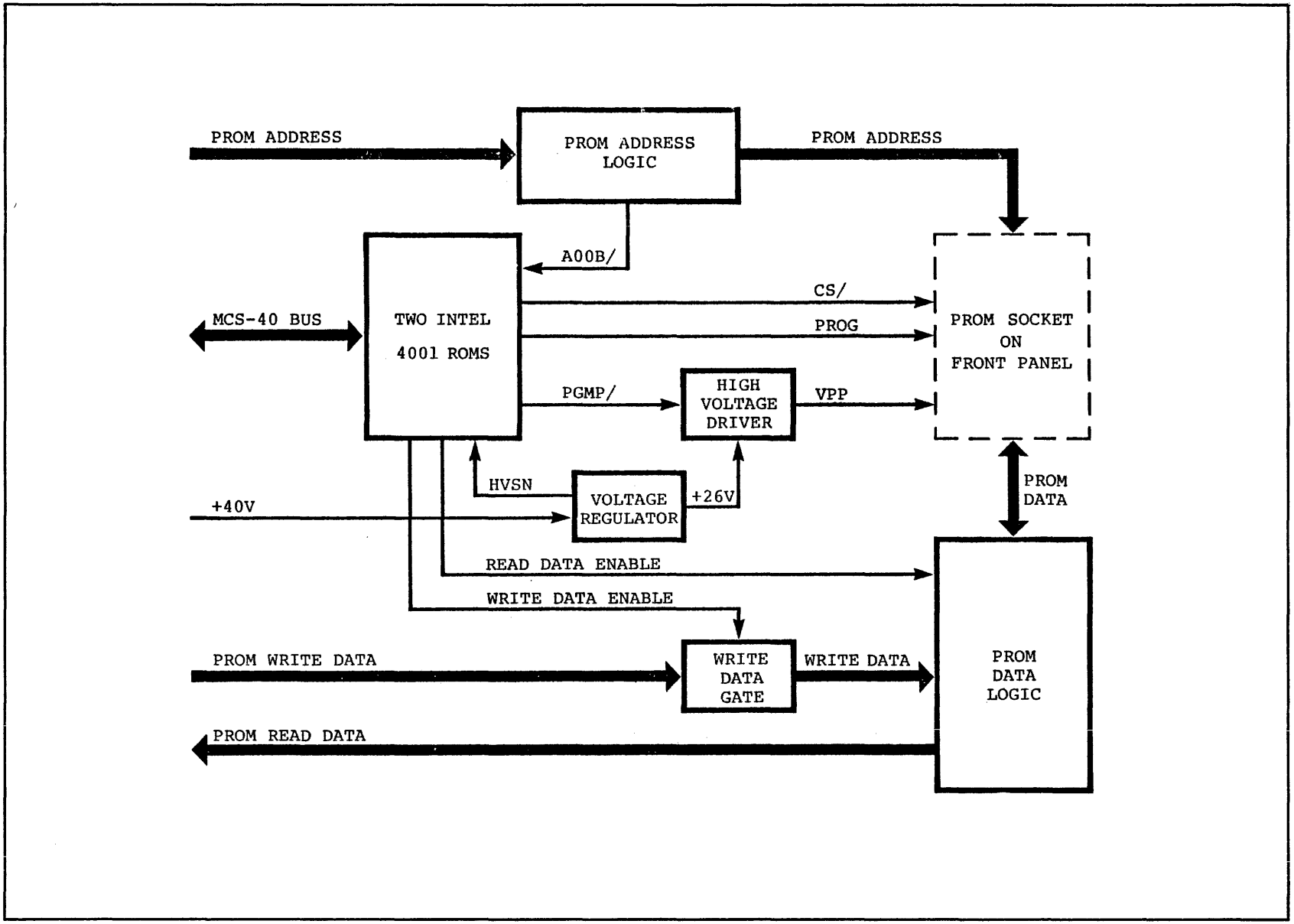


FIGURE 10-2. UPP-816 PERSONALITY CARD BLOCK DIAGRAM

D) The PROM Read Data bus returns the 8-bit data word in the selected PROM location to the Control Board.

There are six major components of the UPP-816 Personality Card as shown in Figure 10-2:

1) The PROM address logic examines the 12-bit address from the Control Board. If the 12-bit address exceeds the bounds of the selected PROM, the logic will activate the address out of bounds line (AOOB/) to port 1 of a 4001 ROM (A12).

2) The two Intel 4001 ROMs are a part of the MCS - 40 (the processor itself is located on the Control Board). The ROMs contain instructions for the MCS - 40 that will effect the reading or programming of a 2716 PROM. The MCS - 40 interacts with the Personality Card through the I/O ports on the two ROM chips. The MCS - 40 selects the 2716 for a program or read operation by generating the chip select (CS/) signal at I/O port 1 on the 4001 ROM at A6. The program pulse (PGMP) that enables the high-voltage PROG driver is output from port 3 of the ROM at A6, while the write data is enabled by the output from port 0 on the same ROM.

3) The Voltage Regulator supplies the +26V (approximate) operating voltages to the PROM at VPP (pin 85). The +26V regulator has two protective circuits. One is a current limit of 300 mA (set by R18 and R19) to protect the regulator and the PROG driver against shorts at the PROM socket. The other is a crow-bar circuit that will short out the +40V supply, should the regulator fail.

4) The Write Data Gate allows the PROM Write Data from the Control Board to move on to the PROM during a program operation. The gate is closed except during a program operation. It is controlled by the Write Data Enable line from port 0 of a 4001 ROM (A6).

5) The PROM Data Logic handles the flow of data to and from the PROM. During a program operation the PROM Write Data is passed on to the PROM through open collector drivers. During a read operation, the Read Data Enable line from port 3 of a 4001 ROM (A12) will signal the PROM Data Logic. This will allow the PROM Read Data to be passed back to the Control Board.

6) The High Voltage Driver performs the actual PROM programming. The VPP line (pin 85) is driven to +26V (approx.) during a programming operation (i.e., when PGMP/ goes low). About 1 msec after VPP rises to +26V, PGMP/ causes the PROG line (pin 82) to rise to approximately +5V. During read operations PROG and VPP are grounded.

The remainder of this section will describe how the above functional blocks interact to perform the two operations: program and read. There are two distinct locations in the ROM on the UPP-816 Personality Card that are the entry points to which the MCS - 40 branches: one entry point for a program operation and one for a read. When the Personality Card receives control it assumes the PROM Address is available on the address bus. In the case of a program operation it also assumes the PROM Write Data is on the data bus. In either case the first step is to check for an address error.

The address check is a matter of testing the Address Out Of Bounds signal (AOOB/). If the signal indicates an address error the Personality Card aborts the operation and returns control to the Control Board. If the address is valid, the operation continues.

PROM READ DATA:

In the case of a read operation there is little left that needs to be done, since the static conditions of the Personality Card present the selected PROM data word to the PROM Data Logic. All the MCS - 40 needs to do is turn on the Read Data Enable line from the 4001 ROM (A12) output port 3. When this is done the PROM Read Data is returned to the Control Board. The Personality Card has then completed the read operation.

PROM PROGRAM DATA:

The program operation is only slightly more involved. After the address has been checked the program operation begins. The sequence of events is as follows:

1) The MCS - 40 checks to see that the Voltage Regulator is receiving +40 volts from the Power Supply. If the signal HVSN from the Voltage Regulator to ROM (A12) port 2 is true, then the 40 volts is available. If not, the program operation is aborted, and control returns to the Control Board.

2) The output from ROM (A12) port 1 causes CS/ to be pulsed as shown on the timing diagram, Figure 10-3.

3) The signal Write Data Enable is switched from low to high allowing the PROM Write Data to be presented to the PROM.

4) The signal PGMP/ is switched from high (its read level) to low, causing the high voltage driver to drive VPP to +26V. Approximately 1 msec. later, PGMP enables PROG to rise to +5V.

5) The Personality Card now holds these conditions constant for 50 msec., while the data is electrically programmed into the PROM.

6) When the 50 msec. have elapsed, the signal PGMP/ is switched back to high, removing the programming pulse PROG from the PROM and grounding VPP.

7) The signal Write Data Enable is switched back to low, removing the PROM Write Data from the PROM.

8) The 4001 ROM (A12) port 1 switches CS/ back to the read level (low).

9) The MCS - 40 verifies the programming operation by reading the programmed PROM location and comparing it to the expected value. If the programming was not successful, the program and verification sequences are repeated. If the PROM location is still not correctly programmed, an error is indicated and control is returned to the Control Board.

10.3 PIN LIST: UPP-816 PERSONALITY CARD

The UPP-816 Personality Card communicates with the Control Board and the PROM socket on the front panel through a 100-pin double-sided PC edge connector. Pin allocations and designated signal functions for this 100-pin connector are given in Table 10-2.

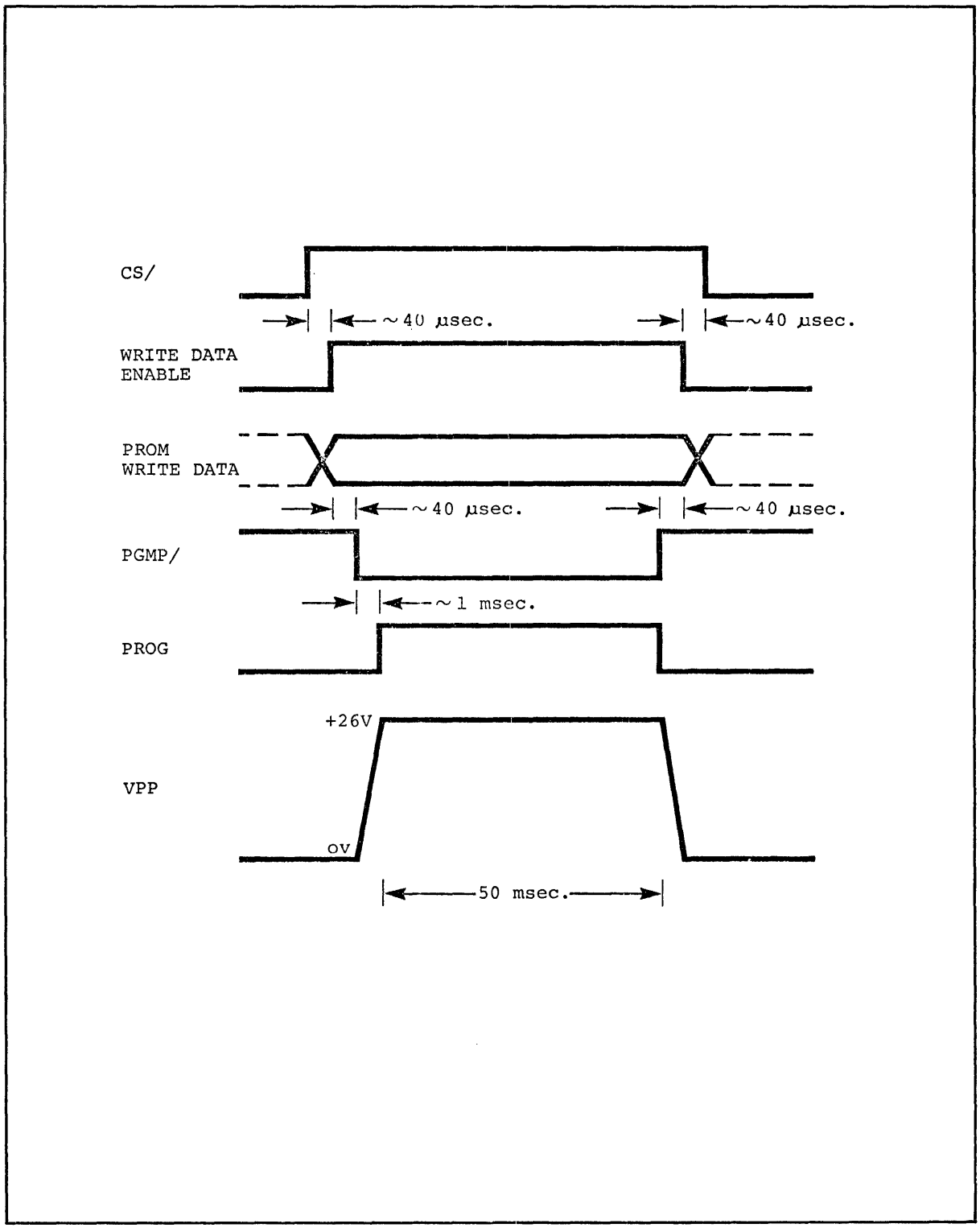


FIGURE 10-3. UPP-816 PERSONALITY CARD PROGRAM TIMING

TABLE 10-2

UPP-816 PERSONALITY CARD PIN LIST

PIN	MNEMONIC	FUNCTION	SOURCE	DESTINATION
1	GND	Ground		
2	GND			
3				
4				
5	VCCH	Power inputs (5.85 VDC)	PS	PC
6	VCCH			
7	VCCH			
8	VCCH			
9	GND	Ground		
10	GND			
11	-10 V	Power inputs	PS	PC
12	-10 V			
13	GND	Ground		
14	GND			
15				
16	BD SEN/	Board sense	PC	CB
17				
18				
19	CONTROL	Control bit		
20				
21	WRITE DATA 0	Write data bus from Control Board	CB	PC
22	WRITE DATA 1			
23	WRITE DATA 2			
24	WRITE DATA 3			
25	WRITE DATA 4			
26	WRITE DATA 5			
27	WRITE DATA 6			
28	WRITE DATA 7			
29	PROM ADDRESS 0	PROM address bus from Control Board	CB	PC
30	PROM ADDRESS 1			
31	PROM ADDRESS 2			
32	PROM ADDRESS 3			
33	PROM ADDRESS 4			
34	PROM ADDRESS 5			
35	PROM ADDRESS 6			
36	PROM ADDRESS 7			
37	PROM ADDRESS 8			
38	PROM ADDRESS 9			
39	PROM ADDRESS 10			
40	PROM ADDRESS 11			
41	D0	MCS - 40 data bus (bi-directional)	CB/PC	PC/CB
42	D1			
43	D2			
44	D3			
45	02	MCS - 40 clock signals	CB	PC
46	01			
47	CM-ROM	ROM bank enable	CB	PC
48				
49				
50	SYNC	MCS - 40 synchronization		

PS=power supply CB=Control Board PC=UPP-816 Personality Card
FP=Front Panel (PROM socket)

TABLE 10-2 (Continued)

PIN	MNEMONIC	FUNCTION	SOURCE	DESTINATION
51	RESET	MCS - 40 reset	CB	PC
52	PROM RD DATA 0/	Data read from PROM	PC	CB
53	PROM RD DATA 1/			
54	PROM RD DATA 2/			
55	PROM RD DATA 3/			
56	PROM RD DATA 4/			
57	PROM RD DATA 5/			
58	PROM RD DATA 6/			
59	PROM RD DATA 7/			
60				
61	A7	Address to PROM	PC	FP
62	A6			
63	A5			
64	A4			
65	A3			
66	A2			
67	A1			
68	A0			
69	01	PROM data (bi-directional	PC/FP	FP/PC
70	02			
71	03			
72	VSS	Power to PROM		
73	VSS			
74	VSS			
75	VSS			
76				
77	04	PROM data (bi-directional)	PC/FP	FP/PC
78	05			
79	06			
80	07		PC	FP
81	08			
82	PROG	TTL program pulse		
83	A10	Address bit 10		
84				
85	VPP	High-volt. program pulse	PC	FP
86	A9	Address to PROM	PC	FP
87	A8			
88	VCC	Power to PROM	PC	FP
89				
90				
91	GND	Ground		
92	GND			
93				
94				
95	+40V	Power to Voltage Regulator	PS	PC
96	+40V			
97				
98				
99	GND	Ground		
100	GND			

PS=Power Supply CB=Control Board PC=UPP-816 Personality Card
FP=Front Panel (PROM socket)

CHAPTER 11

UPP-555 UNIVERSAL PROM-PROGRAMMER ADAPTER

FOR BIPOLAR AND UV ERASABLE PROMS

The UPP-555 Adapter is used with the UPP-101 or UPP-102 Universal PROM Programmer to program and verify a number of bipolar and ultra-violet erasable PROMs.

The bipolar PROMs, which utilize the highly reliable polycrystalline silicone fuse and Schottky barrier diode technology, include the 3604 AL, 3604L-6, 3608, and 3628. The 2758 EPROM with N-channel silicon gate FAMOS technology is also included.

The UPP-101 and UPP-102 are both INTELLEC System Peripherals requiring personality cards compatible with the PROM being programmed. These personality cards are specified in Table 11-1. Either a paper tape or a floppy diskette INTELLEC system may be used with the Universal PROM Mapper (UPM) Program to generate the data patterns for programming the PROM.

11.1 APPLICABLE DOCUMENTATION

The following documents are required to program the PROMs serviced by the UPP-555 Adapter:

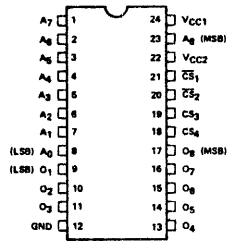
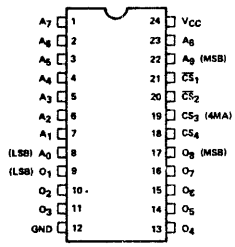
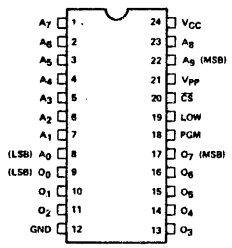
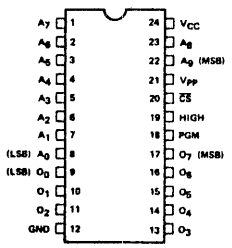
General:

1)	Universal PROM Mapper (UPM) Operator's Manual	98-236
2)	MDS UPP Diagnostic User's Guide	98-460

Paper Tape System:

3)	INTELLEC MDS Hardware Reference Manual	98-132
4)	INTELLEC 800 MDS Operator's Manual	98-129

TABLE 11-1. UPP-555 ADAPTER PROM SET

PROM TYPE	DESCRIPTION	UPP-101 or UPP-102 PERSONALITY CARD	PIN CONFIGURATION
3604L-6 or 3604AL	512 x 8	UPP-865	
3608 or 3628	1K x 8	UPP-865	
2758	1K x 8	UPP-816	
2758 S1865	1K x 8	UPP-816	

Floppy Diskette Operating System:

5)	MDS DOS Hardware Reference Manual, or	98-212
6)	MDS DDS Double Density Diskette System Hardware Reference Manual	98-422
7)	ISIS-II System User's Guide	98-306

-- NOTE --

The UPP-101 and UPP-102 are designed for use with the INTELLEC Development System only. All operations are controlled by the UPM program.

11.2 GENERAL

The UPP-555 Adapter contains a 24-pin zero insertion pressure (ZIP) socket which is used to program the PROMs. Many of the signals from the UPP-101 or UPP-102, such as address and data lines, are common to all PROM types programmed with this adapter. These signals are bused directly through to the ZIP socket. However, those signals which are not common are routed to a set of 16-pin IC sockets, through which the signals are conditioned and/or routed to the PROM ZIP programming socket. A 16-pin jumper block is required to connect the signals to the ZIP socket.

11.3 OPERATING INSTRUCTIONS

Operation of the UPP-555 with the UPP-101 or UPP-102 and the INTELLEC Development System is quite simple, as follows:

1) Insert the 16-pin jumper block into the program socket for the type of PROM to be programmed. The PROM identification is etched on the UPP-555 Adapter Card next to each socket. In the case of the 2758 an additional 2-pin shorting plug must be plugged into the contacts labelled "S" located to the left of the 2758 label. If the 2758 S-1865 variation

is programmed, the 2-pin shorting plug must be removed. For other PROM types, the 2-pin shorting plug installation is a "DON'T CARE" condition.

> -- CAUTION --
>
> Check that the jumper block is inserted into the proper socket, and that only one 16-pin jumper block is inserted at one time. Inserting the jumper block into the wrong socket, or inserting two or more jumper blocks at one time, may damage the PROM and/or the equipment.

2) Check that the correct personality card (Column 3 of Table 11-1) is inserted into the UPP-101 or UPP-102.

3) Plug the UPP-555 Adapter into the UPP-101 or UPP-102 24-pin front panel ZIP socket. Note that the UPP-101 has both a 16-pin and a 24-pin ZIP socket, and that the UPP-102 has two 24-pin sockets.

4) Load the programming data into the INTELLEC System using the UPM program. Execute the program according to the INTELLEC System documentation.

11.4 THEORY OF OPERATION

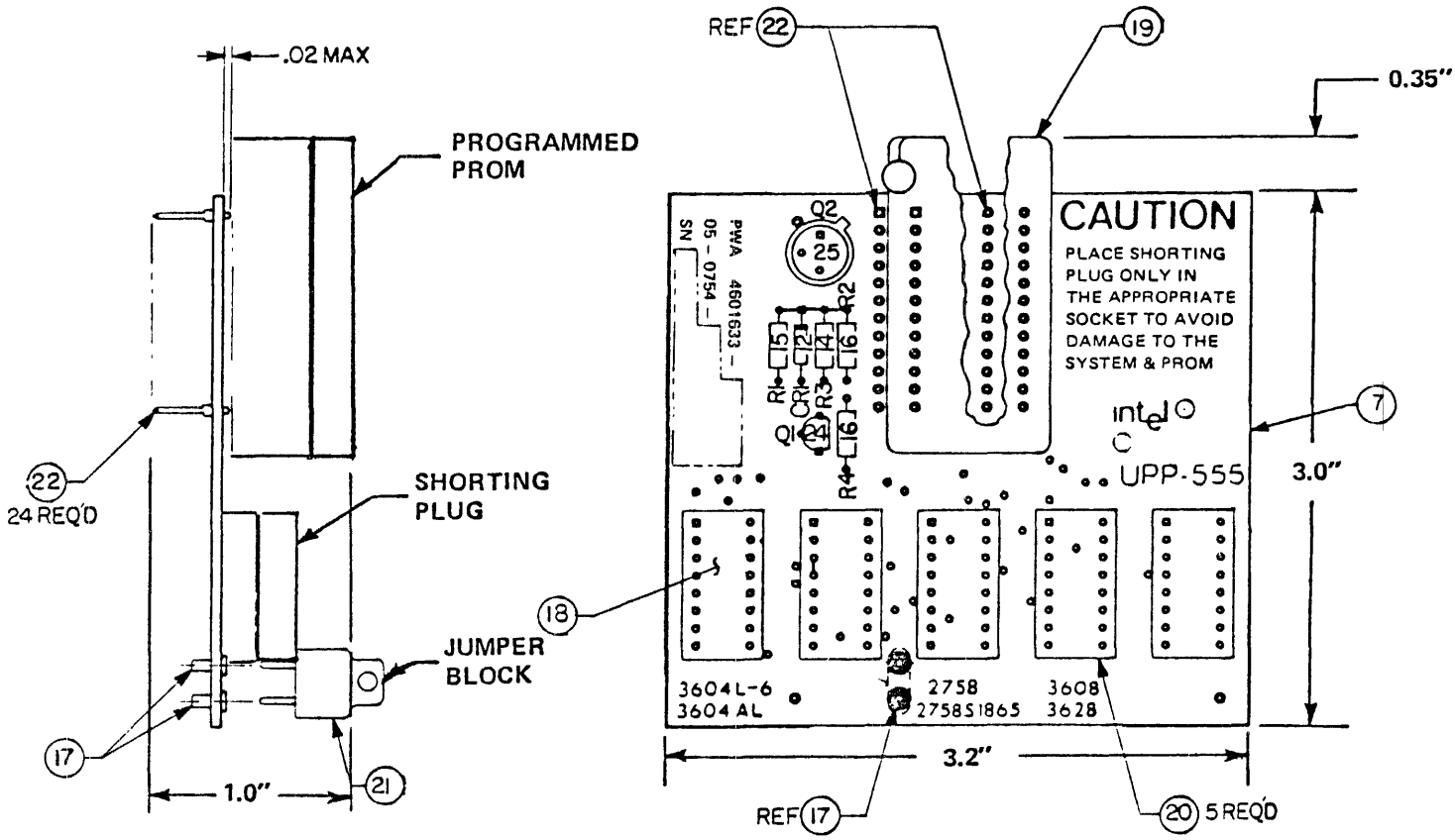
The UPP-555 UNIVERSAL PROM ADAPTER extends the capabilities of the UPP-101 and UPP-102 INTELLEC peripheral PROM programmers to a series of new PROMs which are similar to PROMs developed previously. By adding signal conditioning circuitry and "patching" capabilities to the adapter, existing personality cards are retained at a significant cost savings to the user. Although six PROM types may be programmed with the UPP-555, only one ZIP socket and one jumper

block are required.* Five clearly-labeled 16-pin IC sockets selectively switch the inputs to ZIP socket pins 18 through 24, depending on the specific requirements of the individual PROM types. Since the same jumper block is used with all the IC sockets, the possibility of connecting the wrong signals to the PROM being programmed is minimized. Actual signal connections are summarized in Table 11-2, and may be traced out in the enclosed schematic diagram (01-0754-000). Physical layout is shown in Figure 11-1.

*The 2758 requires an active Low Enable on pin 19, which is accomplished with a 2-pin shorting plug. The 2758 S 1875 is an identical part except that it requires an active High Enable on pin 19, which is accomplished by removing the shorting plug. This additional plug has no effect on the programming of other devices.

TABLE 11-2. SIGNAL SUMMARY

PROM TYPE	DIRECT CONNECTIONS FROM UPP TO ZIP PIN	SIGNALS REROUTED BY ADAPTER					
		FROM (UPP)	TO (ZIP)	NAME (ZIP)	PIN (ZIP)	NAME	COMMENTS
3604L-6 3604AL	1-23				24	V_{CC}	+5V to 12.5V pulse to PROGRAM. OPEN or FLOATING for READ or VERIFY.
2758	1-18, 20-24				19	A 11	Forced LOW (2-pin jumper required).
2758 S1865	1-18, 20-24				19	A 11	Forced HIGH (Zenered to 5.1V).
3608 3628	1-17, 21, 23, 24	20 19 18 22	22 18 19 —	A 9 CS4 CS3 NC	20	CS_2	GROUNDED (Enabled).



Parts List, 05-0754-000					
ITEM NO.	PART NUMBER	DESCRIPTION	UNIT MEAS	QTY	REFERENCE DESIGNATOR
1	01-0754-000	SCHEMATIC, UPP-555	/	REF	
2	03-0754-000	ARTMASTER, UPP-555	/	REF	
7	04-0754-000	PCB, FAB	EA	1	
12	41-0001-027	DIODE, ZENER, IN751A	EA	1	CR1
14	43-0005-301	RES, 300 Ω, ±5%, 1/4W	EA	1	R3
15	43-0005-471	RES, 470 Ω, ±5%, 1/4W	EA	1	R1
16	43-0005-102	RES, 1K Ω, ±5%, 1/4W	EA	2	R2, R4
17	46-0016-005	JACK, SOLDER MOUNT	EA	2	
18	40-0009-000	JUMPER BLOCK	EA	1	
19	46-0019-033	SOCKET, ZIP DIP II	EA	1	
20	46-0019-001	SOCKET, I.C., 16 PIN	EA	5	
21	46-0020-004	PLUG, SHORTING, 16 PIN	EA	1	
22	46-0021-030	STAKE PIN	EA	24	
24	41-0002-038	TRANSISTOR, 2N3904	EA	1	Q1
25	41-0002-039	TRANSISTOR, 2N3467	EA	1	Q2

FIGURE 11-1. PHYSICAL LAYOUT

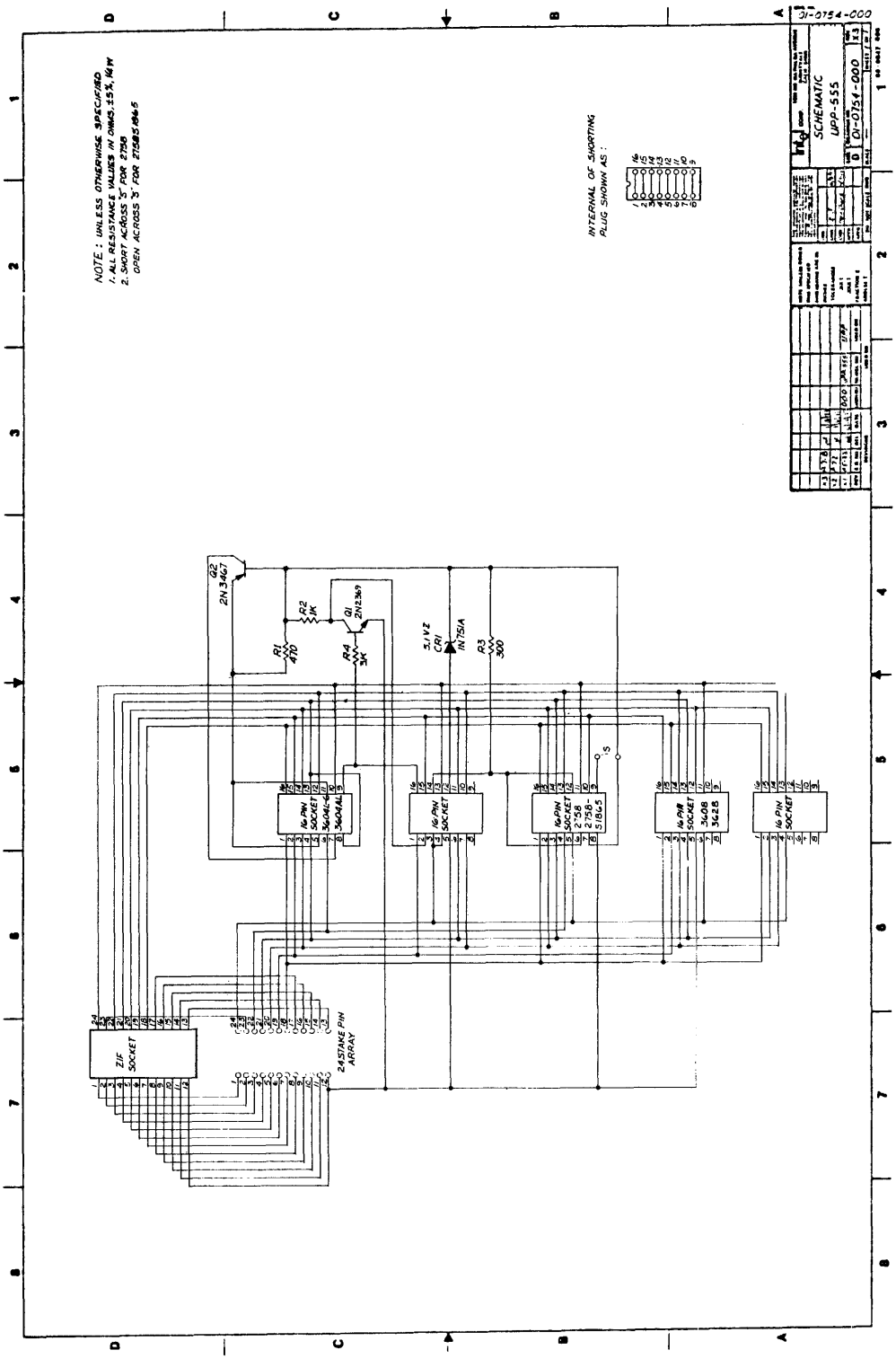


FIGURE 11-2. SCHEMATIC DIAGRAM

CHAPTER 12

THE UPP-865 PERSONALITY CARD

The UPP-865 Personality Card contains the logic for both programming and reading any of the bipolar PROMs manufactured by Intel Corporation, with a single exception of the Intel 3601. The UPP-865 can program the Intel 3604, 3624, 3604A and 3624A PROMs without an adapter; all other PROMs require the use of an adapter. The PROMs that can be used with the UPP-865 and the various adapters are listed in Table 12-1.

The UPP-865 is a direct replacement for the UPP-864, which is described in Chapter 5. The UPP-865 uses an improved programming algorithm that increases programming yield and also minimizes programming time.

The PROMs listed in Table 12-1 are all programmed using the same basic programming algorithm, even though the various devices have different word lengths, access time, amount of storage, and package sizes (e.g., 24, 18 and 16 pin DIP).

Section 12.2 discusses the major components of the UPP-865 Personality Card. It also discusses the sequence and timing of events for programming and read operations.

Section 12.3 contains programming procedures for use with the UPP-865 and the adapters listed in Table 12.1.

Section 12.5 contains the calibration adjustment procedures for the UPP-865. Section 12.6 provides a pin list for the UPP-865 Personality Card. This list includes the allocation and function of each of the signals that appear on the pins of the Personality Card connector.

TABLE 12-1

UPP-865 PERSONALITY CARD

DEVICE SELECTION

PROM	PINS	NO. OF BITS	ORGANIZATION	MAXIMUM ACCESS TIME (ns)	ADAPTER
3602, 3602A	16	2048	512 x 4	70	UPP-562
3604, 3604A	24	4096	512 x 8	70	NOT REQUIRED
3604L-6 3604AL	24	4096	512 x 8	90	UPP-555
3605	18	4096	1k x 4	70	UPP-565
3608	24	8192	1k x 8	80	UPP-555
3621	16	1024	256 x 4	70	UPP-562
3622, 3622A	16	2048	512 x 4	70	UPP-562
3624, 3624A	24	4096	512 x 8	70	NOT REQUIRED
3625	18	4096	1k x 4	70	UPP-565
3628	24	8192	1k x 8	80	UPP-555

12.1 INTRODUCTION

The UPP-865 uses a specially developed programming algorithm that is designed for use with monolithic, bipolar, high speed, Schottky-clamped TTL memory arrays with polycrystalline silicon fuses. All PROMs that are programmable with the UPP-865 are manufactured with all outputs high. Logic low levels are electrically programmed in selected bit locations by the application of a series of programming pulses that blow the selected fuse. Each output that is to be changed from a high to a low (logic one to logic zero) is programmed individually in a sequence of four bits per nibble. To program, the VCC input of the PROM is pulsed at 12.5 Volts. Simultaneously, a 5mA current pulse is applied to the output of the bit to be programmed. The other outputs of the PROM are allowed to float. Each of four bits in the selected nibble are pulsed in succession; and then the sequence is repeated until all four bits are programmed. Prior to each pulse, the output is read to determine whether it has been programmed. After all fuses in the nibble are blown, the UPP-865 applies another 128 pulses to ensure the complete oxidation of the fuse material. Finally, at the end of the series of 128 pulses, the current is applied to all outputs for an additional 2.5 milliseconds. For PROMs with 8-bit organizations, the lower nibble is programmed first, and then the upper nibble.

12.2 FUNCTIONAL DESCRIPTION: UPP-865 PERSONALITY CARD

The UPP-865 Personality Card contains all of the logic needed to either program or read a word of any of the PROMs listed in Table 12-1. The Personality Card operates under the supervision of the control board, which is described in Chapter 2. The PROM itself is plugged into the front panel socket, or an adapter which is in turn plugged into the front panel socket of the PROM programmer (UPP-101 or UPP-102). The front panel socket is wired directly to the personality card.

The control board is responsible for supplying address and data information, and requesting the personality card to perform either a program or a read operation. The Personality Card, in turn, attempts to perform the requested operation, returns data to the control board, and notifies the control board of the success or failure of the operation.

Figure 12-1 is a functional block diagram of the UPP-865 Personality Card. It may be helpful to refer to this diagram frequently during the following discussion. The names of the signals that appear in Figure 12-1 conform to the names used on the schematic diagram of the UPP-865 Personality Card, which is contained in appendix B (see the five sheets of drawing number 2001508). Note that the major blocks shown in the block diagram of Figure 12-1 contain a numeral in the upper right corner of the block; this numeral corresponds to the sheet number of the schematic diagram, for fast reference.

Communications between the Personality Card and the control board are handled by four parallel buses:

A. The MCS-40 bus, which includes the control, timing and data paths that are necessary for the operation of the 4040 processor on the control board and the two 4001 ROMs on the Personality Card.

B. The PROM address bus, which provides the Personality Card with the 12-bit PROM address from the control board.

C. The PROM write data bus from the control board, which provides the 8-bit data word to be programmed into the PROM by the Personality Card.

D. The PROM read data bus, which returns the 8-bit data word in the selected PROM location to the control board.

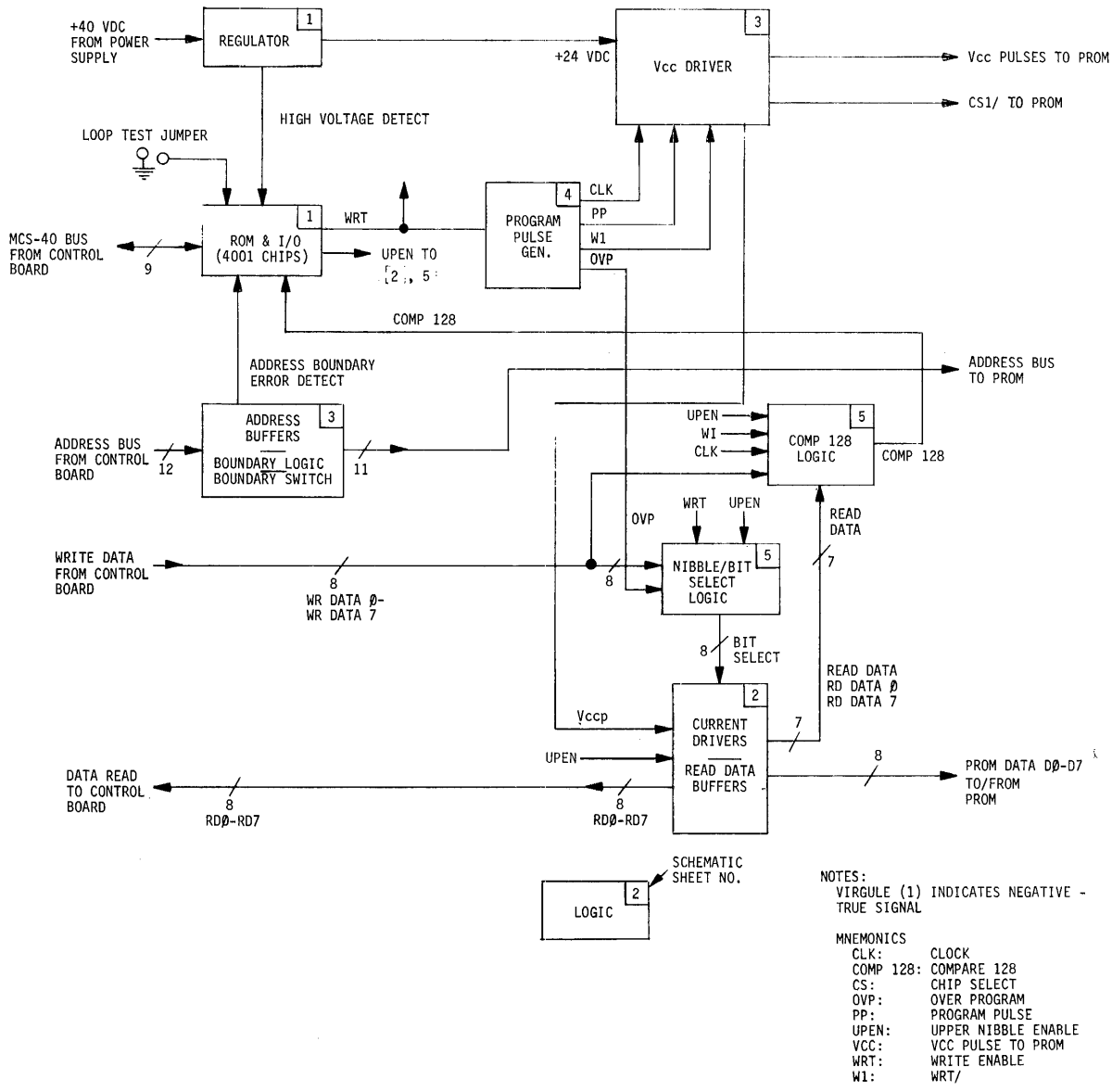


FIGURE 12-1. UPP-865 PERSONALITY CARD FUNCTIONAL BLOCK DIAGRAM

There are eight major components of the UPP-865 Personality Card which are shown in Figure 12-1:

A. The PROM address buffers and boundry logic buffer the address bits from the control board and output the bits to the PROM being programmed. In addition, a logic circuit with a manually-set switch checks the upper four address bits for an address boundary error. Since the UPP-865 can be used to program PROMs with up to 2048 words, all addresses must be within the range of zero to 2047. Switch S1 on the Personality Card is set for the highest address of the PROM being programmed: 255, 511, 1023, or 2047. In all cases, the most significant address bit (PA11) must be zero. Bits PA8, PA9, and PA10 are switched into the boundary error detect gate (A15) by switch S1, as a function of the organization of the PROM being programmed. If the address is out of range, the logic generates an error signal on the boundary error line. The PROM address bits are buffered by open-collector drivers A16 and A24.

B. The two Intel 4001 chips, which combine both ROM and I/O, are part of the MCS-40 system. The processor itself is located on the control board. The ROM contains the instructions that affect the reading or programming of the device. The MCS-40 interacts with the Personality Card through the I/O ports on the two ROM chips.

C. The voltage regulator receives an unregulated +40 Volts from the power supply, and delivers a regulated +24 Volts to the program pulse logic circuit. The voltage regulator is a series-pass circuit with a current limit circuit that limits at 1.2 Amperes.

The regulator has an overvoltage protection circuit: if the regulator output rises above 33 Volts, an SCR switches and grounds the +40 Volt unregulated input through a 1-Ohm resistor. The shorted 40 V input blows the 1-Ampere fuse on the UPP power supply.

The regulator also has a voltage sense circuit. If the 40 Volt input is not present, the voltage sense circuit generates an output that goes to the ROM input port. The software then generates a "hardware error" message.

D. The program pulse generator circuit provides the following signals:

1. A train of clock (CLK, CKL/ and DCLK) pulses. The width of these pulses is about 400 nanoseconds. The clock pulse train is initiated when the program pulse generator receives the write (WRT) signal from the 4001 ROM-I/O chips (shown on sheet 1 of the schematic diagrams). The duration of the clock pulse train is 400 milliseconds. DCLK is the same frequency as CLK, but it is delayed by the propagation time of A14 and A2.

2. A train of variable-width pulses (PP and PP/). PP is used for controlling the PROM programming pulses. The PP pulses are triggered by the CLK/ pulses, so that the trailing edge of each clock pulse is followed immediately by the leading edge of the PP pulse. The duration of the PP and PP/ pulse train is 400 milliseconds.

3. The WRT signal, which is inverted to become the W1 signal.

4. The overprogram pulse (OVP), which is generated after the Comp 128 signal is active.

All of the above signals--except for OVP--go to the VCC driver circuit.

E. The VCC driver circuit receives W1, PP and CLK from the program pulse generator. It also receives +24 V dc from the regulator. The PP pulses drive Q21 and Q22 to generate a series of 400 millisecond VCC pulse trains, which go to the VCC input of the PROM. The timing characteristics of the VCC pulse train are described in section 12.2.2. The baseline of the VCC pulse train is at 4.5 V; peak pulse amplitude is +12.5 V. When the PROM is not being programmed, the steady-state VCC level is +5 V dc.

The CLK/ and the DCLK signals are gated by the VCC driver to form the chip select signal (CS1/), which goes to the PROM. The PROM is selected for the duration of the CLK/ and DCLK signals, prior to each programming pulse. When the chip is selected, the contents of the selected PROM address is read by the personality card and compared to the write data.

F. The Comp 128 logic generates a COMP 128 (compare 128) pulse that goes to the 4001 ROM-I/O chip A22. The Comp 128 logic compares the input data on the write data bus to the data bits that are read back from the PROM during each chip select pulse. The compare 128 logic also receives clock pulses, W1, and UPEN (upper nibble enable) signals. When all four bits on the write data bus agree with the bits that are read from the PROM, a counter in the Comp 128 logic circuit is incremented. After 128 increments (not necessarily successively), the logic generates a COMP 128 signal that returns to the program

pulse logic and the MCS-40. The program pulse logic then generates the over-programming signal (OVP), which is used to over-program all four bits in the nibble simultaneously. The software program then waits for 2.5 milliseconds before turning off the WRT signal.

G. The nibble and bit select logic is used to select bits that will be programmed by the VCC and the current pulses. The nibble logic selects either the upper or lower nibble in the byte as a function of the UPEN signal from the 4001 ROM-I/O circuit. The bit select logic selects each of the four bits in the selected nibble in sequence. Thus, all four bits are selected consecutively in one complete cycle. The bit select outputs go to the current drivers.

H. The current driver circuits perform the read and program functions. During the read operation, they read the PROM data, and return this data on a buffered (tri-state) data read bus to the control card. This circuit also provides the PROM read data to the Comp 128 circuit between programming pulses. During a program operation, the current drivers deliver a 5 mA current pulse to the selected PROM output, as directed by the outputs of the bit select logic. The current drivers have a clamp diode that prevents the output voltage from exceeding the level of the VCC pulse.

The remainder of this section describes how the functional blocks interact to perform the read and write operations. There are two distinct locations in the ROM on the UPP-865 Personality Card that are the entry points to which the MCS-40 branches: one entry point for a program operation and one for a read operation. When a Personality Card receives control, it assumes that a PROM address is available on the address bus. In the case of a program operation, it also assumes that the PROM write data is on the data bus. In both cases the first step is to check for both address and high voltage errors.

When the address boundary error signal at the ROM input port is true, the selected address exceeds the boundary set by switch S1. The Personality Card then aborts the operation and returns the control board. If the address is valid, the operation continues.

The program also checks for the presence of the unregulated +40 Volt power supply input by sampling bit 3 of the ROM input port. If the signal is true, the operation continues.

12.2.1 PROM READ OPERATION

For a read operation the only requirement is that the tri-state output buffers must be enabled. The static conditions of the Personality Card present the selected PROM data word to the output buffers. The MCS-40 enables the output buffers with the UPEN (upper nibble enable) signal, and the PROM read data is returned to the control board. The Personality Card has then completed the read operation.

12.2.2 PROM PROGRAM OPERATION

All PROM program operations performed by the UPP-865 are organized in four-bit nibbles. The lower nibble (least significant bits) is programmed first, and, if it is programmed successfully, then the upper nibble is programmed (providing that the PROM has 8 bits).

To program a nibble, the personality card supplies an address, a series of VCC pulses to the VCC input of the PROM, a series of 5 milliampere current pulses to the outputs being programmed, and a series of chip select pulses (CS/). These pulse trains are shown in Figure 12-2.

VCC Pulses. The VCC pulse train consists of a series of variable-width pulses that continue for 400 milliseconds. Each pulse train has the following characteristics (see also Figures 12-2 and 12-3):

a. The initial pulse width is 200 nanoseconds.

b. Pulse width increases linearly for 180 milliseconds.

c. After 180 milliseconds, the pulse width is 8 microseconds.

d. The 8 microsecond pulses continue for an additional 220 milliseconds.

e. The quiescent period between pulses is 1.8 microseconds.

f. After a total of 400 milliseconds, the PP pulses terminate, which concludes the 400 millisecond programming pulse cycle.

Peak pulse amplitude is 12.5 ± 0.5 Volts.

If the nibble is programmed successfully during the VCC pulse train (i.e., having 128 good compares), the VCC will stay in overprogram mode (at 12.5 V) for 2.5 milliseconds, and then conclude the programming of the nibble.

Current Pulses. All bipolar PROMs are manufactured with all outputs high; i.e. each bit equals a logical one. Programming a bit blows a polycrystalline fuse, and the bit becomes a zero. The output to be programmed is driven with a 5 milliampere current pulse that is concurrent with and the same width as the VCC pulse. The 5 milliampere pulse blows the fuse. During the programming sequence all PROM outputs in the nibble being programmed are driven in succession with current pulses. The output of the least significant bit in the lower nibble is pulsed first, followed by the second output etc. After the fourth output is pulsed, the cycle repeats until all four outputs are properly programmed, or for 400 milliseconds, which-

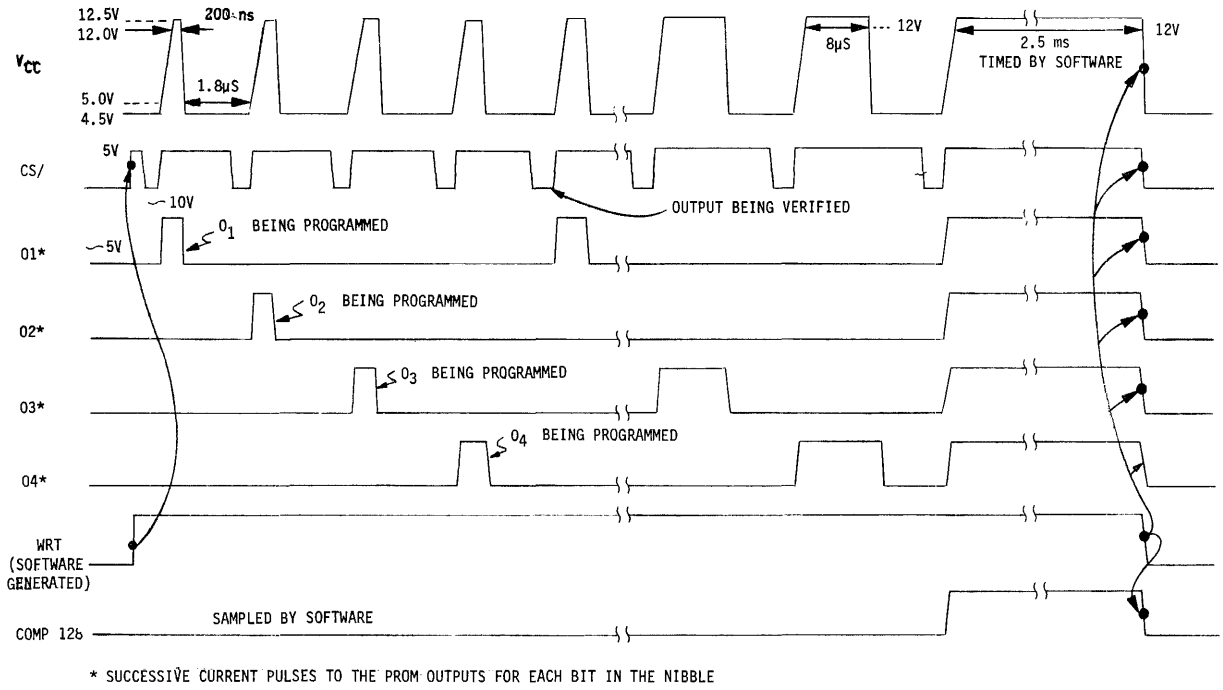


FIGURE 12-2. PROGRAMMING PULSE TIMING DIAGRAM

FIGURE 12-2. PROGRAMMING PULSE TIMING DIAGRAM

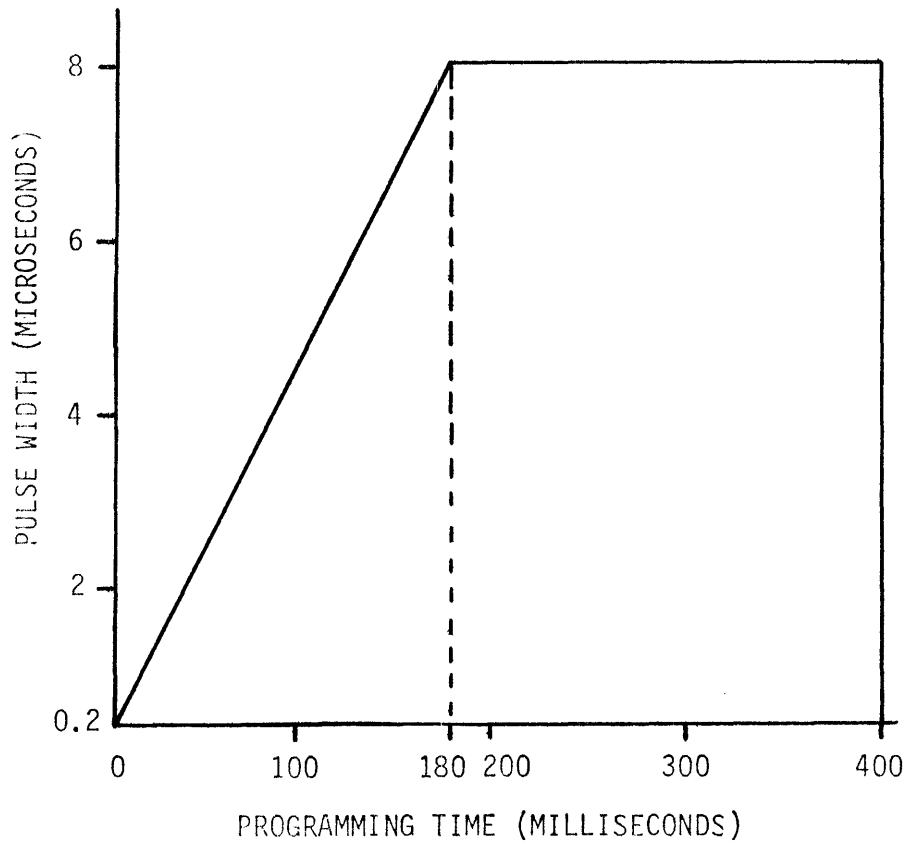


FIGURE 12-3. PULSE WIDTH VS. PROGRAMMING TIME

ever comes first. If the outputs are not programmed within a 400 milliseconds cycle, the entire sequence is repeated up to a maximum of four times. If the programming process is not successful by the end of the fourth cycle, the program is aborted, and an error status is issued.

Chip Select Pulses. During programming the chip select signal (CS/) is held at +5 Volts, so that the chip is not selected. Prior to each of the VCC and programming output pulses, the CS/ signal goes low and the PROM is read. Each output bit is latched in sequence, and if the chip is programmed properly, then the four bits being programmed agree with the input nibble. Each time there is an agreement, it increments the counter circuit in the Comp 127 logic (Figure 12-1). After 128 successful comparisons - not necessarily consecutively - the Comp 128 logic generates a Comp 128 output signal, which indicates a successfully programmed nibble. If the counter has not counted to 128 prior to the end of the 400 millisecond cycle, the sequence terminates and another 400 millisecond cycle starts. If programming is successful before the 400 millisecond pulse train ends, then all outputs in the nibble are over-programmed for 2.5 milliseconds.

Over-Programming. Following a Comp 128 output, the software - which monitors the Comp 128 signal (programming successful) - delays for 2.5 milliseconds. During this time the Comp 128 pulse triggers the OVP (overprogram) signal in the program pulse logic. When the OVP signal comes on, VCC and all current outputs in the nibble being programmed turn on. The duration of the overprogram is 2.5 milliseconds, which is terminated under software control.

12.3 PROGRAMMING PROCEDURE

1. Prior to the installation of the UPP-865 PC assembly, set switch S1 for the appropriate address boundary as indicated below in Table 12-2. The location of S1 is shown in Figure 12-4, and the various functions of S1 are shown

in Figure 12-5. To set the address boundary, set the individual switches between the indicated DIP pin numbers either ON or OFF, as indicated for the number of words in each PROM. To turn a switch ON set the slide to the right.

If the UPP-865 PC assembly has already been installed, set S1 and continue to step 3; if not, set S1 and install the UPP-865 according to the instructions in step 2.

TABLE 12-2

PROM ADDRESS BOUNDARY SWITCH SETTINGS

	SWITCH NUMBER					
PROM WORDS	3	4	5	6	7	8
256	OFF	ON	OFF	ON	OFF	ON
512	ON	OFF	OFF	ON	OFF	ON
1024	ON	OFF	ON	OFF	OFF	ON
2048	ON	OFF	ON	OFF	ON	OFF

2. The UPP-865 Personality Card must be installed in socket J2 on the mother board of the UPP-101, and either J1 or J2 of the UPP-102. See section 3.1.2 for installation instructions. These instructions are important because they point out potential errors, and provide user cautions to prevent damage to the PROM and/or the Personality Card.

> -- CAUTION --
>
> The regulator of the Personality Card may be damaged if the Personality Card is removed while power is on, or prior to discharging the 40 Volt input line. Consequently, it is mandatory to wait 60 seconds after system power off before removing the Personality Card.

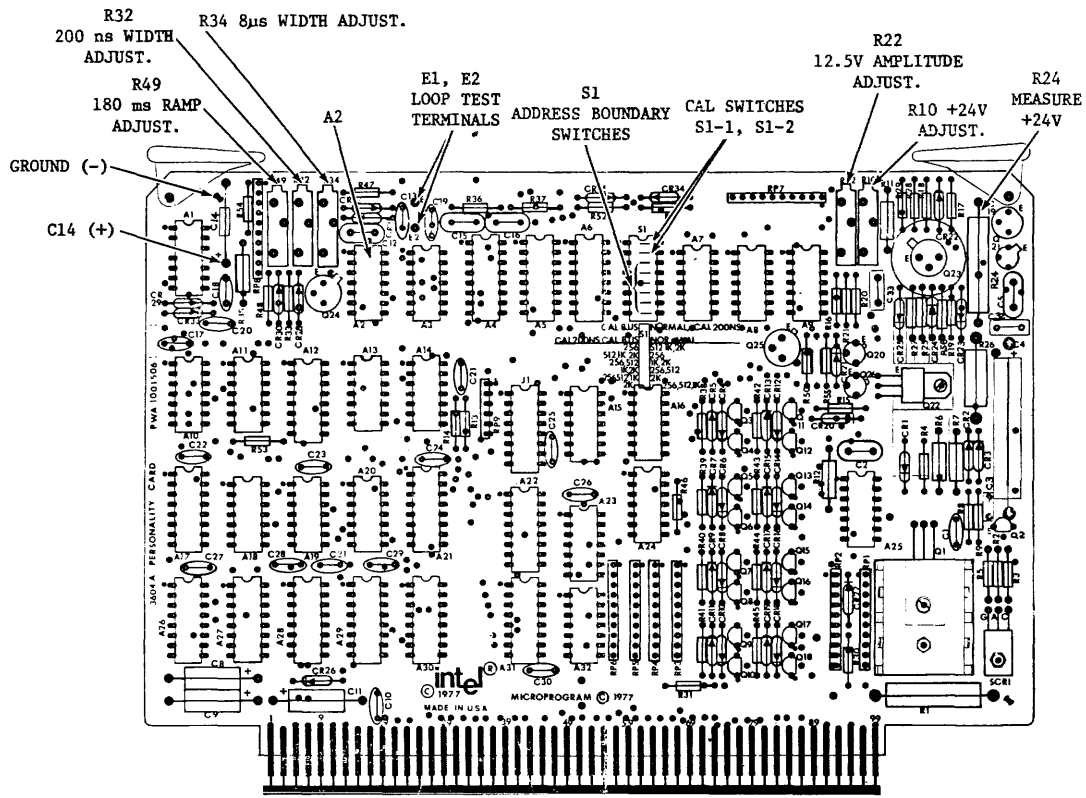
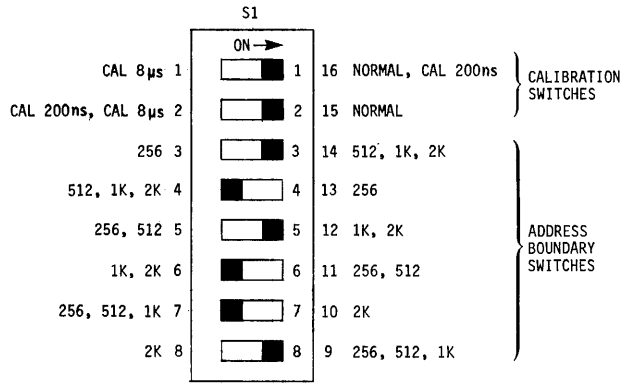


FIGURE 12-4. UPP-865 COMPONENT IDENTIFICATION



Note: The dark area on each switch denotes the position of the slide. Pin numbers are shown outside the switch area and switch numbers are shown inside.

Figure 12-5. Switch Functions for S1. The Switch settings are shown for the 3608 PROM (1k x 8).

3. Select and install the adapter required for programming. Insert the PROM in the adaptor. See Section 12.4 for information on selection and installation of the adapter and the PROM.

> -- CAUTION --
>
> To prevent damage to the Personality Card observe the following cautions:
>
> - DO NOT insert the UPP-555, UPP-562 or the UPP-565 adapters in a socket that is driven by any personality card other than the UPP-865 or the UPP-816.
> - Be sure to insert the adapter so that the lever on the adapter is at the top.
> - Be sure to insert the PROM so that pin 1 is in the upper left corner of the adapter.

4. Load the appropriate software for the PROM to be programmed. Refer to the applicable documentation list in Section 11.1.

12.4 THE UPP-555, UPP-562 AND UPP-565 ADAPTERS

The UPP-865 personality card operates with any one of three optional adapters, which are selected as a function of the device to be programmed. The adapters are the UPP-555, UPP-562 and the UPP-565. The UPP-555 is described in detail in Chapter 11 (including the operating instructions); the UPP-562 and the UPP-565 are shown in Figures 12-6 and 12-7, respectively.

The adapters are marked and can be identified as follows:

Adapter	PROM Socket	Markings
UPP-555	24 pins	UPP-555
UPP-562	16 pins	3602/3622 PWA 1000555
UPP-565	18 pins	3605/3625 PWA 1000745

To install an adapter and a PROM in the UPP-101 or UPP-102, use the following procedure:

1. Select the appropriate adapter for the PROM to be programmed, as indicated in Table 12-1.

2. Check to ensure that the correct Personality Card is installed in the UPP-101 or UPP-102.

3. Plug the selected Adapter in the corresponding front panel ZIP socket that corresponds to the Personality Card. Note that the UPP-101 has both 16-pin and 24-pin front panel ZIP sockets, and the UPP-102 has two 24-pin sockets. Be sure that the adapter is inserted in the socket that corresponds to the UPP-865 Personality Card. The adapter must be inserted in the front panel socket so that pin 1 of the adapter is in the upper left corner. See Figure 12-8. Observe the cautions in Section 12.3.

4. Insert the device to be programmed in the adapter with pin 1 in the upper left corner. If either the adapter or the device is improperly oriented, the programmer will be unable to program the PROM. Observe the cautions in Section 12.3.

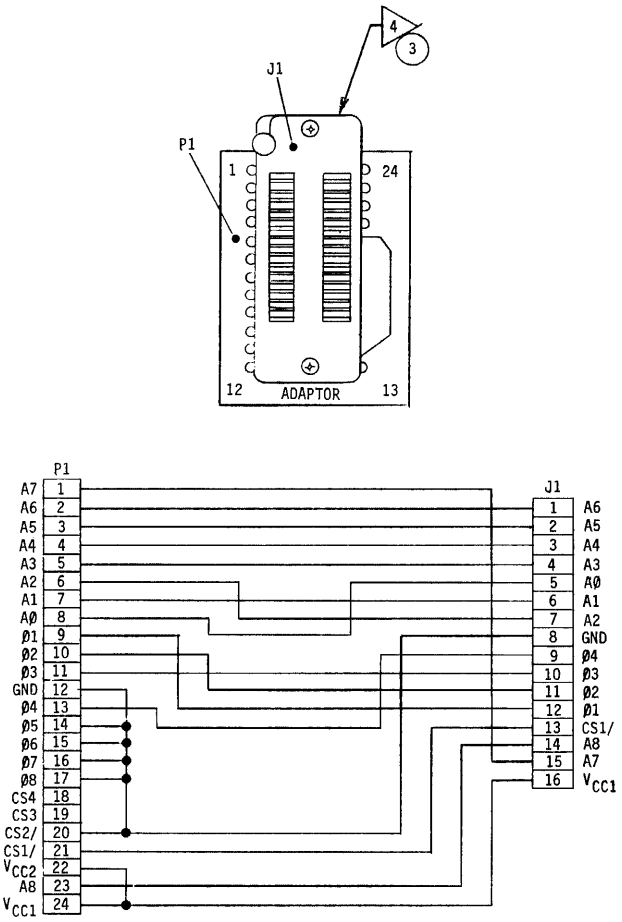


FIGURE 12-6. UPP-562 ADAPTER PIN ASSIGNMENTS

FIGURE 12-6. UPP-562 ADAPTER PIN ASSIGNMENTS

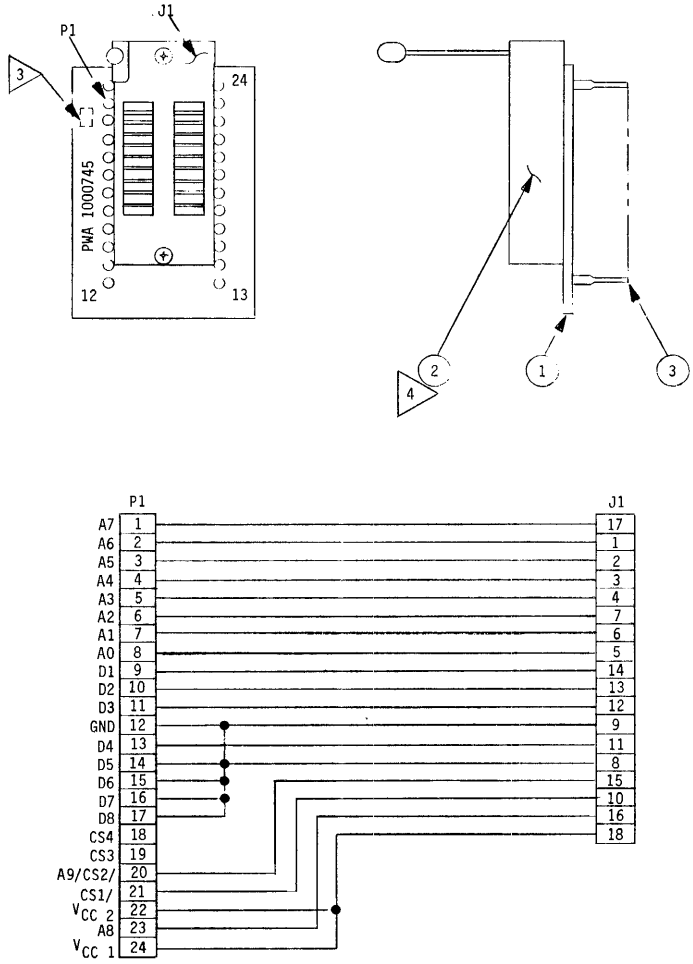


FIGURE 12-7. UPP-565 ADAPTER PIN ASSIGNMENTS

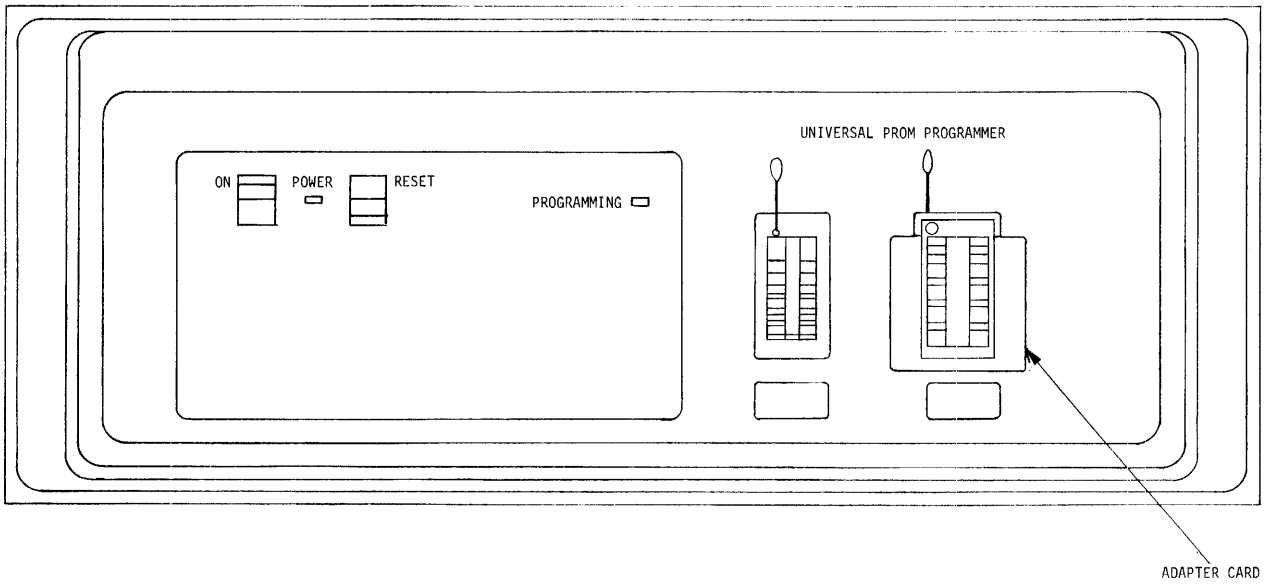


FIGURE 12-8. FRONT VIEW OF UPP WITH ADAPTER

12.5 CALIBRATION PROCEDURES

The UPP-865 Personality Card has five separate calibration adjustments. While calibration is not critical--tolerances are plus or minus 10% in most cases--the calibration should be checked every three months to ensure proper calibration.

Equipment Required. The following instruments are required for calibration of the UPP-865:

1. A 3½-digit digital multimeter or digital volt meter that can resolve 10 millivolts.

2. An oscilliscope that can resolve a 200 ns pulse.

> CAUTION
>
> The regulator of the Personality Card may be damaged if the Personality Card is removed while power is on, or prior to discharging the 40 Volt input line. Consequently, it is mandatory to wait 60 seconds after system power off before removing the Personality Card.

To calibrate the UPP-865 Personality Card use the following procedure:

1. Turn the UPP line power OFF. Wait 60 seconds and remove the UPP-865 from the UPP chassis.

2. Install a jumper between E1 and E2 (see Figure 12-4).

3. For ease of adjustment, insert the UPP-865 in the edge-connector J2 of the UPP motherboard. Remove the personality card from J1 on the UPP motherboard. Programming socket 2 on the UPP front panel must be empty.

4. Set the calibration switches S1-1 and S1-2 to the right, in the NORMAL position (ON). S1-1 and S1-2 are the two top switches on S1; they make contact between pins 1 and 16, and pins 2 and 15, respectively. All component locations are shown in Figure 12-4; the switch numbers, functions and connecting pins are shown in Figure 12-5.

5. Set the address boundary switches S1-3 through S1-8 to any convenient address boundary, such as the 1k boundary, as shown in Figure 12-5.

6. Turn the UPP line power ON.

7. Depress the RESET switch on the UPP front panel.

8. Connect a digital voltmeter to measure the +24 V regulator output. Convenient test points are the top lead of R24 (+), and the top lead of C14 (ground).

9. Adjust R10 so the voltmeter indicates +24.0 ± 0.5 V dc.

10. Measure the voltage at A2 pin 6. If the voltage is less than + 1.1 V dc, then continue to step 11. If the voltage is equal to or greater than 1.1 V dc, then adjust R34 to the center of its rotation. (R34 is a 20-turn trimming potentiometer; turn it clockwise 20 turns, and then turn it counterclockwise 10 turns to the center of rotation). Adjust R32 so the voltmeter indicates 1.0 V.

11. Program all zeroes into PROM location 0 by entering the following MDS monitor commands on the console:

S 7500 XX-00 (CR)
PTX7500, 7500,0 (CR)

Location 7500 is an arbitrary address;
XX = don't care; CR = carriage return.

The PROGRAM indicator light on the UPP should turn ON, indicating that the UPP-865 is looping.

12. Connect an oscilloscope to the (+) lead of C14. Set the oscilloscope sweep speed to 50 ms/div, and trigger on the negative slope of the signal.

13. Adjust R49 so the ramp time is 180 ± 18 ms. The wave form should appear as shown in Figure 12-9.

14. Connect the oscilloscope probe to pin 24 of socket 2 on the UPP front panel.

15. Set the calibration switches S1-1 and S1-2 to the CAL 8 us positions by sliding the switches to the left (OFF).

16. Adjust R22 so the peak pulse amplitude is 12.5 ± 0.5 V.

17. Adjust R34 so the pulse width is 8.0 ± 0.8 us, as measured between the 12-volt levels of the leading and trailing edges of the pulse waveform.

18. Set calibration switches S1-1 and S1-2 to the CAL 200 NS positions: set S1-1 to the right (ON) and S1-2 to the left (OFF).

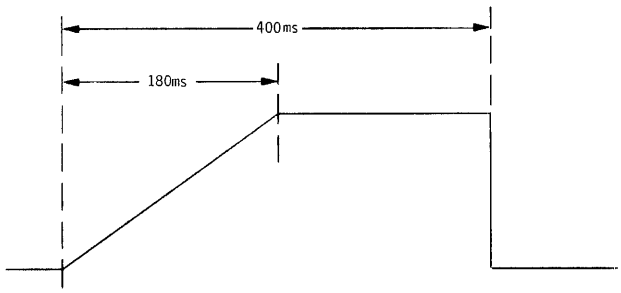


FIGURE 12-9. TIMING RAMP WAVEFORM (Step 13)

19. Adjust R32 so that the pulse width is 200 ± 40 ns, as measured at the 12 Volt level on the leading and trailing edges of the pulse waveform.

20. Repeat steps 15 through 19.

21. Depress the front panel RESET switch on the UPP.

22. Turn the UPP power OFF; wait 60 seconds and remove the UPP-865.

23. Set calibration switches S1-1 and S1-2 to the NORMAL positions (to the right, or ON). Set the address boundary switches S1-3 to S1-8 to the desired boundary as shown in Table 12-2.

24. Remove the shorting jumper between E1 and E2 on the UPP-865.

25. Replace the UPP-865 in its correct socket; if another personality card was removed, replace it also.

26. Turn the UPP power ON.

27. Depress the RESET switch on the UPP. This concludes the calibration adjustment; the UPP-865 is now ready for operation.

12.6 PIN LIST: UPP-865 PERSONALITY CARD

The UPP-865 Personality Card communicates with the control board and the PROM socket on the front panel through a 100-pin double-sided, edge-type pc connector. Pin allocations and designated signal functions for the connector are listed in Table 12-3.

TABLE 12-3

UPP-865 PERSONALITY CARD PIN LIST

PIN	MNEMONIC	FUNCTION	SOURCE*	DESTINATION*
1	GND	Ground		
2	GND			
3				
4				
5	VCCH	Power inputs (5.85V)		
6	VCCH			
7	VCCH			
8	VCCH			
9	GND	Ground		
10	GND			
11	-10VDC	Power inputs	PS	PC
12	-10VDC			
13	GND	Ground		
14	GND			
15				
16	BD SENSE/	Board Sense	PC	CB
17			PS	PC
18				
19	CONTROL	Control bit		
20				
21	WRITE DATA 0	Write data bus fron Control Board	CB	PC
22	WRITE DATA 1			
23	WRITE DATA 2			
24	WRITE DATA 3			
25	WRITE DATA 4			
26	WRITE DATA 5			
27	WRITE DATA 6			
28	WRITE DATA 7			
29	PROM ADDRESS 0	PROM address bus from Control Board	CB	PC
30	PROM ADDRESS 1			
31	PROM ADDRESS 2			
32	PROM ADDRESS 3			
33	PROM ADDRESS 4			
34	PROM ADDRESS 5			
35	PROM ADDRESS 6			
36	PROM ADDRESS 7			
37	PROM ADDRESS 8			
38	PROM ADDRESS 9			
39	PROM ADDRESS 10			
40	PROM ADDRESS 11			
41	D0	MCS-40 data bus (bi-directional)	CB/PC	PC/CB
42	D1			
43	D2			
44	D3			
45	ϕ2	MCS-40 clock (bi-directional)	CB	PC
46	ϕ1			
47	CM-ROM	ROM bank enable	CB	PC
48				
49				
50	SYNC	MCS-40 synchronization		

*PS = Power Supply CB = Control Board PC = 3604 Personality Card
FP = Front Panel (PROM socket)

TABLE 12-3 (Continued)

PIN	MNEMONIC	FUNCTION	SOURCE*	DESTINATION*
51	RESET/	MCS-40 Reset	CB	PC
52	PROM RD DATA 0/	Data read from PROM	PC	CB
53	PROM RD DATA 1/			
54	PROM RD DATA 2/			
55	PROM RD DATA 3/			
56	PROM RD DATA 4/			
57	PROM RD DATA 5/			
58	PROM RD DATA 6/			
59	PROM RD DATA 7/			
60				
61	A7	PROM address	PC	FP
62	A6			
63	A5			
64	A4			
65	A3			
66	A2			
67	A1			
68	A0			
69	D0	PROM data (bi-directional)	PC/FP	FP/PC
70	D1			
71	D2			
72	GND	Ground		
73	GND			
74	GND			
75	GND			
76	GND			
77	D3	PROM data (bi-directional)	PC/FP	FP/PC
78	D4			
79	D5			
80	D6			
81	D7			
82	CS4	PROM chip select/ address	PC	FP
83	CS3,$\overline{\text{A10}}$			
84	CS2/,A9			
85	CS1/			
86	VCC2			
87	A8			
88	VCC1			
89				
90				
91	GND	Ground		
92	GND			
93				
94				
95	+40V	Power inputs	PS	PC
96	+40V			
97				
98				
99	GND	Ground		
100	GND			

*PS = Power Supply CB = Control Board PC = 3604 Personality Card
FP = Front Panel (PROM socket)

APPENDIX A
INTELLEC MDS MONITOR: PROM PROGRAMMER COMMANDS

The INTELLEC® MDS Monitor provides basic utility functions for the INTELLEC® MDS Microcomputer Design Center. The Monitor provides program loading, memory display and modification capability, various utilities for PROM programming, program checkout and debugging facilities, and a generalized and extensible I/O system that is accessible to user programs.

The Monitor provides three commands for use with the Universal PROM Programmer:

- C command - compare the contents of a PROM with data stored in random access memory (RAM).
- P command - program a PROM.
- T command - transfer the contents of a PROM into RAM.

The C, P and T commands each require specification of a "true/false" parameter and a "socket option" parameter.

The "true/false" parameter is specified by the alphabetic character 'T' or 'F'. 'T' specifies positive true programming, while 'F' specifies positive false programming. In the positive true mode, a "1" bit in the PROM corresponds to a "1" bit in the INTELLEC® MDS random-access memory (RAM). In the positive false mode, however, a "1" bit in the PROM corresponds to a "0" bit in RAM.

The "socket option" parameter is designated by the letters X, Y or Z, where:

- X selects socket 2. This operation is considered an 8-bit operation only.

- Y selects socket 1 and treats each PROM word as the four most significant bits of the byte (upper nibble) in the Intellec® MDS memory. Eight bit transfer and program operations will be processed for 8-bit devices. An 8-bit compare may be achieved with a 2-step operation described in example 2.

- Z selects socket 1 and treats each PROM word as the four least significant bits of an 8-bit data byte in the INTELLEC MDS memory. Eight bit transfer and program operation will be processed for 8-bit devices. An 8-bit compare may be achieved with a 2-step operation described in Example 2.

The C, P and T commands are described below:

Compare PROM Command, C:

C<t/f><socket option><low address>,<high address>

The C command compares the contents of a PROM located in the socket on the PROM Programmer peripheral specified by <socket option>, beginning at PROM address 0, with the memory area specified by <low address> through <high address>, inclusive. If the contents of a PROM location are not equal to the contents of the corresponding memory location, the memory address, the contents of the memory location, and the contents of the PROM location are printed on the console for inspection.

Example 1: Socket 1 is a 16 pin (4-bit) socket

```
.CTY200,2FF
0206 A0 FF
0291 23 11   RAM   PROM
.
```

In Example 1, memory locations 206H and 291H upper nibble do not compare with the PROM located in socket 1 (4-bit PROM) of the PROM Programmer peripheral when compared in positive true form.

Example 2: Socket 1 is a 24 pin (8-bit) socket

```
.CFY200,3FF
.CFZ200,3FF
.
```

In the above example, the first compare statement compares the upper nibble of memory locations 200H to 3FFH to the upper nibble of the PROM- no error found. The second compare statement compares the lower byte of memory location 200H to 3FFH to the lower byte of the PROM- no error found. If socket 1 is a 24 pin socket, two monitor compares must be made; one for comparing the upper nibble and one for comparing the lower nibble.

PROM Programming Command, P:

P<t/f><socket option><low address>,<high address>,<PROM address>

Any area of the INTELLEC® MDS addressable memory can be written into a PROM with the P command. The memory area bounded by <low address> through <high address>, inclusive, is programmed into the PROM beginning at the address specified in the command as <PROM address>.

Example 1: Socket 1 is a 16 pin (4-bits) socket

```
PFY100,1FF,0
```

Program the PROM in socket 1 with the upper 4 bits of the contents of memory 100H through 1FFH. A '1' bit in RAM becomes a '0' bit in PROM because of the 'F' (positive false) parameter.

Example 2: Socket 1 is a 24 pin (8-bit) socket

PTY100,1FF,0

Program the PROM (8-bits) in socket 1 with the contents of memory 100H through 1FFH. If socket 1 is a 24 pin socket, the personality card will ignore the nibble select.

Transfer PROM Command, T:

T<t/f><socket option><low address>,<high address>

The contents of a PROM located in the programming socket on the PROM Programmer peripheral selected by <socket option> may be copied into memory with the T command. The PROM data is stored in memory starting at the location specified in the command as <low address> and continuing through <high address>.

If the <t/f> field specifies positive true logic ("T"), a "1" bit in the PROM will be transferred to RAM as a "1". Specifying "F" will cause a "1" bit in PROM to be transferred to RAM as a "0", and vice versa.

Example:

TFY100,1FF

Transfer PROM location 0 to FFH into memory location 100H to 1FFH. An 8-bit transfer is always made. If the PROM is a 4-bit device, the upper and lower nibble are duplicated.

PROM Programmer Error Indications:

During a P command, the monitor transfers data, one byte at a time, to the PROM Programmer, then checks the Universal PROM Programmer's status word waiting for a not busy indication. When BUSY goes false, the monitor checks the status word for any error indications. If an error did occur the monitor will terminate the P command and display the current PROM address on the console, preceded by an asterisk. Aside from checking for the syntactic validity of the command, no other error checking is done by the monitor during a P command.

This same error checking is performed during transfer (T) and compare (C) commands. If an error is detected, an asterisk is displayed at the operator's terminal.

If a PROM Programmer is not connected to the INTELLEC® MDS system, the P, T, and C commands will produce an error indication immediately upon entry of the command character.

APPENDIX B
UNIVERSAL PROM PROGRAMMER SCHEMATICS

Schematic drawings for the Universal PROM Programmer and each of the available personality cards are provided in this appendix.

Information and diagrams in this section are subject to change without notice. The Prom Programmer Reference Schematic Drawings (98-159A) shipped with the PROM Programmer should be used as a reference.

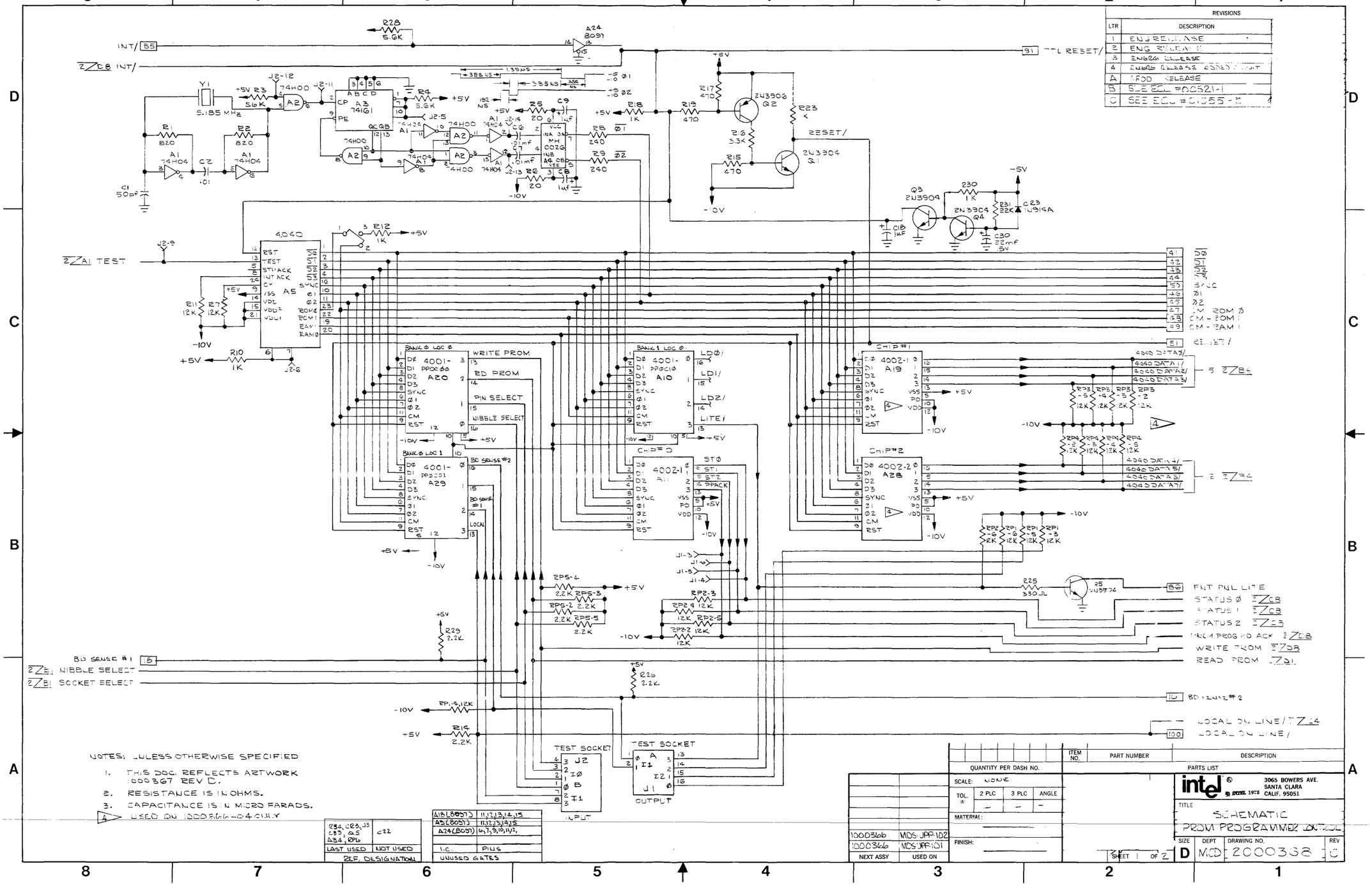


Figure B-1. UPP Control Circuit Assembly (Sheet 1 of 2)

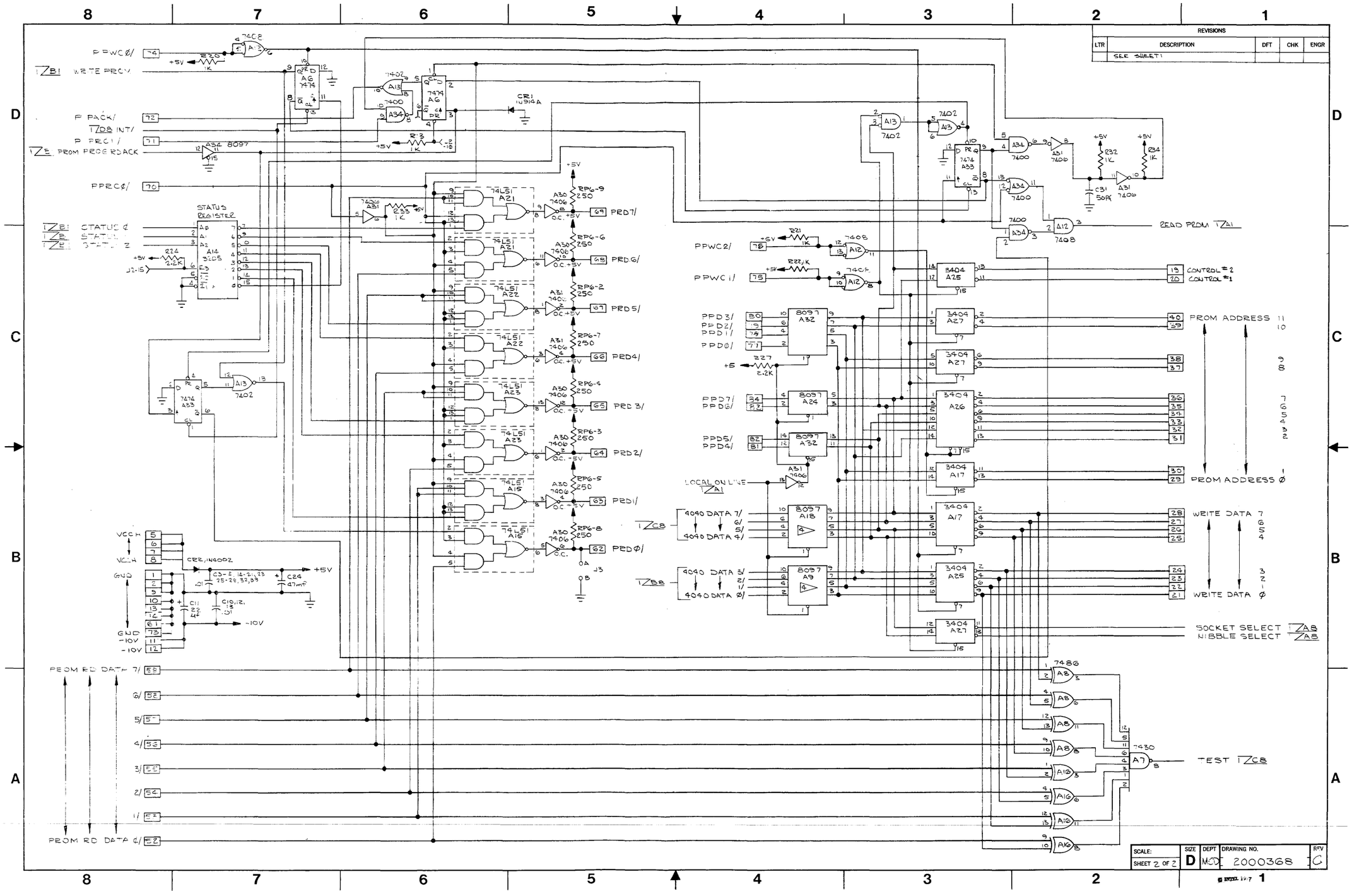


Figure B-1. UPP Control Circuit Assembly (Sheet 2 of 2)

REVISIONS		
ZONE	LTR	DESCRIPTION
C4 C5 NOTE 11	A	PROD REL; P/L CHG
	B	SEE ECO # 00975-

+12V REGULATOR

CROWBAR

+40V
+40V

-5V REGULATOR

PROM ADRS Ø
PROM ADRS 11

PROM ADDRESS

PROM POWER

I.C. POWER PINS			
REF DESIG.	GND	+5V	-10V
A6, A12		5	12

REF DESIG	
LAST USED	NOT USED
A14	A2
R60	R1, R2
RP1	
J4	
J3	
VR4	
C28	C2
J2, S1	
SCR1	

SPARES		
TYPE	REF DESIG	QTY
7404	A5	2

NOTES: UNLESS OTHERWISE SPECIFIED;

1. RESISTORS ARE IN OHMS, ¼W ±5%.
2. CAPACITORS ARE IN MICRO FARADS, +80% −20%, 25V
3. TRANSISTORS ARE 2N3904
4. J1 IS A 16 PIN TEST SOCKET
5. (D.U.P.) DENOTES DEVICE UNDER PROGRAM
6. HEATSINK REQUIRED.
7. TURNING SWITCH 4-5 ON CAUSES PROG. TO REMAIN IN PROG LOOP FOR TEST PURPOSES
8. REMOVAL OF JUMPER ALTERS OPERATING TECHNIQUES.
9. SEE SWITCH TABLE
10. ADJUST 26.5V SUPPLY TO ±1.0% BY ADJUSTING TRIMPOT R17.

NOTES CONT.:
11. THIS DOCUMENT REFLECTS ARTWORK REV. B.

(S1) SWITCH TABLE

FAMILY	1-8	2-7	3-6	4-5
2708	ON	OFF	OFF	NU*
2704	ON	ON	OFF	NU*

NOTE: "ON" INDICATES SHORTING BETWEEN PINS (I.E. 1-8, 2-7) PIN NOS. INDICATED ARE THE DIP (DUAL-IN-LINE-PACKAGE) PIN LOCATIONS. THESE NOS. WILL NOT ALWAYS MATCH THE SWITCH SLIDE NO. NOMENCLATURE.
*NOT USED

ITEM NO.	PART NUMBER	DESCRIPTION
QUANTITY PER DASH NO.		PARTS LIST

SCALE:
TOL. ± | 2 PLC | 3 PLC | ANGLE
MATERIAL:
FINISH:

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TITLE SCHEMATIC
2708 A
PERSONALITY

SIZE	DEPT	DRAWING NO.	REV
D	MCD	2000968	B

SHEET 1 OF 2

1000967 NEXT ASSY | UPP 878 USED ON

Figure B-2. UPP-878 Personality Circuit Assembly (Sheet 1 of 2)

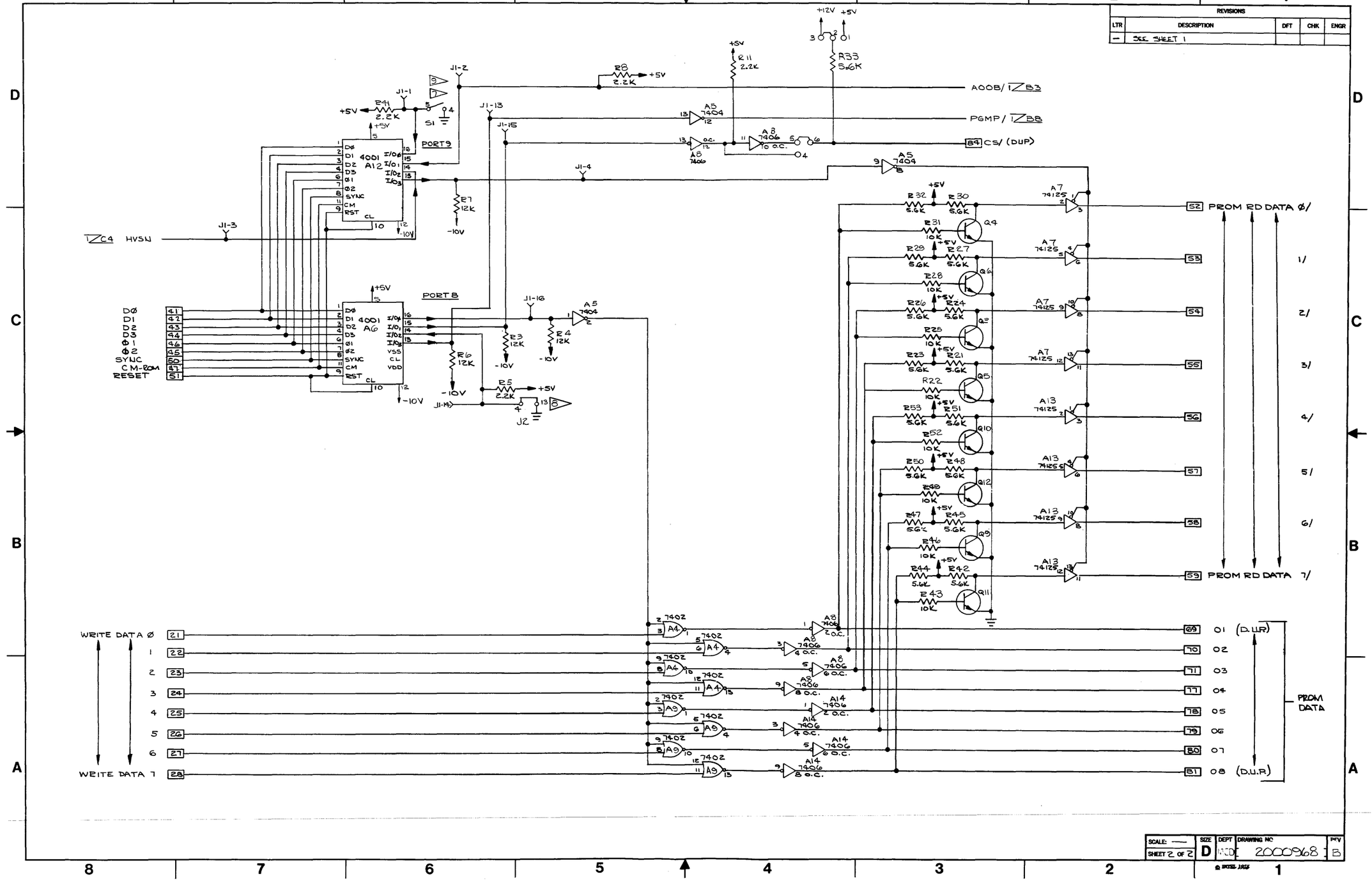


Figure B-2. UPP-878 Personality Circuit Assembly (Sheet 2 of 2)

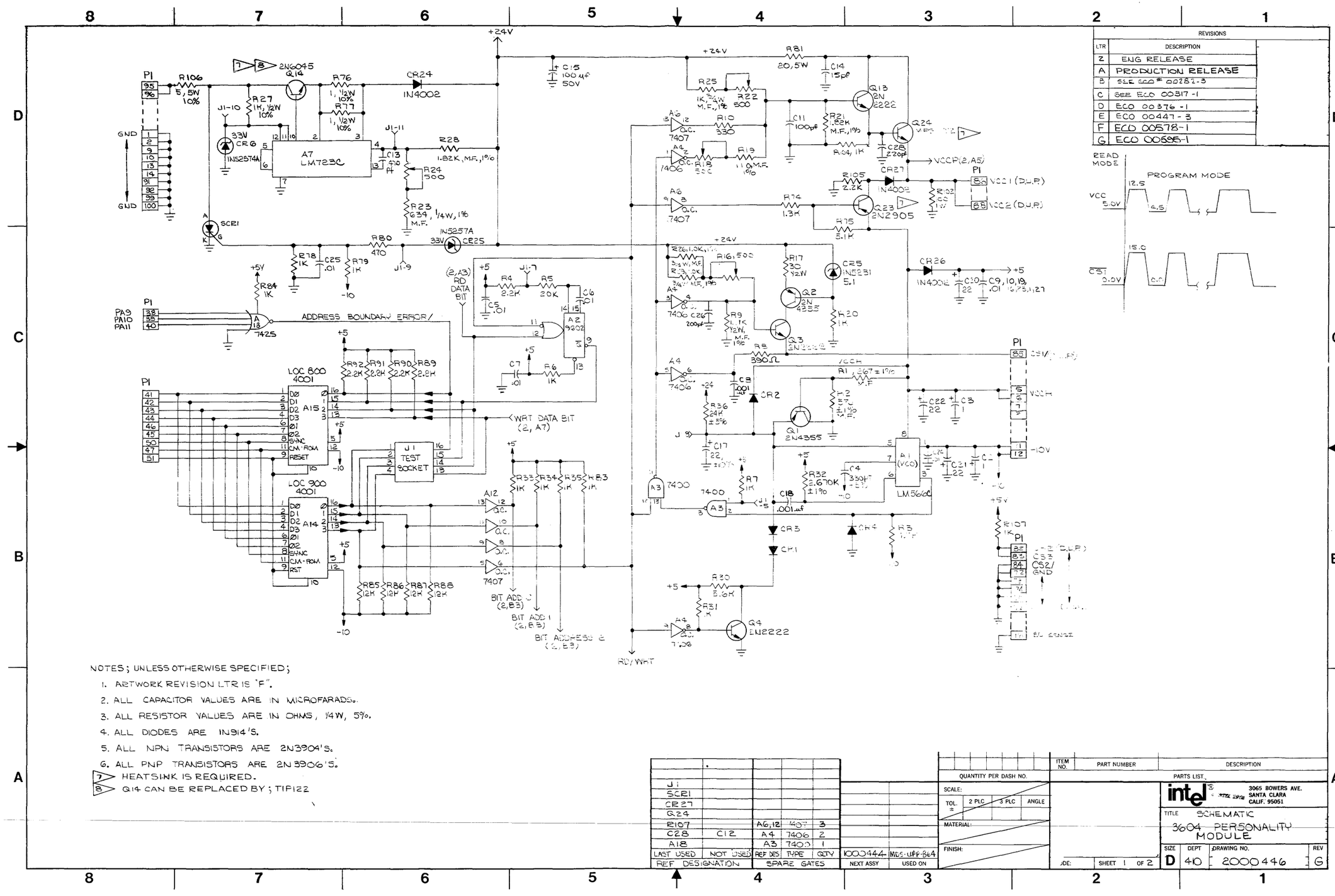


Figure B-3. UPP-864 Personality Circuit Assembly (Sheet 1 of 2)

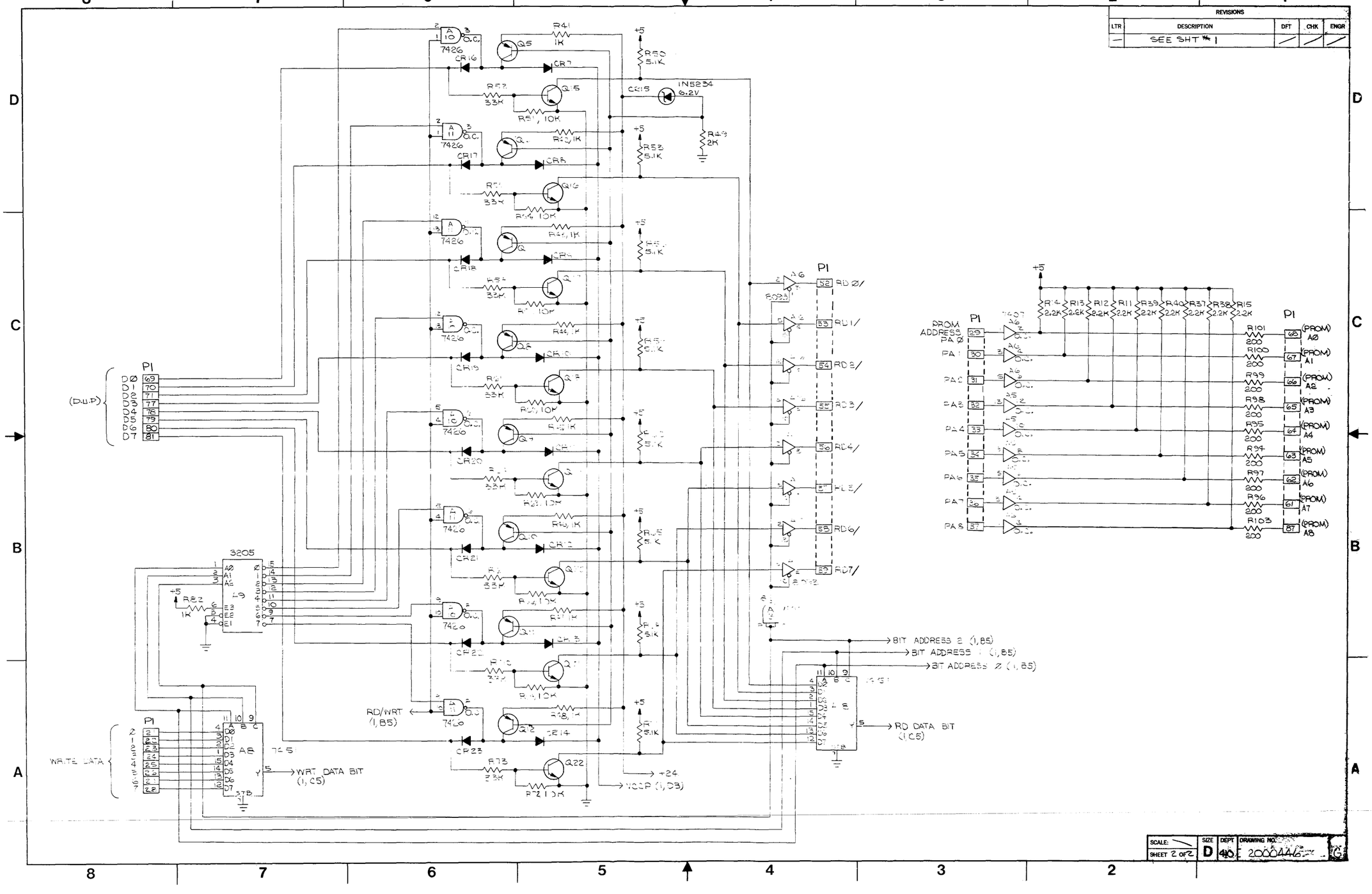


Figure B-3. UPP-864 Personality Circuit Assembly (Sheet 2 of 2)

REVISIONS	
LTR	DESCRIPTION
A	ENG RELEASE
B	PROD RELEASE
C	SEE ECO # 251 of 2
D	SEE ECO # 00280-3
E	SEE ECO # 00367-1
F	SEE ECO # 00436

NOTE : UNLESS OTHERWISE SPECIFIED

1. ARTWORK REVISION IS REV E.
2. RESISTANCE VALUES ARE IN OHMS
3. CAPACITANCE VALUES ARE IN MICROFARADS.
4. DIODES ARE IN914

SPARES		
TYPE	QTY	REF. DES.
7406	2	A4

REF. DES.	
LAST USED	NOT USED
A19	
C30	
CR11	
F.83	
Q12	

ITEM NO.	PART NUMBER	DESCRIPTION
		PARTS LIST

QUANTITY PER DASH NO.

SCALE: NONE

TOL. ± | 2 PLC | 3 PLC | ANGLE

MATERIAL:

FINISH:

NEXT ASSY: 000436 | USED ON: MDS UPP 361

intel 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE: SCHEMATIC, 3601 PERSONALITY MODULE

SIZE	DEPT	DRAWING NO.	REV
D	410	[illegible]0438	F

DE: | SHEET OF 2

Figure B-4. UPP-361 Personality Circuit Assembly (Sheet 1 of 2)

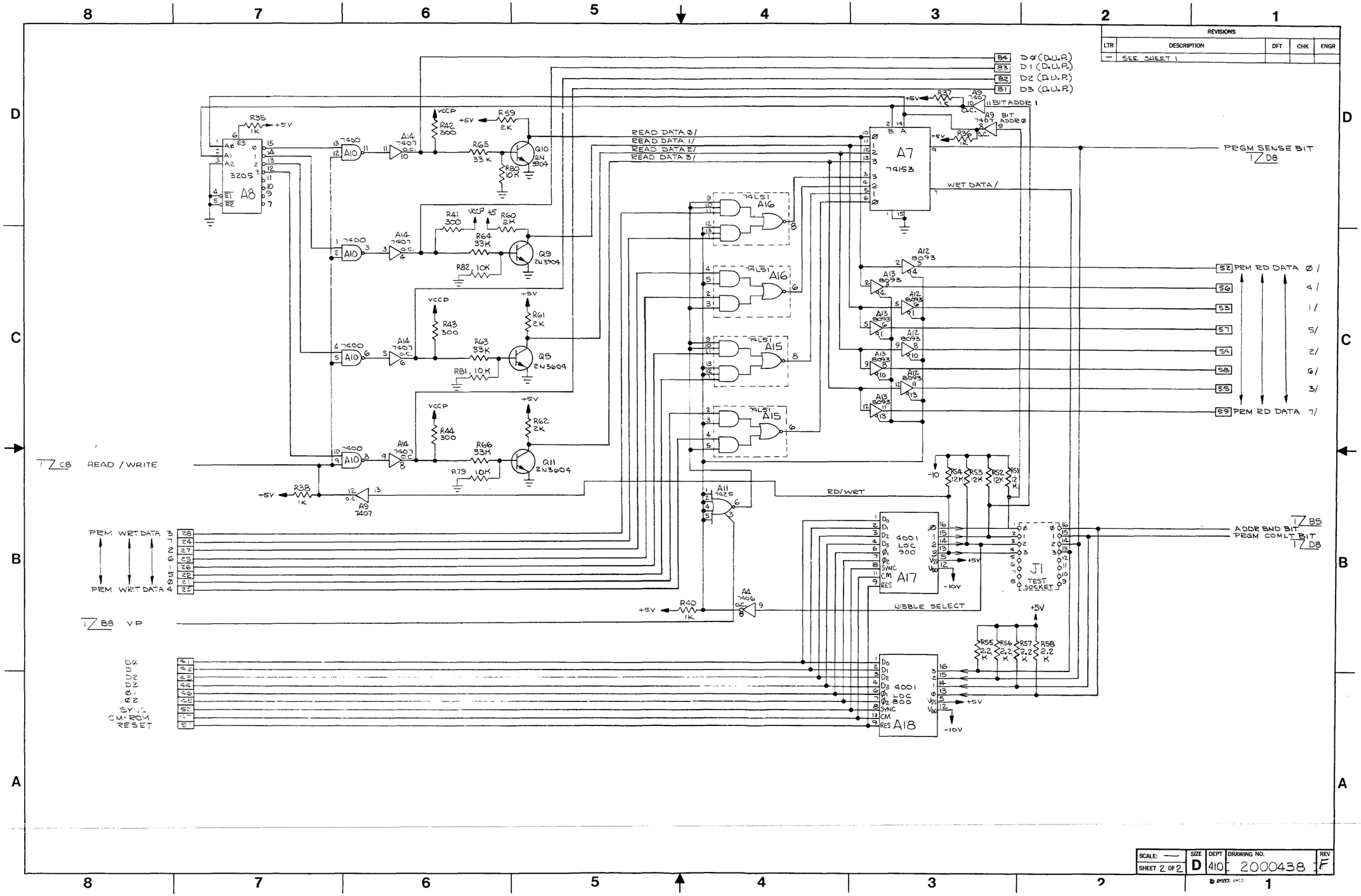
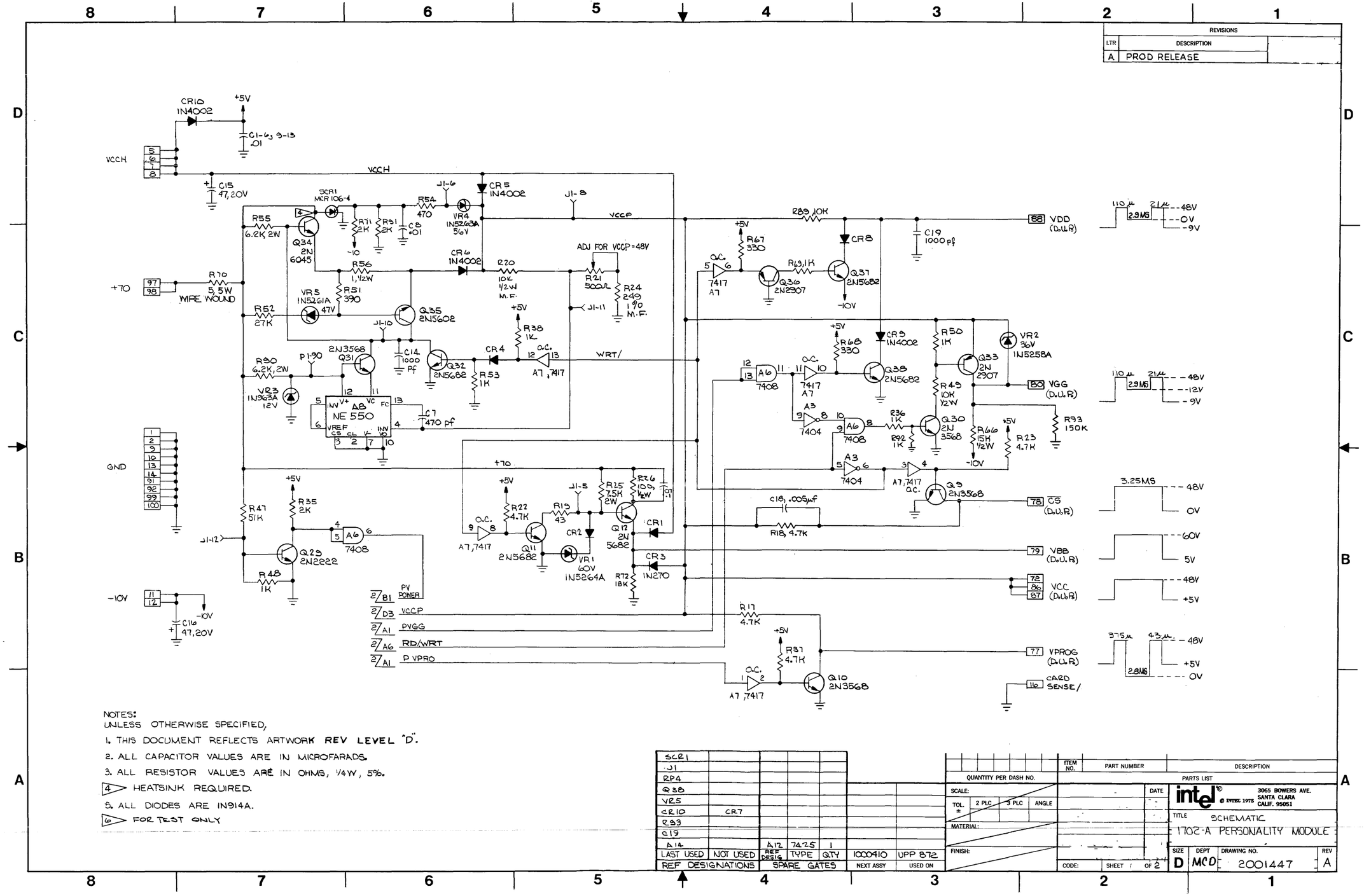


Figure B-4. UPP-361 Personality Circuit Assembly (Sheet 2 of 2)



NOTES:
UNLESS OTHERWISE SPECIFIED,

1. THIS DOCUMENT REFLECTS ARTWORK **REV LEVEL "D".**
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
4. HEATSINK REQUIRED.
5. ALL DIODES ARE IN914A.
6. FOR TEST ONLY

REF DESIGNATIONS		SPARE GATES				
LAST USED	NOT USED	REF DESIG	TYPE	QTY	NEXT ASSY	USED ON
SCR1						
J1						
RP4						
Q38						
VR5						
CR10	CR7					
R93						
C19						
A14		A12	7425	1	1000410	UPP 872

QUANTITY PER DASH NO.

ITEM NO.	PART NUMBER	DESCRIPTION

PARTS LIST

SCALE:
TOL ± | 2 PLC | 3 PLC | ANGLE
MATERIAL:
FINISH:
DATE

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TITLE SCHEMATIC
1702-A PERSONALITY MODULE

SIZE	DEPT	DRAWING NO.	REV
D	MCD	2001447	A

CODE: SHEET 1 OF 2

Figure B-5. UPP-872 Personality Circuit Assembly (Sheet 1 of 2)

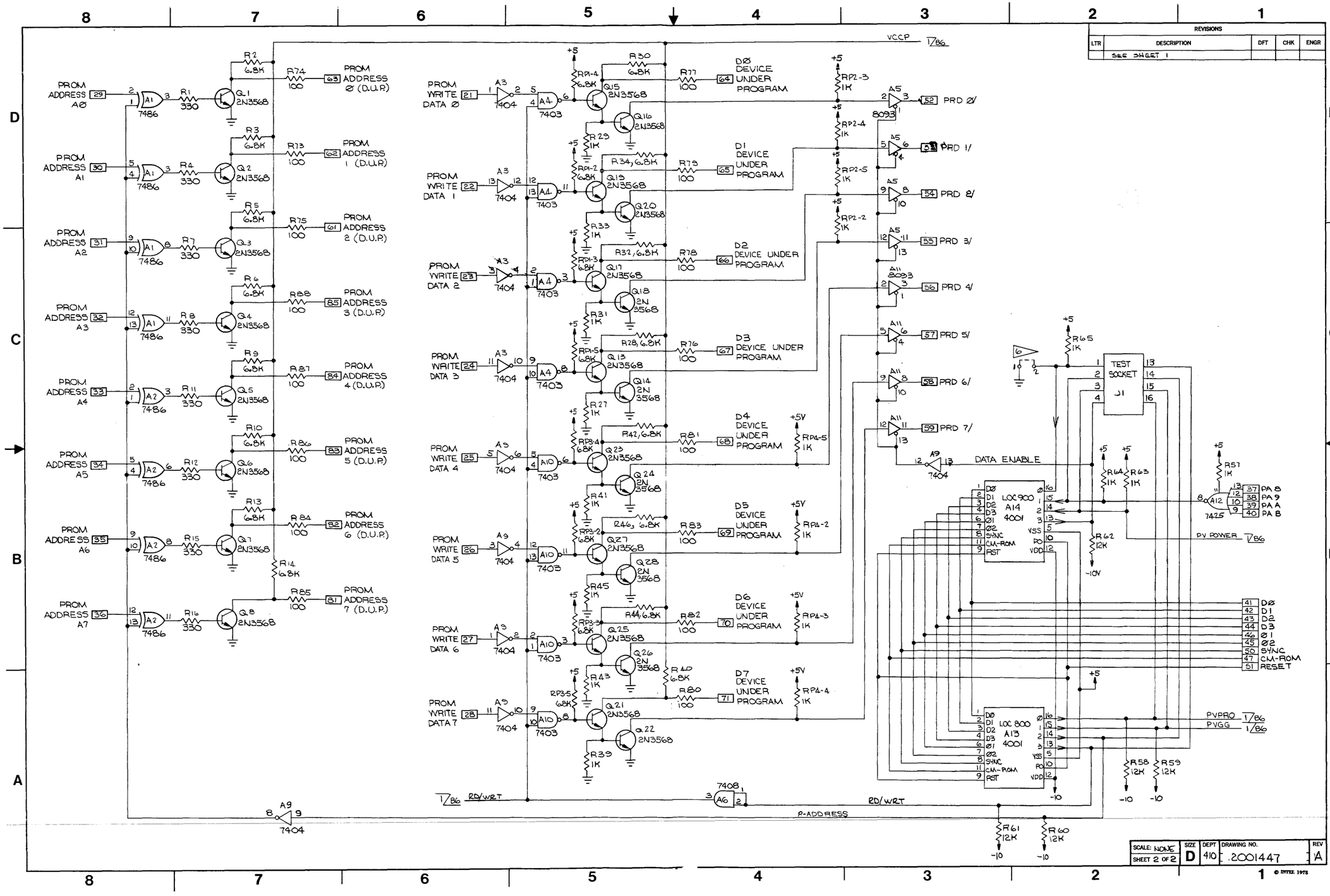

Figure B-5. UPP-872 Personality Circuit Assembly (Sheet 2 of 2)

REVISIONS	
LTR	DESCRIPTION
A	PRODUCTION RELEASE.
B	SEE ECO # 007776-1

NOTES:
UNLESS OTHERWISE SPECIFIED,
1. ARTWORK REV LEVEL IS 'B'.
2. RESISTOR VALUES ARE IN OHMS, ¼W, ±5%.
3. SEE SWITCH TABLE

3 SWITCH TABLE (S1)

PROM	SIZE X 8	1-8	2-7	3-6	4-5
8748	1K	NU*	NU*	ON	ON
	2K	NU*	NU*	OFF	ON
	4K	NU*	NU*	OFF	ON

NOTE: 'ON' INDICATES SHORTING BETWEEN PINS (I.E. 3-6, 4-5) PIN NUMBERS INDICATED ARE THE DIP (DUAL-IN-LINE PACKAGE) PIN LOCATION. THESE NOS. WILL NOT ALWAYS MATCH THE SWITCH SLIDE NO. NOMENCLATURE. * — NOT USED

LAST USED	NOT USED	TYPE	REF DESIG	QTY
W1		7406	A7	1
C26		7407	A1	1
VR2		74LS04	A12	2
CR5		74S04	A3	1
Q8		7400	A5	2
R82				
A19				
REF DESIGNATION		SPARE GATES		

NEXT ASSY	USED ON
1000735	UPP-848

ITEM NO.	PART NUMBER	DESCRIPTION
PARTS LIST		

QUANTITY PER DASH NO.

SCALE:

TOL. ± | 2 PLC | 3 PLC | ANGLE

MATERIAL:

FINISH:

intel 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE SCHEMATIC
8748 PERSONALITY

SIZE	DEPT	DRAWING NO.	REV
D	410	2000737	13

SHEET 1 OF 2

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BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-5200

Figure B-6. UPP-848 Personality Circuit Assembly (Sheet 1 of 2)

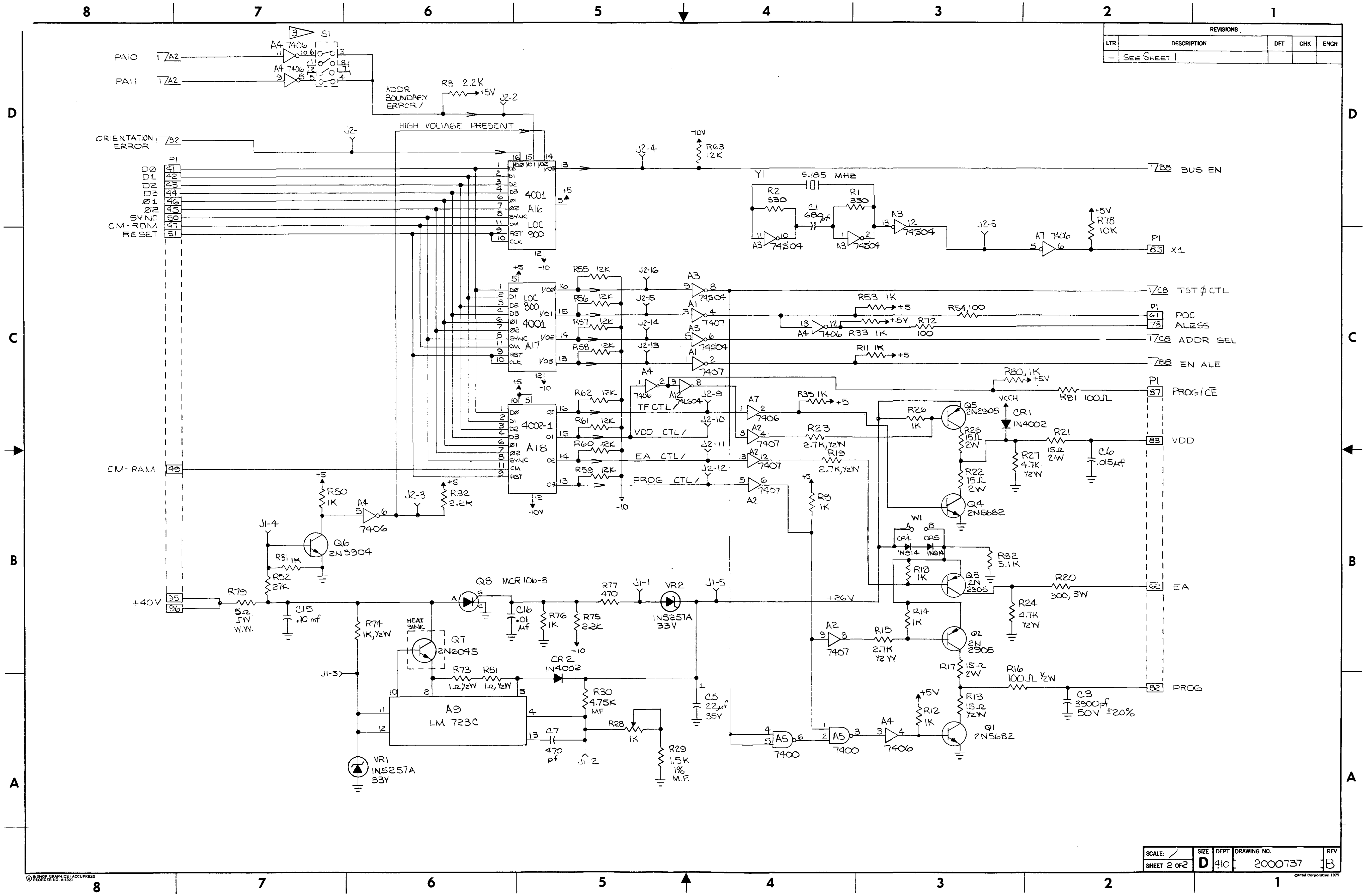


Figure B-6. UPP-848 Personality Circuit Assembly (Sheet 2 of 2)

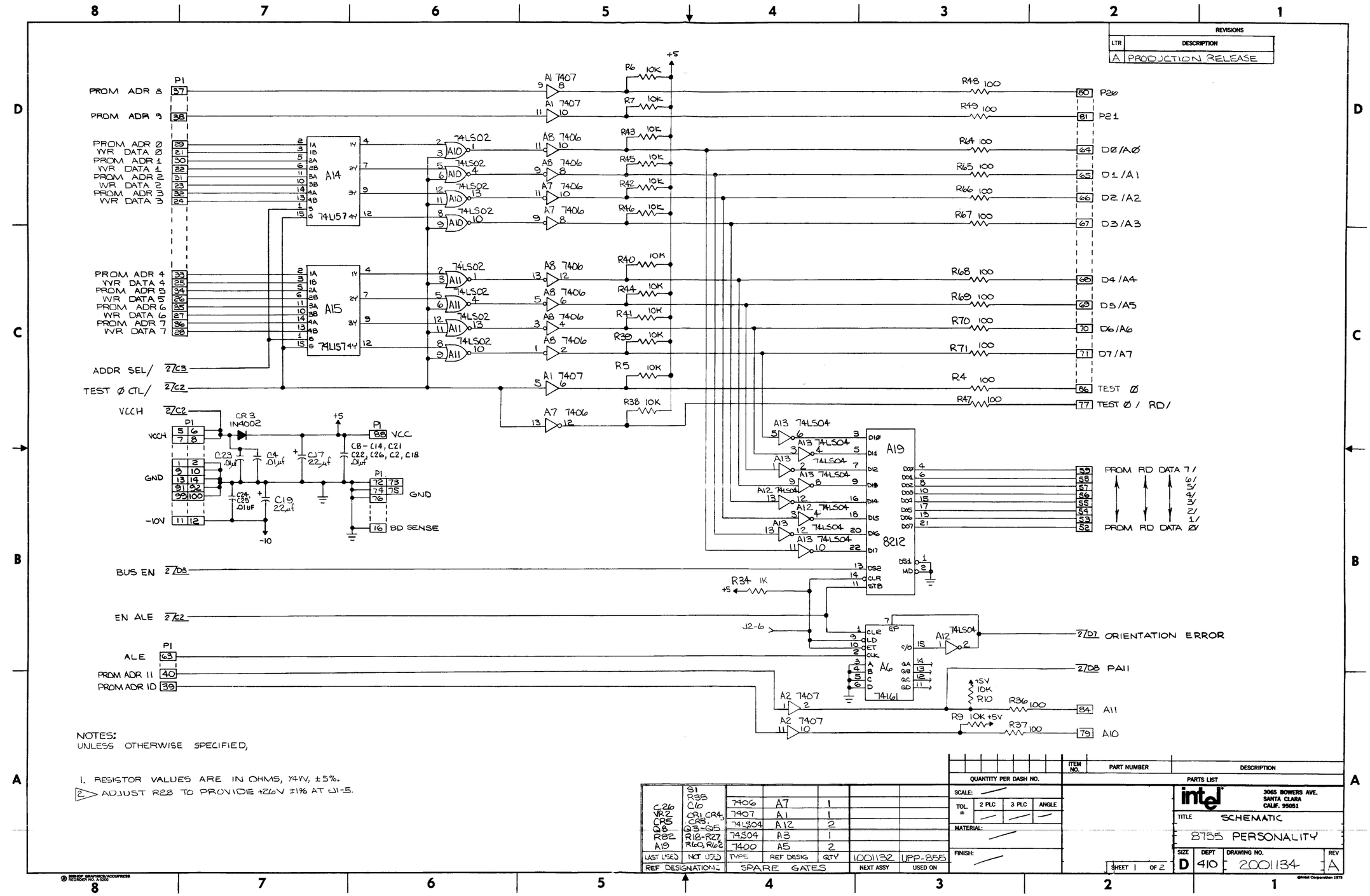


Figure B-7. UPP-855 and UPP-955 Personality Circuit Assembly (Sheet 1 of 2)

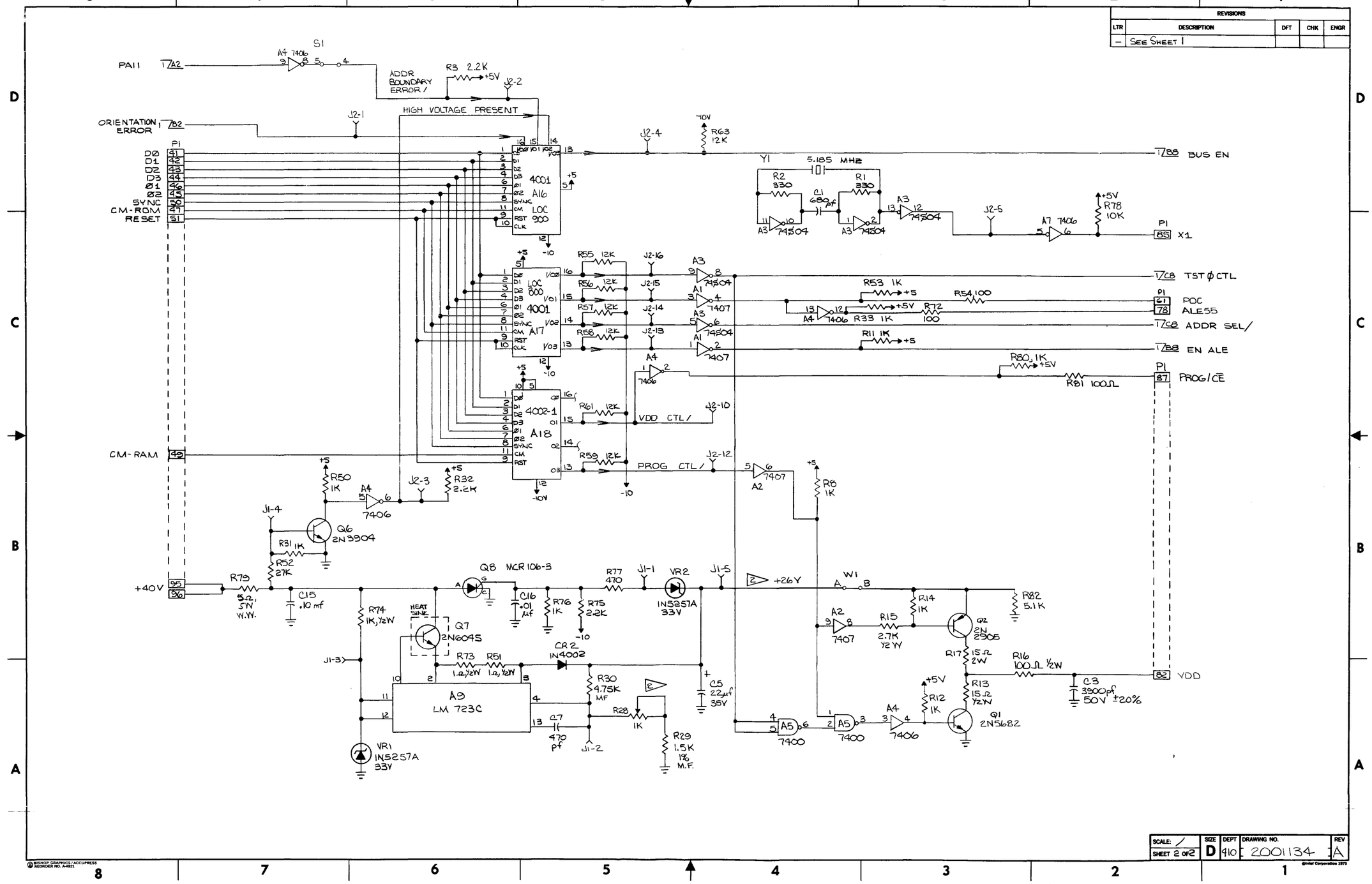
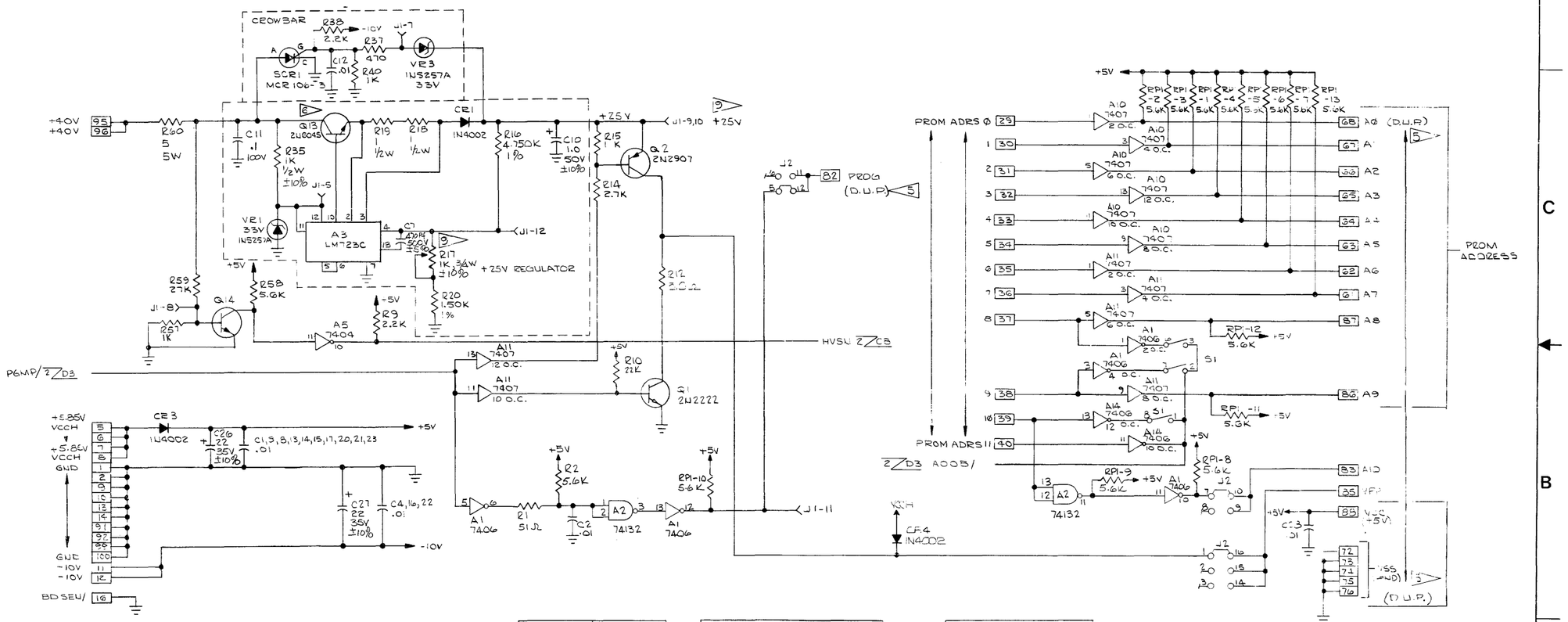


Figure B-7. UPP-855 and UPP-955 Personality Circuit Assembly (Sheet 2 of 2)

REVISIONS				
ZONE	LTR	DESCRIPTION	SIGNATURE AND DATE DFT	CHK	ENGR
D4 B7 B2	A	PROD RELEASE, ECO#'S [illegible]			
	B	SEE ECO # 00375-5			



NOTES: UNLESS OTHERWISE SPECIFIED;

1. RESISTORS ARE IN OHMS, ¼W, 5%.
2. CAPACITORS ARE IN MICRO FARADS, 25V, +80%, -20%.
3. TRANSISTORS ARE 2N3904
4. J1 IS A 16 PIN TEST SOCKET
5. (D.U.P.) DENOTES DEVICE UNDER PROGRAM.
6. HEATSINK REQUIRED.
7. TURNING SWITCH 4-5 ON CAUSES PROG. TO REMAIN L PROG LOOP FOR TEST PURPOSES
8. SEE SWITCH TABLE
9. ADJUST 25VOLT SUPPLY TO ± 1.0% BY ADJUSTING TRIMPOT R17.
10. THIS DOCUMENT REFLECTS ARTWORK REV. B.

REFERENCE DESIGNATION	
LAST USED	NOT USED
A14	
R60	R36,38,39,54-58,13
C28	C6,18,19,24,25
S1	
J2	
CR4	CR2
RP1	
VR3	VR2
Q14	Q3,8
SCR1	

SPARES		
TYPE	REF DESIG	QTY
7404	A5	2
74132	A2	2

I.C POWER PINS		
REF. DESIG.	+5V	-10V
A6, A12	5	12

8 S1 SWITCH TABLE

PROM SIZE X8	1-8	2-7	3-6	4-5
512	ON	ON	OFF	
1K	ON	OFF	OFF	
2K	OFF	OFF	OFF	

NOTE: 'ON' INDICATES SHORTING BETWEEN PINS (I.E 1-8, 2-7) PIN NOS INDICATED ARE THE DIP (DUAL-IN-LINE PACKAGE) PIN LOCATIONS. THESE NOS WILL NOT ALWAYS MATCH THE SWITCH SLIDE NO. NOMENCLATURE.

ITEM NO.	PART NUMBER	DESCRIPTION
QUANTITY PER DASH NO.		PARTS LIST

SCALE:
TOL # | 2 PLC | 3 PLC | ANGLE
MATERIAL:
FINISH:

intel 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE: SCHEMATIC
27-0 PERSONALITY

SIZE	DEPT	DRAWING NO.	REV
D	MCD	2000966	B

SHEET 1 OF 2

1000824 NEXT ASSY | UPP 816 USED ON

Figure B-8. UPP-816 Personality Circuit Assembly (Sheet 1 of 2)

REVISIONS				
LTR	DESCRIPTION	DFT	CHK	ENGR
	SEE SHEET 1			

Figure B-8. UPP-816 Personality Circuit Assembly (Sheet 2 of 2)

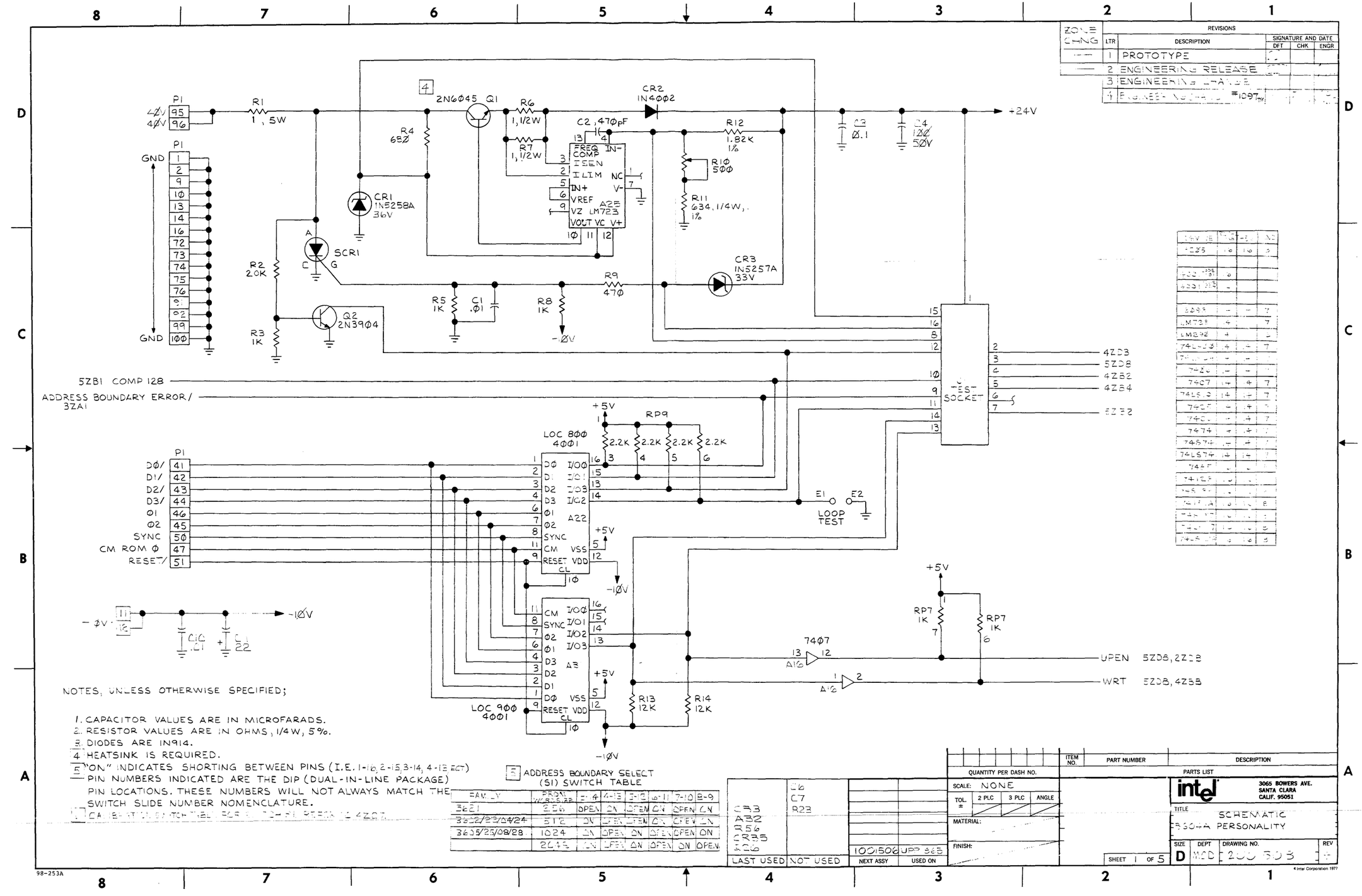


Figure B-9. UPP-865 Personality Circuit Assembly (Sheet 1 of 5)

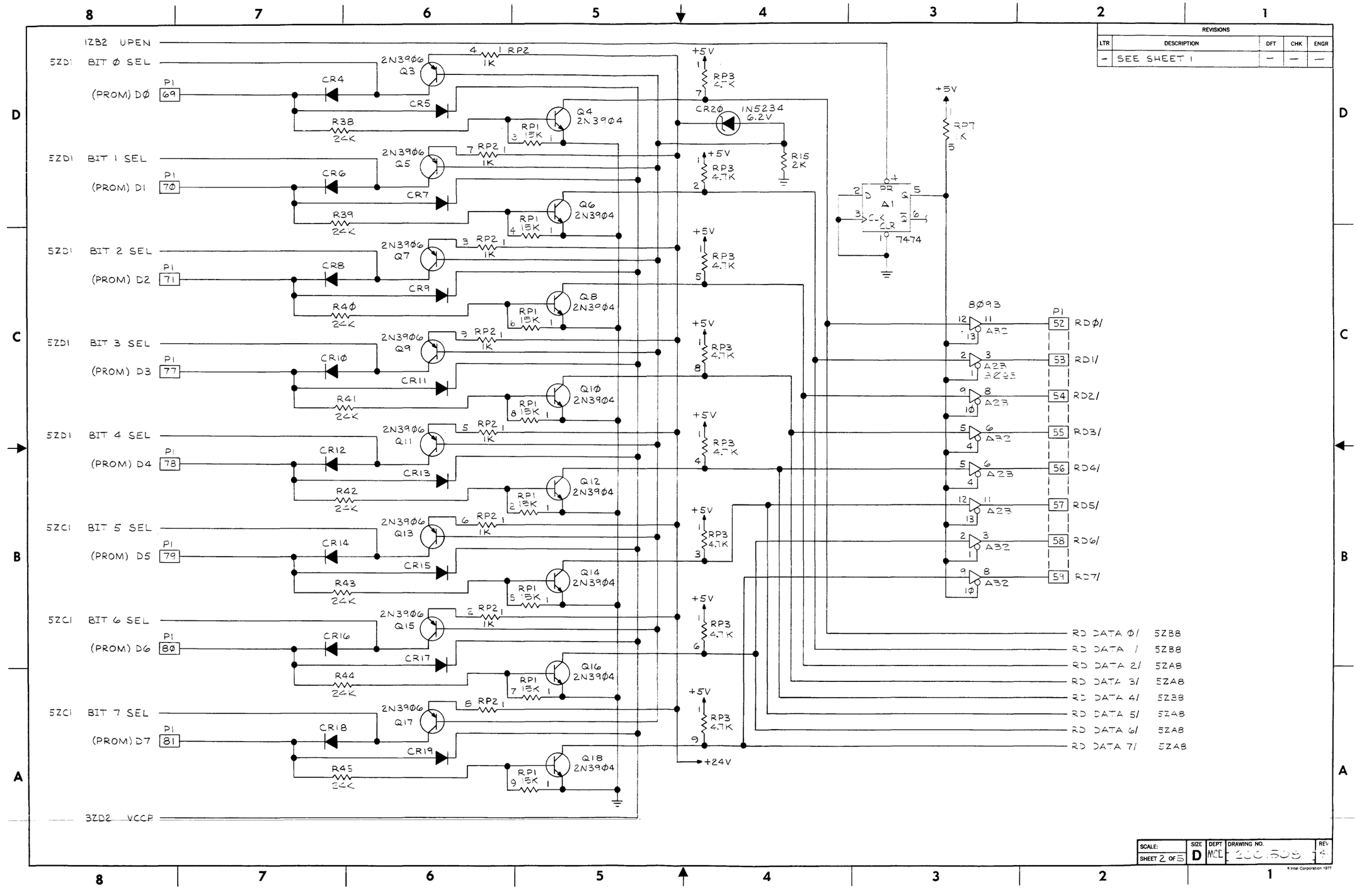
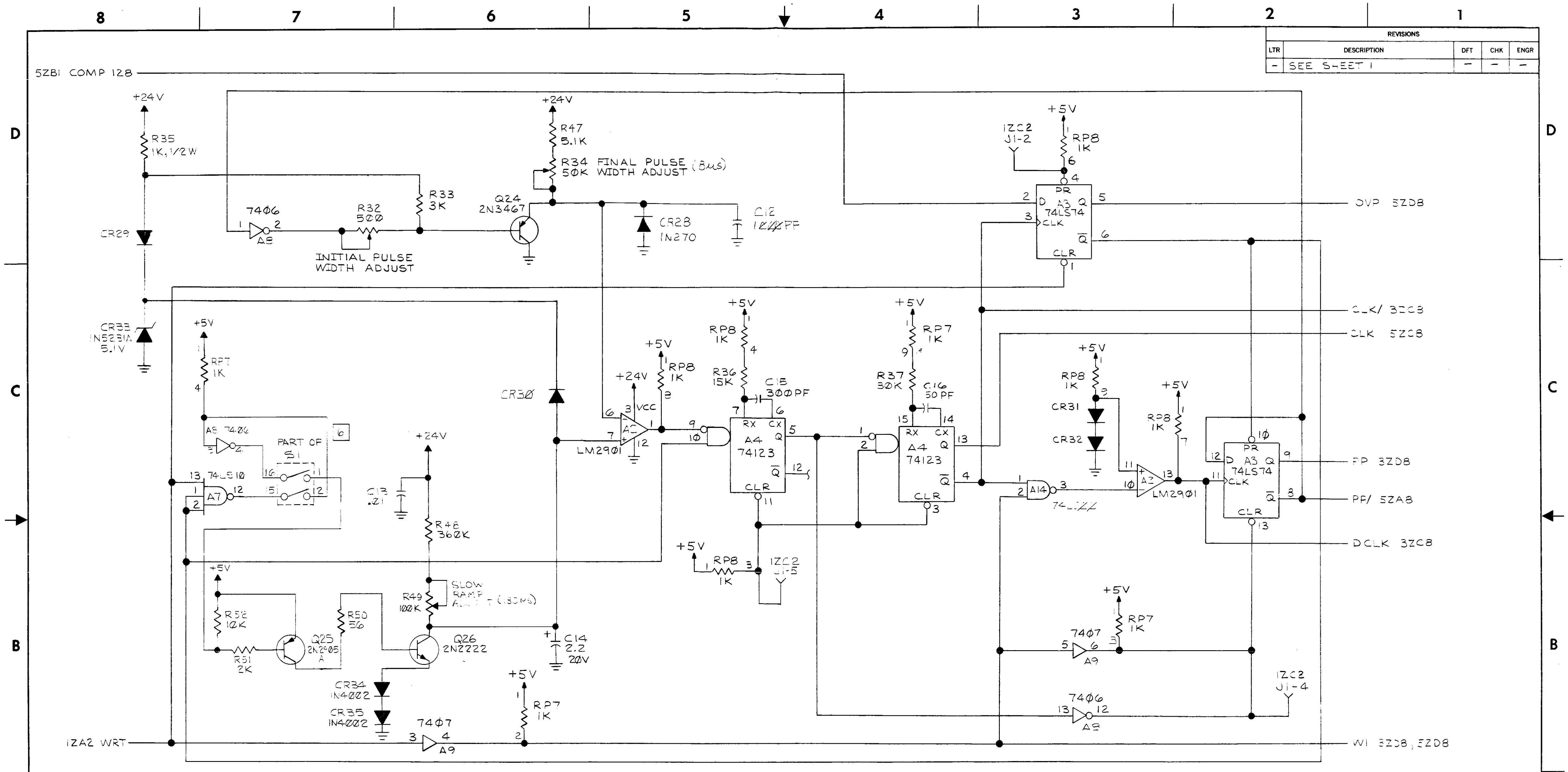


Figure B-9. UPP-865 Personality Circuit Assembly (Sheet 2 of 5)

REVISIONS				
LTR	DESCRIPTION	DFT	CHK	ENGR
–	SEE SHEET 1	–	–	–

Figure B-9. UPP-865 Personality Circuit Assembly (Sheet 3 of 5)



5ZB1 COMP 128
+24V
R35 1K, 1/2W
CR29
CR33 1N5231A 5.1V
7406
A9
R32 500
INITIAL PULSE WIDTH ADJUST
R33 3K
R47 5.1K
R34 FINAL PULSE 50K WIDTH ADJUST (8μs)
Q24 2N3467
CR28 1N270
C12 1000PF
1ZC2 J1-2
+5V
RP8 1K
D A3 Q 74LS74 CLK CLR
OVP 5ZD8
CLK/ 3ZC8
CLK 5ZC8
+5V
RP7 1K
A9 7406
PART OF S1
A7 74LS10
CR30
+24V
C13 .2
R48 360K
SLOW RAMP ADJUST (80μs)
R49 100K
C14 2.2 20V
R52 10K
R51 2K
Q25 2N2905A
R50 56
Q26 2N2222
CR34 1N4002
CR35 1N4002
7407
A9
RP7 1K
LM2901
A4 74123
RP8 1K
R36 15K
C15 300PF
R37 30K
C16 50PF
A4 74123
1ZC2 J1-5
CR31
CR32
A14 74LS00
A2 LM2901
A3 74LS74
FP 3ZD8
PF/ 5ZA8
DCLK 3ZC8
7407 A9
7406 A9
1ZC2 J1-4
1ZA2 WRT
W1 3ZD8, 5ZD8

6

CALIBRATION SWITCH

	S1 SWITCH SETTING 1-16	2-15	LOOP TEST JUMPER E1-E2	ADJUSTMENT
NORMAL	ON	ON	OPEN	
CALIBRATE 800NS VCC	ON	OFF	ON	R32
CALIBRATE 8μs VCC	OFF	OPTIONAL	ON	R34

REVISIONS				
LTR	DESCRIPTION	DFT	CHK	ENGR
-	SEE SHEET 1	-	-	-

SCALE: SHEET 4 OF 5 | SIZE D | DEPT MCD | DRAWING NO. | REV

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Figure B-9. UPP-865 Personality Circuit Assembly (Sheet 4 of 5)

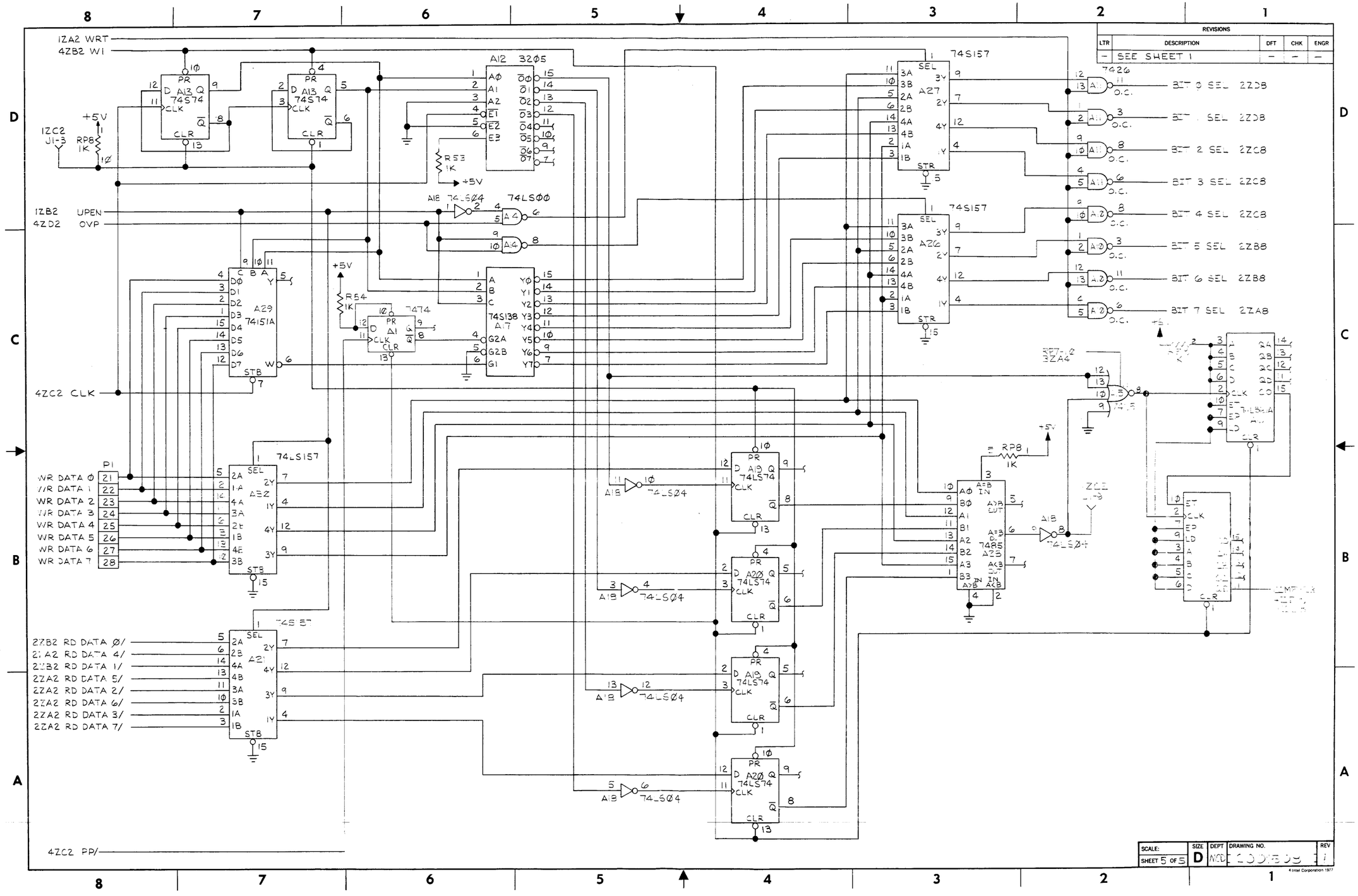


Figure B-9. UPP-865 Personality Circuit Assembly (Sheet 5 of 5)

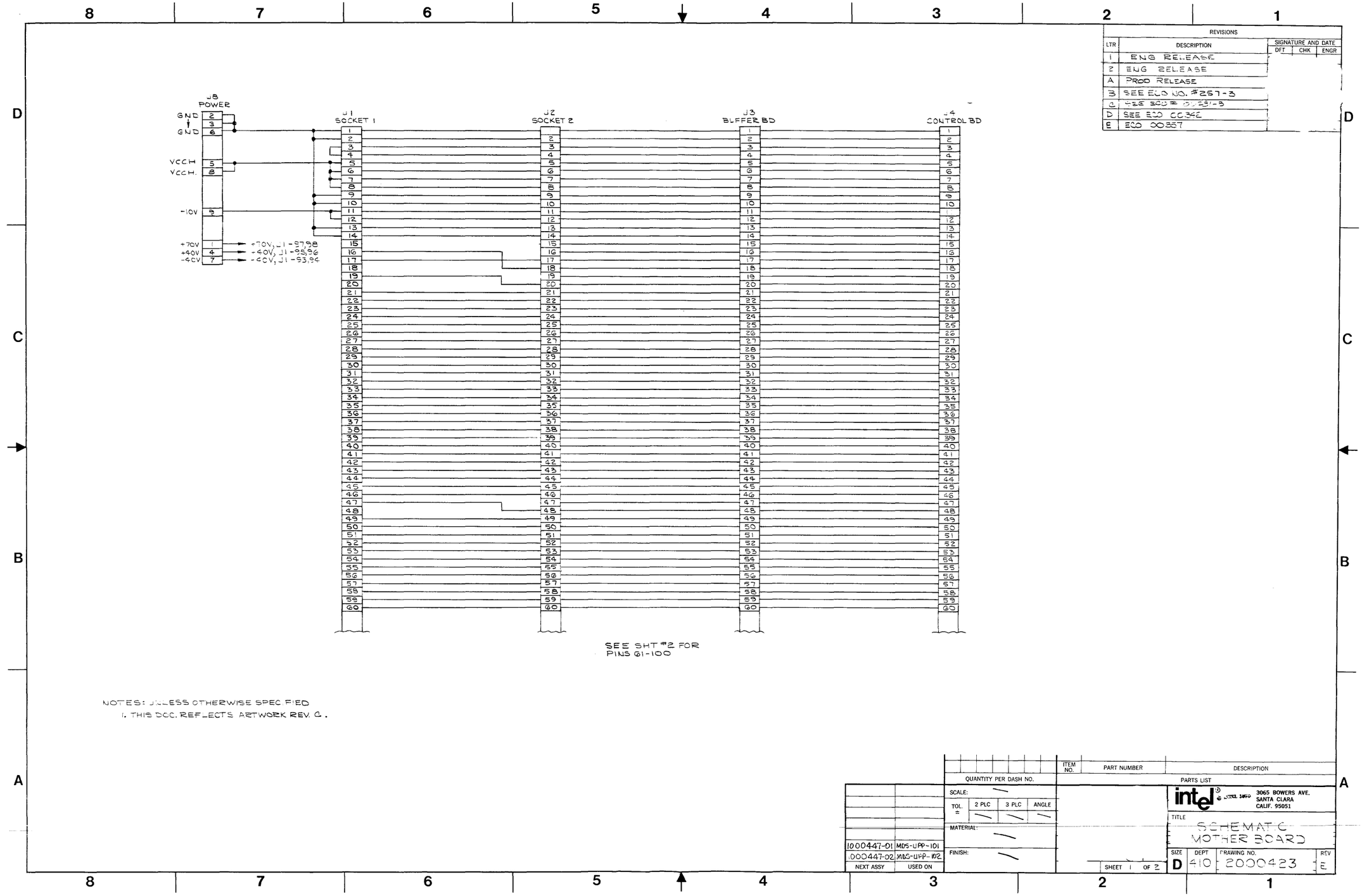


Figure B-10. UPP Mother Board Circuit Assembly (Sheet 1 of 2)

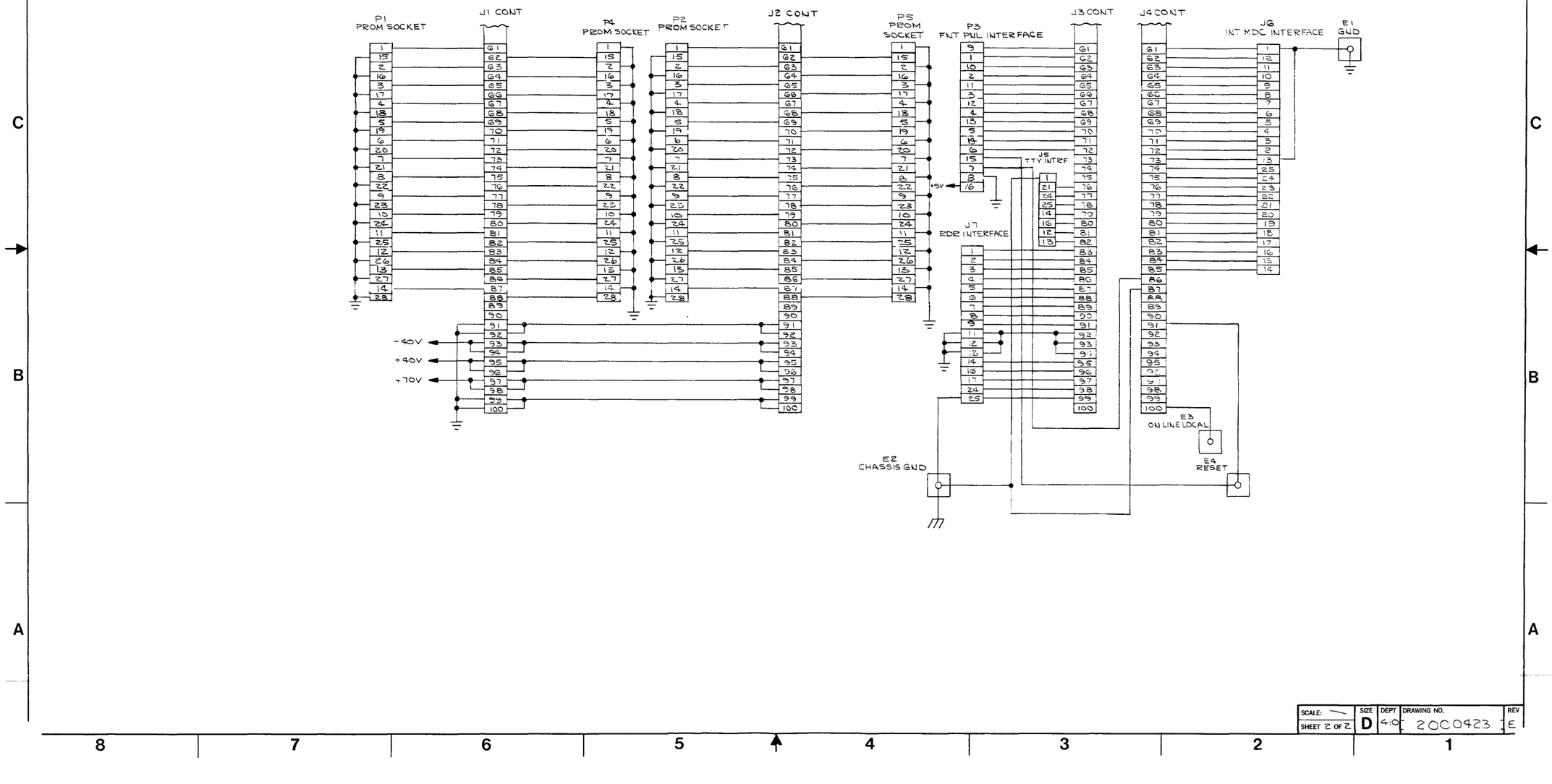
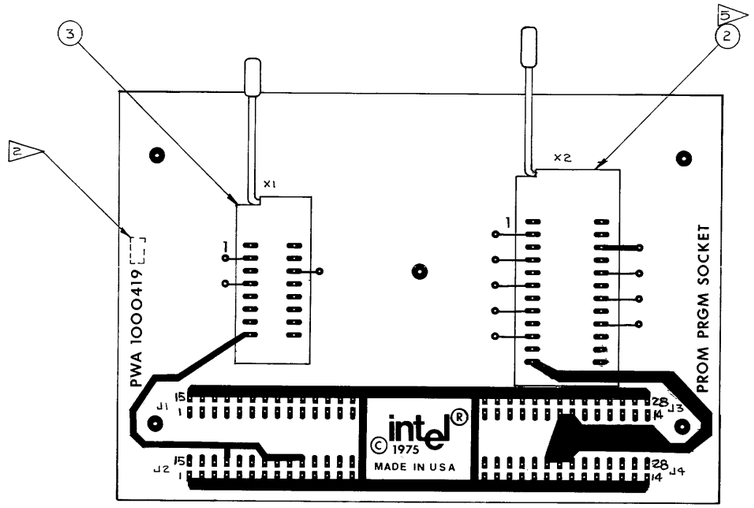
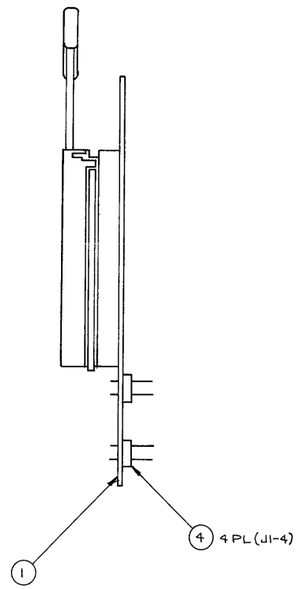


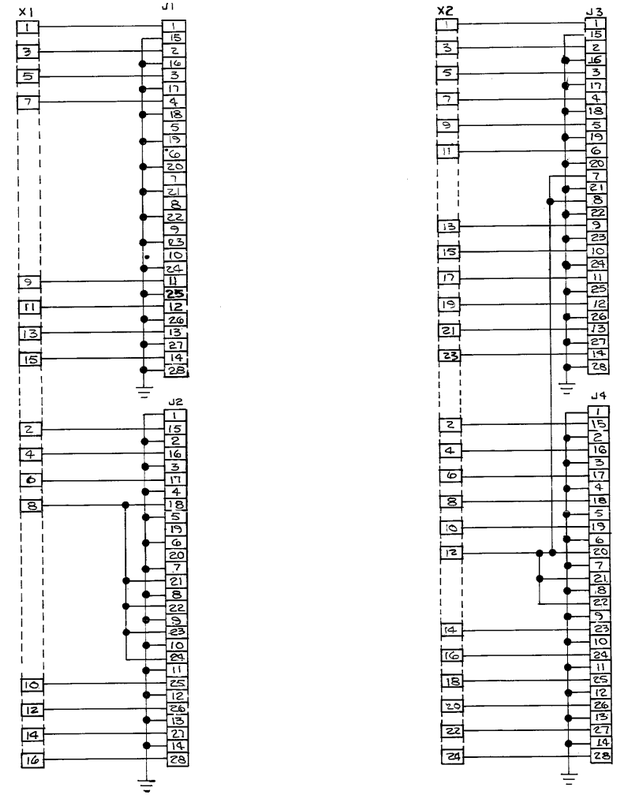
Figure B-10. UPP Mother Board Circuit Assembly (Sheet 2 of 2)

2	ENG RELEASE	
A	PRODUCTION RELEASE	
B	SEE ECO # 00261-1	
C	SEE ECO = 00302	
D	SEE ECO 00500-1	
E	SEE ECO # 00512-1	
F	SEE ECO = 00983-1	





SCHEMATIC



NOTES: UNLESS OTHERWISE SPECIFIED;

1. ASSEMBLY NO. IS 1000419-01.
2. INK STAMP DASH NUMBER & REVISION LEVEL IN POSITION SHOWN. USING CONTRASTING INK CHARACTERS TO BE .12 HIGH.
3. REV. LEVEL OF A/N & PWB ARE THE SAME.
5. ZERO INSERTION PRESSURE SOCKET MOUNTING AND CLEANING INSTRUCTIONS
   - I. MATERIAL NOTE: POLYSUFONE MATERIAL IS GOOD UP TO 150°C CONTINUOUS OPERATION. CLEAN ONLY WITH METHYL ALCOHOL, FREON TE (ONLY) OR WATER AND DETERGENT.
   - II. MOUNTING: THESE SOCKETS ARE DESIGNED PRIMARILY FOR P.C. BOARD MOUNTING OR USE WITH A RECEPTACLE. FOR P.C. MOUNTING SOCKET MUST BE SOLDERED WITH CONTACTS IN THE 'OPEN' POSITION.

ITEM NO	PART NUMBER	DESCRIPTION
4	68-097	CONN, 28 PIN, J1-4
1	68-129	SOCKET 16 PIN, X1
1	68-130	SOCKET 24 PIN, X2
1	1000420-01	PWB PROM PRGM SOCKET 16/24

QUANTITY PER DASH NO — PARTS LIST

SCALE	2:1
TOL: 2 PLC 3 PLC ANGLE	
MATERIAL	5
FINISH	

NEXT ASSY	USED ON
4000848 MDS-UPP-501	
4000571 UPP 501	
4000498 MDS-UPP-104	

SIGNATURE DATE

intel® 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

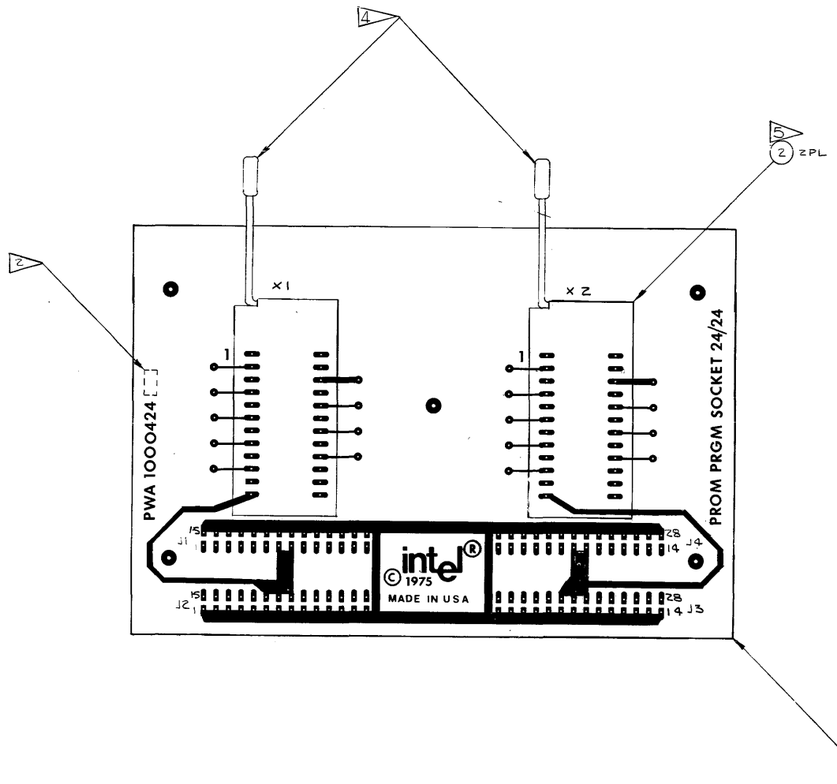
TITLE: PRINTED WIRING ASSEMBLY
PROM PROGRAMMER SOCKET, 16/24

SIZE	DEPT	DRAWING NO	REV
D	MCD	1000419	F

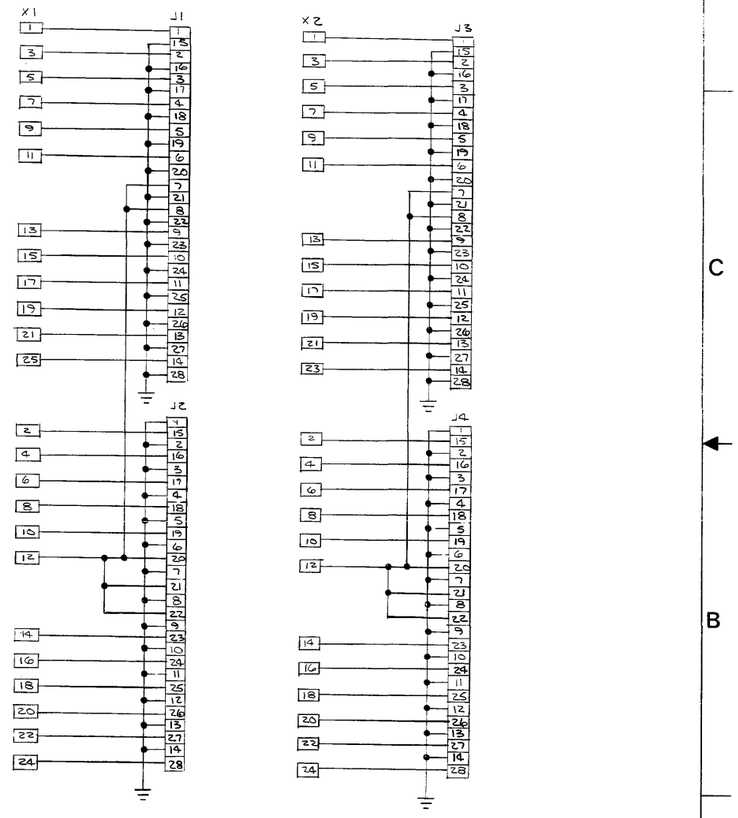
SHEET 1 OF 1

Figure B-12. UPP PROM Socket Assembly (16 & 24 Pin Sockets)

REVISIONS		
LTR	DESCRIPTION	
Z	ENG RELEASE	
A	PRODUCTION RELEASE	
B	SEE ECO 00500-2	
C	SEE ECO# 00512-2	



SCHEMATIC 5



NOTES: UNLESS OTHEWISE SPECIFIED;

1. ASSY NO. IS 1000424-01.
2. INK STAMP DASH NUMBER IN POSITION SHOWN USING CONTRASTING INK CHARACTER TO BE .12 HIGH MIN.
3. LATEST ARTWORK REV NO. IS 'A'.
4. CLOSE CONTACTS ON SOCKETS BEFORE SOLDERING.
5. ZERO INSERTION PRESSURE SOCKET MOUNTING AND CLEANING INSTRUCTIONS.
   - I. MATERIAL NOTE: POLYSUFONE MATERIAL IS GOOD UP TO 150°C. CONTINUOUS OPERATION. CLEAN ONLY WITH METHYL ALCOHOL, FREON TE (ONLY) OR WATER AND DETERGENT.
   - II. MOUNTING: THESE SOCKETS ARE DESIGNED PRIMARILY FOR P.C. BOARD MOUNTING OR USE WITH A RECEPTACLE. FOR P.C. MOUNTING SOCKET MUST BE SOLDERED WITH CONTACTS IN THE 'OPEN' POSITION.

ITEM NO.	PART NUMBER	DESCRIPTION
4	3	68-097	CONN 28 PIN, J1-4
2	2	68-130	SOCKET, 24 PIN, X1-2
1	1	1000425	PWB PROM PRGM SKT, 24/24
-01			PARTS LIST

QUANTITY PER DASH NO.

NEXT ASSY	USED ON
9000572	UPP 502
4000848	MDS UPP 102
4000448	MDS UPP 102

SCALE: 2:1

TOL. ±	2 PLC	3 PLC	ANGLE

MATERIAL: 5

FINISH:

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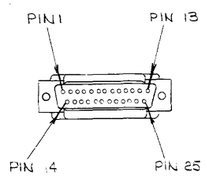
TITLE: PRINTED WIRING ASSEMBLY PROM PRGM SOCKET, 24/24

SIZE	DEPT	DRAWING NO.	REV
D	410	1000424	C

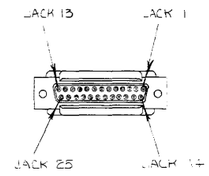
SHEET 1 OF 1

Figure B-13. UPP PROM Socket Assembly (24 Pin Sockets)

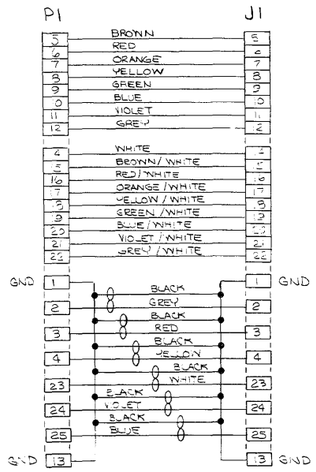
REVISIONS	
LTR	DESCRIPTION
1	ENGR RELEASE
A	PROD RELEASE
B	SEE ECO# D0818
B1	UPDATED N/A USED ON

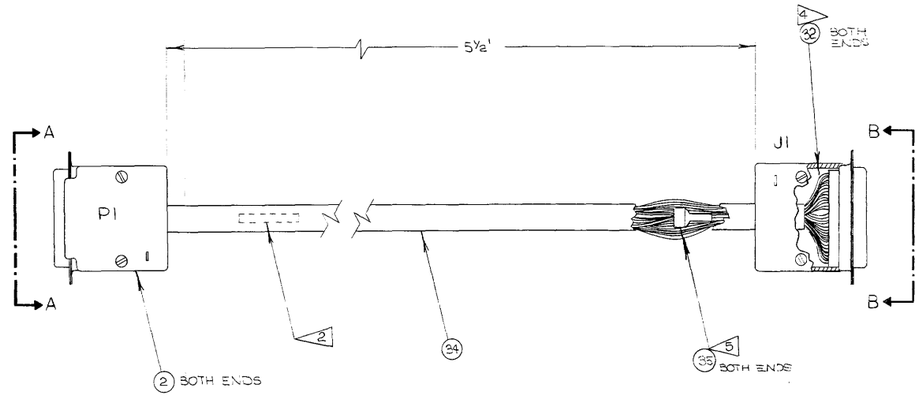


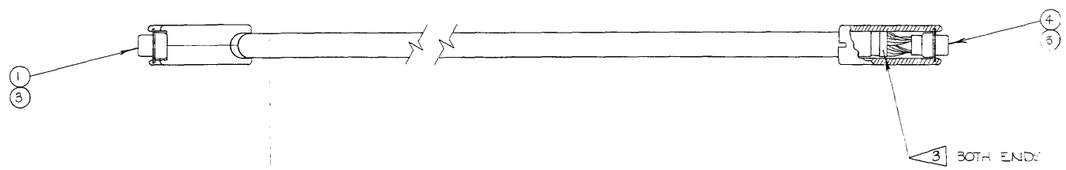
VIEW A-A
(SCALE 1/1)



VIEW B-B
(SCALE 1/1)







NOTES:
UNLESS OTHERWISE SPECIFIED,

1. ASSY NO IS 4000520-01.
2. MARK ASSY NO AND REV LTR IN INK APPROX WHERE SHOWN.
3. BRING INSULATION INSIDE HOOD AND PAST TIE WRAP APPROX 1/8" AS SHOWN.
4. RUN ITEM 32 FROM PIN/JACK 1 TO PIN/JACK 13. SOLDER CONNECT THE BLACK INSULATED GND WIRES OF THE TWISTED PAIRS TO THIS BARE WIRE.
5. TERMINATE BLACK GND WIRES IN LARGE END OF ITEM 35. RUN TWO SINGLE BLACK WIRES (ITEM 32) FROM SMALL END OF ITEM 35 INTO CONNS J1, P1 (ITEMS 1, 4) AND TERMINATE AT PINS 1 AND 13.

ITEM NO.	PART NUMBER	DESCRIPTION
QUANTITY PER DASH NO.		PARTS LIST

NEXT ASSY	USED ON
4000843	MDS-UPP 2151
4000844	MDS-UPP 2251
4000369	MDS UPP 102
4000368	MDS UPP 101

SCALE: 1/1
TOL. ± | 2 PLC | 3 PLC | ANGLE
MATERIAL: SEE P.L.
FINISH:

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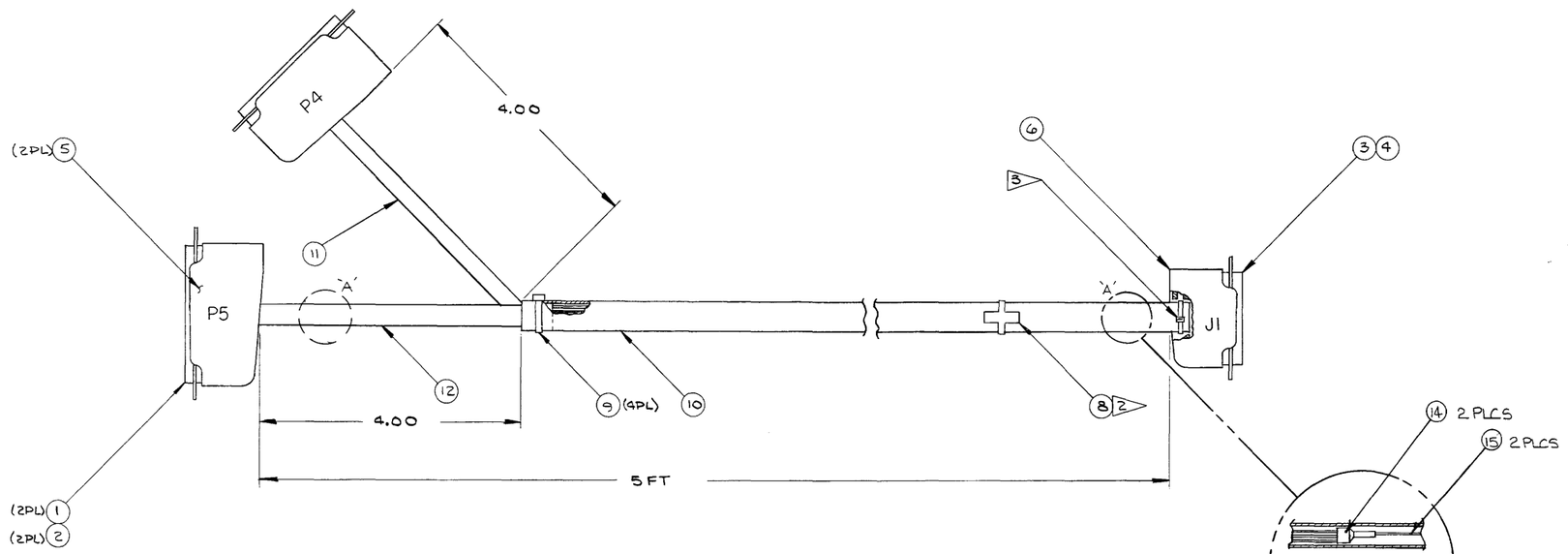
TITLE: UNIVERSAL MULTIMASTER UP CABLE

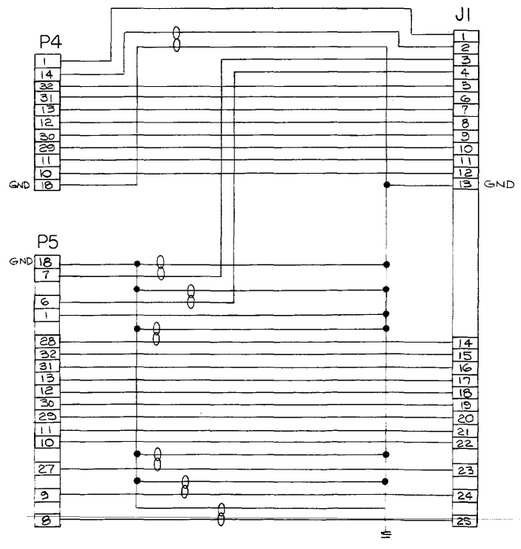
SIZE	DEPT	DRAWING NO.	REV
D	410	40[illegible]002	B1

Figure B-14. UPP-Intellec 8 Interconnecting Cable Assembly

REVISIONS	
LTR	DESCRIPTION
1	ENG RELEASE
A	PROD REL
B	SEE ECO #00343
C	SEE ECO #00394
D	SEE ECO #006116



SKETCH A (2 PLCS)



NOTES: UNLESS OTHERWISE SPECIFIED;

1. P/N IS: 4000544-01.
2. INK STAMP P/N & REV LTR IN POSITION SHOWN.
3. INSTALL TIE WRAP INSIDE CONN HOOD AS SHOWN. (TYP)

ITEM NO.	PART NUMBER	DESCRIPTION
PARTS LIST		

NEXT ASSY	USED ON
4000631	IMM6-90
4000622	IMM8-92
4000621	IMM8-91

QUANTITY PER DASH NO.

SCALE: 1:1

TOL ±	2 PLC	3 PLC	ANGLE
	.125		

MATERIAL: SEE P/L

FINISH:

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TITLE CABLE ASSEMBLY, INTELLEC 8, INTELLEC 8/MDS80 /UPP

SIZE	DEPT	DRAWING NO.	REV
D	410	4000544	D

Figure B-15. UPP-MDS Interconnecting Cable Assembly

APPENDIX C

2708 AUXILIARY PROGRAMMING

SOFTWARE INSTRUCTION

SECTION 1

GENERAL INFORMATION

INTRODUCTION

The Intel®2708, 2704, 8708, and 8704 are eraseable, programmable, read-only memory chips (PROMs). The 2704 and 8704 each contain 4096 bits, arranged as 512 8-bit bytes. The 2708 and 8708 each contain 1024 8-bit bytes. All of these PROMs may be programmed easily using the Universal PROM Programmer (UPP) attachment on the Intellec MDS, erased by exposure to ultraviolet light, and reprogrammed as often as desired. The special construction used in this family of PROMs, however, requires a slightly different programming algorithm from the one normally used to program other Intel PROMs. Therefore, the PROM programming command of the Intellec MDS Monitor cannot be used. The 2708 PROM family may be programmed using Intel's Universal PROM Mapper or the P2708 programming tape supplied with the UPP-878 Personality Card. The following instructions will describe implementation of the P2708 program.

HARDWARE CONFIGURATION

The 2708 PROM Programmer requires the following hardware configuration for support:

- Intellec MDS system (including the MDS Monitor)
- 2K bytes of memory
- Interactive CONSOLE device
- Paper tape reader
- Universal PROM Programmer

USING THE PROGRAM

The program's origin point is 20 (hex). Once the object code has been loaded using the Monitor RØ command, the G command of the monitor is used to initiate execution. The following command line will start execution:

.G20

The prompt character, ":", indicates the program has been successfully entered. All P2708 commands are identical to the monitor commands used for programming 1702As.

NOTE: The P2708 program requires that data to be programmed into a 2708 PROM be provided in 1K blocks.

For example: :PTX1000,13FF,0

1K

SECTION 2

PROGRAM COMMANDS

INTRODUCTION

The Universal PROM Programmer is the hardware device which allows the user to program Intel PROMs using the Intellec MDS. The UPP is available in two configurations: one configuration contains one 24-pin socket and one 16-pin socket, while the other contains two 24-pin sockets. The 16-pin socket, if present occupies the "Socket 1" position on the UPP front panel. The 16-pin socket is used for programming PROMs having a word size of 4 bits, and consequently is not used when programming a 2708-type PROM (which has a word size of 8 bits).

The three commands which are used with the UPP each require two alphabetic parameters, in addition to numeric parameters. One of these is referred to below as <socket option>, which specifies whether the PROM being acted upon is in Socket 1 or Socket 2. A 2708-type PROM can be in Socket 1 only if the UPP is configured with 2 24-pin sockets. This parameter may take on the values X, Y, or Z, which have the following meanings:

X	Select Socket 2 on the UPP for this operation. Treat all data as 8-bit quantities.
Y or Z	Select Socket 1 on the UPP. Treat all data transfers as 8 bits.

The other alphabetic parameter required by all three programming commands is the <true/false> or <t/f>, parameter. This parameter establishes the "sense" of the PROM with respect to MDS RAM, as follows:

> If <t/f> = T, the program assumes that the data in PROM appears in the same sense as it does in MDS RAM; i.e., a "1" bit in PROM corresponds to a "1" bit in RAM, and a "0" bit in PROM corresponds to a "0" bit in RAM.
>
> If <t/f> = F, the program assumes that the data in PROM is the complement of the corresponding data in MDS RAM: i.e., a "1" bit in PROM corresponds to a "0" bit in RAM, and vice versa.

Each command below requires the UPP to be connected to the Intellec MDS, with power on, at the time the command is entered. If the UPP is not in a READY state, the program will immediately issue an error indicator (*) as the command is entered.

PROM PROGRAMMING - P

P <t/f> <socket option> <low address>, <high address>, [<PROM address>]

The P command programs the PROM in the socket specified by <socket option> with data taken from MDS memory locations <low address> through <high address>. <high address> must be equal to <low address> + 1FF (hex) when programming a 2704 or 8704, or to <low address> + 3FF (hex), when programming a 2708 or 8708. Data from <low address> is transferred to the PROM starting at PROM address 0. <PROM address> is optional, but if present must evaluate to 0. If <t/f> = F, the data from MDS memory is complemented as it is transferred to the UPP. The data in MDS memory always remains unchanged.

After the entire PROM has been programmed, the program reads back and compares each location in the PROM with the original data in the MDS memory. If the two values differ, the program displays a discrepancy message consisting of the memory address, the memory contents (showing only those bits being compared), and the PROM contents (showing only those bits being compared). One such message is displayed for every discrepancy found. If no discrepancies are found, a new prompt (:) is issued.

COMPARE - C

C<t/f> <socket option> <low address>, <high address>

The C command compares the contents of a PROM located on the UPP, in the socket specified by the <socket option> input parameter, with the contents of memory in the area specified by the input parameters <low address> through <high address>. If the contents of a PROM location are not equal to the contents of the corresponding memory location, the memory address, contents of the memory location, and the contents of the PROM are printed on the CONSOLE for inspection.

For example, the contents of a PROM is specified as true logic, and is to be compared with the contents of memory from 3000H to 33FFH. The C command would be as follows:

```
:CTX3000,33FF
```

Assume that the contents of memory locations 3006 and 3081 are not equal to the contents of the corresponding PROM locations. The program will print the following message:

```
3006 AA FF                    (typical data)
3081 00 01   RAM   PROM
```

TRANSFER PROM - T

T<t/f> <socket option> <low address>, <high address>

The T command transfers the contents of the PROM in the socket specified by socket option to the area of MDS RAM specified by the <low address>, <high address> pair. If the range of memory locations is smaller than the contents of the PROM, the excess data in the PROM is disregarded. If the range is greater than 1024 bytes (400 hex), the PROM data will be transferred; the excess memory locations will remain unchanged. If the range is greater than 512 bytes (200 hex), and a 2704 or 8704 PROM is being used, the data transferred from PROM address above 1FFH is undefined. If <t/f> = F, the data coming from the UPP is complemented before being stored in MDS RAM.

The program always receives 8 bits of data from the UPP, and stores the entire 8 bits in the next consecutive RAM location. Therefore, a <socket option> of either Y or Z may be used to transfer data from a 24-pin PROM located in Socket 1 of the UPP.

For example, a user wishes to transfer the data in a 2708 PROM to memory locations 4000 to 43FF. The status of the data is false logic. A typical T command appears as follows:

```
:TFX4000,43FF
```

The E command is used to transfer control back to the MDS monitor. The command requires no arguments, and is legal even if a UPP is not connected to the MDS. After the user enters:

```
:E
```

the MDS Monitor will display a message form:

```
*0093                    (typical data)
```

The number may be disregarded. The '.' indicates that control has passed to the MDS monitor and that the monitor is now ready to accept commands.

SECTION 3

PROGRAM ERROR CONDITIONS

INTRODUCTION

The program checks for several error conditions. Whenever an error is deteced, the error character (*) is output to the CONSOLE. A command containing an error is never processed past the point at which the error is discovered.

INVALID CHARACTERS

The program checks the validity of each character as it is entered from the CONSOLE. As soon as the program determines that the last character entered is illegal in its context, it aborts the command and displays a '*' to indicate the error.

For example, suppose a character 'G' is entered in a parameter list where only hexadecimal digits (0-9, A-F) and delimiters (comma, space, carriage return) are valid. The output on the CONSOLE will be as follows:

```
:TTX3000,31G*
```

Suppose that the character 'Y' is used as a command. The program will reject this character and indicate the error as follows:

```
:Y*
```

ADDRESS VALUE ERRORS

Except for the E command, all commands accept an address pair of the form <low address>, <high address>. If, in these commands, the value of <low address> is greater than the value of <high address>, the action indicated by the command will be performed on the data at <low address> only (see the section on the P command for additional address restrictions for that command).

Addresses are evaluated modulo 65,536. Thus, if a hexadecimal address of more than FFFFH (four digits) is entered, only the last four digits are significant. For example, suppose the following address range were entered:

```
:TTX04532AC,945216FCF
```

The above command would be equivalent to TTX32AC,6FCF.

In the P command, the <PROM address> is evaluated modulo 400H, and must evaluate to 0, if present.

Another type of address error may occur when the user specifies an address in memory which does not exist in the Intellec MDS system. For example, a user with a 16K system may enter an address above the highest memory address, as follows:

```
:TTX4000,41FF
```

No error indication is generated by the program for these error addresses. In general, if the source address (address from which data is taken) is nonexistent, the data fetched is unpredictable. If the destination address (address to which the data is to be transmitted) is nonexistent, the command has no effect.

PROM PROGRAMMING ERRORS

If an error is signaled from the UPP during a read PROM operation (the P, C, and T commands all read from the PROM), the command is terminated and a '*' message is output on the CONSOLE. If the UPP is not connected to the MDS when a P, T, or C command is input, and error condition is immediately indicated with the '*' message on the CONSOLE.

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