

M46-250

HIGH SPEED PAPER TAPE READER AND READER PUNCH COMBINATION INTERFACE INSTRUCTION MANUAL

CONSISTS OF:

Installation Specification	02-265A20
Maintenance Specification	02-265R01A21
Programming Specification	02-265R01A22
Schematic	02-265D08
Information Drawing	02-298D12
Information Drawing	02-299D12

**INTERDATA**[®]

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M46-250

HIGH SPEED PAPER TAPE READER AND READER/PUNCH COMBINATION INSTALLATION SPECIFICATION

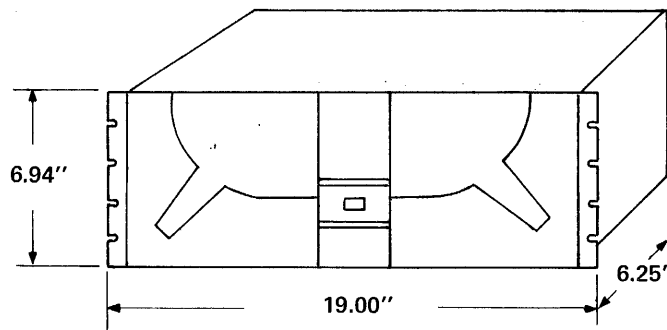
1. INTRODUCTION

This specification provides the information necessary to install the High Speed Paper Tape Reader System and the High Speed Paper Tape Reader/Punch Combination System in a standard INTERDATA 66 inch cabinet.

2. MECHANICAL ASSEMBLY

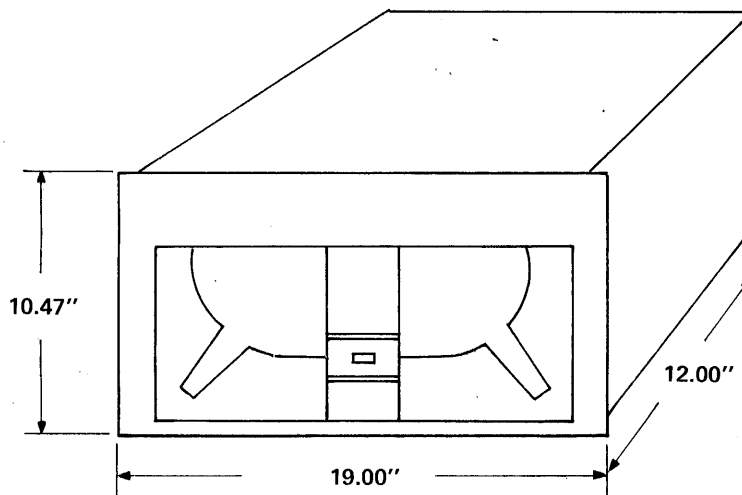
The INTERDATA High Speed Paper Tape Reader System consists of a Paper Tape Reader (27-045), a single seven inch controller (35-439), an interface cable (17-220), and a hardware kit (16-160).

The INTERDATA High Speed Paper Tape Reader/Punch Combination System consists of a Paper Tape Reader/Punch Combination unit (27-046), a single seven inch controller (35-439), an interface cable (17-220), a bracket set (14-363), and a hardware kit (16-160). The physical characteristics of the assembly are shown in Figure 1.



WEIGHT-26.5 LBS.

READER



WEIGHT-60 LBS.

READER/PUNCH

Figure 1. Reader and Reader/Punch Dimensions

A. C. POWER REQUIREMENTS

The INTERDATA High Speed Paper Tape Reader and the High Speed Paper Tape Reader/Punch Combination Systems are normally equipped for 115 VAC, 50/60 Hz operation. For operation with 230 VAC, 50/60 Hz, a minor wiring change is made by removing the cover plate and changing the wiring on the primary of the transformer as follows:

1. Reader Only

Change the White/Black wire at TB1-6 to TB1-5 for 100 VAC, to TB1-7 for 127 VAC, to TB1-8 for 220 VAC, or to TB1-9 for 240 VAC. The fan must remain tied to TB1-6. In addition, a 1.5 amp fuse must be substituted for the 3 amp fuse at F1 when using 220 or 240 VAC. See Figure 2 and the Vendor Technical Manual for detailed information.

2. Reader/Punch Combination

Change the Red wire at TB1-6 to TB1-5 for 100 VAC, to TB1-7 for 127 VAC, to TB1-8 for 220 VAC, or to TB1-9 for 240 VAC. The fan must remain tied to TB1-6. In addition, a 2 amp fuse must be substituted for the 4 amp fuse at F1 when using 220 or 240 VAC. See Figure 2 and the Vendor Technical Manual for detailed information.

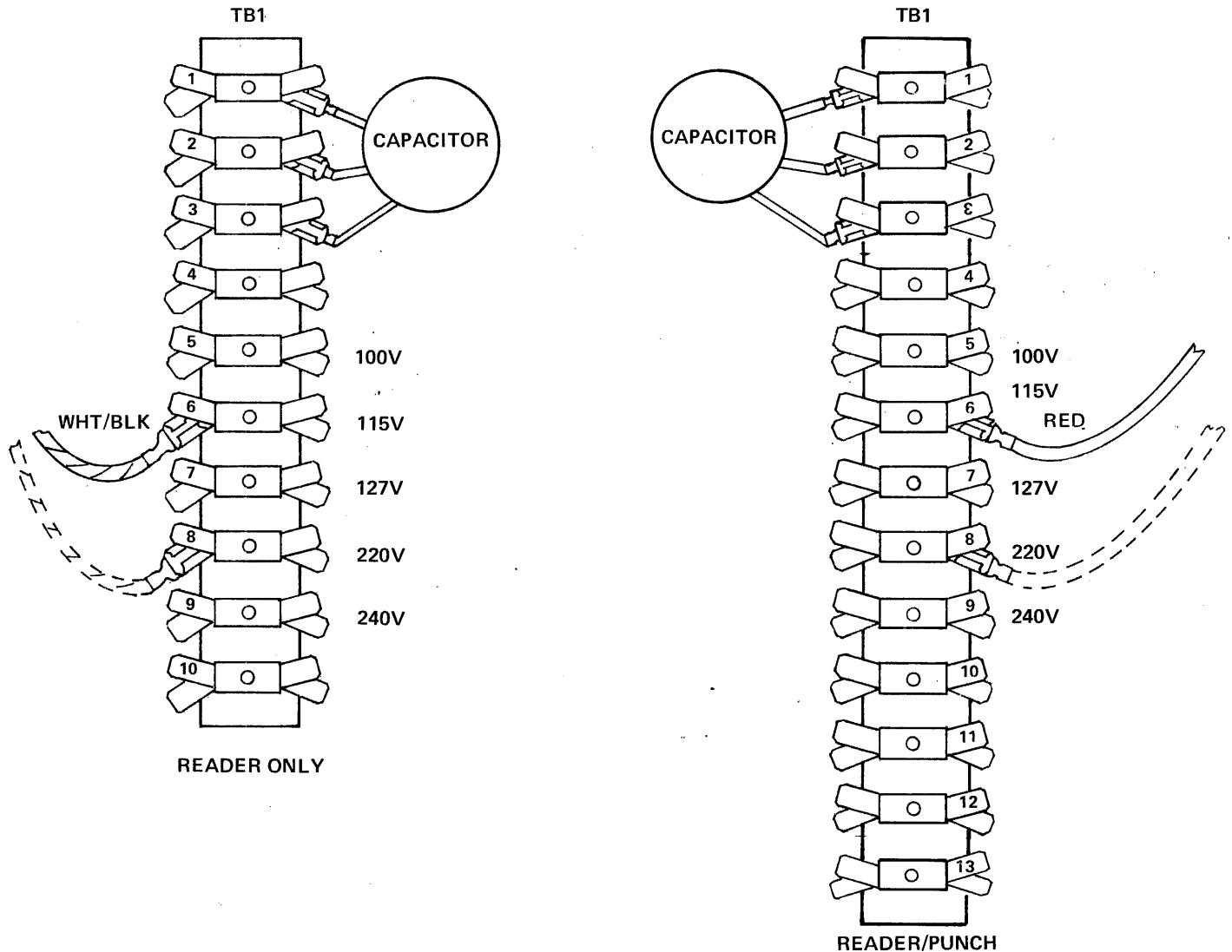


Figure 2. Transformer Wiring Change for Voltages Other Than 115VAC.

4. MOUNTING

4.1 Reader Only

The Reader can be mounted in any standard 19 inch RETMA cabinet or rack. For mounting instructions and procedures, refer to drawing 02-298C12 provided in the Instruction Manual, Publication Number 29-290.

4.2 Reader/Punch Combination

The Reader/Punch Combination unit contains chassis slides which mount to the cabinet. In addition, the front panel secures to the cabinet by means of two mounting studs which snap into sockets. These studs are part of two striker plates which are mounted on each side of the rack by two screws each. To release the sockets from the studs, depress the buttons at the top of the panel. For detailed information, refer to drawing 02-299C12 provided in the Instruction Manual, Publication Number 29-290.

5. SYSTEM CONFIGURATION

The High Speed Paper Tape Reader and Punch Controller may be installed in any standard 15 inch I/O slot of an INTERDATA Processor or expansion card file. Remove the RACKO/TACKO Strap between Back Panel Terminals 122 and 222 at the Controller location. The Controller device address is normally wired for X'13' and X'03'. If a set of addresses different from the normal set is desired, the address strapping at the Controller must be altered.

Information for changing the addresses is provided in the Maintenance Specification 02-265A21.

6. CABLE CONNECTIONS

Figure 3 shows the proper cable connections between the Controller and the Reader only. Note that J1 (CANNON DB-25P) is not used.

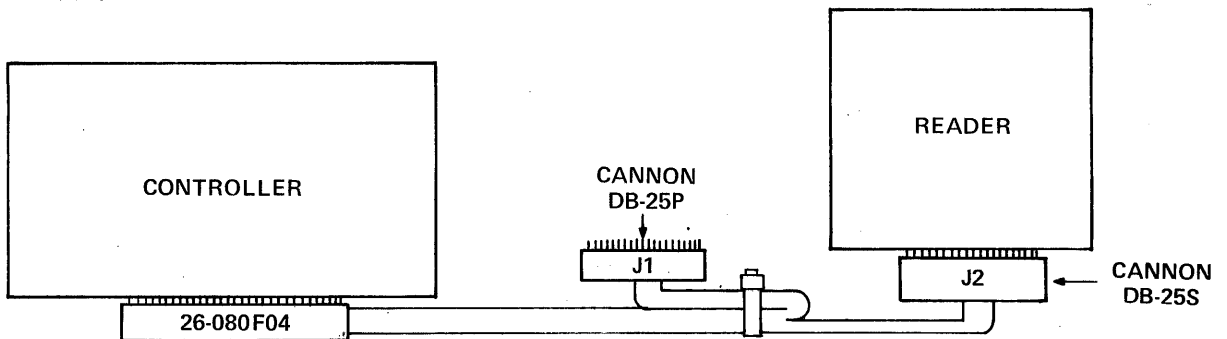


Figure 3. Cable Connection - Controller to Reader

Figure 4 shows the proper cable connections between the controller and the Reader/Punch Combination unit.

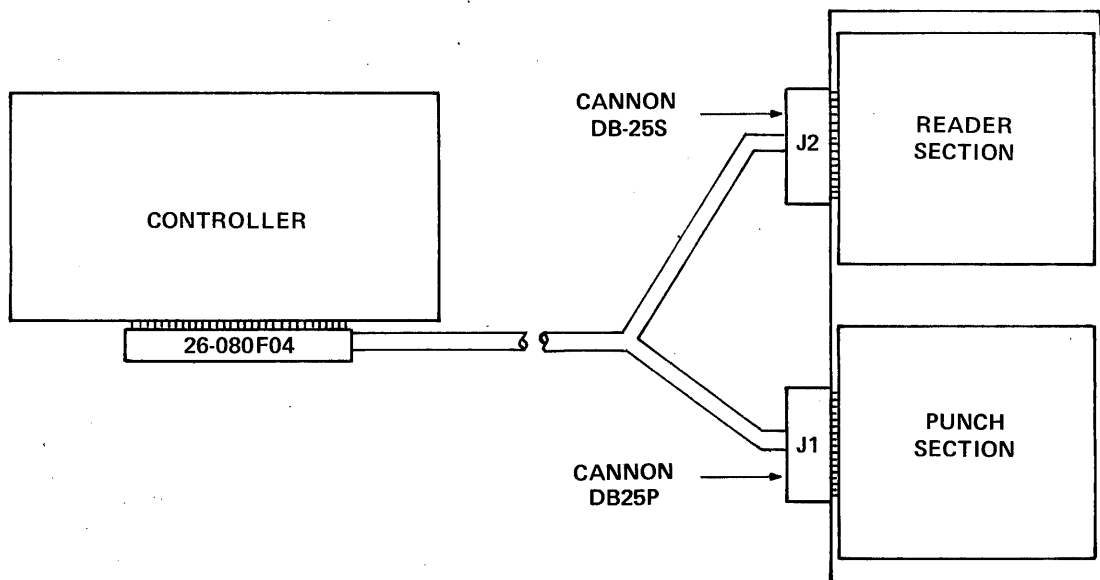


Figure 4. Cable Connection - Controller to Reader/Punch

7. VERIFICATION TEST

After installation, run test program 06-137 to determine that the unit is operating correctly.

M46-250

HIGH SPEED PAPER TAPE READER AND READER PUNCH COMBINATION INTERFACE MAINTENANCE SPECIFICATION

1. INTRODUCTION

The INTERDATA High Speed Paper Tape Reader System consists of a Paper Tape Reader, a single 7 inch controller, and an interface cable. The paper tape reader is rack mounting and equipped with a built-in Power Supply.

The INTERDATA High Speed Paper Tape Reader/Punch Combination System consists of a Paper Tape Reader and a Paper Tape Punch, a single 7 inch controller, and an interface cable. The Reader and Punch are contained in a single unit which mounts on slides and is equipped with a built-in Power Supply.

The following is the relationship between Product Number and Part Number for the various INTERDATA Products.

PRODUCT NUMBER	PART NUMBER	DESCRIPTION
M46-240	02-298	High Speed Paper Tape Reader, 60 Hz, 115V
M46-241	02-300	High Speed Paper Tape Reader, 50 Hz, 230V
M46-242	02-299	High Speed Paper Tape Reader/Punch, 60 Hz, 115V
M46-243	02-301	High Speed Paper Tape Reader/Punch, 50 Hz, 230V
M46-250	02-265	High Speed Paper Tape Reader/Punch Interface

2. SCOPE

This specification provides the information necessary to maintain the High Speed Paper Tape Reader System and the High Speed Paper Tape Reader/Punch Combination System. It includes a Block Diagram, Functional Schematic Analysis, Device Address Strapping, Timing Information, and a Mnemonics List.

3. BLOCK DIAGRAM

The High Speed Paper Tape Reader performs two basic functions:

1. It drives tape in either direction over the read station.
2. It converts the tape information into electrical signals.

These two functions are shown in the block diagram in Figure 1.

The High Speed Paper Tape Reader/Punch Combination performs two basic functions:

1. It controls the operation of the Punch mechanism in response to the input Control signals.
2. It reads tapes.

These two functions are shown in the block diagrams in Figures 1 and 2.

The Interface block diagram is on Sheet 1 of Functional Schematic 02-265D08. All controls come from the Device Controller.

With the HSPTR/P Interface both the Reader and the Punch use a single device controller. Accordingly it can either read or punch at any given time.

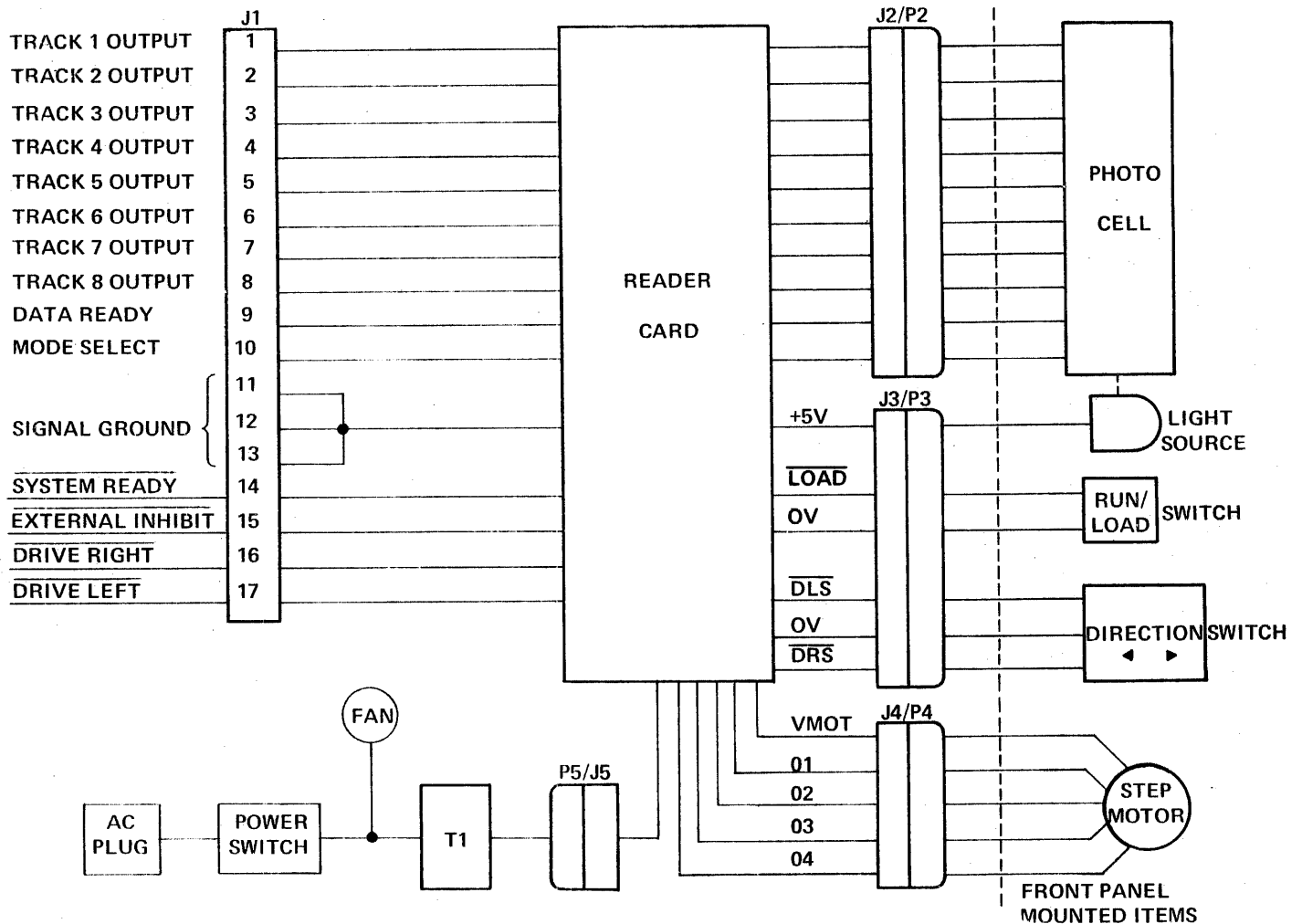


Figure 1. HSPTR Block Diagram

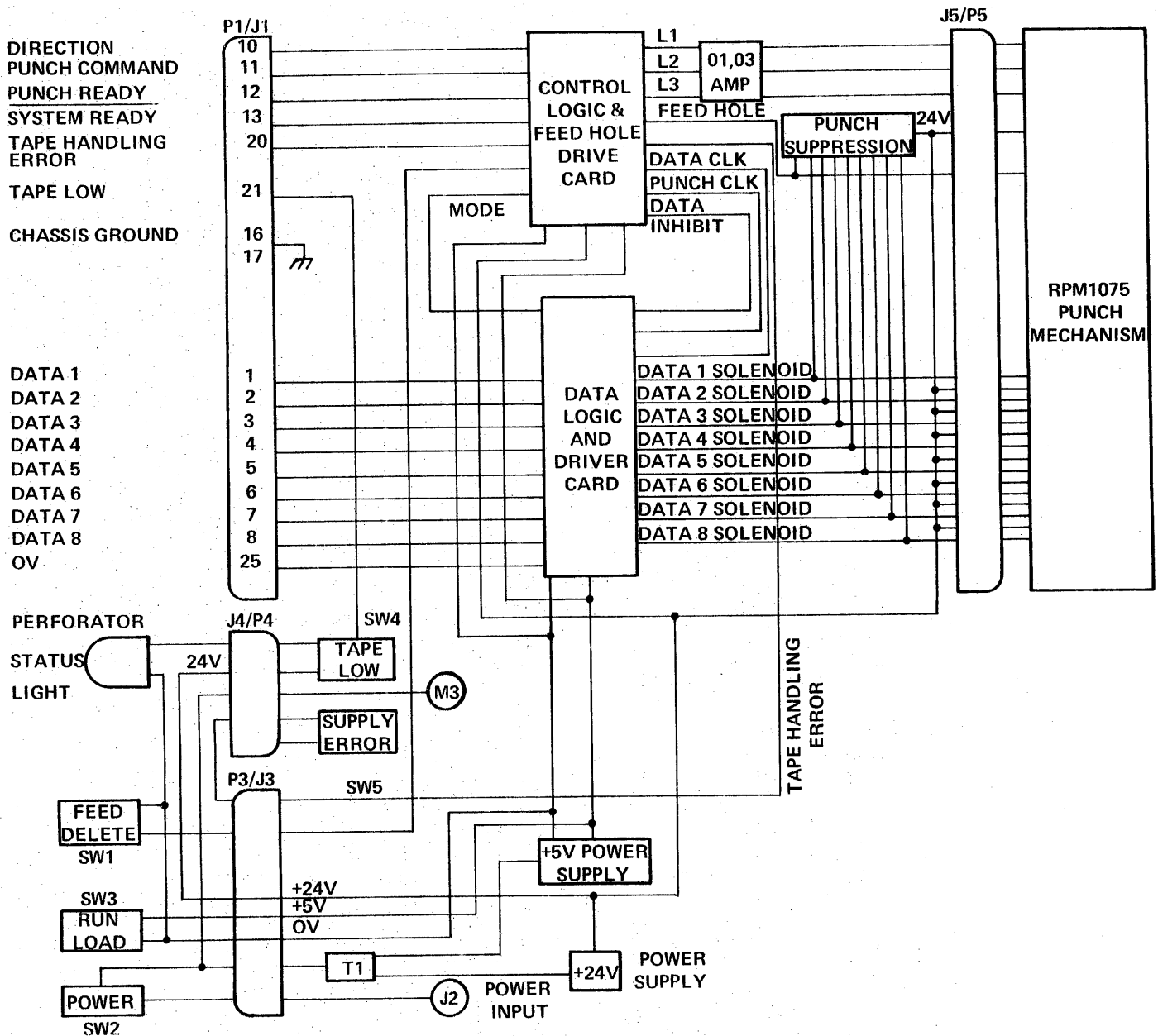


Figure 2. HSPTP Block Diagram

4. FUNCTIONAL SCHEMATIC ANALYSIS

4.1 Addressing

Prior to receiving any commands, the HSPTR/P Device Controller must receive its address and respond properly. This is done through Micro-Sequences which first send the address (X'13' for Reader/Punch Combination, X'03' for Reader only) on the Data Lines (D080 through D150). The Data Lines go through single to double rail converters and address straps which drive a decoding network. The decoding network is ANDed with the inverted signal from ADRS0 and the output sets the Address flip-flop (AD). After a delay, the SYN0 signal goes low and is tested by the Processor to determine if the HSPTR/P has responded to its address. The AD flip-flop being set enables other Modes of operation (e.g. Writing, Reading, Status Request, etc.) in the HSPTR/P Interface. The AD flip-flop is reset by SCLR0 or when another device is addressed.

4.2 Status

The definitions of the Status and Command bits for the HSPTR/P Interface are shown in Table 1. Five Status bits are provided by the HSPTR/P Interface.

The BSY (Busy), EX (Examine), DU (Device Unavailable) and EOM (End of Message-Media) bits occur in the same bit position for all Device Controllers. The HSPTR/P Interface does not use the EOM bit. The EX Status bit is used to indicate that there are other status conditions in the remaining four bits.

TABLE 1. HIGH SPEED PAPER TAPE READER/PUNCH STATUS AND COMMAND BYTE DATA

BIT NUMBER	8	9	10	11	12	13	14	15
STATUS BYTE	OV	0	0	NMTN	BSY	EX	0	DU
COMMAND BYTE	* DISABLE	* ENABLE	STOP	RUN	INCR	SLEW	WRITE	READ

* DISARM = DISABLE • ENABLE

STATUS

BIT	READER	PUNCH
OV	<p>The Overflow bit is set when the Buffer Register is loaded from the Reader before the previous character has been transferred. This condition can only happen in the SLEW Mode. It is reset by:</p> <ol style="list-style-type: none"> 1. Initialization 2. The HSPTR/P changing from Read Mode to Write Mode. 3. The HSPTR/P changing from Write Mode to Read Mode. 4. The Reader changing from STOP to RUN. 	<p>The Overflow bit is always reset in the Write Mode.</p>
DU	<p>The Device Unavailable bit is set when the power to the Reader is OFF, the power is not stabilized, the RUN/LOAD Switch is in the LOAD position, the drive signal is received and a new feed hole is not sensed within 10 milliseconds, indicating either no tape or torn tape. DU also serves as the out-of-tape signal. It is reset when the above conditions are not true.</p>	<p>The Device Unavailable bit is set when the power to the punch is OFF or internal voltages have not stabilized, or RUN-LOAD Switch is in LOAD, or the chad box is full. It is reset when the above conditions are not true.</p> <p>Note that CHAD ERROR is reset by depressing the PERF STATUS Switch.</p>
NMTN	<p>The No Motion Bit is set when the Reader has issued a Stop Command and the tape has been stopped on a character. It is reset when the tape starts moving.</p>	<p>The No Motion Bit is always reset in the Write Mode.</p>
BSY	<p>The Busy bit is set when the Buffer Register is empty, waiting for an output from the Reader. It is also set if the Reader is in the Load condition or the Reader power is not stabilized. It is reset when the above conditions are not true.</p>	<p>The Busy Bit is set when the tape is advancing and in the punch cycle. It is reset when the punch is ready to accept a punch command.</p>
EX	<p>The Examine bit is set whenever OV = 1 or NMTN = 1. It is reset when they are both reset.</p>	<p>The Examine bit is always reset in the Write Mode.</p>

COMMANDS

BIT	READER	PUNCH
DISABLE	This Command inhibits interrupts from the Device Controller from interrupting the Processor. Interrupts are queued.	Same as Reader
ENABLE	This Command permits interrupts from the Device Controller to interrupt the Processor.	Same as Reader
DISARM	Setting both the DISABLE and the ENABLE bits, DISARM prevents the device from interrupting or queuing the interrupts.	Same as Reader
STOP	This Command bit halts the Motion of the tape. The next character to be read is positioned over the sense lights when the tape stops.	Not used.
RUN	This Command starts the tape moving if in the SLEW Mode and always leaves the Controller in the Run Mode.	Not used.
INCR	In this mode of operation, the tape is advanced one character when the Controller is in the Run Mode and a Read Data instruction is executed. The tape stops after encountering the next character. The tape remains stopped until a Read Data instruction, which starts the tape moving again.	Not used
SLEW	In this mode of operation, the tape is advanced continuously until stopped.	Not used
WRITE		Designates the High Speed Paper Tape Punch.
READ	Designates the High Speed Paper Tape Reader.	

4.3 Commands

Any meaningful combination of commands can be simultaneously issued to the Device Controller. The specific command or combination of commands is sent on the Data Lines, followed by the CMD0 signal on the Control Lines. Command enters the Controller as CMD0. This is inverted and ANDed with AD1 to produce CMG0 (Gated Command). This signal is again inverted to gate the bits from the Data Lines to the Command flip-flops.

Because of the dual purpose of the Interface (control of either Read or Write operations), a command to specify a particular operation must be given. If a Read/Run is specified, the WT flip-flop is reset, inhibiting a Write operation from taking place and enabling the status outputs for a Read operation. If a Write operation is specified, the WT flip-flop is set, inhibiting a Read operation from taking place and enabling the status outputs for a Write operation.

Master control over tape movement for the Reader is achieved with the RN flip-flop. When set, the tape moves in a forward direction and the mode is specified by the SL (Slew) flip-flop (continuous run slew if set, one character command increment if reset). When the RN flip-flop is reset, either mode can be established without interfering with the tape movement.

If this Controller is to be used in the interrupt mode, Data Line Bit 9 is set. With D090 active, CMG1 sets the Interrupt Enable flip-flop. Interrupts are generated by the Interface when the reader goes Not Busy (a character is strobed into the Buffer Register from the HSPTR), the Punch goes Not Busy (a character has been output to the HSPTR and the Interface is ready for more data), changes from Write Mode to Read Mode provided the reader is Not Busy, changes from Read Mode to Write Mode provided the Punch is Not Busy, or when the Device Unavailable bit goes true. The interrupt condition is saved in the Attention flip-flop. Enable gates a saved Attention interrupt condition onto the Processor I/O Bus as ATN0. Note that when changing from the Read Mode to the Write Mode, or from the Write Mode to the Read Mode, pending interrupts are cleared, then the busy status of the new device is checked. If the new device is Busy, no interrupt is generated until the device goes Not Busy. If the new device is already Not Busy upon changing Modes, an interrupt will be generated at the time of changing modes.

If the Controller is to be denied interrupt service, Data Line Bit 8 is set. With D080 low, CMG1 resets the Enable flip-flop and sets the Disable flip-flop. Interrupt conditions may still be saved in the Attention flip-flop, but Attention cannot be gated to the I/O Bus. If Data Line Bits 8 and 9 are both set (Disarm), interrupts are neither generated nor queued.

Initialization occurs on power up or when the Initialize Switch on the Processor is depressed. When initialized, interrupts are disarmed. The Disarm, Stop, Increment, and Read Command functions are set and the No-Motion and Examine Status bits are set provided the Reader power is on and the Run/Load Switch is in the Run position.

The active condition on the Initialize Control Line (SCLR0) sets up preferred states by clearing all flip-flops in the Controller. Whenever the Read/Write Mode changes, a partial initialize clears the Overflow, DT, RN, SL, and ATN flip-flops. The operation establishes known control states when changing between the Read and Write Modes, but may be used to clear these flip-flops without changing modes.

4.4 Read Operation

In the Slew Mode of operation, the RN and SL flip-flops are set. This condition, ANDed with FWD1, causes DLT0 (Drive Left) to be active driving the tape to the left continuously until a STOP command is received. The DT flip-flop is reset initially due to either initialization or completion of previous Writes or Reads. This causes BSY1 to be inactive, indicating to the Processor that a character has been read from the paper tape and is awaiting transmission.

The Processor requests data by activating Control Line DR0. The HSPTR/P Interface responds to the Processor request through the derivation of DRG0 which activates the SYN0 signal.

The data which has been previously gated into the HSPTR/P Buffer Register is unloaded onto the Data Lines by the enabling actions of DRG0 through four multiplexors. On the trailing edge of DRG0, the DT flip-flop is set and BSY1 becomes active, indicating to the Processor that the last data has just been taken out of Buffer Register and tape is moving forward for the next data. On the leading edge of the next feed hole, DATRDY1 becomes active. It strobes the data into Buffer Register and fires a one-shot to reset the DT flip-flop and causes BSY1 to go inactive. The main signal describing tape movement is DATRDY1. A True signal indicates that data track outputs are in an "on character" condition. This signal is true with the leading edge of a feed hole and remains true until the next drive signal is accepted. In the Slew Mode, DLT0 is a level. Drive signals are generated inside the Reader 50 microseconds after the leading edge of each DATRDY1 provided DLT0 stays active. If the Processor request for data is late with respect to the next character received from the Reader, OV1 becomes active, giving the Processor an indication that data has been over-written.

In the Incremental Mode, the SL flip-flop is reset. When the HSPTR Interface receives an RD instruction, it first sends out the data in the Buffer Register to the Processor through the Data Lines, then DRG0 sets the DT flip-flop and causes BSY1 to become active. SL0, ANDed with RN1 and DT1, makes DLT0 active which drives the tape to the left until the next character is encountered. On the leading edge of the feed hole, DATRDY1 becomes active and fires a one-shot to reset the DT flip-flop thus making DLT0 inactive and stopping the tape movement. The HSPTR remains in this state until the Processor requests data and DRG0 is activated. Subsequent data requests by the Processor move the tape one character at a time in the manner just described.

4.5 Write Operation

Prior to a Write Operation, a Write Command is issued by the Processor. The Processor transfers data from the Data Lines to the HSPTR/P Interface by activating the DA0 control line. DA0 is inverted in the HSPTR/P Interface and used to derive DAG0. Approximately 200 nanoseconds after DAG0 goes high, SYN1 goes high. SYN1 inverted indicates to the Processor that the HSPTR/P Interface received the information. At this time, BSY1 is inactive due to either initialization or completion of a previous Write or Read operation by the HSPTR/P Interface. DAG0 is inverted and Strobes the information into the Buffer Register. On the trailing edge of DAG0, a one shot is fired and sends the PUNCH Command to the Punch. The PUNCH Command moves tape and initiates punching at up to 75 characters/second. The PRDY1 is inactive during the advance and punch cycle which makes BSY1 active, indicating to the Processor that the Punch is not ready for another Punch Command. At the end of the Punch cycle, PRDY1 becomes active, makes BSY1 inactive, and the HSPTR/P Interface is now ready to receive another byte of data from the Processor.

5. DEVICE ADDRESS STRAPPING

The preferred address for the High Speed Paper Tape Reader Controller is X'03' and for the High Speed Paper Tape Reader/Punch Combination Controller is X'13'. The wire-wrap stakes for strapping are located on the Controller. The Schematic 02-265D08 shows the address X'13' for Reader and Punch Combination. For Reader only (X'03'), connect G to 3 (H and 3 are disconnected).

6. BI-DIRECTIONAL READ OPERATION

With minor changes, the HSPTR/P Interface can perform bi-directional Read operations. Table 2 shows the Status and Command Bytes for bi-directional read operation:

TABLE 2. STATUS AND COMMAND BYTES FOR BI-DIRECTIONAL READ OPERATION

BIT NUMBER	8	9	10	11	12	13	14	15
STATUS NUMBER	OV	0	0	NMTN	BSY	EX	0	DU
COMMAND BYTE	DISABLE	ENABLE	STOP	RUN	INCR	SLEW	REV	FWD

* DISARM = DISABLE . ENABLE

The FORWARD Read Command drives tape in the forward direction (from right to left) and the REVERSE Read Command drives tape in the reverse direction (from left to right). Note that REV and WRITE occupy the same Data Line (Bit 14) (See Table 1); thus, in bi-directional Read operation, the Write Command cannot be executed.

The following are the necessary changes for bi-directional Read operation:

1. HSPTR/P Interface

- a. Remove the diode D7. (Near IC 21, the anode is connected to Pin 4 of IC 21)
- b. Cut the wire between Pin 11 of IC 12 and the feed hole which is also connected to Pin 4 of IC 4.
- c. Ground Pin 4 of IC 4. (See Figure 3 for details.)

2. Reader Head

- a. Insert a piece of tape known to have been punched with all holes having normal registration.
- b. With power ON, the motor should be energized. Use an Allen wrench to loosen the two set screws which hold the motor to the heat sink.
- c. Rotate the motor so that the holes in the tape appear concentric with the fiberglass read heads and the light columns. (See Figure 3 for details.)

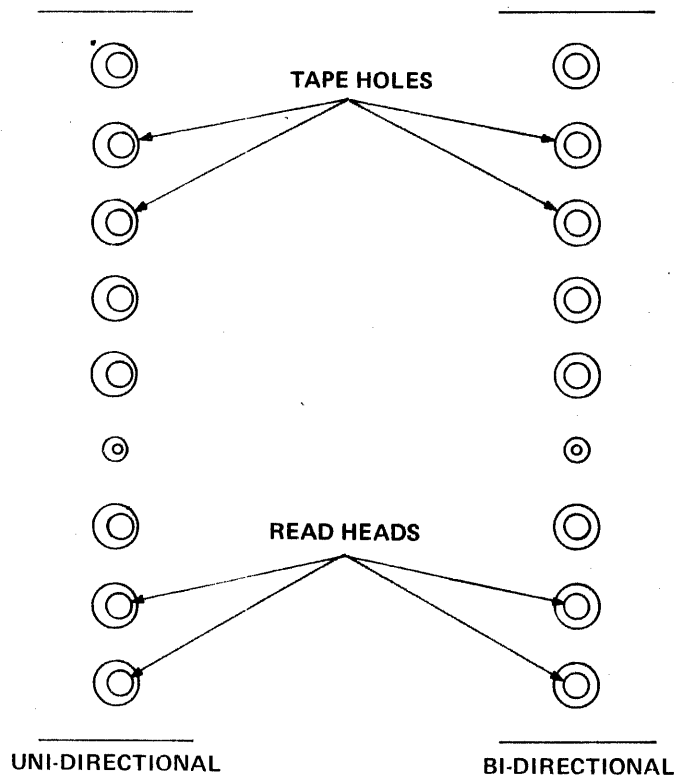
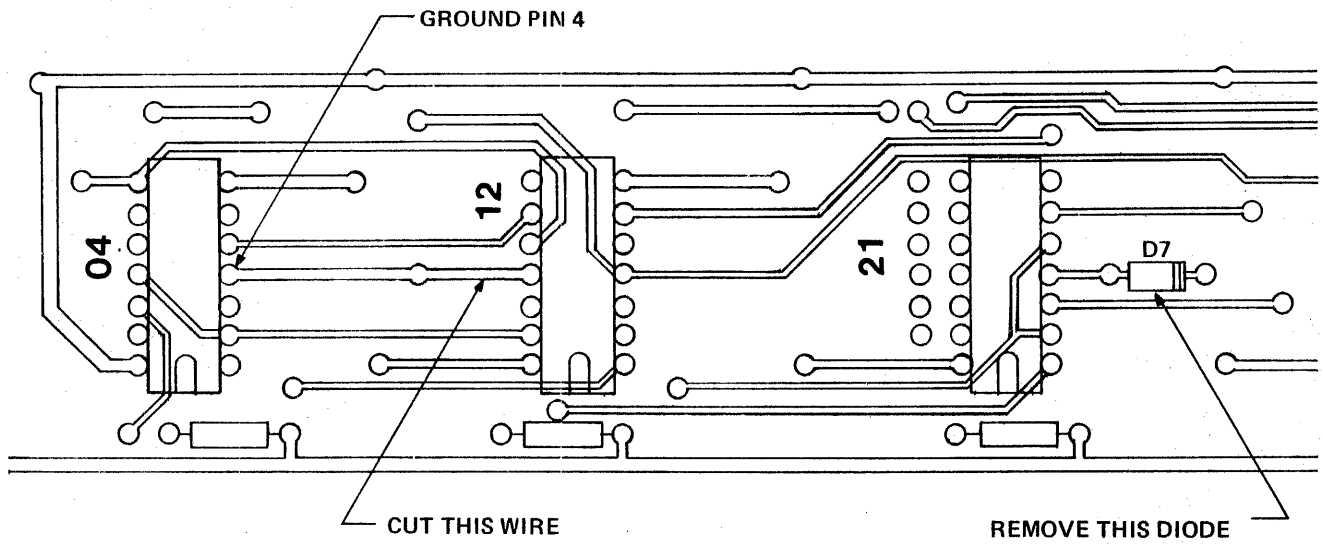


Figure 3. Modifications for Bi-Directional Read

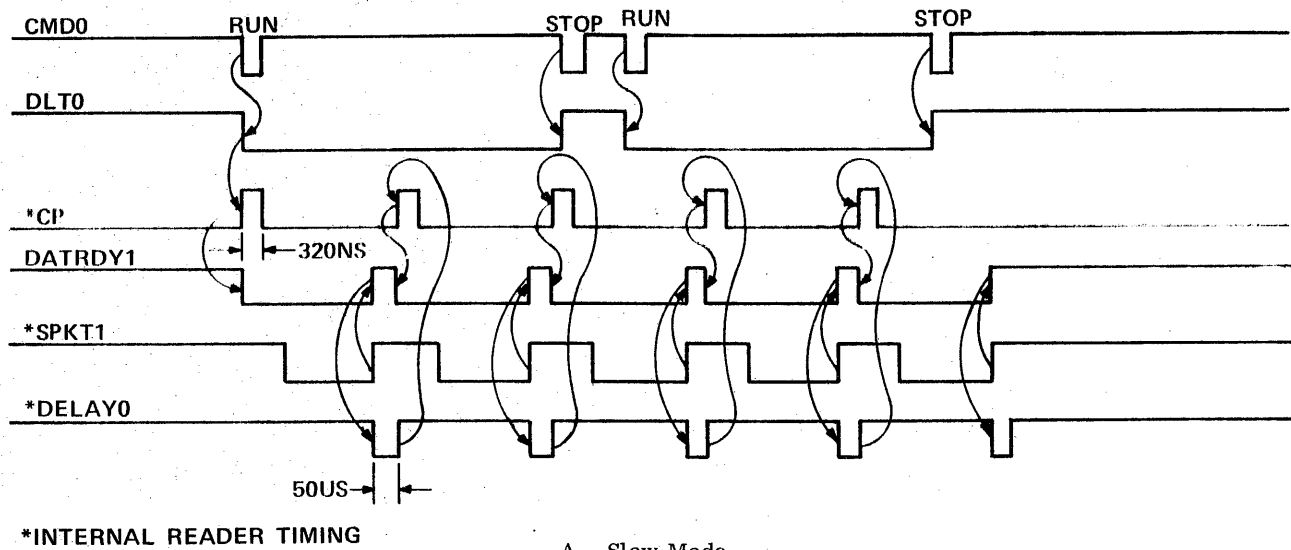
7. MAINTENANCE

The High Speed Paper Tape Reader/Punch Controller requires no periodic maintenance. The Reader and Punch requires periodic maintenance such as cleaning and lubrication. For a procedure and maintenance requirements, refer to the Vendor Technical Manuals, Publication Numbers 29-333 (Reader), and 29-334 (Combination).

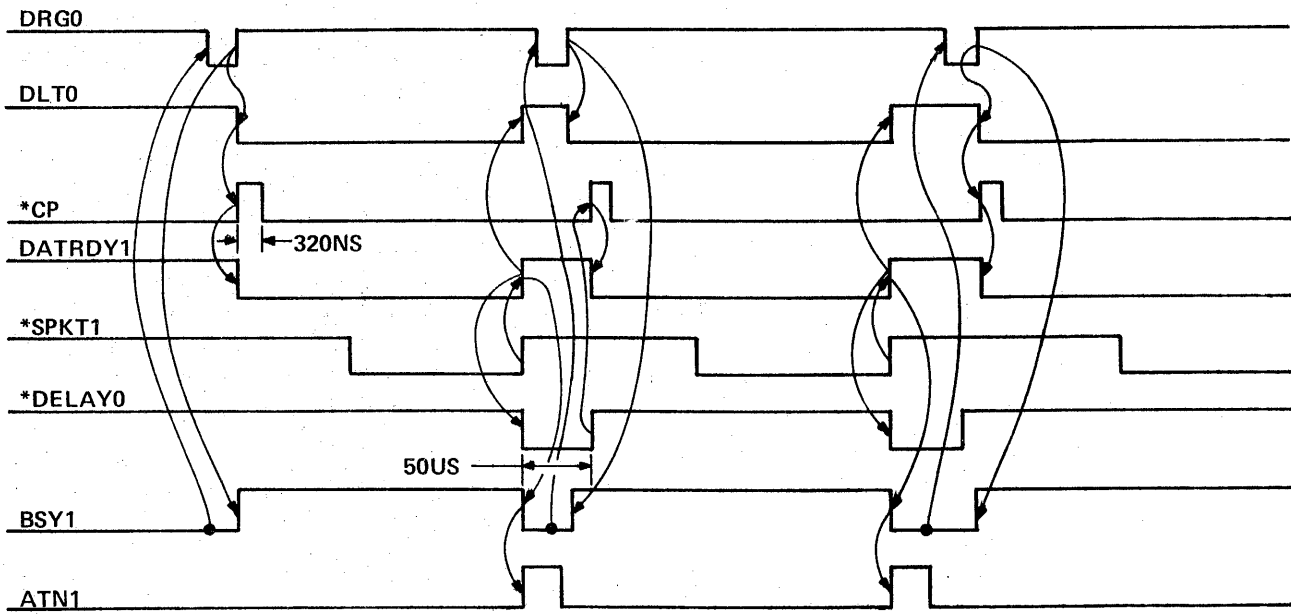
Performance tests of the system can be made on the system by using the test program 06-137. This test program will assist in troubleshooting the Controller.

8. TIMING

The timing diagrams for the Read and Write operations of the Controller are shown in Figures 4 and 5.



*INTERNAL READER TIMING A. Slew Mode



*INTERNAL READER TIMING B. Increment Mode

Figure 4. Read Mode Timing Diagram

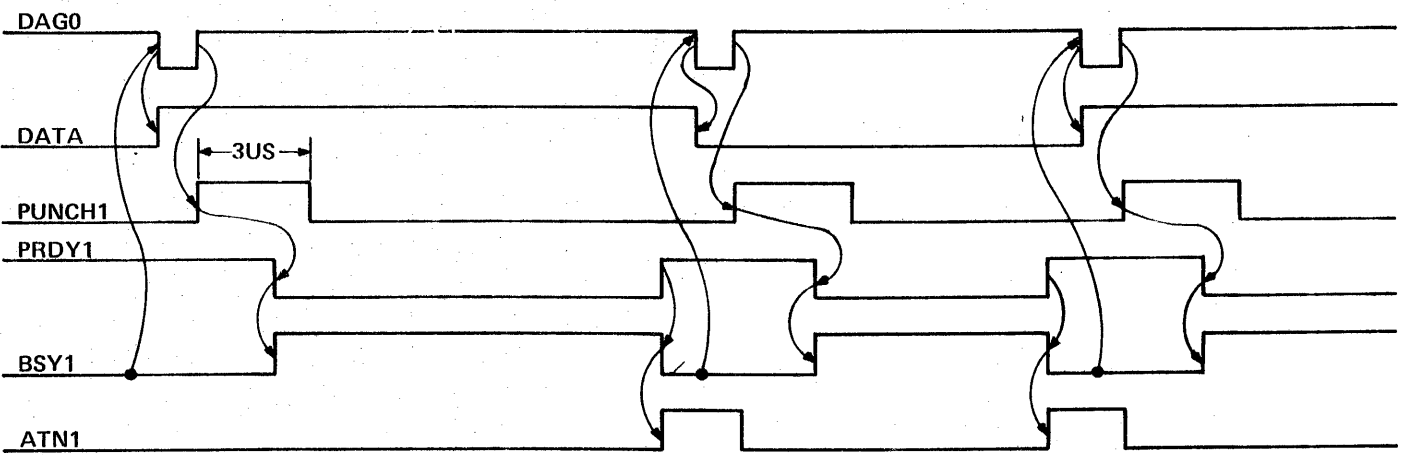


Figure 5. Write Mode Timing Diagram

9. MNEMONICS

The following list provides a brief description of each mnemonic found in the HSPTR/P Device Controller. The meaning and the 02-265D08 source of each signal are also provided.

MNEMONIC	MEANING	LOCATION
AD1	Address Flip-Flop	2G7
ADRS0	Address	2F1
ATN0	Attention	2A1
BSY1	Busy	3F9
CMD0	Command	2D1
CMDRST0	Command Reset	3N9
CMDRST0A	Command Reset	3N9
DA0	Data Available	2D1
DAG0	Gated Data Available	2D9
DATRDY1	Reader Data Ready	3A6
DATA11-DATA81	Punch Data	3G4-3G1
DAT081-DAT151	Read Data	3D4-3D1
D080-D150	Data Lines	2N1-2G1
DISARM0	Disarm	2B9
DLT0	Drive Left	3N3
DR0	Data Request	2E1
DRG0	Gated Data Request	2E9
DRT0	Drive Right	3N3
DT1	Device Transmit Flip-flop	3J5
DU1	Device Unavailable	3F7
EX1	Examine	3M6
FWD1	Forward	3M2
HW0	Halfword	2G9
NMTN1	No Motion	3M6
OV0	Overflow	3J6
PATN0	Pulsed Attention	2B9
PRDY1	Punch Ready	3A8
PSYSRDY0	Punch System Ready	3A7
PUNCH1	Punch	3D7
RACK0	Received Acknowledge	2B1
REV1	Reverse	3N2
RN1	Run Flip-Flop	3K4
RN0	Run Flip-Flop	3K4
SATN0	Set Attention	3J8
SCLR0	System Clear-Initialize	2E1
SL0	Slew Mode	3K4
SR0	Status Request	2E1
SREQ0	Selch Request	2H9
SYN0	System Sync.	2F9
SYSRDY0	Reader System Ready	3A5
TACK0	Transmit Acknowledge	2A5
TERM0	Terminate	2H9
TPHE1	Tape Handling Error	3A8
TR11-TR81	Reader Data Lines	3A1-3A4
WT1	Write Flip-Flop	3M1
XFER0	Transfer	2C1

M46-250

PAPER TAPE READER/PUNCH

PROGRAMMING SPECIFICATION

1. INTRODUCTION

This specification provides information on the operation and programming of the M46-250 combination Paper Tape Reader/Punch interface, which supports the M46-240 Paper Tape Reader or the M46-242 Paper Tape Reader/Punch. Note that with this interface, the PTR/P cannot read and punch tapes simultaneously.

Table 1 lists the general characteristics of the Reader and Punch.

TABLE 1. READER AND PUNCH CHARACTERISTICS

CHARACTERISTICS	READER	PUNCH
Type	Photo-electric	Electro-mechanical
Tape Width	Fixed width of 1 inch	Fixed width of 1 inch
Speed	Maximum of 300 characters-per-second	Maximum of 75 characters-per-second
Tape handling	Oiled or unoled paper, paper-mylar, mylar, and aluminum mylar	Same as the Reader
Stop time	Capable of stopping on a character	Punches character and stops
Read/Load Switch	Allows loading or changing of tapes	Same as the Reader
Power Switch	Applies AC power to Reader motor	Applies AC power to Punch motor

2. CONFIGURATION

The M46-242 Paper Tape Reader/Punch, and the M46-240 Paper Tape Reader only, with the M46-250 interface, require any basic new series Processor configuration. No particular Processor options are necessary. The device is normally used on the Multiplexor Bus.

3. OPERATING PROCEDURES

3.1 Punch Front Panel

The Punch front panel contains three control switches. They are:

1. Power. This rocker switch turns power on or off to the Punch. It lights in the ON position.
2. Feed. This momentary rocker switch causes the unit to feed tape through the punch mechanism. Sprocket holes are punched, but data is inhibited. Note that operation of this switch in conjunction with external input on the punch line is not allowed and can cause erratic punching.
3. Run/Load. This lever, when in the Run position, allows operation of the Punch mechanism. When in the Load position, it dis-engages the pinch roller from the capstan on the Punch mechanism.

3.2 Reader Control Switches

The reader mechanism contains three control switches. They are:

1. Power. This switch turns power on or off to the reader.
2. Run/Load. This switch, which is activated by the tape access door, allows the Reader to operate when the door is closed and inhibits Reader operation when the door is open.
3. Direction Control. This momentary rocker switch enables the user to manually back up or advance the paper tape.

4. DATA FORMAT

4.1 Reader

The High Speed Paper Tape Reader is a byte buffered device capable of reading up to eight channels on a paper tape.

4.2 Punch

The High Speed Paper Tape Punch is a byte buffered device capable of punching up to eight channels in a paper tape.

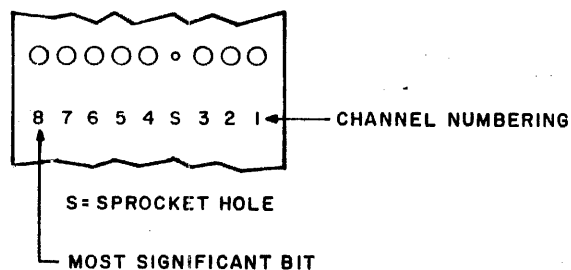


Figure 1. Channel Designations

5. PROGRAMMING INSTRUCTIONS

5.1 Status and Command Bytes

The status and command bytes for the High Speed Paper Tape Reader/Punch Interface are shown in Table 2.

6. PROGRAMMING SEQUENCES

6.1 Punch

The Interface is given an output command to place the device in the Write Mode with interrupts disarmed. A Sense Status instruction is issued followed by a test for Busy. When Busy goes low, a Write Data instruction may be given.

6.2 Read

The Interface is given an output command to place the device in the Read, Run, INCR Mode with interrupts disarmed. A Sense Status instruction is issued followed by a test for Busy. When Busy goes low, a Read Data instruction may be given.

7. INTERRUPTS

When enabled, interrupts are generated by the Interface when:

1. The Reader goes Not Busy. (A character is strobed into the Buffer Register from the HSPTR.)
2. The Punch goes Not Busy. (A character has been output to the HSPTP and the Interface is ready for more data.)
- *3. Change from Read Mode to Write Mode provided the Punch is Not Busy.
- *4. Change from Write Mode to Read Mode provided the Reader is Not Busy.
5. Device Unavailable (DU bit goes from 0 to 1).

Pending Interrupts are cleared by:

1. Initialization.
2. Disarm command.
3. Acknowledge interrupt instruction.
- *4. Changing from Read Mode to Write Mode.
- *5. Changing from Write Mode to Read Mode.

When disabled, interrupts are queued.

When disarmed, interrupts are not generated or queued.

NOTE

To maintain programming compatibility with the 02-031 High Speed Paper Tape Reader/Punch a test for Busy=0 must be performed before changing modes.

8. INITIALIZATION

Initialization occurs on power up or when the Initialize Switch on the Processor is depressed, provided the Reader power is on and the RUN/LOAD Switch is in the RUN position.

When initialized, the following occurs:

1. Interrupts of all kinds are disarmed.
 2. The NMTN and EX status bits are set.
 3. The Disarm, Stop, INCR and Read command functions are set.
 4. The BSY status bit is set or reset depending on the state of the Reader.
- * When changing from Read Mode to Write Mode, or from Write Mode to Read Mode, pending interrupts are cleared, then the Busy status of the new device is checked. If the new device is Busy, no interrupt is generated until the device goes Not Busy. If the new device is already Not Busy upon changing mode, an interrupt is generated at the time of changing mode. The programmer can ignore the last interrupt and change mode directly.

TABLE 2. HSPTR/P INTERFACE STATUS AND COMMAND

BIT NUMBER	8	9	10	11	12	13	14	15
STATUS BYTE	OV			NMTN	BSY	EX		DU
COMMAND BYTE	DISABLE	ENABLE	STOP	RUN	INCR	SLEW	WRITE	READ

DISARM = DISABLE • ENABLE

STATUS

<u>BIT</u>	<u>READER</u>	<u>PUNCH</u>
OV	<p>The Overflow bit is set when the Buffer Register is loaded from the Reader before the previous character has been transferred. This condition can only happen in the SLEW mode. It is reset by:</p> <ol style="list-style-type: none"> 1. Initialization. 2. The HSPTR/P changes from Read Mode to Write Mode. 3. The HSPTR/P changes from Write Mode to Read Mode. 4. The Reader changes from STOP to RUN. 	<p>The Overflow bit is always reset in the Write Mode.</p>
DU	<p>The Device Unavailable bit is set when the power to the Reader is off or the power is not stabilized, or the Reader lever is in the LOAD position, or if the drive signal is received and new feed hole is not sensed within 10ms. It indicates either no tape or torn tape and serves as the Out-Of-Tape signal. It is reset when the above conditions are not true.</p>	<p>The Device Unavailable bit is set when the power to the punch is off or internal voltages have not stabilized, or RUN-LOAD Switch is in LOAD or the chad box is full. It is reset when the above conditions are not true.</p> <p>Note that CHAD ERROR is reset by depressing the PERF STATUS Switch.</p>
NMTN	<p>The No Motion Bit is set when the Reader has issued a Stop Command and the tape has been stopped on the character. It is reset when tape starts moving.</p>	<p>The No Motion bit is always reset in the Write Mode.</p>
BSY	<p>The Busy bit is set when the Buffer Register is empty, waiting for an output from the Reader or the Reader is in Load Condition or the Reader power is not stabilized. It is reset when the above conditions are not true.</p>	<p>The Busy bit is set when the tape is advancing and in the Punch cycle. It is reset when the Punch is ready to accept a punch command.</p>
EX	<p>The Examine bit is set whenever OV=1 or NMTN=1. It is reset when they are both reset.</p>	<p>The Examine bit is always reset in the Write Mode.</p>

COMMANDS

<u>BIT</u>	<u>READER</u>	<u>PUNCH</u>
DISABLE	This command inhibits interrupts from the Device Controller from interrupting the Processor. Interrupts are queued.	Same as Reader.
ENABLE	This command permits interrupts from the Device Controller to interrupt the Processor.	Same as Reader.
DISARM	This command prevents the device from interrupting or queuing the interrupts.	Same as Reader.
STOP	This command bit halts the motion of the tape. The next character to be read is positioned over the sense light when the tape stops.	Not used.
RUN	This command leaves the controller in the Run Mode, and if in the Slew Mode, starts the tape moving.	Not used.
INCR	In this mode of operation, the tape is advanced one character when the controller is in the Run Mode and a Read Data instruction is executed. The tape stops after encountering the next character. The tape remains stopped until a Read Data Instruction, which starts the tape moving again.	Not used.
SLEW	In this mode of operation, the tape is advanced continuously until stopped.	Not used.
WRITE		Designates the High Speed Paper Tape Punch.
READ	Designates the High Speed Paper Tape Reader.	

INSTRUCTIONS

Output command (OC or OCR) - This instruction is used to send a Command Byte to the reader/punch from the Processor.

Sense Status (SS or SSR) - This instruction enables the Status Byte of the Interface to be examined.

Write Data (WD or WDR) - This instruction is used to output a data byte to the punch.

Read Data (RD or RDR) - This instruction is used to input a data byte from the Reader when in the Read mode.

Acknowledge Interrupt (AI or AIR) - This instruction enables the user to examine the Device Address and Status Byte when the Interface generates an interrupt.

Read Block (RB or RBR) and Write Block (WB or WBR) instructions can be used with the reader/punch. Halfword I/O instructions (RII, RIIR, WII, WHIR) are not used with the Reader/Punch.

9. DEVICE NUMBER

The High Speed Paper Tape Reader/Punch, using Device Controller 35-439, is normally assigned address X'03' if using a Reader only. If using both a Reader and a Punch, address X'13' is normally assigned. These device numbers are easily changed by a minor modification to the Device Controller. Refer to the HSPTR/P Interface Instruction Manual, Publication Number 29-290, for details.

10. SAMPLE PROGRAMS

Appendix 1 is a sample program for Models 4, 5, 70, and 80 using the High Speed Paper Tape Reader in the Incremental Mode, using a programmed status loop.

Appendix 2 is a sample program for Models 4, 5, 70 and 80 using the High Speed Paper Tape Reader in the Slew Mode using interrupt control.

Appendix 3 is a sample program for Models 4, 5, 70 and 80 using the High Speed Paper Tape Punch, using a programmed status loop.

Appendix 4 is a sample program for Models 4, 5, 70 and 80 using the High Speed Paper Tape Reader/Punch, using a programmed status loop.

Appendix 5 is a sample program for Models 4, 5, 70 and 80 using the High Speed Paper Tape Reader/Punch under interrupt control.

APPENDIX 1
 SAMPLE PROGRAM
 READER-INCREMENTAL MODE

```

*
* SAMPLE PROGRAM FOR HSPTR (INCREMENTAL MODE)
* USING STATUS LOOPS
*
INPUT      LHI          DEV, 3          SELECT DEVICE NUMBER
           OC           DEV, READ       ISSUE OUTPUT COMMAND
SENSE      SSR          DEV, STATUS     GET STATUS OF READER
           BTC          5, TROUBLE     DU OR EX=1; ERROR
           BTC          8, SENSE       BSY=1; WAIT
           RDR          DEV, TEMP      READ ONE CHAR. FROM TAPE
           B            PROCES        PROCESS THIS CHARACTER
*
TROUBLE    LPSW        STOP            TROUBLE CORRECTED; RETURN
STOP       DC          X'8000', A(INPUT) TO INPUT ROUTINE
*
DEV        EQU         1              DEVICE NUMBER 03
STATUS     EQU         2              HOLDS STATUS BITS
TEMP       EQU         3              TEMPORARY STORAGE
*
READ       DC          X'D9D9'        OUTPUT COMMAND IS X'D9'
*
PROCES     EQU         *
           END

```


APPENDIX 2
SAMPLE PROGRAM
READER-SLEW MODE-INTERRUPT CONTROL

```

*
* SAMPLE PROGRAM FOR HSPTR (SLEW MODE) USING INTERRUPT CONTROL
* READ TAPE UNTIL X'FF' CHARACTER IS ENCOUNTERED OR BUFFER IS FULL
*
INPUT      LHI      DEV, 3      SELECT DEVICE NUMBER
           OC      DEV, DISARM  ISSUE OUTPUT COMMAND
           LHI      CHECK, X'4000' SET NEW PSW
           STH      CHECK, X'44'
           LHI      CHECK, INT    SET EXT INT ADRS
           STH      CHECK, X'46'
           XHR      INDEX, INDEX  ZERO INDEX REG
           LHI      5, 1          SET INCREMENT VALUE
           LHI      6, 4096       SET BXLE LIMIT
           LPSW     ENABLE        ENABLE EXT INTS
ENABLE     DC      X'4000', ENABLE+4
           OC      DEV, READ      ISSUE OUTPUT COMMAND
TROUBLE    LPSW     WAIT          TROUBLE THEN WAIT
WAIT       DC      X'C000', INPUT
INT        AIR      ADR, STATUS   ACKNOWLEDGE INT
           BTC      1, TROUBLE   DU=1 WAIT
           CLHR     ADR, DEV      DID READER INT
           BNE      TROUBLE      NO, WAIT
           RDR      DEV, CHECK    READ CHAR. FROM TAPE
           CLHI     CHECK, X'FF'  IS IT DELIMITING CHAR.
           BE       STOP          YES, STOP TAPE MOTION
           STH      CHECK, BUFFER(INDEX) STORE CHAR. IN BUFFER
           BXLE     INDEX, TROBLE  WAIT FOR INT
STOP       OC      DEV, DONE      OUTPUT COMMAND X'E0'
           LPSW     HALT
HALT       DC      X'8000', INPUT  HALT
DEV        EQU     1              DEVICE NUMBER 03
STATUS     EQU     2              HOLDS STATUS BITS
CHECK      EQU     3              REG USED TO CHECK FOR DELI
INDEX      EQU     4              INDEX VALUE
ADR        EQU     7              HOLDS INT DEV ADRS
DISARM     DC      X'C2C2'        OUTPUT COMMAND DISARM-WRITE
READ       DC      X'5555'        OUTPUT COMMAND ENABLE-RUN, READ
DONE       DC      X'E0E0'        OUTPUT COMMAND DISARM-STOP
BUFFER     DS      4096           BUFFER SIZE
           END

```


APPENDIX 3
SAMPLE PROGRAM
PUNCH

```

*
* SAMPLE PROGRAM FOR THE HIGH SPEED PAPER TAPE PUNCH USING STATUS LOOPS
*
START      LHI      DEV,X'13'      SET DEVICE NUMBER
           LHI      3,1      SET LOW LIMIT AND
           LHI      4,4096    HIGH LIMITS OF THE
OUTPUT     XHR      COUNT,COUNT  BUFFER AREA
           OC       DEV,WRITE    WRITE MODE
SENSE      SSR      DEV,STATUS    CHECK STATUS
           BTC      1,TROUBLE    DU=1; STOP
           BTC      8,SENSE      BUSY=1 WAIT
           WD       DEV,BUFFER,(COUNT) OUTPUT CHARACTER
           BXLE     COUNT,SENSE   DO UNTIL DONE
TROUBLE    LPSW     STOP          TROUBLE CORRECTED; RETURN
STOP      DC       X'8000',A(START) TO OUTPUT ROUTINE
BUFFER    DS       4096
*
DEV       EQU      0      DEV. NUM. X'13'
STATUS    EQU      1      HOLDS STATUS OF THE PUNCH
COUNT    EQU      2      HOLDS LOW LIMIT OF BUFFER
RETURN    EQU      5      RETURN TO MAIN PROC.
WRITE     DC       X'C2C2' OUTPUT COM. X'C2'
           END

```


APPENDIX 4
 SAMPLE PROGRAM
 READER/PUNCH COMBINATION

```

*
* SAMPLE PROGRAM USING THE HSPTR/HSPTP IN MODE SWITCHING
* USING STATUS LOOPS
START      LHI      DEVICE, X'13'      SET DEVICE NUMBER
           LHI      3, 100      SET HIGH LIMIT AND
           LHI      2, 1        LOW LIMITS OF THE
INPUT      XHR      1, 1        BUFFER AREA
           OC       DEVICE, READ  READ MODE
INPI       SSR      DEVICE      STATUS
           BTC      1, TROBLE    DU=1 STOP
           BTC      8, INPI      BUSY=1 WAIT
           RD       DEVICE, BUFFER(1) INPUT CHAR.
           BXLE     1, INPI

*
*
OUTPUT     XHR      1, 1        CLEAR LOW LIMITS
           OC       DEVICE, WRITE  WRITE MODE
OUTI       SSR      DEVICE, STATUS
           BTC      1, TROBLE    DU=1 STOP
           BTC      8, OUTI      BUSY=1 WAIT
           WD       DEVICE, BUFFER(1) OUTPUT CHAR.
           BXLE     1, OUTI
           B        INPUT
TROUBLE    LPSW     STOP        TROUBLE CORRECTED; RETURN
STOP       DC       X'8000', A(START) TO INPUT ROUTINE
READ      DC       X'D9D9'
WRITE     DC       X'C2C2'
DEVICE    EQU      4
STATUS    EQU      5
BUFFER    DS       100
END

```


APPENDIX 5
 SAMPLE PROGRAM
 READER/PUNCH COMBINATION

```

*
* SAMPLE PROGRAM USING THE HSPTR/HSPTP UNDER INTERRUPT CONTROL
*
START      LHI      DEVICE, X'13'      SET DEVICE NUMBER
           OC      DEVICE, DISARM      DISARM DEVICE
           LHI      1, X'4000'      SET NEW PSW
           STH      1, X'44'
           LPSW     ENABLE           ENABLE EXT, INT
ENABLE     DC      X'4000', BEGIN    AT PROCESSOR
*
*
RDINT      AIR      5, 6             ACK INT
           BTC      1, WAIT          DU=1 WAIT
           CLH      5, DEVICE        DID READER INT
           BNE      WAIT            NO WAIT
           RD      DEVICE, BUFFER(1) INPUT CHAR.
           BXLE     1, WAIT
           LHI      1, WRTINT        SET EXT INT
           STH      1, X'46'        ADDRESS
           LHI      3, 100          SET HIGH LIMIT
           LHI      2, 1            AND LOW LIMIT
           XHR      1, 1            OF BUFFER AREA
           OC      DEVICE, WRITE    WRITE MODE
*
*
WRINT      B        WAIT
           AIR      5, 6             ACK INT
           BTC      1, WAIT          DU=1 WAIT
           CLH      5, DEVICE        DID PUNCH INT
           BNE      WAIT            NO WAIT
           WD      DEVICE, BUFFER(1) OUTPUT CHAR.
           BXLE     1, WAIT
BEGIN     LHI      1, RDINT          SET EXT INT
           STH      1, X'46'        ADDRESS
           LHI      3, 100          SET HIGH LIMIT
           LHI      2, 1            AND LOW LIMIT
           XHR      1, 1            OF BUFFER AREA
           OC      DEVICE, READ     READ MODE
*
*
WAIT      LPSW     WAIT+4
           DC      X'C000', START
*
*
READ      DC      X'5959'
WRITE     DC      X'4242'
DISARM    DC      X'C2C2'
DEVICE    EQU     4
BUFFER    DS     100
END

```


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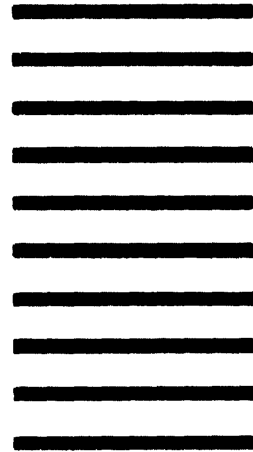
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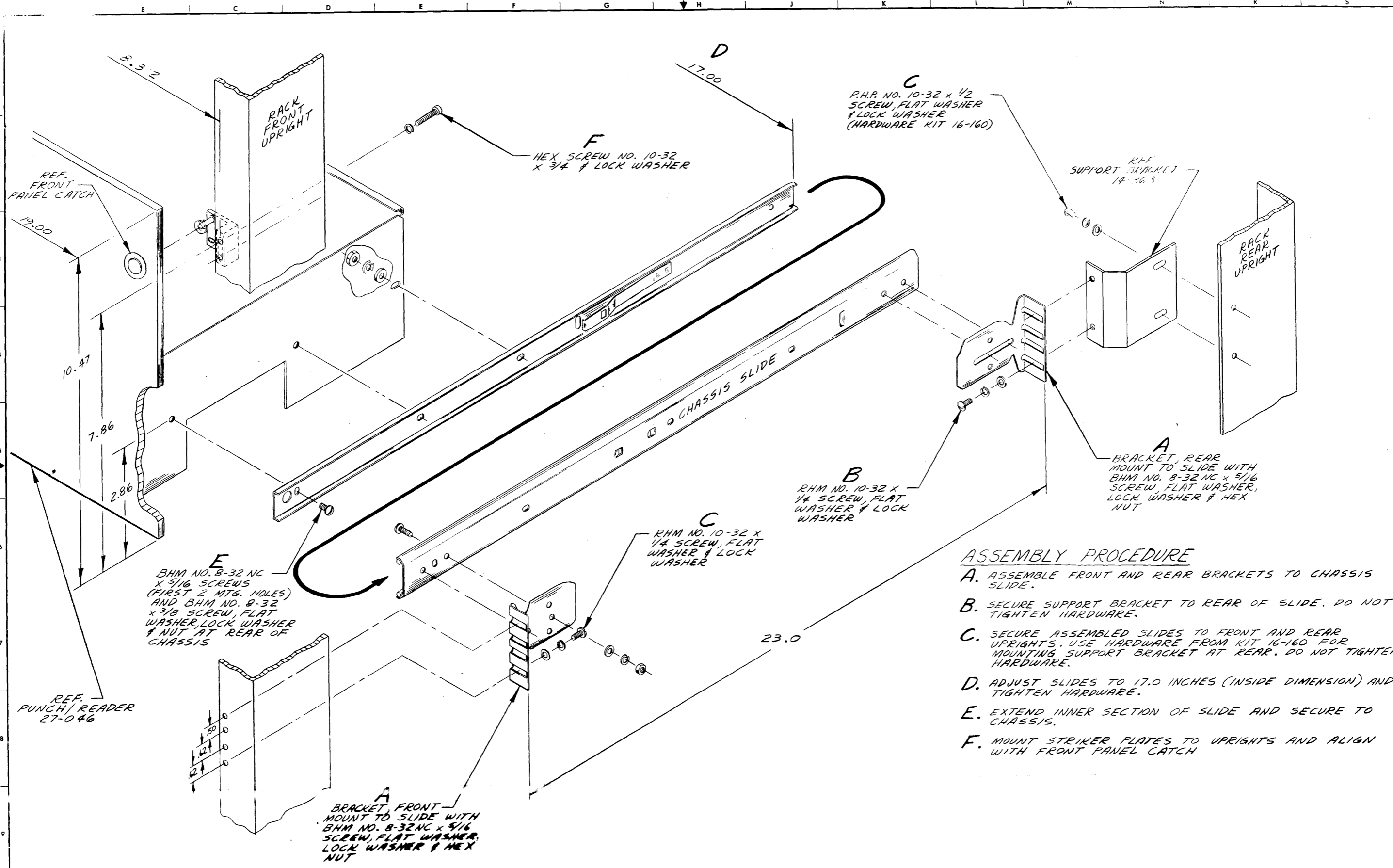


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STAPLE



ASSEMBLY PROCEDURE

- A. ASSEMBLE FRONT AND REAR BRACKETS TO CHASSIS SLIDE.
- B. SECURE SUPPORT BRACKET TO REAR OF SLIDE. DO NOT TIGHTEN HARDWARE.
- C. SECURE ASSEMBLED SLIDES TO FRONT AND REAR UPRIGHTS. USE HARDWARE FROM KIT 16-160 FOR MOUNTING SUPPORT BRACKET AT REAR. DO NOT TIGHTEN HARDWARE.
- D. ADJUST SLIDES TO 17.0 INCHES (INSIDE DIMENSION) AND TIGHTEN HARDWARE.
- E. EXTEND INNER SECTION OF SLIDE AND SECURE TO CHASSIS.
- F. MOUNT STRIKER PLATES TO UPRIGHTS AND ALIGN WITH FRONT PANEL CATCH

NOTES
 1. UNLESS OTHERWISE SPECIFIED MOUNTING HARDWARE IS SUPPLIED WITH P/R UNIT.

2. ASSEMBLY PROCEDURE IS FOR MOUNTING UNIT IN INTERDATA STANDARD RACK.

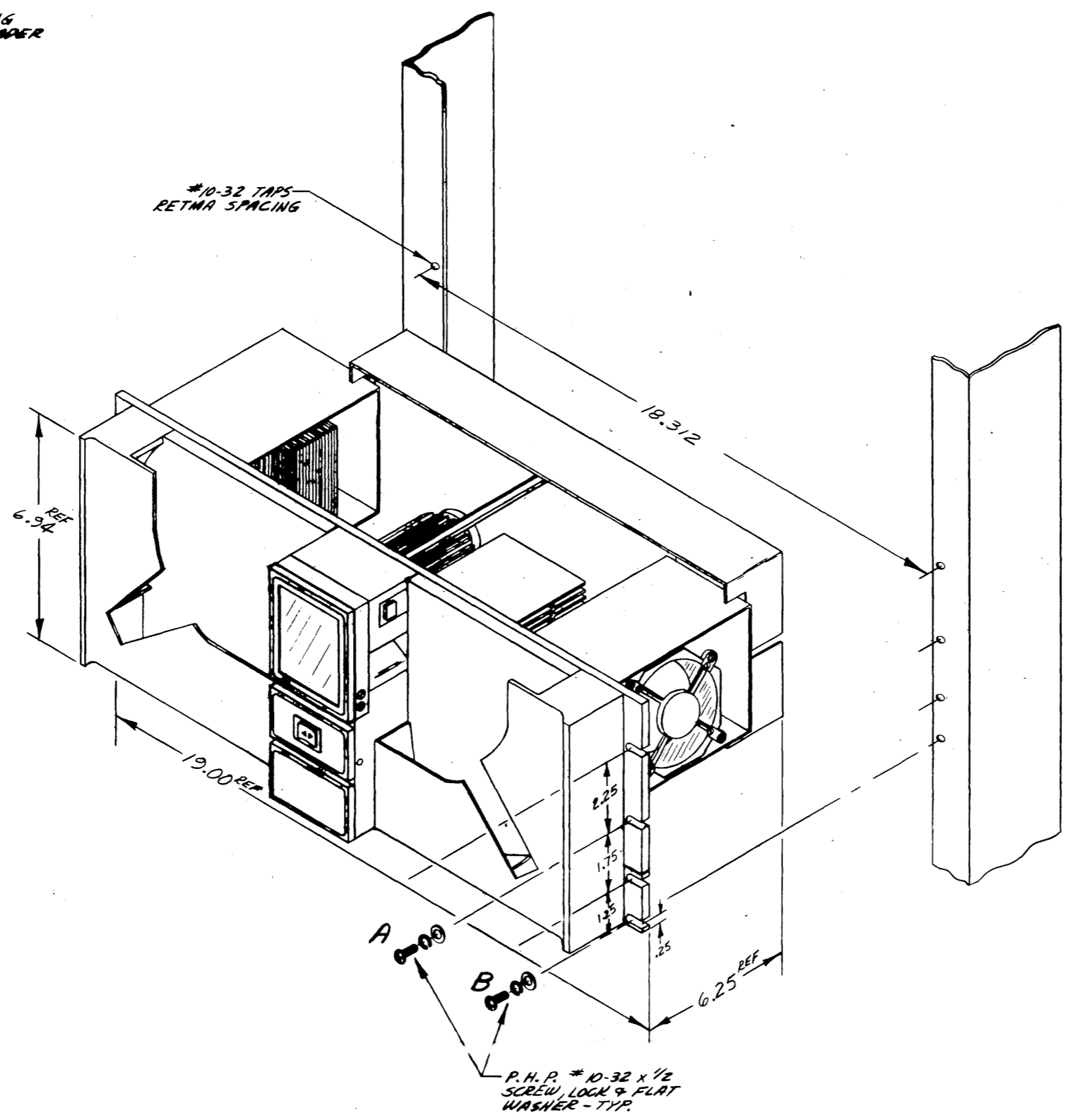
NAME	TITLE	DATE	TITLE INFORMATION
D. BARBER	DRAFT	3-15-73	PUNCH/READER RACK INSTALLATION
H. MATTHEW	CHK	3-15-73	
J. WELLS	ENGR	4-18-73	
	TASK NO.	03017	
	SHEET OF	1-1	



ASSEMBLY PROCEDURE

NOTE: ALL MOUNTING HARDWARE IS PART OF HARDWARE KIT 16-160

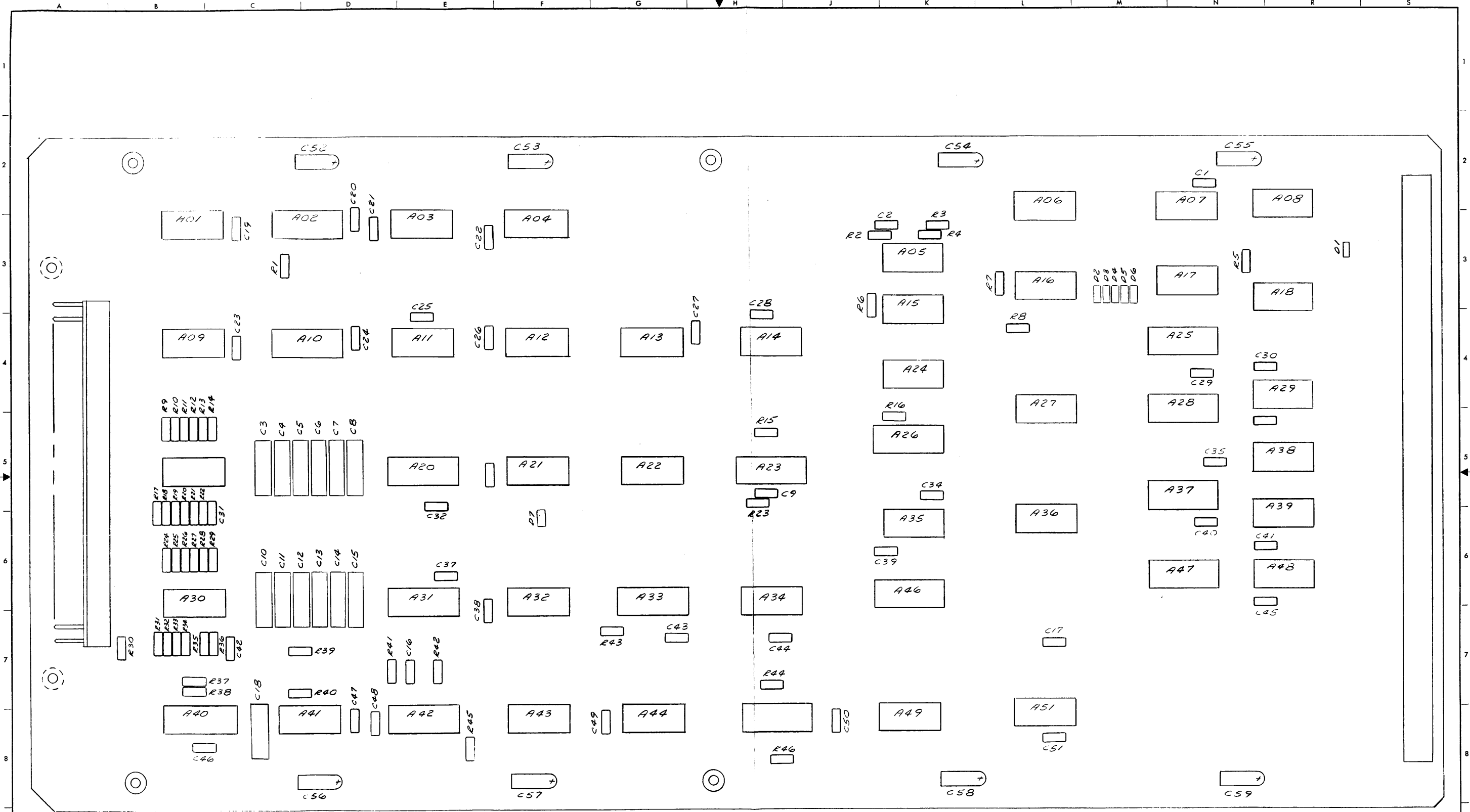
- A. SECURE READER TO RACK WITH #10 HARDWARE.
- B. SECURE FANFOLD BIN MOUNTING FLANGE DIRECTLY BELOW READER PANEL WITH #10 HARDWARE.



NOTES

NAME	TITLE	DATE	TITLE INFORMATION
D. BARKER	DRAFT	3-12-73	READER
H. MATTER	CHK	3-12-73	RACK INSTALLATION
G. WELLY	ENGR	4-18-73	
	DIR ENG		TASK NO. 03017
			DRG NO. 02-298
			DIZ
			SHEET OF 1-1



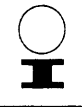


COMPONENT	REFERENCE DESIGNATION
IC	A01 THRU A49, A51
RESISTOR	R1 THRU R46
CAPACITOR	C1 THRU C59

BRUNING 44-231 16042

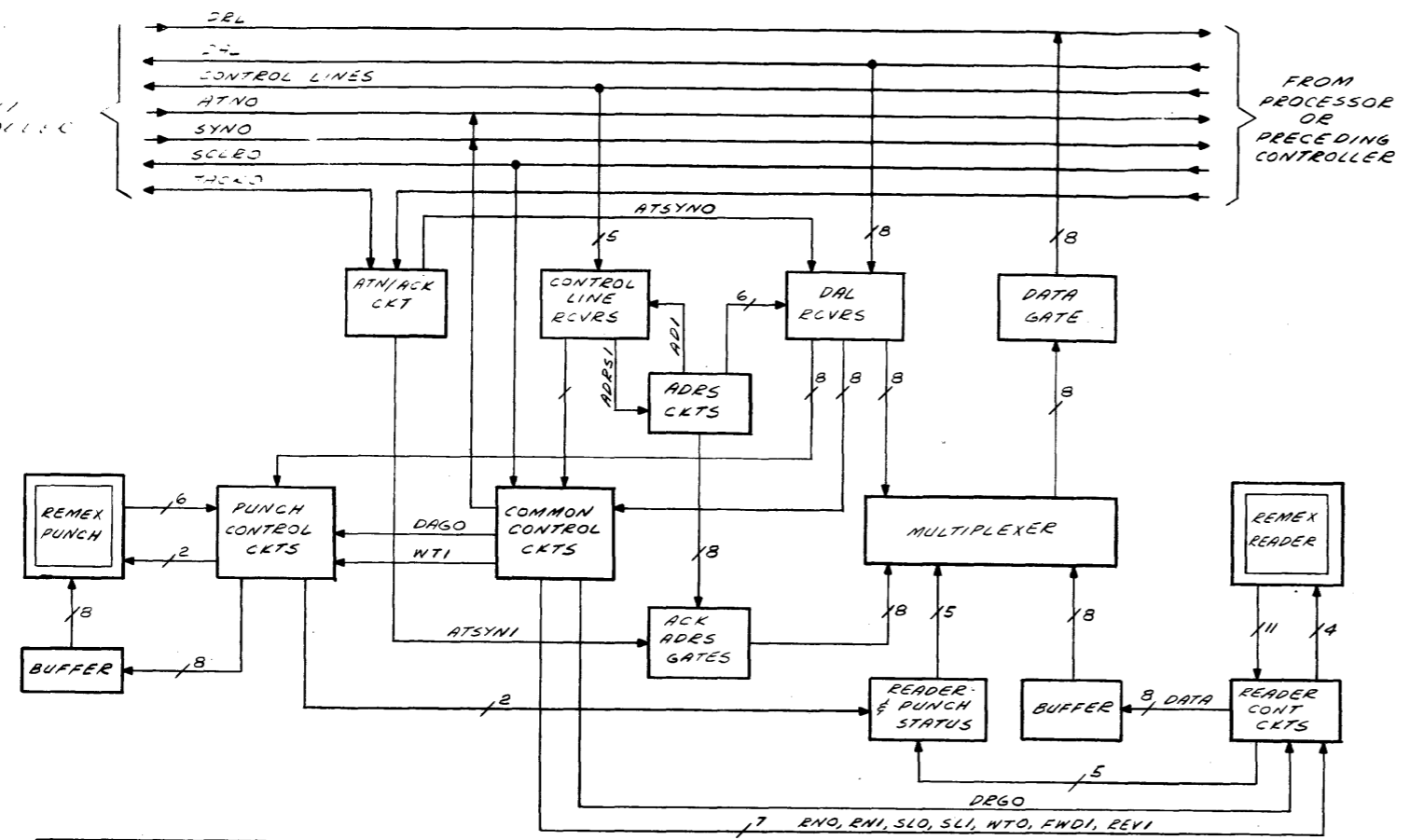
NOTES

NAME	TITLE	DATE	TITLE
D. B. McWILLIAMS	DRAFT	11/17/72	COMP. LOCATOR
	CHK		PAPER TAPE READER
	ENGR		PUNCH INTERFACE
DIR ENG		REV 01017	SHEET OF 4-4
		NO 02-265 U08	



TO NEXT CONTROLLER

FROM PROCESSOR OR PRECEDING CONTROLLER



TERM NO	ROW 1	ROW 2
41	GND	GND
40	PS	GND
39		
38		
37		
36		
35		
34		
33		
32		
31		
30		
29		
28		
27		
26	SCLRO	HWO
25	PATNO	SEBQO
24	XFEPO	TERMO
23	SYNO	ATNO
22	PACKO	TACKO
21	CLOTO	DRO
20	DRO	CMDO
19	SEPO	ADRSO
18	D140	D150
17	D120	D130
16	D100	D110
15	DOBO	DO90
14		
13		
12		
11		
10		
09		
08		
07		
06		
05		
04		
03		
02		
01	PS	GND
00	GND	GND

CONN A
35-439

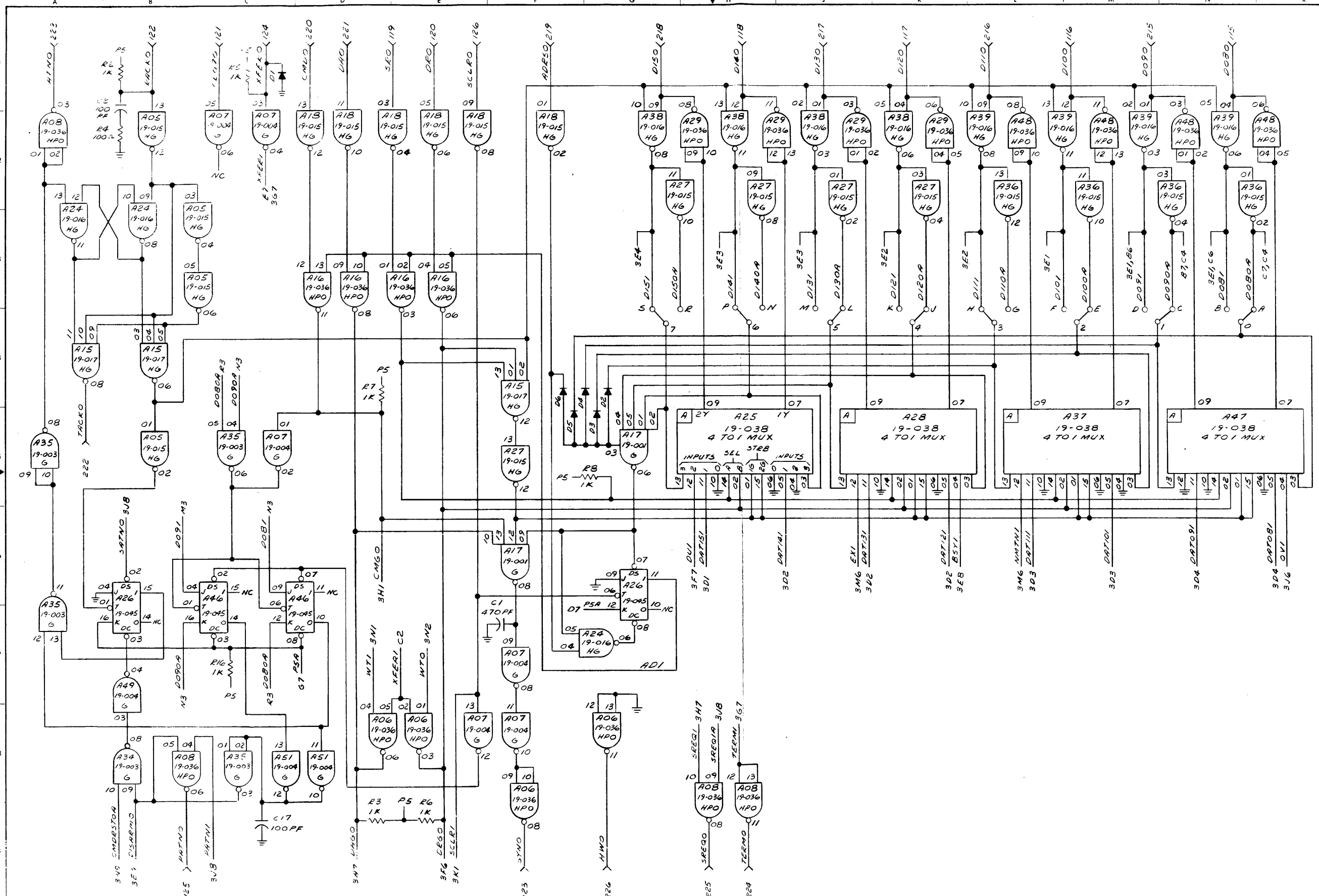
CONN A	TERMINAL	FUNCTION	TERMINAL	FUNCTION
100	PUNCH1	P (PUNCH INPUT)	J1-11	
200				
101	DATA11	P (DATA 1 INPUT)	J1-1	
201				
102	DATA21	P (DATA 2 INPUT)	J1-2	
202				
103	DATA31	P (DATA 3 INPUT)	J1-3	
203				
104	DATA41	P (DATA 4 INPUT)	J1-4	
204				
105	DATA51	P (DATA 5 INPUT)	J1-5	
205				
106	DATA61	P (DATA 6 INPUT)	J1-6	
206				
107	DATA71	P (DATA 7 INPUT)	J1-7	
207				
108	DATA81	P (DATA 8 INPUT)	J1-8	
208				
120	PROY1	P	J1-12	
220				
124	SIGNAL GND		J1-25	
117	TPHE1	(TAPE HAND. ERR. IN. INPUT)	J1-20	
122	TPLOW1	(TAPE LOW OUTPUT)	J1-21	
123	DIRECTION	(DIRECTION INPUT)	J1-10	
221	PSYRDY0	(SYSTEM READY OUTPUT)	J1-13	
224	CHASSIS GND		J1-16,17	
109	TE11	P (DATA 1 OUTPUT)	J2-1	
209				
110	TE21	P (DATA 2 OUTPUT)	J2-2	
210				
111	TE31	P (DATA 3 OUTPUT)	J2-3	
211				
112	TE41	P (DATA 4 OUTPUT)	J2-4	
212				
113	TE51	P (DATA 5 OUTPUT)	J2-5	
213				
114	TE61	P (DATA 6 OUTPUT)	J2-6	
214				
115	TE71	P (DATA 7 OUTPUT)	J2-7	
215				
116	TE81	P (DATA 8 OUTPUT)	J2-8	
216				
119	DATRDY1	P (DATA READY OUTPUT)	J2-9	
219				
118	DLTO	P (DRIVE LEFT INPUT)	J2-17	
218	GND	(SIGNAL GND)	J2-11,12,13	
121	SYSRDY0	(SYSTEM RDY OUTPUT)	J2-14	
222	MODE SELECT		J2-10	
217	DRTO	(DRIVE RIGHT INPUT)	J2-16	
223	EXTINBO	(EXT INHIBIT INPUT)	J2-15	

CABLE 17-220

BRUNING 44-231 16042

NOTES

NAME J. MATTER	TITLE MULTIPLIER	DATE 28 NOV 72	TITLE FUNCT. SCHEMATIC PAPER TAPE READER/PUNCH INTERFACE
CHK ENGR	CHK DIR ENG	2-2-73	03017
		02-265	DOB
			SHEET OF 1-4



1. START ADDRESS IS HS 511 IN 10K
 KEYS & PUNCH COMBINATIONS
 2. START ADDRESS IS 6 TO 31 10K
 KEYS ONLY.

H. MATTEL

FUNCT. SCHEMATIC
 30 BIT PAPER TAPE READER-
 PUNCH INTERFACE

03017
 06-665 002 2 4

