

**M46-102
CRT
(EDITING)
INSTRUCTION MANUAL**

CONSISTS OF:

Installation Specification
Programming Specification
Schematic

02-312A20
02-312A22
02-312B08



INTERDATA®

2 Crescent Place, Oceanport, New Jersey 07757

M46-102 CRT (EDITING) INSTALLATION SPECIFICATION

1. GENERAL

The editing CRT has two Marketing Numbers; M46-102 for the 115/V60Hz version and M46-103 for 240/50Hz. The conversion from 115/60 to 240/50 is implemented with switch options in the CRT. Each product consists of a desktop CRT with keyboard. No other hardware is included. The cables and interfaces which are required may be purchased separately. Table 1 relates Marketing and Hardware Numbers. The interconnections are shown in Figures 1 and 2.

TABLE 1. CRT MARKETING/HARDWARE NUMBERS

MARKETING NUMBER	HARDWARE NUMBER	DESCRIPTION
M46-102	27-054F00	CRT-Editing, 115V, 60 Hz
M46-103	27-054F01	CRT-Editing, 240V, 50 Hz
M46-106	17-272	CABLE, CRT-PASLA, 25 Ft.
M46-105	17-274	CABLE, CRT-MODEM, 50 Ft.
M46-102	02-279	PASLA 7" INF, RS-232
	29-325	CRT Vendor Manual

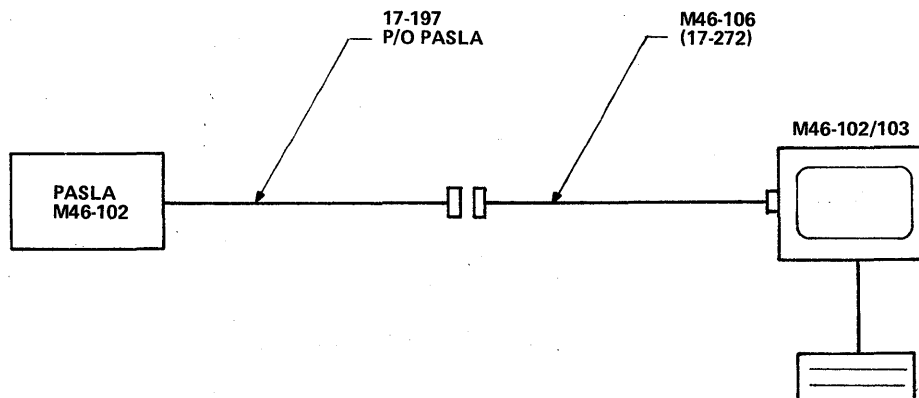


Figure 1. PASLA-CRT (Local) Connection

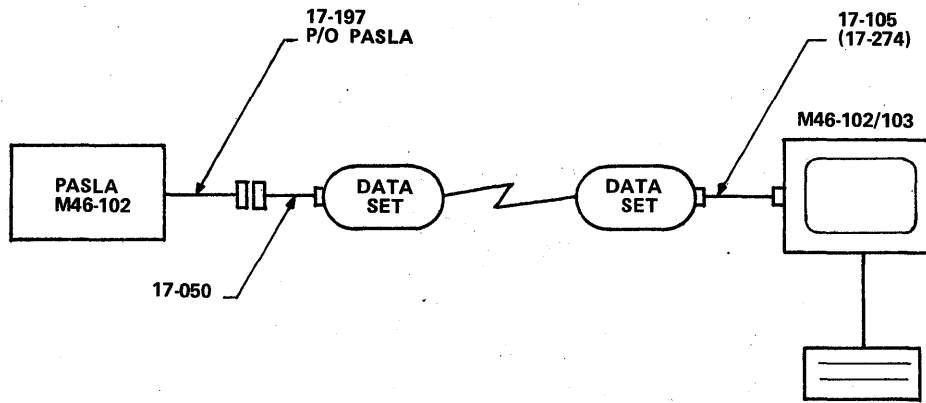


Figure 2. PASLA-CRT Remote Connection

2. INSTALLATION

The CRT Terminal has been carefully packed to insure its arrival in operating condition; however, use the following procedures to establish the mechanical integrity of the unit and prepare it for operation.

2.1 Unpacking

Inspect the shipping carton for external damage. As the equipment is unpacked, check for signs of damage or missing parts.

2.2 Equipment Placement

The CRT Terminals are self-contained and include an attractive enclosure and non-scuffing rubber feet for protection of desk and table tops. Connectors are provided for power (2-wire plus ground), detachable keyboard, video output for remote TV monitor, and communication line (modem or direct connection to Processor). Clearance is required for convection cooling of the electronics.

2.3 Options (Refer to Figures 3 through 7)

Optional features are normally enabled at the factory. If the features are specified at time of order, they are pre-set at the factory. If, however, the CRT is not purchased with an interface or if the customer does not specify options, it is necessary to inspect the PC boards in the CRT and adjust the option switches for the individual requirement. In order to do this, proceed as follows:

1. Release the three $\frac{1}{4}$ turn fasteners on the back panel and remove the back cover. Pull back the two slide latches (at the bottom rear corners), and push forward and upward (enclosures rotated from the bottom front).
2. Remove the following PC Boards.

	LOCATION
Timing Generator	1
Line Memory and Character Generator	2
Control	4
Serial I/O	6
Serial I/O	8

3. Refer to Figures 4 through 7 and implement the required options. The normal options are:

LINE MEMORY AND CHARACTER GENERATOR LOCATION 2

- | | |
|---------------------------|----------------|
| 1. Character Color | White on Black |
| 2. Carriage Return Symbol | Not Displayed |
| 3. Cursor Symbol | Not Displayed |

CONTROL - LOCATION 4

- | | |
|-------------------|-----|
| 1. Auto Line Feed | No |
| 2. Roll Up | Yes |

SERIAL I/O - LOCATION 6

- | | |
|-------------------|------------------|
| 1. Parity | Even Transmitted |
| 2. Number of Bits | 10 |
| 3. Bell | EOL Bell Enabled |
| 4. Transmit Code | X'6A' |

SERIAL I/O - LOCATION 8

- | | |
|--------------------|--|
| 1. Baud Rate | 9600 For Local CRT
300 For Remote CRT |
| 2. Parity | None |
| 3. Receive Inhibit | No |
| 4. Clock | Normal |
| 5. Duplex | Full |

4. Place the Timing Generator PC component side up, card edge connector to the right. The two position switch in the lower left corner should be oriented ⊖ for 60 Hz and ⊕ for 50 Hz.
5. Replace all PC boards.
6. Verify that the AC Select switch located at the rear of this CRT (See Figure 3) is in the proper position to select 115/240 VAC for the low voltage power supply and CRT high voltage power supply. DOWN is for 115 VAC and UP is for 240 VAC.
7. Install all PC boards and the rear cover.

3. APPLYING POWER

Before connecting power to the Terminal:

1. Turn the POWER switch on the back panel to OFF.
2. Plug the keyboard cable into KB-J3 on the back panel. Insure that the slide locks on the connector are securely fastened.
3. Attach the appropriate interface cable to J1 and fasten securely with the two 4-40 screws.
4. Attach the power cord to the POWER CONNECTOR on the back panel and to a standard 115 VAC, 60 Hz, 3 wire grounded outlet (or to 240 VAC if so ordered).

WARNING

USE A 3 PRONG ADAPTER WITH A SAFETY GROUND PROPERLY CONNECTED. NEVER CUT THE SAFETY GROUND PIN ON THE POWER CORD FOR USE WITH A 2-HOLE SOCKET AS SUCH ACTION PRESENTS A SHOCK HAZARD.

5. Turn the POWER switch ON. When the power is applied to the unit, the POWER switch is illuminated. If the switch fails to light, check the 2 amp fuse on the back panel.
6. Allow approximately one minute for the CRT filament to warm up. The blinking cursor should appear in the upper left corner of the screen. If the cursor still does not appear, a malfunction is indicated.
7. The 06-146 CRT Test Program may now be executed for Local Operation.

4. PASLA INTERCONNECTIONS

The CRT may be interfaced to an INTERDATA Processor through the PASLA. The PASLA contains the hardware to receive and transmit most of the normal RS-232C lines in an asynchronous mode. These lines include: RING, DSRDY, CARRIER, DTR, RQ2S, CL2S, TDATA, RDATA, REV CHAN REC, and REV CHAN TRANS.

When connecting the PASLA to a CRT (or most other local terminals), it is necessary to disable (force to zero) the RS-232 status bits which are not equipped on the terminal. The PASLA has wire-wrap stakes equipped for this purpose. The following is a summary of PASLA straps required for operation with the M46-102 or M46-103 CRT.

STRAP	FUNCTION
7-8 (Add)	FDX option
CF-GO (Add)	Force CARR Status = 0
CB-G3 (Add)	Force CL2S active
HD-G4 (REMOVE)	FDX Option

In addition, the straps A1-K1 must be equipped to select the required baud rate. This may be in the range of 75 to 9600 baud and is described in the PASLA Instruction Manual, Publication Number 29-310, which is included with the PASLA. Note that the character format/baud rate of PASLA is programmable. The CRT must be strapped to match these programmed characteristics.

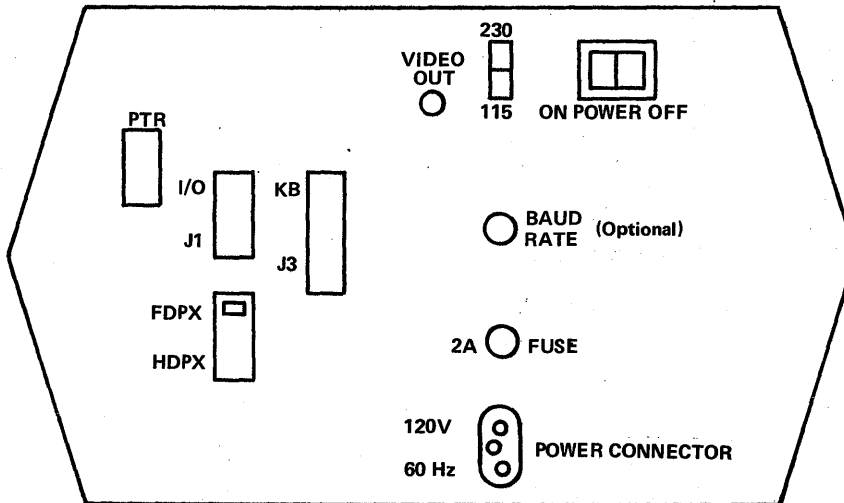
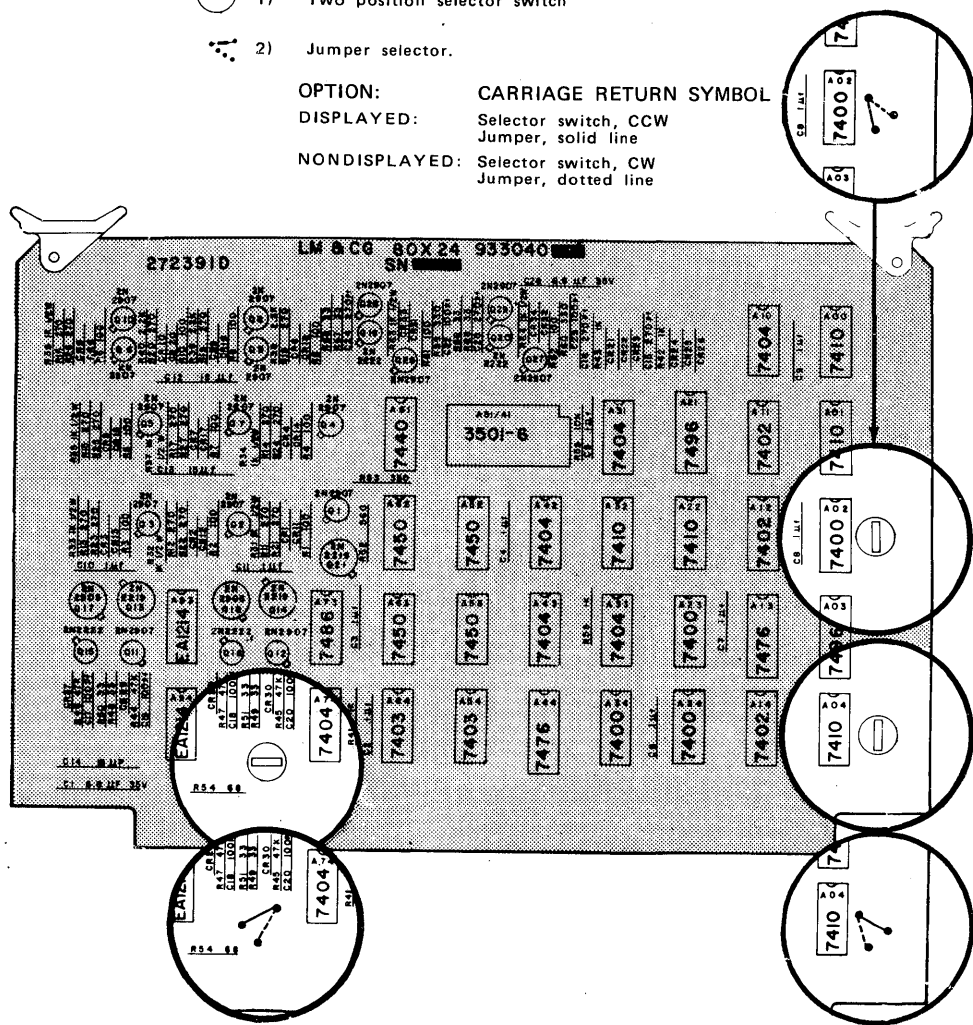


Figure 3. CRT Rear View

NOTE: TWO METHODS OF PCB OPTION SELECTION ARE USED

- 1) Two position selector switch
- 2) Jumper selector.

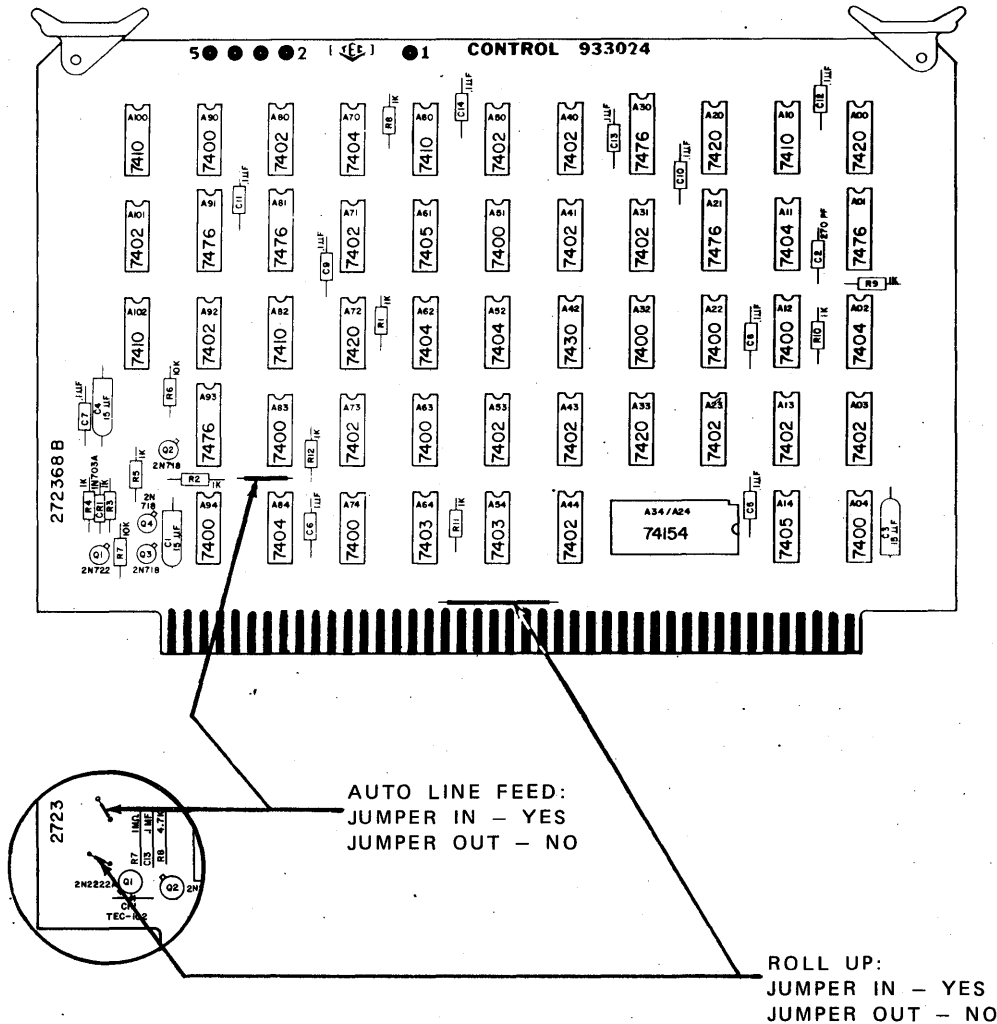
OPTION: CARRIAGE RETURN SYMBOL
 DISPLAYED: Selector switch, CCW
 Jumper, solid line
 NONDISPLAYED: Selector switch, CW
 Jumper, dotted line



OPTION: CHARACTER COLOR
 Black on White: Selector switch, CW
 Jumper dotted line
 White on Black (Normal Video):
 Selector switch, CCW
 Jumper, solid line

OPTION: CURSOR SYMBOL
 DISPLAYED: Selector switch, CW
 Jumper, solid line
 NONDISPLAYED: Selector switch, CCW
 Jumper, dotted line

Figure 4. Switch/Jumper Options on 27-054 Line Memory and Character Generator PCB-Location 2.

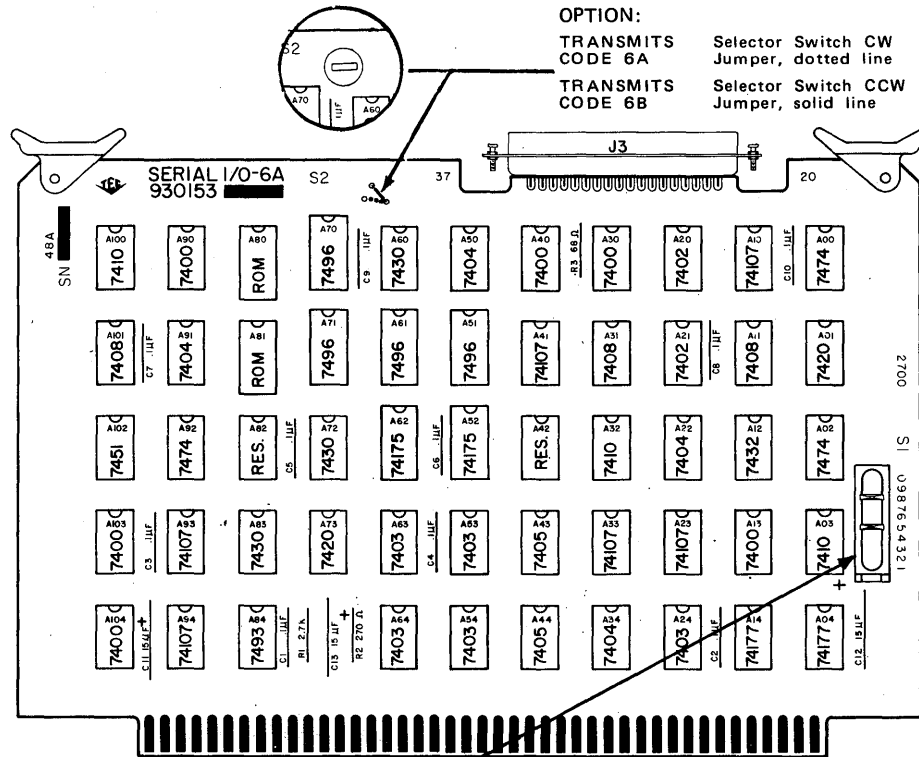


NOTE: TWO CONTROL PCB LAYOUTS ARE IN USE AND AFFECT THE LOCATION OF JUMPER WIRE LOCATIONS AS SHOWN.

Figure 5. Jumper Wire Options on 27-054 Control PCB-Location 4.

NOTE: TWO METHODS OF PCB OPTION SELECTION ARE USED

- 1) Two position selector switch
- 2) Jumper selector.



OPTION:

- TRANSMITS CODE 6A Selector Switch CW Jumper, dotted line
- TRANSMITS CODE 6B Selector Switch CCW Jumper, solid line

SWITCH S1 See Table 4 below:

TABLE 4

SWITCH SETTINGS: SERIAL I/O, BOARD 6A

SWITCH	ROTOR	POSITION	
S1	A	1	Not Used
		2	Even Parity - Transmitted
		3	Odd Parity - Transmitted
		4	No Parity - Mark Transmitted
S1	B	6	10 Bits Transmitted
		7	11 Bits Transmitted
S1	C	9	EOL Bell Disabled
		0	EOL Bell Enabled

Figure 6. Switch Options, Serial I/O PCB-Location 6.

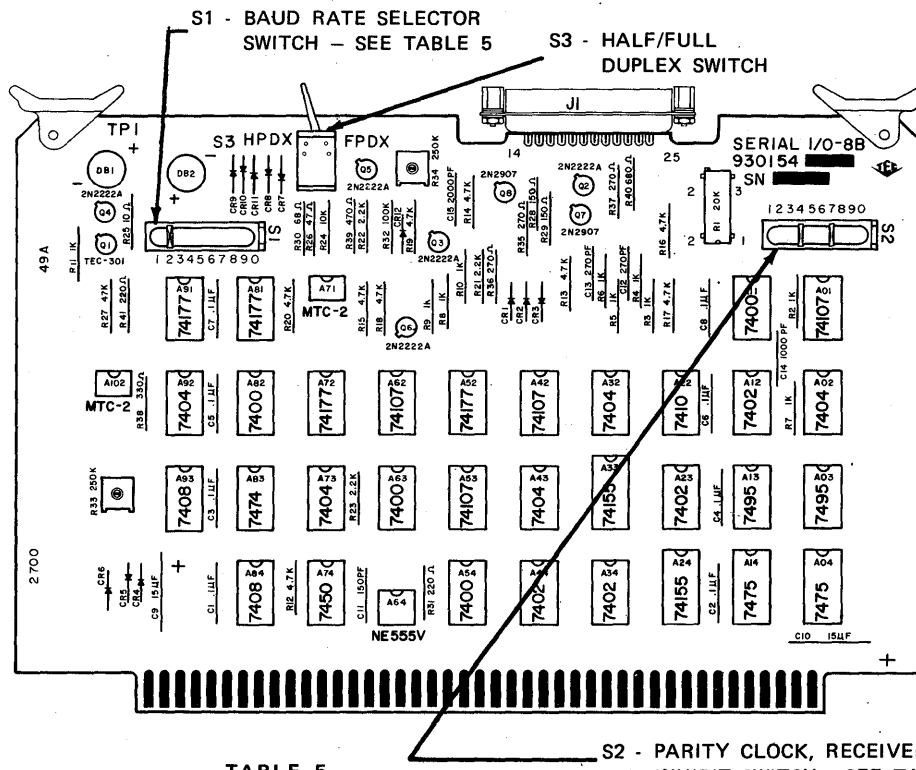


TABLE 5
SWITCH SETTINGS: SERIAL I/O, BOARD 8B

SWITCH	ROTOR	POSITION			
S1	A	3	150 Baud (also 110 Baud)		
		4	300 Baud		
		5	600 Baud		
		6	1200 Baud		
		7	2400 Baud (also 1800 Baud)		
		8	4800 Baud		
		9	9600 Baud		
		0	EXTERNAL CLOCK (Baud Rate Switch Option)		
		S2	A	1	No Parity Check on RCV
				2	Odd Parity RCVD
3	Even Parity RCVD				
5	Normal Clock				
6	Special Clock				
8	Inhibit RCV During Xmit				
9	No Inhibit RCV During Xmit				
S3 (Toggle)		UP	Half-Duplex		
		DOWN	Full-Duplex		

Figure 7. Switch Options, Serial I/O PCB-Location 8.

M46-102 CRT (EDITING) PROGRAMMING SPECIFICATION

1. INTRODUCTION

This specification contains a description of the editing CRT and the information necessary to program the system. The CRT interfaces to the Multiplexor Bus or Selector Channel Bus through the M47-102 Programmable Asynchronous Single Line Adapter (PASLA).

The PASLA comprises one full duplex interface with an even device address for the Receive side and an odd address for the Transmit side. There is an Interrupt flip-flop associated with each side.

2. CONFIGURATION

The CRT can be used on any Model 50, 70, 74, 80 or 85 Processor.

3. OPERATING PROCEDURES

3.1 Applying Power

Before connecting power to the Terminal:

1. Turn the POWER switch on the back panel to OFF. (See Figure 1)

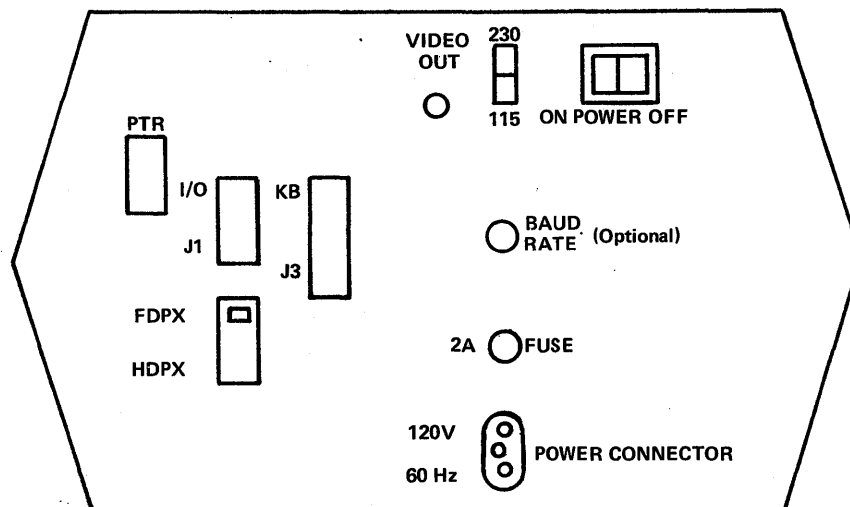


Figure 1. Back Panel

2. Plug the keyboard cable into KB-J3 on the back panel. Insure that the slide locks on the connector are securely fastened.
3. Attach the appropriate interface cable to J1 and fasten securely with the two 4-40 screws.

- Attach the power cord to the POWER CONNECTOR on the back panel and to a standard 115VAC, 60 Hz, 3 wire grounded outlet (or to 240 VAC if so ordered).

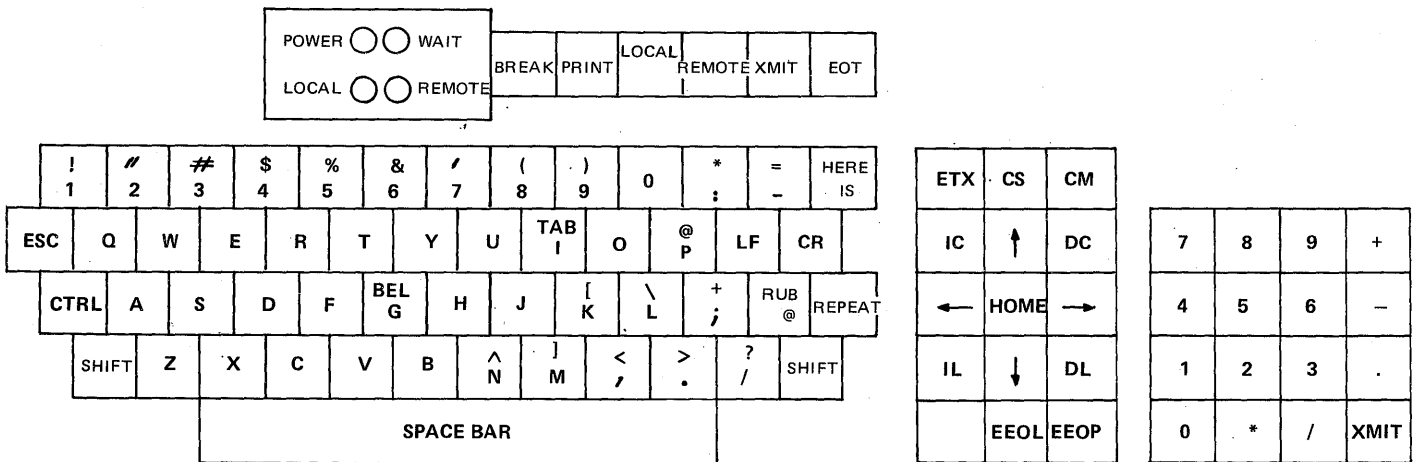
WARNING

USE A 3 PRONG ADAPTER WITH A SAFETY GROUND PROPERLY CONNECTED. NEVER CUT THE SAFETY GROUND PIN ON THE POWER CORD FOR USE WITH A 2-HOLE SOCKET AS THIS PRESENTS A SHOCK HAZARD.

- Turn the POWER switch ON. When the power is applied to the unit, the POWER switch is illuminated. If the switch fails to light, check the 2 amp fuse on the back panel.
- Allow approximately one minute for the CRT filament to warm up. The blinking cursor should appear in the upper left corner of the screen. If the cursor still does not appear, malfunction is indicated.
- The 06-146 CRT Test Program may now be executed for Local Operation.

3.2 Keyboard

The CRT terminal uses the basic keyboard arrangement of a Teletypewriter. Figure 2 shows the keyboard layout. As displayable keys are depressed, the characters appear above the cursor and the cursor is moved right one position. Near the end of a line, the bell in the keyboard rings. At the end of the line, the cursor automatically moves to the beginning (left) of the line below.



NOTE: Refer to Table 1 for the hexadecimal data generated for each key. The CRT transmits even parity if the option is implemented.

Figure 2. Keyboard Arrangement

After the bottom line of the screen is filled, the cursor normally returns to the Home position at the beginning (left) of the top line of the screen. If the Roll up and Auto Line Feed options are implemented, a Line Feed and Carriage Return are generated on the bottom line when the Return Key is depressed. The page of data automatically rolls up one line, erasing the top line and moving line 2 to line 1, etc. The cursor goes to the extreme left of the bottom line which is blank.

If the Return Key is not depressed before the bottom line is filled, no roll up occurs and the cursor goes to the Home position.

TABLE 1. CHARACTER DISPLAY

	CNTRL	SHIFT	CNTRL SHIFT	SHIFT	CNTRL SHIFT
A	AA 41	81	AA 41	81	
B	BB 42	┘┘ 82	BB 42	┘┘ 82	
C	CC C3	┘┘ 03	CC C3	┘┘ 03	
D	DD 44	84	DD 44	84	
E	EE C5	05	EE C5	05	
F	FF C6	06	FF C6	06	
G	GG 47	87 bell	GG 47	87 bell	
H	HH 48	88	HH 48	88	
I	II C9	09 tab	II C9	09 tab	
J	JJ CA	0A	JJ CA	0A	
K	KK 4B	8B	[[DB	1B	
L	LL CC	0C	\\ 5C	9C	
M	MM 4D	8D]] DD	1D	
N	NN 4E	8E	^^ DE	1E	
O	OO CF	0F	<< 5F	9F	
P	PP 50	90	@@ C0	00	
Q	QQ D1	11	QQ D1	11	
R	RR D2	12	RR D2	12	
S	SS 53	93	SS 53	93	
T	TT D4	14	TT D4	14	
U	UU 55	95	UU 55	95	
V	VV 56	96	VV 56	96	
W	WW D7	17	WW D7	17	
X	XX D8	18	XX D8	18	
Y	YY 59	99	YY 59	99	
Z	ZZ 5A	█ 9A	ZZ 5A	█ 9A	
0	00 30	00 30	00 30	00 30	
1	11 B1	11 B1	!! 21	!! 21	
2	22 B2	22 B2	"" 22	"" 22	
3	33 B3	33 B3	## A3	## A3	
4	44 B4	44 B4	\$\$ 24	\$\$ 24	
5	55 B5	55 B5	%% A5	%% A5	
6	66 B6	66 B6	&& A6	&& A6	
7	77 B7	77 B7	'' 27	'' 27	
8	88 B8	88 B8	((28	((28	
9	99 B9	99 B9)) A9)) A9	

:	:: 3A	:: 3A	** AA	** AA
;	;; BB	;; BB	++ 2B	++ 2B
/	// AC	// AC	<< 3C	<< 3C
-	-- 2D	-- 2D	== BD	== BD
.	.. 2E	.. 2E	>> BE	>> BE
/	// AF	// AF	?? 3F	?? 3F
RUB OUT	FF	FF	FF	FF
SPACE	A0	A0	A0	A0
LINE FEED	0A	0A	0A	0A
CAR. RET.	8D	8D	8D	8D
ESC	1B	1B	1B	1B

HERE IS	05	05	05	05
EEOL			63	63
IC			E4	E4
IL			65	65
CS			66	66
→	E7	E7	E7	E7
↓	E8	E8	E8	E8
HOME	69	69	69	69
EEOP			F3	F3
DC			74	74
DL			F5	F5
CM			F6	F6
←	77	77	77	77
↑	78	78	78	78
	E2	E2	72	72
+	++ 2B	++ 2B	++ 2B	++ 2B
XMIT	6A	6A	6A	6A
EOT	84	84	84	84
PRINT	60	60	60	60

EXAMPLE:

KEY (S)	DISPLAY
L	LL CC
L CNTRL	0C
L SHIFT	\\ 5C
L CNTRL SHIFT	9C

3.3 Terminal Codes

Table 2 shows the ASCII codes recognized by the CRT. The codes in Columns 0 and 1 of Table 2 are generated by use of the CTRL key plus the corresponding keys in Columns 4 and 5 respectively. Codes in brackets are used within the Terminal. Codes in parenthesis are also generated directly on the keyboard. All other codes in Columns 0 and 1 are ignored by the Terminal.

TABLE 2. TERMINAL CODE CHART

					Column								
					0	1	2	3	4	5	6	7	
B I T S	4	5	6	7	Row								
	0	1	0	1	0	1	0	1	0	1	0	1	
0	0	0	0	0	0	NUL	DLE	SPACE	0	@	P	[(PRINT)]	[(REL)]
0	0	0	1	1	1	SOH	DC1	!	1	A	Q		
0	0	1	0	2	2	[STX]	DC2	"	2	B	R	(BFK1)	BFK2
0	0	1	1	3	3	[(ETX)]	DC3	#	3	C	S	[(EOL)]	[(EOP)]
0	1	0	0	4	4	(EOT)	DC4	\$	4	D	T	[(IC)]	[(DC)]
0	1	0	1	5	5	(ENQ)	NAK	%	5	E	U	[(IL)]	[(DL)]
0	1	1	0	6	6	ACK	SYN	&	6	F	V	[(CS)]	[(DM)]
0	1	1	1	7	7	[(BEL)]	ETB	'	7	G	W	[((→))]	[((←))]
1	0	0	0	8	8	BS	CAN	(8	H	X	[((↓))]	[((↑))]
1	0	0	1	9	9	[(TAB)]	EOM)	9	I	Y	[(HOME)]	[(SPS)]
1	0	1	0	A	A	[(LF)]	[(SUB)]	(*)	:	J	Z	[(XMIT)]	[(EPS)]
1	0	1	1	B	B	VT	(ESC)	+	;	K	[[(SBS)]
1	1	0	0	C	C	FF	FS	,	<	L	\	[(LCA)]	[(EBS)]
1	1	0	1	D	D	[(CR)]	GS	-	=	M]	[(RCA)]	[(LOCK)]
1	1	1	0	E	E	SO	RS	.	>	N	^	SDR	[(HLO)]
1	1	1	1	F	F	SI	US	/	?	O	-	[(CDP)]	(RUB OUT)

The symbols used on Table 2 that are recognized by the terminal are explained below. An asterisk (*) beside the symbol means that the shift key must also be depressed.

STX Start of Text. The STX character (\perp) is displayed.

ETX End of Text. The ETX character (\lrcorner) is displayed. The ETX code effects the XMIT and PRINT functions.

ENQ Depressing the HERE IS key generates the ENQ code, ASCII 05. Initiates automatic answer back when option is provided.

BEL Bell Code. Rings bell in the keyboard when received.

TAB	Field Tab Code. Causes the cursor to advance to the position immediately following the next tab stop (EPS Code). If no tab stops are present, the cursor will stop at the Home position.
LF	Line Feed. Causes cursor to descend one line, or causes roll-up from bottom line if option is selected.
CR	Carriage Return. The cursor goes to the beginning (left) of the present line. An Automatic Line Feed may be optionally generated.
SUB	The full 35 dot matrix (■) is displayed. This character is optionally displayed if a parity error occurs on a received character.
PRINT	When the PRINT code is received by the terminal, a signal is sent to the optional hard copy adapter to initiate off-line printing. The Processor must have previously issued a Keyboard Lock. Characters are output from the present cursor position to the first ETX character, or to the end of the page if no ETX is present. A Halt Local Output (HLO) command from the Processor causes the printer to stop after the present character.
BFK1, BFK2*	Blank Function Key. This key is located at the bottom left-hand position of the editing controls keyboard. ASCII code 62 or 72 is generated when this key is pressed without or with the Shift Key, respectively.
EEOL*	Erase to End of Line. All characters from the present cursor position to the end of the same line are replaced with spaces (X'20'). Protected characters will not be erased.
EEOP*	Erase to End of Page. All characters from the present cursor position to the end of the page are replaced with spaces. Protected characters are not erased.
IC*	Insert Character. The character at the present cursor position and all characters to its right (on the same line) are moved one space to the right. The cursor remains at the same position which is filled with a space (X'20'). The character moved off the end of the line is lost. This function is inhibited if any protected characters are on the screen.
DC*	Delete Character. The character at the present cursor position is deleted. All remaining characters on the line move one space to the left. The right most character position on the line is filled with a space (X'20'). This function is inhibited if any protected characters are on the screen.
IL*	Insert Line. All characters in the present line and on the remainder of the page are moved down one line. The present line is set to all spaces (X'20'), and the cursor moves to the beginning (left) of the present line. The last line on the screen is lost. This function is inhibited if any protected characters are on the screen.
DL*	Delete Line. All characters in the present line are lost and all remaining lines on the screen move up one line. The cursor goes to the beginning (left) of the present line. The bottom line on the screen is filled with spaces (X'20'). This function is inhibited if any protected characters are on the screen.
CS*	Clear Screen. Spaces (X'20') are written into every position on the screen except those positions that are protected. The cursor moves to the Home position or the first unprotected location if the Home position is protected.
CM*	Clear Memory. Spaces (X'20') are written into every position on the screen, including protected areas. The cursor moves to the Home positions.
→	Right Cursor. The cursor moves right one position. If already at the end of a line, the cursor goes to the beginning of the line below. If at the end of the last line, the cursor goes to the Home position. If the new cursor position is in a protected area, the cursor goes to the first location following the protected area.

←
Left Cursor. The cursor moves left one position. If already at the beginning of a line, the cursor goes to the end (right) of the line above. If at the home position, the cursor goes to the end (right) of the last line on the page. If the new cursor position is in a protected area, the cursor goes to the first location ahead of the protected area.

↓
Down Cursor. The cursor moves down one line, but remains in the same column. If at the bottom line, the cursor moves to the top line, same column. If the new cursor position is in a protected area, it goes to the first location following the protected area.

↑
Up Cursor. The cursor moves up one line, but remains in the same column. If at the top line, the cursor moves to the bottom line, same column. If the new cursor position is in a protected area, the cursor goes to the first location ahead of the protected area.

HOME

Home Cursor. The cursor moves to the beginning (left) of the first line on the screen. If the Home position is protected, the cursor goes to the first unprotected location.

SPS

Start Protect Sequence. An SPS code can only be issued by the Processor. The Processor must have previously issued a Keyboard lock. Any characters appearing after the SPS code and before the next EPS code cannot be modified by Keyboard input. The cursor cannot be manually positioned to a protected area. If the Processor first issues a Keyboard lock, it can modify a protected area. If no EPS code is present, the protected area is from the SPS code to the end of the page unless the SPS code is at the Home position in which case protect is overridden. There must be at least one unprotected area.

EPS

End Protect Sequence. The EPS code is used to identify the end of a protected sequence that began with an SPS code, or as a field tab. See TAB. The EPS code can only be issued by the Processor. A Keyboard Lock must have been previously issued.

XMIT

Transmit. The XMIT function is used to transfer a page or partial page from the CRT to the Processor. Normal operation of the XMIT function is as follows:

<u>Operator</u>	<u>CRT Terminal</u>	<u>Processor</u>
1. Depress Local	Local Light goes on	
2. Compose message	Data displayed on screen	
3. Place ETX at end of message.	ETX character displayed on screen	
4. Home Cursor		
5. Depress Remote	Remote Light goes on	
6. Depress XMIT	X'6A' code output	Receives X'6A' code, Prepares buffer, Transmit Keyboard Lock code, Transmit XMIT code. Switch PASLA to non-echoplex Read Mode.
7.	Message is transmitted to Processor starting at the present cursor position and continuing until an ETX is encountered or the end of the page.	Receives message, Transmits Keyboard release.

Optionally, the XMIT Key can be replaced by any pre-arranged code or set of codes. In response to this, the Processor must transmit a Keyboard Lock and an XMIT code (X'6A') to start the transmission. Appendix 5 is a sample routine for reading the CRT screen.

SBS Start Blink Sequence. The SBS and EBS codes can only be issued by the Processor. Characters following an SBS code and preceding the next EBS code blink at a 2 Hz rate.

EBS End Blink Sequence. The EBS code is used to identify the end of a blink sequence.

LCA Load Cursor Address. When the LCA code is received, the next two characters are accepted as cursor addresses; first the horizontal address (column number), then the vertical address (line number). The two addresses must be presented in ones complement form. The horizontal address can be within the range 0 to 79 decimal. The vertical address can be within the range 0 to 23 decimal. Any address outside the range is ignored.

Table 3 shows the conversion from decimal to ones complement hexadecimal. From the table, the proper sequence of output characters to position the cursor to column 7 of line 12 is:

X'6C' LCA Code
 X'78' Column 7
 X'73' Line 12

TABLE 3. CURSOR ADDRESSES

LSD \ MSD	0	1	2	3	4	5	6	7	8	9
0	7F	7E	7D	7C	7B	7A	79	78	77	76
1	75	74	73	72	71	70	6F	6E	6D	6C
2	6B	6A	69	68	67	66	65	64	63	62
3	61	60	5F	5E	5D	5C	5B	5A	59	58
4	57	56	55	54	53	52	51	50	4F	4E
5	4D	4C	4B	4A	49	48	47	46	45	44
6	43	42	41	40	3F	3E	3D	3C	3B	3A
7	39	38	37	36	35	34	33	32	31	30

To change only the vertical or horizontal cursor address without affecting the other, substitute an invalid address for the vector that isn't to change. For example, the following character sequence sets the cursor to column 72 of the present line:

X'6C' LCA Code
 X'37' Column 72
 X'00' Invalid address, no line change

Seven bits are used by the CRT to determine horizontal cursor address validity. Five bits are used to determine vertical address validity.

Appendix 3 is a sample subroutine for cursor positioning.

RCA Read Cursor Address. When the RCA code is received, the CRT transmits the two character cursor address. The first character is the ones complement of the horizontal address (column number), the second character is the ones complement of the vertical address (line number). The horizontal address is within the range X'7F' to X'30', disregarding the parity bit. See Table 3. The vertical address is within the range X'7F' to X'68' disregarding the parity bit. The PASLA must not be in echoplex to receive the cursor address.

Appendix 4 is a sample routine for reading in the cursor address.

LOCK Keyboard Lock. The LOCK function is issued by the Processor to inhibit data input from the keyboard.

REL Release Keyboard. The REL function is issued by the Processor to re-enable data input from the Keyboard.

HLO Halt Local Output. Signals the Hard Copy Adapter to stop printing. See PRINT.

SDP Set Data Panel. When received, the CRT accepts the next character to light 1 of 16 indicators on the Data Panel Option.

CDP Clear Data Panel. When received, the CRT clears all 16 indicators on the Data Panel Option.

4. DATA FORMAT

The PASLA may be programmed to accommodate a variety of character formats and baud rates. See the PASLA Programming Specification, 02-270A22, in the 29-301 PASLA Instruction Manual. In addition, the CRT has switch options to select parity, number of stop bits, and baud rates. This information is in Manual 29-327 which is included with the CRT.

The following lists the standard characteristics:

	PASLA
BAUD RATE	9600
DATA BITS	7
PARITY	EVEN
STOP BITS	1

Figure 3 shows the Character Format:

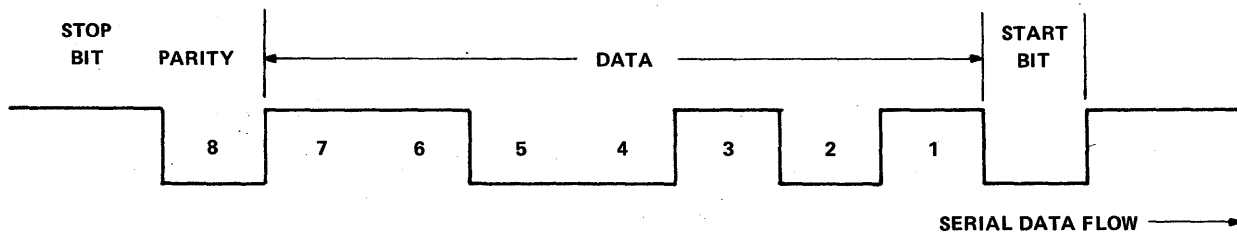


Figure 3. Character Format

5. PROGRAMMING INSTRUCTIONS

The Processor I/O instructions are used to communicate with the CRT Terminal through the PASLA. The following paragraphs describe how Processor I/O instructions may be used with the system.

5.1 Program Instructions

5.1.1 Sense Status (SS or SSR). The Sense Status instruction is used to determine if character transfers are complete.

5.1.2 Output Command (OC or OCR). The Output Command instruction is used to set the PASLA to the Receiver or Transmitter Mode and to select character format. Two command bytes are required to perform these functions with PASLA.

5.1.3 Write Data (WD or WDR). The Write Data instruction is used to output characters to the CRT terminal screen.

5.1.4 Read Data (RD or RDR). The Read Data Instruction is used to input characters from the CRT terminal.

5.1.5 Acknowledge Interrupt (AI or AIR). The Acknowledge Interrupt instruction is used to service interrupts. Execution of this instruction returns the address and status of the interrupting line.

5.1.6 Communications Instructions (PASLA only). The PASLA accommodates the Communication Instructions in the Communications Processors.

5.2 Status and Command Bytes

Table 4 contains the PASLA interface Status and Command Byte Data applicable to the CRT Terminal.

TABLE 4. STATUS AND COMMAND BYTE DATA

BIT NUMBER	0	1	2	3	4	5	6	7
STATUS (REC)	OV	PF	FR ERR	0	BSY	EX	0	0
STATUS (TRANS)	0	0	0	0	BSY	0	0	0
COMMAND 1	DIS	EN	DTR	ECHO- PLEX	0	TRANS LB	WRT/ RD	1
COMMAND 2	0	CLK	← DATA BITS →		STOP BITS	← PARITY →		0

STATUS

*OV The Overflow status bit is set if the previously received character is not read before the present character is assembled. Overflow is reset at the end of the next Read Data only if the failure condition disappears (i. e., a Read Data is issued).

*PF This bit is set when the received parity disagrees with the programmed parity (EVEN parity). The PF status is reset at the end of the next character if the failure condition disappears. The PASLA is normally programmed for no parity checking (Bits 5 and 6 of Command 2 = 00) so PF never sets.

*FRERR This bit is set to indicate that the received character has no stop bits. If the assembled character is zero, then a line break sequence is indicated. This occurs when the Break Key is depressed. This bit resets only when a valid character with stop bits is received.

BSY When this bit is inactive, the device is ready to transfer data. This bit is forced active if the CRT Terminal is Off-Line. In the Read Mode, BSY is active when a character is not assembled; in the Write Mode, BSY is active if the CRT Terminal has not yet accepted a character. If enabled, an interrupt is generated when BSY goes inactive. In the Read mode, when an OV occurs and the BSY status bit is zero, a Read Data instruction must be issued to set the BSY bit to its correct (ONE) state.

EX This bit is set whenever OV, PF, or FRERR is set on the Receive side. This bit is always zero on the Transmit side.

With PASLA, to determine whether the CRT Terminal is On-Line or not, the status of the Receive side must be examined. If the status byte is '0C' (BUSY and EX), a Device Unavailable condition is indicated.

*These status bits are set at End of Character time when BUSY drops. Since the resetting of BUSY causes an interrupt (if enabled), these bits do not generate individual interrupts. At this point a Read Data instruction must be issued to set the Busy bit to its correct (ONE) state.

COMMANDS

In the PASLA Command 1, the DTR, ECHOPLEX, and WRT/RD bits are shared by the Transmitter and Receiver, however, the EN/DIS bits are separate for Transmit and Receive. In FDX operation, the EN/DIS must be independently programmed as follows. To change EN/DIS on the Receive side, issue a Command with the WRT/RD bit = 0. To change the EN/DIS on the Transmit side, issue a Command with the WRT/RD bit = 1.

CLK Setting this bit selects the highest strapped clock rate. Resetting this bit selects the lowest strapped clock rate.

DATA BITS These two command bits select the number of data bits transferred per character as follows:

BIT 2	3	
0	0	5 Data bits
0	1	6 Data bits
1	0	7 Data bits
1	1	8 Data bits

STOP BITS This command bit selects the number of stop bits transferred per character.

BIT 4	
0	1 Stop bit
1	2 Stop bits

PARITY These two command bits select the parity checking logic in the PASLA.

BIT 5	6	
0	0	None
0	1	None
1	0	Odd
1	1	Even

The second PASLA command is shared by both the Transmit and Receive Sides, and consequently may be issued to either device number. The second command has the preferred value of X'78' that conditions the PASLA to the following:

1. Highest strapped baud rate (9600 baud standard)
2. 8 data bits per character
3. No parity checking
4. Two stop bits

<u>DISABLE</u>	<u>ENABLE</u>	
0	0	No change
0	1	Enable
1	0	Disable (Interrupt queued)
1	1	Complement (Change state)

- TRANS LB** Transmit a continuous space (zero) to the Terminal. This bit should always be zero.
- DTR** This bit must always be a one to enable character transfers between PASLA and the CRT.
- ECHOPLEX** When this bit is active, it causes data received from the CRT Keyboard to be transmitted back to the CRT on the TRANSMITTED DATA (BA) line. The PASLA also assembles the character as in the normal data mode. This feature is normally used to provide visual verification of the data received by the CRT. This command must not be issued while transmitting a character. When this bit is inactive, characters read from the Keyboard are not displayed.

6. PROGRAMMING SEQUENCES

Care should be exercised when switching the PASLA from the Write Mode to echopléxed Read Mode. Any time such a transition must be made, the last character output should be a rub-out (all ones). If not, the last character output may be mutilated. Switching from the Write Mode to the non-echopléxed Read Mode causes no problems.

Appendix 1 shows a sample program for transferring data from the CRT keyboard using the PASLA. Appendix 2 shows a sample program for transferring data to the CRT screen using the PASLA.

7. INTERRUPTS

An interrupt occurs, if enabled, when BSY → 0. If a character has ever been input or output, the PASLA will have queued an interrupt whether interrupts were enabled or not.

Consequently, the programmer should always be prepared to ignore the very first interrupt received from either the transmit or receive side. On the first interrupt, if the PASLA status is only Busy, ignore the interrupt.

After outputting a last character, the programmer should wait for the final interrupt that occurs as soon as the PASLA finishes with the last character.

When switching Interrupt Enable from the transmit side to the receive side, an extra output command must be inserted to restore the WRT/READ bit to zero. For example:

1. Output Command Receive side, Enable-Read
2. Output Command Transmit side, Disable Write
3. Output Command Receive side, Read

8. INITIALIZATION

When the Initialize Switch on the Display Panel is engaged (or power failure restart sequence), the PASLA is placed in the Disable Mode. The OV, PF, and BRK status bits cannot be guaranteed. Because of this, the programmer should take precautions to ignore these bits on the first interrupt. A Read Data (RD or RDR) should be issued to insure that BSY is equal to a one (1).

9. DEVICE NUMBER

The PASLA is normally strapped for addresses X'10' and X'11'. The even address is for the Receive side and the odd address is for the Transmit side.

10. SAMPLE PROGRAMS

See Section 6.

11. TESTING

The PASLA is tested independently at INTERDATA using the PASLA OFF-LINE TEST PROGRAM, 06-127. The PASLA and CRT Terminal are then tested together using the CRT TEST PROGRAM, 06-146.

APPENDIX 1.

SAMPLE PROGRAM FOR DATA INPUT FROM THE KEYBOARD

* SUBROUTINE INPUTS A CHARACTER FROM THE
* CRT KEYBOARD. REGISTER DEV0 CONTAINS
* THE PASLA RECEIVE ADDRESS (EVEN ADDRESS)

*

* CALL IS: BAL RET1, INPUT

*

INPUT	OC	DEV0, TREAD	SELECT ECHOPLEX READ
READ	OC	DEV0, SECOND	SET PASLA CONDITION
SENS	SSR	DEV0, STAT	SENSE STATUS
	BO	STATER	BAD STATUS
	BCS	SENS	BUSY, LOOP
	RDR	DEV0, CHAR	INPUT CHARACTER
	BAL	RET2, PARCHK	TEST PARITY
	NHI	CHAR, X'7F'	REMOVE PARITY BIT
	BR	RET1	RETURN

* INPUT CHARACTER IS IN REGISTER CHAR

*

DEV0	EQU	0	REGISTER
RET2	EQU	2	ASSIGNMENTS
STAT	EQU	9	
CHAR	EQU	11	
RET1	EQU	15	

*

*

SECOND	DC	X'7878'	
TREAD	DC	X'B9B9'	

APPENDIX 2.

SAMPLE PROGRAM FOR DATA OUTPUT TO THE CRT SCREEN

* SUBROUTINE OUTPUTS CONTENTS

* REGISTER CHAR TO THE CRT

* REGISTER DEV1 CONTAINS THE PASLA

* TRANSMIT ADDRESS (ODD ADDRESS)

*

* CALL IS: BAL RET2,OUTCHR

*

OUTCHR	OC	DEV1,SECOND	SET PASLA CONDITION
	OC	DEV1,TWRT	SELECT WRITE MODE
SENSE	SSR	DEV1,STAT	SENSE STATUS
	BCS	SENSE	LOOP ON BUSY
	WDR	DEV1,CHAR	OUTPUT CHARACTER
	BR	RET2	RETURN

*

*

DEV1	EQU	1	REGISTER
RET2	EQU	2	ASSIGNMENTS
STAT	EQU	9	
CHAR	EQU	11	

*

*

SECOND	DC	X'7878'
TWRT	DC	X'ABAB'

APPENDIX 3.

SAMPLE PROGRAM FOR POSITIONING THE CURSOR

* SUBROUTINE POSITIONS THE CURSOR TO
 * THE POSITION SPECIFIED IN REGISTER TAB
 *
 * CALL IS: BAL RET1,SETCSR

SETCSR	LHI	CHAR,X'6C'	LCA CODE
	BAL	RET2,OUTCHR	OUTPUT IT
	EXBR	CHAR,TAB	MS 8 BITS = COLUMN
	XHI	CHAR,X'7F7F'	ONES COMPLEMENT
	BAL	RET2,OUTCHR	OUTPUT COLUMN NO.
	EXBR	CHAR,CHAR	LS 8 BITS = LINE
	BAL	RET2,OUTCHR	OUTPUT LINE NO.
	BR	RET1	RETURN

*

*

RET2	EQU	2	REGISTER
TAB	EQU	8	ASSIGNMENTS
CHAR	EQU	11	
RET1	EQU	15	

*

*

APPENDIX 4.

SAMPLE PROGRAM FOR DETECTING THE CURSOR POSITION

- * ROUTINE READS THE PRESENT CURSOR POSITION
- * REGISTER DEV0 CONTAINS PASLA RECEIVE ADDRESS
- * REGISTER DEV1 CONTAINS PASLA TRANSMIT ADDRESS

LHI	CHAR, X'6D'		RCA CODE
BAL	RET2, OUTCHR		OUTPUT IT
SSR	DEV1, STAT		
BTBS	8, 1		WAIT FOR OUTPUT
OC	DEV0, NEREAD		NON-ECHOPLEX READ
BAL	RET1, READ		READ FIRST BYTE
LHR	TAB, CHAR		SAVE COLUMN NO.
BAL	RET1, READ		READ SECOND BYTE
EXBR	TAB, TAB		
OHR	TAB, CHAR		COMBINE WITH LINE NO.
NHI	TAB, X'7F7F'		REMOVE PARITY BITS
XHI	TAB, X'7F7F'		AND ONES COMP
*			
*			
DEV0	EQU	0	REGISTER
DEV1	EQU	1	ASSIGNMENTS
RET2	EQU	2	
TAB	EQU	8	
STAT	EQU	9	
CHAR	EQU	11	
RET1	EQU	15	
*			
*			
NEREAD	DC	X'A9A9'	

APPENDIX 5.

SAMPLE PROGRAM FOR INPUTTING THE ENTIRE CRT SCREEN

* THE OPERATOR HAS INDICATED THAT THE
 * PROCESSOR MAY READ THE ENTIRE CRT SCREEN
 *
 * ROUTINE HOMES CURSOR THEN INPUTS CHARACTERS
 * TO A 1920 BYTE BUFFER UNTIL AN ETX
 * CODE IS RECEIVED.
 *
 * CALL IS BAL RET1,RESCRN

RESCRN	XHR	TAB, TAB	CLEAR BUFFER INDEX
	LHI	CHAR, X'69'	
	BAL	RET2, OUTCHR	HOME CURSOR
	LHI	CHAR, X'7D'	
	BAL	RET2, OUTCHR	KEYBOARD LOCK
	LHI	CHAR, X'6A'	
	BAL	RET2, OUTCHR	XMIT CHARACTER
	SSR	DEV1, STAT	
	BTBS	8, 1	WAIT FOR CHARACTER
	OC	DEV0, NEREAD	SELECT NON-ECHOPLEX READ

*
 LOOP SSR DEV0, STAT
 BO STATER BAD STATUS
 BCS LOOP BUSY, LOOP
 RDR DEV0, CHAR INPUT BYTE
 BAL RET2, PARCHK TEST PARITY

* PARITY OK, CONTINUE

NHI	CHAR, X'7F'	REMOVE PARITY BIT
STB	CHAR, BUFF(TAB)	STORE IT
AIS	TAB, 1	INCREMENT INDEX
CLHI	CHAR, X'03'	ETX ?
BNE	LOOP	NO, LOOP

*

LHI	CHAR, X'70'	
BAL	RET2, OUTCHR	KEYBOARD RELEASE
BR	RET1	RETURN

*

*

DEV0	EQU	0	REGISTER
DEV1	EQU	1	ASSIGNMENTS
RET2	EQU	2	
TAB	EQU	8	
STAT	EQU	9	
CHAR	EQU	11	
RET1	EQU	15	

*

*

NEREAD	DC	X'A9A9'
BUFF	DS	1920

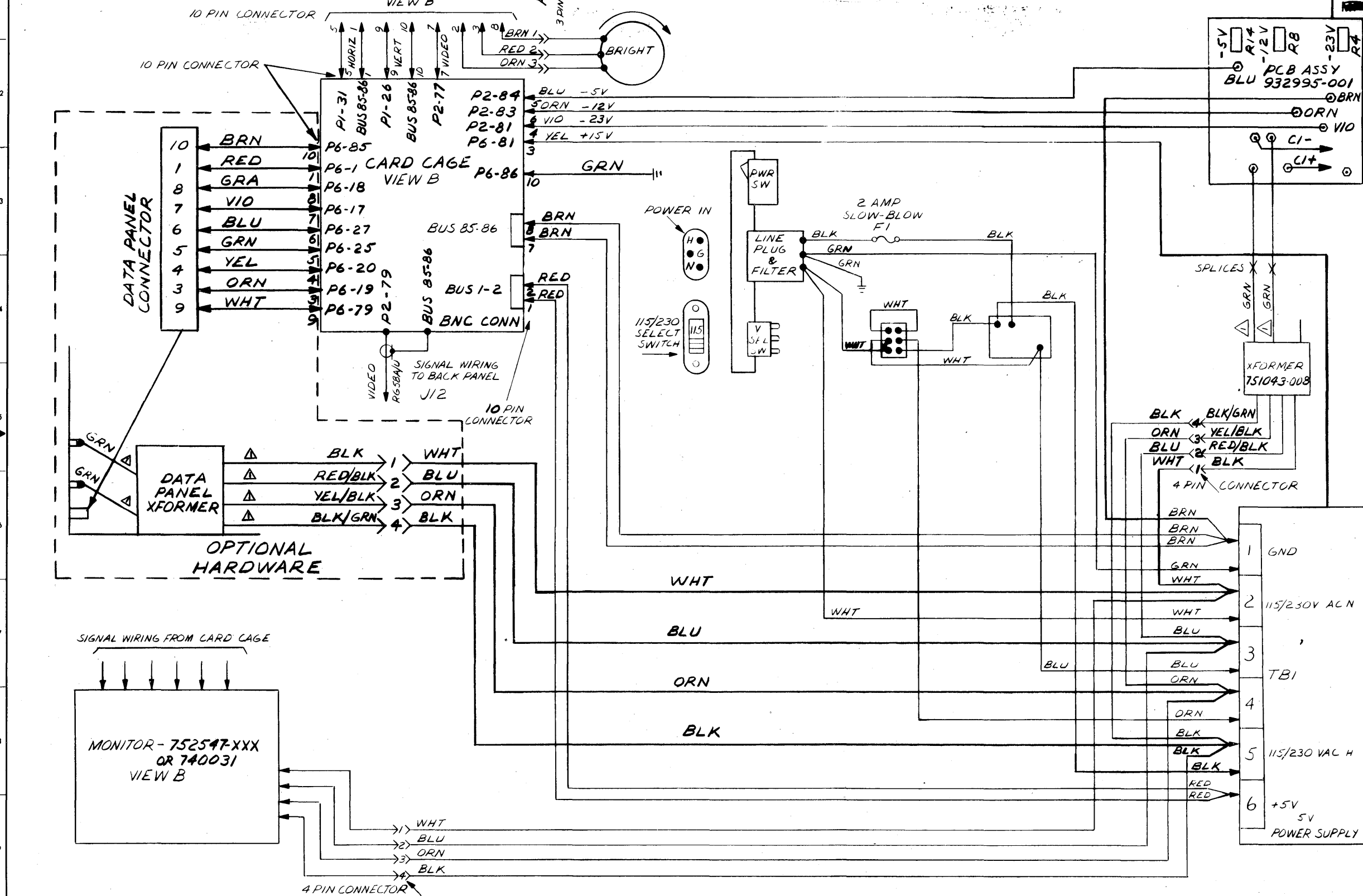
*

*

TEC NO	TERMINAL	SIGNAL WIRING	MONITOR
99/1933-001	DSX-XXXXA	VIEW A	VIEW A
99/1933-002	DSX-XXXXB	VIEW B	VIEW B
99/1933-003	TEC-7325A	VIEW C	VIEW C

A	RELEASED
B	DPA REVISED
C	REV PER DGN-ADDER-003 7630

RELEASED FOR PRODUCTION
 ENG. *Jan* DATE 9/26/73



INDEX TABLE	
SHT. NO.	FUNCTION
1	BLOCK DIAGRAM
2,3	BACK PANEL MAP
4	MONITOR
5,6	POWER SUPPLY
7,8	KEYBOARD
9-12	TIMING GENERATOR
13-15	LINE MEM & CHAR GEN
16-18	PAGE MEMORY
19-24	CONTROL
25-28	CORSOR CNTR
29-33	SERIAL I/O-6A
34-37	SERIAL I/O-8A
38	BACK PANEL COPPER
39	MOTHERBOARD ASSY

NOTE:
 THE REVISION LEVEL OF THIS SHEET IS CONSIDERED TO BE THE REVISION LEVEL OF THE DOCUMENT

REVISIONS				
REV.	DESCRIPTION	DCN	APPD	DATE
A	RELEASED		PM	11/72
B	NO CHG - SEE DCN	8436		
C	NO CHG - SEE DCN	8478		
D	REV PER DCN	8439		
E	NO CHG - SEE DCN	8606		

990051

+5V	1	2	+5V
7MHZ	3	4	
D2C	5	6	
D3C	7	8	SKA
SKB	9	10	SKC
SKD	11	12	SCAN 6
SCAN 7	13	14	SCAN 1&7
SCAN 2&6	15	16	SCAN 3&5
LDSR	17	18	LM CLK
SCAN A	19	20	SCAN X
CGØ1	21	22	CGØ2
ENSPL	23	24	HSYNC
CSR BLINK	25	26	VSYN
INHOSC	27	28	TEST RST
EXTOSC	29	30	
HSYN (M)	31	32	
PMRT	33	34	PMRT
PMCLK	35	36	PMCLK
TIME OUT	37	38	CHAR BLINK
EOM	39	40	EN EXT CLK
LDREG	41	42	BLANK
	43	44	
	45	46	
	47	48	
	49	50	
	51	52	
	53	54	
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	
	65	66	
	67	68	
	69	70	
	71	72	
	73	74	DSPLCK
CTR RST	75	76	DSPCMR
	77	78	
	79	80	
	81	82	
	83	84	
	85	86	

P1
TIMING GEN

+5V	1	2	+5V
7MHZ	3	4	
D2C	5	6	CSR CMR
D3C	7	8	SKA
SKB	9	10	SKC
SKD	11	12	SCAN 4
SCAN 7	13	14	SCAN 1&7
SCAN 2&6	15	16	SCAN 3&5
LD SR	17	18	LM CLK
SCAN A	19	20	SCAN X
CGØ1	21	22	CGØ2
ENSPL	23	24	HSYN
CSR BLINK	25	26	VSYN
LDLMSP	27	28	LD LM
LM→PM	29	30	REC LM
ENLMCLK	31	32	PMCLK→LM
	33	34	
PMCLK	35	36	
	37	38	
	39	40	EN EXT CLK
BLANK	41	42	
	43	44	
PMI1	45	46	PMO1
PMI2	47	48	PMO2
PMI3	49	50	PMO3
PMI4	51	52	PMO4
PMI5	53	54	PMO5
PMI6	55	56	PMO6
PMI7	57	58	PMO7
	59	60	
	61	62	
	63	64	
	65	66	
	67	68	
	69	70	
	71	72	
	73	74	
	75	76	DSPCMR
VIDEO (M)	77	78	
COMP VIDEO	79	80	
-23V	81	82	
-12V	83	84	-5V
GND	85	86	GND

P2
LM & CG

+5V	1	2	+5V
	3	4	
	5	6	ENPMCLK
	7	8	
CLR CAH	9	10	CLR CAV
	11	12	
	13	14	
	15	16	
	17	18	
SCANA	19	20	
	21	22	
	23	24	
LD PM	25	26	LDPMSP
LDLMSP	27	28	
	29	30	
	31	32	
	33	34	
PMCLK	35	36	PMCLK
	37	38	CHAR BLINK
EOM	39	40	
	41	42	EP
	43	44	
PMI1	45	46	PMO1
PMI2	47	48	PMO2
PMI3	49	50	PMO3
PMI4	51	52	PMO4
PMI5	53	54	PMO5
PMI6	55	56	PMO6
PMI7	57	58	PMO7
	59	60	
	61	62	PROTECT
	63	64	CM+MC
	65	66	
	67	68	
LOCK	69	70	
INHEDIT	71	72	
	73	74	
	75	76	
	77	78	
	79	80	
	81	82	
-12V	83	84	-5V
GND	85	86	GND

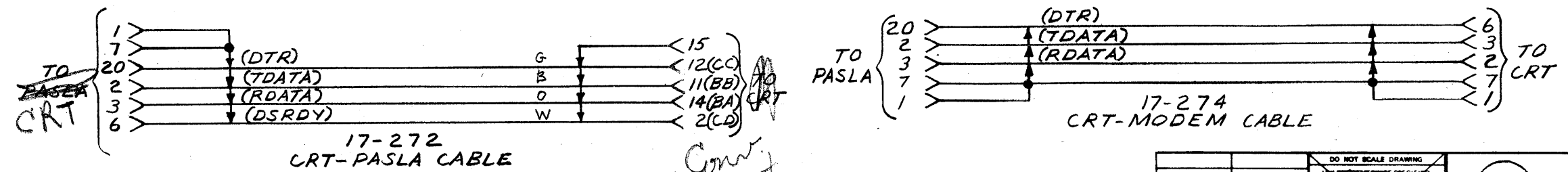
P3
PM

+5V	1	2	+5V
EOL	3	4	CSRCMPRV
CSRCMPR	5	6	
CAV+I	7	8	CAV-I
CLR CAH	9	10	CLR CAV
LD CAH	11	12	LD CAV
EN MAV+I	13	14	CAH
	15	16	CAH-I
	17	18	
DB1	19	20	DB4
DB3	21	22	DB6
DB5	23	24	
DB7	25	26	
LD PM	27	28	LDPMSP
LDLMSP	29	30	
LD→PM	31	32	REC LM
ENLMCLK	33	34	PMCLK→LM
PMRT	35	36	PMRT
	37	38	PMCLK
TIME OUT	39	40	LST LINE
EOM	41	42	EN EXT CLK
LD REG	43	44	EP
	45	46	
PMI1	47	48	PMO1
PMI2	49	50	PMO2
PMI3	51	52	PMO3
PMI4	53	54	PMO4
PMI5	55	56	PMO5
PMI6	57	58	PMO6
PMI7	59	60	PMO7
	61	62	PROTECT
DATA	63	64	CM+MC
RD EN CLR F	65	66	OBFULL
FUNC	67	68	
	69	70	
LOCK	71	72	
INHEDIT	73	74	
	75	76	
	77	78	
MC	79	80	
	81	82	
	83	84	
GND	85	86	GND

P4
CONTROL

+5V	1	2	+5V
EOL	3	4	CSRCMPRV
CSRCMPR	5	6	EMPMCLK
CAV+I	7	8	CAV-I
CLR CAH	9	10	CLR CAV
LD CAH	11	12	LD CAV
EN MAV+I	13	14	CAH+I
	15	16	CAH-I
	17	18	
DB1	19	20	DB4
DB3	21	22	DB6
DB5	23	24	
DB7	25	26	
	27	28	
	29	30	
LST CHAR	31	32	
PMRT	33	34	PMRT
PM CLK	35	36	PM CLK
	37	38	LST LINE
EOM	39	40	
	41	42	BELL
CAH→IR	43	44	CAV→IR
	45	46	CSR1
	47	48	CSR2
	49	50	CSR3
	51	52	CSR4
	53	54	CSR5
	55	56	CSR6
	57	58	CSR7
	59	60	
	61	62	
	63	64	
	65	66	
	67	68	
	69	70	
CTR RST	71	72	
	73	74	DSP CLK
	75	76	DSPCMR
	77	78	
	79	80	
	81	82	
	83	84	
GND	85	86	GND

P5
COUNTERS



*Conn
Panel*

930074		DO NOT SCALE DRAWING		TITLE CARD CAGE CONNECTIONS 400 SERIES
REV	DATE	FRAC	DEC	
1	11/72	1/16	1/100	SCALE: 2 OF 39
2		1/32	1/1000	

99006

REVISIONS			
REV	DESCRIPTION	DCN	DATE
A	RELEASED		9-1-72
B	NO CHG - SEE DCN	8436	9-1-72
C	NO CHG - SEE DCN	8478	9-1-72
D	REV PER DCN	8439	9-1-72
E	NO CHG - SEE DCN	8608	9-1-72

SPARE

+5V	1	2	+5V
EOL	3	4	OD-1
CSRCMPR	5	6	OD-2
CAV+I	7	8	OD-3
CLRCAH	9	10	CLRCAV
PRTCODE	11	12	LDCAV
OD-4	13	14	CAH+I
OD-5	15	16	CAH-I
DB1	17	18	DB2
DB3	19	20	DB4
DB5	21	22	DB6
DB7	23	24	DB8
SI	25	26	OD-6
CI	27	28	OD-7
	29	30	OD-8
PRT BSY	31	32	OA
PMRT	33	34	PMRT
	35	36	ODR
TIME OUT	37	38	LST LINE
EOM	39	40	EN EXT CLK
LD REG	41	42	BELL
CAH-IR	43	44	CAV-IR
CSRI	45	46	PMO1
CSR2	47	48	PMO2
CSR3	49	50	PMO3
CSR4	51	52	PMO4
CSR5	53	54	PMO5
CSR6	55	56	PMO6
CSR7	57	58	PMO7
ID-1	59	60	PMO8
DATA	61	62	PROTECT
RD EN CLR F	63	64	ID-2
FUNCT	65	66	OBFULL
ID-3	67	68	ID-4
LOCK	69	70	ID-5
INHEDIT	71	72	ID-6
	73	74	ID-7
SEG MODE	75	76	ID-8
	77	78	TA
MC	79	80	IDR
+9V	81	82	XMIT
-12V	83	84	-5V
GND	85	86	CHASSIS GND

P6
I/O

+5V	1	2	+5V
	3	4	
	5	6	
	7	8	
	9	10	
	11	12	
	13	14	
	15	16	
	17	18	
	19	20	
	21	22	
	23	24	
	25	26	
	27	28	
	29	30	
	31	32	
	33	34	
	35	36	
	37	38	
	39	40	
	41	42	
	43	44	
	45	46	
	47	48	
	49	50	
	51	52	
	53	54	
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	
	65	66	
	67	68	
	69	70	
	71	72	
	73	74	
	75	76	
	77	78	
	79	80	
	81	82	
	83	84	
GND	85	86	GND

P7

+5V	1	2	+5V
ADR-0	3	4	OD-1
ADR-1	5	6	OD-2
ADR-4	7	8	OD-3
ADR-5	9	10	
	11	12	
ADR-2	13	14	OD-4
ADR-3	15	16	OD-5
	17	18	EIA IN
	19	20	
	21	22	
	23	24	
	25	26	OD-6
	27	28	OD-7
	29	30	TLL OUT
PRT BUSY	31	32	OA
	33	34	
	35	36	ODR
	37	38	
EIA OUT	39	40	
	41	42	OSC
	43	44	1
	45	46	2
	47	48	3
	49	50	4
	51	52	5
	53	54	6
	55	56	7
	57	58	
ID-1	59	60	
	61	62	
ID-2	63	64	TTL-IN
ID-3	65	66	
ID-4	67	68	
ID-5	69	70	
ID-6	71	72	
ID-7	73	74	
SEG MODE	75	76	
TA	77	78	
IDR	79	80	MC
XMIT	81	82	
-12V	83	84	-5V
GND	85	86	CHASSIS GND

P8

+5V	1	2	+5V
	3	4	
	5	6	
	7	8	
	9	10	
	11	12	
	13	14	
	15	16	
	17	18	
	19	20	
	21	22	
	23	24	
	25	26	
	27	28	
	29	30	
	31	32	
	33	34	
	35	36	
	37	38	
	39	40	
	41	42	
	43	44	
	45	46	
	47	48	
	49	50	
	51	52	
	53	54	
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	
	65	66	
	67	68	
	69	70	
	71	72	
	73	74	
	75	76	
	77	78	
	79	80	
	81	82	
	83	84	
GND	85	86	GND

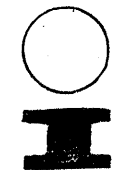
P9

+5V	1	2	+5V
	3	4	
CSRCMPR	5	6	
CAV+I	7	8	
CLRCAH	9	10	CLRCAV
PRTCODE	11	12	
	13	14	CAH+I
	15	16	CAH-I
	17	18	
	19	20	
	21	22	
	23	24	
	25	26	
	27	28	
	29	30	
LST CHAR	31	32	PRT BUSY
	33	34	
PM CLK	35	36	
	37	38	LST LINE
EOM	39	40	HLO
	41	42	
	43	44	
	45	46	PMO1
	47	48	PMO2
	49	50	PMO3
	51	52	PMO4
	53	54	PMO5
	55	56	PMO6
	57	58	PMO7
	59	60	PMO8
	61	62	PROTECT
	63	64	
	65	66	
	67	68	
	69	70	
	71	72	
	73	74	
SEG MODE	75	76	
	77	78	
MC	79	80	
	81	82	
	83	84	
GND	85	86	CHASSIS GND

P10
PRINTER

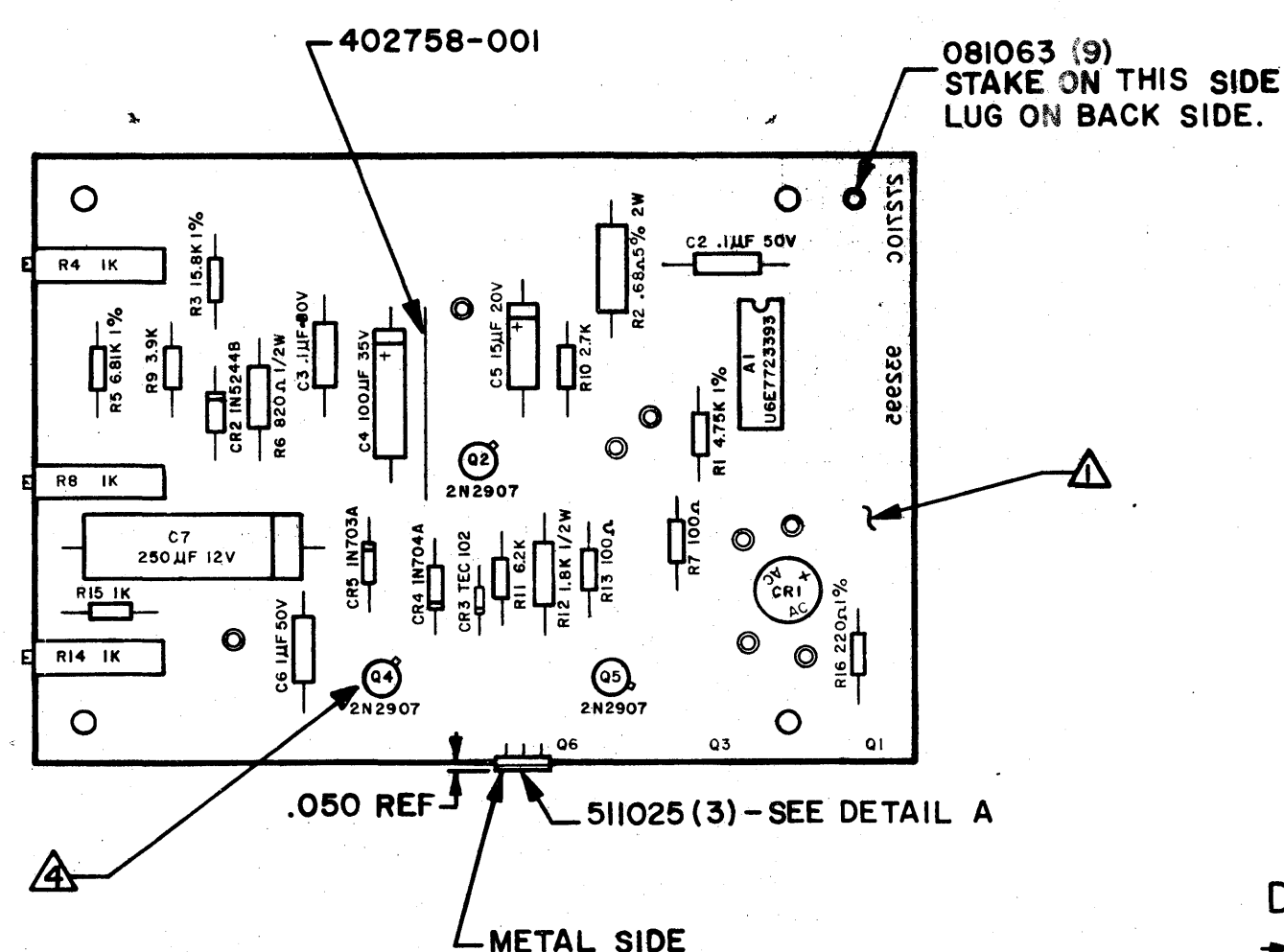
SPARE

SHT 2 OF 2

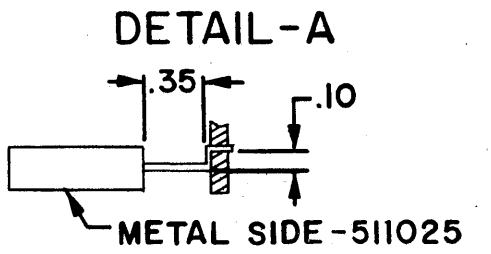
930074			TITLE CARD CAGE CONNECTIONS 400 SERIES SIZE DRAWING NO. REV D 03-312808 E
FINISH	MATERIAL		

932995

REVISIONS				
REV.	DESCRIPTION	DCN	APP'D	DATE
A	RELEASED		<i>JAL</i>	11/1/70
A ₁	REV PER DCN	6795	<i>JAL</i>	11/24/70
A ₂	REV PER DCN	6792	<i>JAL</i>	11/24/70
A ₃	CHG. 511025-001 TO-000 & ADD FORMING DIM. TO DWG.	7297	<i>JAL</i>	3/10/71
A ₄	CHG. C5 FROM 631022 TO 621037	7340	<i>JAL</i>	3/25/71
B	CHG. R2 681023 TO 701058-005. ADDED R16.	7345	<i>JAL</i>	6/10/71
C	REV LEVEL CHG ONLY	8184	<i>gww</i>	20/NOV/72
C ₁	REV PER DCN	8431	<i>gww</i>	21 NOV 72
D	REV PER DCN	8260	<i>gww</i>	22 NOV 72



- NOTES:
1. ASSY NO., DASH NO., AND REF. TO BE RUBBER STAMPED ON BOARD AT ASSY.
 2. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARA. 4.3.2 OF TEC WORKMANSHIP MANUAL.
 3. .050 MAX. SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD.
 4. ALL TRANSISTOR CANS TO HAVE SPACERS UNDERNEATH.



982845	SERIES 400	
MATERIAL		
FINISH		

PARTS LIST ISSUED

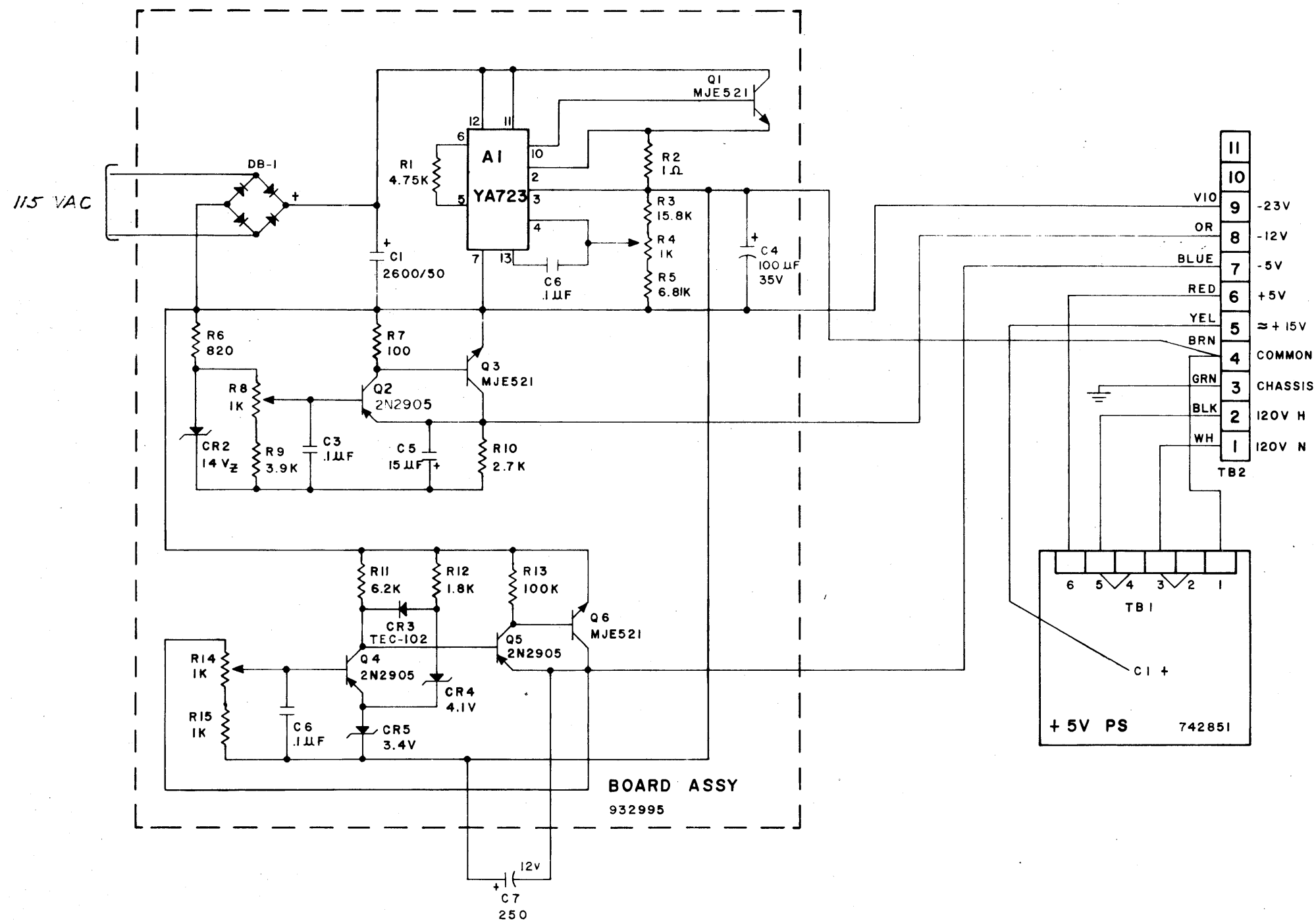
SAT 10F1

P.W. ASSY-POWER SUPPLY

72	DR/WING NO.	
72	02-312 B08	E
	5	39

992845

REV	DESCRIPTION	DCN	APPD	DATE
A	RELEASED			
B	NO CHG - SEE DCN	818		
C	NO CHG - SEE DCN	8184		
D	NO CHG - SEE DCN	36		
E	REV PER DCN	8525		



932995	SERIES 400
DRAWING NO.	
DATE	



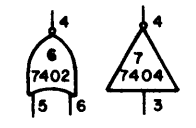
SHT 10E1
SCHEMATIC-
POWER SUPPLY
SERIES 400 CRT
II-10-70
D 02-312 B08 E
6 39

A	RELEASED		
B	REV PER DCN		8622

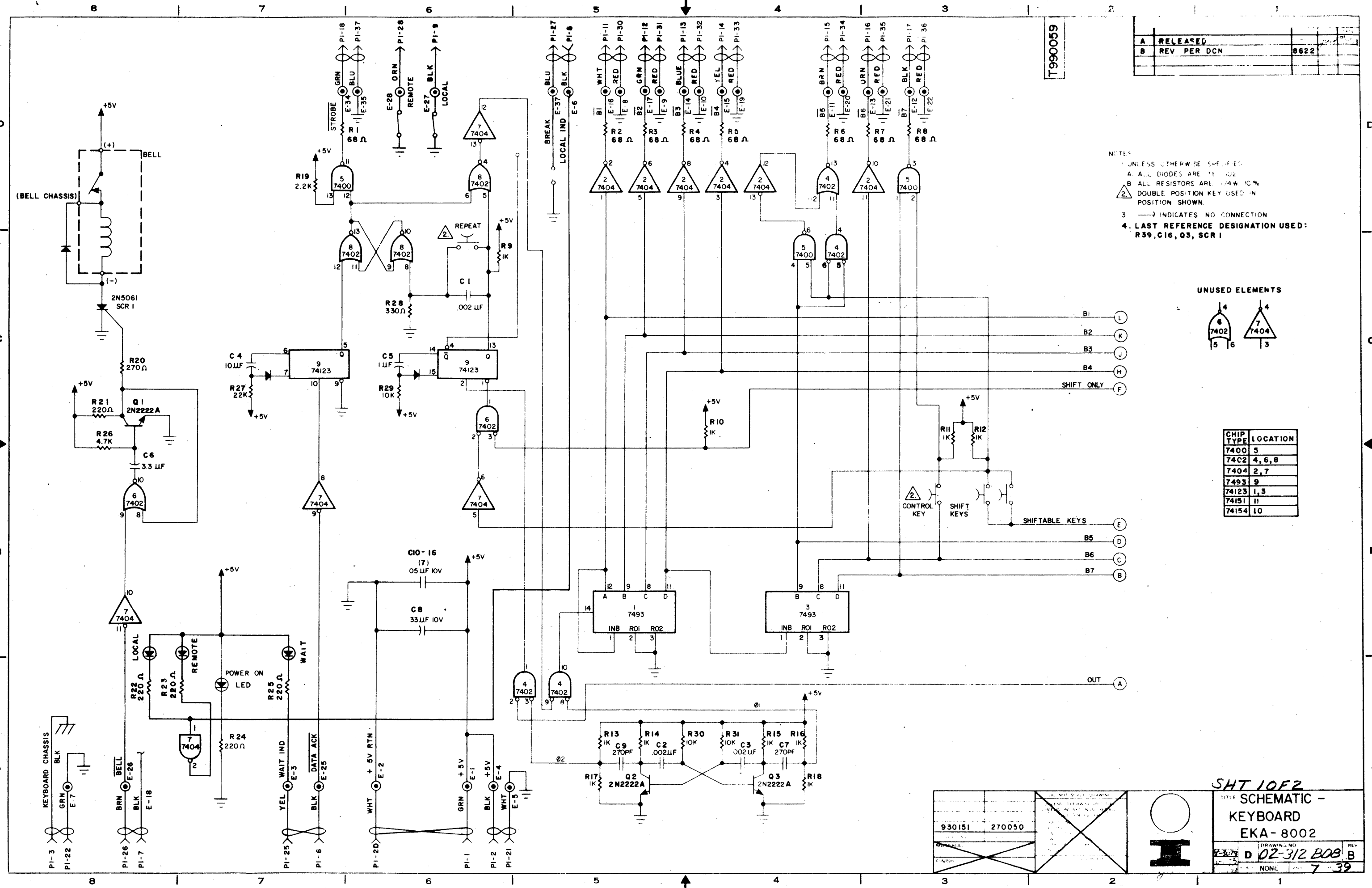
T990059

- NOTES:
- UNLESS OTHERWISE SPECIFIED:
 - ALL DIODES ARE 1N4002
 - ALL RESISTORS ARE 1/4W 10%
 - DOUBLE POSITION KEY USED IN POSITION SHOWN
 - INDICATES NO CONNECTION
 - LAST REFERENCE DESIGNATION USED: R39, C16, Q3, SCR 1

UNUSED ELEMENTS



CHIP TYPE	LOCATION
7400	5
7402	4, 6, 8
7404	2, 7
7493	9
74123	1, 3
74151	11
74154	10



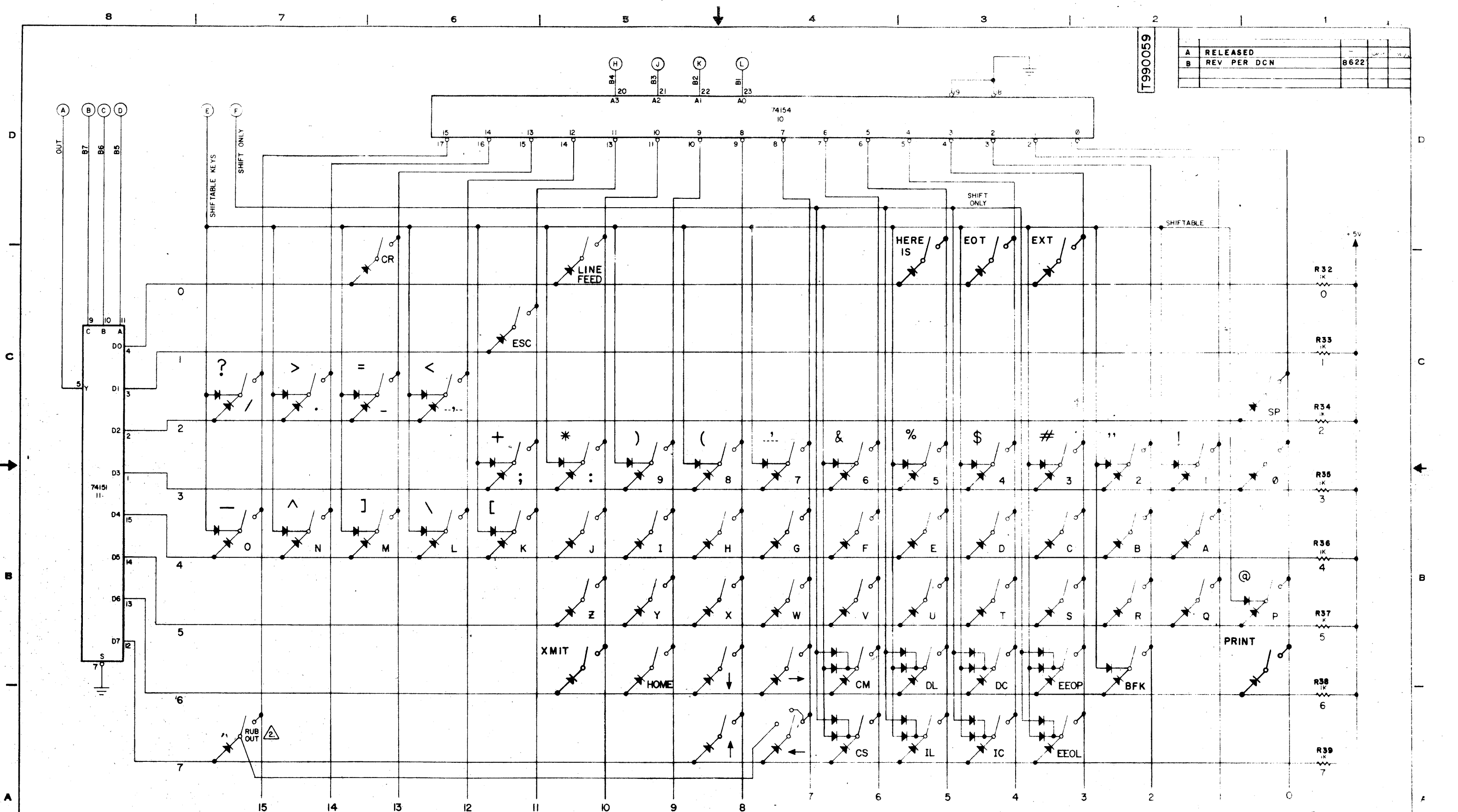
SHT 10F2

TITLE SCHEMATIC -
KEYBOARD
EKA-8002

930151	270050
DRAWING NO. D 02-312 BOB B	
NONE 7 39	

A	RELEASED		
B	REV PER DCN	6622	

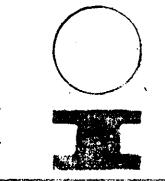
T990059



SHT 2 OF 2

SCHEMATIC-
KEYBOARD, TTY
EKA-8002

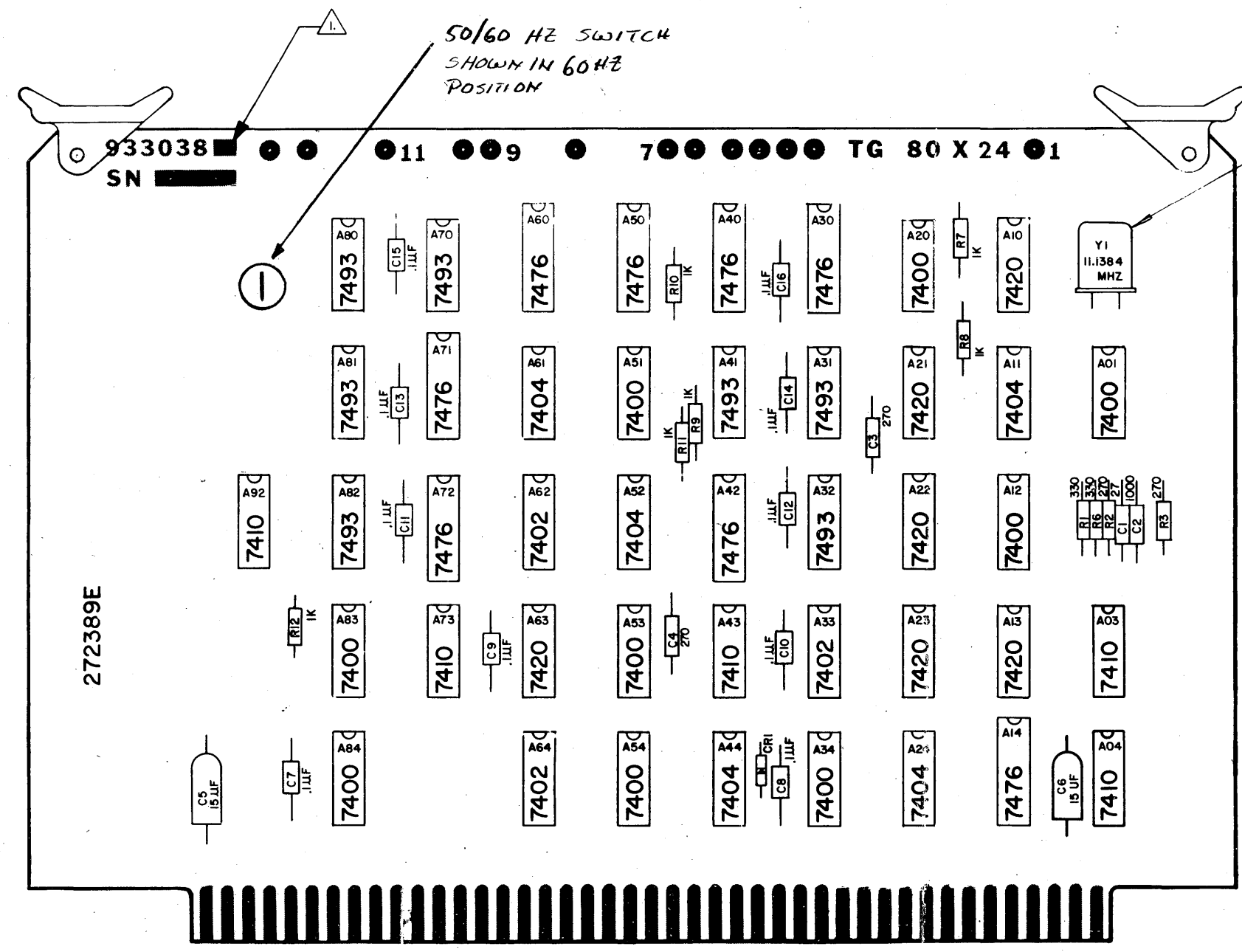
930151	270050
DATE	REV
DESIGNED BY	CHECKED BY
DRAWN BY	APPROVED BY



02-312 B08 B
6-39

933038

A	RELEASED		
B	REV PER DCN	7357	
C	REV PER DCN	7042	
D	REV PER DCN	9077	
E	REV PER DCN	8539	



- NOTES:
1. APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY.
 2. INSERT GRIPLETS IN HOLES WITH SQUARE LAND AREA BEFORE COMPONENT INSERTION.
 3. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARAGRAPH 4.3.2 OF TEC WORKMANSHIP MANUAL.
 4. .050 MAX SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD.
 5. CEMENT CRYSTAL TO BOARD USING S-254 RESIWELD.

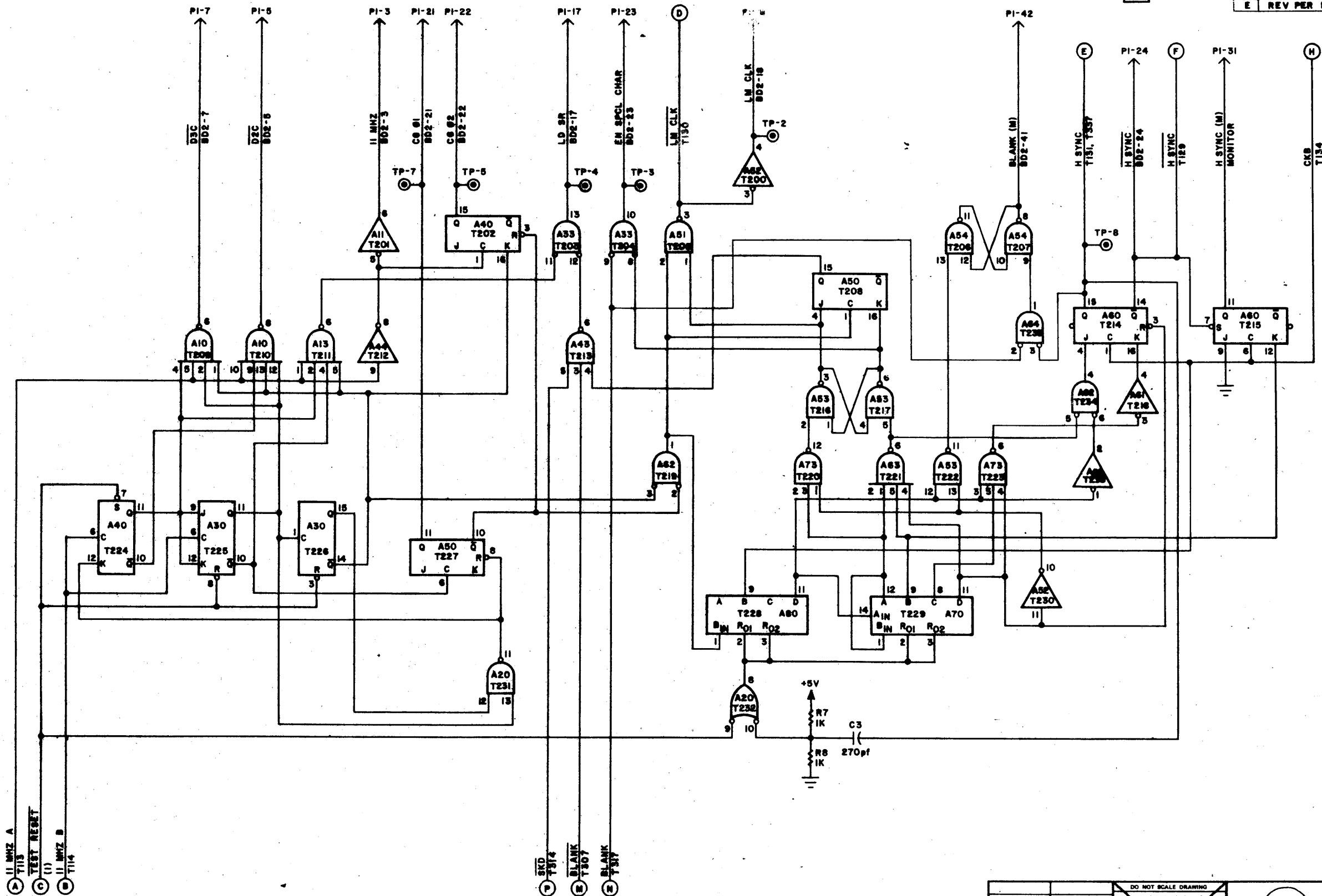
PARTS LIST

SHT 1 OF 1

DSF-8024 DST-8024			P.W. ASSY - TIMING GEN 80 X 24
			4-1-71 02-312 BOSE
			9-39

REVISIONS				
REV.	DESCRIPTION	DCN	APPD	DATE
A	RELEASED			
B	REV PER DCN	7887		6-4-7
C	REV PER DCN	7042		1-4-7
D	REV PER DCN	9077		2-2-7
E	REV PER DCN	8839		5-2-7

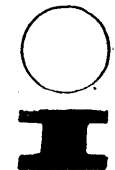
991937



SHT 20F3

TITLE SCHEMATIC -
TIMING GENERATOR
80 x 24

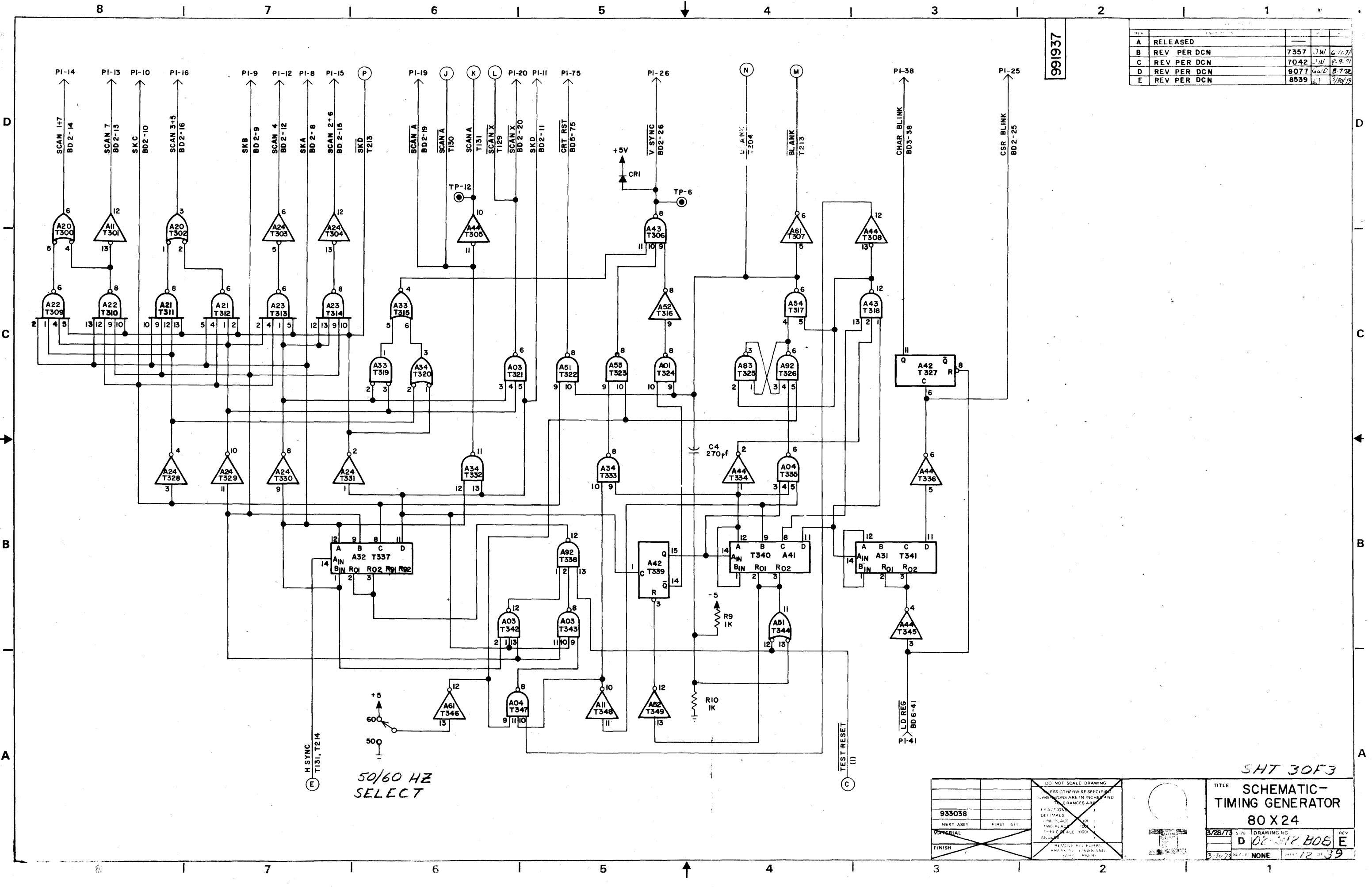
DO NOT SCALE DRAWING	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE:	
FRACTIONS	± .01
DECIMALS	(0) ± .01
TWO PLACE	± .005
THREE PLACE	± .0005
ANGLE	± .01
REMOVE ALL BURRS BREAK ALL EDGES AND SHARP CORNERS	



933038	SIZE	DRAWING NO.	REV
NEXT ASBY	FIRST USED	D 02-312B08 E	
FINISH	SCALE	NONE	SHEET 11 OF 39

REV				
A	RELEASED			
B	REV PER DCN	7357	JW	6-11-71
C	REV PER DCN	7042	JW	8-9-71
D	REV PER DCN	9077	GWD	5-7-72
E	REV PER DCN	8539	BJ	3/24/72

991937

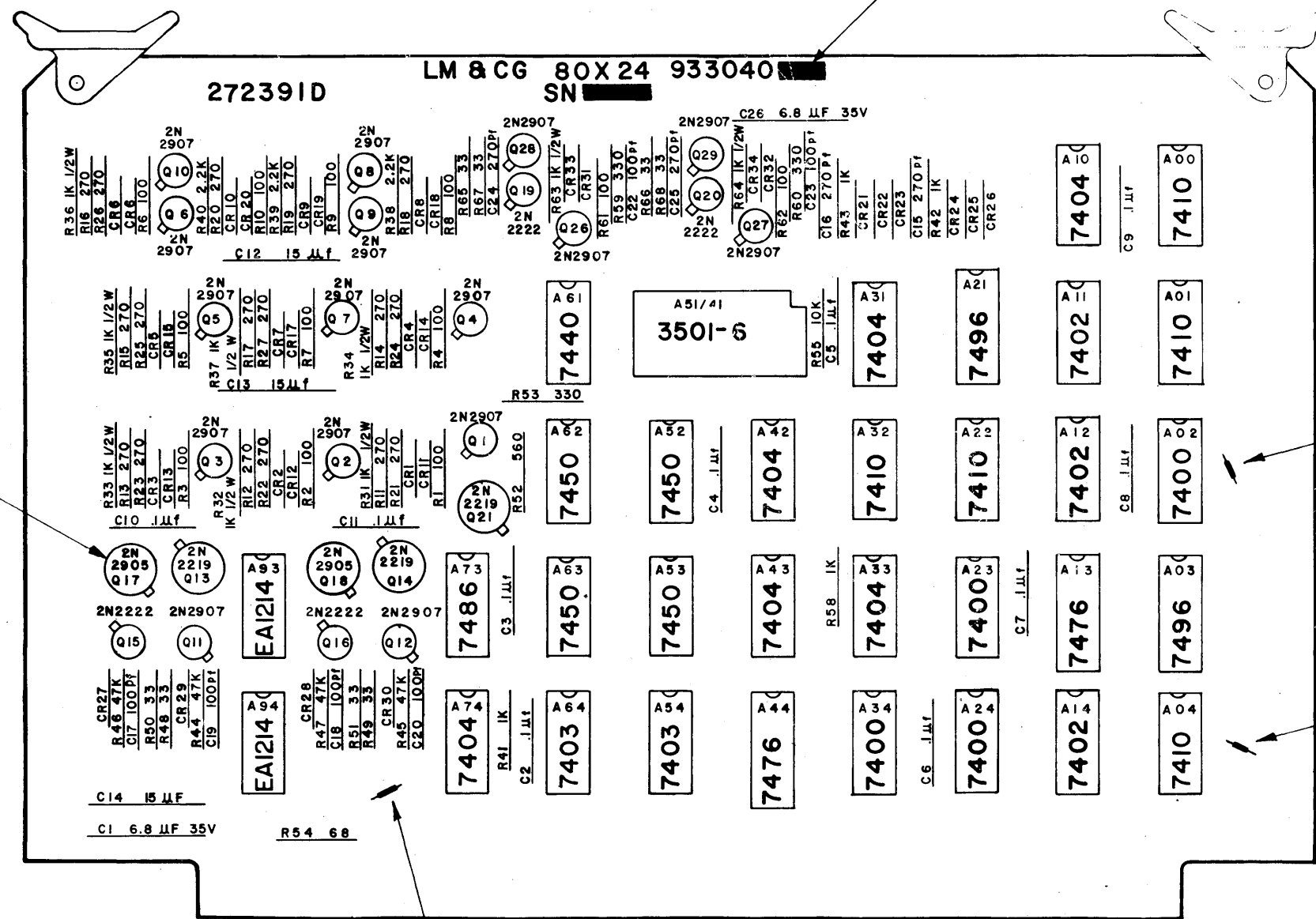


933038		DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE:	
NEXT ASSY	FIRST SET	1/4" ± 0.005	1/16" ± 0.002
MATERIAL		0.015" ± 0.001	0.005" ± 0.0005
FINISH		REMOVE ALL FLARE FROM ALL FITS AND SAFETY MARK	

TITLE	SHT 30F3 SCHEMATIC-TIMING GENERATOR 80 X 24		
DATE	3/28/73	SIZE	DRAWING NO.
	D		02-512 B06 E
SCALE	NONE	SHEET	12 OF 39

933040

D	REV 8 REDRAWN	5882	AM
E	REV PER DCN	8168	End 1/71
F	REV PER DCN	8260	1/71
G	REV PER DCN	8277	2/71
H	REV PER DCN	8401	1/72



272391D LM & CG BOX 24 933040 SN

- NOTES:
1. APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY.
 2. INSERT GRIPLETS IN HOLES WITH SQUARE LAND AREA BEFORE COMPONENT INSERTION.
 3. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARAGRAPH 4.3.2 OF TEC WORKMANSHIP MANUAL.
 4. .050 MAX SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD.
 5. ALL TRANSISTOR CANS TO HAVE SPACERS UNDERNEATH.

DISPLAY 6R (←) JUMPER
402001-025

DISPLAY CURSOR
402001-025

WHITE ON BLACK (NORMAL VIDEO)
JUMPER 402001-025

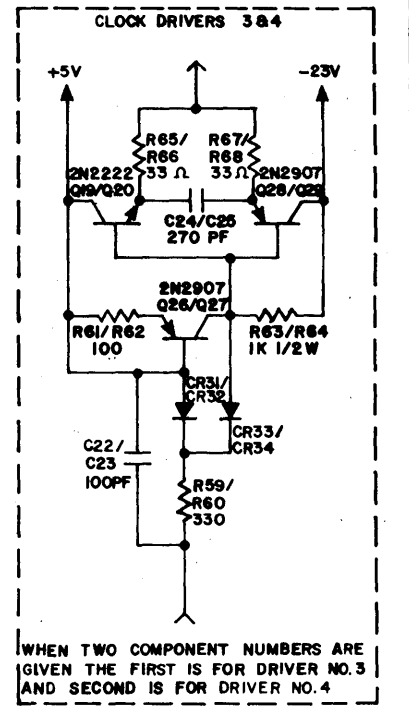
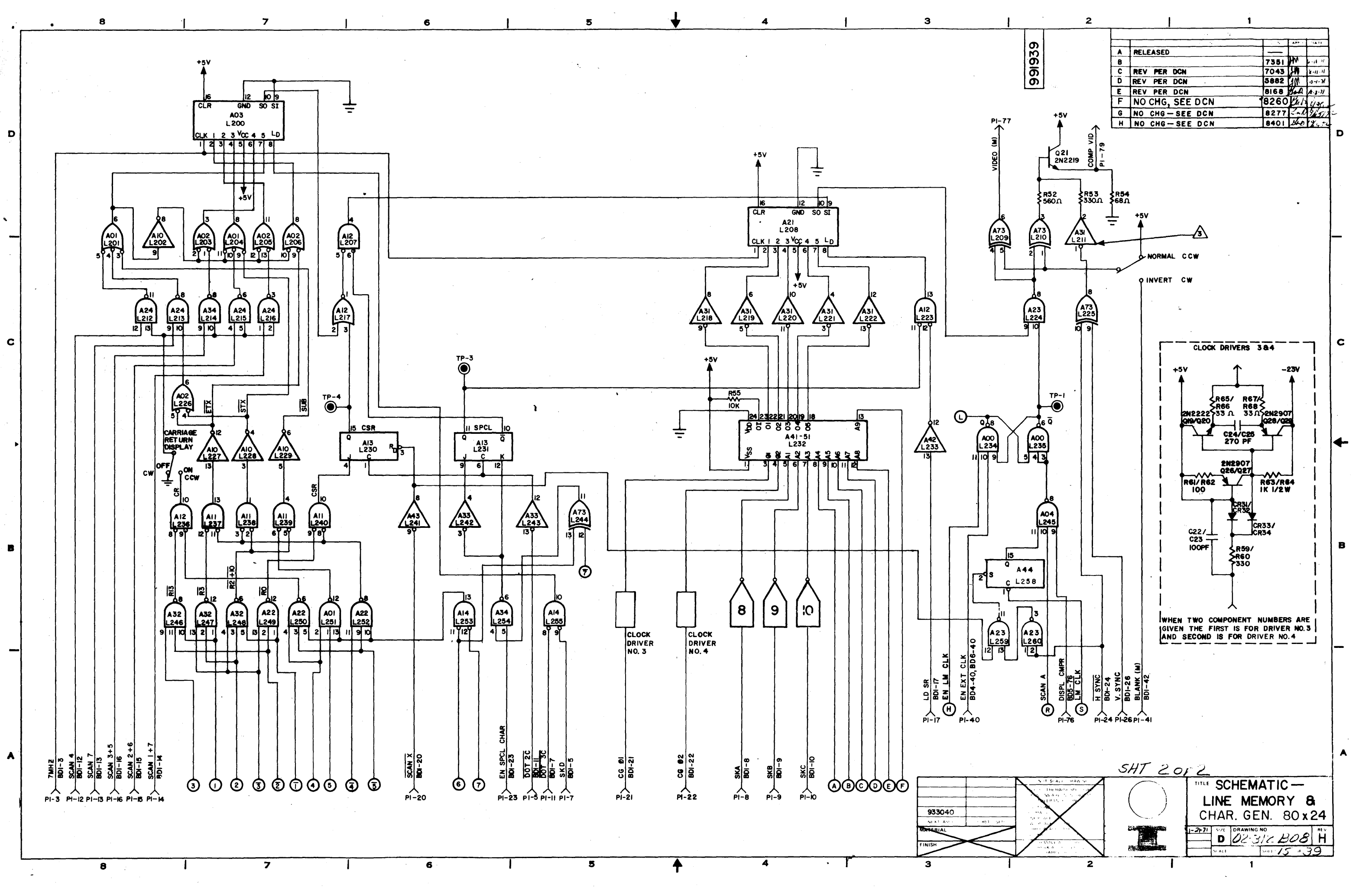
PARTS LIST ISSUED

SHT 10F1

DSP-8024 DST-8024			PW ASS LINE MEMORY & CHAR. GEN. BOX24
			02-312 B08 H
			2/1 13-39

REV	DATE	BY	CHKD
A	RELEASED		
B		7381	
C	REV PER DCN	7043	
D	REV PER DCN	5882	
E	REV PER DCN	8168	
F	NO CHG, SEE DCN	8260	
G	NO CHG - SEE DCN	8277	
H	NO CHG - SEE DCN	8401	

991939

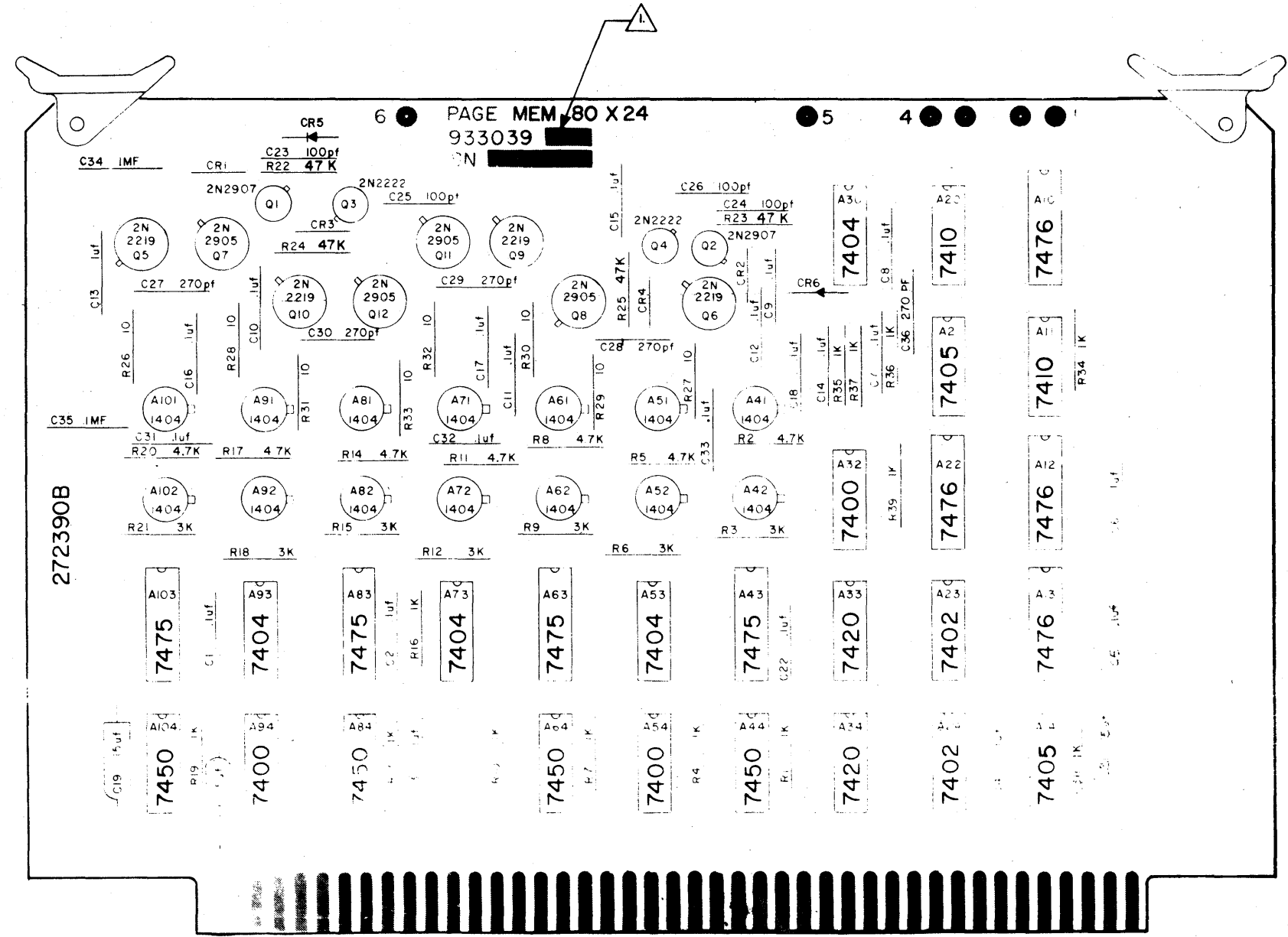


933040	
DATE	REV
MATERIAL	
FINISH	

TITLE		SHT 2012	
SCHEMATIC -			
LINE MEMORY &			
CHAR. GEN. 80x24			
REV	DATE	DRAWING NO	REV
1-271		D 02-31-68 B08	H
DATE	DATE	DATE	DATE
		15	39

933039

A	RELEASED		
B	REV LEVEL CHG ONLY	8184	7-13-77
C	CHG R22-25 FROM 10K TO 47K	8163	11-15-77
D	REV PER DCN	8246	



- NOTES
1. APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY.
 2. INSERT GRIPLETS IN HOLES WITH SQUARE LAND AREA BEFORE COMPONENT INSERTION.
 3. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARAGRAPH 4.3.2 OF TEC WORKMANSHIP MANUAL.
 4. .050 MAX SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD.

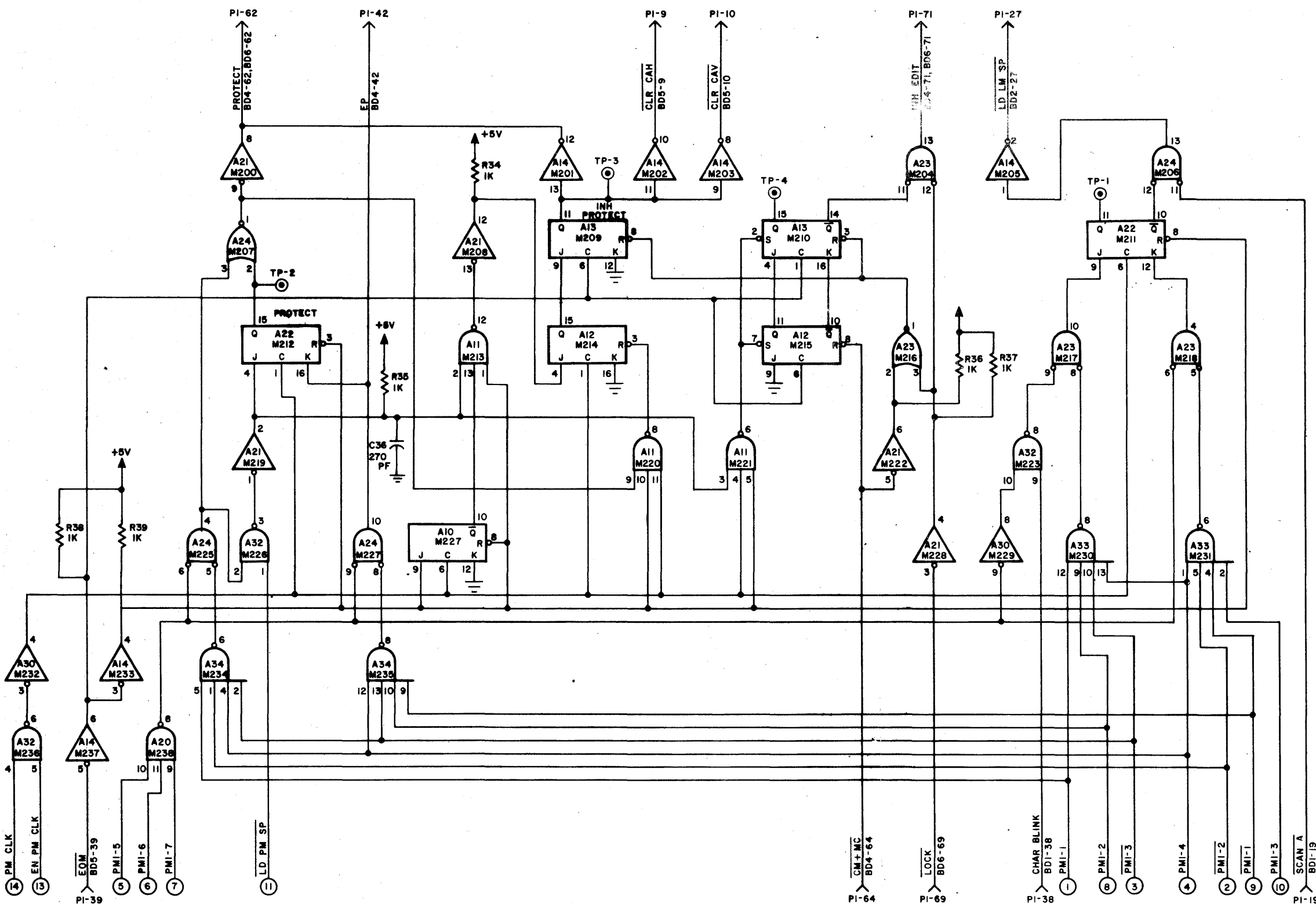
PARTS LIST ISSUED

SHT 10/1

	P.W. ASSY- PAGE MEMORY 80x24	
	D	02-312 B08 D
	2/1	16-39

991938

REV.	RELEASED	DATE
A	RELEASED	
B	SEE DCN 7346 & 7701	
C	NO CHG THIS SHT	8163
D	REV PER DCN	8246



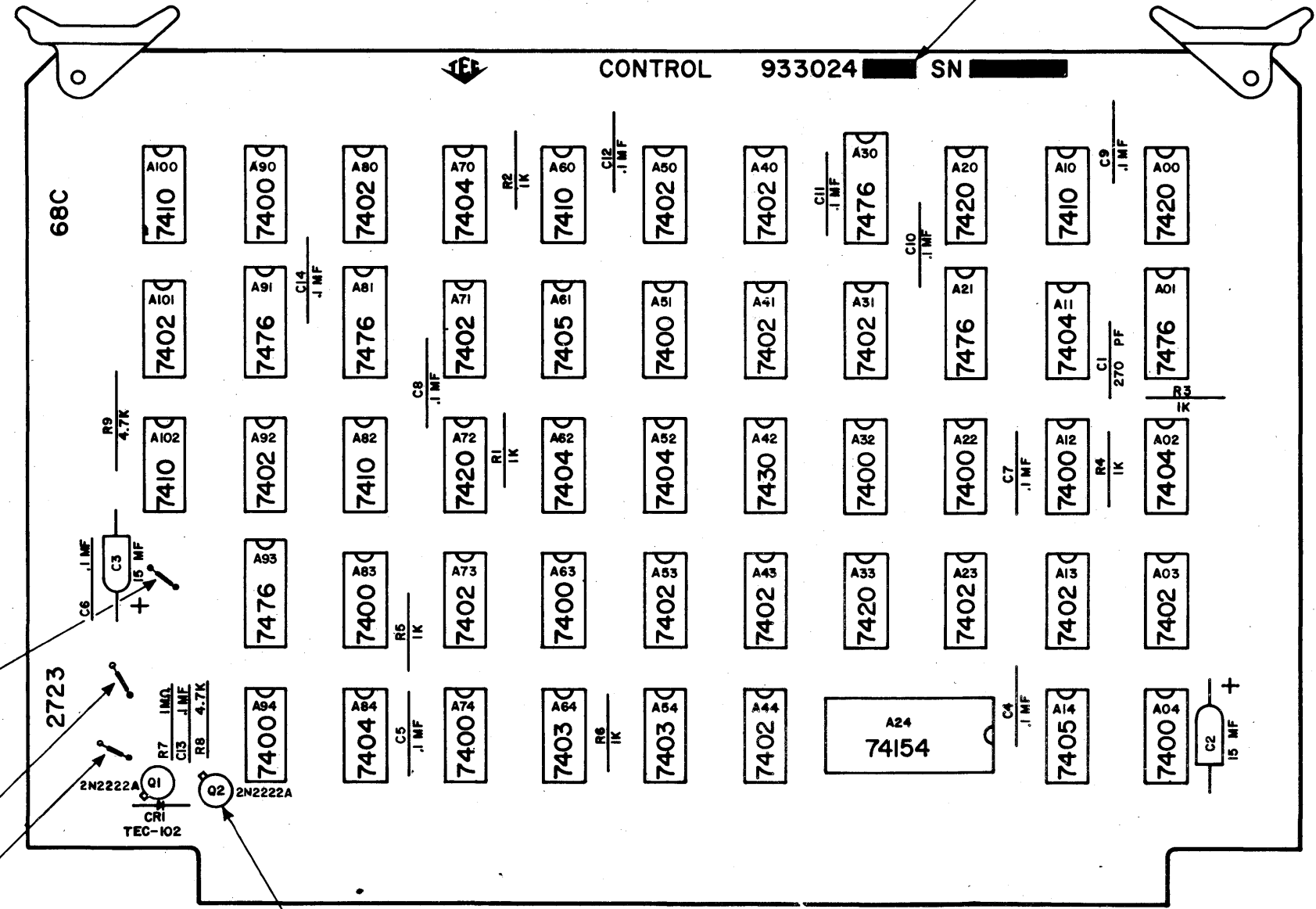
SHT 2 OF 2

933039	TITLE	SCHEMATIC - PAGE MEMORY	
		80x24	
SIZE	D	DRAWING NO.	02-312 B08 D
SCALE	NONE	SHEET	18 OF 39

T-933024

REVISIONS			
REV.	DESCRIPTION	DCN	APPO DATE
E	REV PER DCN	8299	GENCO 27 MAR 73
F	REV PER DCN	8535	GENCO 27 APR 73

CONTROL 933024 SN



- NOTES:
1. APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY.
 2. INSERT GRIPLETS IN HOLES WITH SQUARE LAND AREA BEFORE COMPONENT INSERTION.
 3. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARAGRAPH 4.3.2 OF TEC WORKMANSHIP MANUAL.
 4. .050 MAX SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD.
 5. ALL TRANSISTOR CANS TO HAVE SPACERS UNDERNEATH.

INHIBITS LOAD OF VT CODE JUMPER 402001-025

AUTO LINE FEED JUMPER 402001-025

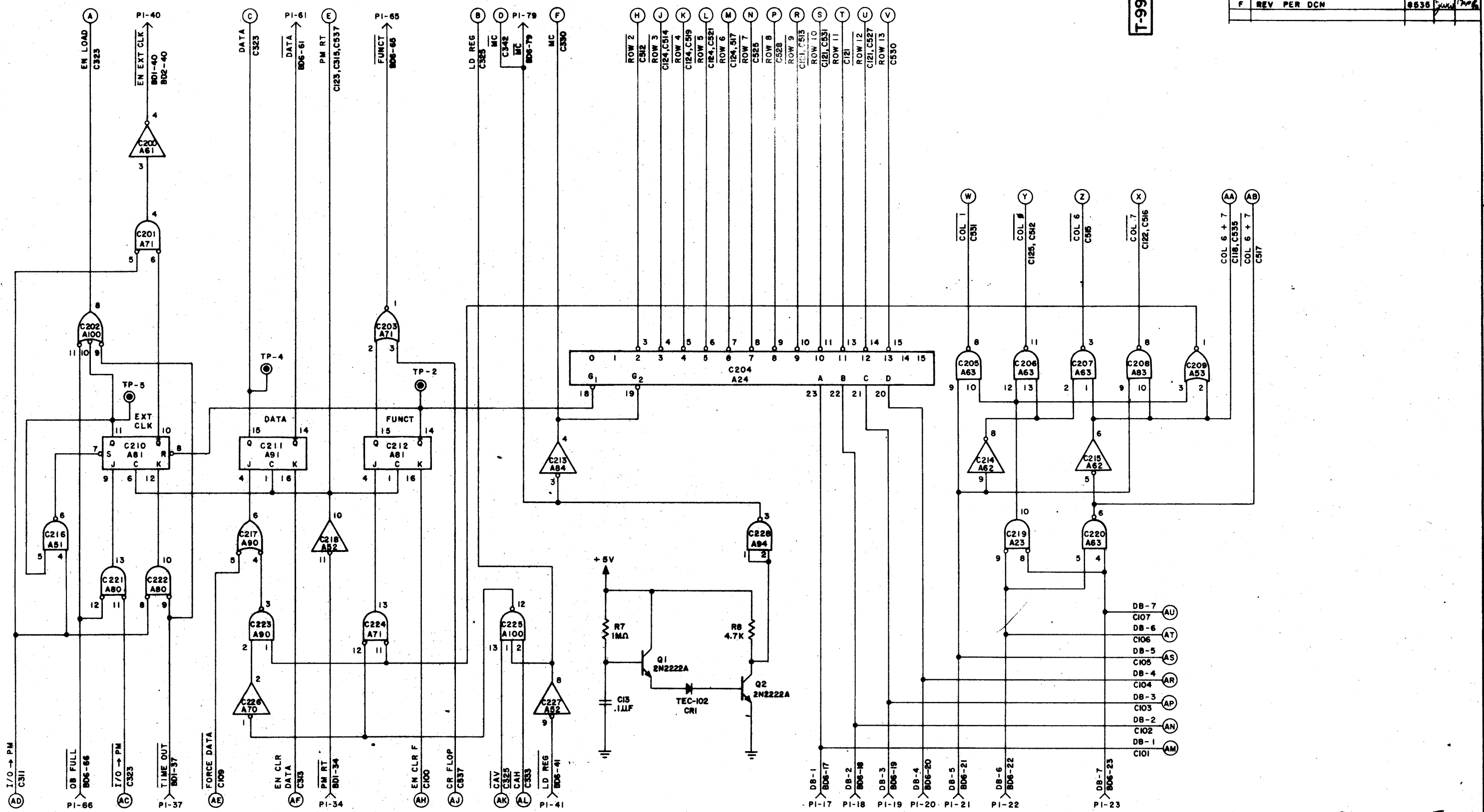
INHIBITS AUTO ROLL UP JUMPER 402001-025

PARTS LIST ISSUED

NEXT ASSY		FIRST USED	
TITLE		SHT 10F1	
P.C.B. ASSY—		CONTROL	
SIZE	DRAWING NO.	REV	
D	02-312 BOB	F	
SCALE	SHEET		OF
2/1	19		39

T-991924

REVISIONS				
REV	DESCRIPTION	DCN	APPO	DATE
E	REV PER DCN	0299		
F	REV PER DCN	0535		

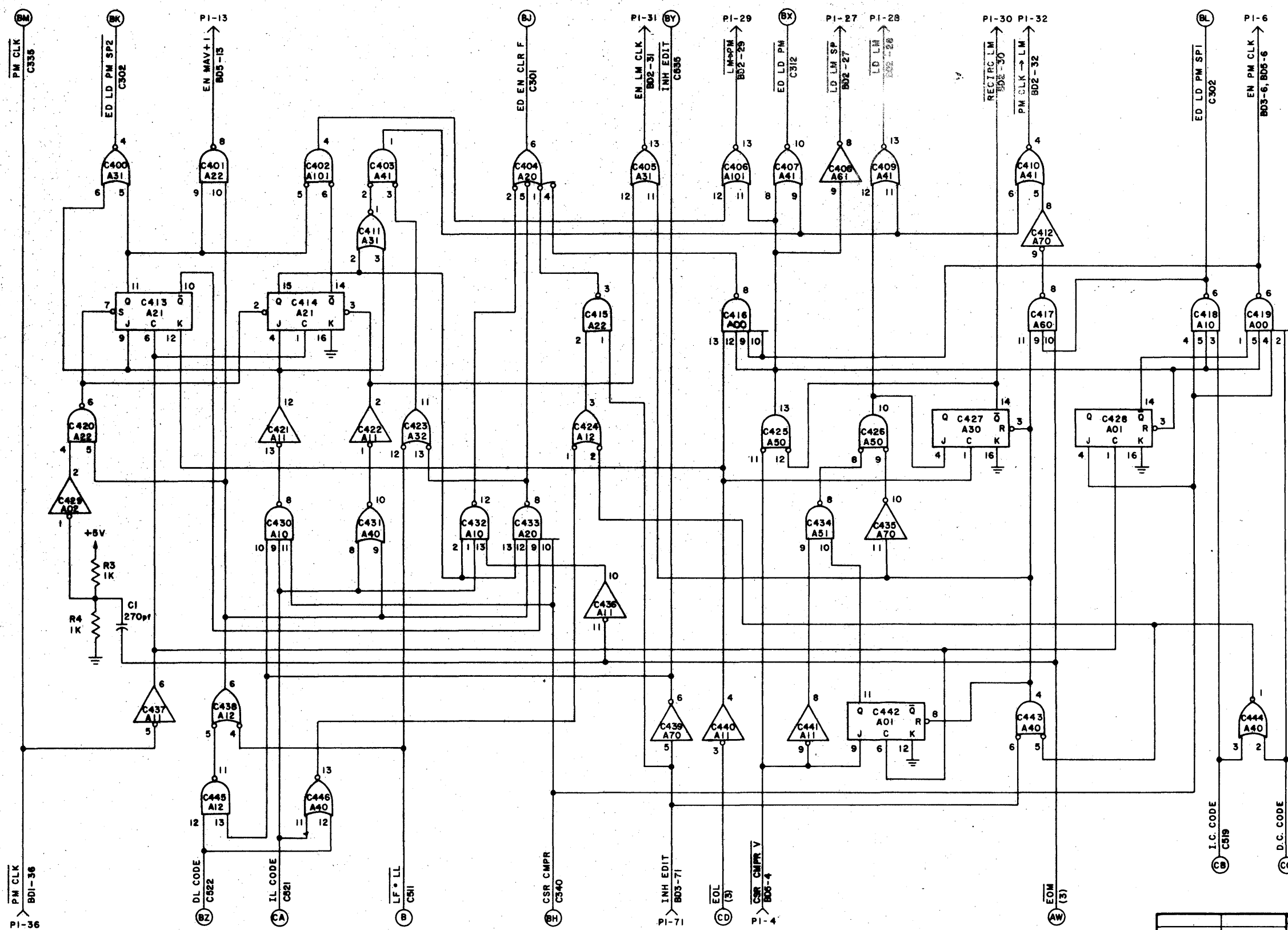


SHT 2 OF 5

933024		NEXT ASSY		FIRST USED	
TITLE: SCHEMATIC-CONTROL					
SIZE: D		DRAWING NO: 02-312 B08 F		SCALE: NONE	
SHEET: 21		OF 39			

REVISIONS			
REV	DESCRIPTION	DCN	APPD DATE
E	REV PER DCN	8299	11/11/72
F	REV PER DCN	8535	1/11/73

T-991924

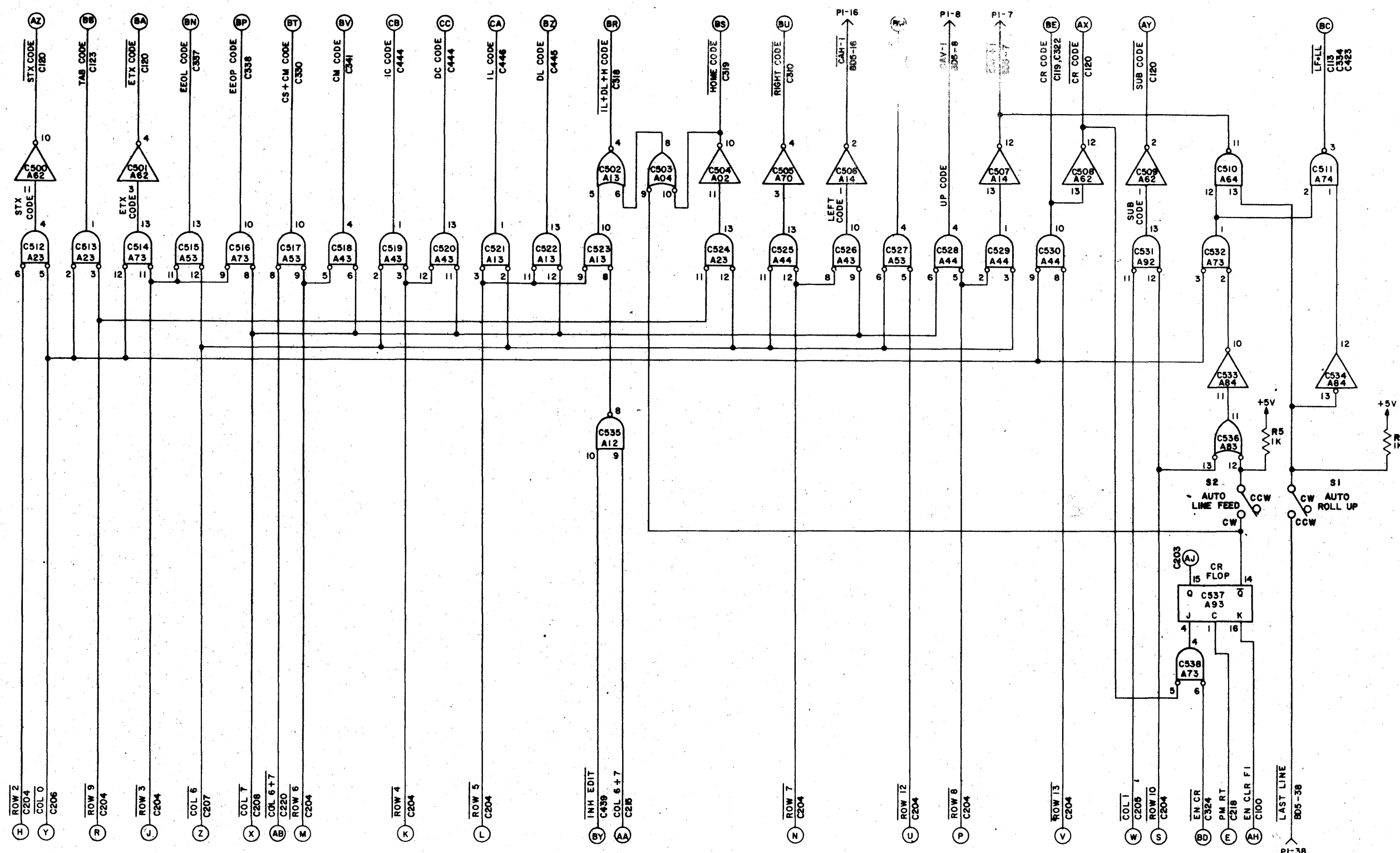


SHT 40F5

933024		 <small>DO NOT SCALE DRAWING</small> <small>USE DIMENSIONS UNLESS OTHERWISE SPECIFIED</small> <small>FRACTIONS SHALL BE IN 16ths</small> <small>ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED</small>	TITLE	
NEXT ASSY	FIRST USED		SCHEMATIC - CONTROL	
FINISH		1-16-72	SIZE	REV
		D	02-312 B08F	
		SCALE	NONE	SHEET 23 OF 39

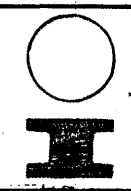
T-991924

REVISIONS				
REV	DESCRIPTION	DCN	APPD	DATE
E	REV PER DCN	8299		
F	REV PER DCN	8535		



SHT 50F5

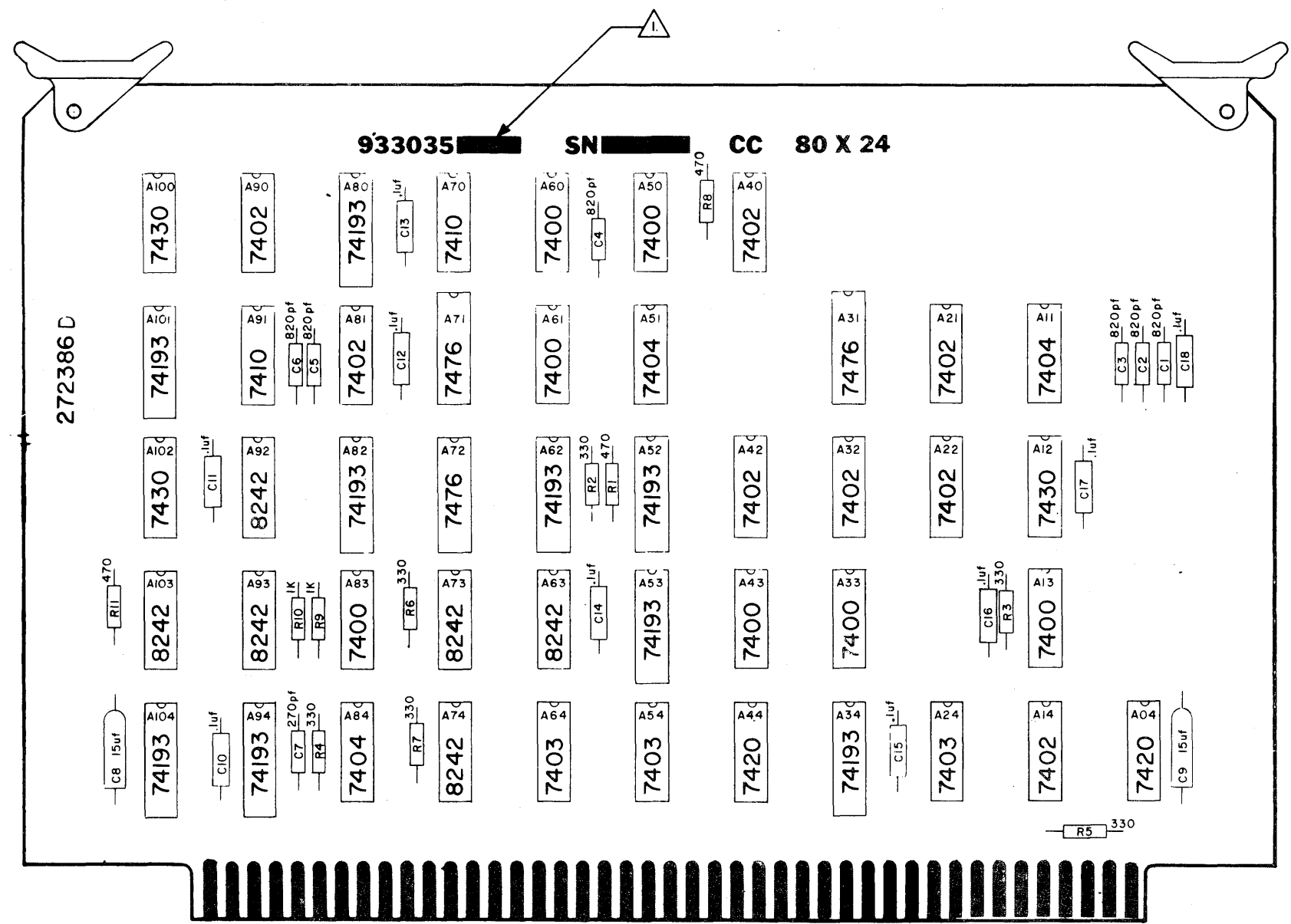
933024	
NEXT ASSY	FIRST USED



TITLE		SCHEMATIC-CONTROL	
1-16-72	SIZE	DRAWING NO.	REV
D		02-312B08 F	
SCALE NONE	SHEET 24 OF 39		

933035

REVISIONS			
NO.	DESCRIPTION	DCN	APPR. DATE
A	RELEASED		
B	REVISED PER DCN	7384	6-15-71
C	REVISED PER DCN	8456	11-1-71



- NOTES
1. APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY.
 2. INSERT GRIPLETS IN HOLES WITH SQUARE LAND AREA BEFORE COMPONENT INSERTION.
 3. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARAGRAPH 4.3.2 OF TEC WORKMANSHIP MANUAL.
 4. .050 MAX SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD.

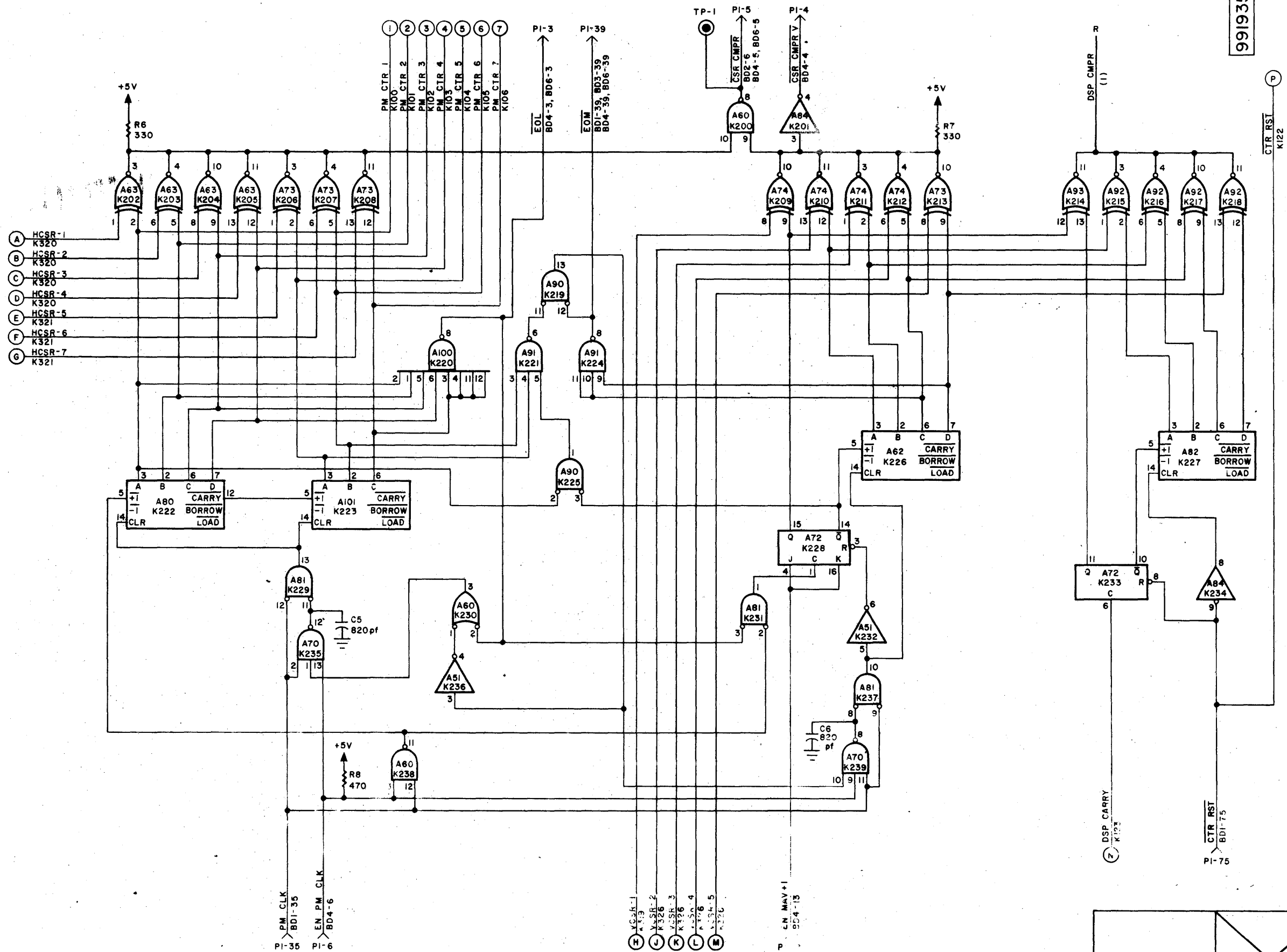
PARTS LIST ISSUED

SHT 1 OF 1

8024			TITLE P.W. ASSY-CURSOR COUNTER-80x24	
DRAWING NO. D 02 312 B08 C			DATE 2/1 1971	

991935

A	RELEASE		
B	NO CHG-BEE DCN	8184	1-1-72
C	REV PER DCN	8456	1-1-72

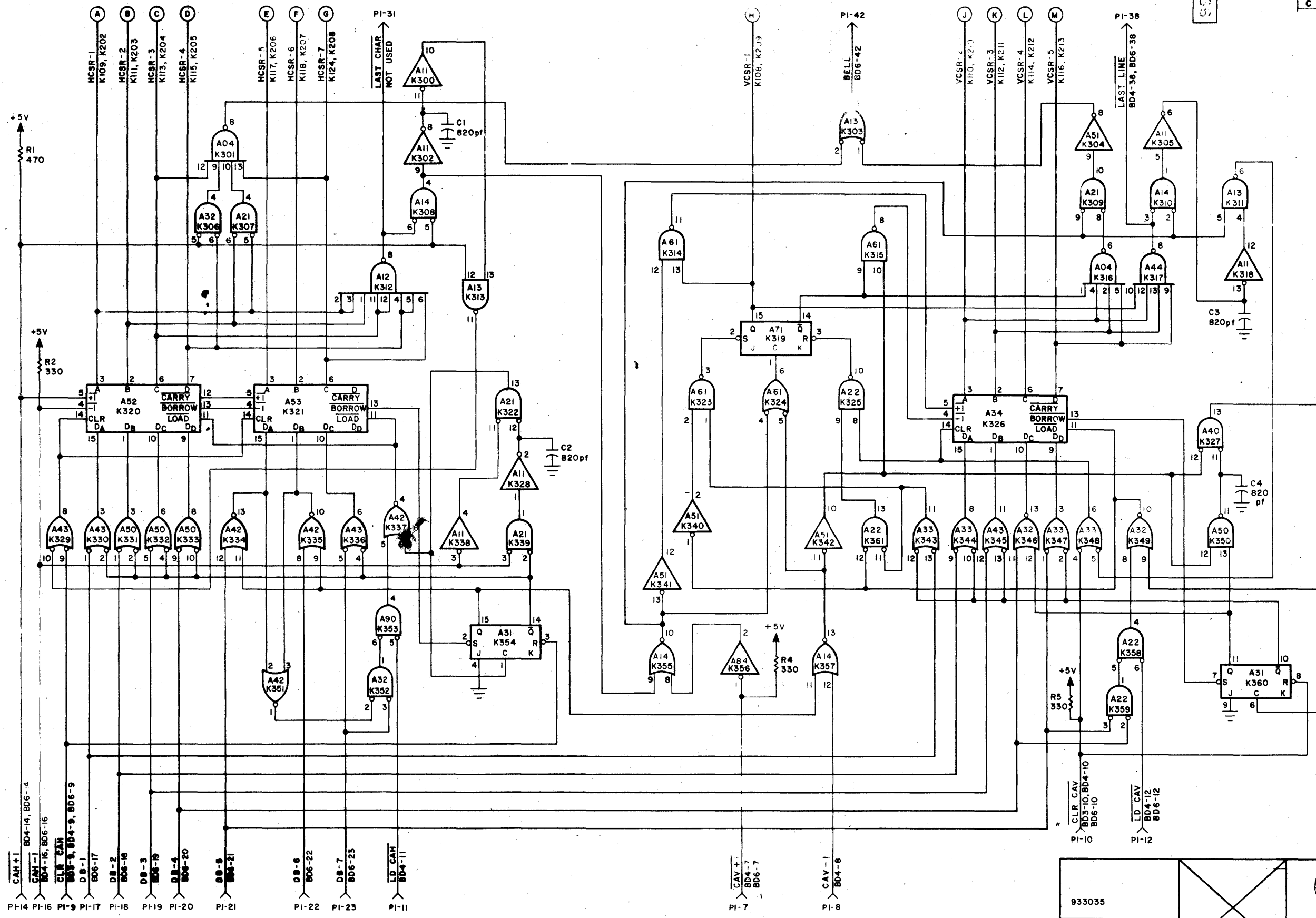


- (A) HCSR-1 K320
- (B) HCSR-2 K320
- (C) HCSR-3 K320
- (D) HCSR-4 K320
- (E) HCSR-5 K321
- (F) HCSR-6 K321
- (G) HCSR-7 K321

SHT 2 OF 3
 SCHEMATIC -
 CURSOR COUNTER
 80x24

02-312 B08C
 NONE 27-39

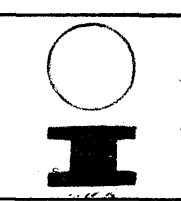
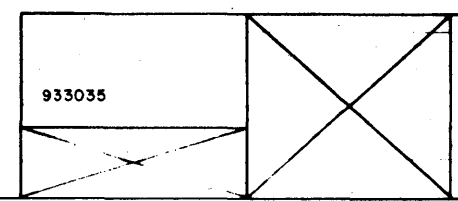
REVISIONS		DATE	BY
A	RELEASED		
B	NO CHG - SEE DCN	8104	W.D. Dyer
C	REV PER DCN	8486	W.D. Dyer



CAH+1 BD4-14, BD6-14
 CAH-1 BD4-16, BD6-16
 CLR CAV BD3-9, BD4-9, BD6-9
 DB-1 BD4-17
 DB-2 BD4-18
 DB-3 BD6-19
 DB-4 BD4-20
 DB-5 BD4-21
 DB-6 BD6-22
 DB-7 BD6-23
 LD CAV BD4-11
 PI-14 PI-16
 PI-9 PI-17
 PI-18
 PI-19
 PI-20
 PI-21
 PI-22
 PI-23
 PI-11

CAV+ BD4-7, BD6-7
 CAV- BD4-8
 PI-7
 PI-8

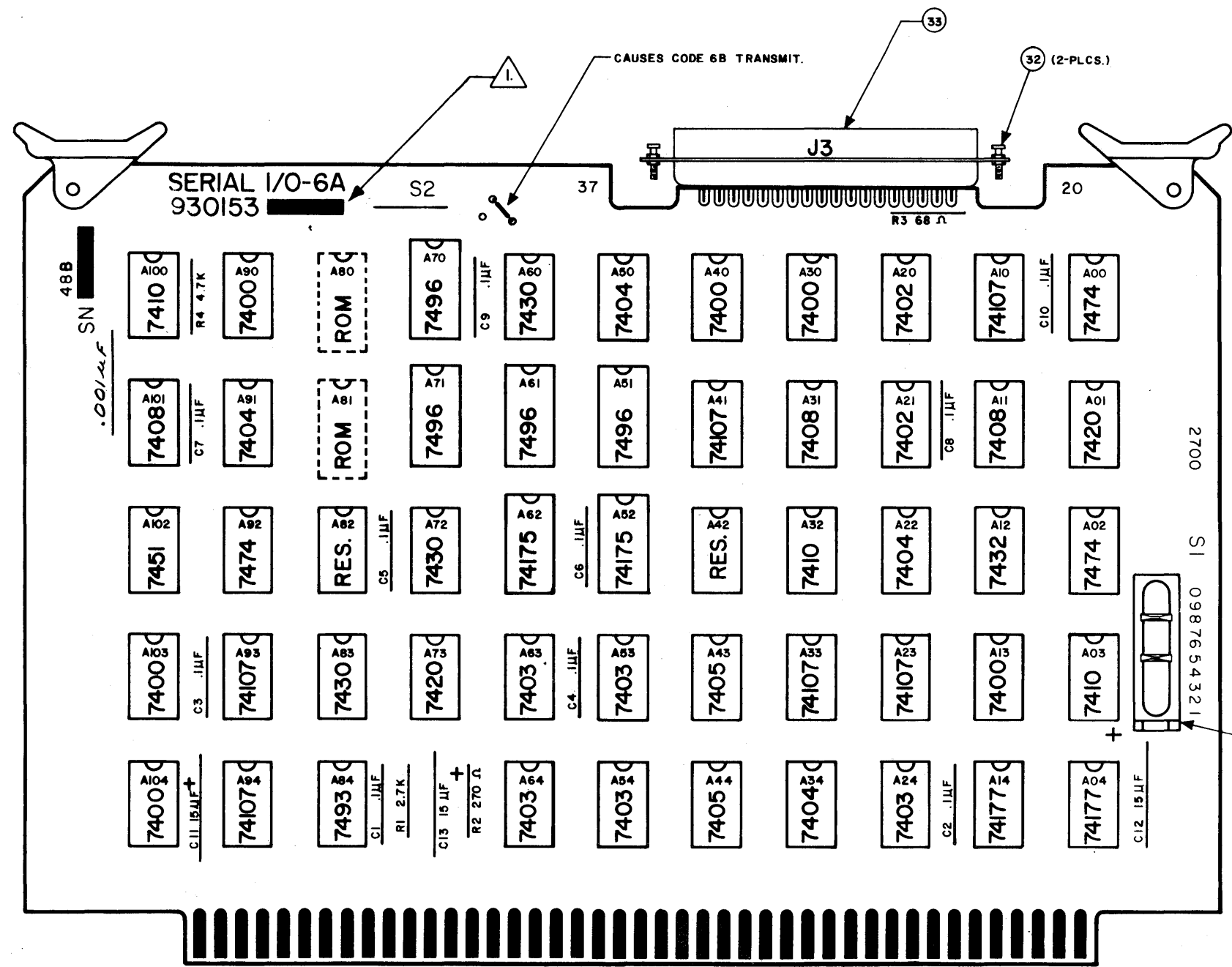
CLR CAV BD3-10, BD4-10, BD6-10
 LD CAV BD4-12, BD6-12
 PI-10
 PI-12



SHT 3013
 TITLE SCHEMATIC -
 CURSOR COUNTER
 80x24
 11-5-70
 D 02-312 B05 C
 NONE 28-39

T-930153

REV.	DESCRIPTION	BY	DATE
A	RELEASED		
B	REV PER DCM	8603	12-27-73



- NOTES:
- APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY.
 - SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER TEC WORKMANSHIP MANUAL.
 - .050 MAX SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD.
 - INTEGRATED CIRCUITS A80 AND A81 ARE CUSTOMER SPECIFIED OPTIONS.

(28)
(29) STOPS TO BE PLACED IN POSITIONS 5 AND 8.

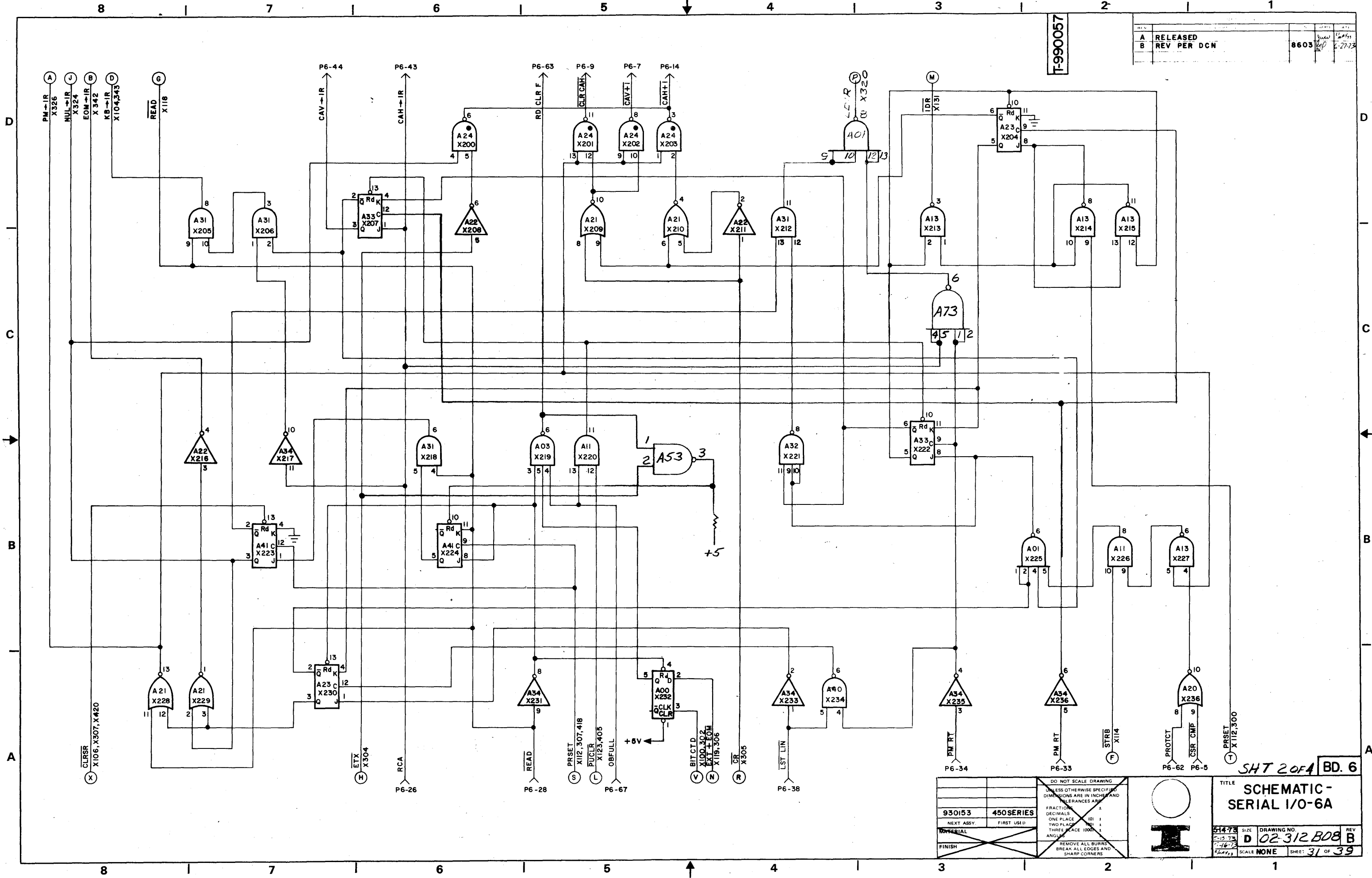
PARTS LIST ISSUED

450 SERIES			TITLE PC.B. ASSY— SERIAL I/O-6A	
NEXT ASSY	FIRST USED		SIZE D	DRAWING NO. 02-312 B08
FINISH		SCALE 2/1	SHEET 29 OF 39	

SHT 1 OF 1
TITLE
PC.B. ASSY—
SERIAL I/O-6A

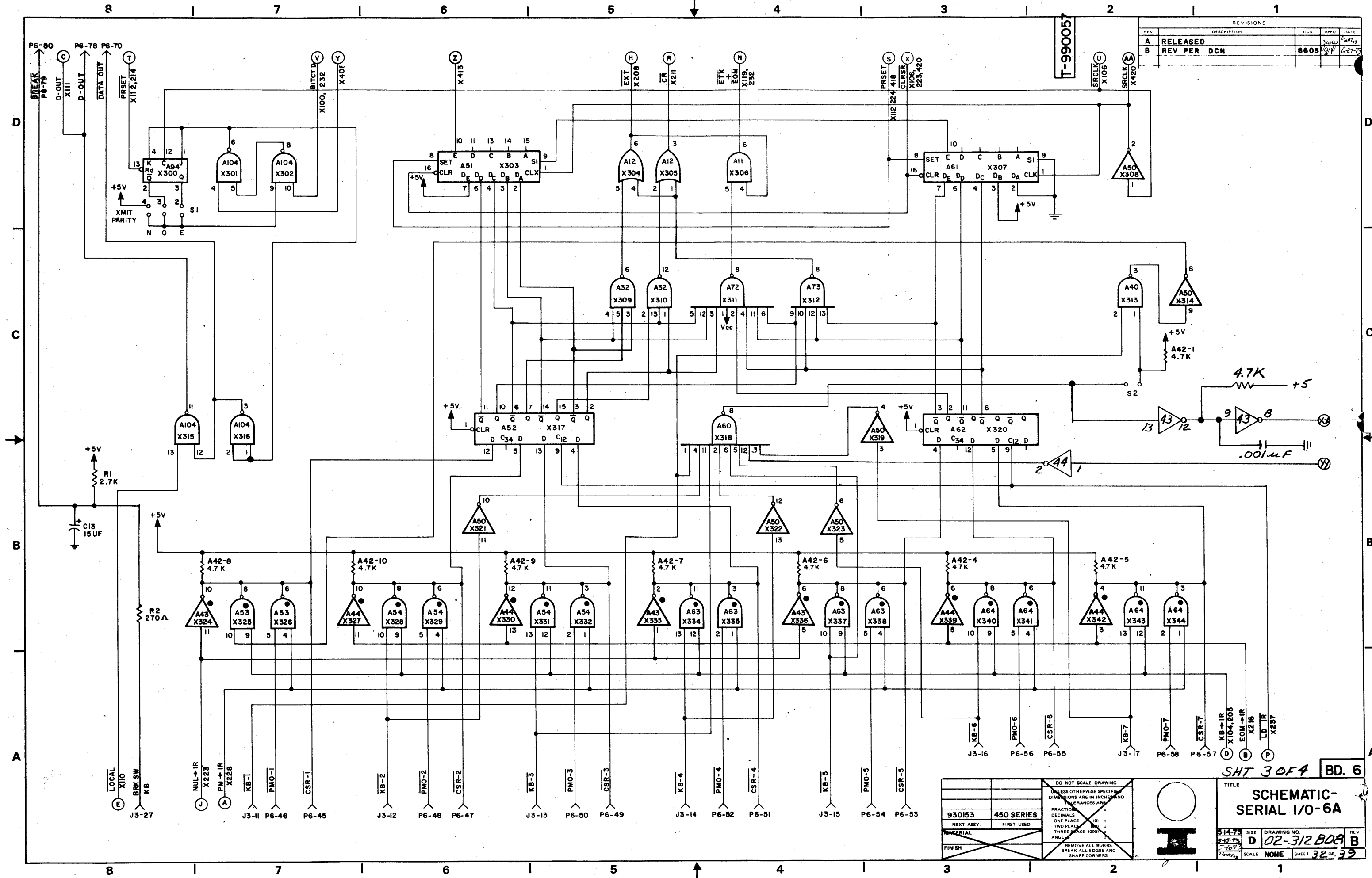
A	RELEASED	REV PER DCN	8603	6-27-73
B				

T-990057



SHT 2 OF 4 BD. 6

DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE			TITLE
930153	450SERIES		SCHMATIC - SERIAL I/O-6A
NEXT ASSY	FIRST USED	SIZE	DRAWING NO.
		D	02-312 B08 B
FINISH		SCALE	NONE
		SHEET	31 OF 39

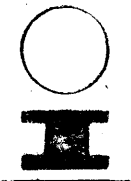


REVISIONS			
REV	DESCRIPTION	DATE	BY
A	RELEASED	10/10/73	204/23
B	REV PER DCN	8605	6-27-73

T-990057

SHT 3 OF 4 BD. 6

930153	450 SERIES
NEXT ASSY.	FIRST USED
SERIAL	ANGLE
FINISH	



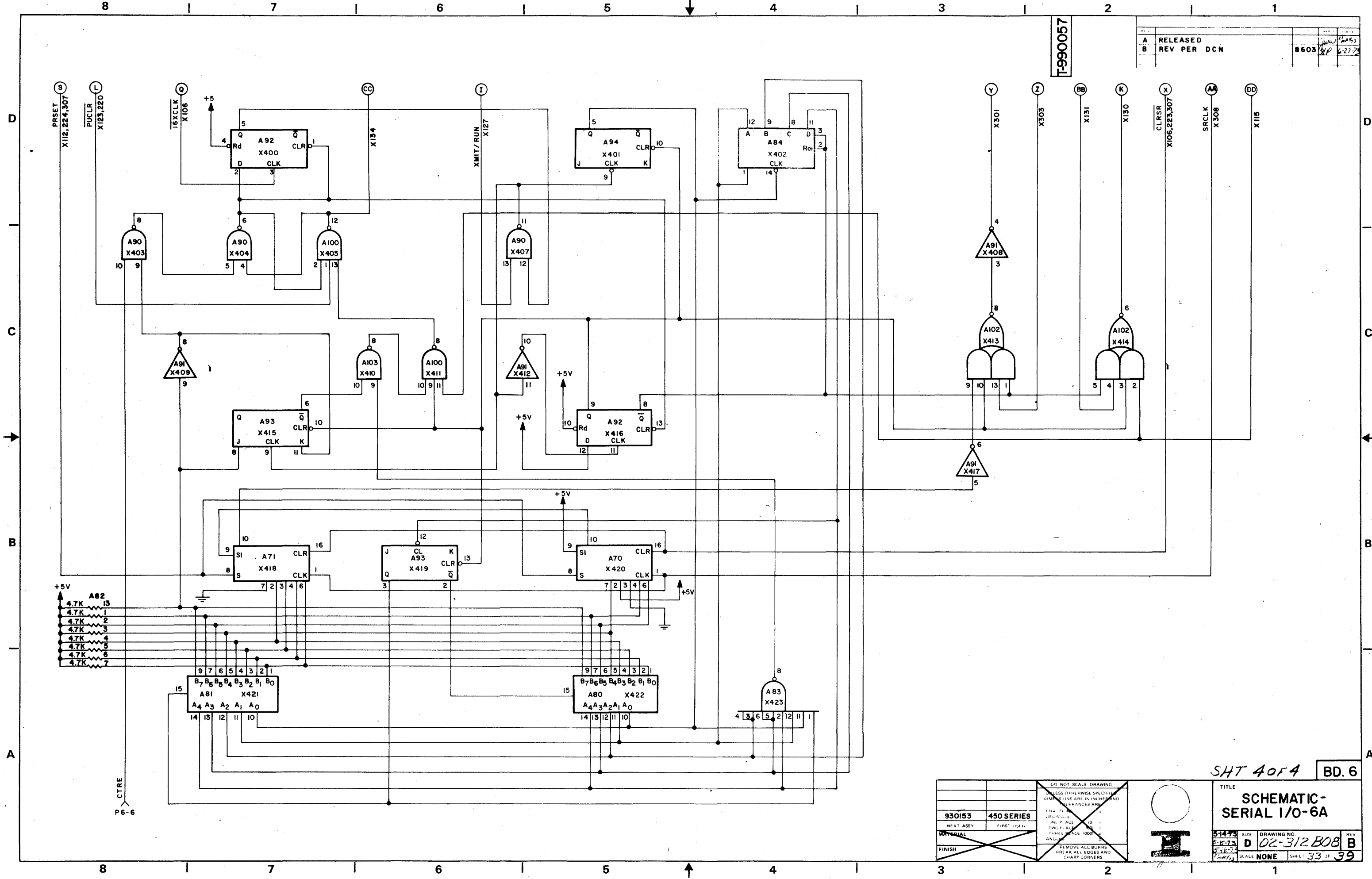
TITLE		SCHEMATIC-SERIAL I/O-6A	
SIZE	DRAWING NO.	REV	
D	02-312 B08	B	
SCALE	NONE	SHEET	32 OF 39

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND
TOLERANCES ARE:
FRACTIONS .10
DECIMALS .01
ONE PLACE .01
TWO PLACE .01
THREE PLACE .001
ANGLE 1/2

REMOVE ALL BURRS
BREAK ALL EDGES AND
SHARP CORNERS

A	RELEASED		
B	REV PER DCN	8603	6-27-73

T-990057

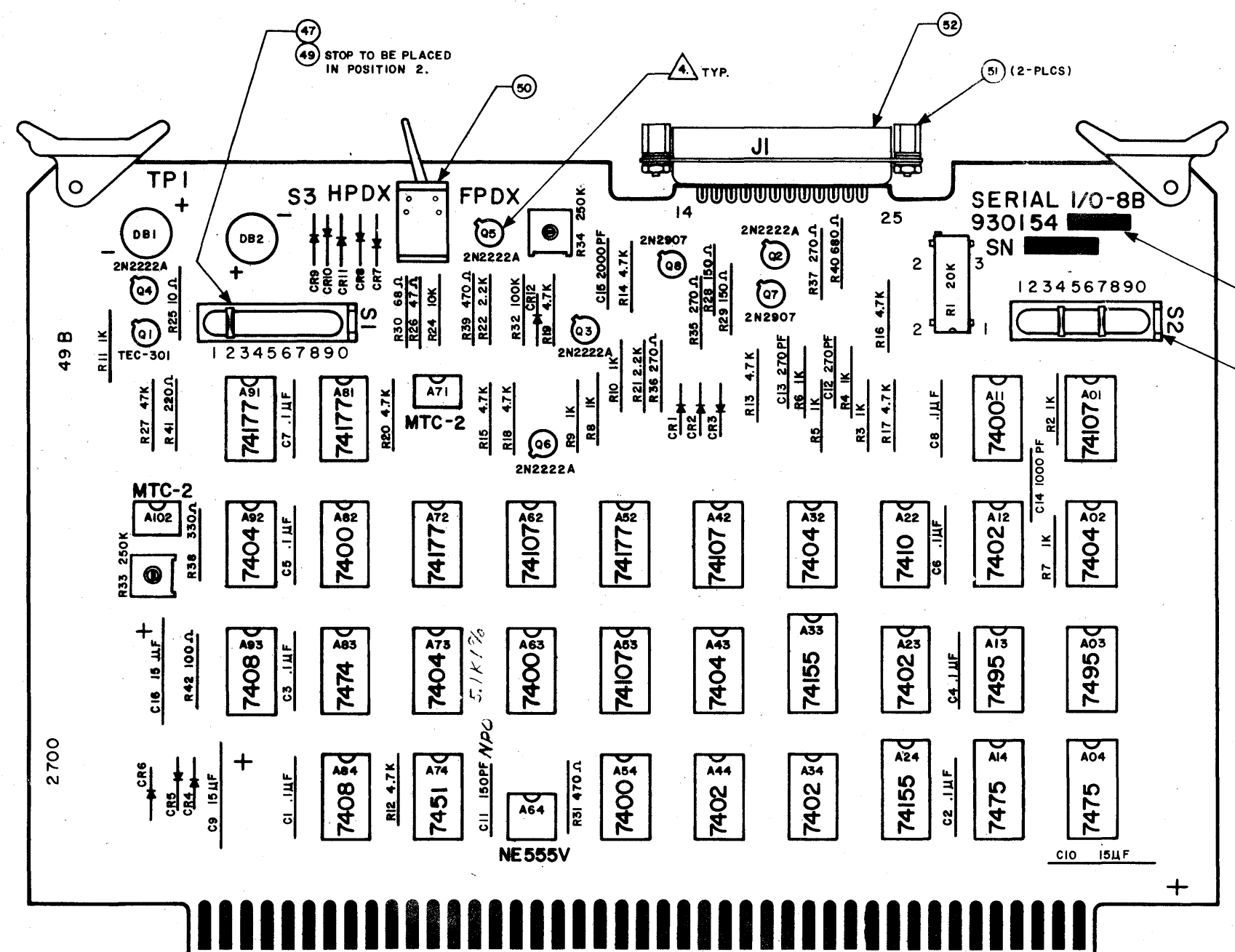


SHT 40F4 BD. 6

930153		450 SERIES	
NEXT ASSY		FIRST USU	
MATERIAL		FINISH	
DO NOT SCALE DRAWING		UNLESS OTHERWISE SPECIFIED	
DIMENSIONS ARE IN INCHES AND		TOLERANCES ARE:	
FRACTIONS		DECIMALS	
IN PLACE		TWO PLACE	
THREE PLACE		FOUR PLACE	
ANGLES		REMOVE ALL BURRS	
BREAK ALL EDGES AND		SHARP CORNERS	
TITLE		SCHEMATIC-SERIAL I/O-6A	
DRAWING NO.		02-312 B08 B	
SCALE		NONE	
SHEET		33 OF 39	

T930154

REV	DESCRIPTION	DCN	APPO	DATE
A	RELEASED			
B	REV PER DCN	8585		12/16/75



NOTES:

- 1. APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY.
- 2. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER TEC WORKMANSHIP MANUAL.
- 3. .050 MAX SOLDER OR LEAD PROJECTION ON CIRCUIT SIDE OF BOARD.
- 4. ALL TRANSISTOR CANS TO HAVE SPACERS UNDERNEATH.

PARTS LIST ISSUED

SHT 10/1

P.C.B. ASSY —
SERIAL I/O-8B

REV	DESCRIPTION	DCN	APPO	DATE
D				

450 SERIES

NEW ASSY FIRST USED

167

2/1

34 39

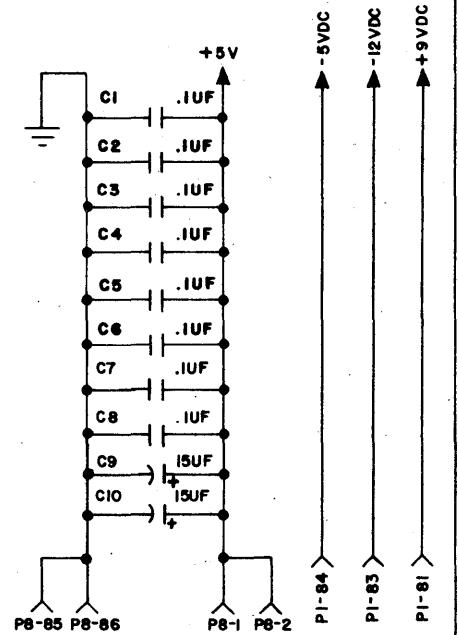
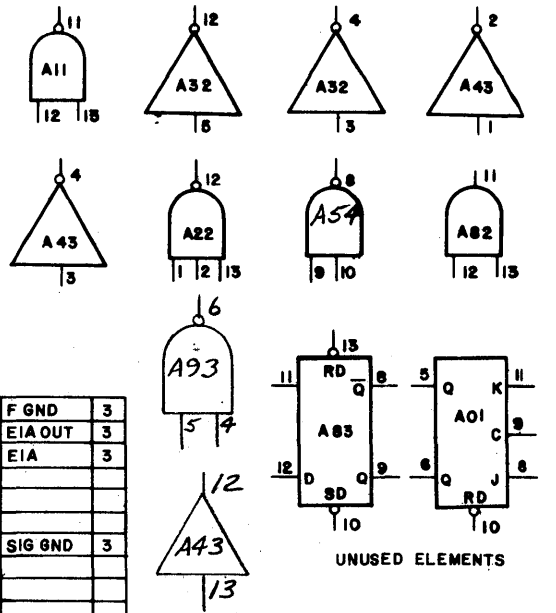
T-990058

REVISIONS				
REV	DESCRIPTION	DCN	APPD	DATE
A	RELEASED			
B	REV PER DCN	8888		5-16-73

NOTES:
 1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 1/4 W, 5%.
 2. LAST REFERENCE DESIGNATION USED:
 C16, CR 12, R41, DB 2, S125, S228, S332.

	+5V	1	2	+5V	3
		3	4	XMIT/RUN	3
		5	6	CTR-E	1
		7	8	WAIT	1
		9	10		
1	PRINT	11	12		
		13	14		
		15	16		
3	DB-1	17	18	DB-2	3
3	DB-3	19	20	DB-4	3
3	DB-5	21	22	DB-6	3
3	DB-7	23	24		
1	SET IND	25	26	RCA	1
1	CLR IND	27	28	READ	1
		29	30		
		31	32	BELL	1
		33	34	PM RT	1
		35	36		
		37	38		
		39	40	HLO	1
1	LD REG	41	42	EXT CLK	2
		43	44		
		45	46		
		47	48		
		49	50		
		51	52		
		53	54		
		55	56		
		57	58		
		59	60	KB LOCAL	1
		61	62		
		63	64		
2	OB FULL	65	66		
2	16X FREQ	67	68		
3	DATA OUT	69	70	LOK+RD	1
3	H DATA	71	72	FUNCT	1
		73	74		
		75	76		
3	D-OUT	77	78		
1	BREAK	79	80	PUCLR	1
		81	82		
	+9VDC	83	84	-8VDC	
	GND	85	86	GND	
PG	NAME	PIN	NAME	PG	

PIN	NAME	PG
1	F GND	3
2	EIA OUT	3
3	EIA	3
4		
5		
6		
7	SIG GND	3
8		
9		
10		
11		
12	CLT	3
13	CLR	3
14	TTL OUT	3
15	TTL	3
16		
17		
18		
19		
20		
21		
22		
23		
24	CLT	3
25	CLR	3



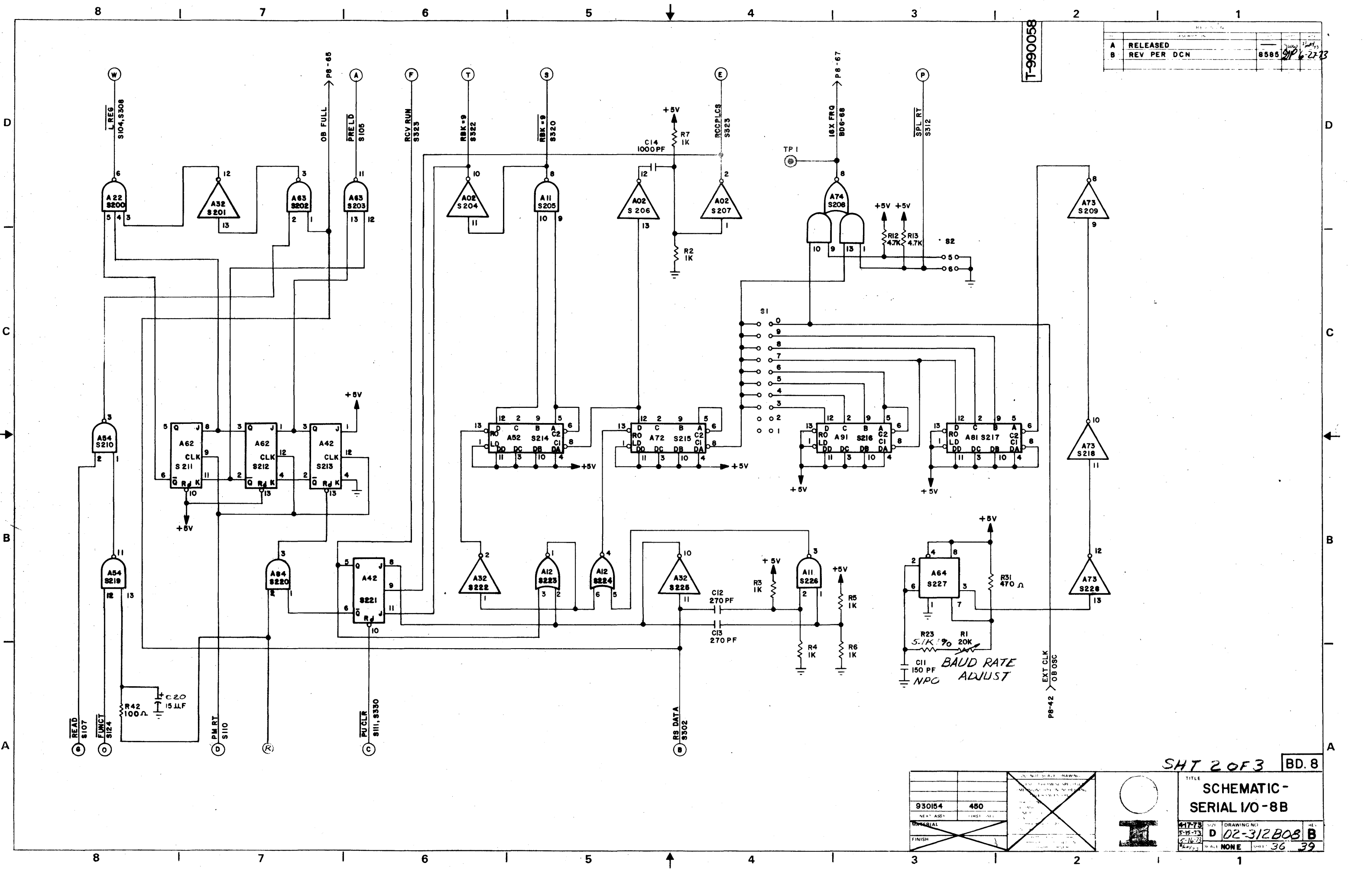
CHIP TYPE	LOCATION
7400	A11, 54, 63, 82
7402	A12, 23, 34, 44
7404	A02, 32, 43, 73, 92
7408	A84, 93
7410	A22
7451	A74
7474	A83
7475	A04, 14
7495	A03, 13
74107	A01, 42, 53, 62
74155	A24, 33
74177	A52, 72, 81, 91
NE555V	A64
MTC-2	A71, 102

SHT 10F3 BD.8

DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE:			TITLE SCHMATIC - SERIAL I/O-8B
930154 NEXT ASSY	450 FIRST USED		
REMOVE ALL BURRS BREAK ALL EDGES AND SHARP CORNERS		SCALE NONE	SHEET 35 39

A	RELEASED		
B	REV PER DCN	8586	9/16/73

T-990058



SHT 2 OF 3 BD. 8

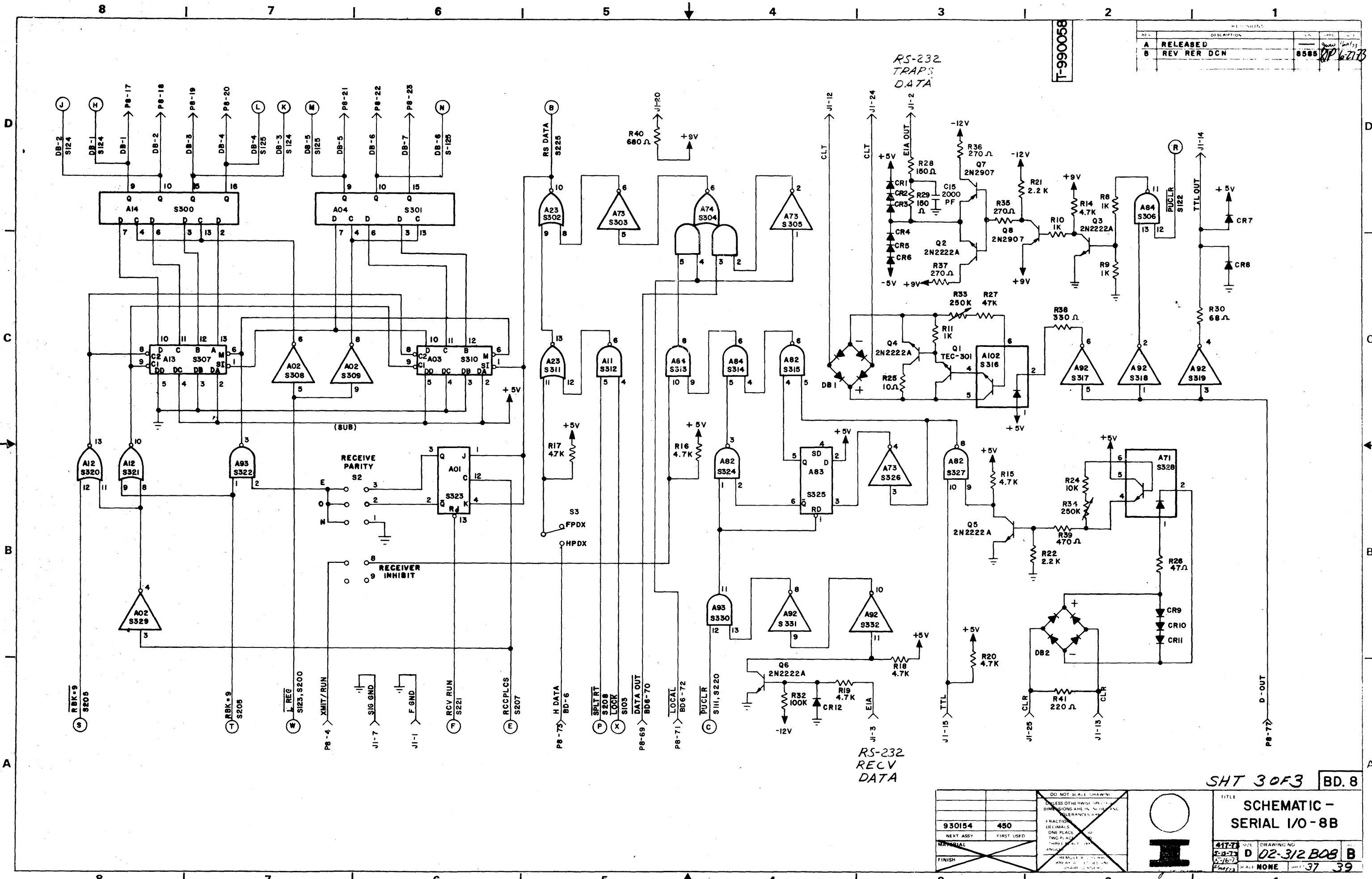
930154		450		SCHEMATIC-SERIAL I/O-8B	
D		02-312B08		B	
NONE		36		39	

REV	DESCRIPTION	DATE	BY
A	RELEASED		
B	REV RER DCN	8585	JP 6/2/73

T-990058

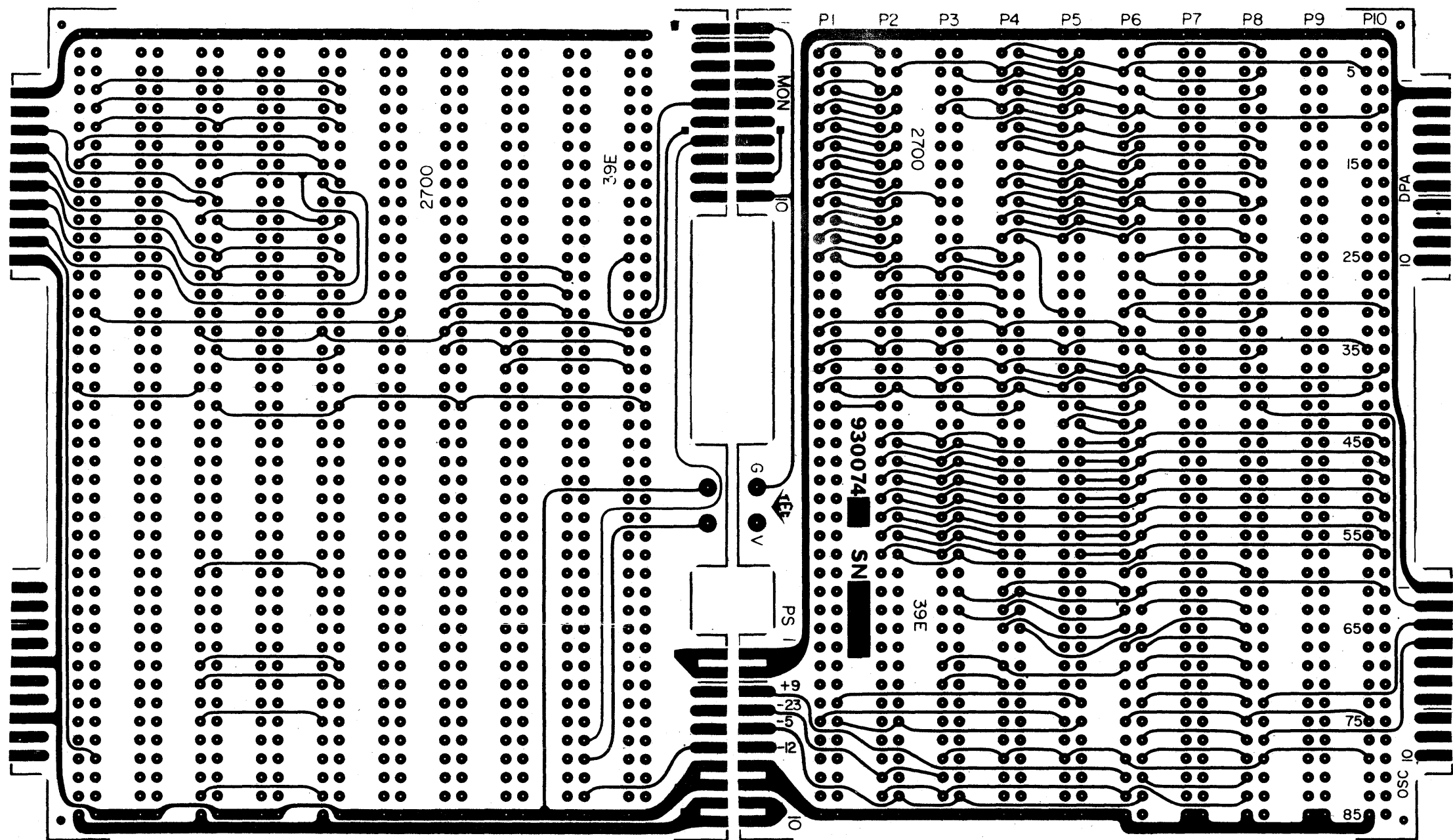
RS-232 TRAPS DATA


RS-232 RECV DATA



SHT 30F3 BD. 8

930154		450		DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ONE PLACE TWO PLACE THREE PLACE	
NEXT ASSY	FIRST USED			REWORK AND REPAIR ARE TO BE DONE IN ACCORDANCE WITH THE DRAWING	
FINISH				TITLE SCHEMATIC - SERIAL I/O - 8B	
				DRAWING NO. D 02-312 B08 B	
				SCALE NONE	
				PAGE 37 39	

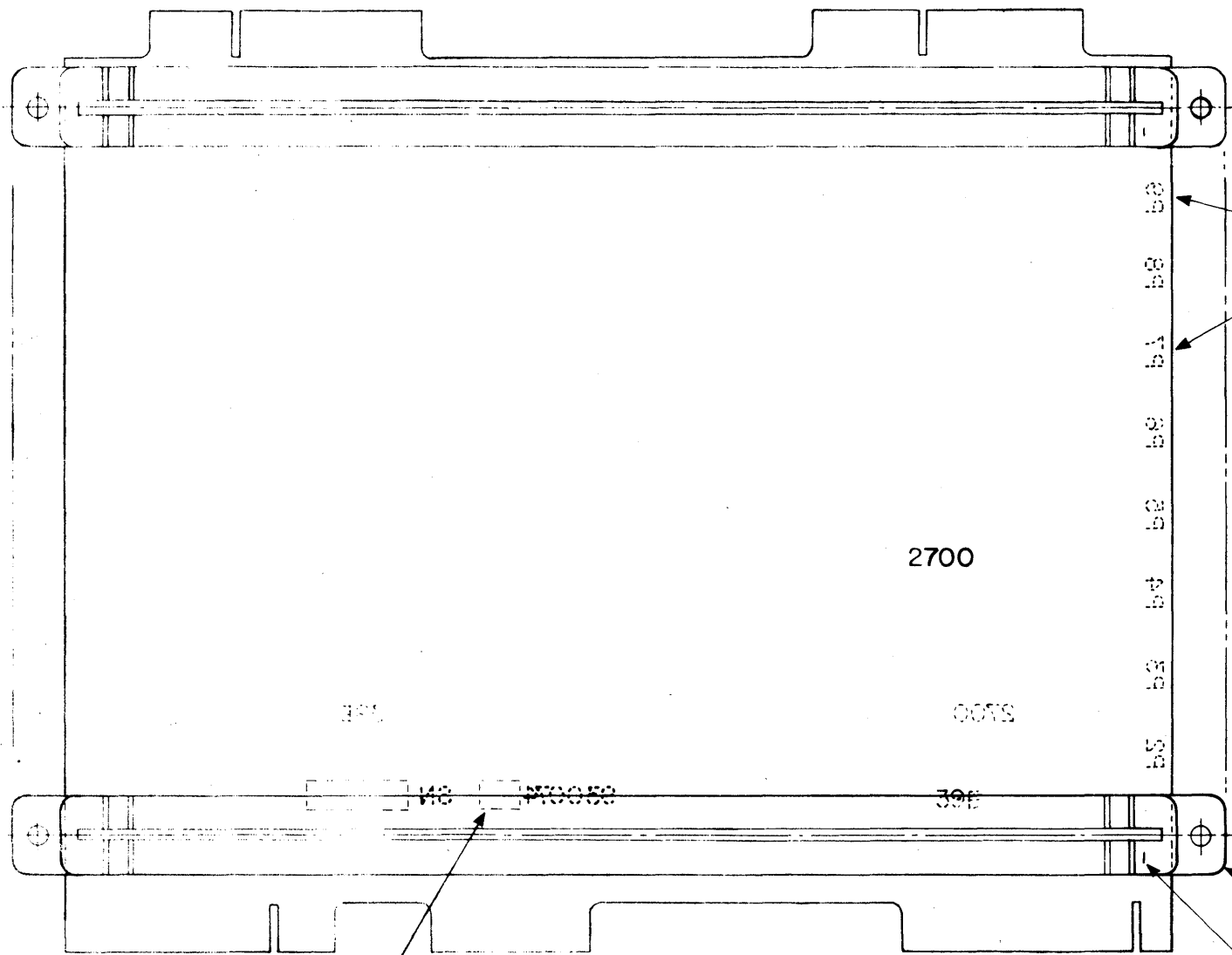


	BACK PANEL
	02-312 B08
	38 of 39

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

930074

REVISIONS			
REV.	DESCRIPTION	DCN	APPD. DATE
A	RELEASED		3/28/72
B	REV PER DCN	8436	3/28/72
C	REV PER DCN	8478	3/28/72
D	REV PER DCN	8439	3/28/72
E	REV PER DCN	8606	3/28/72



DO NOT PUT CONNECTORS IN P7 AND P9.
MASK PAD AREA BEFORE WAVE SOLDERING.

NOTES:

- 1. APPLICABLE DASH NUMBER AND REVISION LEVEL TO BE MARKED ON BOARD AT ASSEMBLY.
- 2. SOLDER COMPONENTS TO CIRCUIT SIDE OF BOARD PER PARAGRAPH 4.32 OF TEC WORKMANSHIP MANUAL.

OPPOSITE SIDE

781456 (8)
CONNECTORS

PIN 1 IS LOCATED AS SHOWN.
TYP. (8).

PARTS LIST ISSUED

SHT 1 OF 1

DO NOT SCALE DRAWING			TITLE	P.C.B. ASSY. MOTHERBOARD "400" SERIES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE			SIZE	DRAWING NO.
NEXT ASSY.	FIRST USED	3-6-72	D 02-312.808 E	
MATERIAL		7-6-72	SCALE 2/1 SHEET 39 OF 39	
FINISH	REMOVE ALL BURRS BREAK ALL EDGES AND SHARP CORNERS			

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

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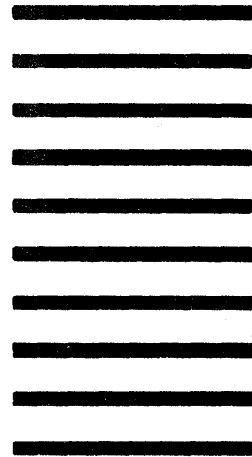
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