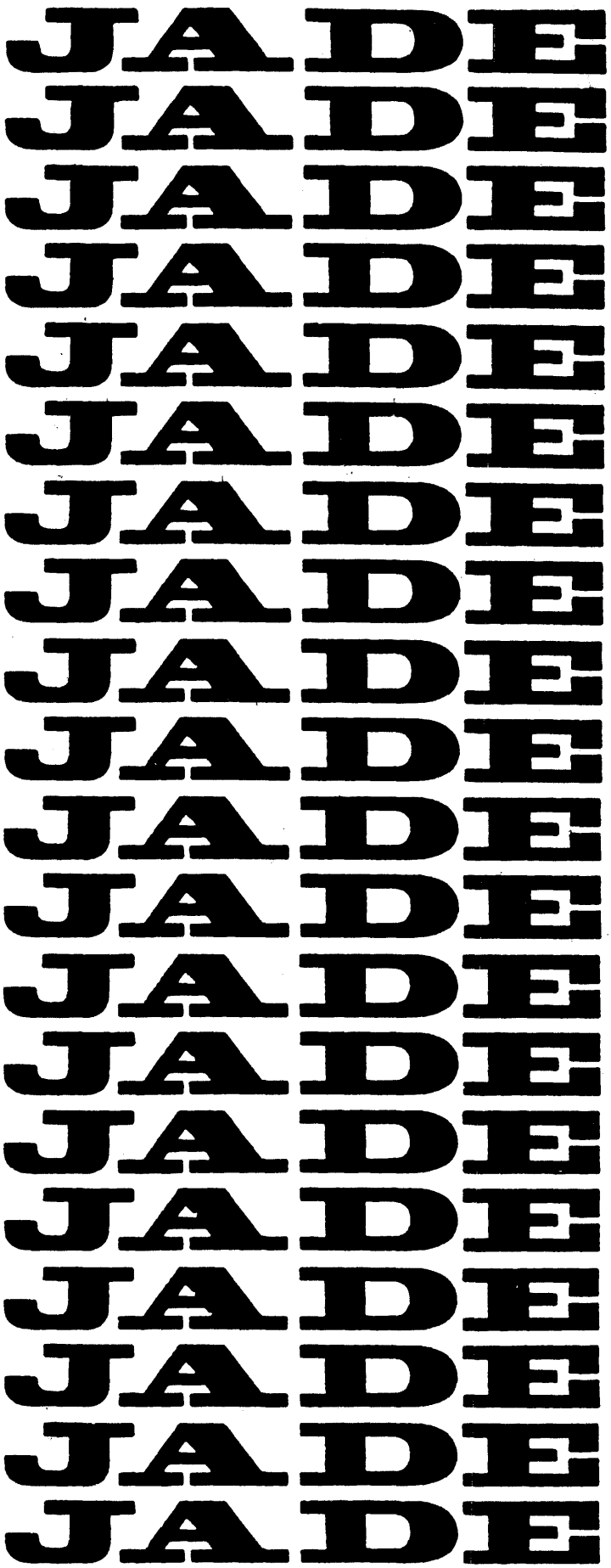

The Double D

4901 West Rosecrans Ave., Hawthorne, Ca. 90250 213-973-7707

JADE COMPUTER PRODUCTS

PRESENTS

Double D

THE DOUBLE DENSITY DISK CONTROLLER

HARDWARE MANUAL

IOD-1200M

REVISION C

Jade Computer Products
4901 Rosecrans Ave
Hawthorne, California
90250

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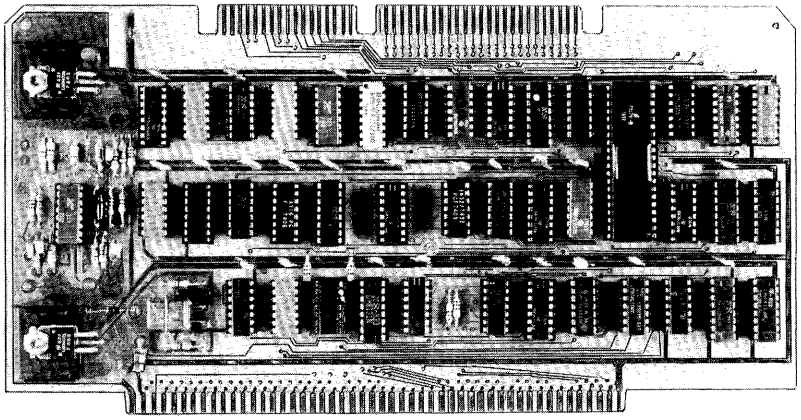

Jade Double D, Double-Density Disk Controller

The new Jade Double D Disk Controller represents a major advance in Floppy disk recording technology. Designed at the leading edge of state-of-art technology, it is the first truly universal disk controller.

The Double D is S-100 compatible and meets all specifications of the proposed IEEE S-100 standard. It is based on the Western Digital 1791 with advanced phase locked-loop frequency control.

- 5¼" or 8" drive capability
- Single or double-sided recording
- Single or double-density recording
- IBM 3740 or System 34 soft sector format
- Use programmable formatting
- Will handle Shugart, MFE, Sieman MPI, and other drives
- Fully CP/M™ compatible
- Programmable single or double-density, and single or double-sided
- Supported by a vast library of software, including an extensive business systems package
- Designed to work with dynamic or static memory cards

SPECIFICATIONS

BUS	S-100	**DIMENSIONS**	Standard S-100 5.0" High, 10.0" Wide
COMPATIBLE CPU'S	Z80, 8080 & 8085, Single Density	**CONNECTORS**	S-100 — 100 pin card edge, .125 spacing
STORAGE CAPACITY	Greater than 8 Megabytes (8 Double-Density, Double-Sided 8" Drives)		5¼" Disk — 34 pin card edge, .100 spacing
	Greater than 1 Megabyte (3 Double-Density, Double-Sided 5¼" Drives)		8" Disk — 50 pin card edge, .100 spacing
POWER REQUIREMENTS	+ 8VDC @ 850 MA (Max) + 16VDC @ 50 MA (Max)	**COST**	Assembled & Tested $299.00
			Kit $249.00
OPERATING TEMP.	0 to 50° C		Bare Board $ 55.00

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JADE Computer Systems
4901 West Rosecrans, Hawthorne, California 90250 (213) 679-3313

TABLE OF CONTENTS

SECTION 1

INTRODUCTION

1.1 SCOPE

This manual contains the complete hardware description of the Jade Double Density Disk Controller. It provides the end user with construction and configuration procedures, and a functional description of the circuitry.

1.2 RELATED DOCUMENTATION

Double D Software Manual P/N IOD-1201M	Jade Computer Products
FD 179X-01 Specifications	Western Digital Corp.
Z80A-CPU Technical Manual	Zilog, Inc.

1.3 DESCRIPTION

The Double D is an intelligent S-100 based disk controller. It is capable of handling up to four full size (8") or mini (5") disk drives. Provisions have been made for double sided drives. Single and double sided drives may be mixed. The controller is capable of single density (FM) and double density (MFM) operation. It can be used in software polled as well as interrupt driven environments. Circuitry is implemented on a four layer printed circuit board where one inside layer is used as a ground plane. This provides for a minimal amount of ground noise. This board was designed to meet the proposed S-100 signal disciplines as defined in IEEE Task 696.1/D2

The Double D contains an on-board Z80A microprocessor with 2K of static memory. The on-board processor runs simultaneously with and transparent to the S-100 bus. All critical timing is handled on-board; data transfers are fully buffered by sector in the on-board memory, two levels of interrupt are implemented on the Z80A, and a wait state generator is used to synchronize the on-board processor to the disk transfer rate. The host system (8080, 8085, Z80, or ?) need only transfer commands and data through a block of static memory, which can be accessed from the bus. This architecture provides a high degree of timing independence from the host system. Also, since the disk controller program is contained on-board in ram, this board's operational characteristics are redefinable at any time during system operation.

The powerful FD 1791-01 Formatter/Controller is used to encode and decode all data transfers to and from the disk drives. It also provides for the generation and checking of address marks, data marks, and the cyclic redundency characters. Write Precompensation can be selected under software control at three levels of intensity, providing flexible data recording. Data separation is achieved by the use of a phase-locked loop to insure maximum immunity to disk speed variation and to enhance data recovery margins in both single and double density.

1.3 DEVICE SPECIFICATION

Power requirements:	+7 TO +11 Volts	0.90 Amp. Typical 1.50 Amp. Maximum
	+14.5 to +21.5 volts	25 Ma. Typical 50 Ma. Maximum
	-14.5 to -21.5 volts	8 Ma. Typical 30 Ma. Maximum
System Port Requirement:	One I/O port, switch selectable	40,41,42,43 Hex
System Memory Requirement:	1K Byte block switch selectable	E000,E400,E800,EC00, F000,F400,F800,FC00 Hex
Recording Method:	Single density in FM Double density in MFM	
External Communication:	One EIA compatable input signal One EIA compatable output signal	
Disk Interface, Connectors:	8" Drives	50 Pin Card Edge Connector AMP P/N 888083-1 3M P/N 3415-0001
	5" Drives	34 Pin Card Edge Connector AMP P/N 583717-5 3M P/N 3463-0001
System Interrupts:	Optional Feature, Vector Interrupt on	VI0* thru VI7*

SECTION 2

HARDWARE DESCRIPTION

2.1 OVERVIEW

The operational characteristics of the DOUBLE D are a function of both hardware and on-board software. The hardware provides the data paths, logic functions, and control signals necessary to implement such operations as head loading, drive selection, head positioning, and transfering data. It is the software that determines how the disk controller commands are interpreted and in what sequence controller events take place. As in all microprocessor designs, the software can do no more than hardware implementation allows. The DOUBLE D is designed to allow the on-board software as much control as possible. For the user who will write control programs for this board, an understanding of the hardware is recommended. This section provides a description of the hardware.

2.2 MEMORY ADDRESS DECODING

The S-100 bus address lines are constantly monitored by the Memory Address Detection circuit. See Figure 2-1. In the Standard address mode, ICs 3H and 3B implement detection of the selected 1K memory block. Switches M10, M11, and M12 are used to locate the selected memory block on any 1K boundry from E000 to FC00. Note: signals SA10, SA11, and SA12 indicate the corresponding address switch settings. See Table 2-1. For the Extended Address Mode, IC 4B must be installed and the Address Mode Block altered to the appropriate position. In this configuration, address decoding is provided for any 1K block in the upper 8K of the 24 bit address bus. In either mode, an address match is indicated by BMA* (Bus - Memory Addressed) being asserted (low).

SWITCH M12	SWITCH M11	SWITCH M10	SA12	SA11	SA10	ADDRESS RANGE IN THE SYSTEM
Closed	Closed	Closed	0	0	0	E000 - E3FF
Closed	Closed	Opened	0	0	1	E400 - E7FF
Closed	Opened	Closed	0	1	0	E800 - EBFF
Closed	Opened	Opened	0	1	1	EC00 - EFFF
Opened	Closed	Closed	1	0	0	F000 - F3FF
Opened	Closed	Opened	1	0	1	F400 - F7FF
Opened	Opened	Closed	1	1	0	F800 - FBFF
Opened	Opened	Opened	1	1	1	* FC00 - FFFF

Table 2-1. Memory Address Selection

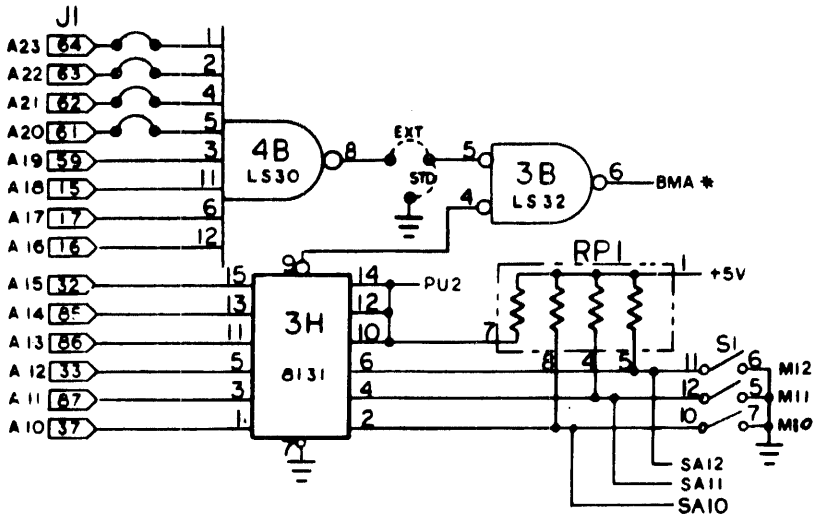


Figure 2-1. Memory Address Detection

2.3 PORT ADDRESS DETECTION

S-100 address lines A0 thru A7 are constantly monitored by the Port Address Detection circuit. This circuit is composed of IC 3F and part of 3E. See figure 2-2. Switches "P0" and "P1" are used to vary the selected port address from 40 thru 43 hex. An address match is indicated by BPA* (Bus - Port Addressed) being asserted.

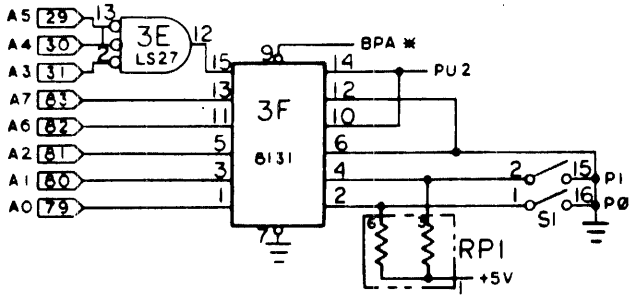


Figure 2-2.
Port Address Detection

SWITCH P1	SWITCH P0	ADDRESS PORT
Close	Close	40
Close	Open	41
Open	Close	42
Open	Open	43

Table 2-2.
Port Address Selection

2.4 BUS CONTROL SIGNALS

All Control Signals from the S100 bus are buffered by ICs 1H and 3K before internal use. These line recievers have schmitt trigger inputs typically offering 400 millivolts hysteresis. See Figure 2-**3**.

In some older mainframes SLVCLR* is not implemented. For use in those systems POC* (pin 99) can be connected to SLVCLR* by a jumper (BRST* to POC*).

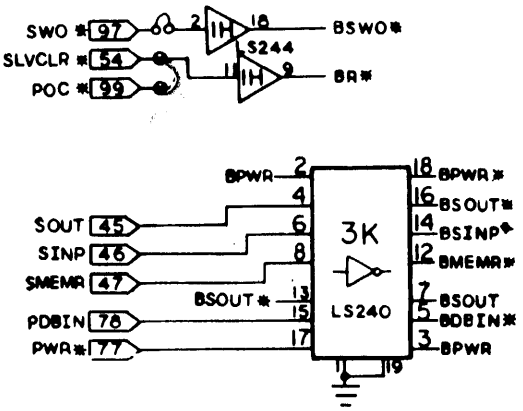


Figure 2-3.
Control Signal Buffers

2.5 DISK PROCESSOR CONTROL PORT

The Disk Processor Control Port is an S-100 output port which provides the host system with control of the on-board processor. The port is strobed by the occurance of sOUT, pWR*, and a matching port address (BPA*). The following functions are implemented.

1. Switch internal memory to and from the bus.
2. Issue an interrupt to the Z80A processr
3. Reset the Z80A processor.

The board reset signal BR* brings the port to the initial state where internal memory is switched into the S-100 bus. Refer to Figure 2-4 for circuit details.

SLVRQ is set by data bit 0. Asserting SLVRQ* initiates the memory switch process. SLVRQ* is applied to the Z80A BUSRQ* pin. When SLVRQ* (RUSRQ*) is asserted, the Z80A tri-states its data, address, and control lines. The Z80A then asserts SLVACK* (BUSACK*). Refer to the Z80A TECHNICAL MANUAL. Assertion of SLVACK* enables the Memory Control circuit to respond to S-100 memory cycles.

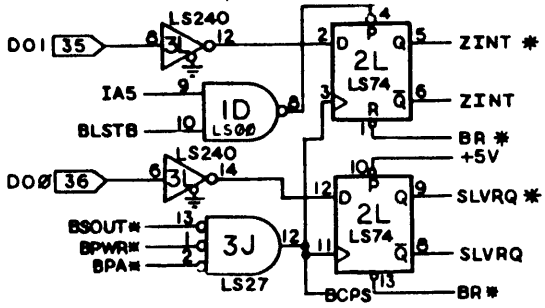


Figure 2-4. Control Port

ZINT is set by data bit 1. ZINT(*) serves a dual function. ZINT* is the maskable interrupt request to the on-board Z80A. Note, circuit implementation makes it possible for the on-board Z80A to test and reset ZINT* under software control. More on this later. ZINT also controls which 1K bank of internal memory is selected for bus access. When memory is switched to the S-100 bus, the on-board Z80A has asserted SLVACK* and will not respond to an interrupt. At this time ZINT is used as internal address bit 10.

ZRST* is the reset line to the on-board Z80A. It is an output of IC 1A, a one-shot, which is triggered by writing to this port while data bit 7 is asserted high.

2.6 DISK PROCESSOR STATUS PORT

The Disk Processor Status Port is an S-100 input port which allows the host processor to examine the current state of the Disk Processor. The port responds to the occurence of pDBIN, sINP, and a matching port address (BPA* asserted). The following states can be determined by reading this port.

1. On-board processor state (Run/Halt)
2. Address of the 1K memory window.

The address of the memory window is determined by reading the M10, M11, and M12 switch positions as indicated by signals SA10, SA11, and SA12. Table 2-1 shows the relation between signals SA10-SA12 and the selected window address. Processor Status Port

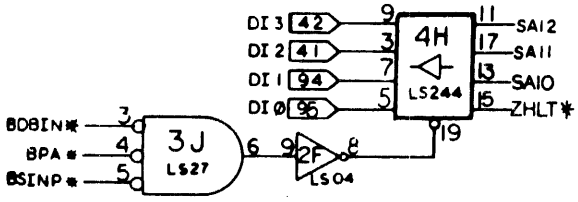


Figure 2-5.
Processor Status Port

The on-board processor state is indicated when reading ZHLT*. This is the Z80A halt flag. Reading a "0" on data bit 0 indicates that the on-board processor has halted.

2.7 CLOCK GENERATION

The clock signals for the Z80A and FD 1791-01 are generated on-board by a crystal oscillator, divider and driver. See figure 2-6. The crystal is a fundamental type operating at 8.000 Mhz. The oscillator is implemented with two sections of IC 3L. A third section is used to square the output of the oscillator. IC 2M is used to divide the clock. The CLOCK SELECT JUMPER is set depending on the disk drive to be used. The FD 1791-01 requires a 2.000 Mhz clock for 8" drives and a 1.000 Mhz clock for the 5" drives. The jumper provides for the selection of a additional divide by 2. With 8" drives the Z80A is run at 4.000 Mhz. With 5" drives the Z80A runs at 2.000 Mhz to provide adequate port enable (RE* and WE*) timing for the FD 1791-01. A section of IC 1F and U-5 provide a MOS level clock driver for the Z80A as recommended by Zilog.

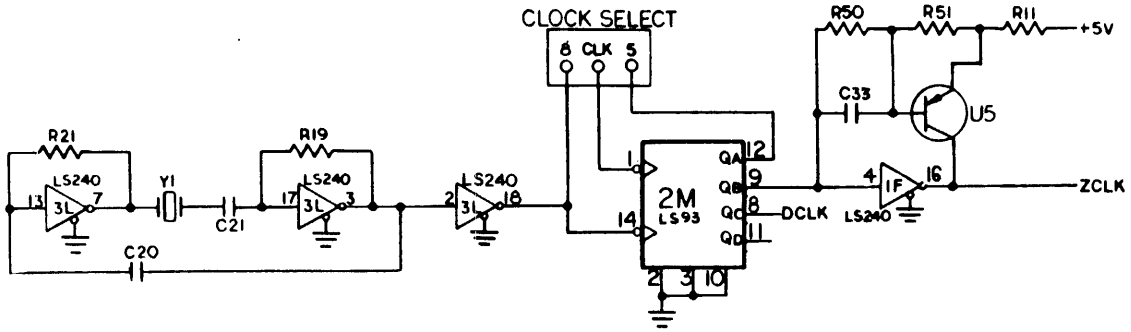


Figure 2-6. Clock Circuit

2.8 PROCESSOR

The on-board processor function is implemented with the Z80A. It was selected because of execution speed and compatability with TTL logic families. The processor uses the on-board 2K static memory for program, stack, parameters, and for buffering single/multiple sectors of data. Because the 5 upper address bits are not decoded, this 2K block appears 32 times in the Z80A 64K address range. This allows internal programs to be assembled on any 2K boundary. Note, the address selected for the memory window has no effect on the on-board processor or the on-board software.

The host system communicates with the on-board processor thru the memory window. During a system boot, the control program must be loaded thru the memory window before the on-board processor can operate properly. It is entirely possible for the initial control program to be a small bootstrap which then loads a larger control program from disk. For reading and writing disk sectors, the host system must block move sector data through the memory window.

Both Z80A interrupts are implemented. The host system issues the maskable interrupt by executing an OUTPUT instruction to the Disk Processor Control Port. The FD 1791-01 issues an interrupt upon command completion. The Z80A NMI* pin is used for interrupts from the 1791-01. This interrupt is clamped by CR18 when DSE (Drive Select Enable) is low.

2.9 DISK CONTROLLER

The Western Digital 1791-01 is used for all data transfers to and from disk. This device is addressed as four I/O ports from the on-board processor. The user should refer to FD 1791-01 specifications for a detailed description of this part. Access to the FD 1791-01 Status Port allows reading the disk interface signals. These are WRITE PROTECT*, READY*, INDEX*, TRACK-ZERO*, and SEEK-COMPLETE*.

2.10 DISK INTERFACE

Disk Interface is provided by two gold-plated card edges at the top of the P.C. board. The 50 pin (J-3) card edge is intended for the 8" disk drives. The mating connector is the same type as is used to connect the other side of the ribbon cable to the disk drive (with most drives). All even numbered contacts (component side) are connected to internal circuitry thru a double set of plate-thru-holes. By cutting the connecting links and adding jumpers, the signal assignments for each contact can be altered. The 34 pin card edge (J-2) is intended for 5" disk drives. All unassigned contacts provide a plate-thru-hole for alteration. Additional signals can be assigned to this connector by jumping from J-3 to J-2. On connectors J-2 and J-3 all odd-numbered contacts are grounded.

2.11 INTERNAL I/O ADDRESSES

There are seven I/O ports available to the on-board processor. These internal ports are not accessable from the host system. They are used for control signals, status information, and data paths. They are decoded using address bits A0 thru A2.

ADDR	TYPE	DESCRIPTION
00	Input	Board Level Status
00	Output	Board Level Command
04	Input	Disk Controller Status
04	Output	Disk Controller Command
05	I/O	Disk Controller Track
06	I/O	Disk Controller Sector
07	I/O	Disk Controller Data

Table 2-3. Internal I/O Ports

Address bits A3 thru A7 have no effect on I/O operations except when accessing the Board Level Status Port. These upper address bits individually trigger on-board events when asserted high during an INPUT operation from this port. A list is provided in Table 2-4. For a detailed description refer to the appropriate section.

BIT	FUNCTION	SECTION
A3	Issue Step Pulse	2.15
A4	Clear Timer	2.14
A5	Reset Host Interrupt	2.5
A6	Initiate Timer	2.14
A7	Wait State Request	2.16

Table 2-4. Address Bit Assignments

2.12 BOARD LEVEL STATUS PORT

The Board Level Status Port is a parallel input port to the on-board Z80A. It provides the processor with access to board signals that cannot be read from the FD 1791-01. These signals are listed and described in Table 2-5. See Figure 2-7 for circuit diagram.

DATA BIT	SIGNAL NAME	DESCRIPTION
0	U0	User 0 switch setting
1	U1	User 1 switch setting
2	TST*	Test mode
3	ZINT	Interrupt req from host
4	SERI	EIA level input bit
5	TOFF	Timer off
6	ILP*	Illegal pack inserted
7	CHNG*	Disk has been changed

Table 2-5. Board Level Status Bits

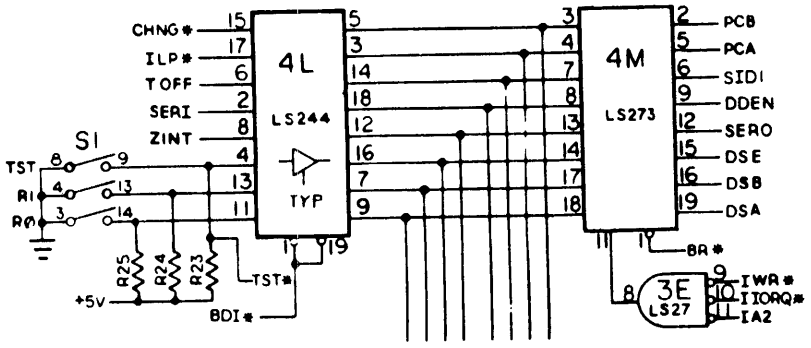


Figure 2-7. Board Level Ports

2.13 BOARD LEVEL COMMAND PORT

The Board Level Command Port is a parallel output port of the on-board processor. It is used to select various parameters as listed in Table 2-6. See Figure 2-7 for circuit details.

DATA BIT	SIGNAL NAME	DESCRIPTION
0	DSA	Drive select bit A (2**0)
1	DSB	Drive select bit B (2**1)
2	DSE	Drive select enable
3	SERO	EIA signal output control
4	DDEN	Double density enable
5	SID1	Side and direction select
6	PCA	Precomp select A
7	PCB	Precomp select B

Table 2-6. Command Port Bits

The signals DSA and DSB are used to determine which drive is selected. DSE must be asserted for drive selection to take place. DSE is also used to enable the on-board processor to accept an interrupt from the 1791-01. See Table 2-7 for drive selection.

DSE	DSB	DSA	DRIVE
0	X	X	NONE
1	0	0	0
1	0	1	1
1	1	0	2
1	1	1	3

Table 2-7.
Drive Selection

Double Density operation is enabled when DDEN is set high. A low SERO signal corresponds with a negative EIA output.

SID1 serves a dual function. When using double-sided drives and performing any type of read or write operation, this signal selects which side of the diskette is used. A low SID1 selects the same side as used on single-sided drives. When stepping operations are being performed, SID1 functions as the direction select, a low SID1 will cause stepping operations to move the head toward track 0 (most drives).

Precompensation is controlled by signals PCA and PCB. These two signls allow precompensation to be enabled and at three different levels of intensity. Table 2-8 lists this function.

PCB	PCA	PRECOMPENSATION
0	0	OFF
0	1	200 ns.
1	0	160 ns.
1	1	120 ns.

Table 2-8. Write Precompensation

2.14 ON-BOARD TIMER

The On-Board Timer provides both a motor control for 5" drives and a means for deselecting any drive if not used for a given period of time. The 1791-01 will unload the head of a drive if not used in 15 revolutions, but in some drives the stepper-motor will still consume power. The timer is under complete control of the on-board processor. It can be set, reset, and examined by appropriate I/O operations. See figure 2-8.

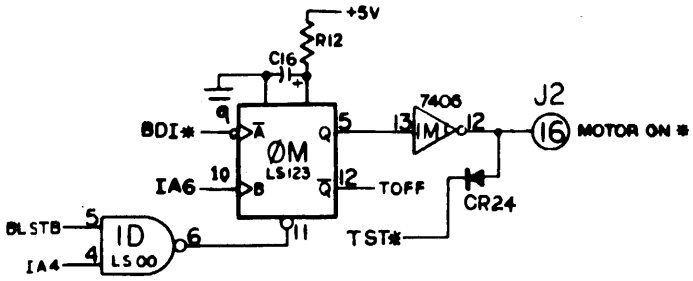


Figure 2-8.
On-board Timer

2.15 STEP CONTROL

The STEP CONTROL circuit provides more flexible control of the step function than the 1791-01. Step pulses are issued under control of the on-board processor. The interval between step pulses are timed by on-board software and can be resolved to better than 0.10 milliseconds. The step pulse width has been set at 3 microseconds. This appears satisfactory for most disk drives. If needed, this value can be altered by chosing a new value for C9 or R10. See Figure 2-9.

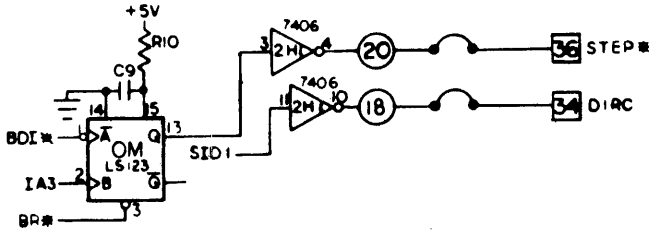


Figure 2-9. Step and Direction

2.16 WAIT STATE GENERATOR

The Wait State Generator is used to synchronize the on-board processor to the Disk Controller when data is being transferred between the Double-D and a disk drive. The wait state is generated during the execution of an input instruction from the Board Level Status Port while address bit A7 is held high. The wait-state is held until the FD 1791-01 issues either a Data Request (DDRQ) or an interrupt (DINT). For circuit details refer to figure 2-10.

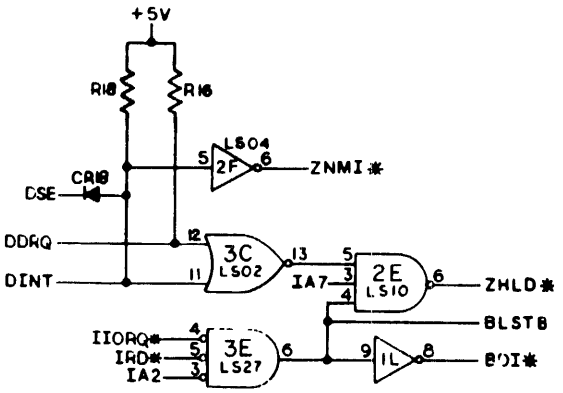


Figure 2-10. Wait States

2.17 VECTOR INTERRUPT GENERATOR

The Vector Interrupt Generator may optionally be used to issue an interrupt to the host processor system. The interrupt is issued on one of VIO* thru VI7*, selectable by jumper, when the on-board processor executes the HALT instruction. The interrupt request is terminated when the host processor either switches the Double-D memory into the S100 bus or issues an interrupt to the Double-D. See figure 2-11 for circuit details.

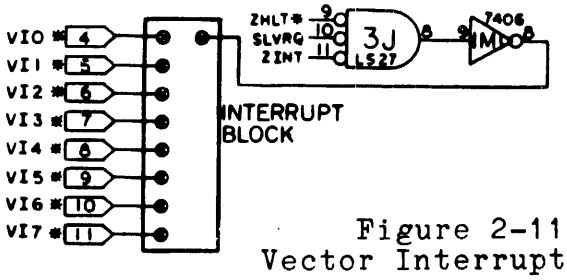


Figure 2-11. Vector Interrupts

2.18 EIA LEVEL INTERFACE

The EIA LEVEL INTERFACE provides the level conversions to and from TTL. These EIA level lines are made available at connector J4, an 8-pin DIP socket located close to IC 1A.

2.19 MEMORY CONTROL

The Memory Control Circuit is used to operate the on-board memory. When SLVACK* is high, the on-board Z80A is performing memory read and write operations. When the internal memory is present in the S100 bus (SLVACK* low), the host processor may perform read and write operations. Refer to Figure 2-12 for circuit diagram.

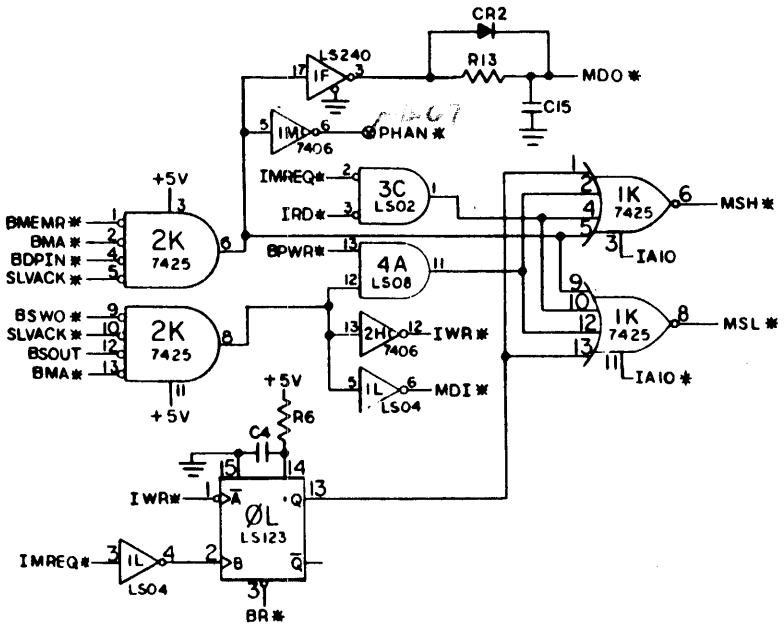


Figure 2-12. Memory Control Circuit

S100 bus requests for read and write operations are decoded by IC 2K. IC 2K pin 6, when high, indicates a memory read is taking place. IC 1M pin 6 can be used to provide PHANTOM* to the S100 bus to avoid a bus driver conflict when using memory cards which overlap the selected memory window address. Many 64k dynamic RAMs cannot disable 1K segments. IC 1F pin 3 is used to enable the data out driver, IC 4J. R13 and C15 provide approximately 120 ns. turn-on delay, allowing PHANTOM* enough time to turn any other memory off. IC 2K pin 8 indicates a bus write is about to take place. This signal pulls IWR* down indicating to the 2114's that this is a write cycle. MDI* is also asserted, which enables the data-in buffer (IC 4K). When pWR* is asserted IC 4A pin 11 goes high. Either pin 6 or 8 of IC 1K then enables a bank of 2114. The memory bank selected is determined by IA10 and IA10* applied to pins 3 and 11 of IC 1K.

IC 3C detects the on-board processor read cycle. IC 1K again provides the bank enable signal. An on-board processor write cycle is detected by one-shot OL (IWR* and IMREQ*). The output OL pin 13 is used to strobe the appropriate bank enable (through IC 1K). During this strobe IWR* is held low, indicating a write cycle for the 2114s.

2.20 WRITE PRECOMPENSATION

The Write Precompensation circuit is used advance or retard the individual write data pulses. This is done to correct for a distortion called BIT SHIFT. This bit shift is observed when reading a data stream from a diskette. Data pulses which are recorded close together, when read back, appear to spread apart. This circuit shifts the pulses being recorded in the direction opposite of the direction of this bit shift. The 1791-01 provides two signals, EARLY and LATE, which are used to advance or retard the individual data pulses. See Figure 2-13 for circuit diagram.

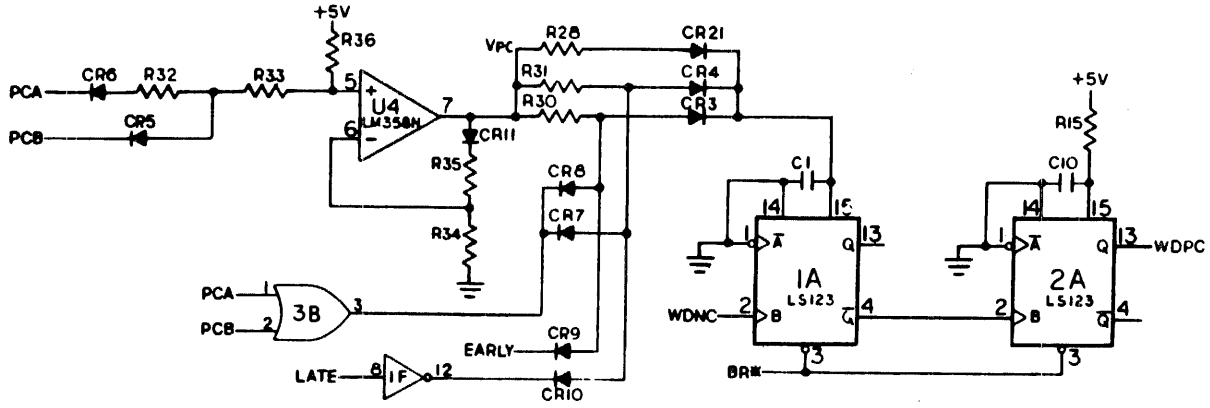


Figure 2-13. Write Precompensation Circuit

Signals PCA and PCB are used to produce three different voltage levels at U4 pin 5. This level is amplified by U4 and then used as the pull-up voltage source for one-shot 1A. R30 and R31 are individually switched by EARLY and LATE to vary the one-shot period. R28 is always in circuit. It determines the longest period. When neither EARLY nor LATE are applied, R28 and R31 in parallel determine the period. With EARLY asserted, R30 is included in parallel to provide the shortest period. The amount of precompensation applied is the difference between the normal period and either the short period or the long period. By selecting the voltage applied to the pull-up resistors, the amount of precompensation is varied. IC 3B is used to inhibit precompensation when PCA and PCB are both low.

2.21 PHASE-LOCKED LOOP

A Phased-Locked Loop is used to generate the read clock as required by the 1791-01 for data seperation. This method was selected as it provides maximum immunity to disk speed variation and provides enhanced data recovery margins in both single and double density. The loop is constructed of both digital and analog circuitry.

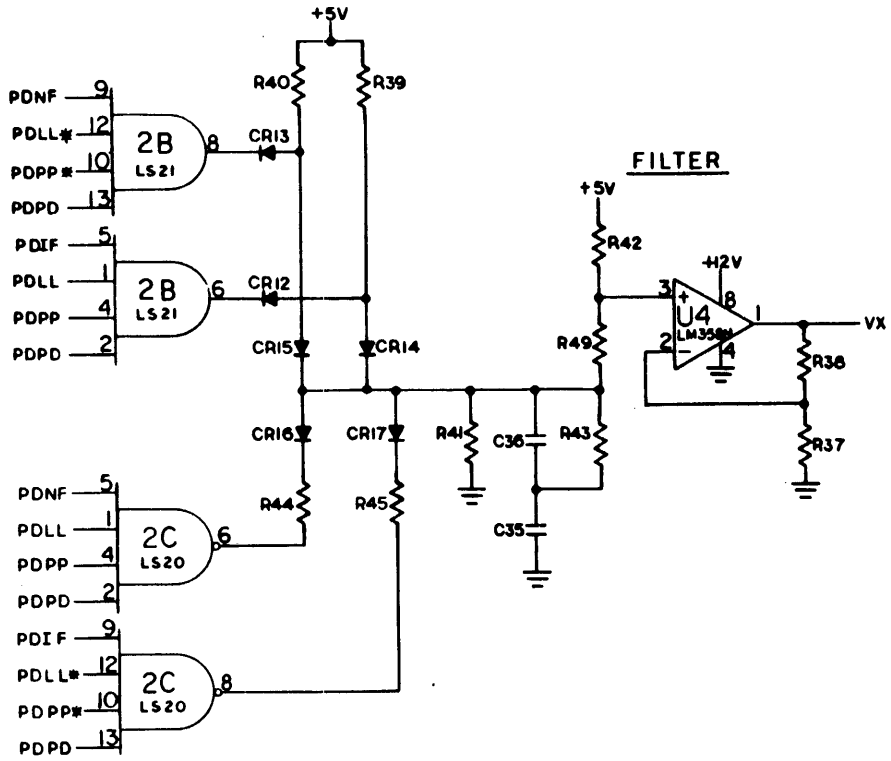


Figure 2-14. Phase Detector and Filter

The Voltage Controlled Oscillator (VCO) is a 74LS123 with both sections configured to trigger each other. The control voltage is applied to the resistors R3 and R4/5. An increase in voltage corresponds to an increase in frequency. IC 2A, a section of a 74LS123, also uses VX to provide this one-shot with a period which proportionally tracks the period of the VCO. See Figures 2-14 and 2-15.

A set of timing signals are generated from the VCO which are used by the Digital Phase Detector. IC's 1C and 3A are 74LS113s and are used to generate these signals. They are all clocked simultaneously to eliminated any skew in the generated signals.

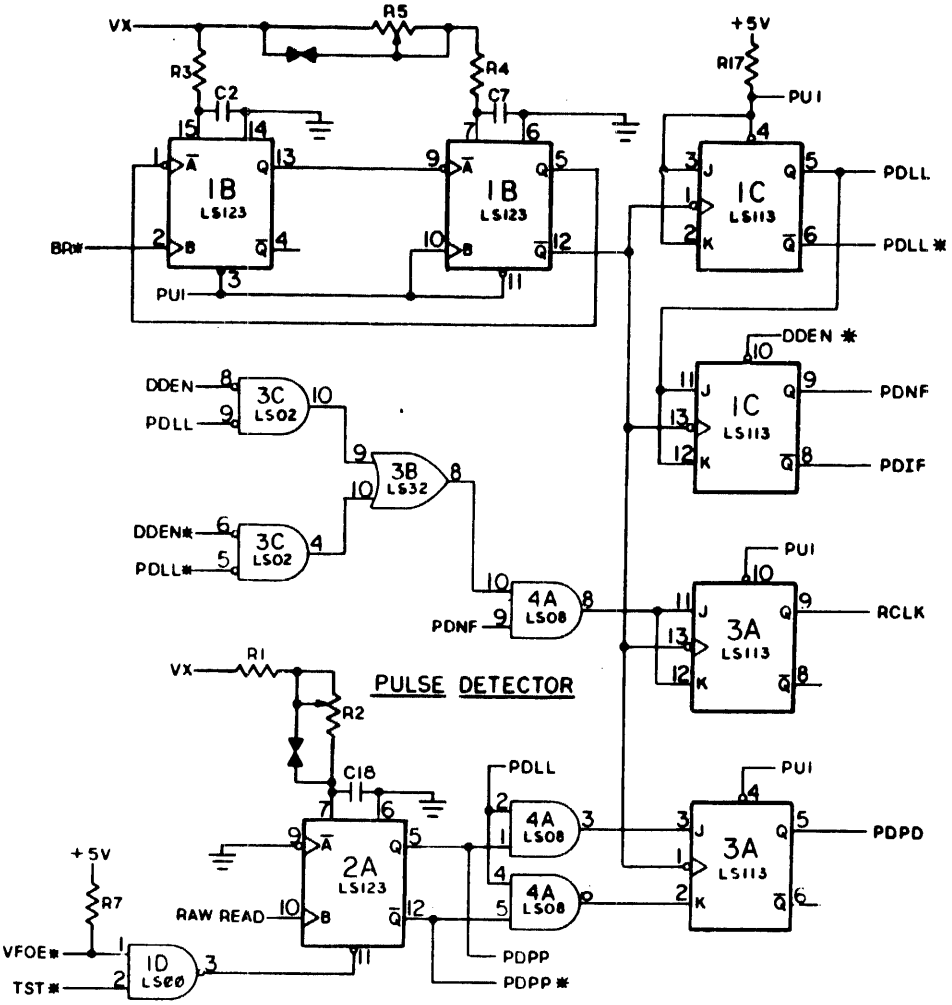


Figure 2-15. VCO and Timing Generator

In the following discussion 8 inch operation is assumed (With 5 inch operation all timings are doubled). In double density (MFM), the incoming data stream contains bits which are separated by 2, 3, or 4 microseconds (wishful thinking!). Read Clock makes a transition every 1 us. The Phase-Locked Loop adjusts the VCO such that each data pulse is centered in the middle of a half-cycle of Read Clock (Window). More precisely, due to bit-shift, very few individual data pulses are centered. They tend to occur either a little early or late but the center of the spread in these pulses is centered in the window.

The signal PDLL (Phase Detector Lead/Lag) divides the window into early and late sections. PDNF (Phase Detector Normal Frame) is always true in double density. Its complement PDIF (Phase Detector Illegal Frame) is used in single density only. In single density, when the data pulses are separated by either 2 or 4 microseconds, every other 1 us frame of the phase detector is an Illegal Frame for single density operation. RCLK (Read Clock) is generated for both FM and MFM. Sections of ICs 3C, 3B, and 4A provide this switching

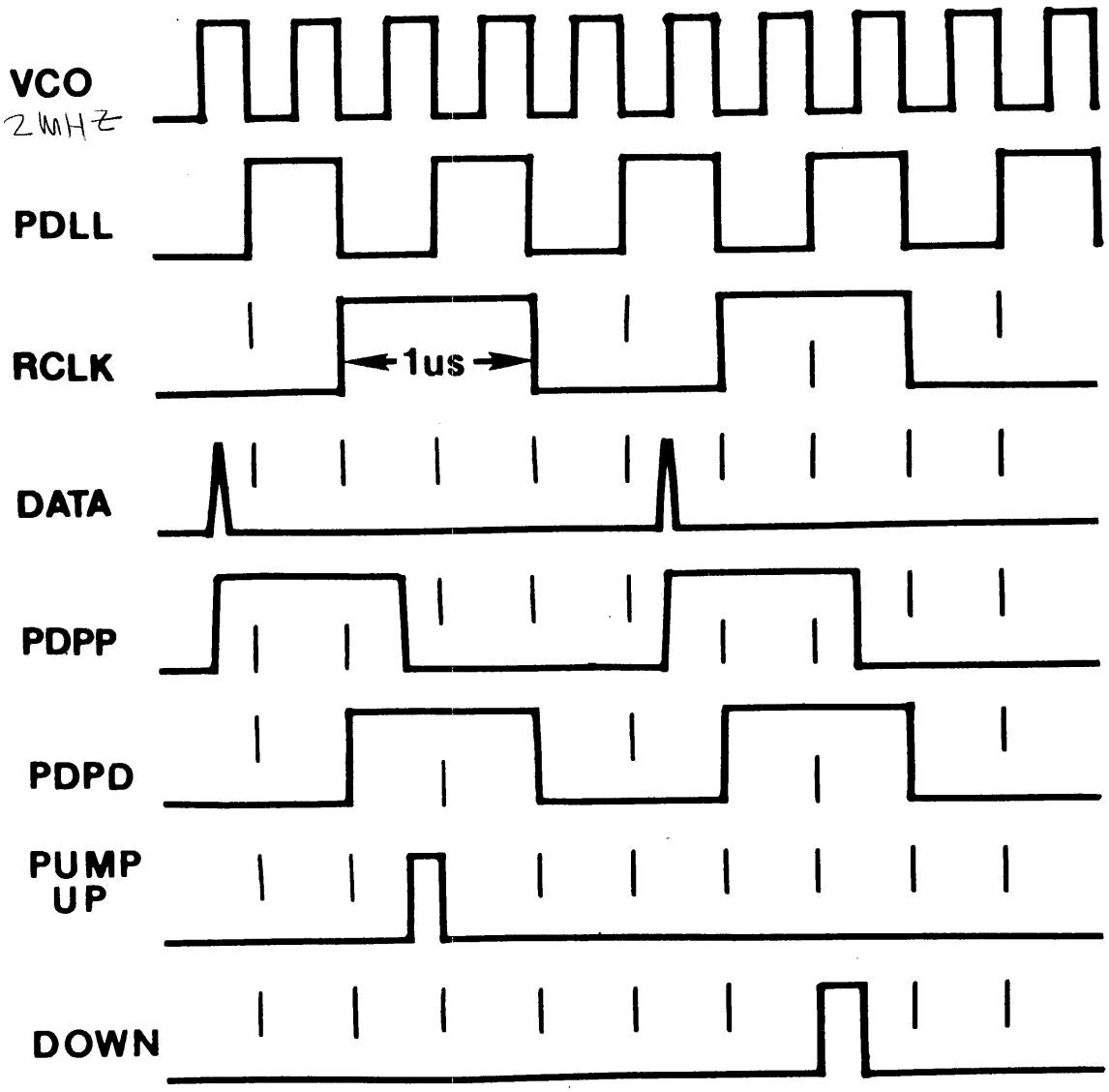


Figure 2-16. 8 Inch MFM Operation

logic. PDPD (Phase Detector Pulse Detected) indicates that during the last 1 us frame a data pulse was detected. This signal is maintained during the entire frame. PDPP (Phase Detector Pulse Present) is the output of a one-shot with a period of 1 us. It is triggered by an incoming data pulse. The falling edge of this signal ocuurs at the same place in the next frame as the data pulse occured that triggered the signal in the preceeding frame.

All these signals are used by the Phase Comparator which adjusts VX. The comparator provides Pump Up and Pump Down signals, where the period of the pump pulse is the same as the deviation of the incoming data pulse from the window's center. See Figure 2-15. This figure shows the internal phase signals, an early and late data pulse, and the corresponding pump pulses.

SECTION 3

BOARD ASSEMBLY

3.1 INTRODUCTION

If you have purchased the JADE DOUBLE D Disk Controller as a kit, we strongly urge you to read this section in its entirety before attempting to assemble the board. This board is intended for those people who have had some prior experience with digital electronics and circuit board assembly. If you do not, it is highly recommended that you find an experienced person to help you with the assembly of this board.

Although there are about as many ways of assembling a board as the number of components factorial, if you will follow the assembly instructions STEP-BY-STEP, construction will be easier for you and much more pleasurable for both of us. It will help to mark the boxes as you complete each step.

Make sure you have the tools you will need to assemble this kit. For this board you will need the following: a soldering iron (25 watts maximum), ROSIN CORE solder (preferably 63/37), diagonal cutters, a small magnifying glass, a screwdriver, a lead former or a pair of needle-nose pliers, and a small tube of heat sink compound.

3.2 ASSEMBLY

[ ] Check the parts recieved againsts the parts list. Take special care to correctly identify look-alike parts; resistors, capacitors, and diodes. If anything is missing from your kit, please call Jade's Customer Service Department and report the shortage immediately.

[ ] USE EYE PROTECTION WHILE SOLDERING OR CUTTING WIRE

[ ] When inserting IC sockets be sure to observe the pin 1 notch for proper alignment.

[ ] Install 8-pin sockets at U4 and J4. Do not solder yet.

[ ] Install 14-pin sockets at 1C, 1D, 1K, 1L, 1M, 2B, 2C, 2E, 2F, 2H, 2K, 2L, 2M, 3A, 3B, 3C, 3E, 3J, 4A, and 4B. Do not solder yet.

[ ] Install 16-pin sockets at OL, OM, 1A, 1B, 1E, 2A, 3F, 3H, and 3M. Do not solder yet.

[ ] Install 18-pin sockets at 4C, 4DL, 4DR, and 4E. Do not solder yet.

[ ] Install 20-pin sockets at 1F, 1H, 3K, 3L, 4F, 4H, 4J, 4K, 4L, and 4M. Do not solder yet.

[ ] Install 40-pin sockets at 1J and 2D. Do not solder yet.

[ ] Place the flat styrofoam cover you recieved with your kit box firmly against the component side of the board. Turn the board over, holding the flat styrofoam piece tightly against the board. Press the board down, forcing the socktes into the styrofoam. Now solder the alternating corner pins of the IC sockets to hold them in place temorarily (pins 8 and 16 on a 16-pin socket, for instance).

[ ] Turn the board over and very carefully inspect it to determine that all the IC sockets are down flat against the board. If you find any that are not down flat, melt the solder joints of the IC socket while pressing it down against the board.

[ ] Now that all IC sockets are down firmly on the board, turn the board solder side up. Make sure all IC socket pins are sticking through the holes. IC sockets are very hard to remove after they are completely soldered in. Remove any socket not installed properly, straighten the pin and re-insert.

[ ] Solder all IC pins.

NOTE: For the following steps the closest IC socket location for each part will be enclosed [IC#].

[ ] Solder in the 1N748-750 diode at CR1 (4M).

[ ] Install nine 1N270 diodes at the following locations:

[ ] CR2 (2L)	[ ] CR5 (U4)	[ ] CR6 (U4)
[ ] CR7 (1A)	[ ] CR8 (1A)	[ ] CR9 (U4)
[ ] CR10 (U4)	[ ] CR22 (U4)	[ ] CR23 (2B)

[ ] Install fourteen 1N914B diodes at the following locations:

[ ] CR3 (U4)	[ ] CR4 (U4)	[ ] CR11 (U4)
[ ] CR12 (2B)	[ ] CR13 (1B)	[ ] CR14 (U4)
[ ] CR15 (U4)	[ ] CR16 (2B)	[ ] CR17 (2B)
[ ] CR18 (3M)	[ ] CR19 (1D)	[ ] CR20 (4L)
[ ] CR21 (1B)	[ ] CR24 (1D)	

[ ] Install the 3.3K ohm 8-pin SIP resistor at RP1 (2F). Be careful to align pin 1.

[ ] Install the 10K ohm trimmers at the following locations:

[ ] R2 (1A) [ ] R5 (1B)

[ ] Be VERY CAREFUL in reading the resistor color codes as there are many different values used in this kit. If needed, use an ohm meter!

[ ] Install the 1.0K resistors (Brown-Black-Red) at the following locations:

[ ] R17 (3B) [ ] R19 (2M) [ ] R21 (3M)

[ ] Install the 4.7K resistors (Yellow-Purple-Red) at the following locations:

[ ] R8 (3A) [ ] R14 (4A) [ ] R22 (3B)
[ ] R23 (4K) [ ] R24 (4L) [ ] R25 (4M)
[ ] R27 (3A) [ ] R39 (2A) [ ] R40 (2A)

[ ] Install four 10K resistors (Brown-Black-Orange) at the following locations:

[ ] R7 (4J) [ ] R16 (3B) [ ] R18 (3C)
[ ] R36 (U4)

[ ] Install the 7.5K resistors (Purple-Green-Red) at the following locations:

[ ] R9 (0L) [ ] R15 (3A)

[ ] Install the 27K resistors (Red-Purple-Orange) at the following locations:

[ ] R20 (1A) [ ] R32 (1A) [ ] R38 (2A)

[ ] Install the 51K resistors (Green-Brown-Orange) at the following locations:

[ ] R29 (2A) [ ] R34 (U4)

[ ] Install the 30K resistors (Orange-Black-Orange) at the following locations:

[ ] R10 (0M) [ ] R35 (2A)

[ ] Install the 4.3K resistors (Yellow-Orange-Red) at the following locations:

[ ] R44 (2A) [ ] R45 (2A)

[ ] Install the 5.1K resistors (Green-Brown-Red) at the following locations:

[ ] R26 (4L) [ ] R52 (1A)

[ ] Install the 33K resistor (Orange-Orange-Orange) at R28 (1A-1B).

[ ] Install the 13K resistor (Brown-Orange-Orange) at R30 (1A).

[ ] Install the 22 ohm resistor (Red-Red-Black) at R11 (1K-2K).

[ ] Install the 240K resisttor (Red-Yellow-Yellow) at R12 (1M).

[ ] Install the 300 ohm resistor (Orange-Black-Brown) at R13 (1L-2M).

[ ] Install the 22K resistor (Red-Red-Orange) at R33 (1A).

[ ] Install the 47K resistor (Yellow-Purple-Orange) at R31 (1A)

[ ] Install the 20K resistor (Red-Black-Orange) at R37 (2A).

[ ] Install the 470K resistor (Yellow-Purple-Yellow) at R41 (2A).

[ ] Install the 390K resistor (Orange-White-Yellow) at R42 (2A).

[ ] Install the 2.4K resistor (Red-Yellow-Red) at R43 (2A).

[ ] Install the 150 ohm resistor (Brown-Green-Brown) at R46 (4M).

[ ] Install the 2.0K resistor (Red-Black-Red) at R47 (U1).

[ ] Install the 120 Ohm resistor (Brown-Red-Brown) at R48 (U1).

[ ] Install the 82K resistor (Grey-Red-Orange) at R49. (2A).

[ ] Install the 220 ohm resistor (Red-Red-Brown) at R51 (1K-1L).

[ ] Install the 2.7K resistor (Red-Purple-Red) at R53 (U1).

[ ] Install the 15 ohm 3 watt resistor (Brown-Green-Black at R54 (U2). Leave a 3/16" gap between the resistor and the PCB.

[ ] Install the 1.2K ohm resistor (Brown-Red-Red) at R50 (1L).

[ ] Install the 0.1 uf capacitors (104) at the following locations:

[ ] C3 (1C)	[ ] C5 (OM)	[ ] C11 (1B)
[ ] C13 (1E-2E)	[ ] C17 (2M)	[ ] C19 (2M)
[ ] C22 (3A-4A)	[ ] C26 (4M)	[ ] C12 (1C)
[ ] C23 (3C-4C)	[ ] C24 (3D-4D)	[ ] C25 (3E)
[ ] C28 (2C-3C)	[ ] C34 (U4)	[ ] C37 (1A)
[ ] C38 (1A)	[ ] C39 (1E)	[ ] C40 (2M)

[ ] Install the 25 pf mica capacitors at the following locations:

[ ] C2 (1B)	[ ] C4 (OL)	[ ] C7 (1A)
[ ] C10 (2A-2B)	[ ] C14 (OL-OM)	

[ ] Install the 200 pf mica capacitors at the following locations:

[ ] C6 (1A)	[ ] C9 (1L-1M)	[ ] C15 (1M)
[ ] C18 (2A)		

[ ] Install the 6.8 uf 35 volt tantalum capacitors at the following locations. Observe polarity.

[ ] C8 (4A) [ ] C31 (U1)

[ ] Install the 10 uf 10 volt (106) tantalum capacitors at C29 (4A-4B). Observe polarity.

[ ] Install the 4.7 uf 25 volt tantalum capacitors at the following locations. Observe polarity.

[ ] C32 (U1) [ ] C41 (4B)

[ ] Install the 10 pf mica capacitor at C1 (1A-1B).

[ ] Install the 47 uf 6.3 volt tantalum capacitor at C16 (1M). Observe polarity.

[ ] Install 0.022 uf (223) ceramic capacitor at C20 (3K-3L).

[ ] Install the 100 pf mica capacitor at C21 (3L-3M).

[ ] Install the 22 uf 25 volt tantalum capacitor at C27 (U3). Observe polarity.

[ ] Install the 33 pf mica capacitor at C33 (1K-1L).

[ ] Install the 0.01 uf ceramic capacitor at C35 (U4).

[ ] Install the 1000 pf mica capacitor at C36 (U4).

[ ] Install the 78M12 regulator at U1 (1A). Use the TO-5 mounting spacer.

[ ] Install the 7805 regulator at U2 (3A-4A) using the heat sink and the #6 hardware. Use the needle-nose pliers to bend the 7805 leads before mounting it. Mount the regulator on the heat sink first, then solder.

[ ] Install the 2N2907A transistors at U5 (2K-2L) and U8 (U1). Use two TO-18 spacers at this time.

[ ] Install the 2N2222A transistor at U7 (U1). Use a TO-18 spacer when mounting.

[ ] Install the 79L12 regulator at U6 (4B). Align part as shown in silkscreen.

[ ] Install the 8.000 Mhz xtal at Y1 (3L).

[ ] Install switch at S1 (3F-3H).

[ ] Insert the DOUBLE D controller card into an S100 mainframe. Turn on the power switch an check the following voltages.

[ ] U2 has +5 volt output.
[ ] U1 has +12 volt output.
[ ] U6 has -12 volt output.

[ ] THE FOLLOWING STEPS ARE FOR 8" DRIVES.

[ ] Install a 10K resistor (Brown-Black-Orange) at R1 (1A).
[ ] Install a 18K resistor (Brown-Grey-Orange) at R3 (1A).
[ ] Install a 15K resistor (Brown-Green-Orange) at R4 (1A).
[ ] Install a 6.2K resistor (Blue-Red-Red) at R6 (OL).
[ ] Install a jumper wire from "CLK" to "8" in the CLOCK SELECT BLOCK near ICs 2L-2M.

[ ] THE FOLLOWING STEPS ARE FOR 5" DRIVES.

- [ ] Install a 24K resistor (Red-Yellow-Orange) at R1 (1A).
- [ ] Install a 39K resistor (Orange-White-Orange) at R3 (1A).
- [ ] Install a 36K resistor (Orange-Blue-Orange) at R4 (1A).
- [ ] Install an 8.2K resistor (Grey-Red-Orange) at R6 (OL).
- [ ] Install a jumper wire from "CLK" to "5" in the CLOCK SELECT BLOCK near ICs 2L-2M.

[ ] For use with a 16 bit address bus install a jumper from "M" to "S" in the ADDRESS MODE JUMPER BLOCK. In this mode IC 4B is not needed.

[ ] For Use with a 24 bit address bus install a jumper from "M" to "E" in the ADDRESS MODE JUMPED BLOCK. In this mode IC 4B is required.

[ ] Insert the LM358 at U4.

[ ] Insert the 74LS00 IC at 1D.

[ ] Insert the 74LS02 IC at 3C.

[ ] Insert the 74LS04 ICs at 1L and 2F.

[ ] Insert the 7406 ICs at 1M and 2H.

[ ] Insert the 74LS08 IC at 4A.

[ ] Insert the 74LS10 IC at 2E.

[ ] Insert the 74LS20 IC at 2C.

[ ] Insert the 74LS21 IC at 2B.

[ ] Insert the 74LS27 ICs at 3E and 3J.

[ ] Insert the 74LS32 IC at 3B.

[ ] Insert the 74LS74 IC at 2L.

[ ] Insert the 74LS93 IC at 2M.

[ ] Insert the 74LS113 ICs at 1C and 3A.

[ ] Insert the 74LS123 ICs at 1A, 1B, 2A, OL, and OM.

[ ] Insert the 74LS240 ICs at 1F, 3K, and 3L.

[ ] Insert the 74LS244 ICs at 1H, 4F, 4H, 4J, 4K, and 4L.

[ ] Insert the 74LS273 IC at 4M.

[ ] Insert the 7425 ICs at 1k and 2K.

[ ] Insert the 7445 IC at 3M.

[ ] Insert the 8131 ICs at 3F and 3H.

[ ] Insert the 16-pin 150 ohm resistor pack at 1E.

[ ] Insert the Z80A microprocessor at 2D.

[ ] Insert the WD-1791-01 controller at 1J.

[ ] Insert the 2114l-3 static rams at 4C, 4DL, 4DR, and 4E.

[ ] Inspect all inserted ICs for bent pins.

[ ] Place DOUBLE D controller board in an extender board in an S100 mainframe. Open all switches in S1. Turn power switch on.

[ ] Adjust trimmer R5 for a 2.0 mhz clock signal at IC 1B pin 12. (1.0 mhz for 5" configuration)

[ ] Turn power switch off. Connect disk interface cable from controller to the disk drive. Observe pin 1 indications. Turn power switch on.

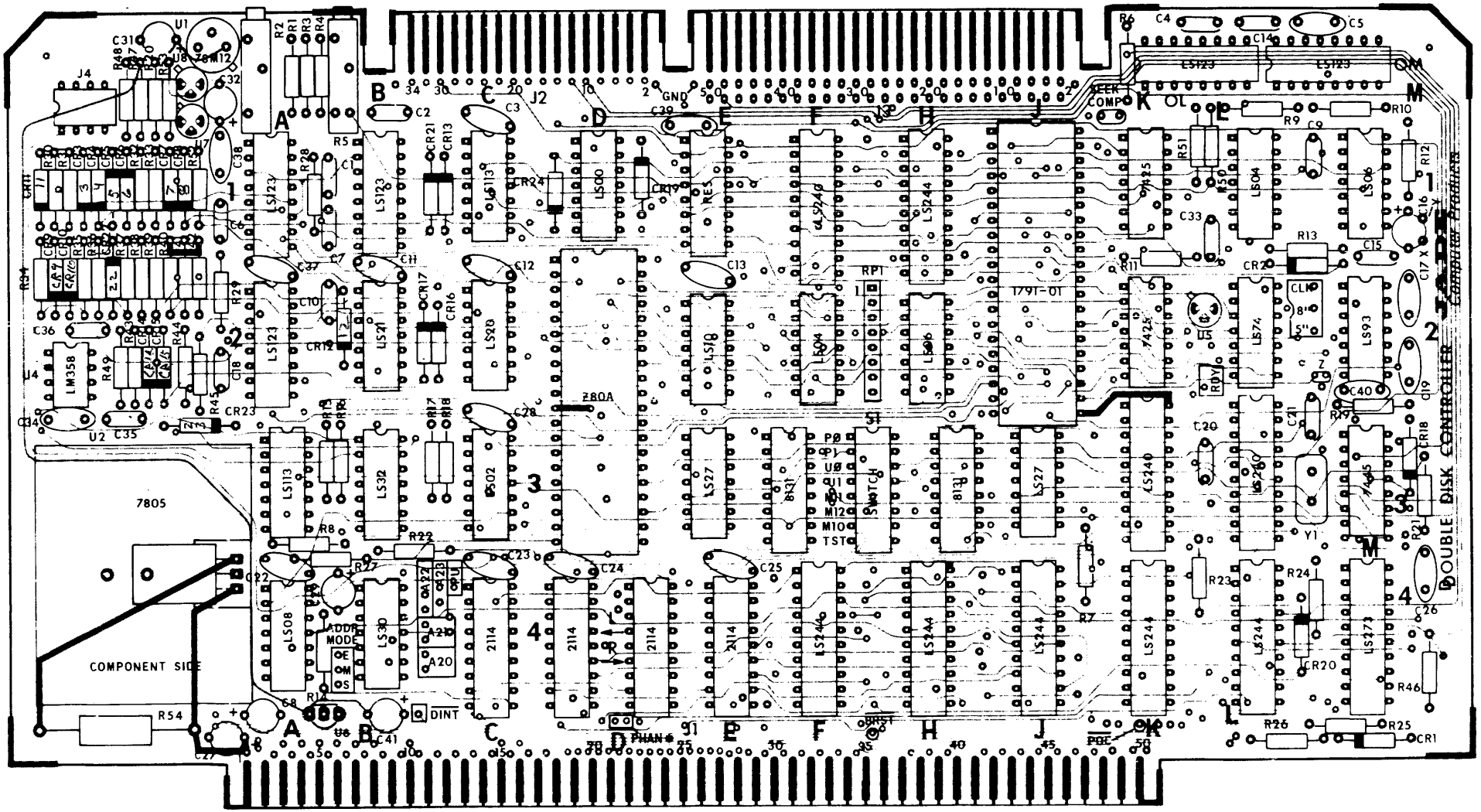
[ ] Insert a preformatted single density diskette into the drive (DRIVE 0) and close the door.

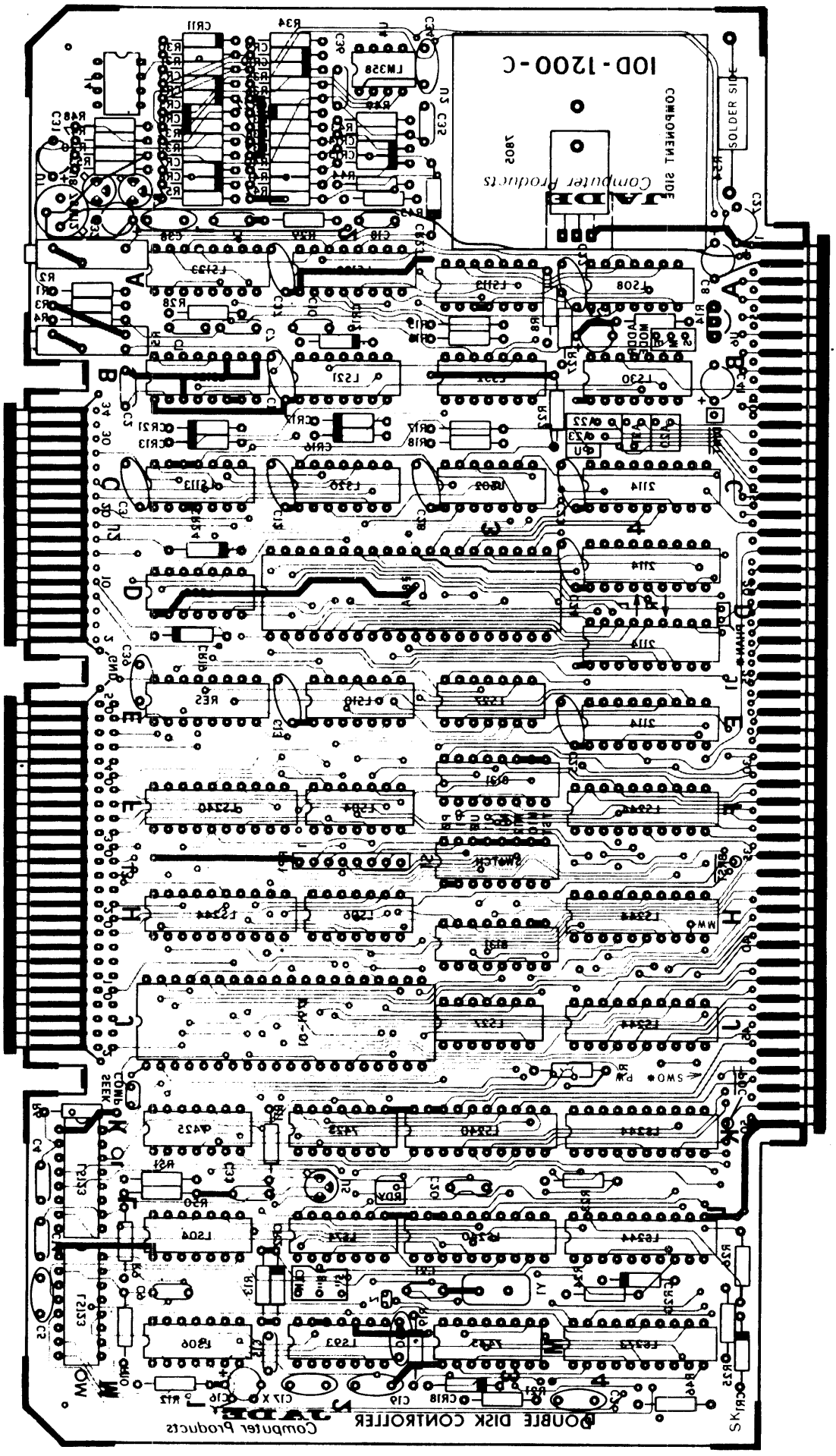
[ ] Close switch TST*. This will select drive 0, turn the motor control on, and load the head.

[ ] Adjust R2 for a 1.0 us output from one-shot 2A pin 5. (2.0 us output on 5" configuration)

[ ] Open switch TST*. Turn power switch off.

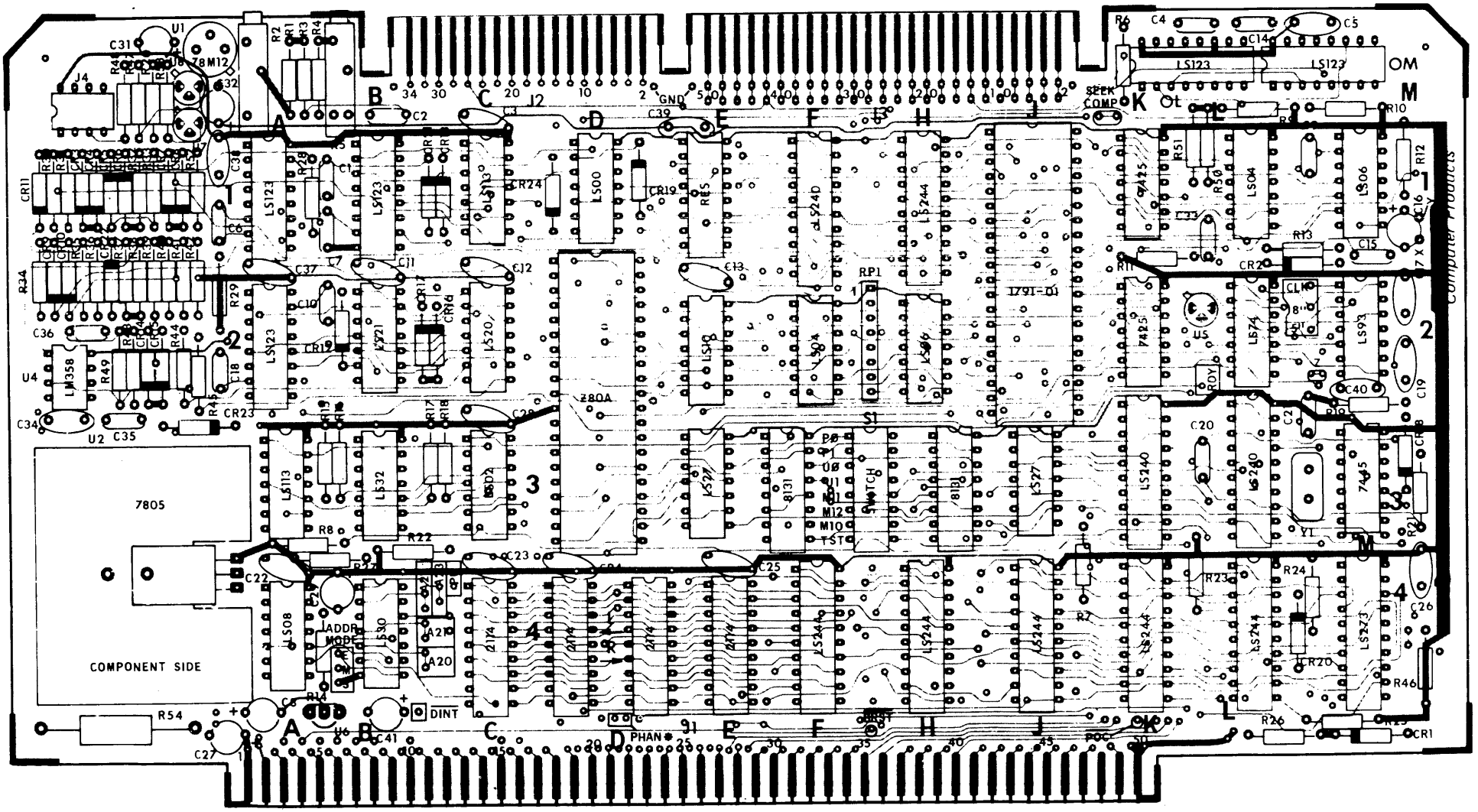
INSIDE SIGNAL LAYER

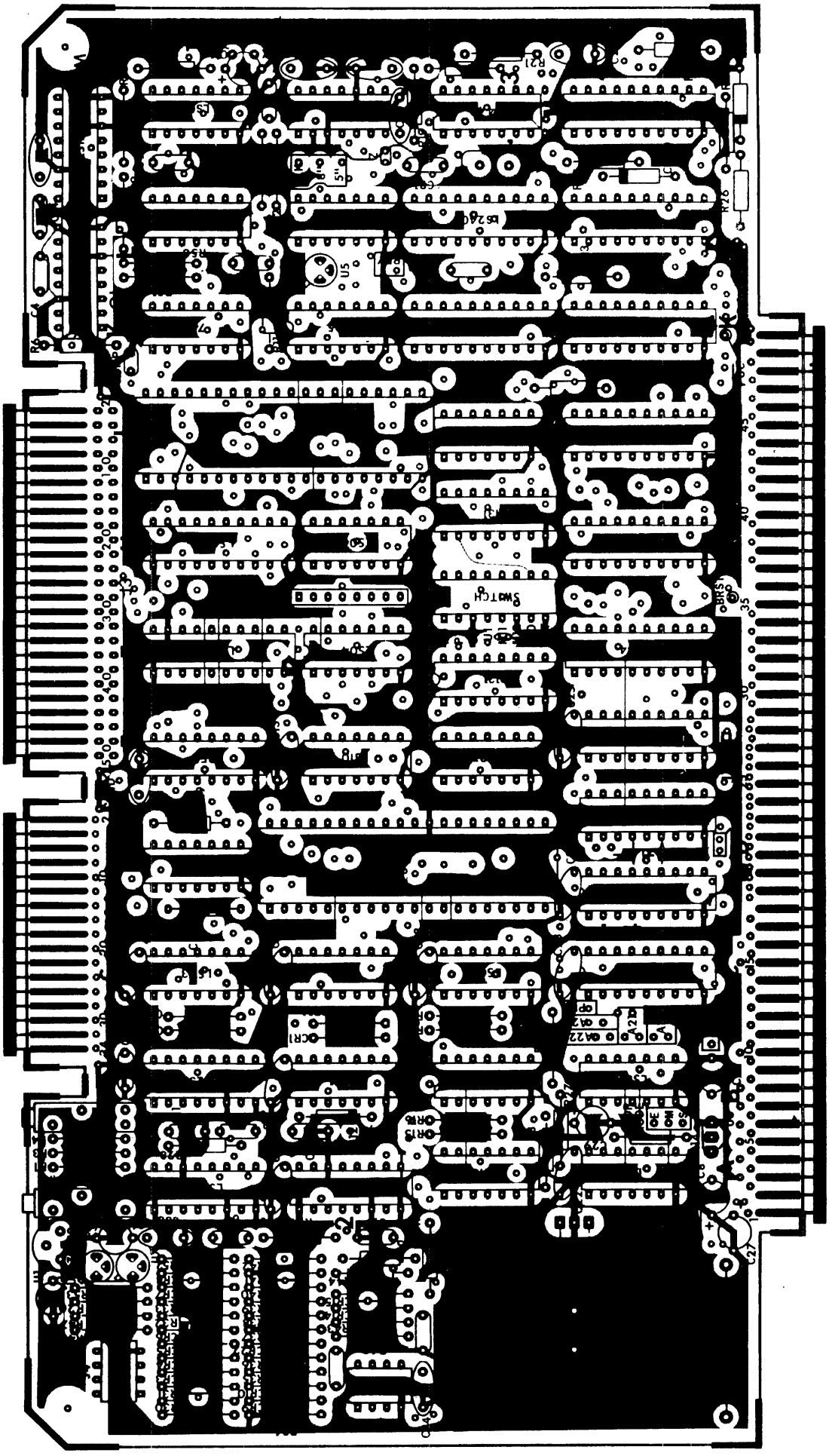



IOD-1200-C
COMPONENT SIDE
SOLDER SIDE
JADE
Computer Products
DOUBLE DISK CONTROLLER

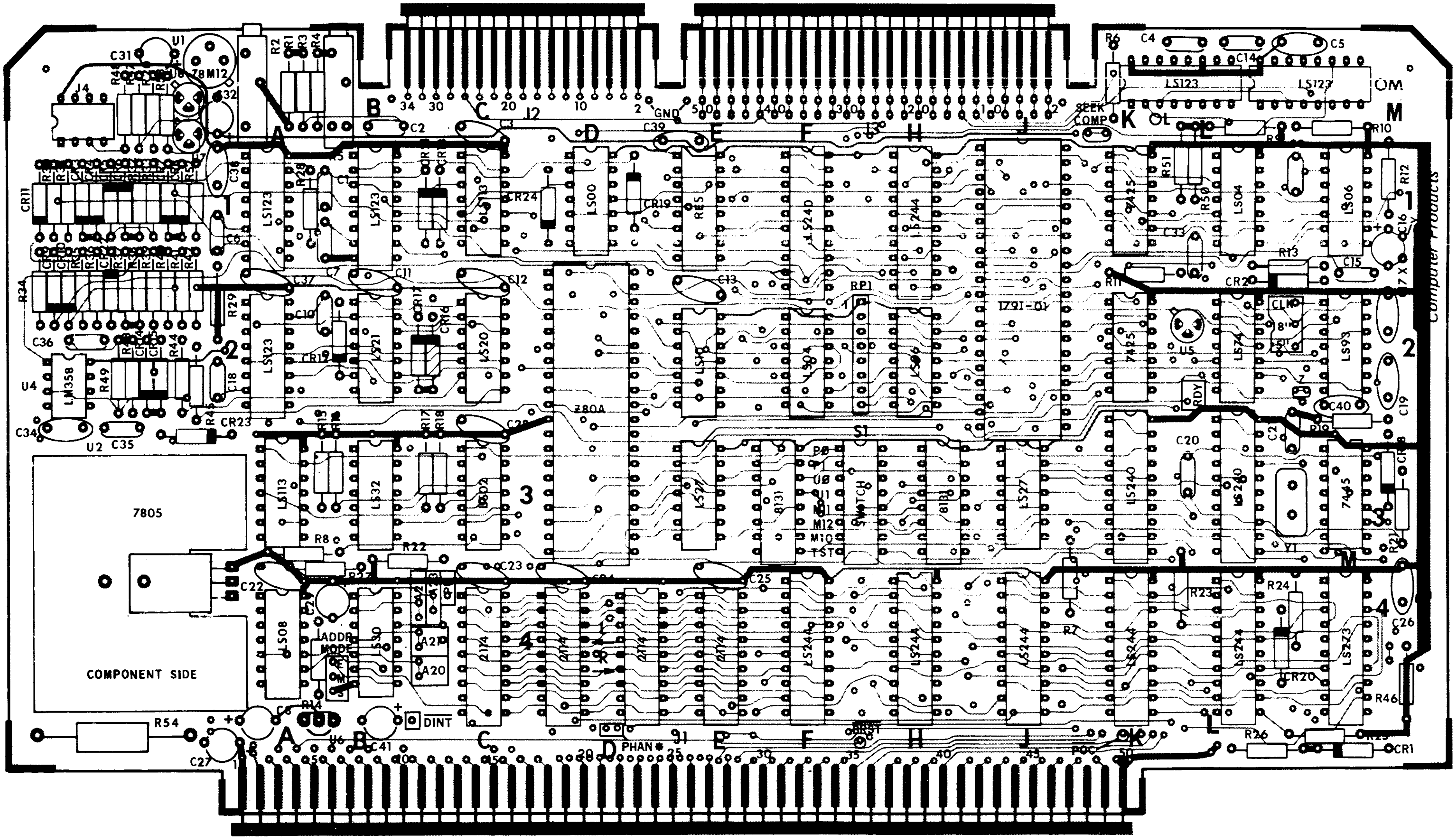
SOLDER SIDE

COMPONENT SIDE





GROUND PLANE

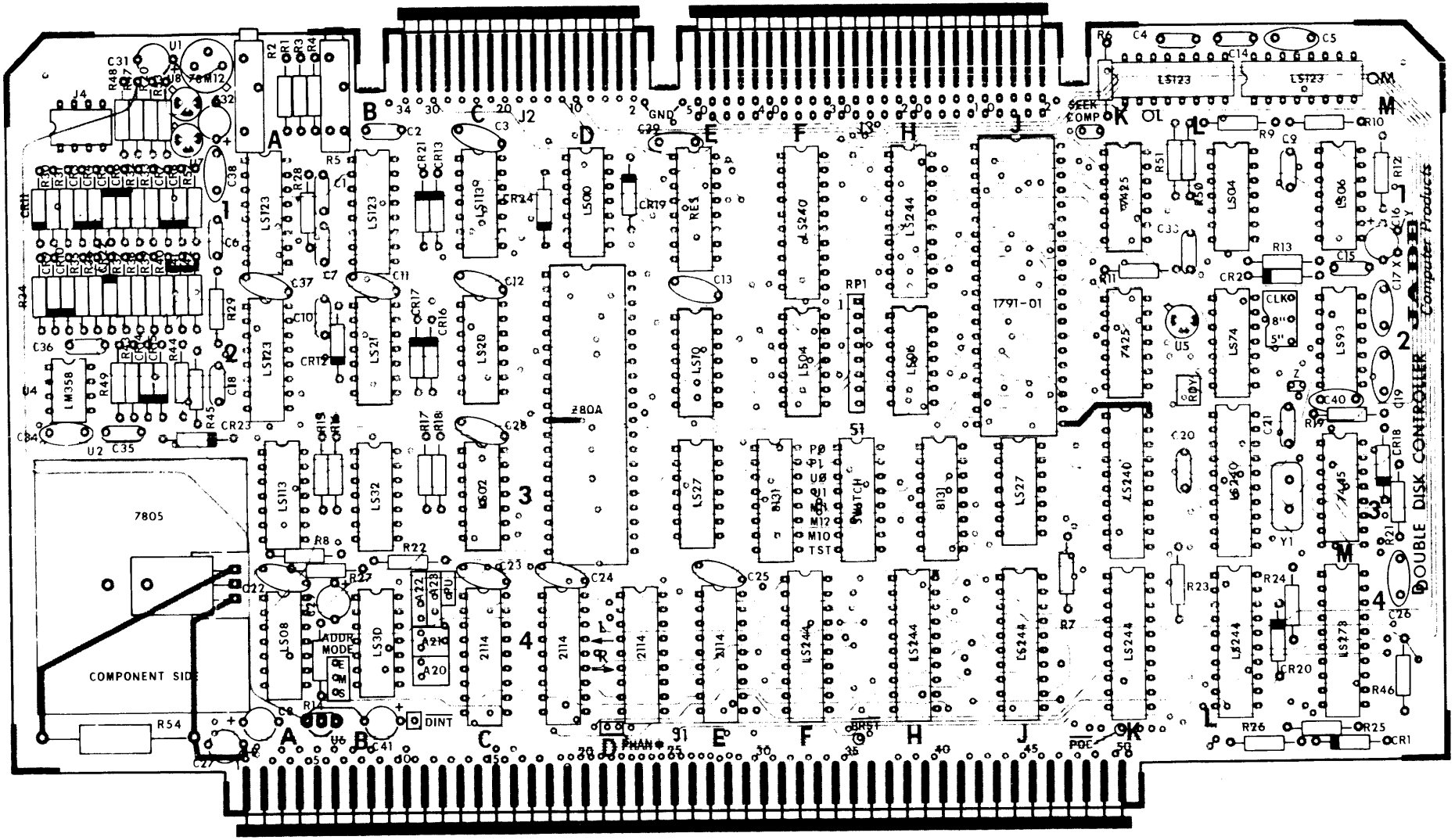


JADE
Computer Products

IOD-1200-C
SHEET 6 OF 7

REVISIONS			
LTR	DESCRIPTION	APPROVED	DATE
A	PROTOTYPE		9·79
C		DD	2·80

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON	DR BY JC	9·79	**JADE** *Computer Products*
	CHK BY		PC ARTWORK (COMP. SIDE)
	APPROVED BY		DD DISK CONTROLLER
PRINTED CIRCUIT DESIGN BY ENGINEERING TUSTIN, CALIF 92680			SIZE C · IDENT NO 10D-1200 · REV C
	NEXT USING DRAWING		SCALE 2:1 · SHEET 2 7



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IOD-1200-C
SHEET 6 OF 7

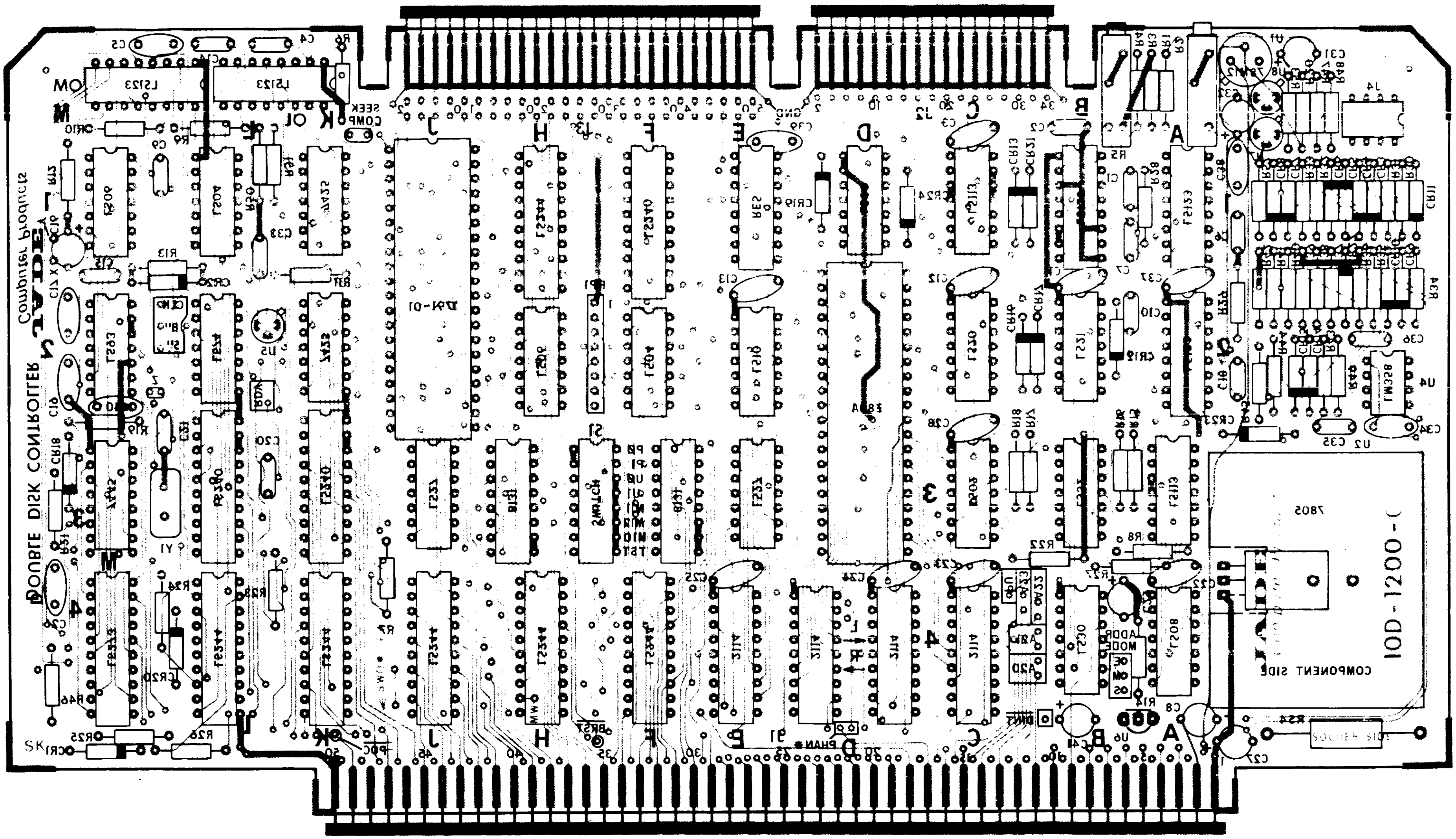
A			9-79
		DD	2-80

			9-79
	APPROVED BY		
PRINTED CIRCUIT DESIGN BY			
ENGINEERING TUSTIN CALIF 92680			

JADE
Computer Products

PC ARTWORK
DD DISK CONTROLLER

	C	IOD-1200	C
SCALE 2:1			SHEET 6 OF 7



JADE

SOLDER SIDE SHOWN

IOD-1200-C

SHEET 6 OF 7

A	PROTOTYPE 9-79
C	DD 7-80

JADE
Computer Products

PC ARTWORK (SOLDER SIDE)

DD DISK CONTROLLER

SIZE	DRAWING NO.	REV
C	IOD-1200	C

PRINTED CIRCUIT
DESIGN BY

ENGINEERING
TUSTIN CALIF 92680

APPENDIX B

PARTS LIST

RESISTORS				LOCATION-IC
R1-8"	~~10K~~ 6.8K	1/4W	5%	1A FCN #2
5"	24K	1/4w	5%	
R2	10K BOURNS	Trimmer 3006P-1-103		1A
R3-8"	~~18K~~ 12K	1/4W	5%	1A
5"	39K	1/4w	5%	
R4-8"	~~15K~~ 10K	1/4W	5%	1A FCN #2
5"	36K	1/4w	5%	
R5	10K BOURNS	Trimmer 3006P-1-103		1A
R6-8"	6.2K	1/4W	5%	OL
5"	8.2k	1/4w	5%	
R7	10K	1/4W	5%	4J-4K
R8	4.7K	1/4W	5%	3A
R9	7.5K	1/4W	5%	OL-1L
R10	30K	1/4W	5%	OM-1M
R11	22 OHM	1/4W	5%	1K-2K
R12	240K	1/4W	5%	1M
R13	300 OHM	1/4W	5%	1L-2M
R14	4.7K	1/4W	5%	4A-4B
R15	7.5K	1/4W	5%	3A-3B
R16	10K	1/4W	5%	3A-3B
R17	1.0K	1/4W	5%	3B-3C
R18	10K	1/4W	5%	3B-3C
R19	1.0K	1/4W	5%	2M-3M
R20	27K	1/4W	5%	U1
R21	1.0K	1/4K	5%	3M
R22	4.7K	1/4W	5%	3B
R23	4.7K	1/4W	5%	4K-4L
R24	4.7K	1/4W	5%	4L-4M
R25	4.7K	1/4W	5%	4M
R26	5.1K	1/4W	5%	4L
R27	4.7K	1/4W	5%	3A-3B
R28	33K	1/4W	5%	1A-1B
R29	51K	1/4W	5%	2A
R30	13K	1/4W	5%	1A
R31	47K	1/4W	5%	1A
R32	27K	1/4W	5%	1A
R33	22K	1/4W	5%	1A
R34	51K	1/4W	5%	2A

R35	30K	1/4W	5%	2A
R36	10K	1/4W	5%	2A
R37	20K	1/4W	5%	2A
R38	27K (5")	1/4W	5%	2A 20K (8") ECN #2
R39	4.7K	1/4W	5%	2A
R40	4.7K	1/4W	5%	2A
R41	470K	1/4W	5%	2A
R42	390K (5")	1/4W	5%	2A 470K (8") ECN #2
R43	2.4K (5")	1/4W	5%	2A 2.7K (8") ECN #2
R44	4.3K	1/4W	5%	2A
R45	4.3K	1/4W	5%	2A
R46	150 OHM	1/4W	5%	4M
R47	2.0K	1/4W	5%	U1
R48	120 OHM	1/4W	5%	U1
R49	82K (5")	1/4W	5%	2A JUMPER (8") ECN #2
R50	1.2K	1/4W	5%	1K-1L
R51	220 OHM	1/4W	5%	1K-1L
R52	5.1K	1/4W	5%	1A
R53	2.7K	1/4W	5%	U1
R54	15 OHM	3 Watt	10%	U2
RP1	8 PIN SIP 3.3K			

(1E) BOURNS 4116R-151
16 PIN 15 RESISTOR
150 OHMS, OR EQV.

DIODES

CR1	1N748-1N750
CR2, CR5, CR6, CR7 CR8, CR9, CR10, CR22 CR23	1N270
CR3, CR4, CR11, CR12 CR13, CR14, CR15, CR16 CR17, CR18, CR19, CR20 CR21, CR24	1N914B, 1N4448, OR EQV

MISCELLANEOUS

1 EA	8 POSITION DIP SWITCH
1 EA	AHAM-TOR #343-4PP HEAT SINK
2 EA	#6 SCREW, NUT, AND WASHER
1 EA	8.000 MHZ XTAL, Y1
1 EA	8 PIN DIP PLUG AND COVER
1 EA	TO-5 SPACER
3 EA	TO-18 SPACER
1 EA	PRINTED CIRCUIT BOARD
1 EA	HARDWARE MANUAL IOD-1200M

CAPACITORS		LOCATIONS
C1	10 PF 5% MICA	1A-1B
C2	25 PF 5% MICA	1B
C3	0.1 UF MONOLYTHIC	1C
C4	25 PF 5% MICA	OL
C5	0.1 UF MONOLYTHIC	OM
C6	200 PF 5% MICA	1A
C7	25 PF 5% MICA	1A-1B
C8	6.8 UF 35V DIPPED TANT.	4A
C9	200 PF 5% MICA	1L-1M
C10	25 PF 5% MICA	2A-2B
C11	0.1 UF MONOLYTHIC	1B-2B
C12	0.1 UF MONOLYTHIC	1C-2C
C13	0.1 UF MONOLYTHIC	1E-2E
C14	25 PF 5% MICA	OL-OM
C15	200 PF 5% MICA	1M
C16	47 UF 6.3V DIPPED TANT.	1M
C17	0.1 UF MONOLYTHIC	2M
C18	200 PF 5% MICA	2A
C19	0.1 UF MONOLYTHIC	2M
C20	0.022 UF CERAMIC 10%	3K-3L
C21	100 PF 5% MICA	3L-3M
C22	0.1 UF MONOLYTHIC	3A-4A
C23	0.1 UF MONOLYTHIC	3C-4C
C24	0.1 UF MONOLYTHIC	3D-4D
C25	0.1 UF MONOLYTHIC	3E-4E
C26	0.1 UF MONOLYTHIC	4M
C27	22 UF 25V DIPPED TANT.	U3
C28	0.1 UF MONOLYTHIC	2C-3C
C29	10 UF 10V DIPPED TANT.	4A-4B
C30	(DELEATED)	
C31	6.8 UF 35V DIPPED TANT.	U1
C32	4.7 UF 25V DIPPED TANT.	U6
C33	33 PF 5% MICA	1K-1L
C34	0.1 UF MONOLYTHIC	U4
C35	0.01 UF 10% CERAMIC	U4
C36	1000 PF MICA 5%	U4
C37	0.1 UF MONOLYTHIC	1A-2A
C38	0.1 UF MONOLYTHIC	1A
C39	0.1 UF MONOLYTHIC	1E
C40	0.1 UF MONOLYTHIC	2M
C41	4.7 UF 25V DIPPED TANT.	4B

DIGITAL CIRCUITS

(1A)	74LS123	(2A)	74LS123	(3A)	74LS113	(4A)	74LS08
(1B)	74LS123	(2B)	74LS21	(3B)	74LS32	(4B)	74LS30
(1C)	74LS113	(2C)	74LS20	(3C)	74LS02	(4C)	2114-3L
(1D)	74LS00	(2D)	Z80A			(4DL)	2114-3L
						(4DR)	2114-3L
(1E)	RES-PK	(2E)	74LS10	(3E)	74LS27	(4E)	2114-3L
(1F)	74LS240	(2F)	74LS04	(3F)	8131	(4F)	74LS244
(1H)	74LS244	(2H)	7406	(3H)	8131	(4H)	74LS244
(1J)	1791-01			(3J)	74LS27	(4J)	74LS244
(1K)	7425	(2K)	7425	(3K)	74LS240	(4K)	74LS244
(1L)	74LS04	(2L)	74LS74	(3L)	74LS240	(4L)	74LS244
(1M)	7406	(2M)	74LS93	(3M)	7445	(4M)	74LS273
(OL)	74LS123	(OM)	74LS123				

ANALOG CIRCUITS

(U1)	78M12	(TO-5)
(U2)	7805	(TO-220)
(U3)	*DELEATED*	
(U4)	LM358	(8-PIN DIP)
(U5)	2N2907	(TO-18)
(U6)	79L12	(TO-92)
(U7)	2N2222	(TO-18)
(U8)	2N2907	(TO-18)

SOCKETS

8 PIN DIP SOCKET	2 EA
14 PIN DIP SOCKET	20 EA
16 PIN DIP SOCKET	9 EA
18 PIN DIP SOCKET	4 EA
20 PIN DIP SOCKET	10 EA
40 PIN DIP SOCKET	2 EA

APPENDIX C

INTERNAL SIGNAL DEFINITIONS

BCPS	BOARD - CONTROL PORT STROBE
BDBIN	BUS - DATA BUS IN
BDI*	BOARD - DATA IN
BLSTB	BOARD - FUNCTION STROBE
BMA*	BOARD - MEMORY ADDRESSED
BMA	BOARD - PORT ADDRESSED
BMEMR	BUS - MEMORY READ
BR*	BOARD - RESET
BPWR	BUS - PROCESSOR WRITE
BSINP	BUS - STATUS INPUT
BSOUT	BUS STATUS OUTPUT
BSWO	BUS STATUS WRITE OUT
CHNG*	DISK CHANGED
DCLK	1791-01 CLOCK
DCRE*	1791-01 READ ENABLE
DCWE*	1791-01 WRITE ENABLE
DDEN	DOUBLE DENSITY ENABLE
DDIN*	1791-01 DISK DATA IN
DDRQ	1791-01 DATA REQUEST
DINT	1791-01 INTERRUPT REQ
DSA	DRIVE SELECT A
DSB	DRIVE SELECT B
DSE	DRIVE SELECT ENABLE
IAnn	INTERNAL ADDRESS BIT nn
IIORQ*	INTERNAL Z80A I/O REQ
ILP*	ILLEGAL PACK
IMREQ*	INTERNAL Z80A MEM REQ
IRD*	INTERNAL Z80A READ CYCLE
IWR*	INTERNAL Z80A WRITE CYCLE
MDI*	MEMORY DATA IN
MDO*	MEMORY DATA OUT
MSH*	MEMORY SELECT HIGH
MSL*	MEMORY SELECT LOW
PCA	PRECOMP SELECT A
PCB	PRECOMP SELECT B
PDIF	PHASE DETECT ILLEGAL FRAME
PDLL	PHASE DETECT LEAD/LAG
PDNF	PHASE DETECT NORMAL FRAME
PDPD	PHASE DETECT PULSE DETECTED
PDPP	PHASE DETECT PULSE PRESENT

RCLK	1791-01 READ WINDOW
SA11	ADDRESS SWITCH M11
SA12	ADDRESS SWITCH M12
SERI	TTL LEVEL OF EIA IN
SERO	TTL LEVEL OF EIA OUT
SID1	SIDE 1 SELECT
SLVACK*	MEM TRANSFER ACK
SLVREQ*	MEM TRANSFER REQ
TOFF	TIMER OFF
TST*	TEST PLL
VFOE*	PHASE LOCK LOOP ENABLE
VPC	PRECOMP INTENSITY
VX	LOOP OSC VOLTAGE
WDNC	WRITE DATA NOT COMPENSATED
WDPC	WRITE DATA PRECOMPENSATED
ZCLK	Z80A CLOCK
ZHLD*	Z80A WAIT REQUEST
ZINT*	Z80A INTERRUPT REQ
ZNMI*	Z80A N.M.INTERRUPT REQ
ZRST*	Z80A RESET

APPENDIX D

S-100 BUS CONNECTIONS

PIN #	SIGNAL	FUNCTION	PIN#	SIGNAL	FUNCTION
1	+8 volts	Power	51	+8 VOLTS	Power
2	+16 volts	Power	52	-16 VOLTS	Power
4	VI0*	Interrupt	53	GND	Ground
5	VI1*	Interrupt	54	SLAVE CLR*	A Reset
6	VI2*	Interrupt	59	A19	Extd Addr
7	VI3*	Interrupt	61	A20	Extd Addr
8	VI4*	Interrupt	62	A21	Extd Addr
9	VI5*	Interrupt	63	A22	Extd Addr
10	VI6*	Interrupt	64	A23	Extd Addr
11	VI7*	Interrupt	67	PHANTOM*	Dsble Slaves
15	A18	Ext Addr	70	GND	Ground
16	A16	Ext Addr	77	pWR	Processor Sig
17	A17	Ext Addr	78	pDBIN	Processor Sig
20	GND	Ground	79	A0	Address 0
29	A5	Address 5	80	A1	Address 1
30	A4	Address 4	81	A2	Address 2
31	A3	Address 3	82	A6	Address 6
32	A15	Address 15	83	A7	Address 7
33	A12	Address 12	84	A8	Address 8
34	A9	Address 9	85	A13	Address 13
35	DO1	Data Out 1	86	A14	Address 14
36	DO0	Data Out 0	87	A11	Address 11
37	A10	Address 10	88	DO2	Data Out 2
38	DO4	Data Out 4	89	DO3	Data Out 3
39	DO5	Data Out 5	90	DO7	Data Out 7
40	DO6	Data Out 6	91	DI4	Data In 4
41	DI2	Data In 2	92	DI5	Data In 5
42	DI3	Data In 3	93	DI6	Data In 6
43	DI7	Data In 7	94	DI1	Data In 1
45	sOUT	Status Out	95	DI0	Data In 0
46	sIN	Status In	97	sW0	Write Out
47	sMEMR	Stat Mem Rd	99	POC*	Power On Rst
50	GND	Ground	100	GND	Ground

WESTERN DIGITAL
C O R P O R A T I O N

FD 179X-02 Floppy Disk Formatter/Controller Family

MAY 1980

FEATURES

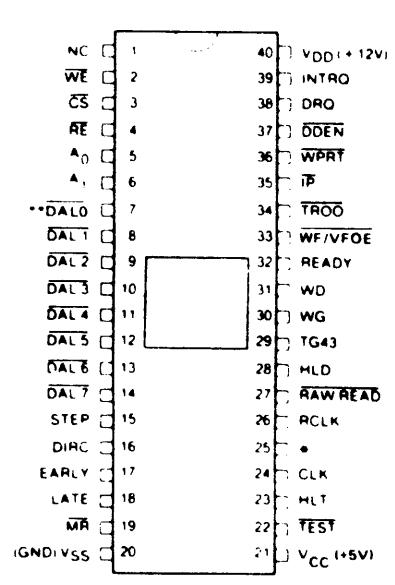
- TWO VFO CONTROL SIGNALS
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable length Sector
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1793	1795	1797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Write Precomp	X	X	X	X
Side Selection Output			X	X

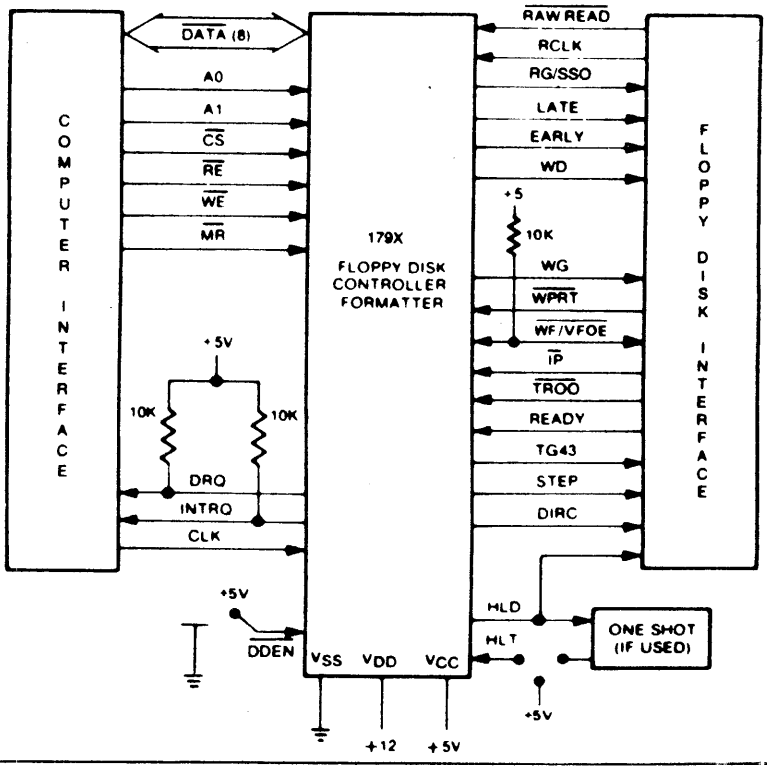
APPLICATIONS

FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/ FORMATTER
NEW MINI-FLOPPY CONTROLLER



*1791/3 = RG 1795/7 = SSO
**1793/7 TRUE BUS

PIN CONNECTIONS



FD179X SYSTEM BLOCK DIAGRAM

GENERAL DESCRIPTION

The FD179X are MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bidirectional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793. On these devices, DDEN must be left open.

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	MASTER RESET	$\overline{MR}$	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
40		V_{DD}	+12V ±5%
COMPUTER INTERFACE:			
2	WRITE ENABLE	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	CHIP SELECT	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	READ ENABLE	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 Status Reg Command Reg 0 1 Track Reg Track Reg 1 0 Sector Reg Sector Reg 1 1 Data Reg Data Reg
7-14	DATA ACCESS LINES	$\overline{DAL0}$-$\overline{DAL7}$	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{WE}$ or transmitter enabled by $\overline{RE}$
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for mini-drives.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged.
25	READ GATE (1791/3)	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S = 1, SSO is set to a logic 1. When S = 0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$ VFO ENABLE	$\overline{\text{WF}}$/VFOE	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD179X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the FD179X when the index hole is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected. This line must be left open on the 1792/4

ORGANIZATION

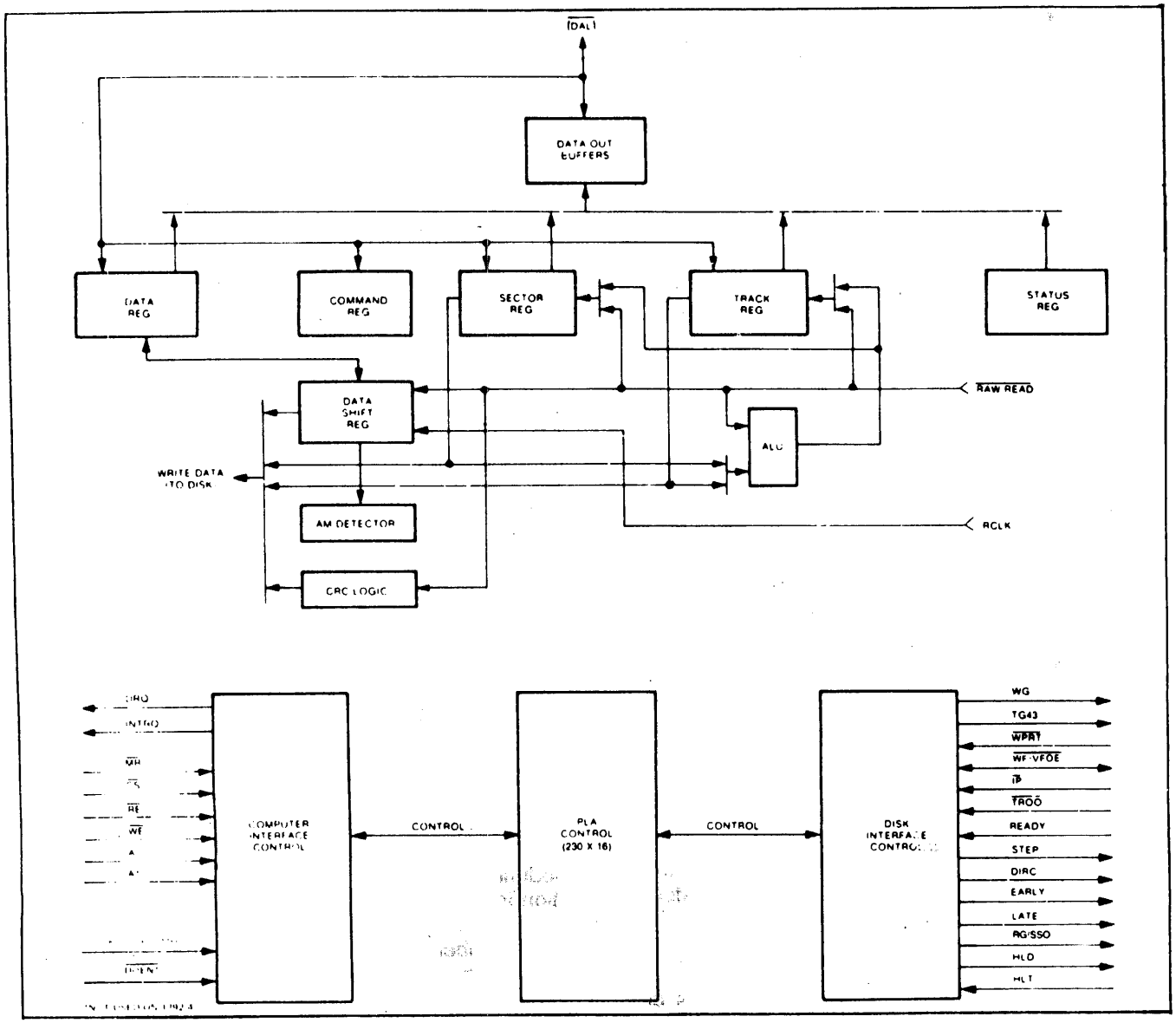
The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register—This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.



FD179X BLOCK DIAGRAM

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1791/3 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN}$ = 0 double density (MFM) is assumed. When $\overline{DDEN}$ = 1, single density (FM) is assumed.

AM Detector—The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD179X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The 179X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

HEAD POSITIONING

Five commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step—A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

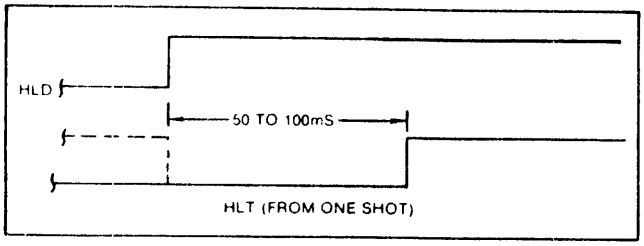
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

Table 1. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1	X	X
R1 R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0 0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0 1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1 0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1 1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{\text{DDEN}}$ should be placed to logical "1." For MFM formats, $\overline{\text{DDEN}}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table.)

For read operations, the FD179X requires $\overline{\text{RAW READ}}$ Data (Pin 27) signal which is a 250 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM. RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{\text{VFOE}}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{\text{VFOE}}$ will go active when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{\text{WF}}/\overline{\text{VFOE}}$ is not used, leave open or tie to a 10K resistor to +5.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{\text{Write Protect}}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the $\overline{\text{Write Fault}}$ bit (bit 5) in the Status Word. The $\overline{\text{Write Fault}}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{\text{DDEN}}$ = 1) and 250 ns pulses in MFM ($\overline{\text{DDEN}}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

Table 2. COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	F_2	E	F_1	0
II	Write Sector	1	0	1	m	F_2	E	F_1	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrrupt	1	1	0	1	I_3	I_2	I_1	I_0

Note: Bits shown in TRUE form.

Table 3. FLAG SUMMARY

TYPE I COMMANDS

h = Head Load Flag (Bit 3)

h = 1, Load head at beginning
h = 0, Unload head at beginning

V = Verify flag (Bit 2)

V = 1, Verify on destination track
V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)

u = 1, Update Track register
u = 0, No update

Table 4. FLAG SUMMARY

TYPE II & III COMMANDS

m = Multiple Record flag (Bit 4)

m = 0, Single Record
m = 1, Multiple Records

a_0 = Data Address Mark (Bit 0)

a_0 = 0, FB (Data Mark)
a_0 = 1, F8 (Deleted Data Mark)

E = 15 ms Delay (2MHz)

E = 1, 15 ms delay
E = 0, no 15 ms delay

(F_2) S = Side Select Flag (1791/3 only)

S = 0, Compare for Side 0
S = 1, Compare for Side 1

(F_1) C = Side Compare Flag (1791/3 only)

C = 0, disable side select compare
C = 1, enable side select compare

(F_1) S = Side Select Flag

(Bit 1, 1795/7 only)

S = 0 Update SSO to 0
S = 1 Update SSO to 1

(F_2) b = Sector Length Flag

(Bit 3, 1975/7 only)

	Sector Length Field			
	00	01	10	11
b = 0	256	512	1024	128
b = 1	128	256	512	1024

Table 5. FLAG SUMMARY

TYPE IV COMMAND

Ii = Interrupt Condition flags (Bits 3-0)

I0 = 1, Not-Ready to Ready Transition
I1 = 1, Ready to Not-Ready Transition
I2 = 1, Index Pulse
I3 = 1, Immediate Interrupt
I_3 -I_0 = 0, Terminate with no Interrupt

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1.

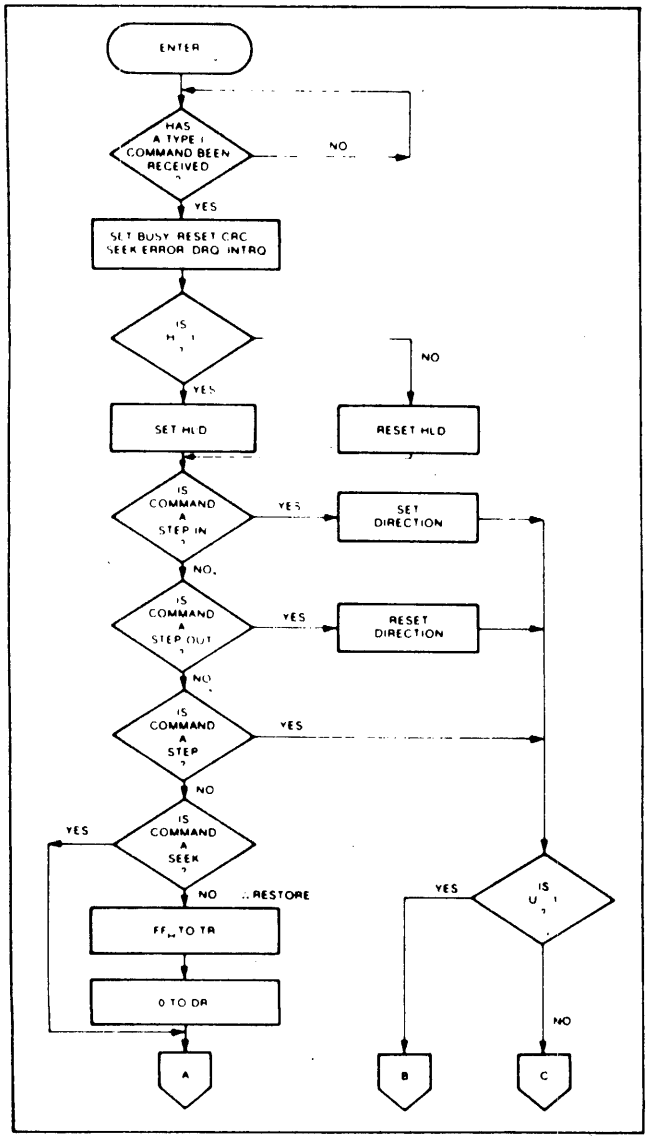
The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD179X receives a command that specifically disengages the head. If the FD179X is idle (busy = 0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

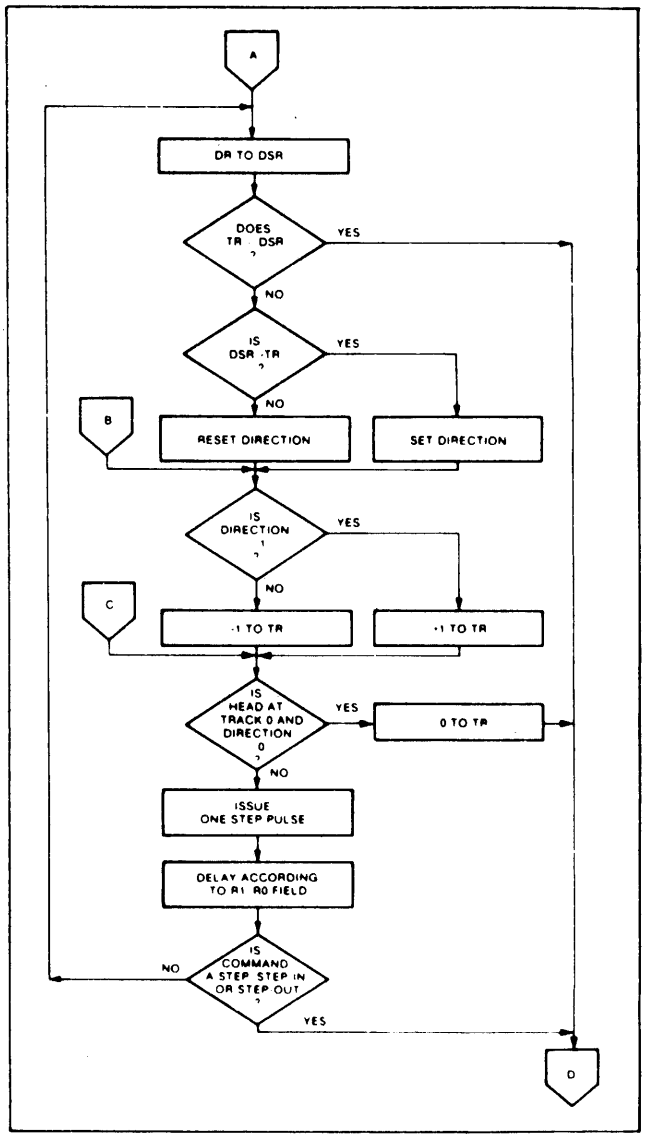
During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FD179X terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.



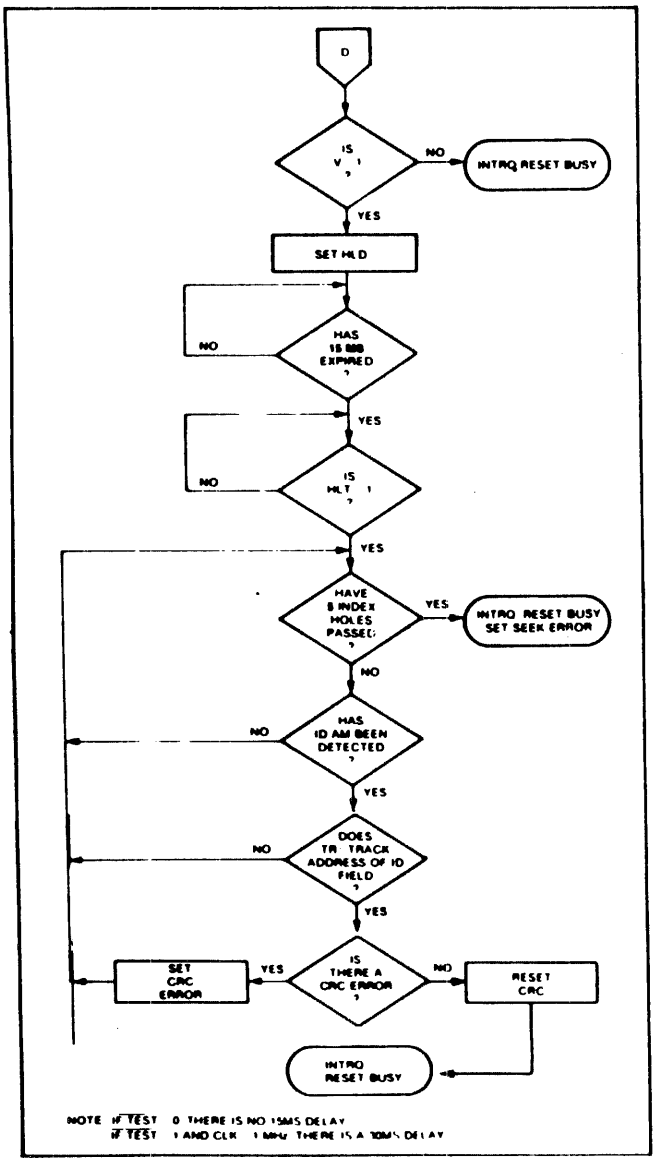
TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r1r0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state.



TYPE I COMMAND FLOW

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

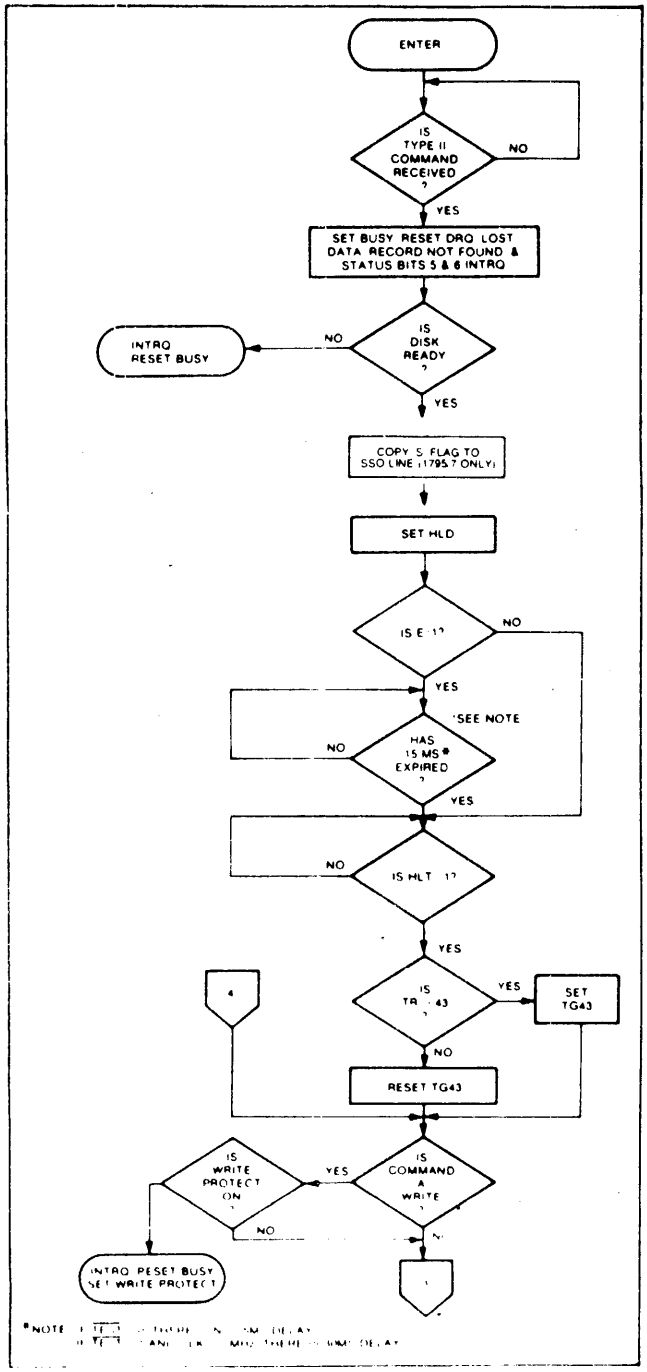
The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next en-

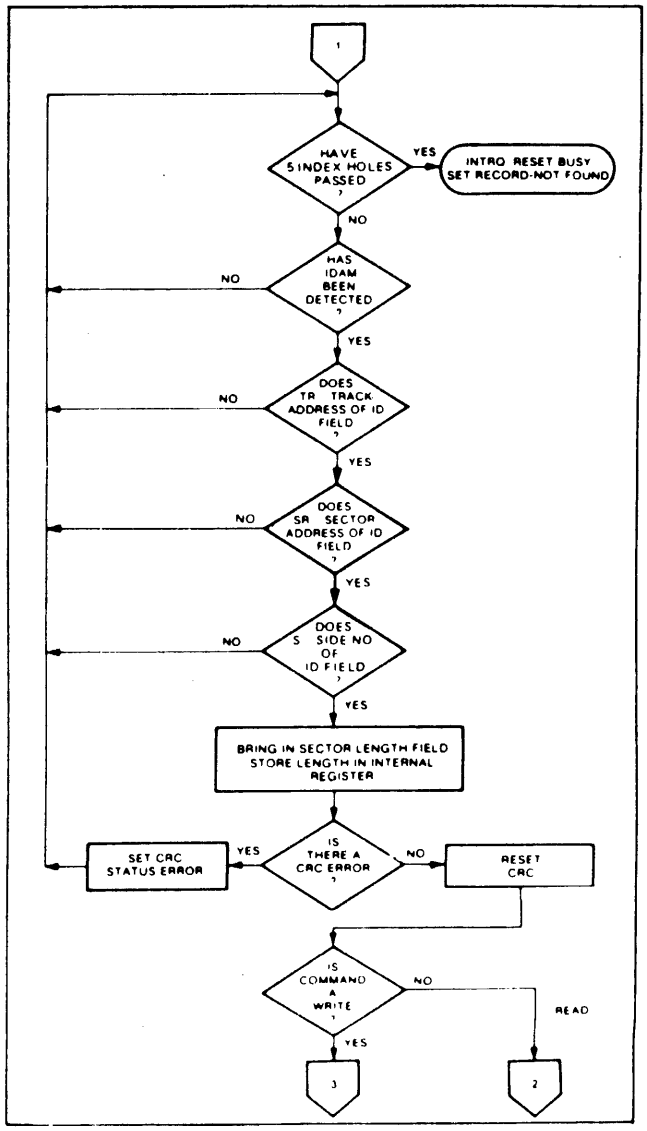
countered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

Sector Length Table	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD179X will continue to read or write multiple records and update the sector register until the sector regis-



TYPE II COMMAND



TYPE II COMMAND

ter exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

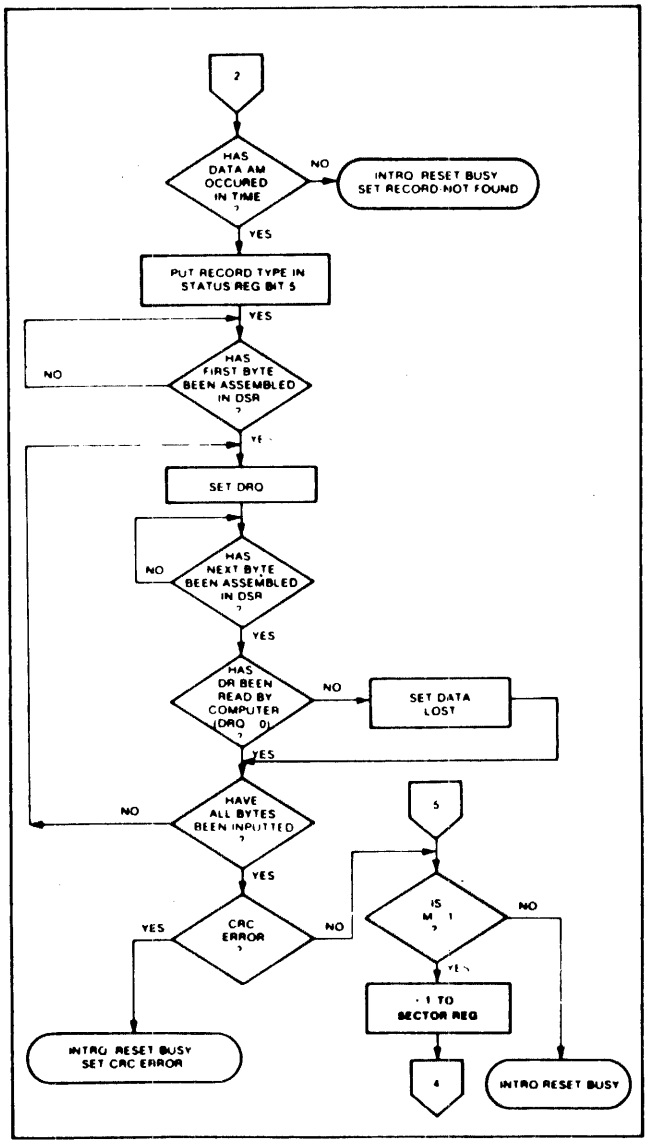
The Type II commands also contain side select compare flags. When C = 0, no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'b' flag. The 'b' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'b' flag should be set to a one. The 's' flag allows direct control over the SSO Line (Pin 25) and is set or reset at the beginning of the command, dependent upon the value of this flag.

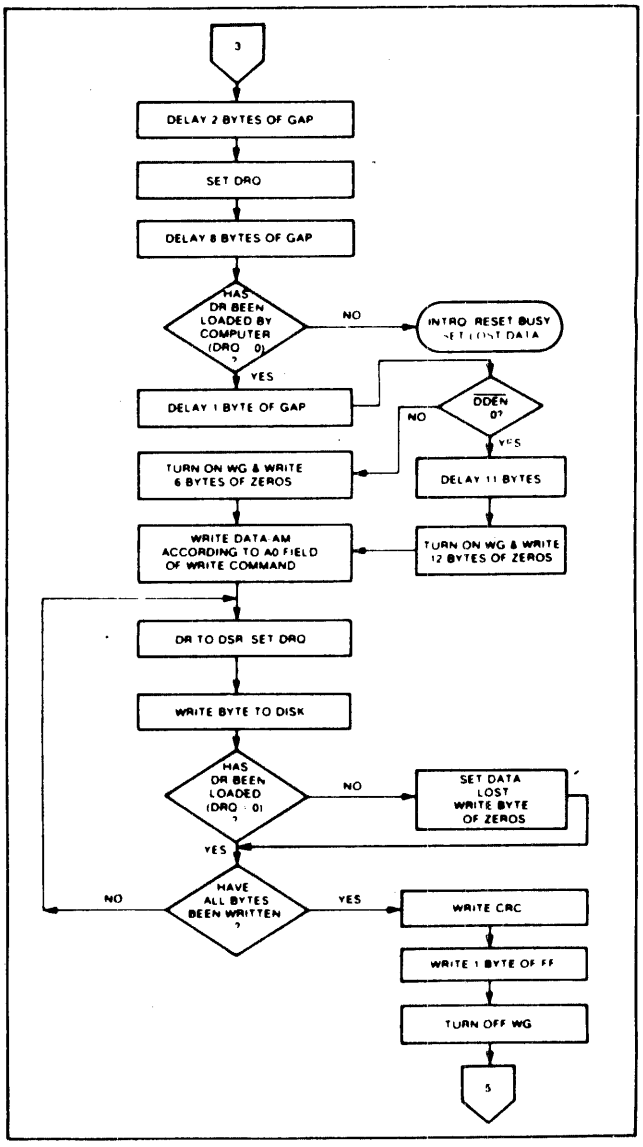
READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and



TYPE II COMMAND



TYPE II COMMAND

the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

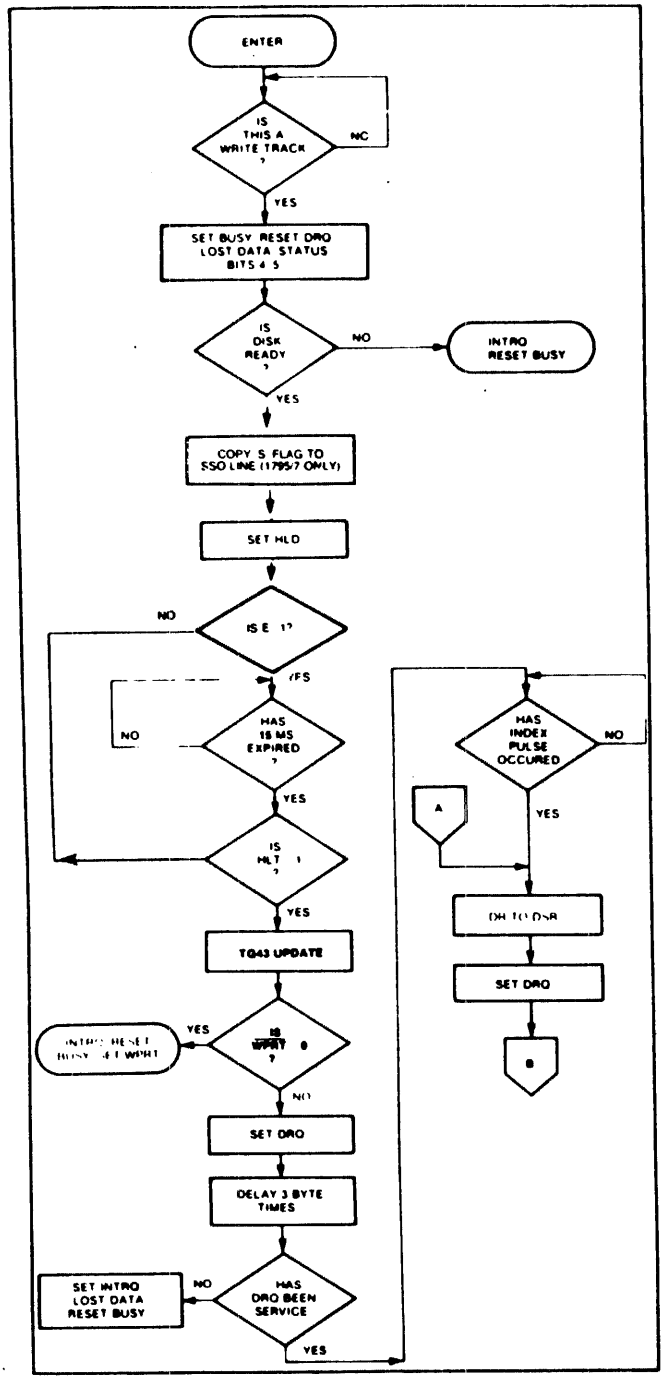
Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track Command. An internal side compare is not performed during a Read Track.

WRITE TRACK

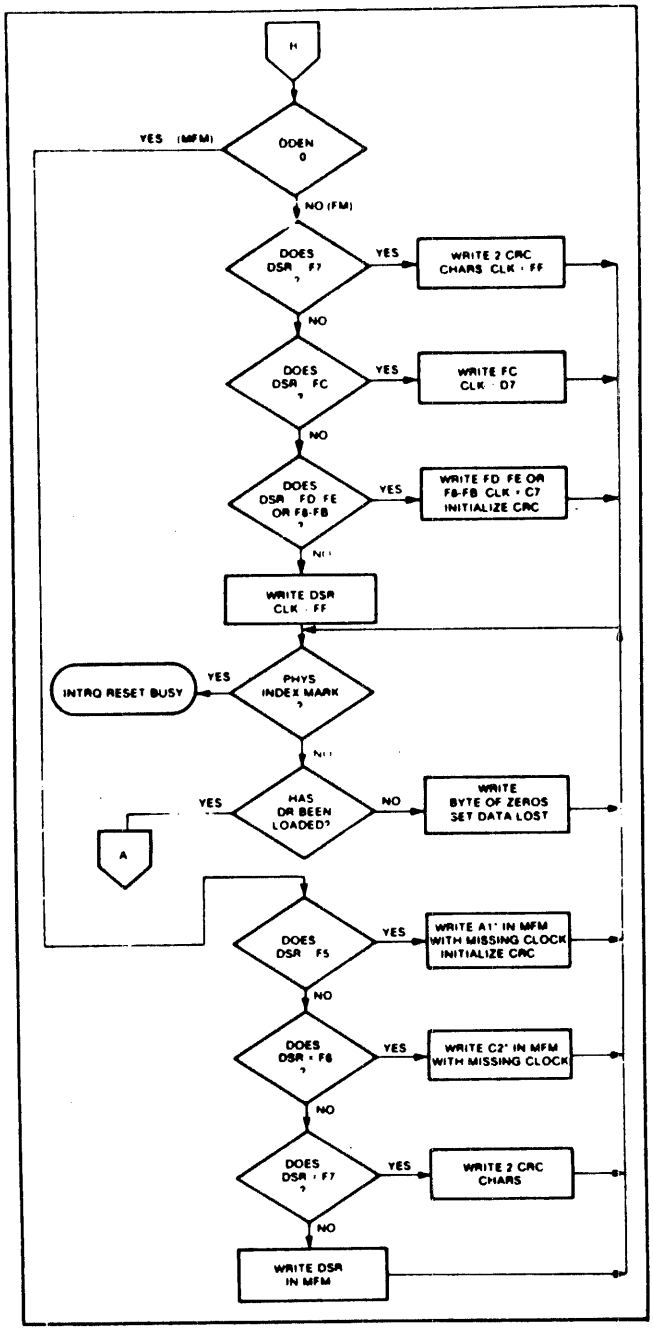
Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD										DATA FIELD		

In MFM only, IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing



TYPE III COMMAND WRITE TRACK



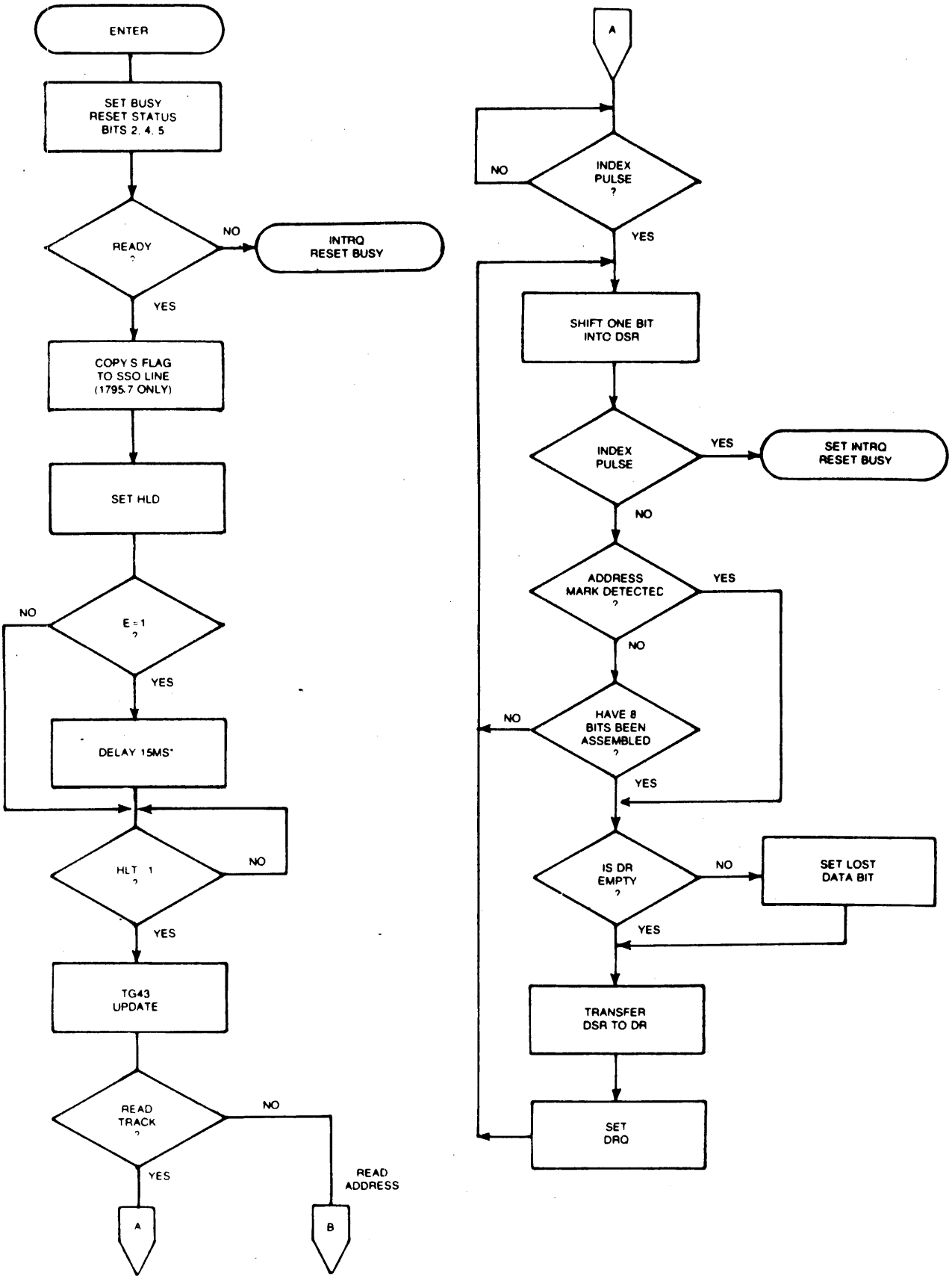
TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	FD1791/3 INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5

**Missing clock transition between bits 3 & 4

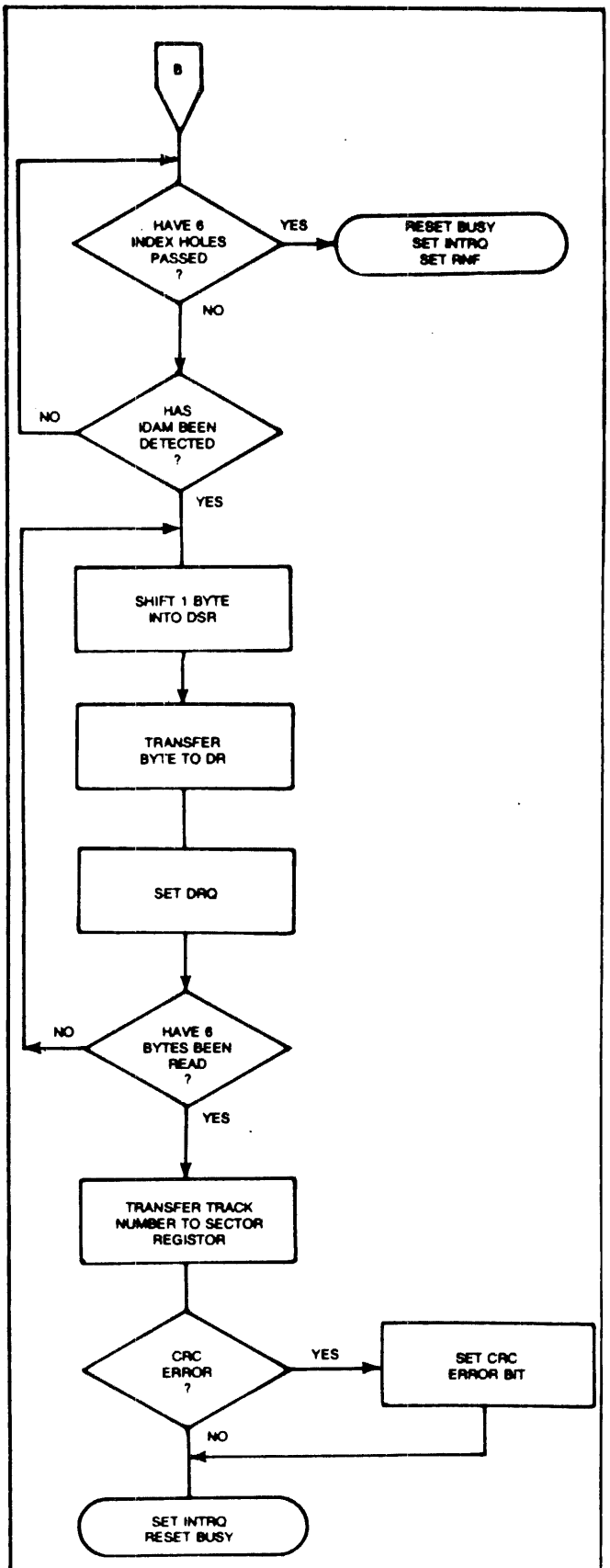


*II TEST 0 NO DELAY

II TEST 1 and CLK 1 MHZ 30 MS DELAY

TYPE III COMMAND

Read Track/Address



TYPE III COMMAND

Read Track/Address

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt (requires reset, see Note)

NOTE: If $I_0 - I_3 = 0$, there is no interrupt generated but the current command is terminated and busy is reset. *This is the only command that will enable the immediate interrupt to clear on a subsequent Load Command Register or Read Status Register.*

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD179X raises the Data Request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD179X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, in FM an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

IBM 3740 FORMAT—128 BYTES/SECTOR

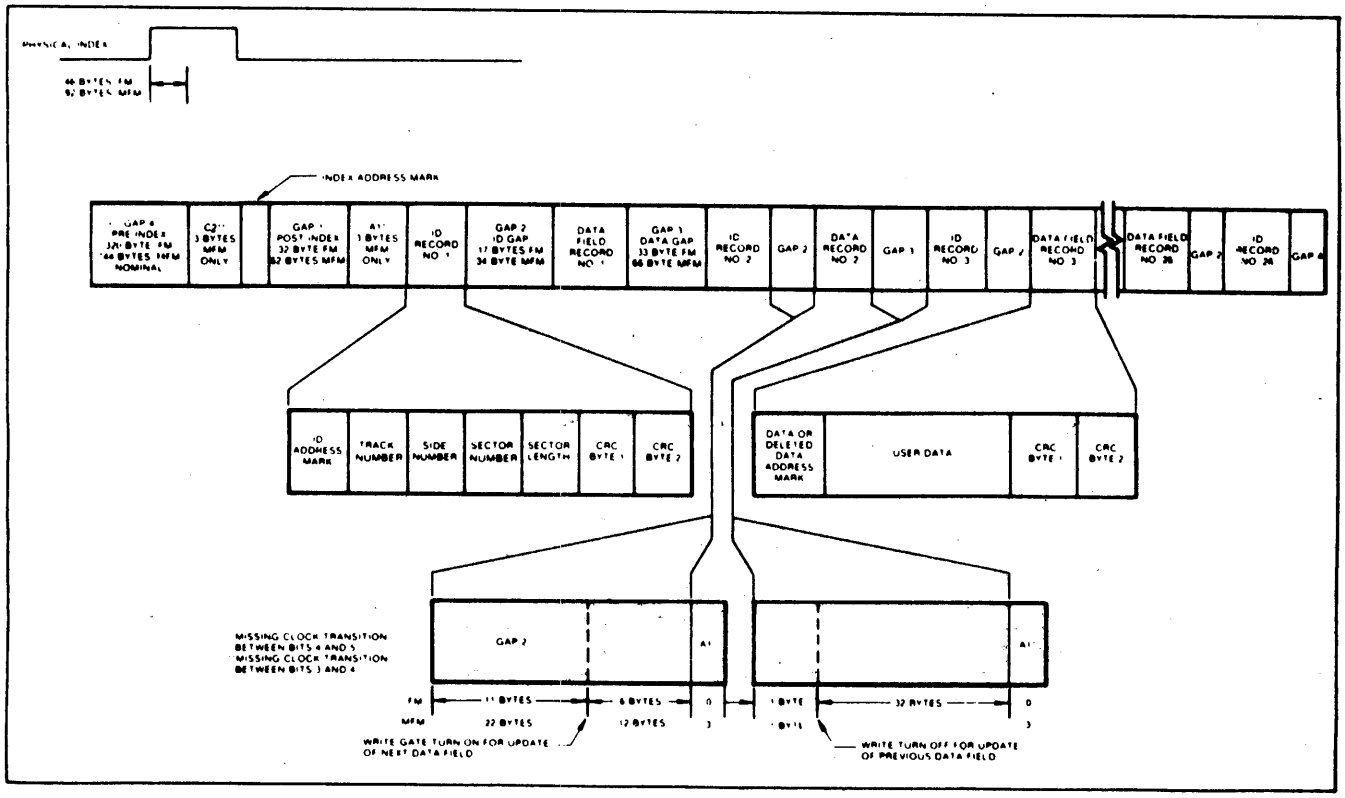
Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)[1]
6	00
1	FC (Index Mark)
26	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)
247**	FF (or 00)

*Write bracketed field 26 times

**Continue writing until FD179X interrupts out. Approx. 247 bytes.

1-Optional '00' on 1795/7 only.



IBM TRACK FORMAT

IBM SYSTEM 34 FORMAT- 256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6
1	FC (Index Mark)
50*	4E
12	00
3	F5
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01
1	F7 (2 CRCs written)
22	4E
12	00
3	F5
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

* Write bracketed field 26 times
**Continue writing until FD179X interrupts out. Approx. 598 bytes.

1. NON-IBM FORMATS

Variations in the IBM format are possible to a limited extent if the following requirements are met: sector size must be a choice of 128, 256, 512, or 1024 bytes; gap size must be according to the following table. Note that the Index Mark is not required by the 179X. The minimum gap sizes shown are that which is required by the 179X, with PLL lock-up time, motor speed variation, etc., adding additional bytes.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00 3 bytes A1
Gap III	10 bytes FF	24 bytes 4E 3 bytes A1
**	4 bytes 00	8 bytes 00
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground) =15 to −0.3V
Max. Voltage to Any Input With Respect to V_{SS} =15 to −0.3V
Operating Temperature 0°C to 70°C
Storage Temperature −55°C to +125°C

V_{DD} = ID ma Nominal V_{CC} = 35 ma Nominal

OPERATING CHARACTERISTICS (DC)

TA = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = OV, V_{CC} = + 5V ± .25V

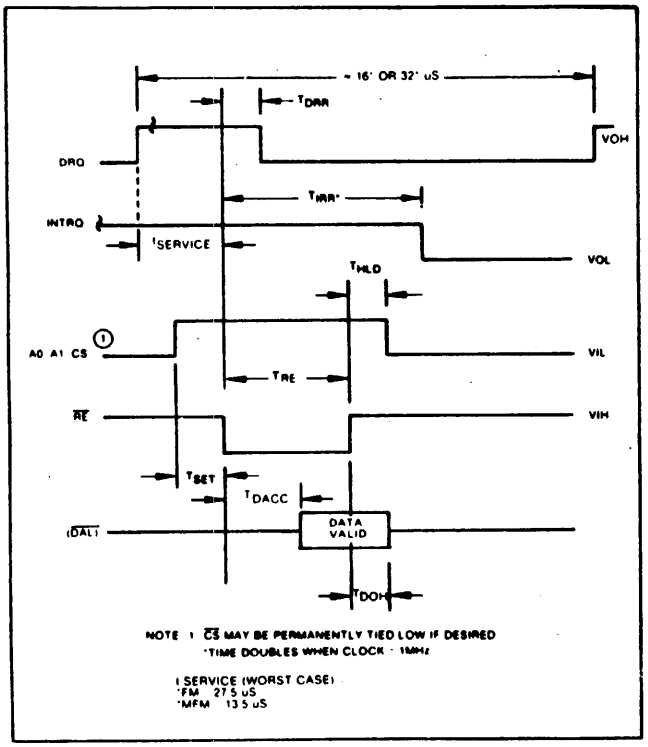
SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{DD}$
I_{OL}	Output Leakage		10	μA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.8		V	$I_O = -100\ \mu A$
V_{OL}	Output Low Voltage		0.45	V	$I_O = 1.6$ mA
P_D	Power Dissipation		0.5	W	

TIMING CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = +5V ± .25V

READ ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	400			nsec	C_L = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note 5
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 50 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 50 pf



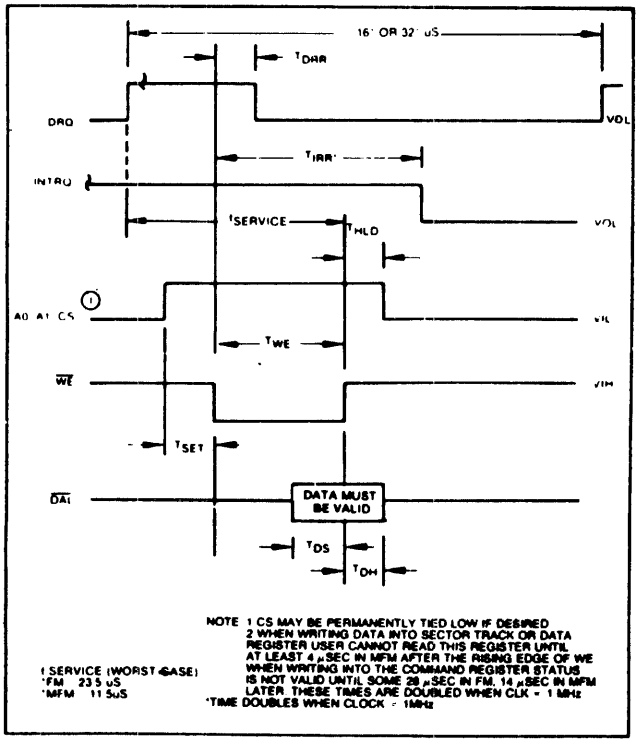
READ ENABLE TIMING

WRITE ENABLE TIMING

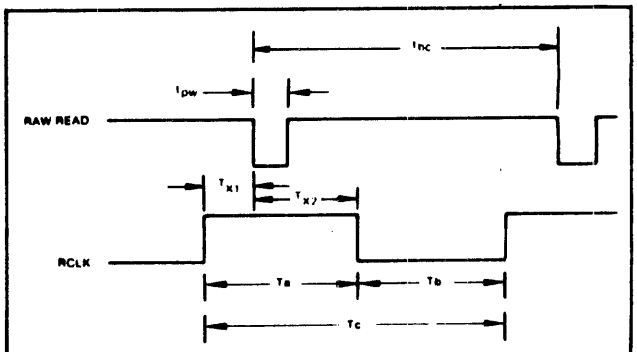
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note 5
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	70			nsec	

INPUT DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Tpw	$\overline{Raw\ Read}$ Pulse Width	100	200		nsec	See Note 1
tbc	$\overline{Raw\ Read}$ Cycle Time		1500		nsec	1800 ns @ 70°C
Tc	RCLK Cycle Time		1500		nsec	1800 ns @ 70°C
T_{X1}	RCLK hold to $\overline{Raw\ Read}$	40			nsec	See Note 1
T_{X2}	$\overline{Raw\ Read}$ hold to RCLK	40			nsec	



WRITE ENABLE TIMING

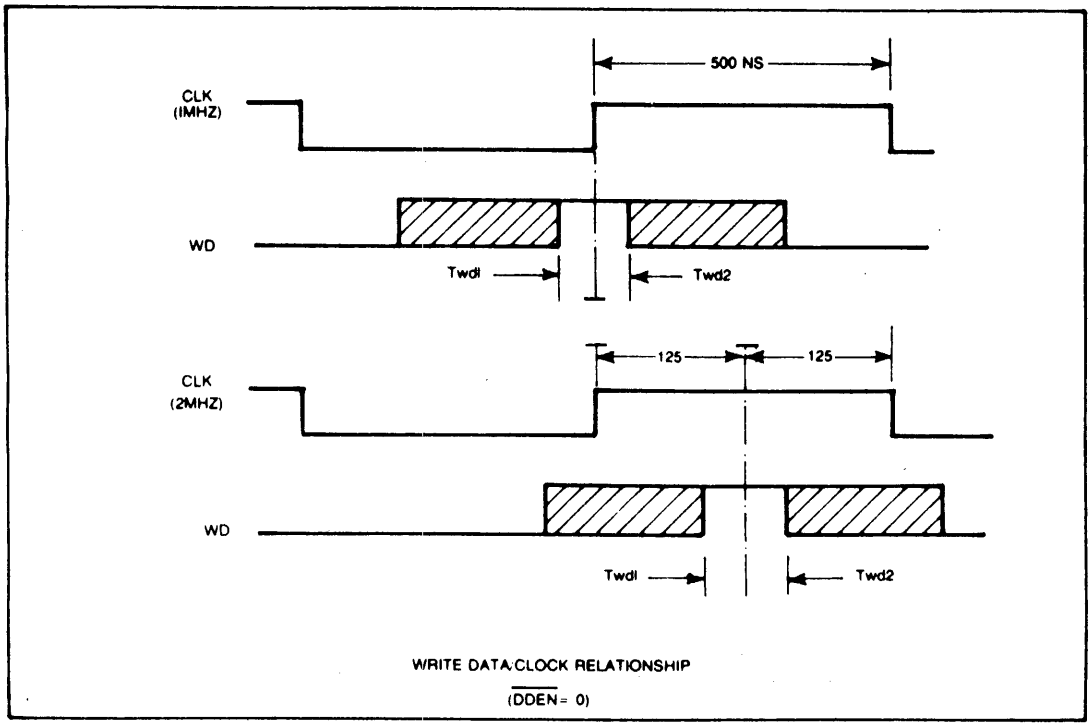


				NOMINAL		
DISKETTE	MODE	$\overline{DDEN}$	CLK	T_a	T_b	T_c
8"	MFM	0	2 MHz	1 μs	1 μs	2 μs
8"	FM	1	2 MHz	2 μs	2μs	4 μs
5"	MFM	0	1 MHz	2 μs	2μs	4 μs
5"	FM	1	1 MHz	4 μs	4 μs	8 μs

INPUT DATA TIMING

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz)

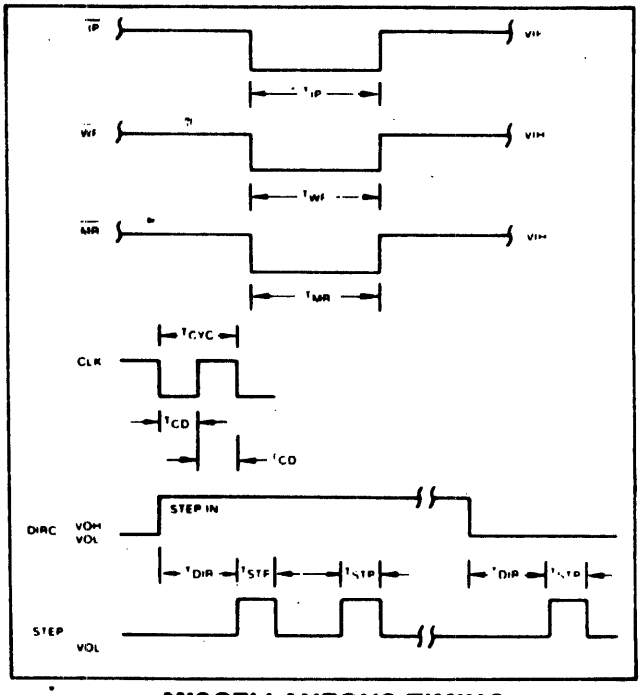
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width	450	500	550	nsec	FM
		150	200	250	nsec	MFM
Twg	Write Gate to Write Data		2		μsec	FM
			1		μsec	MFM
Tbc	Write data cycle Time		2,3, or 4		μsec	±CLK Error
Ts	Early (Late) to Write Data	125			nsec	MFM
Th	Early (Late) From Write Data	125			nsec	MFM
Twf	Write Gate off from WD		2		μsec	FM
			1		μsec	MFM
Twdl	WD Valid to Clk	100			nsec	CLK=1 MHZ
		50			nsec	CLK=2 MHZ
Twd2	WD Valid after CLK	100			nsec	CLK=1 MHZ
		30			nsec	CLK=2 MHZ



WRITE DATA TIMING

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	230	250	20000	nsec	
TCD_2	Clock Duty (high)	200	250	20000	nsec	
TSTP	Step Pulse Output	2 or 4			μsec	See Note 5
TDIR	Dir Setup to Step		12		μsec	± CLK ERROR
TMR	Master Reset Pulse Width	50			μsec	
TIP	Index Pulse Width	10			μsec	See Note 5
TWF	Write Fault Pulse Width	10			μsec	



MISCELLANEOUS TIMING

NOTES:

1. Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. A PPL Data Separator is recommended for 8" MFM.
3. tbc should be 2 μs, nominal in MFM and 4 μs nominal in FM. Times double when CLK = 1 MHz.
4. RCLK may be high or low during $\overline{\text{RAW READ}}$ (Polarity is unimportant).
5. Times double when clock = 1 MHz.

Table 6. STATUS REGISTER SUMMARY

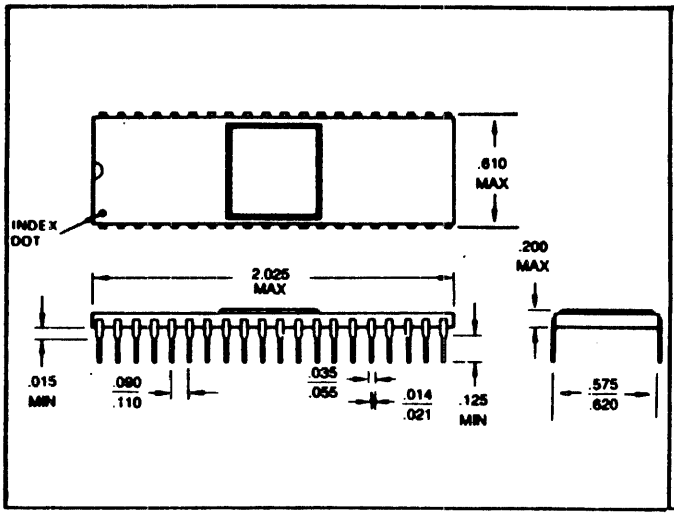
BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

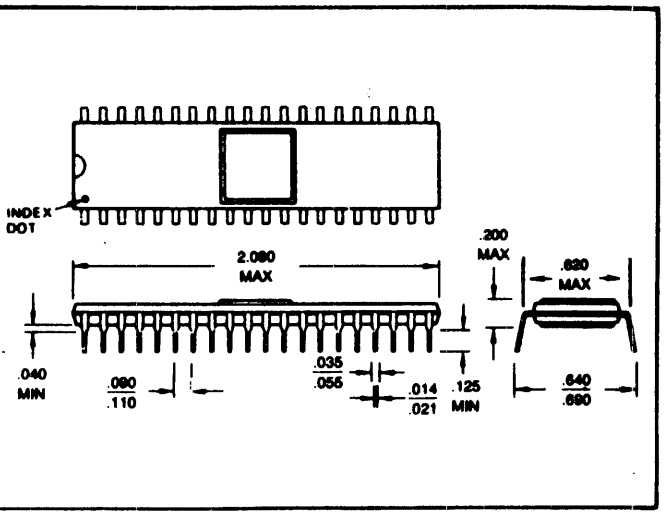
BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TROO}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.



FD179XA-02 CERAMIC PACKAGE



FD179XB-02 PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

WESTERN DIGITAL CORPORATION

3128 REDHILL AVENUE, BOX 2180
NEWPORT BEACH, CA 92663 (714) 557-3550,TWX 910-595-1139

JADE COMPUTER PRODUCTS
4901 W. ROSECRANS BLVD
HAWTHORNE, CALIF 90250

SUBJECT: ENGINEERING CHANGE NOTICE # 1.
PRODUCT: DOUBLE D DISK CONTROLLER.
REVISION: B AND C REVISION BOARDS.
DATE: AUGUST 4, 1980.

IT HAS BEEN REPORTED THAT INSERTION OF THE DOUBLE D DISK CONTROLLER INTO OF SOME S100 SYSTEMS PREVENTS NORMAL OPERATION. USUALLY ON THESE SYSTEMS THE COMMON CHARACTERISTIC IS THAT THEY JUST WILL NOT OPERATE. PLEASE NOTE S100 BUS PINS #20, #53, AND #70 ARE CONNECTED TO GROUND, AS PER S100 STANDARDS, IEEE TASK 696.1/D2. THESE PIN CONNECTIONS DO CAUSE INTERFERANCE WITH IMSAI FRONT PANEL SYSTEMS OR CPU BOARDS DESIGNED TO OPERATE WITH FRONT PANELS. IT IS PERMISSABLE TO CUT THE FOIL LINKS CONNECTING PINS #20, 53, AND 70 TO THEIR RESPECTIVE PLATE-THRU-HOLES. PLEASE VERIFY IN YOUR SYSTEM DOCUMENTATION THAT THESE PINS ARE CAUSING INTERFERENCE BEFORE CUTTING.

SUBJECT: ENGINEERING CHANGE NOTICE # 2.
PRODUCT: DOUBLE D DISK CONTROLLER.
REVISION: B AND C REVISION BOARDS.
DATE: AUGUST 4, 1980.

A REVIEW OF THE DOUBLE D 8" PHASE LOCKED LOOP HAS BEEN COMPLETED. THIS HAS RESULTED IN A RESELECTION OF SOME COMPONENT VALUES. ENHANCED OPERATION, PARTICULARLY IN DOUBLE DENSITY, WILL BE REALIZED WITH THE FOLLOWING MODIFICATION. THIS MODIFICATION WILL DOUBLE THE LOOP CAPTURE RANGE AND ALSO ELIMINATE A CAUSE OF LOOP INSTABILITY.

WITH THE EXCEPTION OF R1, JUST CHANGE THOSE RESISTORS LISTED FOR THE NEW VALUES AS SHOWN IN THE LIST. R1 DOES HAVE A CHANGED VALUE BUT ALSO MUST BE INSTALLED SO THAT IT WILL CONNECT TO +5 VOLTS REGULATED INSTEAD OF THE PREVIOUS CONNECTION TO VX. WITH CAREFUL LEAD BENDING AND RESISTOR PLACEMENT, ONE LEAD CAN SOLDER TO THE +5V FOIL RUNNING FROM PIN #16 OF IC 1A TO PIN #16 OF IC 1B. IT WOULD HELP TO SCRAPE SOME OF THE SOLDER MASK AWAY BEFORE SOLDERING R1 TO THIS FOIL. VX WILL NOW MEASURE ABOUT +5.0 VOLTS. INSTALLATION OF THE MODIFICATION WILL REQUIRE RETUNING THE PLL.

R1	6.8K 1/4W (TO +5V)	R42	470K 1/4W
R3	12K 1/4W	R43	2.7K 1/4W
R4	10K 1/4W	R49	JUMPER
R38	20K 1/4W		

SUBJECT: ENGINEERING CHANGE NOTICE # 3.
PRODUCT: DOUBLE D DISK CONTROLLER.
REVISION: B AND C REVISION BOARDS.
DATE: AUGUST 4, 1980.

THE DOUBLE D DISK CONTROLLER USES S-100 SIGNAL SWO*. CPUS SUCH AS SBC-100 AND SBC-200 DO NOT GENERATE THESE SIGNALS AND THEREFORE PRESENT AN INTERFACE PROBLEM. THE FOLLOWING MODIFICATION HAS SOLVED THE PROBLEM WITH THE ABOVE MENTIONED BOARDS.

1. ON THE SOLDER SIDE OF THE BOARD: CUT THE FOIL LINK FROM S-100 PIN # 97 TO THE PLATE-THRU-HOLE.
2. ON THE SOLDER SIDE OF THE BOARD: USING A SMALL GAUGE WIRE JUMPER IC 1H PIN #2 TO IC 3J PIN #1.

SUBJECT: ENGINEERING CHANGE NOTICE # 4.
PRODUCT: DOUBLE D DISK CONTROLLER.
REVISION: B AND C REVISION BOARDS.
DATE: AUGUST 4, 1980.

THE DOUBLE D DISK CONTROLLER EXHIBITS ERRATIC OPERATION WHEN RUN WITH THE BIG-Z Z80 CPU BOARD. THE PROBLEM EXISTS ON THE BIG-Z BOARD. THE FOLLOWING MODIFICATION FIXES THIS PROBLEM. NOTE: THE BIG-Z DOES NOT SEND OUT WRITE DATA TO THE S-100 BUS UNTIL IT ACTUALLY SENDS THE WRITE STROBE. THIS MODIFICATION ALLOWS THE WRITE DATA TO SETTLE ON THE S-100 BUS BEFORE THE WRITE STROBE IS ISSUED.

1. ON THE SOLDER SIDE BIG-Z: CUT THE FOIL FROM IC 22 PIN # 13.
2. ON THE SOLDER SIDE BIG-Z: JUMP IC 22 PIN # 13 TO PIN # 3.

SUBJECT: ENGINEERING CHANGE NOTICE # 5B.
PRODUCT: DOUBLE D DISK CONTROLLER.
REVISION: B AND C REVISION BOARDS.
DATE: AUGUST 5, 1980.

IMPORTANT NOTICE! BOARD MODIFICATION NEEDED ON REVISION C. THIS ECN PERTAINS TO THE USE OF THE DOUBLE D DISK CONTROLLER WITH JADE RELEASE # 2 OF CP/M 2.2. CONNECTOR J3 PIN #48 WAS DESIGNATED ILLEGAL PACK*. IT HAS BEEN REDEFINED AND IT IS NOW DESIGNATED TWO SIDED*.

MANY SHUGART SA800/801, SIEMENS FD100-8, AND OTHER MODELS OF DISK DRIVES HAVE OPTIONAL DATA SEPERATORS INSTALLED. DISK DRIVES USING THESE OPTIONS USE PIN #48 OF THE 50 LINE RIBBON FOR THE SEPERATED DATA* SIGNAL. AS RELEASE #2 (SPECIFICALLY DCM2) MONITORS THIS SIGNAL LINE FOR TWO SIDED* , ERRATIC DISK OPERATION WOULD BE EXPECTED. PLEASE CUT THE FOIL LINK BETWEEN THE TWO PLATE-THRU-HOLES AT J3 PIN #48 (REVISION C). FOR USE WITH THE SA850/851 DISK DRIVE A JUMPER SHOULD BE INSTALLED ON THE J3 PATCHING AREA FROM THE LOWER PIN # 48 PLATE-THRU-HOLE TO THE UPPER PIN #10 PLATE-THRU-HOLE. THIS COMPLETES THE PATH FOR THE TWO SIDED* SIGNAL FROM THE SA850/851.

SUBJECT: ENGINEERING CHANGE NOTICE # 6.
PRODUCT: DOUBLE D DISK CONTROLLER.
REVISION: B AND C REVISION BOARDS.
DATE: AUGUST 5, 1980.

NOTE: CONCERNING THE DOUBLE D DISK CONTROLLER WHEN USED WITH 64K OF SYSTEM MEMORY OR ANY OTHER MEMORY ARRANGEMENT WHERE THE DOUBLE D MEMORY WINDOW OVERLAPS ASSIGNED MEMORY SPACE.

WHEN USED IN THIS CONFIGURATION THE PHANTOM BLOCK MUST BE JUMPERED TO COMPLETE THE PHAN* SIGNAL PATH TO THE S100 BUS. THE PHANTOM BLOCK IS LOCATED BELOW IC 4D. IT APPEARS AS TWO PLATE-THRU-HOLES ENCLOSED BY A SILKSCREEN BORDER LABELED PHAN*. ADD A JUMPER CONNECTING THESE TWO HOLES TOGETHER. ANY MEMORY BOARD THAT THE DOUBLE D IS TO OVERLAP MUST BE CONFIGURED SO AS TO BE DISABLED WHEN RESPONDING TO THE PHANTOM SIGNAL (PHAN*).

SUBJECT: ENGINEERING CHANGE NOTICE # 7.
PRODUCT: DOUBLE D DISK CONTROLLER.
REVISION: B AND C REVISION BOARDS.
DATE: OCTOBER 6, 1980.

NOTE: USE NATIONAL SEMICONDUCTOR 74LS123 ONE-SHOTS ON THE DOUBLE-D CONTROLLER BOARD. THE RESISTOR / CAPACITOR COMBINATIONS HAVE BEEN SELECTED TO PROVIDE PROPER PULSE PERIODS WHEN USED WITH THIS ONE-SHOT. DOUBLE D DISK CONTROLLER BOARDS (A&T AND KIT) ARE NOW SUPPLIED WITH NATIONAL SEMICONDUCTOR 74LS123S. CUSTOMERS WHO BUILD DOUBLE D BARE BOARDS TAKE NOTE.

SUBJECT: ENGINEERING CHANGE NOTICE # 8.
PRODUCT: DOUBLE D DISK CONTROLLER.
REVISION: C REVISION BOARDS.
DATE: OCTOBER 6, 1980.

THE FOLLOWING LIST CONTAINS CORRECTIONS TO THE DOUBLE D REVISION C SCHEMATIC OF 3/7/80. PLEASE MAKE THESE CORRECTIONS TO YOUR DIAGRAMS.

1. THE OUTPUT OF IC 1M (7406) PIN 6 TO THE PLATE-THRU-HOLE IN THE INTERRUPT BLOCK SHOULE BE LABELED DINT*. (PAGE 1)

2. A SECTION OF IC 3L (PINS 5 AND 15) HAS BEEN DRAWN AND LABELED AS A 74LS244. THIS IS SHOWN ON PAGE 1 CONNECTED TO THE 1791. THIS PART IS A 74LS240.

3. AN INVERTING BUFFER, PART OF IC 3L (74LS240) PINS 11 AND 9, IS NOT SHOWN IN THE DIAGRAM. PIN 11 IS THE INPUT AND IS CONNECTED TO DDEN. PIN 9 IS THE OUTPUT AND IS THE SOURCE FOR DDEN*.

4. FOUR PIN ASSIGNMENTS OF IC 3H (8131) ARE IN ERROR. CHANGE PIN 13 TO PIN 11, PIN 12 TO PIN 10, PIN 11 TO PIN 13, AND PIN 10 TO PIN 12. (PAGE 1)

5. THE INPUT TO IC 4A ON PIN 13 IS LABELED AS BPWR*. THIS LABEL SHOULD READ AS BPWR. (PAGE 2)

SUBJECT: ENGINEERING CHANGE NOTICE # 9.
PRODUCT: DOUBLE D DISK CONTROLLER.
REVISION: B AND C REVISION BOARDS.
DATE: OCTOBER 6, 1980.

THE FOLLOWING JUMPER CONFIGURATION CAN BE USED WITH THE SHUGART SA800/801 MODEL DISK DRIVE.

EACH DRIVE: A, B, C, Y, T2, HL, 800

DRIVE A: DS1
DRIVE B: DS2
DRIVE C: DS3
DRIVE D: DS4

LAST DRIVE: T1, T3, T4, T5, T6

THE L JUMPER IS SET DEPENDING ON THE -5V SUPPLY. CONSULT YOU SA800 MANUAL. USE NO OTHER JUMP PLUGS IN THIS CONFIGURATION.

SIEMENS DISK DRIVE MODELS FD120-8B AND THE NEWER FD100-8D CAN BE USED THE JADE DOUBLE D. EACH DRIVE MUST HAVE THE RADIAL SELECT OPTION PLUG SET TO THE PROPER DRIVE NUMBER. 0 SELECTS DRIVE A, 1 SELECTS DRIVE B, 2 SELECTS DRIVE C, AND 3 SELECTS DRIVE D. ONLY THE LAST DRIVE ON THE RIBBON SHOULD CONTAIN THE RESISTOR PACK. BE SURE TO REVIEW ECN #5. NO OTHER CHANGES ARE NEEDED.

THE FOLLOWING PAGE DESCRIBES A TESTED JUMPER CONFIGURATION FOR THE SHUGART SA850/851 WHEN USED WITH JADE RELEASE # 2 OF CP/M 2.2.

SHUGART SA850/851

START WITH THE DISK DRIVE(S) SET TO FACTORY CONFIGURATION AS DESCRIBED IN THE SERIVE AND MAINTENANCE MANUAL. THEN PERFORM THE FOLLOWING ALTERATIONS TO THE DRIVE(S).

1. REMOVE THE 'IW' PLUG. THIS ALLOWS FOR LOWER WRITE CURRENT ON THE INSIDE TRACKS.

2. REMOVE THE 'RS' PLUG AND INSTALL THIS PLUG AT 'RM'. THIS ALLOWS DRIVE READY TRUE WHEN DIRECTION (SIDE SELECT) IS SELECTING THE WRONG SIDE OF A SINGLE SIDED DISKETTE.

3. BREAK CONNECTION 'X' ON THE SHORTING PLUG AND INSTALL A PLUG AT 'C'. THIS ALLOWS THE DRIVE TO BE SELECTED WITHOUT ENABLING THE STEPPER OR LOADING THE R/W HEAD.

4. BREAK CONNECTION 'Z' ON THE SHORTING PLUG AND INSTALL A PLUG AT 'Y'. ACTIVITY LIGHT ON FROM R/W HEAD LOADED.

5. REMOVE THE 'S2' PLUG AND INSTALL AT 'S1'. THIS ALLOWS SIDE SELECT FROM THE 'STEP DIRECTION' SIGNAL.

6. REMOVE THE '851' PLUG AND INSTALL AT '850'. THIS IS FOR SOFT SECTORED DISKETTES.

7. INSTALL A PLUG AT '2S'. THIS ALLOWS THE DRIVE TO ISSUE THE 'TWO SIDED' SIGNAL WHEN TWO SIDED DISKETTES ARE INSERTED.

8. REMOVE THE 'DL' PLUG.

9. SET -5/-15 ACCORDING TO THE NEGITIVE SUPPLY VOLTAGE YOU ARE USING.

10. DRIVE A: INSTALL PLUG AT 'DS1'.
    DRIVE B: INSTALL PLUG AT 'DS2'.
    DRIVE C: INSTALL PLUG AT 'DS3'.
    DRIVE D: INSTALL PLUG AT 'DS4'.

11. REMOVE THE TERMINATOR FROM ALL BUT THE LAST DRIVE ON THE RIBBON CABLE.

12. INSTALL JADE DOUBLE D ECN # 5.

ENGINEERING

HARDWARE MODIFICATION

REVISION #: G1 **DATE:** **IMP.:** GH-003

AUTH.: G. Herr **DATE:**
ITEM: Jade Double D FDC

REASON FOR CHANGE:

To improve the noise immunity of the Control Port. The existing design strobes data into IC 2L (74LS74) on the leading edge of the S100 I/O write signal. Inverting the clock allows strobing the data on the trailing edge. The gives the data on the bus a longer time to settle.

PROCEDURE:

1. On the component side of the board, cut the trace from the via located above pin 1 of IC 2K. On the solder side, add a 30AWG wire from IC 3J pin 12 to the via between IC 1F and IC 2F, directly above IC 2F pin 14. This reconnects the 'BCPS' clock to IC 1A pin 10, which is required for proper reset.

2. On the solder side of the board, cut the trace between the via located to the right of, and between IC 3L pin 5 and 6, and leading to IC 2L pin 3. Solder a 30AWG wire from this via to IC 1L pin 1. Solder a 30AWG wire from IC 1L pin 2 to IC 2L pin 3.

3. Replace IC 2L (74LS74) with a 7474 for added noise immunity (a slower part).

HARDWARE MODIFICATION

REVISION #: G2 **DATE:** **IMP.:** GH - 003

AUTH.: G. Herr **DATE:**
ITEM: Jade Double D FDC

REASON FOR CHANGE:

To allow the Double D to overlap the System Monitor PROM, an additional signal needs to be provided. This signal is derived from the same signal that generates 'PHAN-', but must be a separate open-collector driver.

PROCEDURE:

1. Add a 30AWG wire from IC 1M pin 5 to IC 1M pin 11.

2. Add a 30AWG wire from IC 1M pin 10 to S100 bus pin 65 (a via is provided).

HARDWARE MODIFICATION

REVISION #: G3 **DATE:** **IMP.:** GH-003

AUTH.: G. Herr **DATE:**
ITEM: Jade Double D FDC

REASON FOR CHANGE:

The Double D only responds to extended address bank 0FFh. The new system requires the Double D to respond to bank 0FEh.

PROCEDURE:

1. Add a 74LS86 exclusive or gate piggybacked on top of IC 4F by:

A. Bend all legs but pin 7 and pin 14 of a 74LS86 IC straight out from the body (a 90 deg. bend).

B. Clip all but 1/16th inch off of the pins bent in step 'A'.

C. Solder pin 7 and pin 14 of the modified IC to the same pins of IC 4F. Make sure the modified IC is on top of IC 4F (IC 4FH).

2. Add a 30AWG wire from IC 4FH pin 1, to pin 14.

3. On the solder side of the board, cut the trace from the via at S100 bus pin 16, to via near IC 4C pin 3.

4. Add a 30AWG wire from the via at the S100 bus pin 16, to IC 4FH pin 2.

5. Add a 30AWG wire from the via near IC 4C pin 3, to IC 4FH pin 3.

6. Make a modified DM8131 IC for IC 3H as follows:

A. Bend pin 10 and pin 12 of a DM8131 IC straight out from the body (a 90 deg. bend).

B. Clip all but 1/16th inch off of the pins bent in step 'A'.

C. As close to the body of the IC as possible, solder a 30AWG insulated wire from pin 7 to pin 10. Continue the insulated wire to pin 12.

D. Replace IC 3H with the modified IC.

HARDWARE MODIFICATION

REVISION #: G4 **DATE:** **IMP.:** GH-003

AUTH.: G. Herr **DATE:**
ITEM: Jade Double D FDC

REASON FOR CHANGE:

In certain conditions, the WD179x controller IC will not generate a termination interrupt and the Double D will lock up. One of these conditions occurrs when a 5" floppy is not installed in the drive. There are no index pulses with this condition and the WD179x IC waits for a fixed number of index pulses to occurr to complete the command. The firmware is then waiting for the WD179x IC to complete.

This solution uses the headload timout to force an interrupt to the embedded processor, thus breaking out of the infinite wait condition.

PROCEDURE:

1. Make a subassembly of two 2N3904 transistors, two 1N4143 diodes, and a 10K ohm 1/4 watt 5% resistor as follows:

A. As close as possible to each other, solder the two transistor emitter leads together. Do the same for the collector leads.

B. As close as possible to each component, solder one end of the 10K ohm resitor to the collector connection made in 'A'. Solder the other end of the resistor and the Anode ends of the two diodes to one transistor's Base lead.

2. On the solder side of the board, cut the trace from IC 1J pin 39 at this pin. Also cut the trace from the anode side of CR18, between IC 2M and 3M.

3. On the solder side of the board, cut the trace from the via at S100 bus pin 16, to via near IC 4C pin 3.

4. Remove R18.

5. Add a 470 ohm 1/4 watt 5% resistor on the bottom of the board from the via between IC 3F pins 7 and 10, and S1 pin 8 (ground).

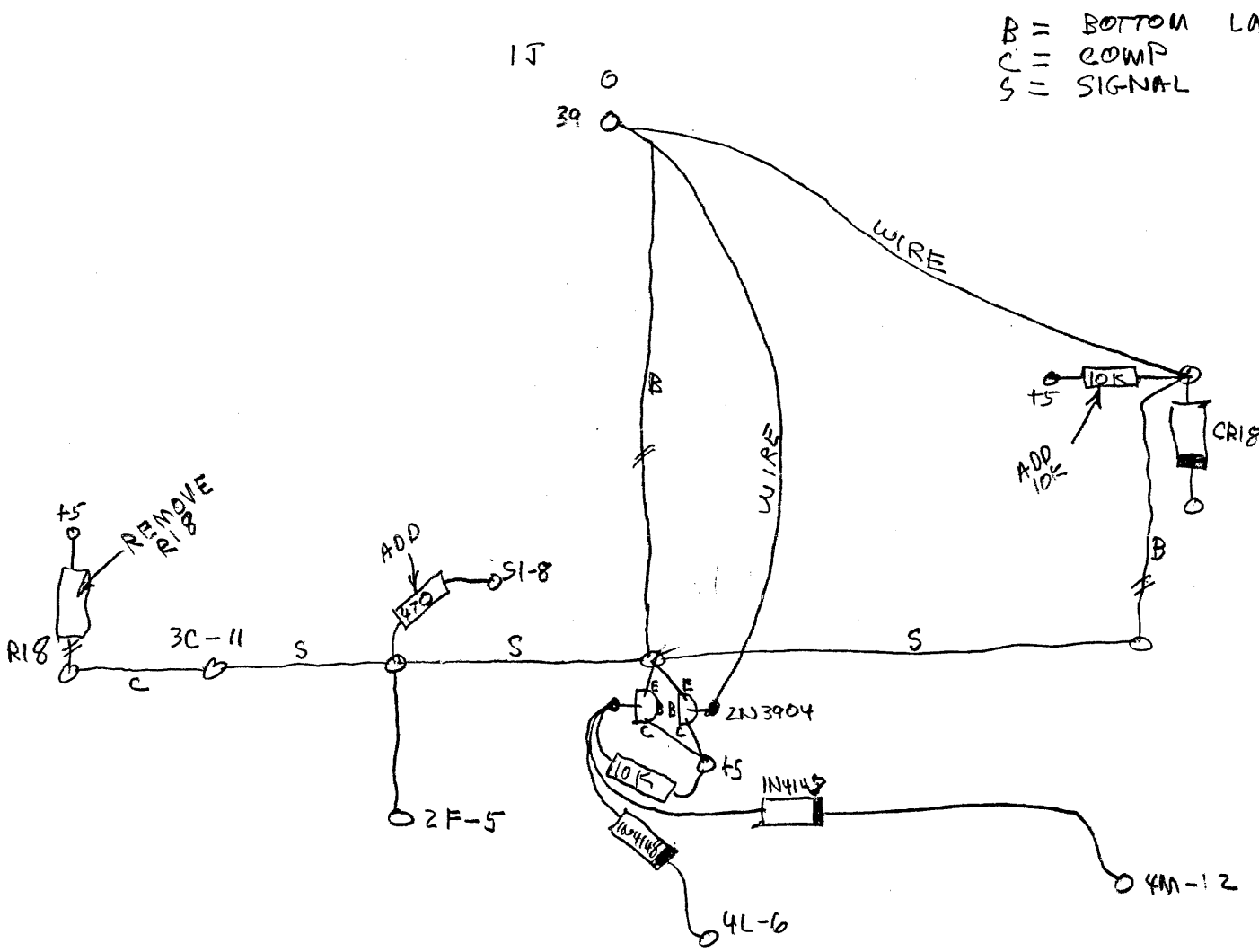
6. On the component side of the board, solder the emitters of the assembly made in step 'A' to the via above and to the right of the top pad of R7 (between IC 3J and IC 3K). Solder the collectors to the via between R7 and IC 4K pin 1 (+5v).

7. Solder a 30AWG wire to the anode of one 1N4148 diode connected to the assembly base. Solder the other end of this wire to IC 4L pin 6.

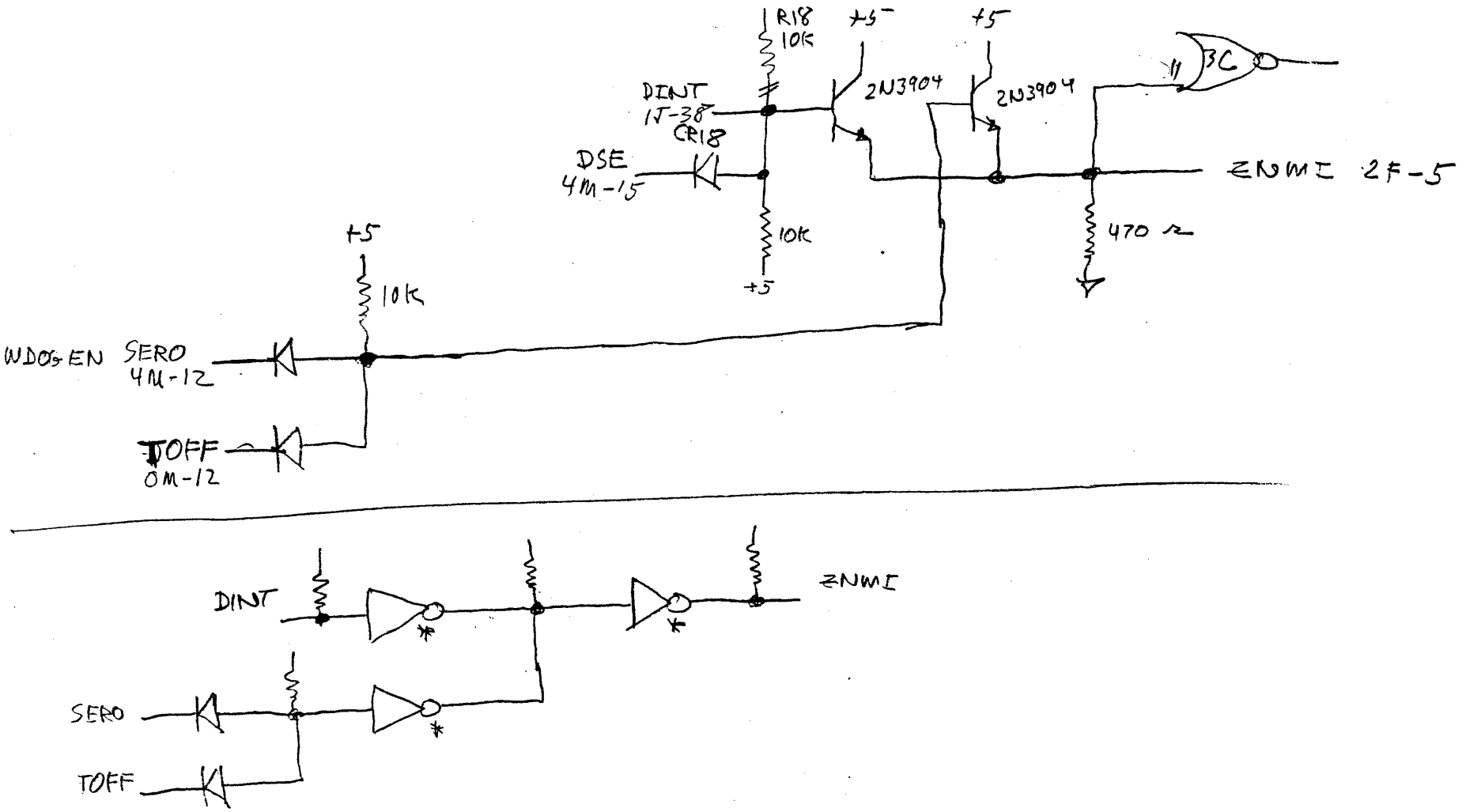
8. Solder a 30AWG wire to the anode of the other 1N4148 diode connected to the assembly base. Solder the other end of this wire to IC 4M pin 12.

9. Solder one end of a 10k ohm 1/4 watt 5% resistor to the anode of CR18. Solder the other end of the resistor to the via above and to the right of IC 3M pin 1.

10. Solder a 30AWG wire fto the other 2N3904 base. Solder the other end of this wire and a second 30AWG wire to IC 1J pin 39. Solder the other end of the second wire to the anode of CR18.



WATCHDOG MOD



WATCHDOG MOD.

REV ~~C3~~ C4

HARDWARE MODIFICATION

REVISION #: G5 **DATE:** 1-12-92 **IMP.:** GH-003 1-12-92

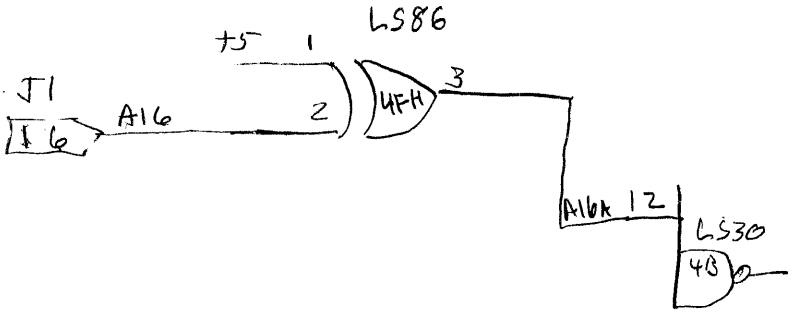
AUTH.: G. Herr **DATE:** 1-12-92
ITEM: Jade Double D FDC

REASON FOR CHANGE:

Some 8" drives require a "Motor On" signal on pin 4. The Double D does not connect this signal to pin 4, only on the 5" connector.

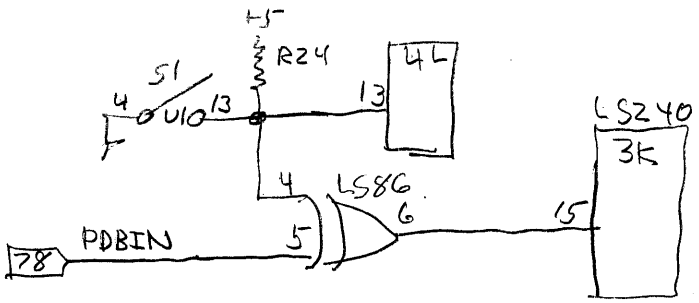
PROCEDURE:

1. Solder a 30AWG wire from the pad at J2 pin 16 to the pad for J3 pin 4.



BANK FE MOD

G-5 3



ADBIN INVERT MOD

G-6

JADE would welcome your comments about this board. We are very much interested in you, our customer, and we want to provide ourselves with some feedback about how you like the product and documentation. Please take a moment and fill out the questionaire and return it to us at the address below.

JADE COMPUTER PRODUCTS
TECHNICAL SUPPORT GROUP
4901 WEST ROSECRANS
HAWTHORNE, CA 90250

1. Was your DOUBLE D damaged in shipment? YES NO

2. Were any parts missing? YES NO

   If yes, what were they? _____

   _____

3. Was the quality of the material and

   workmanship good? YES NO

4. Did you have any trouble understanding the manual? YES NO

   If yes, in what area(s)? _____

   _____

5. Have you encountered problems with the DOUBLE D? YES NO

   If yes, what? _____

   _____

6. Did you solve the problem? YES NO

   If yes, how? _____

   _____

   _____

7. Are you satisfied with your DOUBLE D? YES NO

   If not, why? _____

   _____

SEE OTHER SIDE

8. Do you have any suggestions for design improvement? YES NO

   If yes, what? _____

   _____

9. In your opinion, what are the advantages and disadvantages of the DOUBLE D? _____

   _____

   _____

10. Other comments? _____

    _____

    _____

    _____

    _____

    _____

    _____

    _____

    _____

    _____

    _____

    _____

    _____

11. NAME: _____

    ADDRESS: _____

    CITY, STATE: _____

    ZIP·CODE: _____

    PHONE: _____

THANK YOU

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	C	PRODUCTION 'C' BOARD	3-7-80	S Faulk

SYMBOLS

- PLATED THRU HOLE
- (T) TERMINATOR
- OPTIONAL JUMPER FACTORY INSTALLED
- OPTIONAL JUMPER USER INSTALLED

QTY REQD	PSCR NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO

APPROVALS	DATE
DRAWN STAN KRUMME	11/79
CHECKED	
ISSUED	

MATERIAL

FINISH

DO NOT SCALE DRAWING

NEXT ASSY | USED ON

APPLICATION

JADE Computer Systems

DOUBLE DISK CONTROLLER

SIZE D | FSCM NO. | DWG. NO. IOD-1200 | REV C

SCALE | SHEET 1 OF 2

ZONE	REV	DESCRIPTION	DATE	APPROVED
	C	PRODUCTION 'C' BOARD	3-7-80	S. Mak
		C3 WATCHDOG TIMER MOD	5-29-91	K. Au

VOLTAGE REGULATORS

V.C.O.

CLOCK GENERATOR

PHASE COMPARATOR

FILTER

2X GAIN

PULSE DETECTOR

WRITE PRECOMPENSATION

CLOCK SELECT

QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
			PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
XX ±
XXX ±

CONTRACT NO

APPROVALS	DATE
DRAWN STAN KRUMME	11/79
CHECKED	
ENGR	
MFG	

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

JADE Computer Systems

DOUBLE DISK CONTROLLER

SIZE	FSCM NO	DWG NO	REV
D		IOD-1200	C
SCALE		SHEET 2 OF 2	

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	C	PRODUCTION 'C' BOARD C1 VCO MOD, RONDIS (2D3, 2C8) C2 BOARD ACK ON DI4 (1C6)	3-7-80 3-13-86	Stank Hem

SYMBOLS
- PLATED THRU HOLE
- TERMINATOR
- OPTIONAL JUMPER FACTORY INSTALLED
- OPTIONAL JUMPER USER INSTALLED

PARTS LIST

QTY REQD	FSCM NO	PART OR IDENTYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS ±; DECIMALS ±; ANGLES ±°

CONTRACT NO

APPROVALS	DATE
DRAWN STAN KRUMME	11/79
CHECKED	
ENGR	

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

JADE Computer Systems

DOUBLE DISK CONTROLLER

SIZE D | FSCM NO | DWG NO IOD-1200 | REV C

SCALE | SHEET 1 OF 2

DWG. NO.		SH	REV.

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	C	PRODUCTION 'C' BOARD	3-7-80	Stan K.

VOLTAGE REGULATORS

V.C.O.

CLOCK GENERATOR

PHASE COMPARATOR

FILTER

CLOCK SELECT

PULSE DETECTOR

WRITE

PRECOMPENSATION

QTY. REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
			PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS | DATE

DRAWN STAN KRUMME 11/79

CHECKED

ENGR

JADE Computer Systems

DOUBLE DISK CONTROLLER

SIZE D | FSCM NO. | DWG. NO. IOD-1200 | REV C

SCALE | SHEET 2 OF 2