INTRODUCTION

The purpose of this Application Note is to assist the user in the use of the Peripheral Expansion Interface on the Megatel Quark family of single board computers. The note discusses and provides schematics showing how 8080-, 6500-, and 6800-type peripheral devices can be connected to a Quark. A schematic is also included to illustrate how the Quark's address, data and control lines can be buffered.

DESCRIPTION

The various members of the Quark family of single board computers provide all of the functions necessary to integrate standard peripheral devices into many complete, stand-alone computer systems. Sometimes though, special or additional I/O functions are needed in some applications. The Quark can accomodate these special functions through its Peripheral Expansion Interface. The Interface provides external access to the eight data lines, the six least-significant address lines, and to appropriate timing and control lines.

The Read ($\overline{RD}$) and Write ($\overline{WR}$) lines generated by the Z80B are brought out on the Peripheral Expansion Interface. These two lines would be used with some 8080-compatible peripheral devices, such as the 8251 UART or the 8255 PPI. Other 8080-compatible devices (chiefly A-version types like the 8255A) require that the Address and $\overline{CS}$ lines be stable before $\overline{WR}$ goes low. Check the timing diagrams for the device against the timing diagram for the Quark given in Figure 1. If the Address and $\overline{CS}$ lines need not be stable before the $\overline{WR}$, then connect the device as shown in Figure 2. Alternatively, if the $\overline{CS}$ must be stable before the $\overline{WR}$ goes low, then connect the device as shown in Figure 3.

To connect 6500- and 6800-compatible devices, the E-clock output and the $\overline{WR}$ line are used. For these devices, the $\overline{WR}$ line functions as the 6500/6800 RD/$\overline{WR}$ line. See Figure 4.

The Z80B's Interrupt Input line ($\overline{INT}$) is available on the Peripheral Expansion Interface to allow external devices to generate interrupts to the Z80B. The active-low Power-On-Reset output ($\overline{POR}$) is also provided to reset external peripheral devices. Finally, a decoded active-low chip-select line ($\overline{CS}$) corresponding to I/O address between C0 and FF (hex) is created on-board and can be used to select a single external peripheral device, or to qualify the decoding of some of the address lines for several external chip-select lines. See Figure 5. Figure 6 illustrates an application of this decoding process.

The $\overline{POR}$ output on the Peripheral Expansion Interface is an active-low buffered reset output which should be used in resetting external peripheral devices. Note that 8080-type devices require an active-high reset signal, so the $\overline{POR}$ line would have to be inverted to service these devices.

To ease timing requirements for interfacing external peripheral devices to the 6MHz CPU, four wait states are added to all I/O cycles. These four T-states are in addition to those which are added to extend every memory cycle to mod-4 T-states. Thus an I/O instruction which would execute in 10 cycles, for example, would be first extended to 12 cycles and then further extended to 16 cycles. This relaxes the bus timing requirements for I/O operations, thus allowing lower speed and lower cost peripheral devices, such as "A"-version (1.5MHz) 6800/6500 devices, to be used.

If several external peripheral devices are to be connected to the Quark's Peripheral Expansion Interface, or if the Interface's lines are to be extended any significant distance, it is recommended that the address, data, and control lines being used be buffered by TTL drivers. Figure 7 shows a schematic for buffering all of the available data and address lines, and some of the control lines. Two TTL packages are sufficient for this purpose if only 8080- or only 6500/6800-type peripheral chips are used. If both types are employed then an additional buffer is necessary, unless five or fewer address lines are required.

Megatel offers a number of Quark Transition Board (QTB) products to assist the user in the use of the Quark and its Peripheral Expansion Interface. For information on any of these products, or for further technical support on the use of the Interface, please contact the factory or your local distributor.

 Order #QT000040-R1

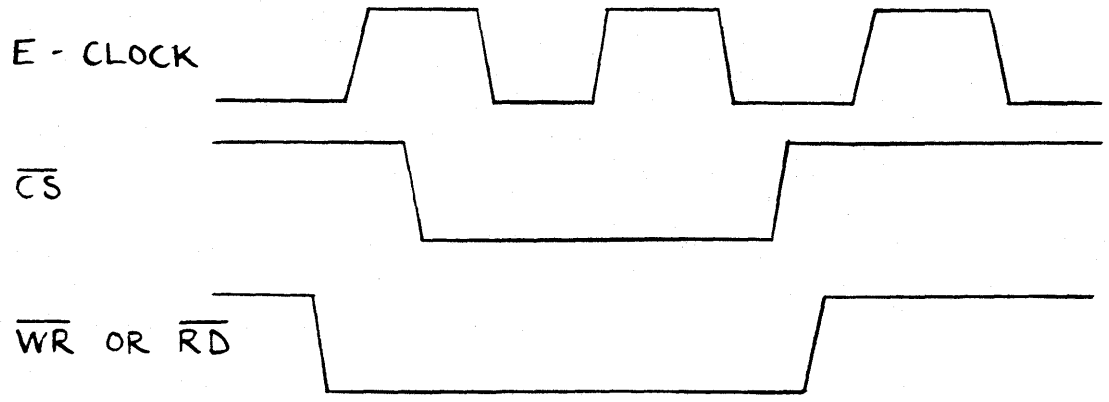


FIGURE 1. Relative Signal Timing on the Peripheral Expansion Interface

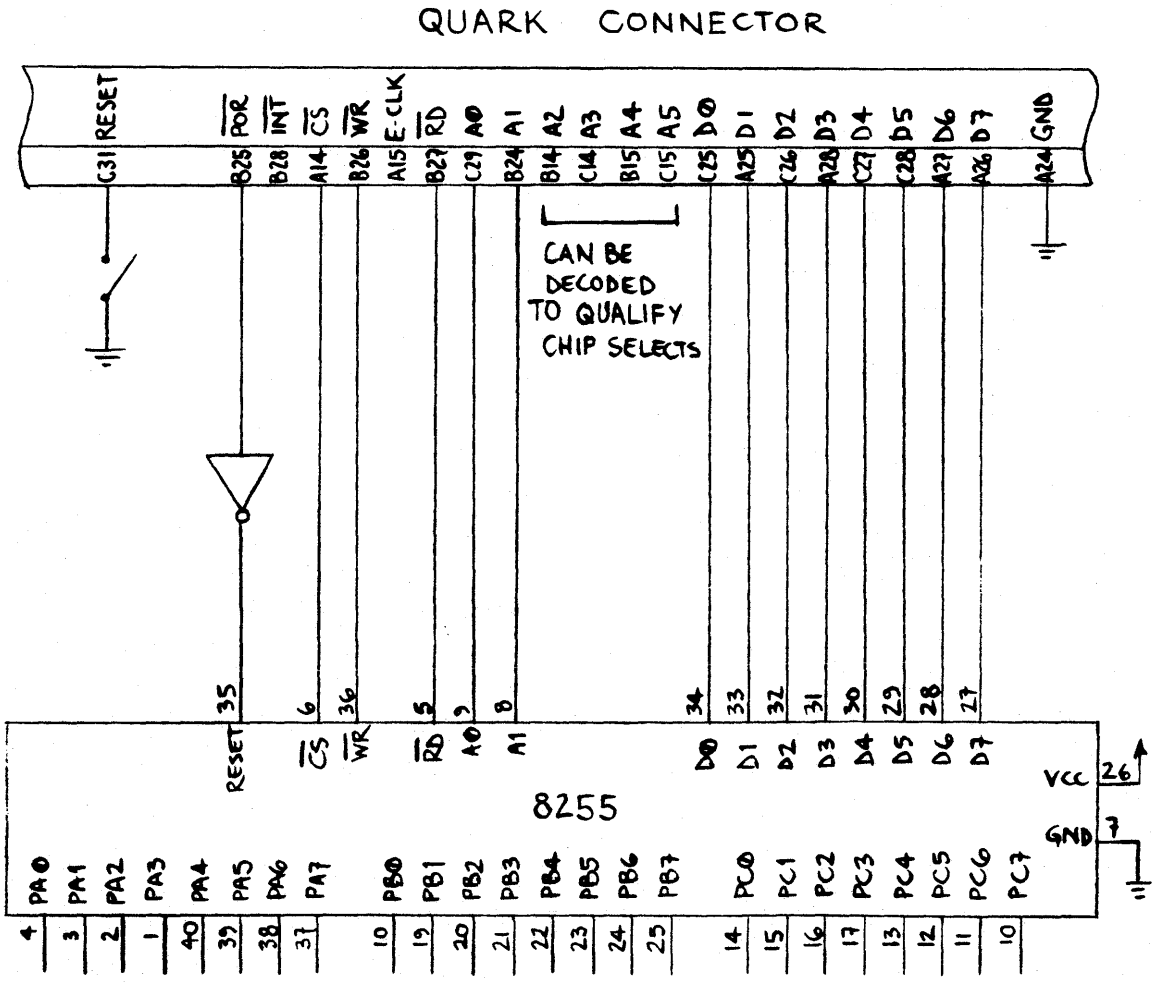
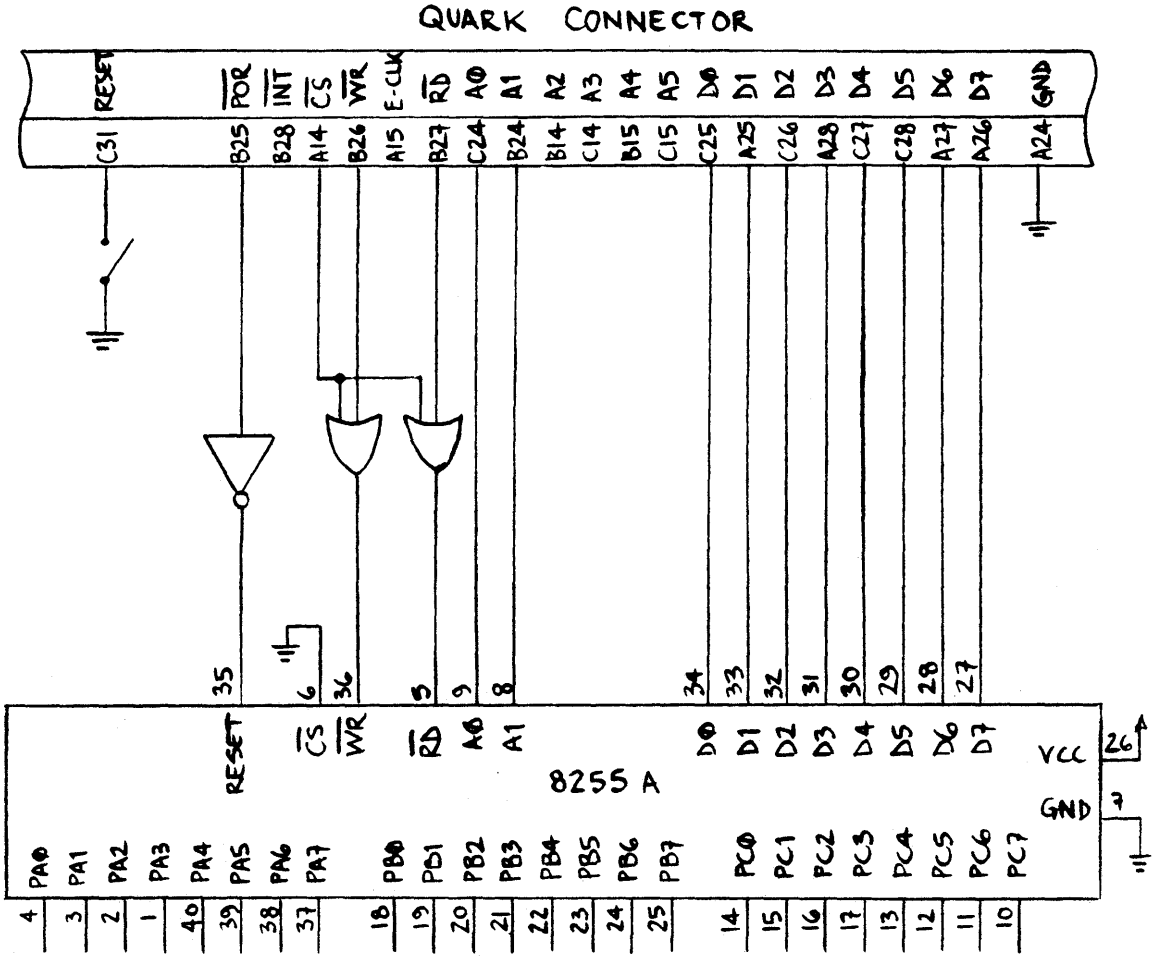
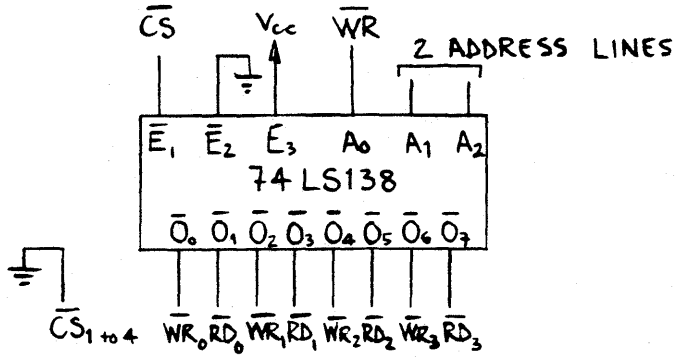


FIGURE 2. Adding a Single "Non-A" 8080-type Device



Adding a single 8080A-type device.



Decoding multiple pairs of $\overline{RD}$ and $\overline{WR}$ lines.

FIGURE 3. Adding "A"-version 8080-type Devices

The USER $\overline{CS}$ is used to gate the $\overline{RD}$ and $\overline{WR}$ control outputs.

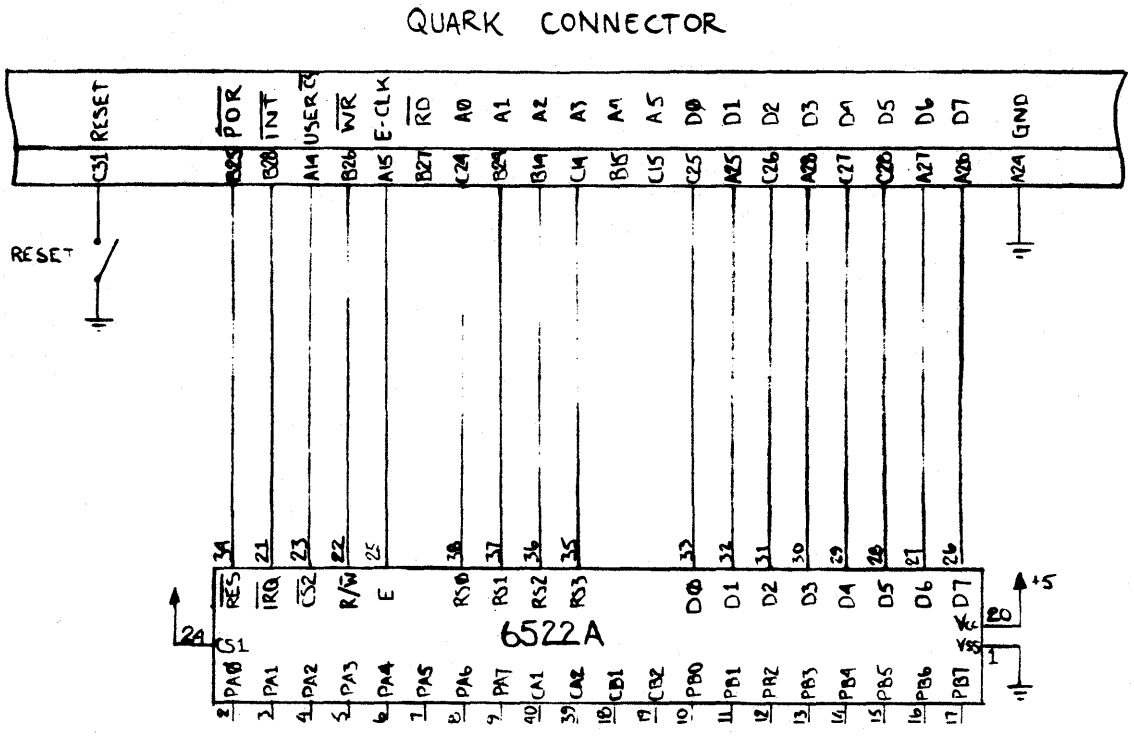
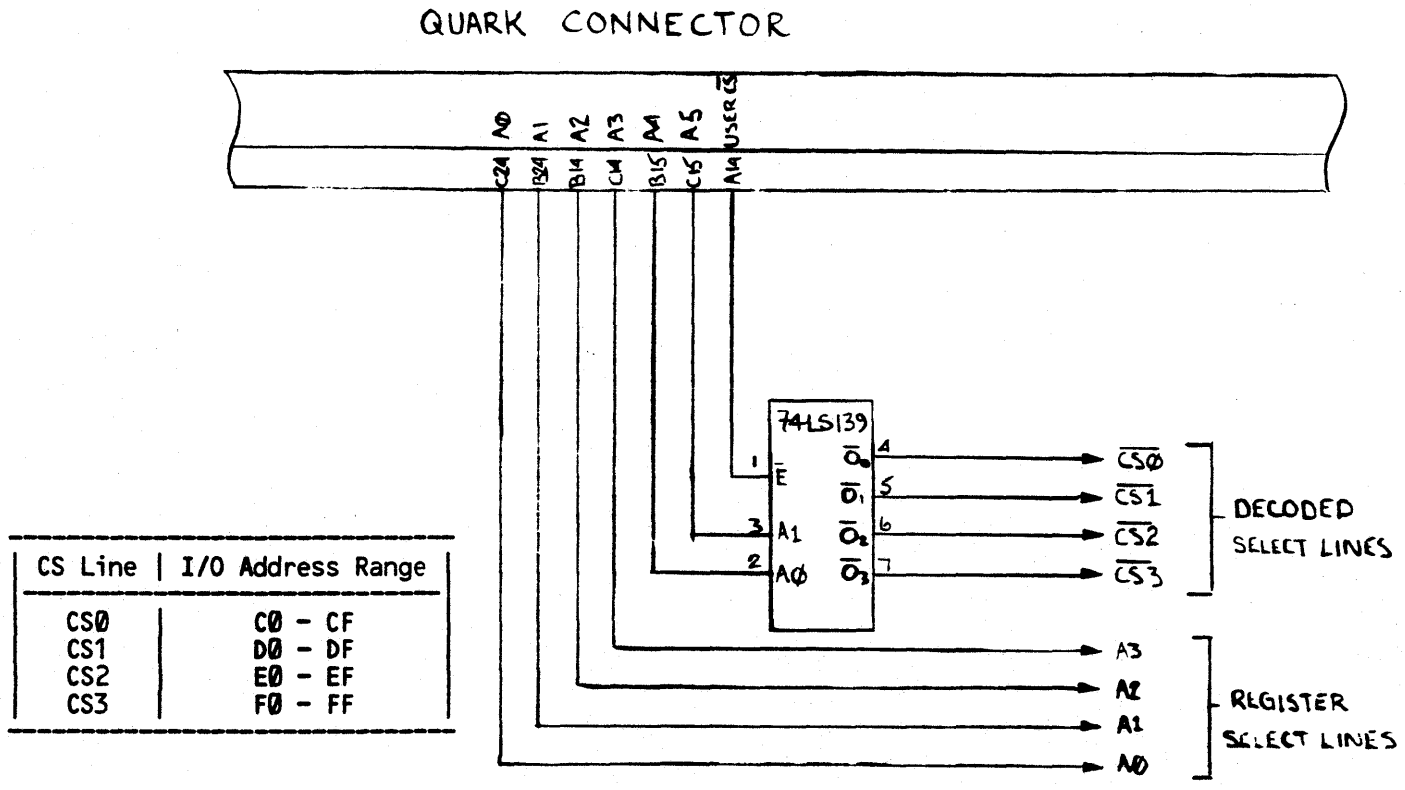
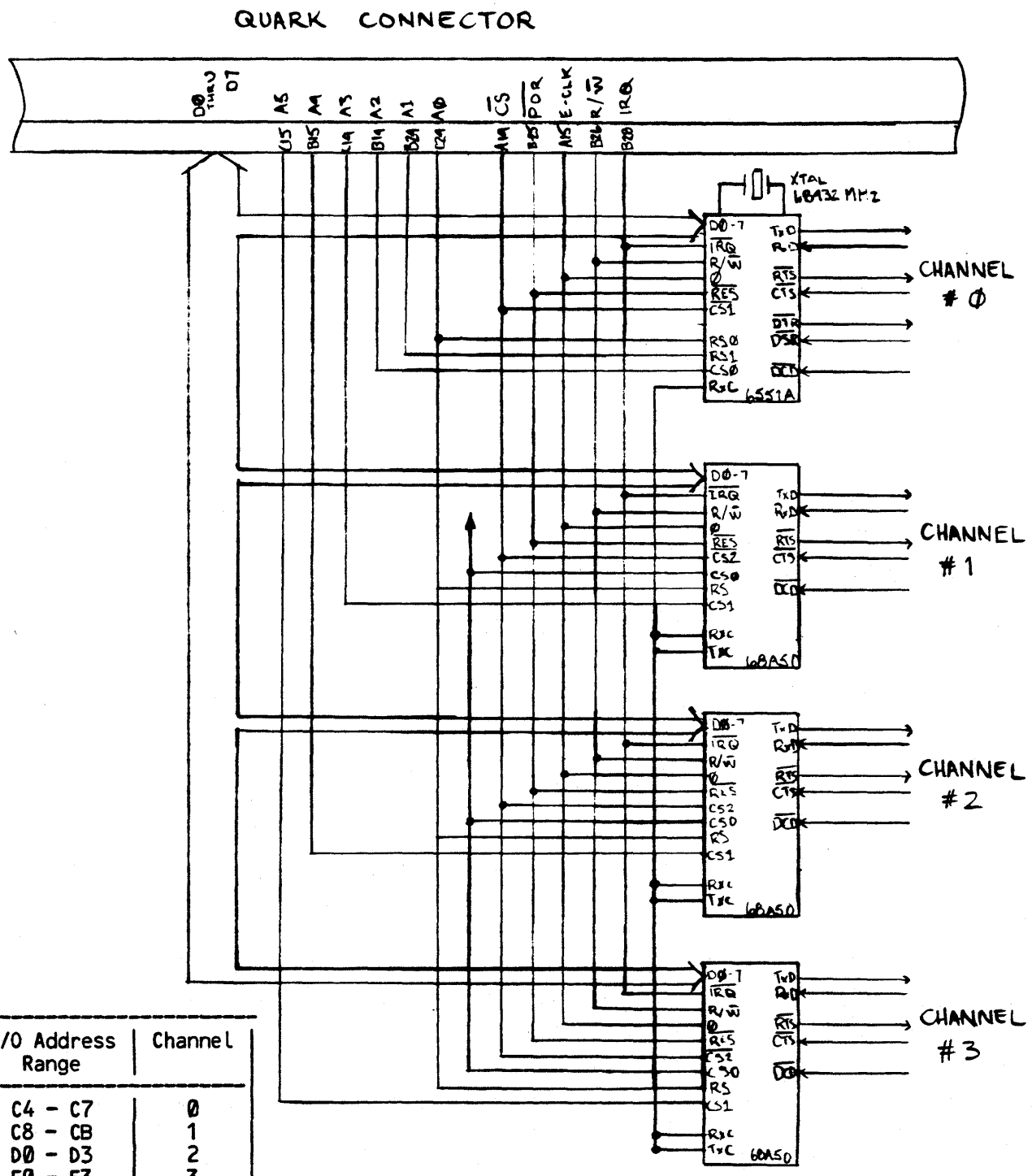


FIGURE 4. Adding a Single 6500/6800-type Device



CS Line	I/O Address Range
CS0	C0 - CF
CS1	D0 - DF
CS2	E0 - EF
CS3	F0 - FF

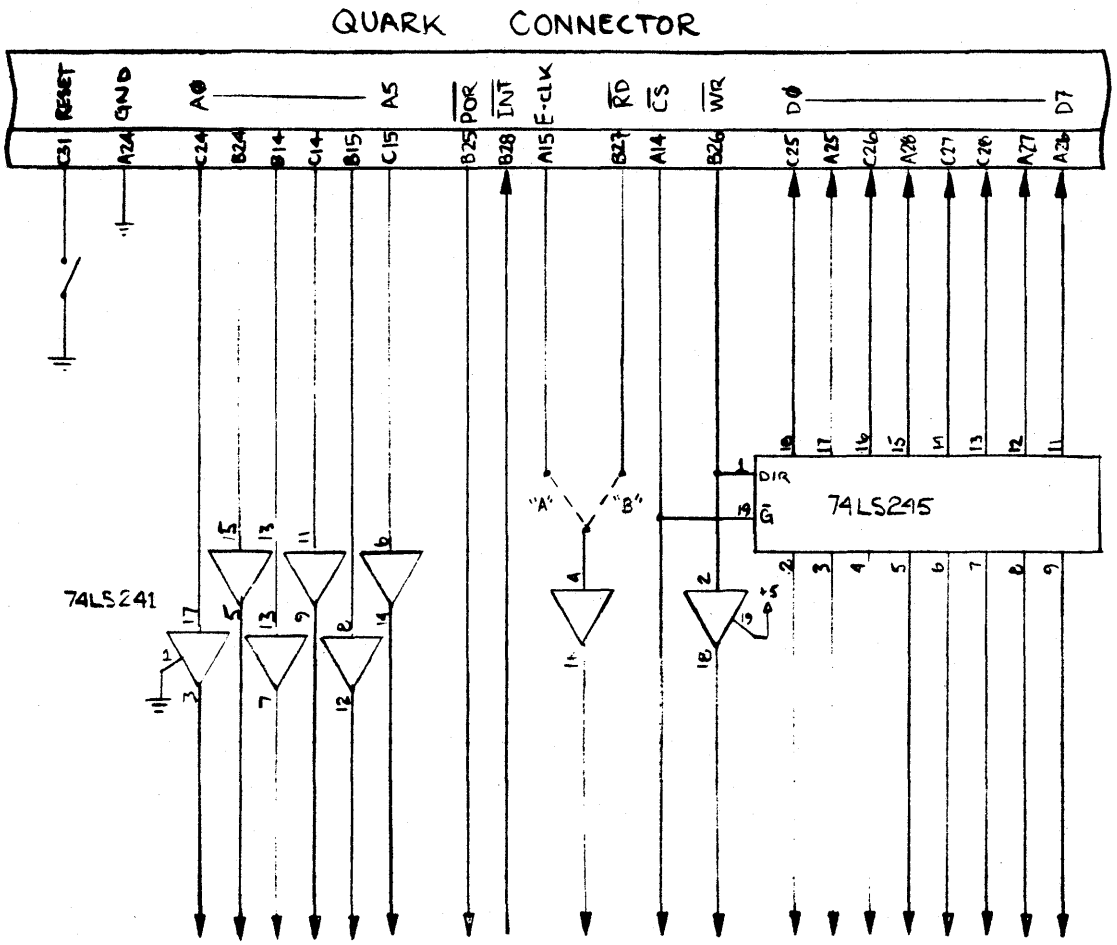
FIGURE 5. Decoding Four Chip-Select Lines Using USER $\overline{CS}$ and Two Address Lines



I/O Address Range	Channel
C4 - C7	0
C8 - CB	1
D0 - D3	2
E0 - E3	3

Baud rates for all channels are generated by the 6551A. RS-232C drivers and receivers are not shown for simplicity.

FIGURE 6. Adding Four External Asynchronous Serial Channels



Use connection "A" for 6500/6800-type devices. Use connection "B" for 8080-type devices. To use both types, add an additional buffer.

FIGURE 7. Buffering the Peripheral Expansion Interface

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