MSV05 / MSV05B
Tape Controller Manual

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MICRO TECHNOLOGY, INCORPORATED

This document is intended to provide the user with detailed information sufficient for the understanding, installation and use of the equipment involved.

Every effort has been made to ensure the information contained herein is current and accurate as of the date of publication, however no guarantee is given or implied as to its accuracy.

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Contents

Appendix

Tables

Figures

Section 1

General Information

1. OVERVIEW

The MSV05B is a single dual height module interfacing a wide variety of standard QIC-02 interface 1/4" cartridge tape drives to the Q-22 LSI-11 bus. The MSV05B controller, together with the 1/4" cartridge drive emulates the DEC TSV05 subsystem except for the constraints outlined in this document. The MSV05B contains a set of built in diagnostics which assures the integrity of the controller whenever it is initialized or first powered up.

1.1. APPLICABLE HARDWARE

This document describes the functionality and use of the Micro Technology MSV05B cartridge tape controller. The MSV05B controller is compatible with the LSI-11, LSI-11/2, LSI-11/23, LSI-11/73 CPU's and the Micro-Vax processors. All the circuitry is contained on one dual-height board that plugs directly into any standard Q-22 LSI-11 backplane. Alternate address, vector selection, and optional configuration jumpers provide the user added flexibility for various drive and system configuration. The controllers support block mode DMA which can be enabled or disabled at the user's option. The controllers interface to most QIC-02 type drives through a 50 conductor flat ribbon cable.

1.2. GLOSSARY OF TERMS

Table 1-1 is a list of terms that will be used within this document. Included with each term is its definition.

Terms	Definition
Command Packet (I/O Request)	A set of control words issued from the CPU (i.e., operating system, I/O driver or diagnostic program) to the MSV05B to initiate and control operation.
Command Buffer	An area of contiguous 16-bit words in the host CPU's memory space. The I/O Request Packets are built there and are retrieved by the MSV05B.
Command Pointer	The high (most significant) 16 bits of an 18-bit Modulo-4 address which points to a Command Packet located in the CPU's memory space. In extended operation, "Command Pointer" refers to the high 20 bits of a 22-bit Modulo-4 address which points to a Command Packet located in the CPU's memory space.
Header Word	The Header Word is the first word of a Command Packet or a Message Packet.
Message Buffer	An area of contiguous words in the CPU's memory space. The Message Packets are stored there by the MSV05B.
Message Packet	A group of status words issued from the MSV05B to the CPU to indicate status of the magtape subsystem and/or operation completed.
Modulo-4 Address	An address within the CPU's memory space that is evenly divisible by 4 (i.e., octal 0, 4, 10, 14, 20, etc.)
Packet	A contiguous sequence of words.
Q-22	LSI-11 system bus containing 22-bit memory addressing capability.

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Table 1-1 Glossary of Terms

Terms	Definition
Streaming Technology	Operation of a magtape transport without stopping in the interrecord gap. Requires that, for maximum efficiency, commands of similar type, speed and direction be supplied by the controller within a relatively short "reinstruct" period. The 1/4 inch streaming QIC-02 cartridge drives operate in this fashion.
Conventional, or Stop/Start Technology	Operating characteristic of a magtape drive that can rapidly accelerate and decelerate tape motion to allow the tape to come to rest with the read/write head positioned in the interrecord gap.
Reinstruct Time	The period of time following reading or writing the last character of a record allowed by a tape transport for a controller to issue the next command in order to avoid slowing or stopping the tape.
Access Time	The time between issuance of a tape read, write or space command (by the controller) and the reading or writing of the first character in the target tape record.
Command Delay	The elapsed time between the indication from the controller signifying the completion of an operation (e.g., Read or Write) and the issuance of the next command to the controller by the operating software.
Repositioning	A characteristic of a streaming tape drive whereby tape motion is halted and the tape is readied for the next operation by decelerating the tape current direction and bringing it to a stop, then accelerating and decelerating the tape in the opposite direction and bring it to a stop. The tape is not stopped in the gap, as with conventional tape drives.

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Table 1-1 (cont'd) Glossary of Terms

Term	Definition
Record Buffering	Capability of the MSV05B to store an entire tape record, up to 15872 bytes in length, during Read or Write command sequences to allow overlapping of tape repositioning with transfer of data to/from the CPU.
Packet Protocol	Method of communication between CPU software and the MSV05B via areas in CPU memory space, following the rules dictated by DEC's TSV05 compatibility requirements. A "packet" is a contiguous series of words residing in CPU memory space. The MSV05B accesses a Command Packet (in a Command Buffer area in CPU memory space) to provide status information to the software. This technique allows large amounts of information to be passed while allowing the device to occupy only two hardware I/O addresses.
MSDB	MSV05B Data Buffer Register -- a Write-Only hardware register in the I/O address space.
MSBA	MSV05B Bus Address Register -- a Read-Only hardware register in the I/O address space
MSSR	MSV05B Status Register -- A Read/Write register in the I/O address space
MXSTn	Extended Status Register n -- one of five status registers deposited into the Message Buffer area.
Extended Features	Mode of operation of the MSV05B that extends the functionality of the subsystem beyond that allowed by DEC's TS11/TS04 compatibility. Includes 22-bit memory addressing and additional status and functions. Requires use of special software, which is not supplied and/or may not exist.
BOT/EOT	Beginning of Tape and End of Tape markers which mark the physical beginning and end of tape, respectively.

Table 1-1 (cont'd) Glossary of Terms

1.3. FUNCTIONAL OVERVIEW

The functions listed in Table 1-2 summarize the MSV05B Subsystem Command Set. These commands utilize "command packets" stored in the computer system's memory to operate the transport and transfer data. Some commands have various sub-commands, termed "modes". The interface's device registers are used to initiate command packet processing and retrieve basic status. This section describes register manipulation and provides an overview of packet protocol (the format used to transfer commands and data). A detailed description of the commands is provided in another section of this document.

The MSV05B has four device registers which occupy only two LSI-11 Bus word locations: a Data Buffer (MSDB), a Bus Address Register (MSBA), a Status Register (MSSR), and an Extended Data Buffer (MSDBX). The MSDB is an 18-bit register that is parallel loaded from the LSI-11 Bus. A 16-bit portion of this register is used as a word buffer register; it is written into by the host CPU to initiate an operation. The MSDB can be loaded from the LSI-11 Bus by four different transfers from the CPU. Three transfers are for maintenance purposes (not supported, controller reports special condition with register modification refused bit set) and the fourth is for the normal word transfer (DATO) to initiate an operation. This register is write-only and is not cleared at power on, subsystem initialize, or bus initialize. This register can be loaded without the tape transport connected, since all controller functions reside within the controller.

Commands are not written to the MSV05B's LSI-11 Bus registers. Instead, command pointers, which point to a command packet somewhere in CPU memory space, are written to the MSDB register. The command pointer is used in the MSV05B subsystem to retrieve words in memory called the Command Packet. The words in the Command Packet instruct the system as to the function to be performed. These words contain function parameters such as bus address, byte count, record count, and modifier flags.

The MSBA is an 18-bit register (22-bits when the extended features jumper is enabled) that is parallel loaded from the MSDB whenever the MSDB is written. MSBA bits 1 and 0 are always zero specifying a modulo-4 address. MSBA bits 15-2 are loaded from MSDB bits 15-2. MSBA bits 17 and 16 are respectively loaded from MSDB bits 1 and 0. MSBA bits 17 and 16 are displayed in MSSR bits 9 and 8, respectively. When extended features is enabled the MSBA is extended to 22 bits by first loading the high byte of the MSSR with bits 21-18 of the MSBA. If extended features is disabled these bits are ignored. The MSBA is incremented by two for DMA word transfers or by one for DMA byte transfers.

Command Names	Mode Name/Description
Get Status	Get Status (update the Extended Status registers in the message buffer in memory)
Read	- Read Next (Forward) - Read Previous (Space Reverse - Read Forward - Space Reverse)* - Reread Previous (Space Reverse - Read Forward)* - Reread Next (Read Forward - Space Reverse)*
Write Characteristics	Load Message Buffer Address and Set Device Characteristics
Write	- Write Data - Write Data Retry (Illegal Function Reject)
Position	- Space Records Forward - Space Records Reverse** - Skip Tape Marks Forward - Skip Tape Marks Reverse** - Rewind
Format	- Write Tape Mark - Erase - Write Tape Mark Retry (Illegal Function Reject)
Control	- Message Buffer Release - Rewind and Unload - NOP (Retension Tape) - Rewind with Immediate Interrupt
Initialize	Controller/Drive Initialize
Write Subsystem Memory	Diagnostic Function (Illegal Function Reject)

*These commands are currently rejected but are under consideration based on software requirements

**These commands are supported with limitations as to the number of tape marks skipped or records spaced.

Table 1-2 Legal Command Mode Summary

The MSBA register is used for two purposes. As a command pointer to the functional device registers, the MSBA is used as a pointer to the command and message buffers located in the LSI-11 address space. As a data pointer, the MSBA is used as an address pointer to the LSI-11 address space during data transfers between the drive and the host CPU memory.

The MSSR is a 16-bit register that can be updated only from the controller logic. It cannot be modified from the LSI-11 Bus. In this register, major system status can be observed.

Before the MSV05B can begin a function, a command packet must be assembled in the CPU's system memory. In every case, the packet requires all four words. The packet may be thought of as being three remote device registers, some of which are not used for non-data transfer commands (Figure 1-1):

1. Command Register (CMDR)

2. Data Pointer (DPR) which is comprised of two word locations:

   a. CMDR+2: Low order address word (A15:00)

   b. CMDR+4: High order address word. In standard mode, only bits 1 and 0 of this word are used, specifying address bits A17 and A16. Loading the high byte of the MSSR first, 22-bit addressing mode can be specified, (if extended features is enabled), in which case bits 5-2 are used to specify address bits A21-A18.

3. Positive Byte Count Register (BCR):

   a. CMDR+6: Data operations (DPR required)
   b. CMDR+2: Non-data operations (no DPR required)

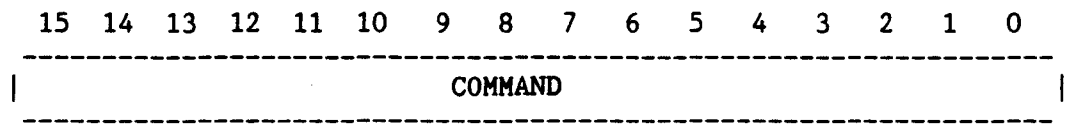
The command pointer must be an address on a modulo-4 boundary (i.e. octal 0, 4, 10, etc.) due to the address limitations of the MSBA register.

The command register is decoded by the controller logic and if valid initiates the appropriate function. Detailed function description are provided in the following sections. The data pointer register (DPR) is loaded into the MSBA to be used as the LSI-11 Bus address for DMA transfers. The Byte Count Register (BCR) is used to indicate the number of bytes (8 bits of data per byte) to be moved to or from the drive during a data transfer. It is also used to specify the number of records in a space record command or the number of files in a skip tape marks command.

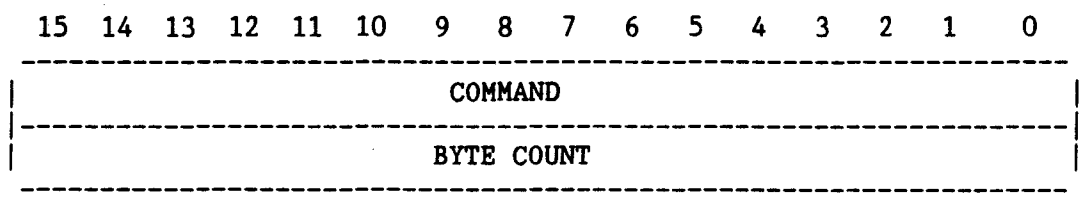
Message packets are sent by the controller to the host CPU memory space. Proper operation of the controller requires a message buffer address. This buffer address is specified on a write characteristics

command and must be the first command issued to the controller after an initialize. Otherwise, all other commands will be rejected.

1 - Word Type



2 - Word Type



4 - Word Type

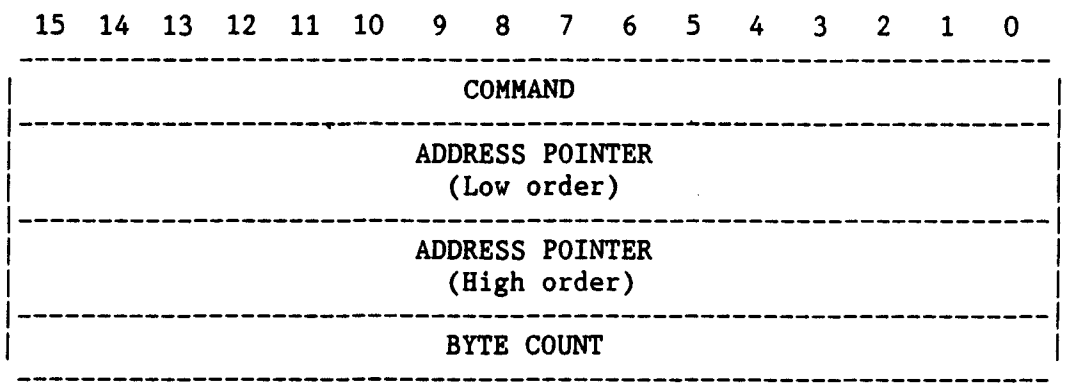


Figure 1-1 Command Packets

1.4. SPECIFICATIONS

1.4.1. Mechanical

Size: Dual-height, standard length module.

Connectors: Two connectors used:

1. Standard Q-22 LSI-11 bus edge connector using the A and B rows
2. 50 pin right angle flat cable connector located at the handle end of the module for interface to industry standard QIC-02 drives.

Jumpers: Jumpers are available to select address, vector, interrupt priority, block mode control, extended features, and various drive characteristics.

Indicator: Single LED used to indicate that the controller passed internal diagnostics initiated during initial power up. Upon successful completion the LED stays on continuously.

1.4.2. Electrical

Power requirements	+5VDC ± 5% at 3.0 Amps (max.)
LSI-11 bus loading:	1 DC bus load 2 AC bus loads
LSI-11 bus interface:	Adheres to the Q-22 specification but does not generate or check parity. Only uses the A and B rows. Receives the following LSI-11 bus signals: BDAL00-BDAL21, BDIN, BDOUT, BSYNC, BRPLY, BWTBT, BBS7, BIRQ4, BIRQ5, BIRQ6, BIAKI BDMGI, BSACK, BINIT, BREF Drives the following LSI-11 bus signals: BDAL00 - BDAL21, BDIN, BDOUT, BSYNC, BRPLY, BWTBT, BBS7, BIRQ4, BIRQ5, BIAKO, BDMR, BDMGO, BSACK

Does not interface the following LSI-11 bus signals:

BHALT, BDCOK, BPOK, BEVNT

Drive interface: Adheres to the ANSI X3T9.6183-20 specifications - QIC-02 device level interface for streaming cartridge tape drives.

Transmitter:
Signal assertion = 0.0VDC to 0.4VDC
Min drive capability = 24 ma (sink) @ 0.50VDC
Signal non-assertion = 2.5DC to 5.25VDC
Signal type = Tristate

Receiver:
Signal assertion = 0.0VDC to 0.8VDC
Input load (max.) = 0.4ma @ 0.4VDC
Signal non-assertion = 2.0VDC to 5.25VDC
Hysteresis (min) = 0.2VDC

Receives the following signals:

CB7, CB6, CB5, CB4, CB3, CB2, CB1,
CB0, ACK, RDY, EXC, DIR

Transmits the following signals:

CB7-CB0,
ONL, REQ, RST, XFR

Does not interface to the following signals:

CBP

1.4.3. Environmental

Temperature: 5 to 50 degrees C (41 to 122 degrees F)

Humidity: 10% to 90% (non-condensing)

1.4.4. Performance

Transfer rate: Burst 200 Kbytes/sec
Average 86.7 Kbytes/sec

Capacity: Limits established by drive characteristics and tape length.
Note: It is not advised to use

300 ft. tapes due to the fact the tape characteristics will not function reliably with streaming cartridge drives. The MSV05B controller measures tape length and will reject the 300 ft. tape with function reject error.

1.4.5. Reliability

MTBF	32,300 hrs.
MTTR	.5 hr.

1.5. COMPATIBILITY

1.5.1. Hardware

The MSV05B controller is compatible with the LSI-11, LSI-11/2, LSI-11/23, LSI-11/73 CPU's and the Micro-Vax processors. All the circuitry is contained on one dual-height board that plugs directly into any standard Q-22 LSI-11 backplane. Alternate address, vector selection, and optional configuration jumpers provide the user added flexibility for various drive and system configuration. The controllers support block mode DMA which can be enabled or disabled at the user's option. The controllers interface to most QIC-02 type drives through a 50 conductor flat ribbon cable.

Device Address:	
Standard	772520
1st Alternate	772524
2nd Alternate	772530
3rd Alternate	772534

Device Vector:	
Standard	224
1st Alternate	floating (jumper selectable)
2nd Alternate	floating (jumper selectable)
3rd Alternate	floating (jumper selectable)

Interrupt Priority:	
Standard	level 5
Alternate	level 4

Jumper Options:	
Block Mode Control	Enables block mode DMA

Extended features	Enables 22-bit addressing
Drive Configuration	Configures the controller for various drive features

Features:

22-bit Addressing	The MSV05B controller generates a 22-bit address compatible with DEC's TSV05 when Extended Features are enabled. When Extended Features are disabled the MSV05B generates an 18 bit address compatible with DEC's TS11.
Record Buffering	The MSV05B uses a record buffering technique to optimize operation of streaming tape drives. Records are buffered in an on board 16K byte buffer to avoid the inherent long respositioning delay associated with streaming drives. Reading from the tape operates in the opposite fashion. Records are buffered in the on board buffer to allow for both software overhead and target device latency
Micro Diagnostics	Internal diagnostics check various controller components in order to insure proper operation of the MSV05B. These include: a. Basic Processor tests b. Scratch RAM test c. Host DMA controller test d. Drive DMA controller test e. RAM buffer test

1.5.2. Software

The controller is compatible with DEC's TSV05 packet protocol and emulates the TSV05 subsystem within the constraints of the streaming cartridge drive. The product is designed to operate with the basic utilities in DEC's RT11, RSTS, and RSX11M operating systems such as PIP, BRU, DSC, etc. In addition, the new utility BUP (RT11) is supported and provides an excellent high speed backup utility optimized for use with RL02 and TSV05 products. Diagnostic software is supplied to insure that the controller is functioning properly.

1.5.3. Media

The DEC TSV05 subsystem is based on industry standard 1/2" 9 track tape recorded at 1600 BPI in various formats. The most common format is ANSI standard and provides a convenient means of interchange in both the DEC community and with other available systems.

The MSV05B interfaces most QIC-02 compatible drives. The predominant manufacturers use the 1/4" cartridge tapes and record in what is termed QIC-24 format.

Since the tapes written on these drives are QIC-24 format compatible it is possible to use drives available from various manufacturers maintaining compatibility.

Cartridge drives implementing the QIC-120 format provide increased data storage capacity while maintaining read compatibility with QIC-24 format tapes. These QIC-120 drives will write one 600 ft. tapes only; other length tapes are rejected by the drive.

1.6. PRODUCT FEATURES

The MSV05B is a cost effective back up device for the DEC compatible marketplace. Emulating the TSV05 subsystem this product interfaces with standard QIC-02 compatible streaming drives. All electronics are contained on a single dual-height controller and interface to drive on a single 50 conductor flat ribbon cable. Either the 5 1/4" full or half height drives provide an excellent package for small system or table top applications. The major features include:

- o dual height board
- o 22-bit addressing
- o block mode DMA support
- o extended features options
- o TSV05 compatibility
- o interface with low cost QIC-02 cartridge streaming drives

1.6.1. Multi-Volume Support

In order to properly write data across volume boundaries, it is necessary to identify the end-of-tape (EOT) as with 1/2 inch tape. For 1/2 inch tape, EOT is a warning and a limited amount of information can continue to be written to the tape. Since the physical EOT on the

streaming type drives allows only two blocks to be written, a logical EOT (LEOT) was needed.

In order to generate a LEOT status, the cartridge/drive type, number of tracks and tape length are needed. The first two pieces of information are provided with jumpers on the controller. Tape length must be measured. Revision C and later versions of the firmware implement a sizing algorithm described as follows:

When a tape cartridge is inserted, it is rewound to BOT and an attempt is made to read the first block. If a valid header is read with a valid tape length, the tape is rewound and the length is saved. If an error occurs during the first read or the length is 0 (as for tapes written with older firmware), the tape is measured by timing a retension pass, and the length is saved. On the first write to tape, the length is saved. Subsequent use of the cartridge will not require resizing since the length is stored on tape.

The cartridge tape lengths that are currently supported are:

150 feet
450 feet
555 feet
600 feet

Please note that a 300 ft cartridge will cause abnormal tape head wear and is not recommended by the QIC-02 drive manufacturers. An attempt to write on a 300 ft cartridge will result in a Function Reject termination.

Media types other than cartridge are rewound to BOT only, and no sizing is done since the length is determined by jumpers.

Multi-volume copies are supported for the following utilities:

RT11	BUP
RSX	BRU
	DSC
	PIP
RSTS	SAVRES
	PIP

When copying to a tape, if the LEOT is encountered, the behavior of the copy is the same as for 1/2 inch tape. The volume will be rewound and unloaded and a message will be displayed on the operator's console to change the tape. The controller will poll the drive for a new cartridge inserted status, size the tape if required (in the off-line mode) and then go on-line, allowing the copy to continue.

1.6.2. File Utility Support

An overwrite scheme has been incorporated which allows the controller to closely emulate the full start stop features of the 1/2 inch tape products. The MSV05B supports RSX PIP and RSTS PIP in either ANSI or DOS format. Additional file utility support is under current evaluation.

1.6.3. QIC-11 Tape Format Support

When appending to information on the tape, the MSV05B has taken advantage of QIC 24 format which erases a leader past the last written block as a clear delineation of the end of recorded media. The QIC-11 format does not provide this erased area at the end of recorded media and prevented the previous firmware versions of the MSV05B from using this format. Since there is a substantial installed base of QIC-11 format drives, features have been added to eliminate this problem. An erase tape command has been added to provide a means of erasure other than bulk erasing. The TSV05 erase tape command is used with a second word for qualification to prevent accidental erasure. While erasing, the tape length is measured, and when complete, a header containing the length is written to tape so that further sizing is not needed.

To invoke this command with ODT, deposit 100411 (8) in any modulo 4 memory location (eg., 1000 (8), 1004(8) or 1010(8)) and 1234(8) in the next location. Then write the first address to MSV05B base address (772520(8) is standard address). A retension command is also available and can be invoked in a similar manner with a command word of 101012. A qualifying word is not needed for retension.

1.7. PRODUCT LIMITATIONS

The MSV05B controller emulates the TSV05 subsystem within the constraints of the available 1/4" cartridge streaming tape drives. The major limitation imposed by these drives is their inability to overwrite existing files. This limitation prevents the MSV05B from implementing any function which implies a destructive write. These functions include:

write data retry

erase

write tape mark retry

positioning to previously recorded data and writing

The controller responds to these functions with an illegal function reject. Both the write data retry and the write tape mark retry are not necessary because of the automatic verification rewrite logic imbedded within the drive. The erase function is typically not used.

Positioning functions such as Space Records Forward, Space Records Reverse, Skip Tape Marks Forward, and Skip Tape Marks Reverse are implemented to the extent that they will allow proper operation of DEC operating systems and utilities. These commands are supported with limitations as to the number of tape marks skipped or records spaced.

Any attempt to position the tape to previously recorded data and to subsequently overwrite is inhibited by most of the available 1/4" cartridge tape drives. Overwriting is prevented because of the unsaturated recording method and the lack of a track erase head. An erase bar is available to write on track 0 while simultaneously erasing the full width of the tape. Under normal use the operating systems software does not implement destructive writes. The MSV05B incorporates a pseudo-overwrite which allows it to overwrite a limited number of blocks. This number is sufficient to allow proper operation of most DEC software.

There are optional software switches available to allow the user to overwrite either files or records on the tape. These commands/switches must be avoided and if used will result in illegal function or various error conditions presented to the software drivers.

Section 2

Installation

2. GENERAL

The MSV05B controller is shipped with the standard options configured. The primary address and vector are configured to 172520(8) and 224(8), respectively, the device interrupt priority is set to level five, the extended features option is enabled and the automatic retension option is disabled.

2.1. CONFIGURATION

Refer to Table 2-1 for a summary of the factory options. As delivered, the controller will be configured for proper operation with standard 9 track QIC-02 interface tape drives. Refer to Tables 2-2, 2-3 and 2-4 for alternate options regarding the selection of the controller's base address, interrupt vector address and interrupt priority level. The physical location of the jumpers is shown by Figure 2-1.

Several of the options are selectable by using BERG 76264-101 pin jumpers. If these or similar pin jumpers are not available use #30 wire wrap.

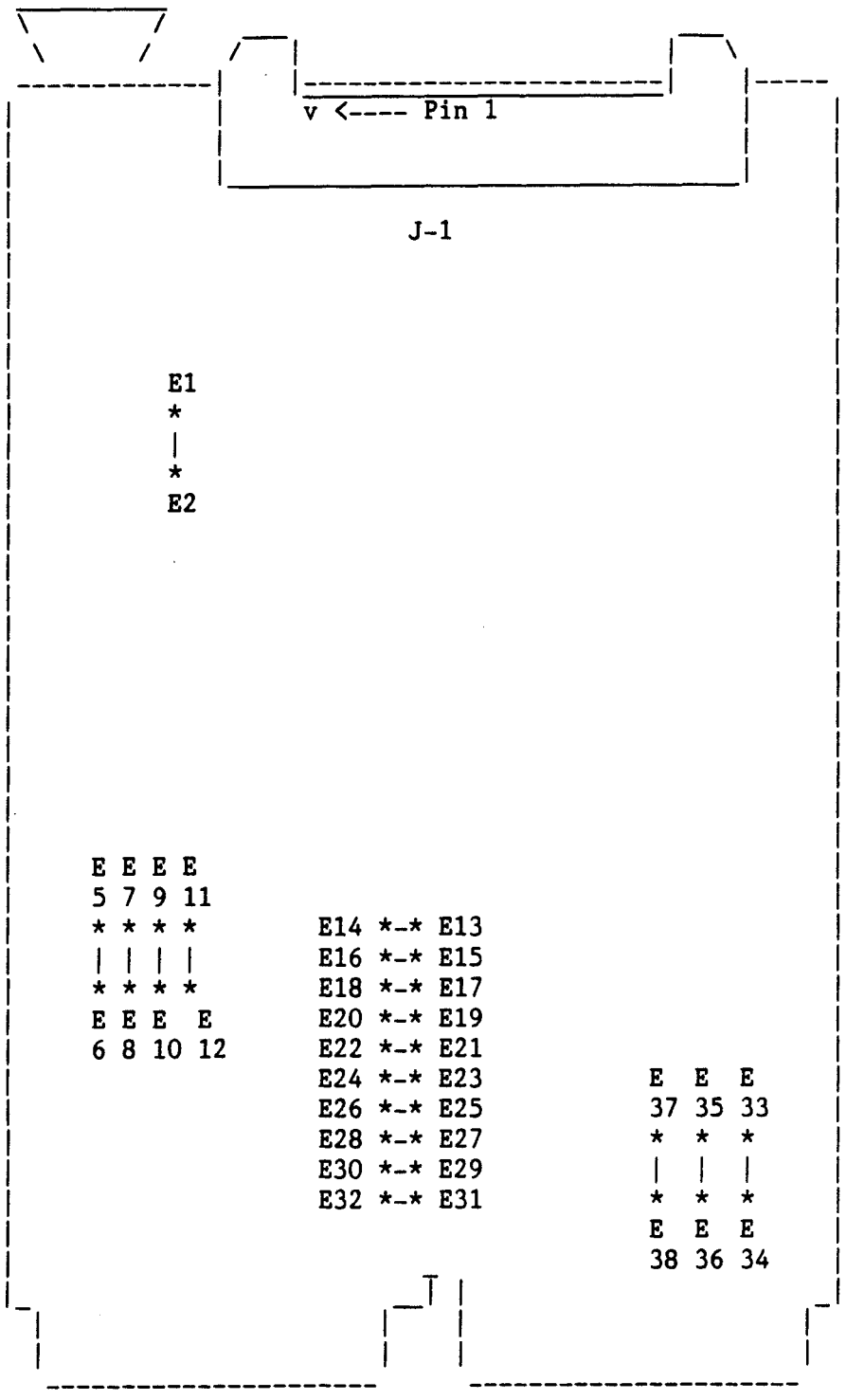


Figure 2-1 MSV05B Configuration Jumper Locations

JUMPER	USAGE	STATUS
E1 - E2	Not used	NA
E5 - E6	Retension Option (Disabled)	OUT
E7 - E8	Diagnostic enable (Disabled)	OUT
E9 - E10	Address Select Bit 0-----+	IN
E11- E12	Address Select Bit 1--+ |	IN
	| |	
	IN = 0 0 0 = 772520	
	OUT = 1 1 0 = 772524	
	0 1 = 772530	
	1 1 = 772534	
E13- E14	Drive Configuration 2 (See Table 2-6)	IN
E15- E16	Extended Features enable	IN
E17- E18	Drive Configuration 0 (See Table 2-6)	OUT
E19- E20	Drive Configuration 1 (See Table 2-6)	OUT
E21- E22	Interrupt Vector Bit 7	OUT
E23- E24	Interrupt Vector Bit 6	IN
E25- E26	Interrupt Vector Bit 5	IN
E27- E28	Interrupt Vector Bit 4	OUT
E29- E30	Interrupt Vector Bit 3	IN
E31- E32	Interrupt Vector Bit 2	OUT
E33- E34	Interrupt Priority Level 5	IN
E35- E36	Interrupt Priority Level 4	OUT
E37- E38	Block Mode DMA enable	OUT

Table 2-1 Factory Option Summary

2.1.1. Address/Vector Selection

The controller is shipped with the primary device address and vector assignments preset to 172520(8) and 224(8), respectively. Three alternate address assignments are available using jumper options. The alternate address assignments available are 172524(8), 172530(8), and 172534(8). The alternate vector assignments available are jumper selectable within the range of 0-374. Any change in these assignments would necessitate a change in system software.

If an alternate address/vector combination is required, refer to Table 2-2 for the proper address jumper configuration and refer to Table 2-3 for the proper vector jumper configuration.

OPTION	JUMPERS	
	E11- E12	E9- E10
Standard Address * 172520	IN	IN
1st Alternate Address 172524	OUT	IN
2nd Alternate Address 172530	IN	OUT
3rd Alternate Address 172534	OUT	OUT
* Factory Preset		

Table 2-2 Base Address Configuration

	Vector Address Selection Bits / Jumpers							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	E21-E22	E23-E24	E25-E26	E27-E28	E29-E30	E31-E32		
224 *	OUT	IN	IN	OUT	IN	OUT	NA	NA
* Factory Preset OUT = 1								

Table 2-3 Vector Address Configuration

2.1.2. Device Interrupt Priority

The MSV05B supports the four-level device interrupt priority scheme compatible with the LSI-11/23. The controller asserts interrupt requests and monitors higher level request lines during interrupt arbitration. The level four request is always asserted by the controller, regardless of its priority, to maintain compatibility with the LSI-11 and LSI-11/2 processors.

The interrupt priority level is configured to level five at the factory. Refer to Table 2-4 for the proper jumpers to insert for the desired priority level.

OPTION	JUMPERS	
	E33- E34	E35- E36
Interrupt Priority Level 5 *	IN	OUT
Interrupt Priority Level 4	OUT	IN
* Factory preset		

Table 2-4 Interrupt Priority Level Configuration

2.1.3. Extended Features

Extended features mode of operation expands the functionality of the subsystem beyond that of the TS11/TS04. This mode includes 22-bit addressing along with additional functions and status. The controller is shipped with Extended Features enabled. This feature is enabled/disabled via jumper E15-E16. See Table 2-5.

Extended Features	JUMPER
	E 15 - E 16
Enabled *	IN
Disabled	OUT
* Factory preset	

Table 2-5 Extended Features Configuration

2.1.4. Drive Type

The MSV05B controller interfaces with one QIC-02 drive. The controllers are factory configured for standard QIC-02, QIC-24 9 track drives only. To select the desired Drive Type refer to Table 2-6 for the appropriate jumpers.

DRIVE TYPE / SIZE	JUMPERS		
	E13-E14	E19-E20	E17-E18
Cartridge 9 track *	IN	OUT	OUT
Cartridge 4 track	IN	OUT	IN
Cartridge 15 track (QIC-120)	IN	IN	OUT
Cartridge 12 track	IN	IN	IN
Reserved	OUT	OUT	OUT
Rosscomp 190 MB	OUT	OUT	IN
Reserved	OUT	IN	OUT
Cassette 20 MB	OUT	IN	IN
* Factory Preset			

Table 2-6 Drive Type / Size Configuration

Cartridge drives implementing the QIC-120 format provide increased data storage capacity while maintaining read compatibility with QIC-24 format tapes. These QIC-120 drives will write on 600 ft. tapes only; other length tapes are rejected by the drive.

2.1.5. Diagnostic Enable

The MSV05B controller incorporates a set of internal diagnostics to verify proper controller operation. With the diagnostic enable jumper removed the internal diagnostics only operate once during the power up cycle. Upon successful completion the green LED at the edge of the board is turned on. When the diagnostic enable jumper is installed, the controller continuously operates the self diagnostics turning off the LED at initiation and turning on the LED upon successful completion of each pass of the diagnostics. The effect is to blink the LED once for each successful pass of the diagnostic. If an error occurs the diagnostics will loop on the failing test until successfully completed.

Self tests include:

a) Proper Micro-processor operation
b) Condition code testing
c) Register tests
d) ALU operation test
e) RAM verification
f) Instruction tests

The controller is shipped with this feature disabled. It is only necessary to enable the diagnostics to determine if the controller is not functioning properly. When the self diagnostics are enabled all other controller operations are suspended. To enable this option, refer to Table 2-7.

DIAGNOSTICS	JUMPERS
	E7 - E8
DISABLED *	OUT
ENABLED	IN
*Factory Preset	

Table 2-7 Diagnostic Enable

2.1.6. Automatic Retension Enable

When a tape cartridge is inserted into the drive, the default operation of the MSV05B is to rewind to BOT and attempt to read the first block. If valid tape length information is found the drive is rewound and marked online. If an error occurs during this first read or a length of zero is found the tape is sized by timing a retension pass. This information is temporarily held by the controller until the first write to tape, at which time it is saved as part of a header block. Subsequent use of the tape does not require sizing since the length information is stored on tape.

If it is desireable to retension tapes on a regular basis the Automatic Retension option may be enabled. In addition to the default operation, this will cause the MSV05B to do a retension pass each time a tape is inserted into the drive.

AUTOMATIC TAPE RETENSION	JUMPERS E5 - E6
DISABLED *	OUT
ENABLED	IN
*Factory Preset	

Table 2-8 Automatic Retension Enable

2.2. DRIVE CONFIGURATION

The controller provides an industry standard QIC-02 interface compatible with most available drives. However, for proper operation, each drive must be configured with attention to several options. The drive must be strapped to respond to drive select "0", cartridge drives must be operating at 90 ips., QIC-24 format is recommended. If QIC-11 operation is required it will be necessary to bulk erase the tapes prior to the first write operation. This erasure is to insure the proper detection of NDT(no data detected) when appending.

2.3. CABLING

A 50-conductor ribbon cable connects the controller to any QIC-02 interface compatible drive. Connect the socket connector to the appropriate header located at the edge of the controller board. Observe the alignment of pin 1 of the socket connector and header as indicated by

the arrows shown in Figure 2-1. The edge connector should be connected to the drive, again observing the location of pin 1.

If the optional cable is purchased from an independent source, the following list of materials (or equivalent) will help in the construction of the required cable.

QTY	DESCRIPTION	MFG	NUMBER
1 each	50 pin socket connector	3M	3425-3000
1 each	50 pin edge connector	3M	3415-0001
A/R	50 conductor ribbon cable	3M	3365-50

Figure 2-2 illustrates the pin out of connector J-1. The signals named in the figure are described in greater detail in section 4.2.2, Tape Drive Interface.

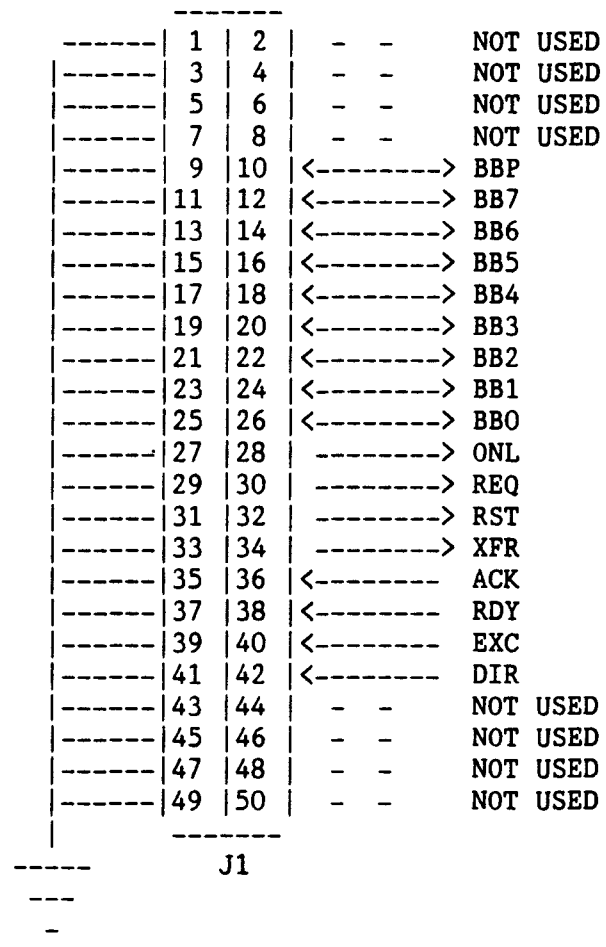


Figure 2-2 Connector Pin Definitions

2.4. INITIAL INSTALLATION AND CHECKOUT

Before the following procedures are followed and for purposes of checkout, verify that the controller and drive have been configured correctly as described in Sections 2.1 - 2.3.

1. Insert the MSV05B controller into the first available Q-22 slot, ensuring the component side is facing the same direction as the other cards.

2. Verify that bus grant continuity has been maintained. Failure to maintain bus grant continuity will cause the system to hang.

3. Connect tape drive cable to MSV05B controller card, aligning pin 1(red) on the cable with connector arrow.

4. Place the Run/Halt switch on the processor to the Halt position and turn on the processor.

5. Verify that the green LED on the MSV05B card edge is illuminated. This indicates the successful completion of the power-up micro-diagnostics by the controller.

   If, after initial application of power, the drive does not calibrate or the LED does not illuminate, check the cabling and power supplies. Most QIC-02 drives have separate power connectors for the formatter and tape drive. Verify proper power application.

6. If the standard address assignment is selected, open the MSDB register by entering 172520(8) thru console ODT. The processor will display the contents of the MSDB register which at this point is typically 377(8).

7. Open the MSSR register (location 172522(8)) using the console ODT as described above. The contents of this location should be 002200(8). For a detailed description of the register protocol and bit definition, refer to Section 3.

8. Micro Technology's MSV05B diagnostic (VMSDG) should be used to verify the complete operation of the subsystem. Refer to MTI diagnostic manual, P/N 830002-130, for instructions regarding the operation of the VMSDG diagnostic.

9. If the above procedures function as described, the controller is ready for use; otherwise consult the factory or your local representative for assistance.

Section 3

Functional Description

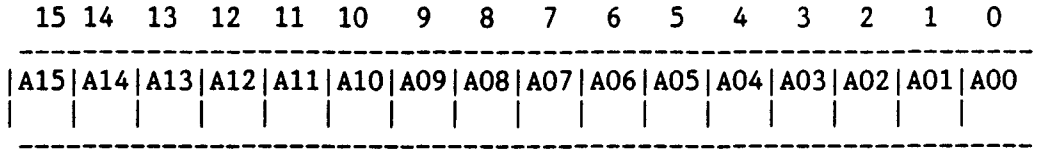
3. OVERVIEW

This section of the document presents the bit definitions for the MSV05B registers, register (packet) protocol and the command summary. The intent of this section is to provide the programming aspects of the MSV05B controller. In general the MSV05B is identical to DEC's TSV05 which is similar to DEC's TS11/TS04. Where differences exist they are noted in the text.

3.1. REGISTER DEFINITION

3.1.1. MSV05B Bus Address Register (MSBA)

The Bus Address Register (MSBA) is a read-only register located at the first I/O register address. In normal operating mode, it displays the low-order 16 bits of the memory address to be used or being used by the controller to access system main memory (e.g., for command buffer fetch, message buffer store, or data transfer).



MSBA Register Format

Bit	Description
15-00	A<15:00>--Address bits 15 through 00 - These bits normally reflect the low-order 16 bits of the 22-bit address used by the controller to access LSI-11 bus memory. These bits are loaded as follows: 1. Writing a word into MSDB, to define the address of the Command Buffer for the next operation. MSDB<15:02> are copied into MSBA<15:02>, and MSBA<01:00> are set to 0.

2. During DMA operation the controller updates the MSBA specifying the DMA address.

NOTE

The MSBA is NOT modified by initialize.

3.1.2. MSV05B Data Buffer Register (MSDB)

The MSDB appears as a 16-bit write-only register on the LSI-11 bus. Actually it is a 22-bit register which can be updated by four different types of transfers. Three of these transfers are for maintenance purposes, which is not supported. The fourth is a normal word output transfer (DATO) to specify a command pointer.

The 4-bit extension to MSDB is written at the high byte of the MSSR location. These address bits are ignored if the Extended Features jumper is removed. The extension is cleared after it is used once and so must be reloaded if extended addressing is to be used on subsequent command pointers. (Must be loaded before the MSDB is loaded.) It is also cleared by Initialize.

The controller will respond whenever the MSDB location is written to, but will be loaded only when the SSR bit in the MSSR register is set (if SSR is clear, the RMR bit in the MSSR will be set). Writing into MSDB clears SSR.

NOTE

Maintenance mode is not supported at this time. Attempts to enter Maintenance Mode will result in an RMR error with SC set.

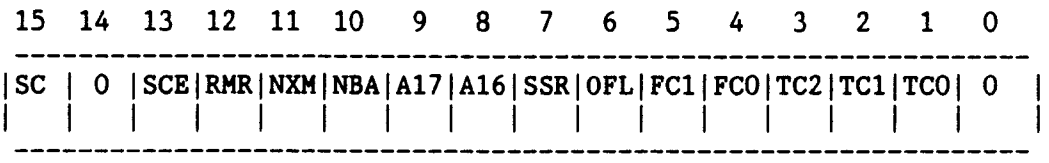
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P17	P16
M15	M14	M13	M12	M11	M10	M09	M08	M07	M06	M05	M04	M03	M02	M01	M00

MSDB Register Format

Bit	Definition
15-02 01-00	P<15:02> P<17:16> -- Command pointer. When the MSDB is written as a word and SSR is asserted, the data are loaded into bits 17-02 of the MSBA. MSBA bits 01-00 are cleared to 0. In addition, the extended address register MSDBX is loaded into MSBA bits 21-18. Note the MSDBX must be loaded before writing the MSDB with the command pointer.

3.1.3. MSV05B Status Register (MSSR)

The MSSR is a 16-bit register whose contents can only be updated by the controller; it cannot be directly modified from the LSI-11 Bus. The register is defined as Read/Write. It can be read to examine status, while writing into it causes a hardware initialize of the controller. A byte transfer (DATOB) to the high byte of the MSSR loads the extended data buffer register (MSDBX).



MSSR Register Format

Bit	Definition
15	SC -- Special condition--when set indicates that the last command was not completed correctly: either an error was detected or an exception condition (e.g., tape mark, BOT, etc.) was encountered. Also set with error bits RMR and NXM. Indicates that the termination class bits are valid (unless RMR is the only error). Cleared by initialize (can be set by a self test error).
14	Not defined. Always set to zero.
13	SCE--Sanity check error--set when the controller detects an internal RAM failure. A message buffer is not sent out.
12	RMR--Register Modification Refused--set when the MSDB is written from the LSI-11 bus and subsystem ready (SSR) is not asserted. Causes special condition (SC) bit to be set but no termination class code.
11	NXM--Nonexistent Memory--set when attempting a DMA transfer to or from a memory location which doesn't exist (does not respond within 20 us).
10	NBA--Need Buffer Address -- When set, indicates that the MSV05B needs a Message Buffer address. Cleared during the Write Characteristics command (if a valid address was given). If NBA=1 and any command other than Write Characteristics is given, the operation is terminated with Function Reject.

09-08 A<17:16> -- Address bits 17-16 -- A17 and A16 display bits 17 and 16 of the internal Bus Address Register (MSBA) which holds the command pointer or DMA address.

07 SSR -- Sub-system Ready -- When set indicates that the MSV05B controller is not busy and is ready to accept a new command pointer. Cleared by writing the MSDB. Also cleared by initialize and set by the controller upon successful completion of the internal micro diagnostics.

06 OFL -- Off-Line--When set, indicates that the tape transport is off-line and unavailable for any tape motion commands. This bit can cause a Termination Class of 1 or 3 (results in Non-Executable Function, NEF, status). This bit does not indicate the current status of the Tape Transport (updated on command completions).

05-04 FC<1:0> -- Fatal Termination Class Code -- Used to indicate the type of fatal error which has occurred. This code is only valid when the SC bit is set and the termination class code is 7 (all bits set). These bits are otherwise clear. The FC codes are defined:

Code	Meaning
0	Internal diagnostic failure. See error code byte (high byte of MXST3). Initialize must be issued for the controller to accept further commands.
1-3	Reserved-(not used)

03-01 TC<2:0> -- Termination class code -- This 3-bit field acts as a word offset value whenever an error or exception condition occurs on a command. Each of the 8 possible values of this field represents a particular class of errors or exceptions. The conditions in each class have similar significance and recovery procedures (as applicable). The codes are:

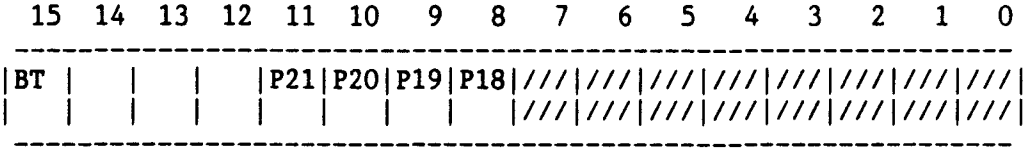
Code	Meaning
0	Normal Termination
1	Attention Condition
2	Tape Status Alert
3	Function Reject
4	Recoverable Error - tape position is one record down tape from start of function
5	Recoverable Error - tape not moved
6	Unrecoverable Error - tape position lost
7	Fatal Controller Error - (See Fatal Class Codes)

00 Not used. Always set to zero.

3.1.4. MSV05B Extended Data Buffer Register (MSDBX)

The Extended Data Buffer Register (MSDBX) is a write-only byte register. This address corresponds to the high-order byte of the MSSR register. The MSDBX is used to specify the most-significant four bits of the 22-bit address of the command sequence to be performed. MSDBX can only be written by a byte-access (DATOB) cycle addressed to the high byte of MSSR. If the Extended Features switch is Off when MSDBX is written, only the Boot bit is examined; the other bits are ignored.

Once written, the contents of the least-significant four bits of MSDBX are transferred to bits 18 through 21 of the internal MSBA (Bus Address) register for use as a command pointer. Subsequently writing the MSDB with the low order 18 bits of the command pointer starts operation and then clears MSDBX. Therefore, a subsequent load of only the MSDB will specify a 22-bit address with the upper four bits equal to zero. For the MSDBX register to be properly written, the SSR (Subsystem Ready) bit in MSSR must be set; if it is not, modification to MSDBX will not occur. When the MSDBX is written, the SSR bit is not cleared. Therefore, RMR should be checked for before MSDB is written. Writing the MSDB will begin processing on MSDBX. If the Boot bit is not set the command pointed to by the 22-bit MSDB will be retrieved, and command processing will begin. If the Boot bit is set, SSR will remain clear until the boot sequence is complete or until an error occurs.

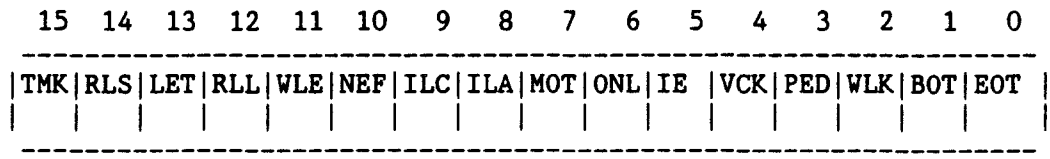


MSDBX Register Format

Bit	Definition
15	BT - Boot Command - When written to a 1 with SSR asserted causes a rewind to BOT, the first record to be skipped and the first 512 bytes of the second record to be read and transferred to host memory starting at location 0.
14-12	Reserved
11-08	P<21:18> Command pointer bits 21-18. When the MSDBX is written, if the SSR bit is asserted and the extended features jumper is enabled, the data are loaded into bits 21-18 of the MSBA register. The MSDBX is cleared after MSDB is written and is also cleared by Initialize. If Extended Features is off, bits 21-18 will be ignored.

3.1.5. Extended Status Register 0 (MXST0)

Extended Status Register 0 (MXST0) is available in the fourth word of the Message Buffer which is updated by the MSV05B upon completion of a command.



MXST0 Register Format

Bit	Description
15	TMK -- Tape Mark Detected. Set whenever a tape mark is detected during a read, space or skip command. Also set as a result of the write tape mark command.
14	RLS -- Record Length Short -- This bit is set if the record length was shorter than indicated by the byte count on a read operation. Also set if during a space record operation either a tape mark or BOT was encountered before the position count was exhausted or a skip tape marks command was terminated by encountering BOT or a double tape mark (if this operational mode is enabled) prior to exhausting the position counter.
13	LET -- Logical End of Tape -- If enabled through the use of the write characteristics command, this bit is set when either two contiguous tape marks are detected or when moving off of BOT and the first record encountered is a tape mark.
12	RLL -- Record Length Long -- Set when the record read on a read was longer than the byte count specified.
11	WLE -- Write Lock Error -- Set when a write operation is attempted on a write protected tape.
10	NEF -- Non-Executable Function -- Set when a command could not be executed due to one of the following conditions: --The command specified reverse tape direction but the tape was already at BOT. --The issuing of any motion command when the Volume Check bit is set or ONL is clear. --Any command, except get status or drive initialize, when the transport is offline.

--Any write command when the tape is not write enabled (also causes Write Lock Status - WLS).

09 ILC -- Illegal Command -- Set whenever a command is issued with either the command field or command mode field containing codes not supported by the MSV05B.

08 ILA -- Illegal Address -- Set when a command specifies an address more than 18 bits (when the Extended Features switch is off) or more than 22 bits (when the Extended Features switch is on), or an odd address when an even one is required.

07 MOT -- Motion -- Tape is moving. Indicates that the transport is asserting Formatter Busy or Rewinding status.

06 ONL -- On Line -- When set, indicates that the transport is on-line and operable. A change in this bit can cause a Termination Class of 1. If ONL is clear and a motion command is issued, causes NEF (Termination Class 3).

05 IE -- Interrupt Enable -- Reflects the state of the Interrupt Enable bit supplied on the last command.

04 VCK -- Volume Check -- When set, indicates that the transport has been either powered down or off-line. Cleared by the Clear Volume Check (CVC) bit in the Command Header word. This bit can cause a Termination Class of 3.

03 PED -- Phase-Encoded Drive -- Always set.

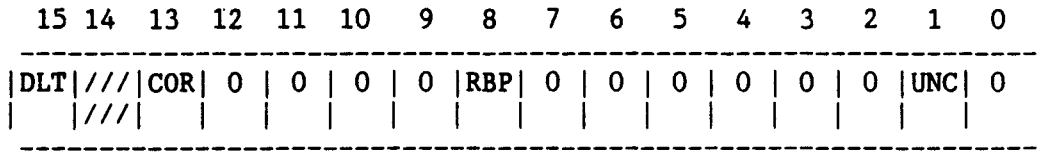
02 WLK -- Write Locked -- When set, indicates that the mounted cartridge has its file protect tab toward safe. The tape is, therefore, write protected.

01 BOT-- Beginning of Tape -- When set, indicates that the tape is positioned at the load point as denoted by the BOT hole on the tape.

00 EOT -- End of Tape -- This bit is set whenever the tape is positioned beyond either a calculated logical end of tape or the end of tape hole, whichever is sooner. Since the controller is operating in buffered mode, when the calculated logical end of tape is encountered before the physical end of tape hole, buffering will be terminated and when the buffer empties this bit will be set. When reading because of buffering the EOT will not be set until the program requests the last record previously recorded associated with the calculated logical EOT.

3.1.6. Extended Status Register 1 (MXST1)

Extended Status Register 1 (MXST1) is available as the fifth word of the Message Buffer which is updated by the MSV05B upon completion of a command or on an Attention (ATTN).

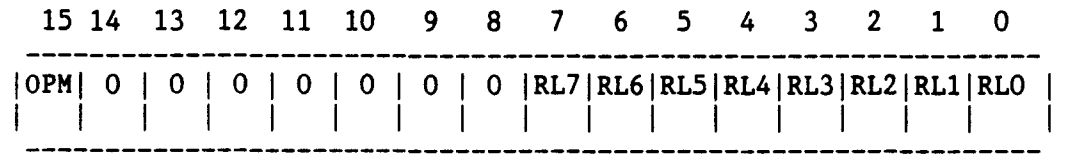


MXST1 Register Format

Bit	Description
15	DLT -- Data Late -- Set whenever the buffer becomes full on a read and the drive attempts to transfer another byte or when the buffer becomes empty on a write and the drive requests another transfer. These conditions are the result of latency on the LSI-11 Bus which exceed the data transfer rate of the MSV05B.
14	Not used.
13	COR -- Correctable Data -- Set to indicate a correctable data error occurred while reading or writing. Always set to zero. The streaming drives automatically handle errors during reading or writing. On a Write, the controller also sets a termination class code 4. On a read, the controller sets a termination class code 0.
12-9	Not used -- Always set to zero. In the TS11 these bits indicate various errors associated with the drive.
8	RBP -- Read Bus Parity Error -- The MSV05B does not implement bus parity on the drive interface. Thus this bit is always set to zero.
7-2	Not used -- Always set to zero. In the TS11 these bits indicate various errors associated with the drive.
1	UNC -- Uncorrectable or Hard Error -- Set to indicate that the drive encountered an uncorrectable error during the last command.
0	Not used -- Always set to zero. In the TS11 these bits indicate various errors associated with the drive.

3.1.7. Extended Status Register 2 (MXST2)

Extended Status Register 2 (MXST2) is available as the sixth word of the Message Buffer which is updated by the MSV05B upon completion of a command. Note that the lower byte of this register only has meaning for Write Characteristics and Get Status commands.



MXST2 Register Format

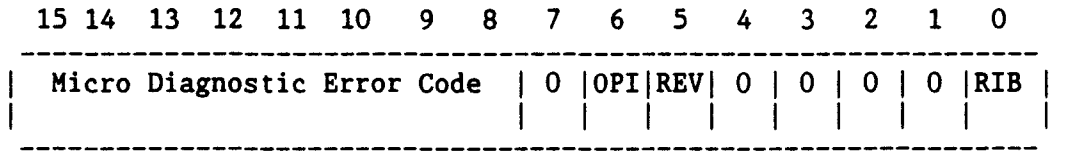
Bit	Description
15	OPM -- Operation in Progress -- Drive is busy
14-8	Not Used -- Always set to zero.
7-0	RL -- Revision Level -- In response to a Write Characteristics command this field displays the following:

7	Extended Features Jumper
6	Buffer Enable Jumper
5-0	Microcode Revision Level

On all other commands bits 2-0 show the unit number of the currently selected drive.

3.1.8. Extended Status Register 3 (MXST3)

Extended Status Register 3 (MXST3) is available as the seventh word of the Message Buffer which is updated by the MSV05B upon completion of a command.

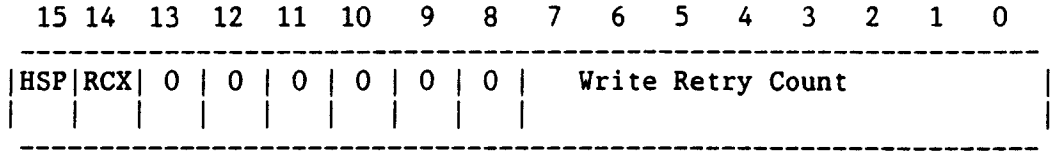


MXST3 Register Format

Bit	Description
15-8	MDE -- Micro Diagnostic Error Code -- This field is encoded by the controller to indicate a failure detected by the internal micro diagnostics.
07	Not used -- Always set to zero.
06	OPI -- Operation Incomplete -- Set whenever a read, space or skip command moves tape without detecting data for a fixed period of time.
05	REV -- Reverse -- Set when the current operation causes reverse tape motion.
04-01	Not used -- Always set to zero.
00	RIB -- Reverse Into BOT -- Indicates a reverse motion encountered a BOT. Tape motion is halted.

3.1.9. Extended Status Register 4 (MXST4)

Extended Status Register 4 (MXST4) is available as the eighth word of the Message Buffer which is updated by the MSV05B at the completion of a command. Note that for this word to be updated the extended features option must be enabled requiring the Message Buffer extent parameter to be increased by 2.



MXST4 Register Format

Bit	Definition
15	HSP -- High Speed -- This bit is set when buffered high speed mode is selected.
14	RCX--- Retry Count Exceeded -- Indicates when set that the controller could not successfully output the record within the specified number of retries. Since streaming drives deal with errors automatically this indicator will remain zero.
13-8	Reserved -- Always set to zero

7-0 WRC -- Write Retry Count -- Indicates that the controller initiated the displayed number of retries in order to write the previous buffered record. Since the streaming drives deal with errors automatically these bits will remain zero.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSBA (R/O)	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
MSDB (W/O)	P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P17	P16
MSSR (R/W)	SC	0	SCE	RMR	NXM	NBA	A17	A16	SSR	OFL	FC1	FC0	TC2	TC1	TC0	0
MSDBX (W/O)	BT	0	0	0	P21	P20	P19	P18	MSDBX P<21:18> only available when Extended Features are enabled							

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MXST0	TMK	RLS	LET	RLL	WLE	NEF	ILL	ILA	MOT	ONL	IE	VCK	PEO	WLK	BOT	EOT
MXST1	DLT	///	COR	0	0	0	0	RBP	0	0	0	0	0	0	UNC	0
MXST2	OPM	0	0	0	0	0	0	0	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
MXST3	Micro Diagnostic Error Code								0	OPI	REV	0	0	0	0	0
MXST4	HSP	RCX	0	0	0	0	0	0	Write Retry Count							

Figure 3-1 Register Summary

3.2. REGISTER/PACKET PROTOCOL

The CPU communicates with the controller using buffers in CPU memory. Commands are issued by storing control information in a Command Buffer and then passing the location of the Command Buffer to the controller using the MSDBX and MSDB registers. The controller then becomes "busy," fetches the control information and executes the command. When finished, the controller deposits status information into a Message Buffer in CPU memory, interrupts (if the IE bit is set) and then indicates it is ready to execute another command by setting SSR.

The CPU can then examine the MSSR hardware register and the Message Buffer to determine if the command was executed successfully.

All commands are handled in a similar way. The following paragraphs discuss buffer control, Message Buffer format and attention handling.

3.2.1. Buffer Ownership and Control

To prevent the controller from updating the Message Buffer while the CPU is reading it, or the CPU from updating the Command Buffer while the controller is reading it, the concept of "ownership" is defined. Each buffer may be owned by the controller or the CPU, but not by both. Ownership of a buffer can only be transferred by the current owner.

There are four different combinations of transferring the two buffers in the two directions:

1. Command Buffer from the CPU to the Controller.

   The CPU transfers ownership of the Command Buffer to the Controller by writing the address of the Command Buffer into the MSDB register. This clears the SSR bit in MSSR.

2. Command Buffer from the controller to the CPU

   The Controller transfers ownership of the Command Buffer back to the CPU by depositing a Message Packet (in the Message Buffer) that has the Acknowledge (ACK) bit set in the message header word. After the message is deposited by the controller, it sets the SSR bit in MSSR. The MSV05B always responds with the ACK bit set transferring ownership of the Message Buffer.

3. Message Buffer from the CPU to the Controller.

   The CPU transfers ownership of the Message Buffer to the controller by setting the ACK bit in the Command Buffer and then initiating the command by passing the Command Buffer to the controller using the MSDBX/MSDB registers. If the command buffer does not contain the ACK bit, the controller will know that the CPU did not see the last Message Buffer and the Controller still owns it. The Controller, in response to the CPU writing into MSDB, will set SSR and perform an interrupt (if the IE bit is set) without sending out a message, since it does not own the buffer.

4. Message Buffer from the Controller to the CPU.

   The Controller transfers ownership of the Message Buffer to the CPU by writing the Message Buffer and setting the SSR bit. This can happen at the end of a command.

In addition, an Initialize aborts any operation in progress and gives ownership of both the Command and Message Buffers to the CPU.

3.2.2. Message Packet Format

The format of the message packet which is stored in the Message Buffer is shown in Figure 3-2. The format is used for all messages, whether the message contains command execution status or the reason for an attention. The message consists of a Header word, a Data Field Length word, a Residual Byte/Record/Tape-Mark Count word and either four or five Extended Status Registers (five if Extended Features is enabled).

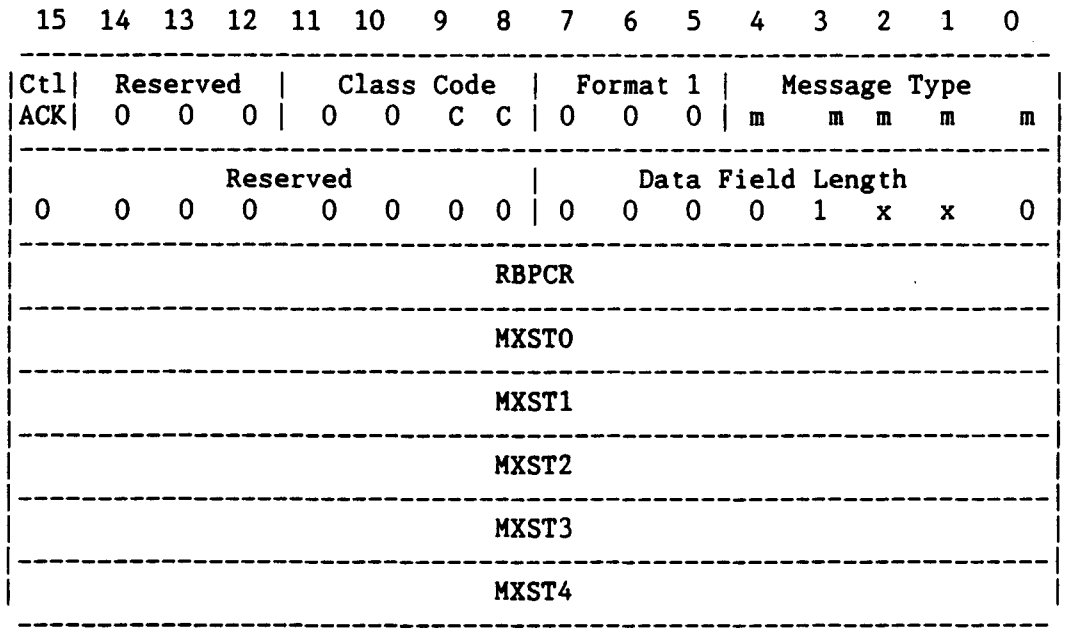
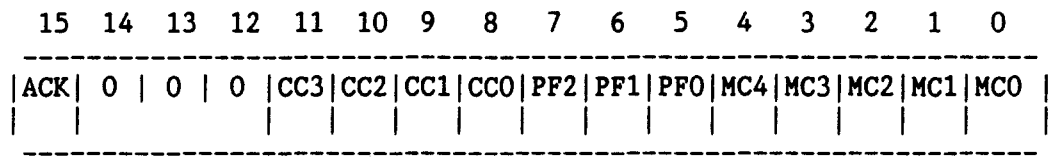


Figure 3-2 Message Packet

3.2.2.1. Header Word

The Header word is available in the first word of the message packet.



Header Word Format

Bit	Definition
15	ACK--Acknowledge--This bit is set by the MSV05B to inform the CPU that the Command Buffer is now available for any pending or subsequent command packets.
14-12	Reserved. Written as zeroes.
11-08	CC<03:00>--Class Code field--These bits define the class of failure when the Message Type Code field (Header word bits 04-00) is not indicating a normal End Message. Codes are:

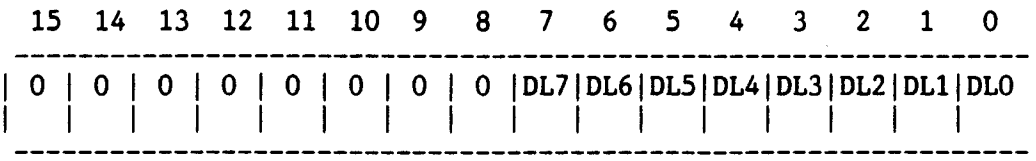
Message Type	Class Code	Definition
ATTN	0000	On or off line
ATTN	0001	Not used
FAIL	0000	Not used
FAIL	0001	Illegal Command (ILC), Illegal Address (ILA) or Need Buffer Address (NBA) on a tape motion command.

07-05	PF<02:00>--Packet Format field--Written as zeroes, which specifies a one word message header.
04-00	MC<04:00>--Message Type code--The Message Type Code is of the form 10xxx, which indicates that the message contains a Header word, a Data Length word and then xxx Data/Status words. This field is related to the Termination Class Code (MSSR bits 03-01) as follows:

Termination Class Code	Message Type (binary)	Definition
0,2	10000	End
3	10001	Fail
4,5,6,7	10010	Error
1,7	10011	Attention

3.2.2.2. Data Length Word

The Data Length word is available in the second word of the message packet.

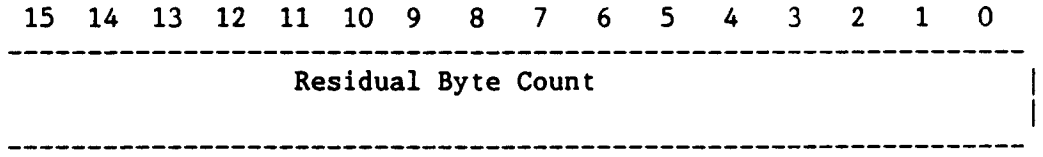


Data Length Word Format

Bit	Definition
15-08	Reserved. Written as zeroes
07-00	DL<07:00>--Data Field Length--This field specifies how many bytes of information follow in the message. If Extended Features is disabled, this field contains a 12 (octal) indicating that the rest of the message consists of the RBPCR and four Extended Registers. With Extended Features enabled, this field contains a 14 (octal) indicating that an additional Extended Status Register (MXST4) also follows.

3.2.2.3. Residual Byte/Record/File Count Register (RBPCR)

The Residual Byte/Record/File Count Register is a multi-purpose register that is available as the third word of the message packet.



Residual Byte/Record/File Count Register Word Format

Bit	Definition
15-00	RBPCR<15:00>--Residual Byte/Record/File Count Register--This word contains a non-zero value whenever the count specified in a command is larger than the number of operations performed.

Function	Value Definition
Read	Value indicates the number of bytes by which the tape record was shorter than the expected length.

Space Records or Skip Tape Marks	Value contains the difference between the number of records or tape marks actually skipped and the specified number.

3.2.2.4. Extended Status Register 0 (MXST0)

Extended Status Register 0 is available in the fourth word of the message packet.

3.2.2.5. Extended Status Register 1 (MXST1)

Extended Status Register 1 is available in the fifth word of the message packet.

3.2.2.6. Extended Status Register 2 (MXST2)

Extended Status Register 2 is available in the sixth word of the message packet.

3.2.2.7. Extended Status Register 3 (MXST3)

Extended Status Register 3 is available in the seventh word of the message packet.

3.2.2.8. Extended Status Register 4 (MXST4)

Extended Status Register 4 is available in the eighth word of the message packet. This register is only supplied when Extended Features is enabled.

3.3. GENERAL STATUS PROCESSING INFORMATION

3.3.1. Termination Class/Message Type Relationship

The relationship between the Termination Class code (TC2-TC0 of the MSSR Register) and the Message Type Code (MC4-MC0 of the Message Buffer Header word) is summarized below.

TC Code	Message Type Code (Octal)	Definition
0	END (20)	Normal termination. The operation was completed without incident.

1	ATTN (23)	Attention condition. This code indicates that the drive has undergone a status change, such as going Off-Line or coming On-Line.
2	END (20)	Tape status alert. A status condition has been encountered that may affect the program. Additional information may be provided by bits in the Extended Status Registers, such as TMK (Tape Mark), EOT (End of Tape) and RLL (Record Length Long).
3	FAIL (21)	Function reject. The specified function was not initiated. Additional information may be provided by MSSR bit OFL (Off Line) or Extended Status Register bits VCK (Volume Check), BOT (Beginning of Tape), WLE (Write Lock Error), ILC (Illegal Command) and ILA (Illegal Address).
4	ERROR (22)	Recoverable error. The tape position is one record beyond what its position was when the function was initiated.
5	ERROR (22)	Recoverable error. The tape position has not changed.
6	ERROR (22)	Unrecoverable error. The tape position has been lost.
7	ATTN(23) or ERROR(22)	Fatal subsystem error. The subsystem is incapable of performing properly. Refer to the Fatal Termination Class Code (FC1-FC0) in the MSSR for additional information.

3.3.2. Additional Information on Status Processing

The following points should be considered in reference to status and error processing.

1. The Special Condition (SC) and Register Modification Refused (RMR) bits of the MSSR are cleared by successfully loading a command pointer into the MSDB.

2. All commands, including the Get Status command, clear the internal controller copy of the error bits in the Extended Status registers, except for bits 15-8 of MXST3. Therefore, a Get Status command will not return the error bits generated by a previous tape operation.

3. A Read operation which encounters a Tape Mark will not transfer any data and will give a Tape Status Alert termination. The Tape Mark and Record Length Short status bits will be set, and the RBPCR word in the message buffer will contain the original byte count as specified in the command.

4. A Space Records operation will automatically terminate when a Tape Mark is traversed, and the TMK status bit will be set. Also, Record Length Short (RLS) will be set if the record count was not decremented to zero.

5. A Skip Tape Marks operation will automatically terminate when two consecutive Tape Marks are encountered and the "Enable Skip Stop" (ESS) mode is enabled via the Write Characteristics command. Record Length Short (RLS) will be set if the count was not decremented to zero. The same is also true if a Tape Mark is the first record off BOT and both the ESS and ENB bits were set in the previous Write Characteristics data word.

6. Any Write or Write Tape Mark command which is executed at or beyond the calculated EOT will result in a Tape Status Alert termination. The internal controller EOT status bit will remain set until the calculated EOT is passed in the reverse direction by Rewind, Space Records Reverse, etc.

7. A Read Reverse, Space Records Reverse, or Skip Tape Marks Reverse command which encounters BOT after the operation is underway will result in a Tape Status Alert termination (the RIB status bit will be set).

8. If a Read Reverse, Space Records Reverse, or Skip Tape Marks Reverse command is issued while the tape is already at BOT, a Function Reject (NEF - Non-Executable Function) status will be returned.

9. When a normal Rewind command is issued, the termination message and interrupt will not occur until the tape reaches BOT and has stopped.

10. When a Rewind with Immediate Interrupt command is issued the controller commands the transport to rewind, checks for proper status, and then issues an interrupt and END message for normal termination. If a new tape motion command is issued to a rewinding unit, the controller will wait until the tape has been rewound to BOT before proceding with the new command. During execution of a Rewind with Immediate Interrupt, the Motion (MOT) bit in MXST0 will be set if a Get Status command is performed.

11. The Rewind/Unload command will cause an interrupt and termination to occur immediately. The drive will go off-line, rewind, then remain off-line until the cartridge is removed and a cartridge is reinserted.

12. Since records are buffered for writes, the controller issues Normal termination messages and interrupts immediately after the data to be written have been stored in the controller's RAM and before the data are actually written onto tape. The possibility exists that the record cannot successfully be written onto tape with the first attempt, in which case a retry algorithm is executed to attempt to successfully write the data. If the data are eventually successfully written, the CPU will not know that any problem occurred unless the Extended Features option is enabled, in which case the Write Retry Count field in MXST4 can be examined in the message terminating the next command.

If retries are therefore to be logged, the software should examine the Write Retry Count field in each message packet.

13. If the controller cannot write a stored record successfully from RAM (retry count exhausted), the next Tape Motion command following the Write command associated with the failed record will be terminated with Termination Class 6 (Tape Position Lost) and the Retry Count Exceeded (RCX) bit in MXST4 will be set. In addition, the Uncorrectable Error (UNC) bit in MXST1 will be set. The tape will be positioned one record beyond the last successfully written record.

3.4. COMMAND PROTOCOL

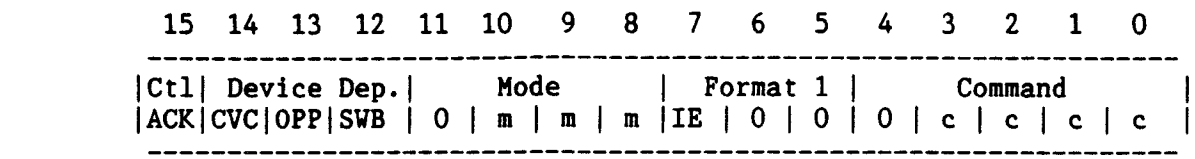
The command protocol used by the MSV05B is for the most part identical to DEC's TSV05 subsystem. With extended features disabled except for extended error status bits and limitations previously noted, read, write, position and get status commands function identically to the TSV05. With Extended Features enabled 22-bit addressing is enabled along with some command modes as with the TSV05. The following paragraphs describe the general command format followed by a detailed description of each command.

3.4.1. Command Packet Definitions

The CPU issues a command to the MSV05B controller by first building a Command Packet in CPU memory space (on a modulo-4 address boundary) then writing the address of the packet into the MSV05B MSDB register. The address written is termed the Command Pointer. Assuming that the MSV05B is ready to accept a command, writing of the Command Pointer initiates command processing, in which the controller fetches the Command Packet and executes the command encoded within the packet.

Logically, a Command Packet can be composed of one, two, three or four 16-bit words, depending upon the type of command and the amount of information it needs to proceed with execution. All Command Packets begin with a Command Packet Header Word. The format of this word is the same for all commands; the encoding of the various fields within the word distinguishes one command from another. Table 3-1 summarizes the Command Code and Command Mode field definitions.

All undefined bits in the Header Word as with other words within the command packet should be written as zero to avoid termination with a Function Reject (Termination Class 3).



Bit	Description
15	ACK--Acknowledge--this bit is set by the CPU when issuing a command (when the CPU owns the Message Buffer) to inform the MSV05B that the Message Buffer is available for use. This passes ownership of the Message Buffer to the MSV05B controller.
14	CVC--Clear Volume Check--When set causes the Volume Check condition, caused from the drive changing from off-line to on-line, to be cleared allowing tape operations to be executed on the drive.
13	OPP--Opposite--This bit is ignored.
12	SWB--Swap Byte--This bit is ignored and assumed zero thus forcing the standard DEC method of retrieving bytes from memory where the "first" byte in the word is the least significant byte (bits 7-0).
11-8	Command Mode Field--This field acts as an extension of the Command Code and allows additional specification of device commands.
7-5	Packet Format Field--Defines the header type and interrupt enable. The only two valid configurations are:

Field	Definition
000	Interrupts disabled
100	Interrupts enabled

4-0	Command Code--Defines the command category. Used together with the Command Mode field to specify the command.

Command Code	Command Name	Command Mode	Mode Name
00001	READ	0000	- Read Next (Forward)
		0001	- Read Previous (Space Reverse-Read Forward-Space Reverse)*
		0010	- Reread Previous (Space Reverse Read Forward)*
		0011	- Reread Next (Read Forward, Space Reverse)*
00100	WRITE CHARACTERISTICS	0000	-Load Message Buffer address and Set Device Characteristics
00101	WRITE	0000	- Write Data (Next)
		0010	- Write Data Retry (Illegal Function Reject)
00110	WRITE SUBSYSTEM MEMORY	0000	- Illegal Function Reject
01000	POSITION	0000	- Space Records Forward
		0001	- Space Records Reverse**
		0010	- Skip Tape Marks Forward
		0011	- Skip Tape Marks Reverse**
		0100	- Rewind
01001	FORMAT	0000	- Write Tape Mark
		0001	- Erase
		0010	- Write Tape Mark Retry (Illegal Function Reject)
01010	CONTROL	0000	- Message Buffer Release
		0001	- Rewind and Unload
		0010	- NO-OP (Retension Tape)
		0100	- Rewind with Immediate Interrupt
01011	INITIALIZE	0000	- Controller/Drive Initialize
01111	GET STATUS	0000	- Get Status (output Extended Status message)

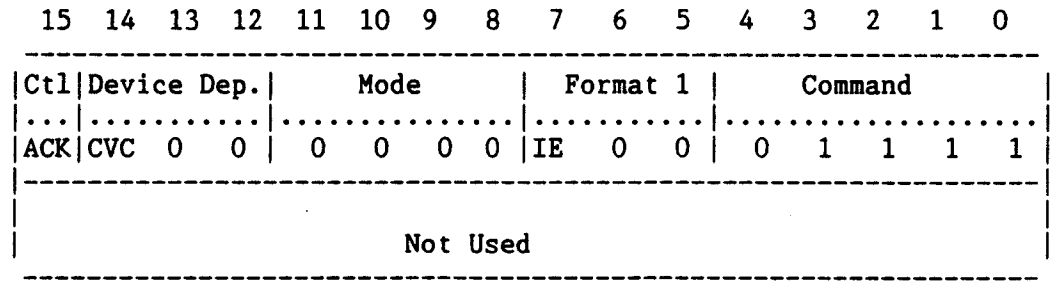
*These commands are currently rejected but are under consideration based on software requirements

**These commands are supported with limitations as to the number of tape marks skipped or records reversed.

Table 3-1 Command Code and Mode Field Definition

3.4.2. Get Status Command

The Get Status command causes a message packet to be deposited in the Message Buffer area in order to update the Extended Status registers. Normally the Extended Status registers are updated after each command except Message Buffer Release, so the Get Status command is only needed when the MSV05B has been idle for some time, when a status register update is desired without performing a tape motion command or when the unit number of the currently selected tape transport is desired (bits 2-0 of MXST2)



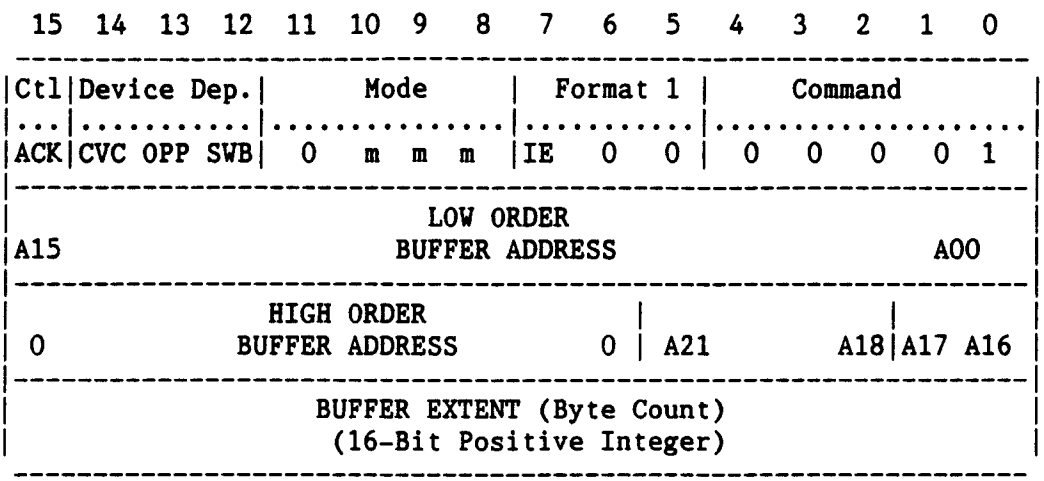
Get Status Command Packet

3.4.3. Read Command

The read command has four modes as shown below

Mode	Function
0000	Read Next (Forward)
0001	Read Previous (Space Reverse-Read Forward-Space Reverse)*
0010	Reread Previous (Space Reverse, Read Forward)*
0011	Reread Next (Read Forward, Space Reverse)*

*These commands are currently rejected but are under consideration based on software requirements.



Read Command Packet

The Read command requires a four word packet consisting of a header word, two words for the data buffer address in CPU memory and the Buffer Extent (byte count) word specifying the number of bytes expected in the tape record to be read. A byte count of 0 indicates that 65,536 bytes are expected. Figure 3-3 (pg. 59) illustrates the byte positioning used by the MSV05B when encountering an odd address and/or an odd byte count.

The third word of the packet specifies the high order address bits of the data buffer. This word will differ depending on the status of the Extended Features option:

a. Extended Features disabled--If any of bits 15-02 are non-zero, the function will not be executed but will instead terminate with a Function Reject with Illegal Address (ILA) error. Otherwise, bits 01-00 specify A17-A16 and together with the 16 bits in the second word of the packet define an 18 bit address.

b. Extended Features enabled--If any of bits 15-06 are non-zero, the function will not be executed but will instead terminate with a Function Reject with Illegal Address (ILA) error. Otherwise, bits 05-00 specify A21-A16 and together with the 16 bits in the second word of the packet define a 22 bit address.

The Read operation is assumed to be for a record of known length. Therefore, the correct record byte count (fourth word of the packet) must be known. If the byte count exactly equals the record length, normal termination occurs. If the record is shorter than the specified byte count, the Record Length Short (RLS) error bit will be set in MXST0 and a Tape Status Alert termination occurs. If the record on tape is larger than the byte count, the Record Length Long (RLL) error bit will be set in MXST0 and Tape Status Alert termination given; in this case, only the number of bytes specified in the byte count will be transferred to the data buffer. Also, any Read operation that encounters a Tape Mark will not transfer any data. In this case,

the Tape Mark (TMK) and Record Length Short (RLS) bits will be set and a Tape Status Alert termination given.

Reverse Read operations which pass BOT cause the Reverse Into BOT (RIB) bit in MXST3 to be set and Tape Status Alert termination given. If the tape is already at BOT when a Reverse Read is issued, there will be no tape motion and Function Reject termination will occur with the Non-Executable Function (NEF) error bit set in MXST0.

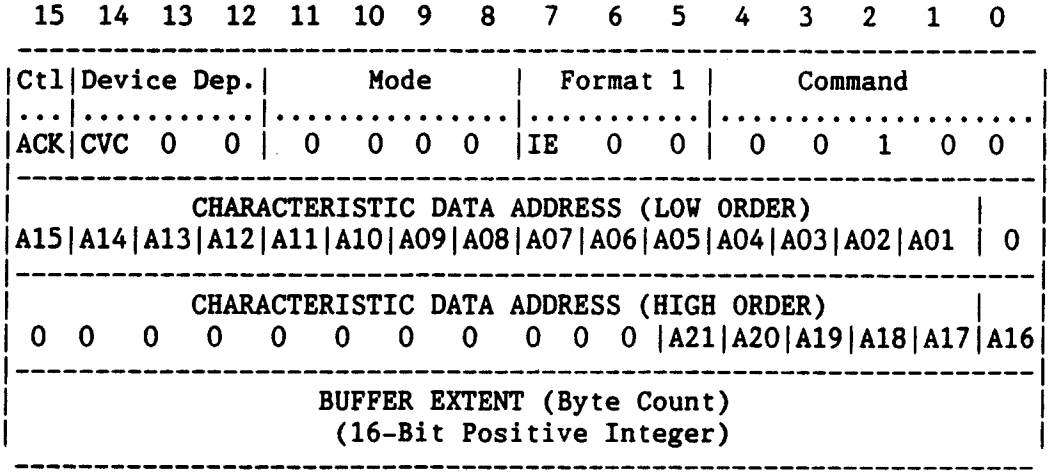
Note: The OPP and SWB bits of the Header word are ignored.

3.4.4. Write Characteristics Command

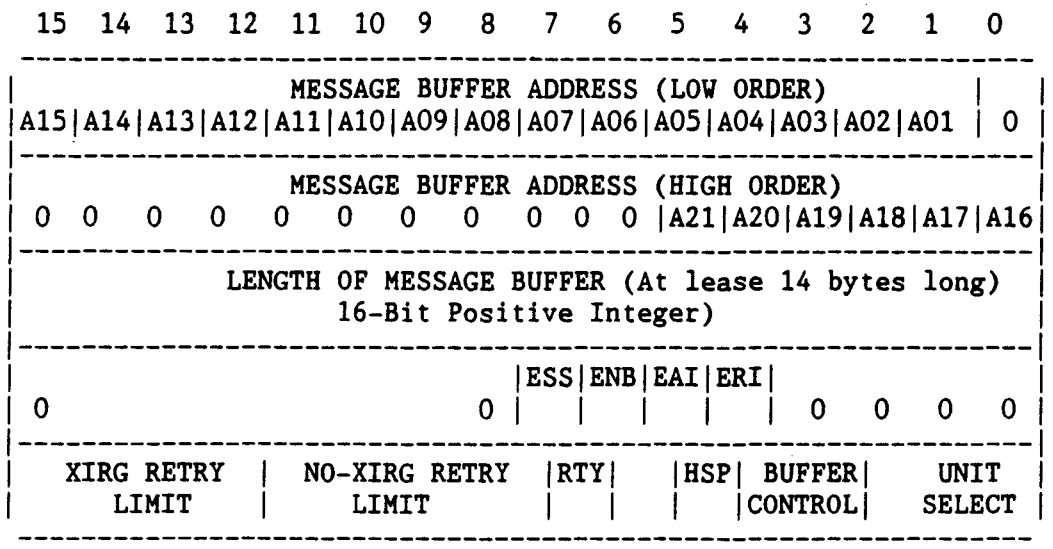
The Write Characteristics command describes the location and size of the Message Buffer to the MSV05B and must be the first command issued to the MSV05B after an initialization (all other commands will be rejected). It also specifies the action that the MSV05B is to take when certain conditions are encountered. The Message Buffer must be at least seven contiguous words long (eight when Extended Features is enabled) and reside on a word boundary.

The second and third word of the command packet specify the location of the associated characteristics data buffer. This data buffer must have an even address in CPU memory space. If bit 0 of the second command packet word (low order Characteristic Data address) or bits 15-02 (Extended Features disabled) or bits 15-06 (Extended Features enabled) of the third command packet word (high order characteristics data address) are not zero, the Write Characteristics command is not executed but is terminated with a Function Reject. Otherwise, the second and third words specify an 18 or 22-bit characteristic data buffer address.

The fourth command packet work specifies the length in bytes of the characteristic data buffer. This length must be at least 6 and can be 10 when Extended Features is enabled.



Command Packet

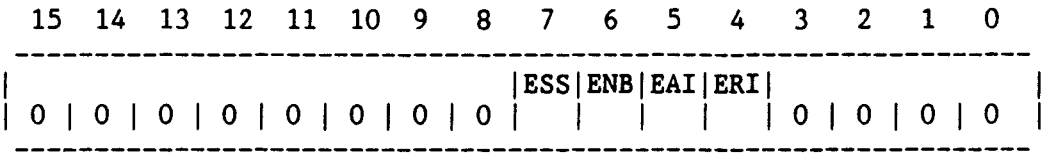


Characteristics Data
Write Characteristics Command Format

The first two Characteristics Data words specify the address of the Message Buffer. 18-bit address may be specified if Extended Features is disabled; 22-bit addresses may be specified if Extended Features is enabled.

The third Characteristics Data word specifies the Message Buffer length in bytes. This value must be at least 16 (octal) and can be 20 (octal) if Extended Features is enabled so that MXST4 can be output by the controller.

The fourth Characteristics Data word is the Characteristics Mode word and causes specific actions in response to certain conditions.



Characteristic Mode Word Format

Bit	Definition
15-08	Not defined. Set to zeroes.
07	ESS--Enable Skip Tape Marks Stop--When set, this bit instructs the controller to stop and set the Logical End of Tape (LET) status bit during a Skip Tape Mark command when a double tape mark (two contiguous tape marks) have been detected. Setting this bit also enables operation of the ENB bit. In the default setting of 0, the Skip Tape marks command will terminate only on tape mark count exhausted, if it runs into BOT, or if it runs into the EOT.

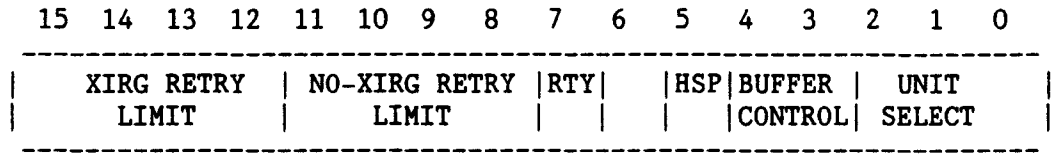
06 ENB--Enable Tape Mark Stop Off BOT--This bit is meaningful only if the ESS bit is set. When this bit is set (and ESS=1), the tape is at BOT, a Skip Tape Marks Forward command is issued, and the first record seen is a tape mark, then the controller will stop the operation and set the Logical End of Tape (LET) status bit in MXST0. If this bit is clear under these conditions, the controller will merely count the tape mark and continue.

05 EAI--Enable Attention Interrupts--Not used by the MSV05B. Should be set to zero.

04 ERI--Enable Message Buffer Release Interrupts--If this bit is 0, interrupts will not be generated upon completion of a Message Buffer Release command. Upon recognition of the command, only Subsystem Ready (SSR) will be reasserted. If ERI is 1, an interrupt will be generated (without an accompanying message packet).

03-00 Not defined. Set to zeroes.

The fifth Characteristic Data word is the Extended Characteristics word and is used to specify parameters for the buffered mode of operation. It is also used to select a unit in a multi-drive system. This word can only be specified when Extended Features is enabled.



Extended Characteristics Word Format

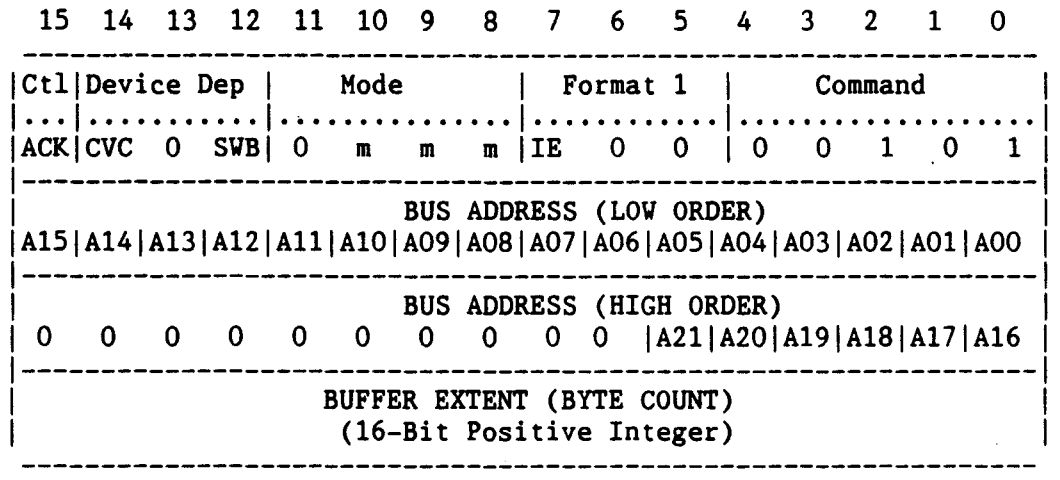
Bit	Definition
15-12	Extended Interrecord Gap (XIRG) Retry Limit--not used by the MSV05B. Should be set to zero.
11-08	Non-Extended Interrecord Gap (NXIRG) Retry Limit--not used by the MSV05B. Should be set to zero.
07	Retry Algorithm Control--Not used by the MSV05B. Should be set to zero.
06	Not defined. Should be set to zero.
05	High Speed Select--When 0 selects low transport speed; when 1 selects high transport speed.
04-03	Buffering Mode Control--always buffered, these bits are ignored.

02-00 Unit Select--Selects the transport number for subsequent tape operations. Initialize sets the unit selection to zero. Only one transport per controller supported at this time.

3.4.5. Write Command

The MSV05B controller only supports the Write Data command. The acceptable modes and corresponding functions are:

Mode	Function
0000	Write Data
0010	Write Data Retry-(Illegal Function Reject)



Write Command Packet

The command packet for a Write contains four words: a Header word, two words specifying the address of the data buffer in CPU memory space where the data to be written onto tape is stored, and a Buffer Extent (Byte Count) word specifying the number of bytes available in the data buffer and the number of bytes to be written onto tape. A byte count of 0 specifies that 65,536 (64K) bytes are to be written. Figure 3-3 illustrates the byte positioning used by the MSV05B when encountering an odd address and/or an odd byte count.

The second word in the packet specifies the low order bits (A<15:0>) of the starting address of the data buffer. The third word in the packet specifies the high order bits of the starting address. Bits 5-0 of the word represent bits A<21:16>. When the Extended Features option is disabled only the two low order bits (A17 and A16) of the high order address word may be non-zero. In this case, these bits together with the 16 bits specified by the low-order starting address word form an 18-bit starting address of the data buffer. If any other bits (15-2) of the high order address word are nonzero the function will not be performed but will terminate with a Function Reject with Illegal

Address (ILA) error status. When Extended Features mode is enabled, the low-order 6 bits of the third word are used to specify bits A21-A16 of a 22-bit starting address. In this mode, if any other bits (15-6) in the third word are nonzero, the command is aborted with a Function Reject termination with Illegal Address (ILA) error status.

The Swap Bytes (SWB) bit in the command header word is ignored. The controller does not support byte swapping and only writes the standard DEC format starting with the low order byte of the word.

If a Write command is executed at or beyond either the calculated logical end of tape or physical end of tape marker the data will be written but a Tape Status Alert (TSA) termination will occur. EOT will remain set until passed in the reverse direction.

The MSV05B does not support bus parity communicating with drive interface. However the streaming drives incorporate a sophisticated write verify mechanism to insure that the information written to the tape is valid.

Buffer Address = 1000
Byte Count = 10(8)
Block Size = 10(8) bytes

1000	1	0
1002	3	2
1004	5	4
1006	7	6

Buffer Address = 1001
Byte Count = 10(8)
Block Size = 10(8) bytes

1000	0	
1002	2	1
1004	4	3
1006	6	5
1010		7

Buffer Address = 1000
Byte Count = 7
Block Size = 7 bytes

1000	1	0
1002	3	2
1004	5	4
1006		6

Buffer Address = 1001
Byte Count = 7
Block Size = 7 bytes

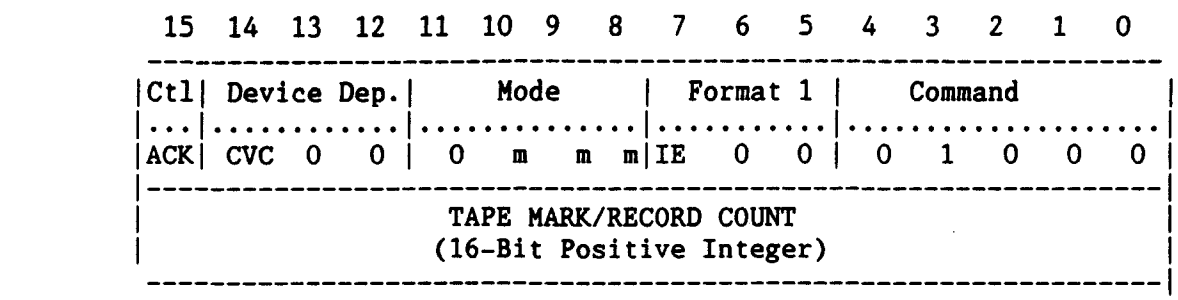
1000	0	
1002	2	1
1004	4	3
1006	6	5

Figure 3-3
Memory/Tape Data Byte Positioning

3.4.6. Position Command

This command causes the tape to space records either forward or reverse, skip tape marks either forward or reverse, or to rewind to BOT. The acceptable modes and corresponding functions are:

Mode	Function
0000	Space Records Forward
0001	Space Records Reverse
0010	Skip Tape Marks Forward
0011	Skip Tape Marks Reverse
0100	Rewind (Record Count Ignored)



The command packet consists of two words: A header word and a tape mark/record count word. The second word is ignored for a Rewind command.

The Space Records operation skips over the number of records specified in the Record Count word of the command packet. However, the operation automatically terminates, with a Tape Status Alert termination code, when a tape mark is traversed. (The tape mark is included in the record count.) Also, the Record Length Short (RLS) status bit in MXSTO will be set if the record count is not decremented to zero.

A Skip Tape Marks command skips over the number of tape marks specified in the second word (Tape Mark/Record Count) of the command packet. However, for Skip Tape Marks Forward, if Enable Skip Stop (ESS) bit was set on the last Write Characteristics command, the operation will automatically terminate if a double tape mark (two contiguous marks without intervening data) is encountered. Automatic termination will occur if a tape mark is the first record off of BOT and both Enable Skip Stop (ESS) and Enable Tape Mark Stop off BOT (ENB) were both set on the last Write Characteristics command. A Record Length Short (RLS) status bit is set if the tape mark count is not decremented to zero.

If a BOT is encountered during either a Space Records Reverse or Skip Tape Marks Reverse the Reverse Into BOT (RIB) status bit is set and causes a Tape Status Alert Termination. If either of these reverse commands is issued while the tape is already positioned at BOT, the Nonexecutable Function (NEF) error bit will be set and Function Reject termination given; in this case, the tape will not move.

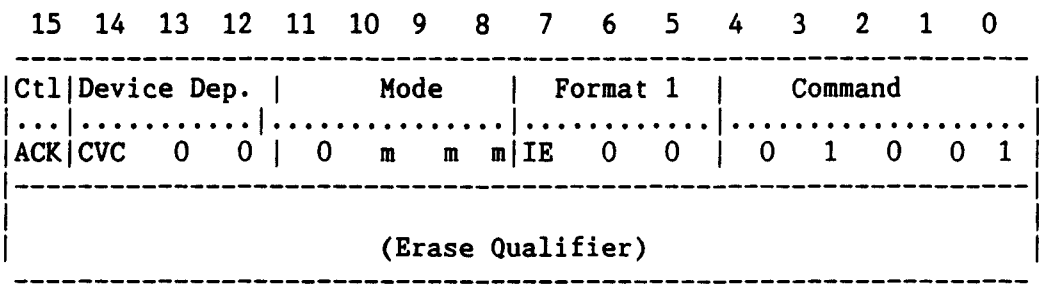
When a Rewind command is issued, the interrupt (if enabled) will not occur until the tape reaches BOT and has stopped.

Positioning functions such as Space Records Reverse and Skip Tape Marks Reverse are implemented to the extent that they will allow proper operation of DEC operating systems and utilities. These commands are supported with limitations as to the number of tape marks skipped or records spaced.

3.4.7. Format Command

This command can cause a tape mark to be written on the tape or total erasure of the tape. The acceptable modes and corresponding functions are:

Mode	Function
0000	Write Tape Mark
0001	Erase
0010	Write Tape Mark Retry (Illegal Function Reject)



Format Command Packet

The command packet consists of two words: A header word and a second word which is ignored for a Write Tape Mark operation.

The Write Tape Mark command causes a unique record to be written on the tape. If this command is executed beyond either the calculated Logical End of Tape or the physical EOT mark, a Tape Status Alert Termination will occur. The EOT bit will remain set until the EOT marker is passed in the reverse direction.

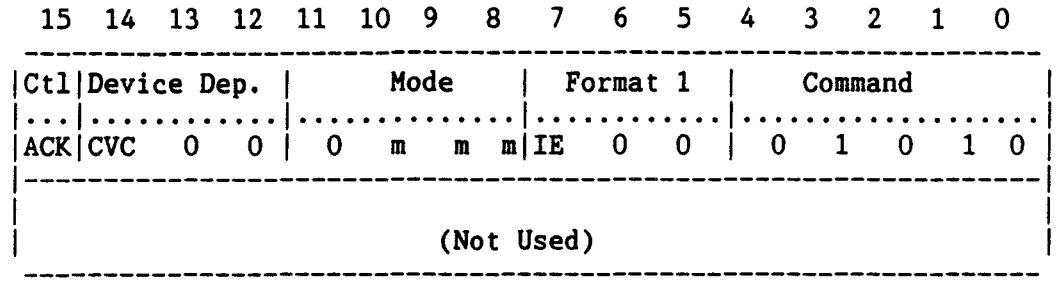
The Erase command will totally erase the tape and then write length information at the beginning. To prevent accidental erasure, this command must have a second packet word of 1234(base 8).

Write Tape Mark Retry commands will terminate with a Function Reject Termination and the Illegal Command (ILC) error bit will be set.

3.4.8. Control Command

The command provides four modes of control. These are: Message Buffer Release, Rewind and Unload, NO-OP, and Rewind with Immediate Interrupt. The acceptable modes and their corresponding functions are:

Mode	Function
0000	Message Buffer Release
0001	Rewind and Unload
0010	NO-OP (Retension)
0100	Rewind with Immediate Interrupt.



Control Command Packet

The command packet consists of two words: The Header word and a second word which is read but ignored.

The Message Buffer Release command, when executed with the ACK bit set, passes ownership of the Message Buffer to the controller. Since the MSV05B doesn't implement Attention this command is ignored.

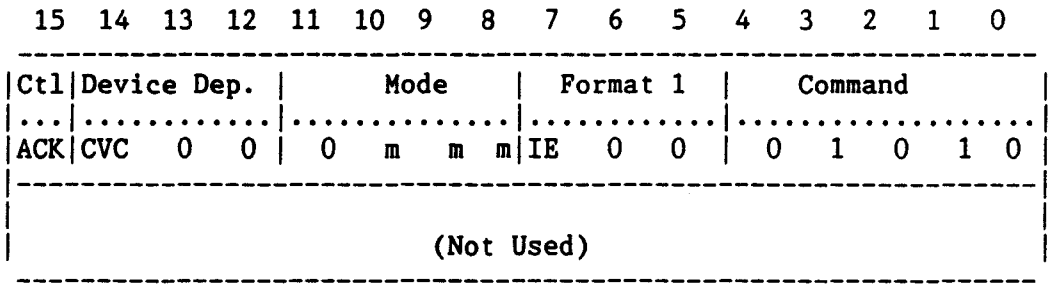
The Rewind and Unload command rewinds the tape to the BOT marker. When this command is executed, termination occurs immediately, the rewind is started, then the drive is shown off-line. The drive will remain off-line until the tape reaches BOT, the cartridge is removed, and a cartridge is reinserted.

The NO-OP command causes a tape retension pass.

The Rewind with Immediate Interrupt causes the tape to be rewound to BOT. This command differs from the normal rewind command in that termination occurs at the start of rewind. This command is applicable to multi-transport systems. The Motion (MOT) bit in MXST0 will be set if a Get Status command is performed.

3.4.9. Initialize Command

This command performs a NO-OP. Normal termination occurs but no action is performed.



Initialize Command Packet

3.4.10. Write Subsystem Memory Command

This command was defined to allow a diagnostic program to access almost every area of the controller. However, due to the differences in implementation of the MSV05B, this command is not implemented and will terminate with a Function Reject with the Illegal Command (ILC) bit set.

Section 4

Hardware Description

4. OVERVIEW

This section reviews the controller block diagram concentrating on the host interface, device interface and the micro engine architecture. In addition a complete description of all inputs and outputs is provided.

4.1. BLOCK DIAGRAM

The block diagram of the MSV05B is shown in Figure 4-1. During a DMA write, data are transferred from the Q-BUS to RAM and from RAM to the tape drive. During a DMA read, data are transferred from the tape drive to RAM, and from the RAM to the Q-BUS. The microengine does not handle data directly. It directs the data at a block level, supervises all operations within the controller, and handles commands and status for the Q-BUS. The block diagram is divided into 3 major sections: Q-BUS interface, microengine, and drive interface. They will be described in more detail in the text that follows.

4.1.1. Q-Bus Interface

The Q-BUS interface communicates data, commands, and status to the Q-BUS. It is subdivided into the following:

4.1.1.1. Q-Bus Data/Address Interface

Buffers data, address, command, and status information.

4.1.1.2. Bus Data Register

Passes bidirectional DMA data and receives command packet address from the Q-BUS.

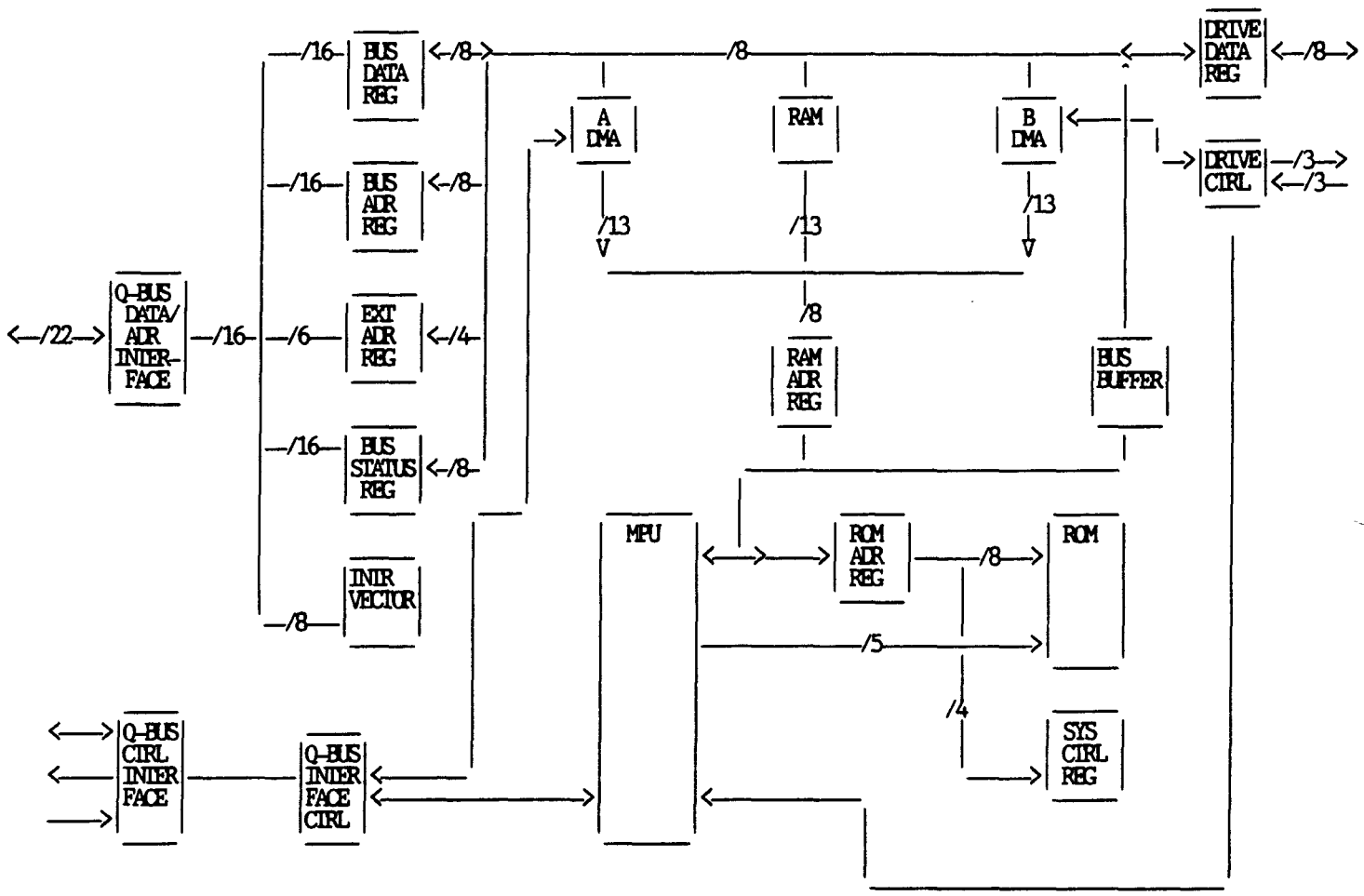


Figure 4-1 MSV05B Block Diagram

4.1.1.3. Bus Address Register

Generates the 16 lower address bits for DMA operations. It is incremented for each transfer (twice for word). A carry is forwarded to the extended address register. It is loaded with the starting address by the MPU at the start of each transfer.

4.1.1.4. Extended Address Register

Handles address bits 16-21. It is loaded from the Q-BUS for command packet pointer, or from the MPU at start of DMA transfers.
During DMAs, it is incremented on a carry from the address register.

4.1.1.5. Interrupt Vector

Is output to the Q-BUS during an interrupt

4.1.1.6. Q-Bus Control Interface

Buffers the Q-BUS control lines.

4.1.1.7. Q-Bus Interface Control

Handles all handshaking with the Q-BUS. It acquires the bus for DMA and interrupt operations and controls the bus registers and interface. It passes control and status between the interface and the MPU and A-DMA controller.

4.1.1.8. A-DMA

Addresses internal RAM for the data communicated on the Q-BUS. It also keeps the byte count and interrupts the MPU when the transfer is complete.

4.1.2. Microengine

The microengine supervises all functions within the controller. It recognizes commands from the Q-BUS and returns status information. It sends the necessary commands to the tape drive and processes drive status. It keeps track of the ring buffer, determines when there are free blocks to be filled or full blocks to be emptied and calculates block addresses which are passed on to the DMA controllers.

4.1.2.1. MPU

Is the heart of the microengine. It fetches and executes instructions and does calculations necessary for its control functions. It has access to one page of the RAM buffer which it uses for writing and reading control headers and for handling command and message packets.

4.1.2.2. ROM Address Register

Holds the lower 8 bits of the ROM address during the data portion of the instruction fetch.

4.1.2.3. ROM

Holds all the instructions for the MPU.

4.1.2.4. System Control Register

Contains 16 individual control lines selected by 4 bits of the ROM address. When enabled by a MPU port bit, these signals are used to enable internal bus sources, clock data into bus destinations, and perform various control functions.

4.1.2.5. BUS Buffer

Isolates the microengine from the internal data bus so that the MPU can fetch and execute instructions while DMA operations are being performed by the DMA controllers.

4.1.2.6. RAM Address Register

Holds the RAM address during the data portion of a RAM read or write cycle by the MPU. Addresses 8 - 14 are pulled high for this function.

4.1.2.7. RAM

Contains 32 pages of 512 bytes each for the temporary storage of data. Since the MPU is not in the data path, all data into or out of the controller must pass through the RAM.

4.1.3. Drive Interface

The drive interface passes data, control, and status between the controller and the tape drive.

4.1.3.1. B-DMA

Addresses RAM for data to or from the tape drive. It keeps track of the byte count and informs the microengine of the block completion.

4.1.3.2. Drive Data Register

Transmits and receives data over the drive data lines.

4.1.3.3. Drive Control

Performs the handshaking with the tape drive interface. It controls the drive data register and communicates with the B-DMA controller for byte transfer timing.

4.2. TECHNICAL DESCRIPTION

4.2.1. Q-BUS Interface

4.2.1.1. Input/Output Pin Assignments

Pin	Mnemonic	Function
AA1	BIRQ5 L	Interrupt request priority level 5
AB1	BIRQ6 L	Interrupt request priority level 6
AC1	BDAL16 L	Address line 16/memory error line.
AD1	BDAL17 L	Address line 17/memory error enable
AE1	SSPARE1	Special spare
AF1	SSPARE2	Special spare
AH1	SSPARE3	Special spare
AJ1	GND	Ground
AK1	MSPAREA	Maintenance spare
AL1	MSPAREB	Maintenance spare
AM1	GND	Ground
AN1	BDMRL	Direct memory Access (DMA) request
AP1	BHALT	Processor halt
AR1	BREF L	Memory refresh
AS1	+5B or +12B	+12 or +5 Vdc battery backup power
AT1	GND	Ground
AU1	PSPARE1	Power spare 1
AV1	+5B	+5 V battery power
BA1	BDCOK H	DC power OK
BB1	BPOK H	AC power OK
BC1	BDAL18 L	Address line 18
BD1	BDAL19 L	Address line 19
BE1	BDAL20 L	Address line 20

BF1	BDAL21 L	Address line 21
BH1	SSPARE	Special spare
BJ1	GND	Ground
BK1	MSPAREB	Maintenance spares
BL1	MSPAREB	Maintenance spares
BM1	GND	Ground
BN1	BSACK L	This signal is asserted by a DMA device in response to the processor's BDMGO L signal, indicating that the DMA device is bus master.
BP1	BIRQ7 L	Interrupt request priority level 7
BR1	BEVNT L	External event interrupt request
BS1	+12B	+12 Vdc battery backup power
BT1	GND	Ground
BU1	PSPARE2	Power spare 2
BV1	+5	+5 V power
AA2	+5	+5 power
AB2	-12	-12 V power (optional)
AC2	GND	Ground
AD2	+12	+12 V power
AE2	BDOUT L	Data output
AF2	BRPLY L	Reply is asserted in response to BDIN L or BDOUT L and during IAK transaction.
AH2	BDIN L	Data input is used for two type of bus operation: 1. When asserted during BSYNC L time, BDIN L implies an input transfer with respect to the current bus master. 2. When asserted without BSYNC L, it indicates that an interrupt operation is occurring.
AJ2	BSYNC L	Synchronize is asserted by the bus master device to indicate that it has placed an address on the bus.
AK2	BWTBT L	Write/byte is used in two ways to control a bus cycle: 1. It is asserted during the leading edge of BSYNC L to indicate that an output sequence is to follow. 2. It is asserted during BDOUT L, in a DATOB bus cycle, for byte addressing.
AL2	BIRQ4 L	Interrupt request priority level 4
AM2	BIAKI L	Interrupt acknowledge in
AN2	BIAKO L	Interrupt acknowledge out
AP2	BBS7 L	Bank 7 select--The bus master asserts this signal to reference the I/O page.
AR2	BDMGI L	Direct memory access grant--in
AS2	BDMGO L	Direct memory access grant--out
AT2	BINIT L	Initialize
AU2	BDAL0 L	Data/address line 00
AV2	BDAL1 L	Data/address line 01
BA2	+5	+5 Vdc power power
BB2	-12	-12 Vdc power (optional)
BC2	GND	Power supply return

BD2	+12	+12 Vdc power
BE2	BDAL2 L	Data/address line 02
BF2	BDAL3 L	Data/address line 03
BH2	BDAL4 L	Data/address line 04
BJ2	BDAL5 L	Data/address line 05
BK2	BDAL6 L	Data/address line 06
BL2	BDAL7 L	Data/address line 07
BM2	BDAL8 L	Data/address line 08
BN2	BDAL9 L	Data/address line 09
BP2	BDAL10 L	Data/address line 10
BR2	BDAL11 L	Data/address line 11
BS2	BDAL12 L	Data/address line 12
BT2	BDAL13 L	Data/address line 13
BU2	BDAL14 L	Data/address line 14
BV2	BDAL15 L	Data/address line 15

4.2.2. Tape Drive Interface

4.2.2.1. Input/Output Pin Assignments

PIN#	NAME	DESCRIPTION
12	HB7	HOST BUS BIT 7 - MSb of 8 bit bi-directional data bus
14	HB6	HOST BUS BIT 6
16	HB5	HOST BUS BIT 5
18	HB4	HOST BUS BIT 4
20	HB3	HOST BUS BIT 3
22	HB2	HOST BUS BIT 2
24	HB1	HOST BUS BIT 1
26	HB0	HOST BUS BIT 0 - LSb of 8 bit bi-directional data bus
28	ONL	ON LINE - This signal is grounded by the host. Always On line.
30	REQ	REQUEST - Host generated signal which indicates that command data have been placed on the data bus or status data have been accepted from the data bus.
32	RST	RESET - Host generated to cause drive reset. Same as power up reset.
34	XFR	TRANSFER - Host generated to indicate write data have been placed on, or read data have been taken from the data bus
36	ACK	ACKNOWLEDGE - Drive generated to indicate that the drive has taken write data from, or placed read data on the data bus.
38	RDY	READY - Drive generated to indicate the following: 1 command data have been taken from the bus 2 status data have been placed on the bus 3 rewind, retension, or erase command has completed

4 a buffer is ready to be filled, or a write file mark may be issued in write mode
5 a write file mark has completed
6 a buffer is ready to be emptied in read mode
7 the drive is ready to receive a new command

40	EXC	EXCEPTION - Drive generated to indicate an exception condition within the drive
42	DIR	DIRECTION - Drive generated to control the direction of the bi-directional data bus. False (high) indicates host to drive, true (low) indicates drive to host.

All odd pins are grounded at both host and drive.

Section 5

Software Considerations

5. GENERAL

Operational characteristics of cartridge tape drives supporting QIC-24 format and adhering to the QIC-02 interface standard limit the MSV05B controller from fully emulating the TSV05 subsystem. A few commands used by the various utilities of DEC operating systems and diagnostics are not supported. This section addresses those limitations and points out alternative methods of use providing a performance and function trade-off.

5.1. OPERATION WITH DEC DIAGNOSTICS

Most DEC system users possess the XXDP+ diagnostic programs for verifying proper operation of peripherial devices, controllers and processors included within their system. Since the MSV05B emulation does not support all TSV05 commands, most XXDP+ diagnostic test functions are not supported.

5.2. MTI DIAGNOSTICS

The diagnostics supplied with the MSV05B are a set of programs designed to exercise and report the operational status of the MSV05B controller. These programs are user friendly and exceptionally easy to use (refer to MTI Diagnostics Manual, Part No. 830002-130).

5.3. OPERATION WITH RT-11

The MSV05B supports a comprehensive set of file and device oriented backup utilities for RT-11. These utilities include the backup and utility program (BUP), the device utility program (DUP), the peripheral interchange program (PIP) and the source and binary compare utilities (SRCCOM and BINCOM). Although there are several methods of using this device the following sections outline the optimal use of the MSV05B controller.

Copy or PIP under RT-11 does not support multi-volume operations. Upon detecting end of tape, PIP prompts with "Pip-F-device full!"

5.3.1. Backup Utility Program (BUP)

BUP is a specialized file transfer program for backing up and restoring large files or volumes. Using this utility an RL02 or equivalent disk can be backed up in less than three minutes. The program's design makes effective use of the MSV05B streaming mode. No special operating consideration is necessary when using the MSV05B as a single backup device. The following examples show keyboard monitor and applicable command string interpreter (CSI) commands for performing device and file backup and restore operations:

Keyboard	CSI
Backing up a device on the tape	
	.RUN BUP
.BACKUP/DEVICE DK: MS:	*MS:=DK:/I
Restoring the device from the tape	
	.RUN BUP
.BACKUP/DEVICE/RESTORE MS: DK:	*DK:=MS:/I/X
Backup of a file	
	.RUN BUP
.BACKUP DK:FILENAME.EXT MS:	*MS:=DK:FILENAME.EXT
Restoring a file	
	.RUN BUP
.BACKUP/RESTORE MS: FILENAME.EXE DK:	*DK:=MS:FILENAME.EXT/X

Multi-volume Backup operations should proceed as follows:

```
.BAC/DEV DU: MS:

Mount output volume in MS0; Continue? Y

MS0:/BUP Initialize; Are you sure? Y

?BUP-I-Creating volume 1

Mount output volume in MS0; Continue? Y

MS0:/BUP Initialize; Are you sure? Y

?BUP-I-Creating volume 2

BUP-I-Copy operation complete
.
```

5.3.2. Device Utility Program (DUP)

DUP is a device maintenance program used to initialize and create files. Although DUP doesn't make full use the MSV05B features it provides several alternate backup methods. The following examples show the various DUP functions performed with the MSV05B:

Keyboard	CSI
Initializing the tape	
	.RUN DUP
.INITIALIZE MS:	*MS:/Z
Copying a device to a file	
	.RUN DUP
.COPY/DEVICE/FILE DL: MS:DL.DSK	*MS:DL.DSK=DL:*.*/I/F
Restoring a device from a file	
	.RUN DUP
.COPY/DEVICE/FILE MS:DL.DSK DL:	*DL:*.*=MS:DL.DSK/I/F
Initialize bootable tape	
	.RUN DUP
.INITIALIZE/FILE:MBOT16.BOT MS:	*MS:=DK:MBOT16.BOT/Z
An alternative to BUP for storing multi-volumes on tape	
	.RUN DUP
.COPY/DEVICE/FILE DL0: MS:DL0.DSK	*MS:DL0.DSK=DL0:*.*/I/F
.COPY/DEVICE/FILE DL1: MS:DL1.DSK	*MS:DL1.DSK=DL1:*.*/I/F
.COPY/DEVICE/FILE DY1: MS:DY1.DSK	*MS:DY1.DSK=DY1:*.*/I/F
Restoration can be selective	
	.RUN DUP
.INITIALIZE/NOQUERY DY:	*DY:/Z/Y
.COPY/DEVICE/FILE MS:DY1.DSK DY:	*DY:*.*=MS:DY1.DSK/I/F

5.3.3. Peripheral Interchange Program (PIP)

PIP is a file transfer and file maintenance utility program. Like DUP, the PIP program does not buffer its input/output data sufficiently to allow the MSV05B to maintain continuous streaming. All PIP functions are supported by the MSV05B except the VERIFY or /H switch option. Source and binary compare utilities can be used to provided the verify function. An example of PIP commands to copy various types of files to and from the cartridge tape:

Keyboard	CSI
Copying all MAC files to tape	
	.RUN PIP
.COPY DL:*.MAC MS:/POS:-1	*MS:/M:-1=DL:*.MAC

Copying entire tape to disk

```
.COPY MS:*.*/POS:0 DL:*.*
```

```
.RUN PIP
*DL:*.*=MS:*.*/M:0/W
```

Selective copy of a tape file to disk

```
.COPY MS:ONEFIL.MAC/POS:0 DL:
```

```
.RUN PIP
*DL:*.*=MS:ONEFIL.MAC/M:0/W
```

Operations involving multiple file transfers to tape should include the position switch setting of minus one (-1). This will eliminate the excess tape positioning performed by PIP at the completion of each file transfer.

5.3.4. Source and Binary Compare Utility

The source and binary comparison programs (SRCCOM and BINCOM) compare two ASCII or binary files and lists the differences between them. These utilities can be used to perform the verify function of PIP which is unsupported. An example of each utility is as follows:

Keyboard

```
Verification of ASCII type files

.DIFF MS:*.MAC DL:*.MAC
```

CSI

```
.RUN SRCCOM
*TT:=MS:*.MAC,DL:*.MAC
```

Keyboard

```
Verification of binary type files

.DIFF/BINARY MS:*.SAV DL1:*.SAV
```

CSI

```
.RUN BINCOM
*TT:=MS:*.SAV,DL1:*.SAV
```

5.3.5. Making a Bootable RT-11 Tape

When the MSV05B is used as the primary system backup device the importance of bootable tapes is evident. Consider a Winchester disk based system which has the MSV05B as the load medium. Such a system requires bootable tapes that contain executable programs which allow the user to format the Winchester disk, perform the initial loading of the operating system, and/or restore system backups. The example command file shown will create a bootable MSV05B tape containing all the files referenced. This command file can be modified to add or delete files as required. The tape generated may be used as a method of getting the BUP utility onto a disk in order to then restore a previously generated BUP backup tape or to run standalone programs such as diagnostics.

Example of a command file which would build a bootable tape containing various individual files:

```
ASSIGN DKn DIS
ASSIGN MS TAP
!
! LOGICAL NAME 'DIS:' MUST BE ASSIGNED TO THE SOURCE DISK
! LOGICAL NAME 'TAP:' MUST BE ASSIGNED TO THE TAPE BEING BUILT
```

```
!
! INTITALIZE BOOTABLE TAPE
!
INITIALIZE/NOQUERY/VOLUMEID/FILE:DIS:MBOT16.BOT TAP:
RTV5
DIS MT 1/2
!
! BUILD THE TAPE - FILE ORDERING IS IMPORTANT!
! COPY MDUP FILES
!
COPY/SYS DIS:MSBOOT.BOT TAP:MSBOOT.BOT/POS:-1
COPY/SYS DIS:MDUP.MS TAP:MDUP.MM/POS:-1
COPY/SYS DIS:MDUP.MS TAP:MDUP.MT/POS:-1
COPY/SYS DIS:MDUP.MS TAP:MDUP.MS/POS:-1
!
! COPY MONITOR FILES
!
COPY/SYS DIS:SWAP.SYS TAP:SWAP.SYS/POS:-1
COPY/SYS DIS:RT11SJ.SYS TAP:RT11SJ.SYS/POS:-1
!
! TT MUST FOLLOW MONITOR
!
COPY/SYS DIS:TT.SYS TAP:TT.SYS/POS:-1
!
! COPY ALL DISK HANDLERS
!
COPY/SYS DIS:DL.SYS TAP:DL.SYS/POS:-1
COPY/SYS DIS:DY.SYS TAP:DY.SYS/POS:-1
COPY/SYS DIS:DU.SYS TAP:DU.SYS/POS:-1
COPY/SYS DIS:MS.SYS TAP:MS.SYS/POS:-1
COPY/SYS DIS:VM.SYS TAP:VM.SYS/POS:-1
COPY/SYS DIS:NL.SYS TAP:NL.SYS/POS:-1
!
! COPY SYSTEM UTILITIES
!
! PIP, DUP, DIR MUST BE FIRST, IN THAT ORDER
!
COPY DIS:PIP.SAV TAP:PIP.SAV/POS:-1
COPY DIS:DUP.SAV TAP:DUP.SAV/POS:-1
COPY DIS:DIR.SAV TAP:DIR.SAV/POS:-1
COPY DIS:IND.SAV TAP:IND.SAV/POS:-1
COPY DIS:BUP.SAV TAP:BUP.SAV/POS:-1
COPY DIS:STARTS.COM TAP:STARTS.COM/POS:-1
!
! COPY STANDALONE DISK FORMATTER/DIAGNOSTIC
!
COPY DIS:RL02DG.SYS TAP:RL02DG.SYS/POS:-1
```

Command File Example 1

Note that the COPY commands uses the qualifier /POS:-1. This keeps the tape from rewinding between each file, making the transfer much faster. Copy operations from tape to disk should use the qualifier /POS:0; this

will cause the tape to rewind initially but does not rewind between files.

The following command file is an adaptation of DISMT1 to build a bootable image of Micro Technologys RL02DG.SYS disk formatter utility.

This file could be used to build a bootable image of any standalone RT-11 type program. Bootable programs copied to tape in this manner will be self starting and should prompt the user as they normally would shortly after the boot operation is started.

Example of a command file which would build a bootable tape containing only the desired program:

```
ASSIGN DKn DIS
ASSIGN MS TAP
!
! LOGICAL NAME 'DIS:' MUST BE ASSIGNED TO THE SOURCE DISK
! LOGICAL NAME 'TAP:' MUST BE ASSIGNED TO THE TAPE BEING BUILT
!
! INTITALIZE BOOTABLE TAPE
!
INITIALIZE/NOQUERY/VOLUMEID/FILE:DIS:MBOT16.BOT TAP:
RTV5
DIS MT 1/2
!
! COPY BOOTABLE MTI DIAGNOSTIC ONTO TAPE RENAMING IT
! MSBOOT.BOT SO MBOT16.BOT CAN FIND IT AND BOOT IT.
!
COPY/SYS DIS:RL02DG.SYS TAP:MSBOOT.BOT/POS:-1
```

Command File Example 2

The tapes generated by these command files will be bootable using the available hardware bootstraps or the MSV05B boot program described in Appendix A. Once a tape containg MSBOOT is successfully booted it will give the following prompt:

```
MSBOOT V05-00
*
```

If the tape has been booted in order to load a standalone program or diagnostic, that program name should be entered now(e.g.,RL02DG.SYS). MSBOOT will then search the tape for the desired program, load it into memory and transfer control at the starting address. If the tape was booted to load system software or perform a backup operation, the user must enter " MDUP.MS ". The MSV05B will then load MDUP.MS from the tape and it will prompt with:

```
MDUP V05.01
*
```

At the "*" prompt the user can initialize the target disk by entering " DDn:/Z " or cause MDUP to do the restore operation by entering " DDn:A=MS: " where DDn: is the target disk (i.e. " DL0: "). MDUP restores a minimal RT-11 system from the MSV05B and then attempts to boot it. Once this minimal system is running, other files on the MSV05B may be restored by using COPY command:

```
COPY/SYS/NOREPLACE MS:*.* DDn:
or
COPY MS:INFILE.EXT DDn:
```

At this point the BUP utility could be used to restore backup tapes to the approiate devices. See section 5.3.1 for BUP operation.

5.3.5.1. MSBOOT Bootable Program

Any standalone RT-11 structured program can be made bootable by use of the following guide lines. The MSBOOT program searches the input device to locate and read the specified file into memory. After successfully loading the program, MSBOOT starts the loaded program at the relative start address minus 2 specified in block 0 offset 40 of the program image. It is therefore necessary for the user to insure that the bootable program start address is preceeded by a valid one word instruction (e.g. HALT, NOP, etc.). An alternate method is to modify location 40 of the program in question:

```
.R SIPP
*Program.SAV
Base?
Offset?   40
Base          Offset        Old     New?
 000000        000040     xxxxxx     xxxxxx+2
 000000        000042     xxxxxx     ^Y
*^C
.
```

Note that this method requires that the program's location be restored prior to running it under an RT-11 monitor.

If you are attempting to create a bootable tape containg only the desired program as described previously by Command File Example 2, it is not necessary to change the start address.

5.3.6. Unsupported Utility Function

All switch options are supported with the exception of the PIP verify, switch option /V. This option requires the support of the backspace command (not currently supported). There is no work around for this function at this time.

NOTE

The MSV05B is a fast and reliable device for performing backup function. However, when used with utilities not designed to provide data at a high rate the controller and therefore its drive may not stream continuously.

5.4. OPERATION WITH RSX-11M

The volume manipulation programs supported by the multiuser RSX-11M system are utilities suitably designed to embellish the operation of the MSV05B controller.

5.4.1. RSX11M PIP

An example of an RSX11M PIP operation follows:

```
>ALL MSO:                              ; Allocate MSO:
>INIT MSO:MTI                          ; Init volume
>MOU MSO:MTI                           ; Mount volume
>PIP                                   ; Invoke PIP
PIP>MSO:=DUO:[*,*]*.*;*                ; Copy all files to
                                       ; tape
MTAACP -- MOUNT NEXT VOLUME ON MSO:    ; This message will
                                       ; occur if another
                                       ; tape is required.
PIP>                                   ; Normal termination
```

5.4.2. Backup and Restore Utility (BRU)

The backup and restore utility (BRU) online and stand-alone versions (BRUSYS.SYS or BRU64K.SYS) can be used with the MSV05B cartridge tape unit. The "/VERIFY" switch can only be used if the tape is to contain only one backup set. If "/VERIFY/APPEND" switch combination is used, BRU will try to backspace to the beginning of the appended backup set to verify it. The MSV05B will report an error on this backup operation.

The following are examples of backup and restore commands:

Backing up the system device

```
>BRU/REWIND/MOUNT/VERIFY SY: MS:
```

Restore to like device

```
>BRU/REWIND/VERIFY/INITIALIZE MS: DL1:
```

Restoring a file

```
>BRU/REWIND/VERIFY MS:[1,51]BRU64K.SYS DL:
```

Backing up an account

```
>BRU/REWIND/MOUNT DL:[1,54] MS:
```

Appending an account to a previously generated backup tape

```
>BRU/REWIND/MOUNT/APPEND DL:[1,54] MS:
```

Preparing for account restore

```
>PIP [ggg,mmm]*.*;*/DE
```

Restoring account

```
>BRU/REW MS: DL:[ggg,mmm]
```

Comparing previous restore for verification

```
>BRU/COMPARE/REW MS: DL:[ggg,mmm]
```

An example of a multi-volume BRU:

```
>BRU/REW/MOU DU: MS:

BRU - Staring Tape 1 on MS0:

BRU - End of Tape 1 on MS0:

BRU - Mount Tape 2 on MS0:                    ; At this point
                                              ; operator must
                                              ; insert new tape
BRU - End of Tape 2 on MS0:

BRU - Completed

BRU>
```

5.4.2.1. Creating a Standalone BRU Tape

The following example assumes that the stand-alone backup and restore program BRU64K.SYS and BRU64K.STB, its symbol table file, are located in UIC [1,51]:

Build image of stand-alone program

```
>VMR [1,51]BRU64K
```

Writes bootable image

```
VMR>SAVE MS:BRU64K
```

5.4.2.2. Creating a Bootable BRU Tape

The MS: boot on the quad-wide 11/23 (KDF11-B) and 11/73 (KDF11-B) boards will not boot RSX stand-alone BRU tapes because it loads the tape boot block into memory and looks for a NOP (240) in location 0. RSX stand-alone BRU boot blocks have a BR+20 (410) in location 0 so the boot progran assumes it is not bootable. In order to use either processor ROM boot program the boot block must be patched to contain a NOP (240) in location 0 and a BR+16 (407) in location 2.

This example illustrates one method of patching and generating a bootable BRU tape.

```
>VMR                                    ; Invoke VMR
ENTER FILENAME:  BRU64K                 ; Create a bootable image
VMR>SAV MS:BRU64K                       ; Save it on tape
VMR>^Z                                  ; Exit VMR
>FLX                                    ; Invoke FLX
FLX>MS:[*,*]/DO/LI                      ; Directory of MS0:

DIRECTORY        MS:[0,0]
29-APR-74

MFRH$/LN8.LAL           257.      12-AUG-78 <40> [40,40]

TOTAL OF 257. BLOCKS IN 1. FILES

FLX>DU0:[1,51]/IM=MS:[*,*]*.LAL/DO      ; Copy the image from Tape to
                                        ;  Disk
FLX>^Z                                  ; Exit FLX
>RENAME *.LAL;* BRU64K.SAV              ; Give it a meaningful name
>ZAP                                    ; Invoke ZAP
ZAP>DU0:[1,51]BRU64K.SAV/AB             ; Open the file
_0/                                     ; Dump location zero
000: 000000/  000410                    ; It contains a BR+20
_240                                    ; Change loc. 0 to a 240
_407                                    ; Change loc. 2 to a 407
_X                                      ; Exit ZAP
>FLX                                    ; Invoke FLX
FLX>MS:/ZE/DO                           ; Initialize the tape
FLX>MS:/IM/DO=DU0:[1,51]BRU64K.SAV/RS   ; Copy out the patched file
FLX>^Z                                  ; Exit FLX
>                                       ; Done
```

5.4.2.3. Restoring a Bootable BRU Tape

If hardware bootstrap isn't available then the program listed in Appendix A can be used and is entered into memory starting at address 7776. Once

the code has been entered and verified, start the processor at location 10000 with line clock disabled. At the completion of the bootstrap operation, indicated by program identification at system console, enable the line clock. Additional information will be displayed. Refer to section 7.5 of the RSX-11M Utilities Manual for further operating instruction. Since the default vector address established for the MS device is incorrect, it is important that the user enter the following command when using the MSV05B as one of the BRU devices:

```
MS:/VEC=224
```

5.4.3. Disk Save and Compress Utility (DSC)

The disk save and compress utility (DSC) and stand-alone versions (DSCSYS.SYS/DSC64K.SYS) can be used with the MSV05B controller to save and restore disks volumes. The following RSX commands are examples of how to use DSC with the MSV05B:

Compressing disk to tape

```
>DSC MS:/RW=DL1:
```

Restoring tape to disk

```
>DSC DL2:=MS:/RS
```

Comparing input and output volumes

```
>DSC DL2:=MS:/RW/CMP
```

5.4.4. Unsupported Operations

The BRU "/APPEND/VER" switch combination is not supported.

5.5. OPERATION WITH RSTS

The capabilities of the MSV05B controller are well suited for the role of backup within the RSTS timesharing environment. The backup package of programs allows the user to preserve and recall files stored under one or more user accounts.

5.5.1. Save and Restore Utility (SAV/RES)

All tape options of the SAVE and RESTORE function are supported by the MVS05.

An example of a SAVRES operation is as follows:

```
Option: SAVRES <CR>

SAV/RES Function: SAVE <CR>

From RSTS disk? DL0 :<CR>

***  Pack ID/default Save Set Name is "NAME"

To device? MS0: <CR>

***  Save Set Name is "NAME"

Expiration Date <dd-mmm-yy>? <LF>

Verify (Yes or No) <No>? <LF>

Proceed (Yes or No)? Yes <CR>

***  Initiating first SAVE volume

***  Begin SAVE from DL0: to MS0: at hh:mm AM/PM
```

The SAVRES utility now does the save operation and after completion reports the results and some timing information.

5.5.2. Backup Utility

BACKUP is a menu driven utility allowing the user to back up any number of individual accounts or files. Basic operations provided by this utility are supported by the MSV05B. As of this writing, the limited space reverse capabilities of the MSV05B will cause BACKUP to report an error at the completion of its operation if the index file contains more than approximately 160 entries. Even though an error is reported, the tape generated by this operation is good and the index file may be dumped or the accounts restored. An error is also encountered at the end of tape during a multi-volume backup. The message "retry legal" will be displayed. Type "RETRY <CR>". Backup will rewind the tape, search forward, then read verify the last record and request the next volume.

5.5.3. RSTS/E PIP

RSTS/E PIP operations are supported by the MSV05B. A few examples of basic PIP operation follow:

```
*MS0:/ZE                          Zero MS0

*MS0: = SY:[1,2]                  Copy all the files in
                                  account [1,2] onto tape
```

```
*SY[1,1] = MSO:[1,2]*.SAV          Copy all the files with the
                                   .SAV extenstion in account
                                   [1,2] from tape to the system
                                   disk account [1,1]
```

The following DCL commands demonstrate additional RSTS/E tape operations:

```
>INIT MSO:                                  ; Init the tape
Density will be 1600
Tape will be in DOS format
Any existing files on the tape will be deleted
Proceed (Y or N)?  Y
>
>COPY SY:[2,3] MSO:[2,3]                    ; DCL logs files
                                            ; copied

[File SY:[2,3]ERRLOG.FIL copied to MSO:[2,3]ERRLOG.FIL]
            "                 "             "
            "                 "             "
[File SY:]2,3]ERRDIS.HLP copied to MSO:[2,3]ERRDIS.HLP]
>
```

PIP does not support multi-volume tapes when in DOS format.

```
>PIP
*MSO:/ZE
Really zero MSO:/PARITY:ODD/DENSITY:1600 ? Y
*MSO:[*,*]=SY:[*,*]*.*
; Upon reaching EOT, PIP will prompt with:
?No room for user on device - file MSO:[*,*]file.ext
*
```

The following command sequences show multi-volume operation in ANSI mode:

```
>INIT MSO:MTI
Density will be 1600
Tape will be in ANSI format
Any existing file will be deleted
Proceed (Y or N)?       Y
>
>PIP
*MSO:[*,*]=SY:[*,*]*.*                      ; copy all the files

%End of ANSI magtape output volume has      ; end of tape
%been reached
```

```
%Please type the device name and unit      ; new, initialized
%number of the drive where the next        ; tape must be
%volume may be found              ? MSO:   ; inserted

*                                          ; normal completion
```

5.6. OPERATION WITH MICROVMS

The MicroVMS operating system as supplied by DEC does not support TS-11 type devices because no TS-11 driver is provided. A MicroVMS TS-11 driver which will operate on the MicroVAX I or MicroVAX II processors is available from Micro Technology Inc.

In order to provide full tape support, the System Program Developement option (SYSP) of MicroVMS is required. Included in the SYSP option is the Magnetic Tape Ancillary Control Process (MTACP) which is required to support the tape as a file structured device. Baseline MicroVMS will support TS11 for backup and restore operations only.

Some default files (SYSLOGIN.COM) equate the INIT command to INIT/NOHIGHWATER. Since magtapes do not support this option an error occurs upon initialization as follows:

```
$ INIT MSA0: LABEL<CR>
%INIT-F-ILLOPT, qualifier(s) not appropriate to this device
```

If this occurs, the SYSLOGIN.COM file can be modified or the INIT/HIGHWATER Command can be used to override the defaults as follows:

```
$ INIT/HIGHWATER MSA0: LABEL<CR>
```

5.6.1. MicroVMS Backup

The Backup facility available under MicroVMS can be used to backup entire disks, accounts or individual files. Backup requires the tape to be mounted foreign. This can be accomplished as follows:

```
$ MOUNT/FOR MSA0:
%MOUNT-I-MOUNTED,       mounted on _MSA0:
$
```

By default, the BACKUP utility uses three data buffers during backup operations, each 8kb in size, and performs a Cyclic Redundancy Check (CRC) on save-set data. This command shows a disk image backup using the defaults:

```
$ BACKUP /REWIND /IMAGE
_From:   DUA0:
_To:     MSA0: LABEL /SAVE_SET
```

A major improvement in performance can be obtained by invoking the '/NOCRC' switch. This eliminates the software CRC calculation on the save-set data, which allows the MSV05B to maintain streaming and greatly

reduces the overall time required to backup. All QIC-02 drives perform a read-after-write data check which includes a CRC check. This makes the software CRC redundant.

```
$ BACKUP /REW /IMAGE /NOCRC
_From:   DUA0:
_To:     MSA0: LABEL /SAVE_SET
```

Additional speed improvements can be realized by increasing the number of buffers used to five with the '/BUFFERS=5' switch and by changing the size of blocks written to tape from 8kb to 65kb with the '/BLOCK_SIZE=65354' switch.

```
$ BACKUP /REW /IMAGE /NOCRC /BUFFERS=5 /BLOCK_SIZE=65354
_From:   DUA0:
_To:     MSA0: LABEL /SAVE_SET
```

Using a Standalone Backup Kit the image save-sets created by the previous command sequences can be restored to disk as follows.

```
$ BACKUP
_From:    MSA0: LABEL /SAVE_SET
_To:      DUA0:
```

Refer to the MicroVMS Users manual for further information regarding the use of the Backup command.

5.6.2. MicroVMS Copy

The MicroVMS copy facility allows the MSV05B to be used as a file oriented device. Copy requires that tapes be properly initialized and mounted.

```
$ INIT/HIGHWATER MSA0: LABEL
$ MOUNT MSA0: LABEL
%MOUNT-I-MOUNTED, LABEL mounted on _MSA0:
$
```

Once this is accomplished files can be transferred as follows:

```
$ COPY
_From:   SYS$MANAGER:SYSTARTUP.COM
_To:     MSA0:
```

Refer to the MicroVMS Users manual for further information regarding the use of the Copy command.

Appendix A

MSV05B BOOTSTRAP

MSV05B Bootstrap Program

The following code is provided for your use in bootstrapping an MSV05B tape. This program can be entered into memory from ODT and executed or assembled and run from an existing system device. An executable version is provided on the LABEL diagnostic diskette which was provided with your MSV05B controller. To invoke this program, boot the diagnostic diskette and at the "." prompt, type " R MSBOOT ".

```
 1                                  .TITLE  MS BOOTSTRAP MODULE
 2      000000                      .ASECT
 3              007776              . = 7776
 4      007776  046523              .WORD   "SM"            ;Device ID backwards
 5      010000  012701      START:  MOV     #172522,R1      ;R1=MSSR
                172522
 6      010004  010102              MOV     R1,R2           ;R2=MSSR
 7      010006  005000              CLR     R0              ;Clear R0
 8      010010  105711      1$:     TSTB    @R1             ;Wait for SSR
 9      010012  100376              BPL     1$
10      010014  010704              MOV     PC,R4           ;R4=PC of "SM"+20
11      010016  112737              MOVB    #200,@#172523   ;Write byte bit 15
                000200
                172523
12      010024  005242              INC     -(R2)           ;Write into MSDB
13      010026  105711      2$:     TSTB    @R1             ;Wait for SSR
14      010030  100376              BPL     2$
15      010032  005711              TST     @R1             ;? Error ?
16      010034  100761              BMI     START           ;If SC=1 retry, else
17      010036  005007              CLR     PC              ;jump to zero...
18              010000              .END    START
```