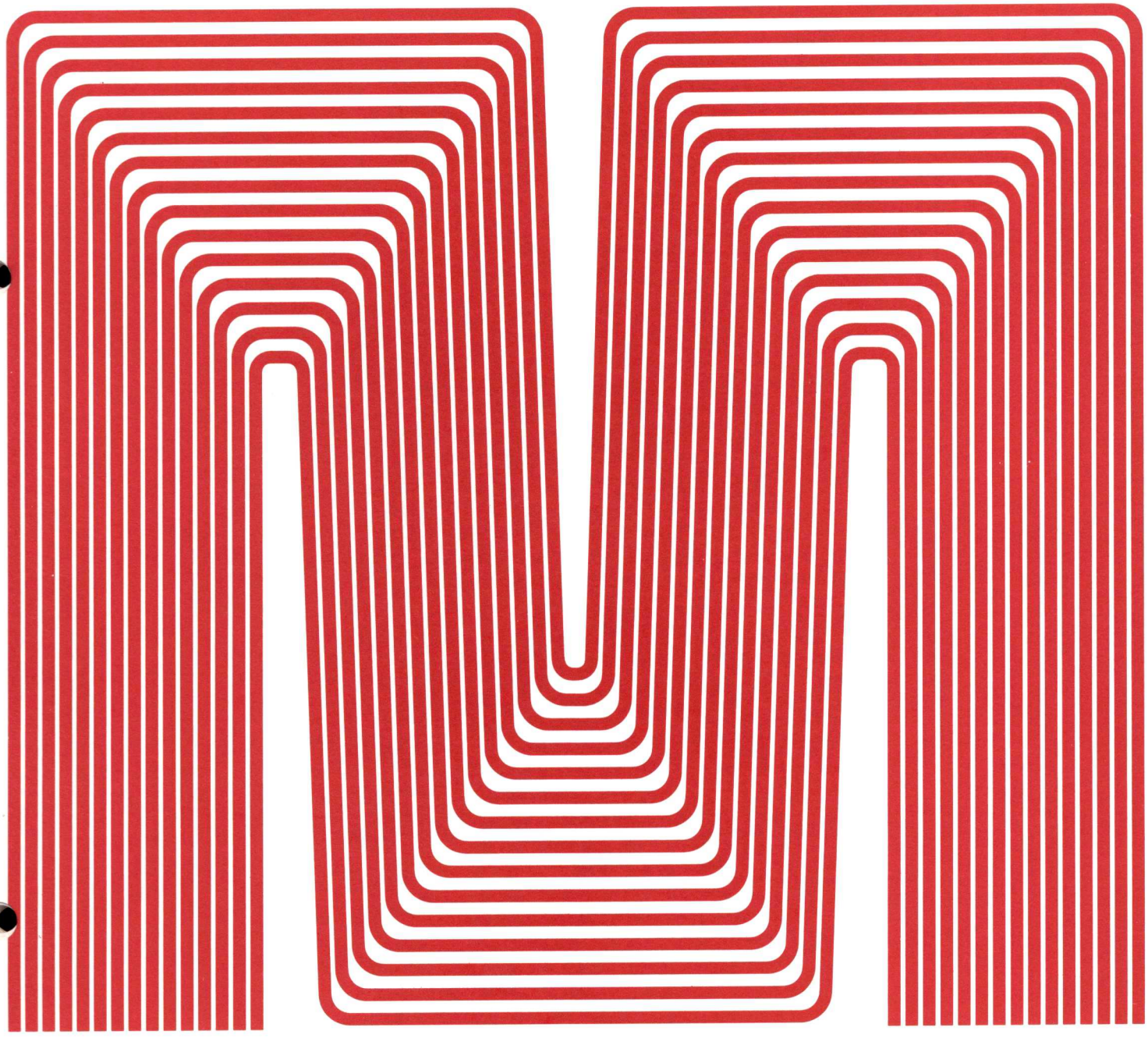
MicroSystems Inc.

Micro 800 Computer Reference Manual



MICRO 800 COMPUTER

REFERENCE MANUAL

69–3–0800–001

June 1969

MICRO SYSTEMS INC. · 644 East Young Street · Santa Ana, California 92705

Printed in USA

TABLE OF CONTENTS

APPENDIXES

ILLUSTRATIONS

TABLES

MICRO 800 COMPUTER

1. SYSTEM DESIGN FEATURES

MICRO 800 is a small byte oriented microprogrammed computer designed for dedicated applications. The functional, mechanical and electrical design of the computer result in a set of functional elements which can be tailored to specific application requirements. The MICRO 800 is a basic set of hardware which forms the basis for a series of machines.

The design concepts embodied in the MICRO 800 provide a unique combination of features unavailable in other small computer systems. These include:

Microprogramming

The MICRO 800 incorporates a set of commands that exert powerful micro-control over the machine's data manipulation paths and control. Command sequences which form microprograms are stored in a read only storage. The MICRO 800 can be programmed to emulate instructions of general or special purpose computer or to perform specific applications.

Speed

The machine incorporates a 1.1 microsecond core memory cycle time and a 220 nanosecond command execution time. This speed permits rapid emulation of macro instructions and can be used to minimize interface hardware by applying the speed of the machine to interface functions.

Modularity

The modular electrical and mechanical design results in the flexibility needed to apply the MICRO 800 to a wide range of applications. The modular design of the core memory read only storage, processor options, and input/output elements permits expansion of the system as required. The compact 8-3/4 inch high enclosure has a number of spare circuit board slots and ample power for system and peripheral interfaces even when the processor is fully expanded.

Low Cost

The MICRO 800 uses TTL monolithic integrated circuits including a large number of the medium scale integration type for savings in parts and assembly time. The use of a read only storage for control further reduces the number of circuits that might otherwise be required to provide the same functional capability. Packaging and powering of the MICRO 800 has been designed for small "micro" systems resulting in a savings in system cost.

Software

Programs for the MICRO 800 include: An assembler written in FORTRAN for use on large-scale computers, utility programs for generating the read only storage maps, and processor and memory diagnostics.

GENERAL CHARACTERISTICS

The advanced features and operating characteristics include:

- Memory addressing to 32k
- 4096 byte memory modules
- 16,384 bytes of memory in basic 8-3/4 inch high cabinent
- 1.1 microsecond memory speed (full cycle)
- 8, 9 or 10 bit memory bytes for efficient character handling; extra bits for memory parity and special application
- direct memory access (DMA) option
- 16 general-purpose eight-bit file registers
- up to 1024 words of read only storage in 256 word modules
- 220 nanosecond microcommand execution time
- real-time clock (optional)
- memory protect (optional)
- power-fail option for automatic shutdown in the event of a power failure, and automatic startup when power returns
- seven I/O transfer modes
- 15 basic commands
- three versions of control consoles
- TTL integrated circuitry
- operating temperature range 0°C to 50°C
- dimensions: 8-3/4 inches high, 19 inches wide, 23 inches deep
- power: 115/230 vac, 50-60 cycle

MICRO 810 MACRO-PROGRAMMED COMPUTER

The MICRO 810 is a microprogrammed adaptation of the MICRO 800 hardware. The microprogram (firmware) converts the basic MICRO 800 system into a software programmable macro level general purpose computer. Detailed description of the MICRO 810 can be found in the MICRO 810 Reference Manual. The salient characteristics of this machine include:

- variable length instructions
- 16-bit accumulator, extended accumulator, and index register
- eight memory referencing address modes
- multiply and divide
- variable 8, 16, 24, and 32-bit operations
- programmed, buffered concurrent, and DMA input/output transfers
- priority interrupt system
- software includes: two pass assembler, and teletype operating system
- bootstrap loader in non-volatile read only storage
- up to 64 priority interrupts expandable in groups of 8

2. SYSTEM ORGANIZATION GENERAL DESCRIPTION

The MICRO 800 is a bus organized machine built around a file of 16 programmable registers and employing microprogrammed control. The basic elements of the machine are shown in the block diagram of Figure 1.

The machine executes 15 basic commands with many variations. All commands are 16 bits in length and are one of two formats. MICRO 800 programs, which are known as microprograms, are placed in a read only storage and thereafter become a part of the machine's hardware. The program can be changed by replacing the printed circuit boards containing the read only storage. The commands read out of the store control all aspects of the operation of the basic machine and are executed in a single machine clock cycle.

The eight-bit arithmetic/logic unit performs all manipulation of data including: addition, logical AND, logical OR, logical exclusive OR, and one bit left and right shifts. The output of this logic network is the A-bus which is the input to the file and other machine registers. All byte data movement is performed over this bus. The output of the file is one of the inputs to the arithmetic/logic unit; the other is the B bus. Inputs to this bus are determined by the command, its options, and the I/O mode. Bus inputs are the true output of the T register, the complement output of the T register, the Input bus and the eight bit literal contained in some commands.

The memory data and address busses communicate between the four memory modules, the processor and the DMA option. Either the processor or the DMA may operate with the memory, with the DMA having top priority.

The registers, file, arithmetic/logic unit and bussing are organized onto two identical "data" printed circuit boards–a four bit slice of the machine on each board. All command decoding, control, clock generation and memory timing are located on a single "control" board. Each 256 words of read only storage requires a single board and the core memory requires a pair of boards.

REGISTERS AND FILE

There are eight registers and 16 file registers. Each of the registers has a specific use in the processor, while the file is used for general storage and flags.

T Register

The eight-bit T register serves as the operand register for most of the operate class commands, and as a buffer register for output and memory operations. The T register is expanded to nine bits when the spare memory bit option is included in the processor. Both the true and complement output of the T register can be gated to the B-bus as an operand. When both the contents of T and its complement are selected as operands, the effective operand is all 1-bits; while if neither is selected the operand is all 0-bits.

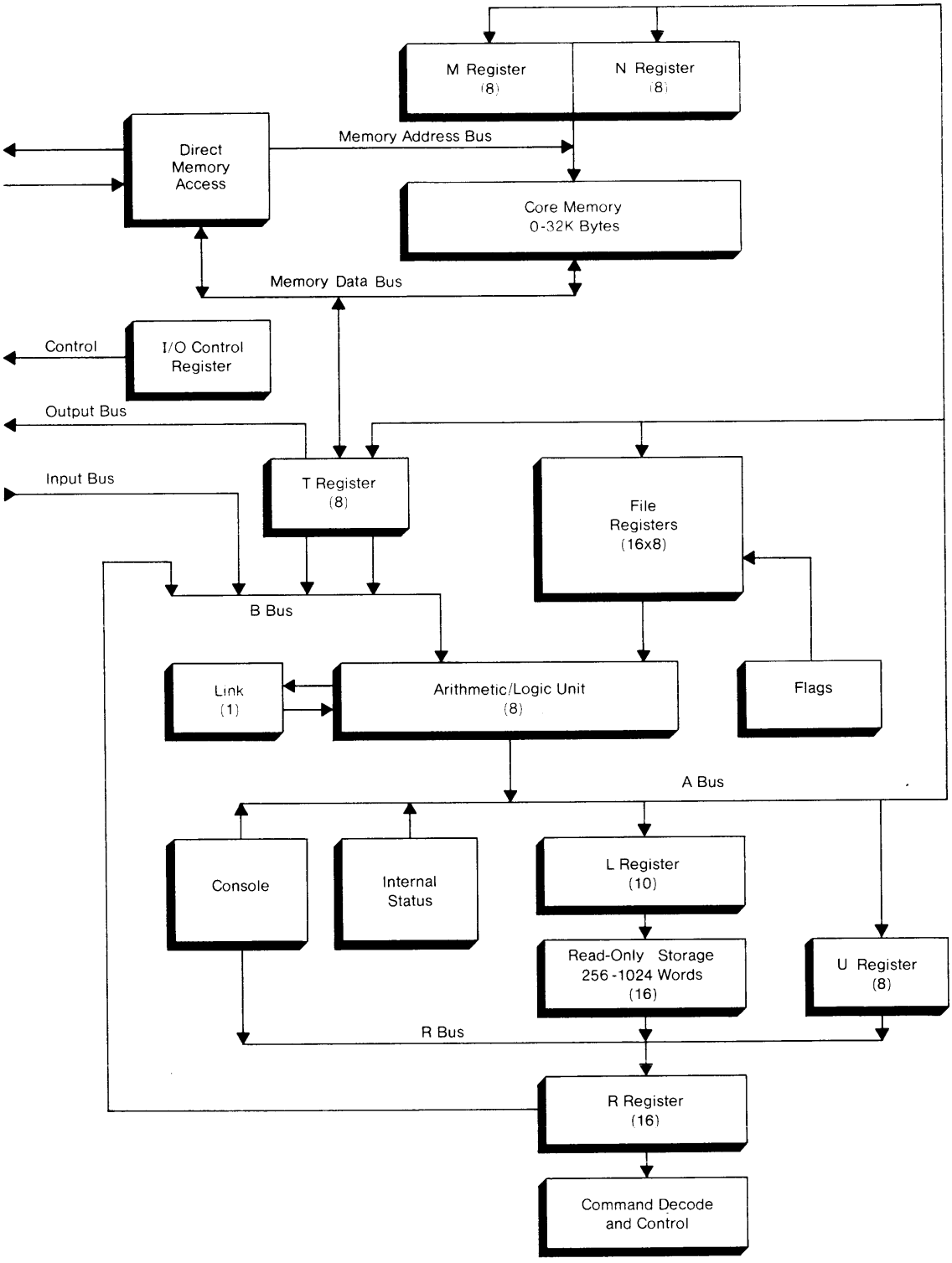


FIGURE 1. MICRO 800 BLOCK DIAGRAM

M Register

The eight-bit M register contains the seven high order bits of the processor memory address. This register is gated onto the memory address bus at all times except when a DMA operation is in process.

N Register

The eight-bit N register contains the eight low order bits of the processor memory address. This register is gated onto the memory address bus at all times except when a DMA memory operation is in process.

L Register

The 10-bit L register is the machines' program counter and contains the read only storage address of the next command to be executed, unless altered by a Jump command. The eight low order bits of the L register are a counter which is incremented by one at each clock time when the processor is running unless, there is a command execution delay imposed.

U Register

The eight-bit U register is used to modify the output of the read only storage. For commands with 0's in the four high order bits or 1's in bit 15 and the three low order bits, the contents of the U register is inclusive -ORed with the eight high order bits of the read only storage output as it is gated into the R register. This allows for dynamic modification and changing of operation codes and file register designators.

R Register

The 16-bit register holds the command being executed. Its output is decoded and controls the operation of the processor at each clock time.

LINK Register

The one-bit LINK register holds the adder's high order carry from Add, Subtract, and Compare commands and the shifted off end bit from the Shift command.

I/O Control Register

This three-bit register generates the control signals for the I/O bus by a decoding of the register outputs. It is loaded and cleared by a Control command and therefore the timing of I/O control signals is under command control. There are three output modes and four input modes. The high order bit of the register is the input flag. When this bit is a 1-bit the Input bus is substituted for the T register when it is selected and the Input bus is the source of data when executing an external I/O Control command.

File Registers

The file consists of 16 eight-bit operational registers. All commands except the load register (1) specify a file register to be operated on or to provide an operand. All file registers are

functionally identical except for file register 0 which contains eight flags, and cannot be used for general storage. The flags of file register 0 are given in Table 1.

TABLE 1. FILE REGISTER 0 FLAGS

BIT	FLAG
0	– Overflow Result Condition
1	– Negative Result Condition
2	– Zero Result Condition
3	– Concurrent I/O Request Line
4	– Internal Interrupt
5	– I/O Reply Line
6	– Serial Teletype and/or T_8
7	– External Interrupt Line

CORE MEMORY

The magnetic core memory is organized into two board pluggable modules of 4096 bytes. The memory is addressed at the byte level and each byte contains 8, 9, or 10 bits. The ninth and tenth bits are devoted to the spare memory bit and memory parity bit options. Memory may be expanded up to four modules (16,384 bytes) within the basic 8-3/4 inches cabinet. Addressing to 32,768 bytes permits modular expansion using an auxiliary cabinet.

The memory is operated in read/write and full/half cycle operations. The full-cycle memory timing is five 220 ns clock cycles (1.1 microseconds); the half-cycle timing in the system is three clock cycles (660 ns). For a read operation, the accessed data is placed in the T register two clock cycles after the start of the memory operation. Full cycle regeneration of the data in the memory does not require the use of the T register and T may be modified by the microprogram before completion of the restore part of the cycle.

The four memory modules plug into the memory address and data busses which run vertically on the back-plane. A spare board slot wired for access to this bus is dedicated to one or more direct memory access options which can include a DMA I/O channel, a special DMA peripheral controller, and expansion to additional memory modules outside the basic enclosure.

READ ONLY STORAGE

The read only storage provides the storage for commands and constants of the microprogram. Its output is gated into the R register where it controls the operation of the machine at the next clock time.

The read only storage is organized into modules of 256 words contained on a single printed circuit board. Each of the four possible read only storage boards receives an address from the L register via the read only storage address bus, and the selected board gates its addressed contents onto the read only storage data bus where it is entered into the R register.

The store is constructed of diodes with a diode being placed at the proper coordinates for 1-bits in the commands. The commands are designed to use 0-bits as the normal case to reduce the number of diodes on the board; on the average, about 1/3 of the total bits contain ones.

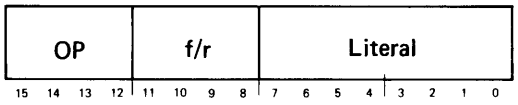
The read only storage is always accessed for the next command while the current command is being executed. This lookahead helps achieve faster command execution time. When the sequence of command execution is altered by a jump or skip, an additional cycle must be taken to perform an access before the next command is executed. When the machine is halted, the L register contains the address of the first command to be executed when operation is started.

COMMAND FORMATS

There are three basic command formats. Each command is 16 bits in length and is contained in a single read only storage location.

Literal Commands

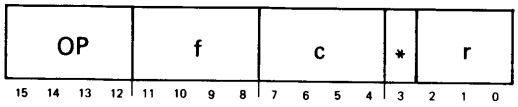
The literal class of commands have the following format:



In this format the operation code occupies the four high order bits. Bits 11-8 contain either a file register designator (f) or a register or control group designator (r). Bits 7-0 contain an eight-bit literal which is transferred as an operand to the B-bus.

Operate Commands

The operate class of commands have the following format:



In this format the operation code occupies the four high order bits. Bits 11-8 contain a file register designator (f) which specifies one of the 16 file registers to be used in command execution. Bits 7-4 contain control option bits (c) which are unique to the specific command. When bit 3 is a one, the result of an operate class command is inhibited from being placed in the designated file register. Symbolically, this is specified to the program assembler by appending an * to the command mnemonic. The register designator (r) in bits 2-0 specifies a processor register to receive the result of the operation. The register's

identifier is added as a second character of the command mnemonic. The register codes are given below:

TABLE 2. REGISTER DESIGNATORS FOR OPERATE COMMANDS

DESIGNATOR	MNEMONIC	REGISTER
0		none
1	T	T Register
2	M	M Register
3	N	N Register
4	L	L Register—addresses: 000-OFF and 200-2FF
5	K	L Register—addresses: 100-1FF and 300-3FF
6	U	U Register
7	S	U Register ORed into command (except for Control command)

Execute Command

The execute command causes the contents of the U register to be ORed with the eight high order bits of the command to form an effective command. This operation is also performed when r = 7 for the operate class commands. The Execute command has zero-bits in the four high order bits. The remainder of the command has the format required for the effective command to be executed.

STATUS AND CONDITION FLAGS

Internal Status

Eight internal status bits are provided to designate a particular internal interrupt condition. When any of the internal status bits are a 1-bit, the internal interrupt flag (bit 4) in file register 0 is also a 1-bit. This flag bit is tested by the microprogram to detect the presence of the internal interrupt condition. The internal status bits are entered via the A-bus into the selected file register by a Control command, at which time the status bits are cleared. The eight internal status bits have the assignments given in Table 3.

TABLE 3. INTERNAL STATUS BITS

BIT	INTERNAL STATUS
0	Console Interrupt
1	(spare)
2	Real-Time Clock Interrupt
3	Memory Protect Error Interrupt
4	Memory Parity Error Interrupt
5	Memory Boundary Error Interrupt
6	Console Halt Switch
7	Power Fail/Restart Interrupt

All the internal status bits except the console interrupt and halt are associated with processor options and may be reassigned for special applications.

Condition Flags

The overflow, negative and zero conditions resulting from an operation involving the arithmetic/logic unit may be stored in file register 0, (see Table 1). The condition flags are updated for command 7 and for commands 8, 9, B – F if bit 4 is a 1-bit. These condition flags can be tested by the microprogram for implementing various conditional operations. Definition of the condition flags is as follows:

Overflow – The Overflow condition flag stores the arithemtic overflow condition during an Add, Subtract or Copy command. Arithmetic overflow occures when the carry out of the high order bit of the adder differs from the carry into the high order bit. The overflow condition flag stores the shifted off end bit during a Shift command.

Negative – The Negative condition flag stores the high order bit of the result on the A-bus.

Zero – The Zero condition flag stores the zero test condition of the result on the A-bus. When the link control (bit 7) of the operate commands is a 1-bit, the zero condition flag may not be set to indicate a zero result unless it is already set; it may be reset to indicate a non-zero result. This provides a linked zero test over multiple bytes of a variable byte operation.

COMMAND TIMING

Each command is executed in a single clock cycle time, although execution may be delayed because of core memory or read only storage operations. The system clock rate is 4.55 mHz, and the clock cycle 220 nanoseconds.

Memory Busy Delays

If the memory is busy, because of processor or DMA operation, at the time a Read or Write memory command or a command which will modify the M or N registers is to be executed, execution is delayed until the memory operation is completed. These commands are executed on the last clock of the memory half or full cycle. If a DMA request is pending at the time a Read or Write memory command is to be executed, execution is delayed to give the DMA memory priority.

Memory Data Delays

Operate class commands which select the contents of either the T register or its complement during the first two cycles of a processor memory read operation are executed during the third cycle of the read operation. This allows time for the accessed byte to be placed in the T register.

Read Only Storage Delays

An extra cycle is required for command execution because of the look ahead nature of the read only storage for the following conditions:

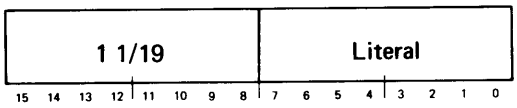
- Jump command
- Test If Zero command when a skip occurs
- Test If Not Zero command when a skip occurs
- Compare command when a skip occurs
- Operate class commands which have the L register designated

3. COMMAND REPERTOIRE

This section contains descriptions of all MICRO 800 commands. With each description is a diagram showing the format of the command and its operation code, given in hexadecimal. Above each diagram is the command's mnemonic code and the name of the command. Under each diagram is a description of the command, followed by a list of the registers and indicators that can be affected by the command. The timing of each command is one clock cycle (220 ns) unless the L register is designated as the destination of the result, in which case the command execution time is two cycles.

LITERAL COMMANDS

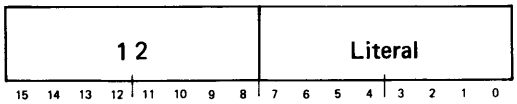
LT LOAD T



The contents of the eight-bit literal field are placed in the T register. If the spare memory bit option is implemented in the machine, T_8 is cleared with code 11 and is set to a 1-bit with code 19. The condition flags and LINK register are not affected.

Affected: T

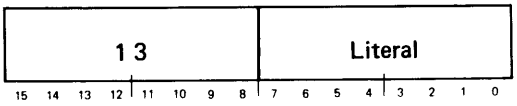
LM LOAD M



The contents of the eight-bit literal field are placed in the M register. The condition flags and LINK register are not affected.

Affected: M

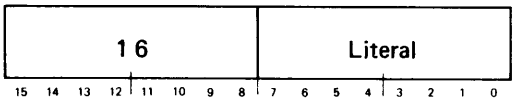
LN LOAD N



The contents of the eight-bit literal field are placed in the N register and the M register is cleared. The condition flags and LINK register are not affected.

Affected: M, N

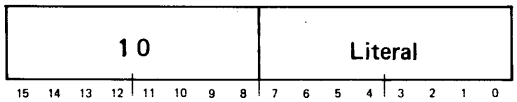
LU LOAD U



The contents of the eight-bit literal field are placed in the U register. The condition flags and LINK register are not affected.

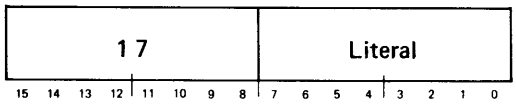
Affected: U

LZ LOAD ZERO CONTROL



The eight bits of the literal field may be used to perform control functions for special applications. No control funtions in this group are implemented in the standard machine.

LS LOAD SEVEN CONTROL



The eight bits of the literal perform control functions as described below. If more than one bit of the literal field is on at a time, the last two digits of the command are determined by ORing the bits of the literal.

1700 – **No Operation**

1701 – **Enable Serial Teletype**: The serial teletype input is gated to bit 6 of file register 0, (see Table 1) for one clock cycle when the spare memory bit option is implemented.

1702 – **Reset T_8**: When the spare memory bit option is implemented, T_8 is cleared.

1F02 – **Set T_8**: When the spare memory bit option is implemented, T_8 is set to a 1-bit.

1704 – **Disable External Interrupts**: Recognition of external interrupts is inhibited.

1708 – **Enable External Interrupts**: Recognition of external interrupts is enabled.

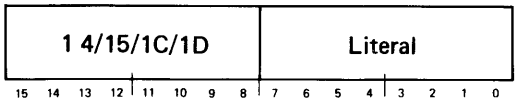
1710 – **Disable Real Time Clock**: The real-time clock and interrupt are disabled.

1720 – **Enable Real Time Clock**: The real-time clock and interrupt are enabled.

1740 – **Load Protect Bit**: The content of bit 8 of the T register (T_7) is placed in the memory protect control storage for the memory page currently addressed by the contents of the M register.

1780 – **Halt**: The processor is halted.

JP JUMP

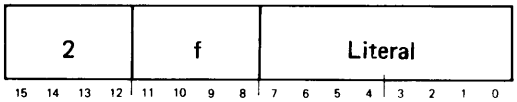


The contents of the eight-bit literal are placed in the eight low order bits of the L register; the content of bit 8 is placed in L_8 and the content of bit 11 is placed in L_9. The location of the next command to be executed is at the address specified by the new contents of the L register. The execution time of the command is two cycles. The Jump operation codes for the four 256 word pages in read only storage are as follows:

14 – Jump to locations 000-0FF (page 0)
15 – Jump to locations 100-1FF (page 1)
1C – Jump to locations 200-2FF (page 2)
1D – Jump to locations 300-3FF (page 3)

Affected: L

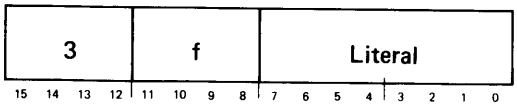
LF LOAD FILE



The contents of the eight-bit literal field are placed in the file register designated by f. File register 0 can not be loaded by this command. The condition flags and LINK register are not affected.

Affected: F

AF ADD TO FILE



The contents of the eight-bit literal field are added to the contents of the file register designated by f and the sum replaces the original contents of the file register. Subtraction is performed by placing the 2's complement of the number in the literal field. The condition flags and LINK register are not affected.

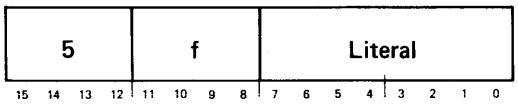
Affected: F

TZ TEST IF ZERO

If, for all the 1-bits of the literal field, the corresponding bits of the file register designated by f are 0-bits, the next command is skipped. The condition flags, LINK register and file register are not affected. If the skip is taken, the timing of the command is two clock cycles.

Affected: L

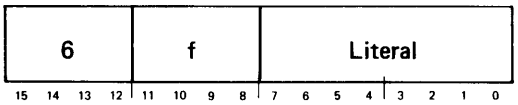
TN TEST IF NOT ZERO



If, for any bit of the literal field which is a 1-bit, the corresponding bit of the file register designated by f is also a 1-bit, the next command is skipped. The condition flags, LINK register and file register are not affected. If the skip is taken the timing of the command is two clock cycles.

Affected: L

CP COMPARE

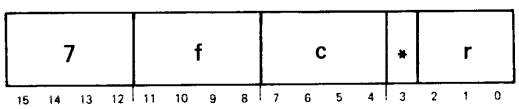


If the sum of the contents of the file register designated by f and the contents of the eight-bit literal is greater than 2^8-1, the next command is skipped. The condition flags, and file register are not affected. If the skip is taken the timing of the command is two clock cycles. The LINK stores the carry out of the adder.

Affected: LINK, L

OPERATE COMMANDS

K CONTROL



Control operations associated with special data flow and input/output are performed by this command. The exact operation is designated by the c field as explained below. Source data from the file, internal status, console sense switches or input bus are placed in the file register designated by f, if * is a 0-bit, and the register designated by r. The condition flags are unconditionally updated. Destination r = 7 is undefined for this command.

When c equals 8-F, the operations are associated with external input/output, and the three low order bits of c are placed in the I/O Control register. On the same operation, data can be moved from the designated file register or the input bus, as determined by the current contents of the I/O Control register, to the designated file or destination register. The data source is specified as follows:

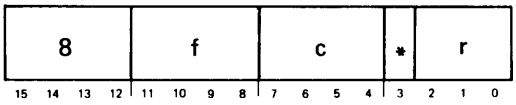
I/O Control Register Mode	Source
0 – 3	Designated file register
4 – 7	Input bus

The operations designated by c are described below:

c	Operation	Explanation
0	– No Operation	
1	– Enter Sense Switches:	The status of the four console sense switches are placed in the four high order bits of the file register designated by f. The four low order bits are set to 1-bits.
2	– Shift File Right 4:	The four high order bits of the file register designated by f are placed in four low order bits of the file register. The four high order bits are set to 1-bits.
4	– Enter Internal Status:	The eight internal status bits are placed in the file register designated by f.
7	– Enter Console Switches:	The contents of the eight low order console command switches are ANDed with the eight low order bits of the next command. File register 0 must be selected to prevent any modification of the file during the execution of the Control command. The command preceding this operation must not cause a read only storage delay.
8	– Clear I/O Mode:	The I/O Control register is cleared. Data from the designated file or Input bus can be transferred to the designated file register and register (r).
9-F	– Set I/O Mode:	The I/O Control register is loaded with the three low order bits of c placing it in one of seven I/O bus or serial teletype modes. These modes are described in Section 4. Data from the designated file or Input bus can be transferred to a designated file register and register (r).

Affected: F, I/O Control, Condition Flags, r

A ADD



The selected operand is added to the contents of the file register designated by f. The sum is placed in the file register (f), if * is a 0-bit, and in the register designated by r. The state of the carry out of the high order bit of the adder is placed in LINK. The c field controls selection of the operand, incrementing the result and modification of the condition flags as follows:

c-bits 7 6 5 4	Operation
1 x x x	**Link Control**:The content of LINK is added to the sum. The zero condition flag can be reset but cannot be set, providing a linked zero test over multiple bytes.
x 1 x x	**Add One**: One is added to the sum.
x x 1 x	**Select T**: The contents of the T register or the input bus are selected as the operand. If the T register is not selected, the operand is zero.
x x x 1	**Modify Condition Flags**: The condition flags are modified by execution of the command.

Affected: F, LINK, Condition Flags, r

S SUBTRACT

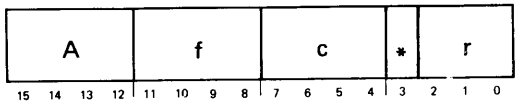
The complement of the selected operand plus one is added to the contents of the file register designated by f. The difference is placed in the file register (f) if * is a 0-bit, and in the register designated by r. The result is a 2's complement subtraction. The state of the carry out of the high order bit of the adder is placed in LINK. The c field controls selection of the operand, incrementing the result, and modification of the condition flags as follows:

c-bits 7 6 5 4	Operation
1 x x x	**Link Control**: The content of LINK is added to the sum. Selection of the LINK inhibits the automatic addition of one. The zero condition flag cannot be set, providing a linked zero test over multiple bytes.
x 1 x x	**Inhibit Add One**: If Link Control is not selected, one is automatically added to the result to produce a 2's complement subtraction. This control bit inhibits this addition, providing a 1's complement subtraction.

c-bits 7 6 5 4	Operation
x x 1 x	**Select T**: The complement of the contents of the T register are selected as the operand. If not selected, the operand consists of a 1-bit in each bit position.
x x x 1	**Modify Condition Flags**: The condition flags are modified by execution of the command.

Affected: F, LINK, Condition Flags, r

R READ MEMORY W WRITE MEMORY



The contents of the file register designated by f is unaltered, incremented, or decremented as controlled by the c field. The result is placed in the file register (f) if * is a 0-bit, and in the register designated by r. At the same time, a read (R) or write (W) memory operation is initiated as controlled by bit 4. If the operation is a memory read, the T register is cleared and the accessed data is set into the T register after two clock cycle times. Data to be written into memory must be placed in the T register before the write memory command, if the operation is a half cycle write, and by the first clock cycle time after the write memory command on a full cycle write The condition flags and LINK are not affected. Execution of the memory command is delayed if the memory is in a busy condition from a previous R or W command or DMA operation.

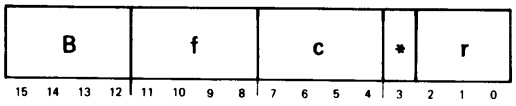
The bits of the c field control the transfer of data from the file register and the type of memory operation as follows:

c-bits 7 6 5 4	Operation
0 0 x x	**Transfer**: The contents of the file register are transferred unaltered.
0 1 x x	**Decrement**: The contents of the file register minus one are routed as specified. If the M register is selected as the destination and the content of LINK is a 1-bit, the contents of the file register are transferred without being decremented. This provides a decrement with link control when M is the destination.
1 0 x x	**Add Link**: The content of LINK is added to the contents of the file register, and the sum is transferred as specified.
1 1 x x	**Increment**: The contents of the file register plus one are transferred as specified.

c-bits 7 6 5 4	Operation
x x 1 x	**Half Cycle**: If this bit is a 1-bit, a half cycle memory operation is performed; otherwise a full cycle operation is selected.
x x x 1	**Write**: If this bit is a 1-bit, a write memory operation is performed; otherwise a read operation is selected.

Affected: F, Memory, r

C COPY

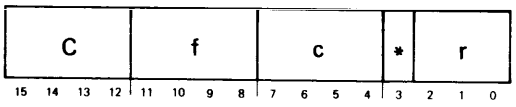


The selected operand is placed in the file register designated by f, if * is a 0-bit, and in the register designated by r. The LINK is not affected. The c field controls selection of the operand, incrementing the operand, and modification of condition flags as follows:

c-bits 7 6 5 4	Operation
1 x x x	**Link Control**: The content of LINK is added to the sum. The zero condition flag can be reset but cannot be set, providing a linked zero test over multiple bytes.
x 1 x x	**Add One**: One is added to the sum.
x x 1 x	**Select T**: The contents of the T register or Input bus are selected as the operand. If the T register is not selected, the operand is zero.
x x x 1	**Modify Condition Flags**: The condition flags are modified by execution of the command.

Affected: F, Condition Flags, r

O OR



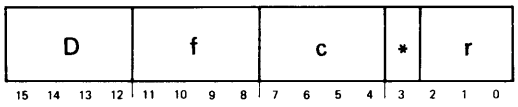
The selected operand is logically inclusive-ORed with the contents of the file register designated by f and the result is placed in the file register, if * is a 0-bit, and in the register

designated by r. The LINK is not affected. The c field controls selection of the operand and modification of the condition flags as shown below:

c-bits 7 6 5 4	Operation
1 x x x	**Link Control**: The zero condition flag can be reset but cannot be set, providing a linked zero test over multiple bytes.
x 1 x x	**Select Complement T**: The complement of the contents of the T register is selected as the operand. If the T register is also selected, the effective operand contains a 1-bit in each bit position.
x x 1 x	**Select T**: The Contents of the T register or Input bus are selected as the operand. If neither the T register nor the complement of the T register is selected, the operand is zero.
x x x 1	**Modify Condition Flags**: The condition flags are modified by execution of the command.

Affected: F, Condition Flags, r

X EXCLUSIVE OR

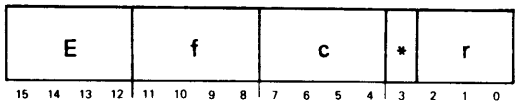


The selected operand is logically exclusive-ORed with the contents of the file register designated by f and the result is placed in the file register, if * is a 0-bit, and in the register designated by r. The LINK is not affected. The c field controls selection of the operand and modification of the condition flags as shown below:

c-bits 7 6 5 4	Operation
1 x x x	**Link Control**: The zero condition flag can be reset but cannot be set, providing a linked zero test over multiple bytes.
x 1 x x	**Select Complement T**: The complement of the contents of the T register are selected as the operand. If the T register is also selected, the effective operand contains a 1-bit in each bit position.
x x 1 x	**Select T**: The contents of the T register or Input bus are selected as the operand. If neither the T register nor the complement of the T register is selected, the operand is zero.
x x x 1	**Modify Condition Flags**: The condition flags are modified by execution of the command.

Affected: F, Condition flags, r

N AND

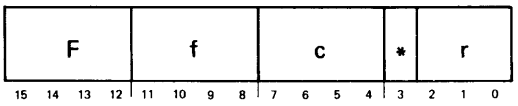


The selected operand is logically ANDed with the contents of the file register designated by f and the result is placed in the file register, if * is a 0-bit, and in the register designated by r. The LINK is not affected. The c field controls selection of the operand and modification of the condition flags as shown below:

c-bits 7 6 5 4	Operation
1 x x x	**Link Control**: The zero condition flag can be reset but cannot be set, providing a linked zero test over multiple bytes.
x 1 x x	**Select Complement T**: The complement of the contents of the T register are selected as the operand. If the T register is also selected, the effective operand contains a 1-bit in each bit position.
x x 1 x	**Select T**: The contents of the T register or Input bus are selected as the operand. If neither the T register nor the complement of the T register is selected, the operand is zero.
x x x 1	**Modify Condition Flags**: The condition flags are modified by execution of the command.

Affected: F, Condition Flags, r

H SHIFT



The contents of the file register designated by f is shifted left or right one bit position and placed in the file register, if * is a 0-bit, and in the register designated by r. The high order or low order bit which is shifted off is placed in LINK and in the overflow flag if the modify condition flag is selected. The c field controls the direction of shift, entry of an end bit, and modification of the condition flags as follows:

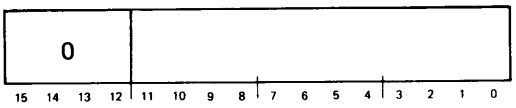
c-bits 7 6 5 4	Operation
1 x x x	**Link Control**: The content of the LINK is inserted into the vacated low order or high order bit position. The zero condition flag can be reset but cannot be set, providing a linked zero test over multiple bytes.
x 1 x x	**Insert One**: A 1-bit is unconditionally inserted into the vacated low order or high order bit position; otherwise a 0-bit is inserted unless the contents of LINK is selected.

c-bit 7 6 5 4	Operation
x x 1 x	**Shift Right**: If bit 5 is a 1-bit, the operation is a right shift; otherwise a left shift is performed.
x x x 1	**Modify Condition Flags**: The condition flags are modified by execution of the command. The content of the bit shifted out is placed in the overflow flag.

Affected: F, LINK Condition Flags, r

EXECUTE COMMAND

E EXECUTE



The eight-bit contents of the U register are ORed with the eight high order bits of the Execute command to form an effective command. This provides a means of partially modifying the contents of a read only storage location. The ORing is performed before the output of the read only storage is gated into the R register. The meaning of bits present in positions 0-11 is dependent upon the desired effective operation code after the modification. Due to the look ahead feature of the read only storage, the new contents of the U register is not available until after one machine cycle following the transfer of data to it.

4. INPUT/OUTPUT

GENERAL DESCRIPTION

The MICRO 800 input/output capability is powerful and easy to apply. The microprogramming can be used to achieve powerful and efficient input/output procedures. Standard procedures are defined for the MICRO 810 general purpose computer, and a complement of standard peripherals and interface devices compatable with these standards are available.

The MICRO 800 has three input/output facilities as shown in Figure 2. These are:

- Serial Teletype
- Direct Memory Access (DMA)
- Byte I/O Bus

A description of each follows in the remainder of this section. The three I/O facilities are included in the basic machine without the need for processor or I/O options. The DMA I/O is a hardware system. The serial teletype and Byte I/O bus systems are under microprogram control and therefore their functional capability and performance are firmware dependent. A description of the capability of the MICRO 810 I/O firmware is included.

SERIAL TELETYPE

The processor contains a serial teletype interface capable of communicating with a full duplex teletype. The input from the teletype appears as bit 6 of file register 0 where a 1-bit indicates that the teletype is transmitting a SPACE. The output to the teletype normally transmits a 20 milliampere MARKing current which can be keyed off to send a SPACE signal by placing the I/O Control register in mode 3. Character assembly and disassembly, including all timing and synchronization, are performed by microprogramming.

The serial teletype input/output is standard. A teletype wired for 4-wire full duplex 20 milliampere operation may be directly connected to the cable provided with the machine. Other types of serial I/O devices may also use this connection.

DIRECT MEMORY ACCESS

The direct memory access (DMA) interface allows for direct connection to the memory address, data and control busses. Within the machine enclosure there is a circuit board slot which is reserved for the DMA. This board may contain a channel to which a number of peripheral devices are connected, or a device controller which has direct memory access capability. Generally the DMA system will be customized for special applications.

The maximum data transfer rate is 910,000 bytes per second. The DMA I/O takes precedence over the processor for memory operations. The DMA must supply its own address control.

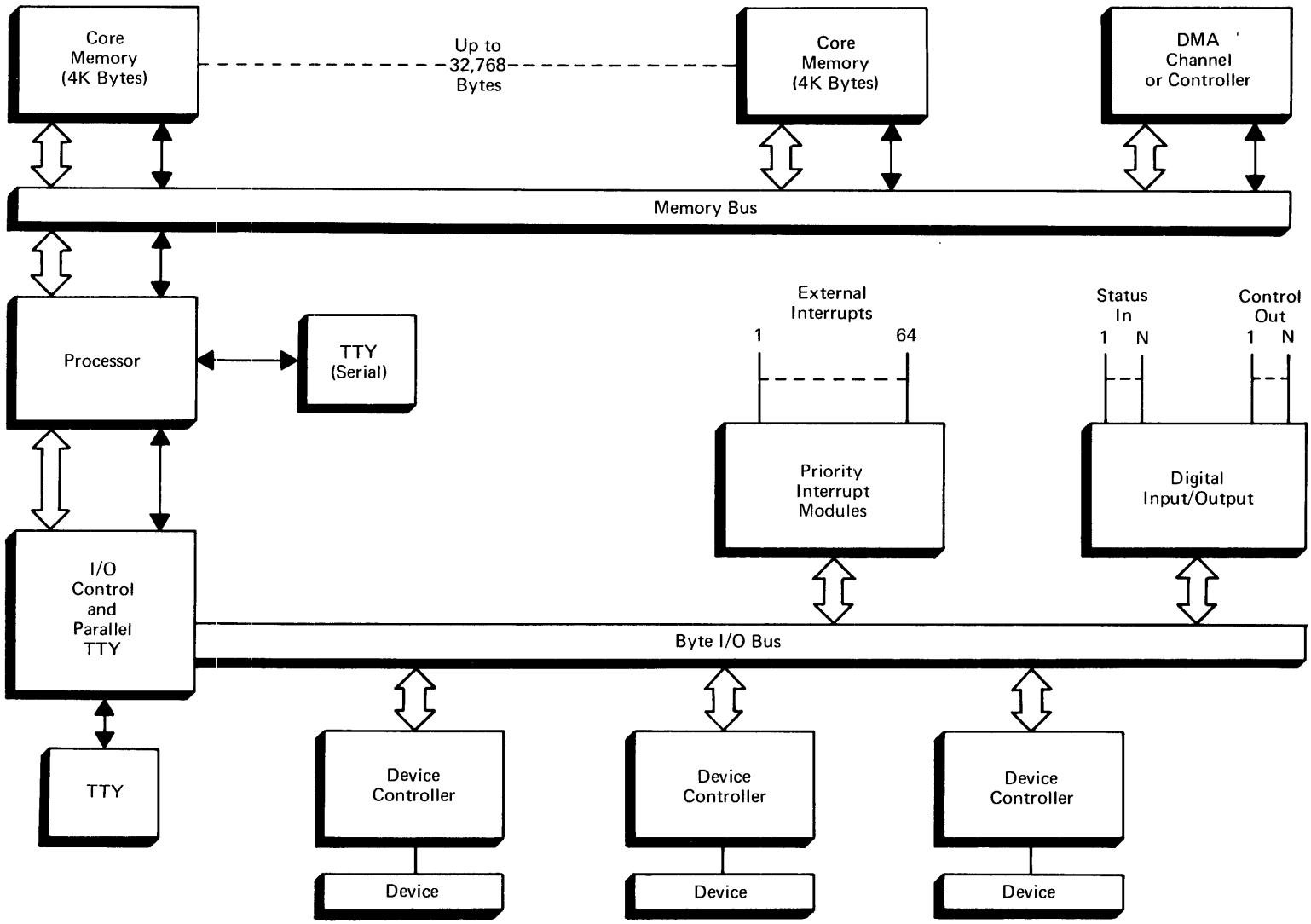


FIGURE 2. INPUT/OUTPUT ORGANIZATION

BYTE I/O BUS

The Byte I/O facility allows for data transfers over a party-line I/O bus under microprogram control. Firmware can implement macro I/O instructions and fully buffered concurrent I/O. This I/O facility consists of a byte input bus, a byte output bus, and a three-bit I/O Control register.

The I/O Control register is loaded by bits 6-4 of the Control command. The contents of the I/O control register defines a I/O bus mode. The output of the I/O Control register is decoded on an optional I/O control board and/or device controller boards to form individual control signals. These control signals define the type of transfer being performed on the Byte I/O bus and the state of the serial teletype output. Of the eight possible states of the I/O Control register one represents no activity on the bus, three are output modes, and four are input modes. One of the output modes removes the MARKing current from the serial teletype output causing a SPACE to be output.

The I/O Control register modes are given in Table 4 below:

TABLE 4. BYTE I/O CONTROL MODES

Mode	Control Activity
0	None
1	Control Output (COXX/)
2	Data Output (DOXX/)
3	Space Serial Teletype
4	Spare
5	I/O Acknowledge (IOAK/)
6	Data Input (DIXX/)
7	Spare

BUS LINES

The Byte I/O bus consists of the following lines:

- nine input data lines
- five input control lines
- nine output data lines
- ten output control lines

The arrangements of the input and output bus lines are shown in Figure 3.

Input Lines

The nine data lines are an input to the B bus gating, and the t_8 gating for the spare bit option. Three of the control lines are input to bits of file register 0 (see Table 1). The input lines are ground TRUE signals which are properly terminated at the processor. If the buss is carried out of the basic enclosure it must be terminated at the remote end also. Each peripheral device gates information onto the bus by means of open collector type 944 DTL drive circuits. Up to 15 drivers may be connected to each line.

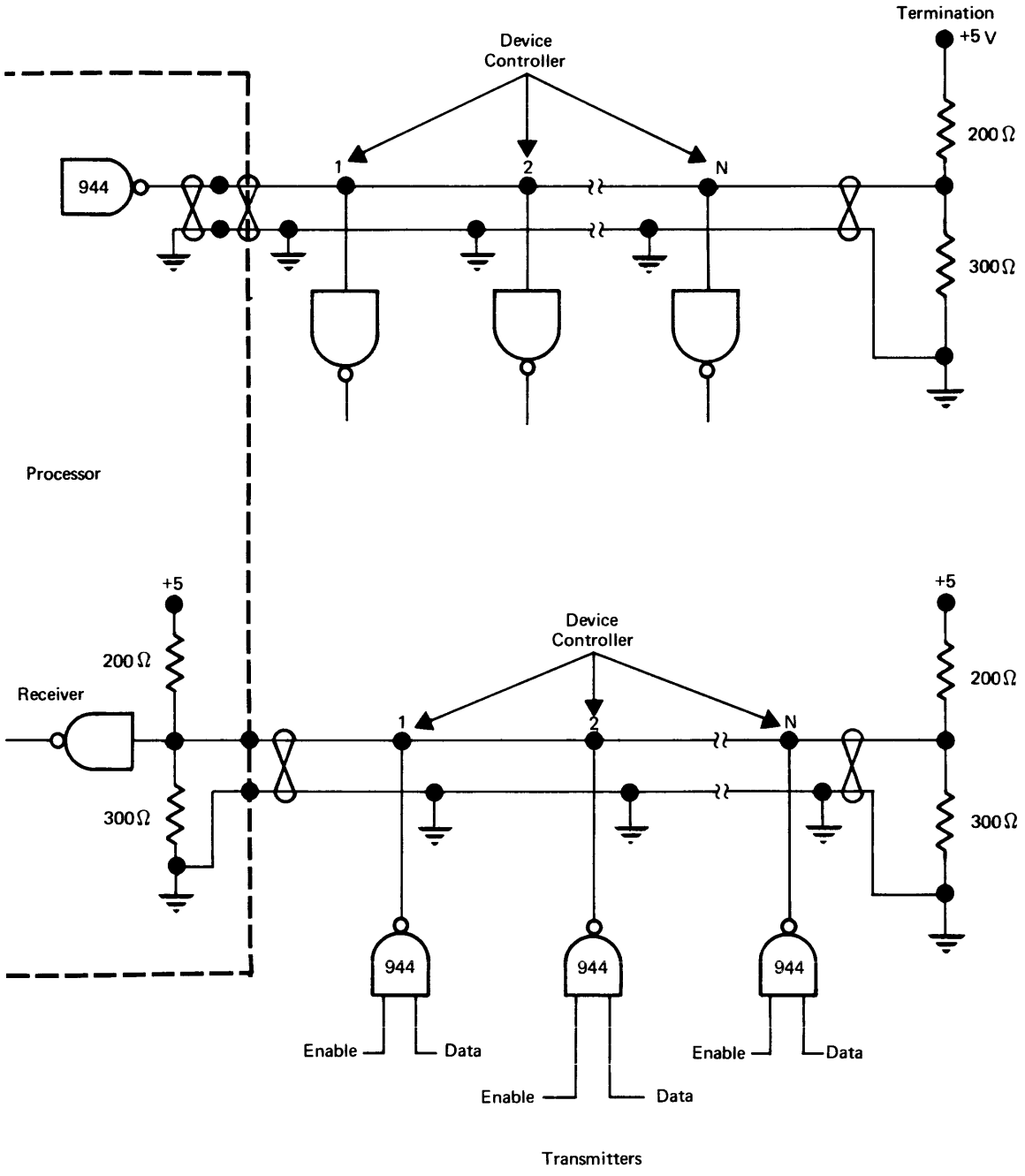


FIGURE 3. BUS LINES

The logic levels on the twisted pairs are:

One – 0 volts
Zero – +3 volts

Output Lines

The nine output data lines originate with the FALSE output of the T register. The output control lines originate with the I/O Control register. If all peripheral devices on the bus are local to the enclosure, and the bus does not leave the enclosure, then the bus is standard logic levels and no DTL drivers and terminations are used. It may be necessary to repower the signals. If the bus leaves the enclosure, an I/O control board is required to provide type 944 DTL output drivers and decoding the control register. The cable length can be up to 30 feet in length and must be terminated at the remote end. Up to 15 receivers can be accommodated. The levels on the twisted pairs are:

One – 0 volts
Zero – +3 volts

CONTROL LINES IN

External Interrupt (EINT/): A peripheral device makes this line low to request an interrupt of the macroprogram. The program must respond with an I/O Acknowledge (mode 5) signal. This line is bit 7 of file register 0 where a 1-bit indicates an external interrupt request.

I/O Reply (ERPY/): A peripheral device makes this line low in response to an I/O operation when closed loop operation is required. This line is bit 5 of file register 0. The standard MICRO 810 I/O procedures do not use this line.

I/O Request (ECIO/): A peripheral device makes this line low in order to request a concurrent data transfer. The program must respond with an I/O Acknowledge (mode 5) signal. This line is bit 3 of file register 0 where a 1-bit indicates a concurrent I/O request.

Device Protect (EDPR/): An external device makes this line low during a data input if it is in a protected state thus allowing it to write into a protected area of memory when the memory protect option is installed.

Priority Return (PRRT/): This line is the return of the priority signal line.

CONTROL LINES OUT

I/O Clock (KOXX/): A 50% duty cycle signal at half of the processor clock rate.

Master Reset (MRES/): A low signal when either the RESET or SAVE switches on the console is depressed.

Control Output (COXX/):	A low signal which specifies that a control byte containing a device number and device order is on the output bus. The device being addressed accepts the byte.
Data Output (DOXX/):	A low signal which specifies that an information byte is on the output bus for the previously addressed external device.
I/O Acknowledge (IOAK/):	A low signal which inputs an I/O Acknowledge byte from the external device requesting an interrupt or concurrent I/O transfer.
Data Input (DIXX/):	A low signal which input an information byte from an addressed external device.
Priority Out (PROT/):	This line is the start of the priority signal line. A ground on this line gives priority to the next device on the line.

PRIORITY

Devices on the byte I/O bus are assigned a priority for control of the external interrupt and I/O request lines. The priority is achieved by a signal line (PROT/ or PRRT/) which links all of the peripheral devices, not necessarily in the same order as the physical wiring of the I/O bus. A ground condition received on the priority-in signal line indicates that a device has priority if it wants to make an interrupt or I/O request. If so a ground is placed on the appropriate request signal line and not on the priority-out line. If the device does not want to make a request it places a ground on the priority-out signal line.

The processor replies to an external interrupt (EINT/) or I/O request (ECIO/) with an I/O Acknowledge which causes the device to identify itself by sending an I/O Acknowledge byte on the input bus.

MICRO 810 BYTE I/O BUS STANDARDS

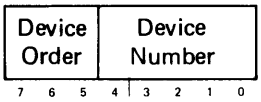
The MICRO 810 Firmware provides macro input/output instructions and a buffered concurrent I/O system. The I/O instructions perform transfers with registers and memory. The concurrent I/O performs block transfers of data which proceed concurrently with, and independent of, the macro instruction sequences being executed by the processor.

BUS MODES

In the MICRO 810 the Byte I/O Bus modes are used as described below.

Control Output

A control byte having the following format is placed on the output bus along with a mode 1 control signal (COXX/) prior to a data transfer and when some non-data transfer action is to be taken by a peripheral device.



The five-bit Device Number addresses one of 32 possible devices on the Byte I/O bus. The three bit Device Order specifies a particular action to be performed or indentifies the type of subsequent data transfer. The addressed device accepts the control byte and remains connected until the data transfer occurs. The non-addressed devices ignore the control byte and subsequent data transfer. The control signal is removed after four clock cycles.

Data Output

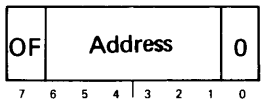
A data byte to be output is placed on the output bus along with the mode 2 control signal (DOXX/). A data byte is normally eight bits, but is expanded to nine bits if the spare memory bit option is available. The data on the bus is accepted by the addressed device and the control signal is removed after four clock cycles.

Space Serial Teletype

This mode is not associated with the Byte I/O bus, but instead controls the output state of the serial teletype interface. When the I/O Control register is in mode 3 current is removed from the output line.

I/O Acknowledge

An I/O Acknowledge byte is input from the device making an External Interrupt or Concurrent I/O Request in response to the mode 5 control signal (IOAK/). The byte has the following format:



The six bit address is normally the five-bit device address with a high order 0-bit. In the case of external interrupts not associated with peripheral devices a six-bit address can be used. The output flag in bit 7 is a 1-bit when the device wants to perform concurrent output and is a 0-bit when it wants to perform concurrent input or is requesting an external interrupt. The processor uses the address in the acknowledge byte to locate the concurrent I/O control address words or interrupt sub-routine address which are located in memory.

Data Input

A data byte to be input is placed on the input bus by the peripheral device in response to a mode 6 control signal (DIXX/). The data byte is normally eight bits, but can be expanded to nine bits if the spare memory bit option is available. The data on the input bus must be copied by some operate class command. The ninth bit of the bus can only be routed to T_8 and cannot be operated on. The control signal is removed after four clock cycles.

CONCURRENT I/O

The concurrent I/O facility performs buffered block transfers of data between an external peripheral device and memory. The maximum total transfer rate is 50,000 bytes per second. Address control for each device is performed by two 16-bit addresses located in core memory. The first address specifies the current memory address and the other specifies the last address of the data block.

The peripheral device is placed in a concurrent input or output mode by a control byte sent to the device. The device requests data transfers by the I/O Request line. When the processor recognizes the request it performs the transfer and increments the current address. When the current address equals the end address +1, the processor sends a control byte to the device to stop the concurrent operation.

Concurrent Data Input Procedures

a. Device wanting to input data to memory and having highest priority grounds the I/O request control line.

b. When the processor's microprogram senses an I/O Request at bit 3 of file register 0 it grounds the I/O Acknowledge.

c. Device sending I/O Request senses I/O Acknowledge and places an I/O Acknowledge byte, with and 0-bit in bit 7, on the input bus.

d. Processor's microprogram inputs acknowledge byte and removes I/O acknowledge signal.

e. Device senses removal of the I/O Acknowledge and removes I/O Request signal.

f. Processor's microprogram grounds data input signal.

g. Device gates input data byte onto input bus.

h. Processor's microprogram inputs data byte, removes data input signal, and stores data in memory at address determined by address control words in memory.

Concurrent Data Output Procedures

a. Device wanting to receive data from memory and having the highest priority grounds the I/O Request control line.

b. When the processor's microprogram senses the I/O request at bit 3 of file register 0 it grounds the I/O Acknowledge.

c. Device sending I/O request senses I/O Acknowledge and places an I/O Acknowledge byte with a 1-bit in bit 7, on the input bus.

d. Processor's microprogram inputs address byte and removes I/O Acknowledge signal.

e. Device senses removal of the I/O Acknowledge and removes I/O Request signal.

f. Processor's microprogram places accessed data on output bus and sends Data Output signal. Memory location of data is determined by address words in memory.

INTERRUPT

The Interrupt facility makes use of a single interrupt line which a priority interrupt channel or an End-of-Block interrupt from an I/O Device may activate. When the processor recognizes the interrupt request (between macro instructions), the interrupting device identifies itself. In core memory, the address of the interrupt handling sub-routine is kept at a fixed address. The device identification, along with a displacement, is used to refer to that fixed address, and then a Return Jump is activated into the sub-routine.

Interrupt Procedures

a. Device wanting to interrupt and having highest priority grounds External Interrupt (EINT/) control line.

b. When the processor's microprogram senses an External Interrupt request at bit 7 of file register 0 it grounds the I/O Acknowledge.

c. Device sending External Interrupt senses I/O Acknowledge and places an I/O Acknowledge byte on the input bus.

d. Processor's microprogram inputs acknowledge byte and removes I/O Acknowledge signal.

e. Device senses removal of I/O Acknowledge and removes External Interrupt and the acknowledge byte.

f. Processor's microprogram uses acknowledge byte to determine interrupting device and processes interrupt accordingly.

5. OPTIONS

Various standard hardware options are available for the MICRO 800 series of machines. These include additions to the basic processor and to the input/output. These options are designed to mount on circuit boards which plug directly into the basic enclosure. Sufficient power is available in the basic power supply to handle a full expanded cabinet. All the processor options are placed on a single circuit board.

In addition to the option hardware, proper firmware must be provided to implement system action and response. This firmware may be designed specially for a given application. Standard firmware for each option described below is provided as part of the MICRO 810 configuration. This firmware can also be used on other configurations as desired.

CENTRAL PROCESSOR OPTIONS

Memory Parity

The memory parity option allows checking of all read operations. The checking operation is automatic and does not require microprogramming. A detected error causes an internal interrupt by setting condition flag bit 4 (Table 1) and places a 1-bit in internal status bit 4 (Table 3). The parity interrupt condition must be sensed by the microprogram and appropriate action taken. The option requires providing an extra memory bit to store the byte parity (even).

Memory Boundary Error

The memory boundary error option is an internal interrupt which detects the addressing of a non-existent memory module. This error causes an internal interrupt by setting condition flag bit 4 (Table 1) and places a 1-bit in internal status bit 5 (Table 3). The boundary error interrupt condition must be sensed by the microprogram and appropriate action taken. A standard interrupt entry procedure is provided in the MICRO 810 configuration.

Memory Protect

The memory protect option provides a guarantee that protected areas of memory cannot be written into by a program residing in an unprotected memory area or by unprotected peripheral devices.

The memory is divided into a maximum of 32 protected areas; the number of bytes in a protected area is a function of the memory size as follows:

Memory Size	Protected Area Size (bytes)
4K	256
8K	256
12K or 16K	512
24K or 32K	1024

The option provides a 32 bit storage register to store the protection state of each of the possible 32 protected areas. This storage is loaded by command 1740 which transfers the state of bit 7 of the T register (T_7) to the protect storage bit corresponding to the area addressed by the M register. A 1-bit indicates that the area is protected. In the MICRO 810 a macro level instruction is provided to perform this operation.

When a protected area violation is detected, the write operation is automatically converted to a read-restore operation, and an internal interrupt is generated by setting condition flag bit 4 (Table 1). A 1-bit is also placed in internal status bit 3 (Table 3).

The protect option guards bytes in protected areas against illegal full cycle write operations as follows:

a. An instruction stored in a non-protected area may not write into a protected area.

b. A peripheral device on the byte I/O channel which is in a non-protected state may not write into a protected area.

c. A peripheral device on the DMA channel which is in a non-protected state may not write into a protected area.

Instructions stored in protected areas and protected byte I/O channel and DMA devices may write into protected areas.

Memory Spare Bit

The spare bit option provides a spare memory bit for special application. This option expands the memory byte length, the T register, and the I/O bus to nine bits. This bit is not handled in the normal data paths except for the memory, T register and I/O bus.

The spare bit in the T register (T_8) is loaded by bit 11 of a Load T microcommand or the Control Group Seven is designated with bit 1 set. The Load T command effects the entire T register while Load Seven Control command effects only T_8.

Operation	Load T	Load Seven Control
Reset T_8	– 11xx	1702
Set T_8	– 19xx	1F02

Real-Time Clock

The real-time clock option provides an internal interrupt at a crystal-controlled timing rate. This may be used at the macro-programming level for a real-time clock. The timing is derived from the processor internal clock which is divided down by some integer number less than 2^{13}, as determined by optional strapping on the option board.

When the timing signal occurs, it provides an internal interrupt by setting condition flag bit 4 and bit 2 of the internal status byte. The timing signal internal interrupt may be disabled and enabled by commands 1710 and 1720 respectively. The microprogram must detect the internal interrupt and take appropriate action. Special real-time clock interrupt handling firmware is provided in the MICRO 810 configuration.

Power-Fail/Automatic Restart

The power-fail and automatic restart option provides the following:

a. An internal interrupt and a 1-bit on internal status bit 7 upon detection of loss of primary power.

b. A machine reset when the computer is halted after loss of primary power.

c. A machine reset for 200 milliseconds after power is applied.

d. Automatic switch to Run mode after the power-on reset period.

e. Power fail interrupt immediately after automatic switch to Run mode.

A power-fail interrupt detected while the machine is in the Run mode can be used to cause the machine registers to be stored and to bring the processor to a halt. The automatic machine reset that follows the halt and the one following power-on prevents any spurious operations in the core memory. At power-on, the machine reset clears the L register causing the machine to start at read only storage location 0. The power-fail interrupt which occurs at this time can be detected and treated as a restart interrupt to cause a restoring of the machine registers. Standard power fail/automatic restart interrupt firmware is provided in the MICRO 810 configuration.

6. OPERATOR CONTROLS

CONSOLES

Three control console options are available: system console, operator console, and basic console. These consoles differ in their number of displays and controls. This range of consoles permits the user to tailor the cost to meet the control and display capability required for a particular application. The control console is shown in Figure 4.

SYSTEM CONSOLE

The system console provides complete control and display facilities. It is primarily used for maintenance, system and firmware checkout. This console provides for display of the MICRO 800 registers in addition to the functions of the operator console. The features include:

- Run and Halt indicators
- Display of A-bus
- Display of M, N, and L registers
- Display of output of read only storage
- Four sense switches
- Six control switches including: Run, Step, Interrupt, Clock Reset, and Save.
- Manual Command execution
- Power On/Off

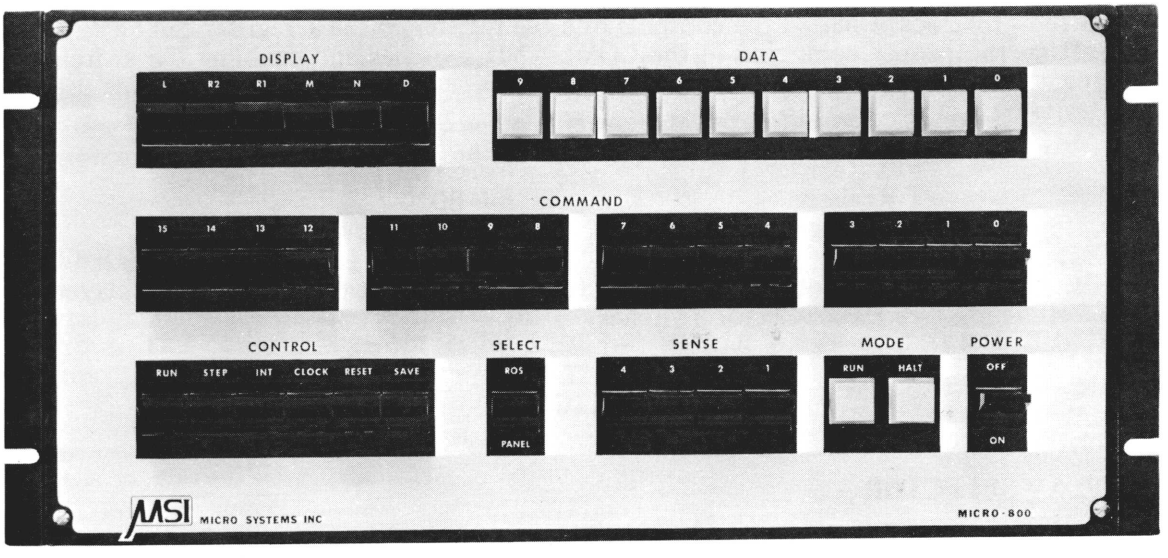


FIGURE 4. CONTROL CONSOLE

OPERATOR CONSOLE

The operator console provides the same features as the system console except that display of the M, N and L registers and the output of the read only storage is not provided. The data display is at the A bus.

BASIC CONSOLE

The basic console provides minimal control capability and is designed for dedicated system applications where operator control is not required. The features include:

- Run and Halt indicators
- Four sense switches
- Six control switches including: Run, Step, Interrupt, Clock, Reset, and Save.
- Power On/Off

DISPLAYS

RUN LAMP

The run lamp is illuminated when the processor is running.

HALT LAMP

The halt lamp is illuminated when the power is on and the process is not running.

DATA DISPLAY

On the operator console eight lamps display the data which is on the A bus of the processor. When the processor is halted the contents of a file register or the T register can be displayed by setting the proper command in the COMMAND switches and enabling the switches by placing the SELECT switch in the PANEL position. The hexadecimal commands used for display are:

File Register f	– Cf00
T Register	– B020
Link Register	– B080

On the system console a set of Display Selector switches select the data to be displayed on a set of 10 lamps. (see Data Selector Switches)

SWITCHES

DISPLAY SELECTOR

These seven interlocked switches select the register or bus to be displayed on the system console. The displays which can be selected are:, L register, M register, N register, eight high order bits of the read-only-storage output, eight low order bits of the read-only-storage and the A-bus. When the machine is halted the output of the read-only-storage is the same as the contents of the R register, and is the next command to be executed.

COMMAND

These 16 alternate action switches are substituted for the read only storage on the system and operator consoles when the SELECT switch is in the PANEL position. Depressing the CLOCK switch causes the command set on the switches to be executed. The command may also be executed repeatedly by depressing the RUN switch. These switches are used to gate registers to the A bus display and for entering data into the file and registers.

SELECT

This alternate action switch selects the console panel command switches (PANEL) or the read only storage (ROS) as the command to be executed next. This switch is not available on the basic console.

SENSE

The four alternate action sense switches are available on all consoles. The state of these switches may be transferred to a file register or machine register by the Control command. These switches may be used to provide manual control of micro level and macro level programs.

RUN

This momentary contact switch places the processor in the run mode causing it to execute microcommands.

STEP

This momentary contact switch places the processor in the run mode and as long as the switch is depressed causes an internal interrupt. The halt internal interrupt is bit 7 of the internal status. This switch is normally microprogrammed to cause a processor halt. Since the processor is forced to run when the switch is depressed, the machine can be microprogrammed to cause a single macro instruction to be executed.

INTERRUPT

This momentary contact switch places the processor in the run mode and causes an internal interrupt. The console interrupt is bit 0 of the internal status. This switch is normally microprogrammed to cause a console interrupt.

CLOCK

This momentary contact switch causes the processor to execute a single microcommand. If the processor is running at the time the switch is depressed the processor will come to a forced halt.

RESET

This momentary contact switch halts the processor and clears the L register, I/O control register and other control flip-flops. The reset is made available to I/O devices.

SAVE

This alternate action switch is the same as the RESET switch but can be set on providing a continuous reset. If this switch is on at the time the power is turned on or off the contents of the memory will not be lost or altered.

APPENDIXES

APPENDIX A

SYMBOLIC LANGUAGE

The source language is a sequence of symbolic instructions, called statements. Each statement is written on a single line and may consist of from one to four entries: a name field, an operation field, and operand field, and a comments field.

Name Field

The name field entry is a symbol composed of from one to six characters. The first character of a symbol is alphabetic, subsequent characters may be alphabetic, numeric, or a period. A name entry is usually optional. When an asterisk, *, appears as the first character the remainder of the line is considered as comment.

Operation Field

The operation field entry is a mnemonic operation code specifying the machine command as an assembly pseudo-instruction. The field begins in column 8. All machine command mnemonics are two characters except those of the operate class where no destination register is designated. The operate class commands have a basic single letter mnemonic. If the result of the operation is to be sent to a machine register then the register identifier character, r, is appended as the second character of the mnemonic. Register identifier characters are shown below. An asterisk, *, is appended to the mnemonic if the result of the operation is not to be placed in the designated file register. Some of the mnemonics accepted by the assembler are commonly used forms of other commands.

Register Designator	r	Register
0		None
1	T	T Register
2	M	M Register
3	N	N Register
4	L	L Register addresses: 000-0FF and 200-2FF
5	K	L Register addresses: 100-1FF and 300-3FF
6	U	U Register
7	S	U Register ORed in command (Except for K command)

Operand Field

The operand field entries provide the file register designators, literals, and option bits for the machine commands. It normally starts in column 14 and is terminated by the first blank column. One or more operands, separated by commas may be written, depending on the needs of the command. All entries in the operand field, except the single character option bit identifiers for the operate class commands, are expressions. An expression is a symbol, decimal number, or hexadecimal number, or a combination of these terms made by + and – operators.

The following single character option identifiers, designators and literals may appear in the operand field.

L	– Link Control
I	– Add one or insert one on Shift
D	– Decrement one
T	– T register operand
F	– Complement of T register operand
H	– Half cycle memory operation (otherwise full cycle)
R	– Right shift (otherwise left shift)
C	– Set condition flags
f	– File register designator (0-15)
c	– Option code (0-15)
n	– Literal (8, 9, or 10 bit)

Comment Field

The comment field normally starts in column 30 but may start immediately after the operand field. It is terminated with column 72. Any symbols including blanks may appear in this field.

APPENDIX B

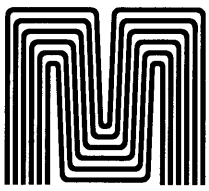
MICROCOMMANDS

Command	Mnemonic	Operand Field
Load T	LT	n
Load M	LM	n
Load N	LN	n
Load U	LU	n
Load Zero Control	LZ	n
Load Seven Control	LS	n
Jump	JP	n
Load File	LF	f,n
Add to File	AF	f,n
Test If Zero	TZ	f,n
Test If Not Zero	TN	f,n
Compare	CP	f,n
Execute	Er*	f,c
Control	Kr*	f,c
Add	Ar*	f,L,I,T,C
Increment	Ir*	f,L,C
Subtract	Sr*	f,L,D,T,C
Decrement	Dr*	f,L,C
Copy	Cr*	f,L,I,T,C
Read	Rr*	f,L,I,D,H
Write	Wr*	f,L,I,D,H
Logical OR	Or*	f,L,F,T,C
Move	Mr*	f,L,C
Exclusive-OR	Xr*	f,L,F,T,C
Logical AND	Nr*	f,L,F,T,C
Shift	Hr*	f,L,I,R,C

APPENDIX C

ALPHABETIC LIST OF COMMANDS

Command	Mnemonic	Operation Code	Page
AND	N	Ef	20
Add	A	8f	16
Add To File	AF	3f	13
Compare	CP	6f	14
Control	K	7f	14
Copy	C	Bf	18
Exclusive – OR	X	Df	19
Execute	E	0	21
Jump	JP	14,15,1C,1D	13
Load File	LF	2f	13
Load T	LT	11,19	11
Load M	LM	12	11
Load N	LN	13	11
Load U	LU	16	12
Load Seven Control	LS	17	12
Load Zero Control	LZ	10	12
OR	O	Cf	18
Read	R	Af	17
Shift	H	Ff	20
Subtract	S	9f	16
Test if Zero	TZ	4f	14
Test if Not Zero	TN	5f	14
Write	W	Af	17



Micro Systems Inc.

COMMENT AND EVALUATION SHEET

MICRO 800 COMPUTER
Reference Manual

Pub. No. 69–3–0800–001 June 1969

YOUR EVALUATION OF THIS MANUAL WILL BE WELCOMED BY MICRO SYSTEMS INC. ANY ERRORS, SUGGESTED ADDITIONS OR DELETIONS OR GENERAL COMMENTS MAY BE MADE BELOW. PLEASE INCLUDE PAGE NUMBER REFERENCE.

FROM NAME: _____

BUSINESS
ADDRESS: _____

NO POSTAGE STAMP NECESSARY IF MAILED IN U.S.A.

FOLD ON DOTTED LINES AND STAPLE

STAPLE STAPLE

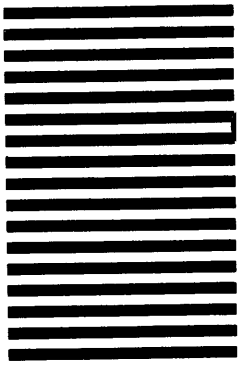
FOLD FOLD

First Class
Permit No. 1972
Santa Ana
California 92711

BUSINESS REPLY MAIL
NO POSTAGE NECESSARY IF MAILED IN THE U.S.A.

Postage Will Be Paid By

MICRO SYSTEMS INC.
644 East Young Street
Santa Ana, California 92705



FOLD FOLD

STAPLE STAPLE

MicroSystems Inc.

644 East Young Street
Santa Ana, California 92705
Telephone: (714) 540-6730
TWX: 910-595-1764