Microdata

3200 Computer

GENERAL DESCRIPTION

The Microdata 3200 is a modular microprogrammable, 16-bit digital computer which may be used to emulate a wide range of powerful special-purpose and general-purpose digital computer systems. It employes a 32-bit microinstruction, a 135-nanosecond microinstruction execution cycle, and provides for up to 4K of microinstruction control memory. The main memory and I/O controllers interface to the processor on a common asynchronous bus (the monobus) which provides a 16-bit data path and addressing to 256K bytes. The 300 nanosecond memory modules utilize MOS storage elements and provide 4K or 8K 16-bit words.

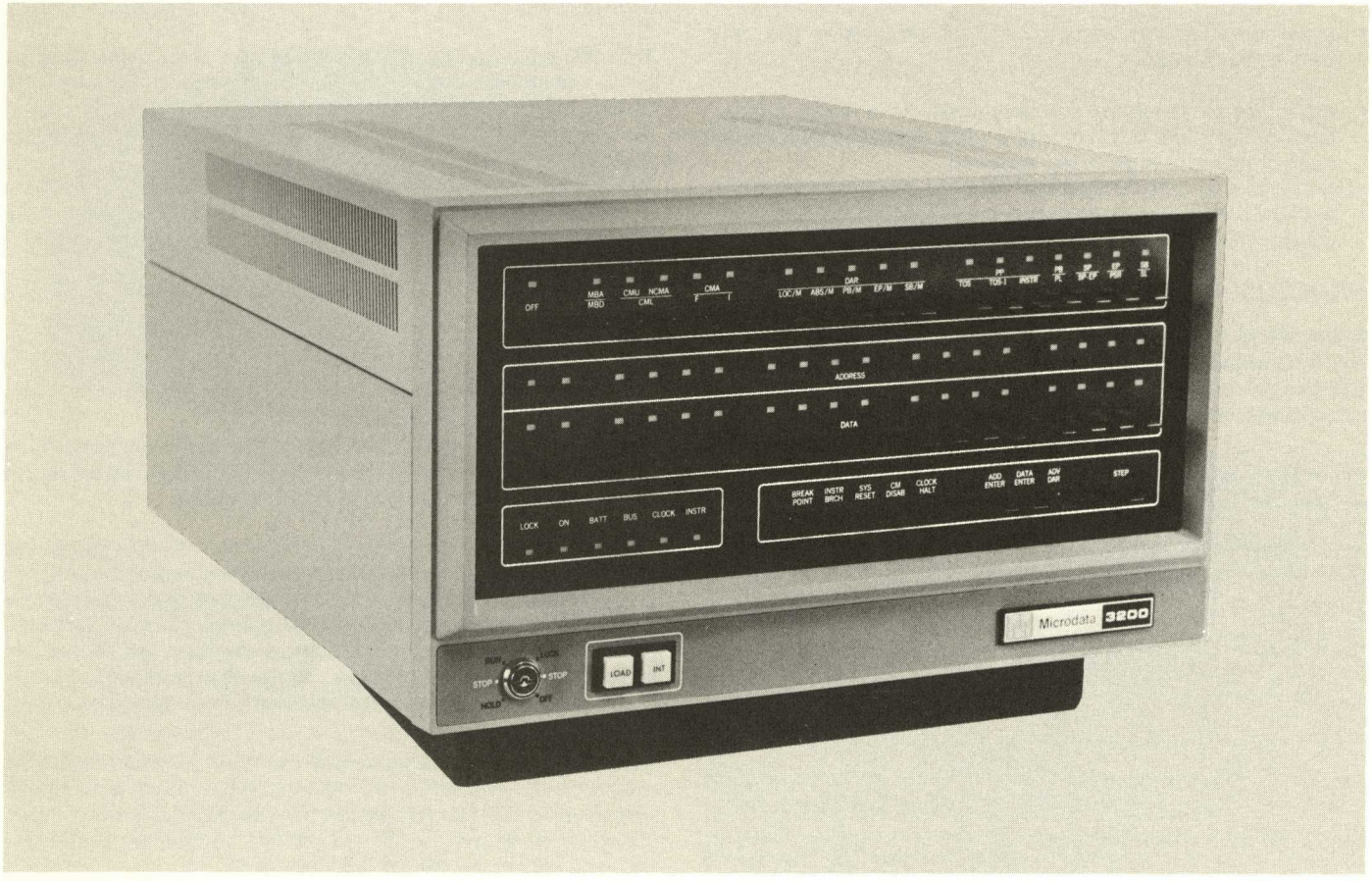
Central to the 3200 system organization is the *Monobus*, an asynchronous high speed system bus which provides for easy configuration of almost any system. All transfers between processors, memories, and input/output devices is via this high speed data path. Since the monobus is printed on the system backplane, modules may be added or deleted from the system by plugging and unplugging them from the chassis.

The 3200 microprocessor can be applied directly to a system problem by programming at the microlevel. This produces a very high performance customized processor. Or it may be microprogrammed to emulate a macro level computer, allowing the use of software that is already written, debugged, and documented. In this case software instructions are fetched from main memory and executed by micro level routines stored in the control memory. In a similar manner, the 3200 can be applied to create an entirely new software level architecture which can then be tailored to a particular class of applications.

APPLICATION

The 3200 is an extremely general-purpose base for microprogramming a wide range of software level computer architectures. Its high speed, wide 16-bit word length, and powerful 32-bit microinstruction result in high performance software level machines. For example, the Microdata 821 has been microprogrammed on the 3200 to yield a 10-to-1 performance improvement. This *emulation* of the 821 on the 3200 is referred to as the Microdata 3230 and is available as a standard Microdata product.

An important feature of the 3200 is the logic which implements a high speed push-down stack within the register file. This feature is exploited in another standard Microdata software level computer microprogrammed on the 3200, the Microdata 32/S. The 32/S is an emulation of a unique push-down stack architecture which has been designed to be



optimized for executing programs written in a high-level language. The Microdate Programming Language, (MPL), has been developed for the 32/S. The MPL compiler produces 32/S programs which are as efficient as the machine-language programs which can be obtained with an assembler on a conventional architecture computer.

For each particular type of computer application, a set of microprogram routines is written to make the 3200 microlevel computer behave like the software level computer which is optimum for the end use intended. In essence there is a microprogram routine for each software level instruction operation code (e.g., Add to Accumulator), for each type of addressing mode (e.g., direct addressing with indexing), and for each type of interrupt (e.g., real-time clock). There may also be a microprogram routine to implement the sequence of operations on the input/output bus. In practice, the standard programming technique of common subroutines is used to minimize the amount of control memory required to program the software level machine. This microprogram is referred to as the computer's *firmware.*

New firmware may be debugged by employing a read/write control memory (i.e., one implemented with read/write memory). Checkout of new software level computers proceeds much more quickly than it would with equivalent *hard-wired* machines.

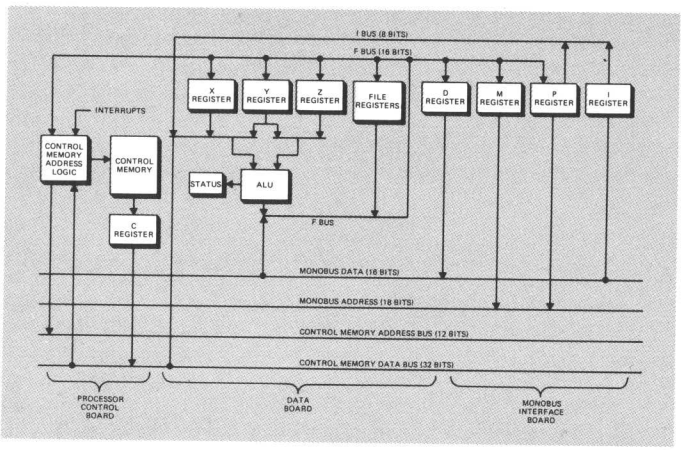
In addition to software programmable computer systems, the 3200 can be used to emulate special-purpose computers and controllers. In this case the main memory may be used to store data and variables, but all processing is controlled exclusively by the microprogram in the control memory.

In any application, the microprogrammable 3200 offers three advantages over the development of new hard-wired software level computer systems.

- lower development costs, as a microprogram is the only item to be developed
- capability to design in extremely powerful software instructions at very low cost, as only a small amount of additional control memory is generally required
- availability of proven, high-production, standard Microdata chassis, main memory, I/O controller and power supply

PROCESSOR ORGANIZATION

A simplified block diagram of the 3200 processor is shown in the following illustration. The logic is implemented on three boards, as indicated at the bottom of the diagram, and interconnected via six main buses in the backplane board.



The Processor Control Board holds the first 2K words of control memory, the 32-bit data register (C) for this memory and the logic for generating the control memory address. This logic receives inputs from the F bus, from fields of the current control memory word, and from both external and internal interrupts, and generates the address for both the control memory on this board and on optional additional control memory boards. The control memory data is bused with data from these additional boards. The switches on the maintenance control panel may also be used to supply microinstructions.

The Data Board contains three 16-bit working registers, X, Y and Z, which receive inputs from the F bus, and drive the 16-bit ALU. The ALU outputs data to the F bus, and result status to the Status Register. The 32 file registers are loaded from, and read out to the F bus. Data from the Monobus Data Bus can also be routed directly onto the F bus.

The Monobus Interface Board contains the 16-bit Monobus Data Register (D), the 18-bit Monobus Address Register (M), the 18-bit Program Pointer Register (P), and the 16-bit Instruction Register (I). The I Register is automatically loaded from the Monobus Data Bus whenever the P Register is loaded or incremented to an even byte address. A subsidiary 8-bit register (not shown) holds the instruction byte currently being processed by the microprogram.

Both main memory modules and I/O controllers attach to the Monobus Data Bus and Monobus Address Bus. The combination of monobus address bits which indicate that the address is within the bank of 4K word addresses reserved for I/O controllers is decoded within the processor and supplied on the backplane to simplify the address decoding in the controllers. Although control memory is normally read via the control memory address and data buses, it may be accessed via the system monobus. This facility allows writing of read/write control memory and verifying of any type of control memory.

The 32 bit microinstruction is divided into eight encoded fields which generally specify the arithmetic function, the sources, the destination, the control memory addressing mode, the control memory address constant, the branch conditions, the general register addressing, and a constant for the microinstruction. Control memory is addressable to 4K locations and is available in various size modules of read only, programmable read only, and read/write storage which can be mixed in a single system.

MODULARITY

The emphasis in the 3200 design has been on modularity providing a wide range of capability by simply selecting the desired configuration of off-the-shelf modules.

The 3200 CPU is implemented on three circuit boards; the Data Board, the Monobus Interface Board and the Processor Control Board. Additional control memory boards are available to provide additional control memory of either the read-only or read/write type. More than one CPU can be employed to implement multi-processor configurations.

Each MOS main memory board contains up to 8K words of memory. The first 4K words are contained on the board itself, and another 4K words are contained on a secondary board which is plugged into this board. The combined module fits into one connector slot of the backplane.

Each standard I/O controller is contained on one circuit board. However, multi-board controllers can be accommodated, with inter-connections provided with a flex-cable between the tops of these boards.

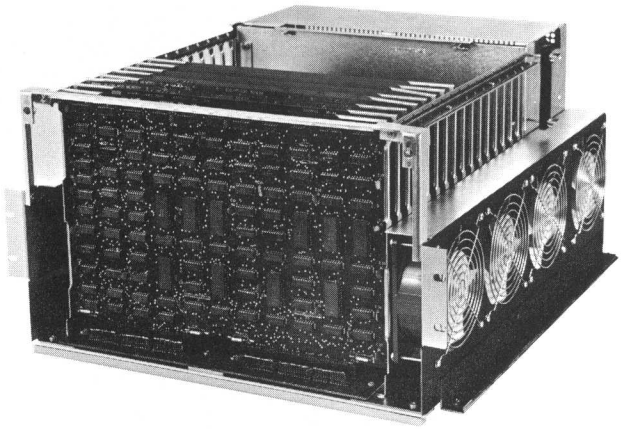
PACKAGING

The 3200 chassis has been designed so that any board can be serviced without the use of an extender board, and so that maximum cooling is provided even while servicing the unit. Printed circuit boards, 14 inches wide by 9 inches high, are plugged vertically into a printed circuit backplane board which serves as the floor of the chassis. The backplane provides 16 connector positions. An integral power supply plugs into the last connector at the rear of the backplane. The chassis is mounted on slides for servicing in a rack configuration.

The maintenance panel assembly contains a printed circuit board which holds all of its lights and switches. This board is connected by flex cable to a logic board which plugs into the backplane.

Four fans, mounted along one side, provide forced air cooling to the circuit boards and the power supply. Ribbon-type I/O cables plug into headers mounted along the upper side of the cards; they exit to the rear of the chassis along the channel over the fans, and along a similar channel on the other side of the chassis.

Any board in the computer may be plugged into any connector in the backplane. The maintenance or basic control panel is easily removed and hung to one side, permitting total access to the board inserted in the first backplane connector. As a result, any board may be serviced by plugging it into the first connector, eliminating the need for troublesome extender boards.



MAIN MEMORY

A main memory module uses 128 1K MOS memory chips, of the 6002-type, to provide 8K words of storage. The module contains a 4-bit selector switch to permit it to be manually set to respond to the desired 8K word address bank. The memory is addressable to the byte level. The memory module contains its own timing logic, including that required for automatic refresh in response from signals supplied by the power supply. A block of 32 addresses in each chip are refreshed simultaneously every 30 microseconds during normal computer operation. To reduce battery drain during standby, all addresses are refreshed in a burst every two milliseconds.

POWER SUPPLY

The power supply provides the conventional +5 volts required by the logic, and +12 and −12 volts required by I/O controllers and core memory. In addition, it supplies the +21 volts required by the MOS memory. This latter voltage can be backed up by a gel-cell battery to maintain data in the MOS memory in case of ac line drop-out for more than half-a-dozen cycles. In addition, the key-lock on the control panel provides a position for turning off all channels of the supply except the +21. This standby power mode is used for periods when the computer is not used.

I/O CONTROLLER MODULES

Each standard I/O controller module consists of a single circuit board which plugs into the backplane. Standard I/O controllers include those for disc files, industry-standard magnetic tape drives, card reader, line printer, paper tape reader and punch, and serial devices such as teletypes, modems, and CRTs.

CONSOLE MODULES

Two control console options are available with the Microdata 3200; a maintenance console and a basic console.

The maintenance console will display eighteen different pairs of registers or data paths and is an exceptional tool for debugging hardware, firmware, or software. Several of the displays are firmware controlled allowing the panel functions to be tailored to any class of application.

The basic console provides only the controls needed for system operation. It includes an operator interrupt and an automatic program load feature and is adequate for most system applications. Both consoles are plug-in modules and are fully interchangeable.

ADVANTAGES

Flexibility

Microprogramming permits tailoring of processor architecture to individual system needs.

Modularity

Monobus system organization allows easy, economical expansion using standard system modules in any combination.

Expandability

Extra space and power in the basic enclosure permits growth from a minimum to a fully expanded configuration. User designed interfaces can be easily installed in the computer chassis.

Economy

Low price for both the basic and expanded configurations. Simple interfacing and expansion minimize overall system costs.

Utility

Many designed in features make the 3200 easy to install, program, operate, and maintain.

SPECIFICATIONS

Microprocessor Module

Arithmetic ..... Sixteen bit, binary, fixed point; separate firmware and software carry indicators, negative, zero and overflow indicators; byte operations with byte level indicator setting.

Word Length ..... Sixteen bits; byte or word transfers, multiple precision operations are supported.

Processor Registers ..... 32 general purpose 16-bit file registers, three working registers, software level program pointer and instruction registers, memory address and data registers, microcommand and address storage registers, interrupt register, shift counter.

CPU Operation ..... Controlled by execution of microcommand sequence stored in high speed control memory.

Microcommand Execution Time ..... 135 nanoseconds per step.

Microcommand Format ..... Partially encoded – 32-bit microcommand, divided into eight 4 bit fields, some conditional encoding of fields; each command is a conditional jump with two alternate destinations; microcommands need not be sequentially accessed.

Software Fetch ..... Software level instruction look-ahead keeps next software instruction queued in advance; next operation branch performs 48 way branch based on 16 internal and external interrupt conditions, four bits of next software instruction and a jump condition.

System Console ..... Full system maintenance panel or basic operators panel.

Control Memory

Word Length ..... 32 bits

Speed ..... 60 nanoseconds access 135 nanoseconds cycle

Types ..... Mask programmed read only, electrically programmed read only, read/write control memories.

Size ..... Maximum size – 4096 32-bit words; read only memories expandable in 512 word increments, read/write expandable in 256 word increments; up to 2048 words read only memory packaged on processor control board, up to 4096 words of read only or 512 words of read/write memory packaged on control memory expansion board.

Main Memory

Type ..... Semiconductor, 6002 type MOS storage array.

Speed ..... 300 nanoseconds write cycle, 400 nanosecond read cycle with 300 nanosecond access.

Word Length ..... Sixteen bits

Memory Size ..... Expandable from 4K to 128K words in 4K increments.

Module Sizes ..... 4K and 8K words.

Power Fail Protect ..... Standard battery option maintains 16K words for two weeks at room temperature, longer protection available with paralleled battery options.

Memory Ports ..... Monobus organization allows any number of processors to share memory.

Packaging/Environment

General ..... Microprocessor contained on three printed circuit boards, main memory, expansion control memory, console, I/O controllers on one board per module.

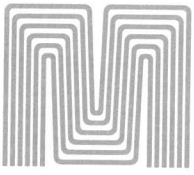
Monobus ..... Contained on printed circuit backplane; modules added by plugging into any card slot; no central bus control, speed limited only by sending and receiving modules.

Chassis Types ..... Rack and table top units, console and expansion chassis, console or decorative panel snaps on front; 16 card slots with side to side forced air cooling, power supply in last card slot.

Chassis Dimensions ..... Chassis – 10.5 inches high, 19 inches wide, 21 inches deep.

Power ..... Requirements – 115/230 Vac ± 10%, 47 to 63 Hz average configuration less than 500 watts; output capacity – 35 amps at –12 vdc, 3 amps at +21 vdc.

Operating Environment ..... 0 to 50°C, 0 to 95% relative humidity (without condensation).



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