Microdata

Micro 400 Computer

GENERAL DESCRIPTION

The Micro 400 is a low cost, high performance, general purpose computer designed to fill the gap between conventional minicomputers and special purpose digital hardware. Applications heretofore denied the use of a computer because of high cost can now realize the advantages of a fully programmable processor. With powerful computing ability, a wide range of peripherals and complete support software, the Micro 400 is truly a systems processor, while its totally modular construction and ease of system integration make it the perfect computer for OEM applications.

Through the use of MSI circuitry and printed circuit packaging techniques, the entire processing unit is contained on a single circuit board, as is the core memory (up to 4096 bytes). All system components are interconnected using a unique MICRObus concept consisting of a single flat cable instead of expensive wired backplanes. This single cable "daisychains" to all system components for simplicity and economy of system expansion.

The modular design of the Micro 400 means added economy for the OEM user. The Micro 400 central processor, memory modules, peripheral interfaces and control console can be purchased separately on an as-required basis. Thus, the customer may buy only what is actually needed for his specific application.

The net result of these packaging/price/performance breakthroughs is a general purpose, programmable computer at a price which allows use of the Micro 400 as a digital controller or true systems computer, available in a form tailored to the needs of the OEM customer.

SYSTEM FEATURES

Standard

- Unique MICRObus Structure
- Multi-Accumulator Arithmetic
- 118 Program Instructions
- Direct and Indexed Addressing
- Memory Directly Addressable to 4096 Bytes
- Two's Complement Arithmetic
- Local/Remotable Operator's Console
- Hardware Index Register
- Priority Interrupt (one level)

Optional

- Programmed I/O
- Base Register Addressing to 65K Bytes
- Additional Hardware Index Register
- Automatic I/O (Direct Memory Access)
- Power Fail/Restart
- Real Time Clock
- Hardware Bootstrap Loader
- Full Line of Peripheral and System Interfaces
- Priority Interrupts (8 levels)

ORGANIZATION

Central Processor

The Micro 400 is organized around the MICRObus and consists of five 8-bit registers, two 12-bit registers and one 16-bit register. All information transferred within the processor between registers and memory is transmitted bit-parallel on the MICRObus. The data on this bus are at all times under control of the central processor control logic. When the contents of a register (or memory) are placed on the bus, the data are presented to the inputs of all other registers and the memory logic. The control unit then strobes the data into the proper destination.

This organization permits high data throughput and minimum time between successive bus transfers, and makes possible the cost saving MICRObus concept.

Core Memory

The Micro 400 core memory is modular in 1024-byte and 4096-byte (8-bit) increments, and each module contains its own data and address registers. The central processor enclosure may contain up to two memory modules of 1K or 4K bytes each. The Micro 400 memory size can be expanded by adding memory modules up to the full 65K byte maximum. Expansion enclosures are available to house the additional modules.

Accessing of core memory is accomplished under programmed control or, as an option, automatically using the Direct Memory Access channel. The standard Micro 400 with index register permits direct addressing of all memory in a 4096-byte page and indexed addressing to the maximum 65K memory size. Programs are executed within 4096-byte pages which may be located in the lower 8K bytes of core memory.

With the optional Base Register Module, the 4K program execution pages may be located anywhere within 65K bytes, and a second index register is available to the programmer.

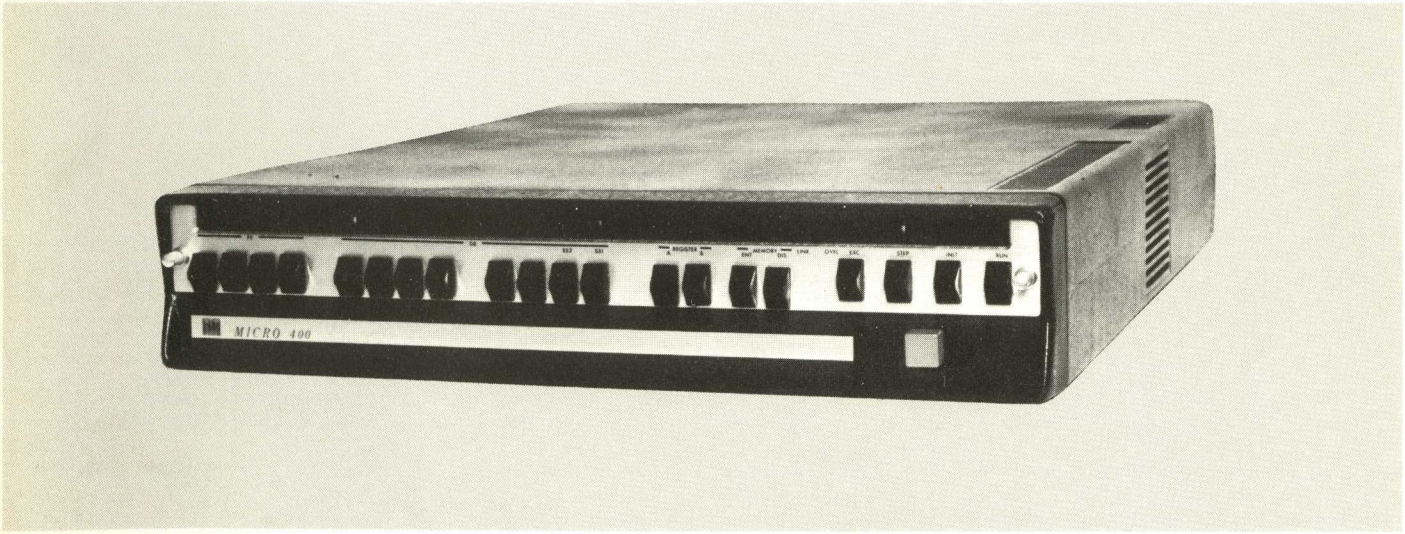


Figure 1. Micro 400 General Purpose Computer

Interrupts

The basic Micro 400 Computer contains a single, common interrupt request line which may be shared in parallel by the Real Time Clock option and several peripheral device controllers. Each device on the interrupt line has its own priority assignment and a unique interrupt address.

A priority interrupt option may be added which provides eight individual interrupt lines. The Power Fail/Restart option has its own interrupt lines.

Central Processor Options

Direct Memory Access – The maximum rate for data transfers between external devices and core memory is approximately 77,000 bytes per second when the transfers are executed under program control. To allow more efficient use of the Micro 400 with high speed external devices, a Direct Memory Access (DMA) option is available. DMA is a direct channel to memory through which data may be transferred automatically using one processor cycle (1.6 microseconds) per data byte. This allows transfers at up to 625,000 bytes per second.

At data rates lower than 625,000 bytes per second, the DMA channel frees the processor to execute program instructions between DMA byte transfers.

Power Fail/Restart – The purpose of the Power Fail/Restart (PF/R) option is to prevent loss of volatile program data and computer operating status in the event of a primary power failure or shutdown. When power returns, the option causes the computer to return to the operating condition which existed at the time of the power down. These actions occur in response to "save" and "restore" subroutines initiated by the PF/R option.

Real Time Clock – To permit event timing and interruption of the computer at known time periods for program sequencing, a Real Time Clock (RTC) option is available for the Micro 400.

The Real Time Clock option utilizes an internal or user supplied timing signal to operate a timing counter and to generate real time interrupts. The RTC interrupt address would normally point to a user routine to perform the desired real time activities.

Base Register Module – The basic Micro 400 Computer contains an index register which allows indexed addressing to 65K bytes of memory. The optional Base Register Module contains an additional 16-bit index register and two 16-bit base registers. The index register provides additional indexing capabilities to 65K bytes of memory. The base registers provide an offset to the directly addressable 4K page which allows the user to execute and relocate programs within 65K bytes of memory. Forty-nine additional instructions are permitted with this option to facilitate use of the base and index registers.

Hardware Bootstrap Loader – The Hardware Bootstrap Loader is designed to eliminate the time and effort involved in manually loading the Bootstrap routine via the Micro 400 control panel. This option automatically loads the Bootstrap program from an internal read-only memory and executes the Bootstrap to load the Binary Loader routine from either a teletype paper tape reader or high speed paper tape reader (selectable via a sense switch).

The procedure for loading the Binary Loader using the Hardware Bootstrap option is simple and consists of the following steps:

- Position the Binary Loader tape on the paper tape reader.
- With the Micro 400 in the STEP mode, press the INITIALIZE switch.
- Press the BOOTSTRAP switch.
- The tape will load automatically.

CONTROL CONSOLE

The Micro 400 operator's control console was designed with the OEM user in mind. The console may be mounted on the computer enclosure (if used) or remotely located up to two feet from the processor and memory electronics. Special cables are available for this purpose.

The Micro 400 may be used without the operator's console in many cases such as digital controller applications.

INPUT/OUTPUT SYSTEM

The Micro 400 communicates with peripheral devices over a parallel I/O bus. Information exchanges with these devices are normally synchronized by peripheral device controllers.

To permit use of the peripheral devices and controllers available for the Micro 400 (except TTY or modem controllers which plug directly into the central processor), a set of input/output drivers are utilized. This standard feature of the Micro 400 buffers the internal data and control lines and presents them to the controllers in the form of an I/O bus.

A complete set of data transfer and sense commands are provided to accomplish programmed transfers as well as the DMA option for automatic data exchanges. The optional priority interrupt system may also be utilized to provide more efficient I/O operations by eliminating time consuming sense operations.

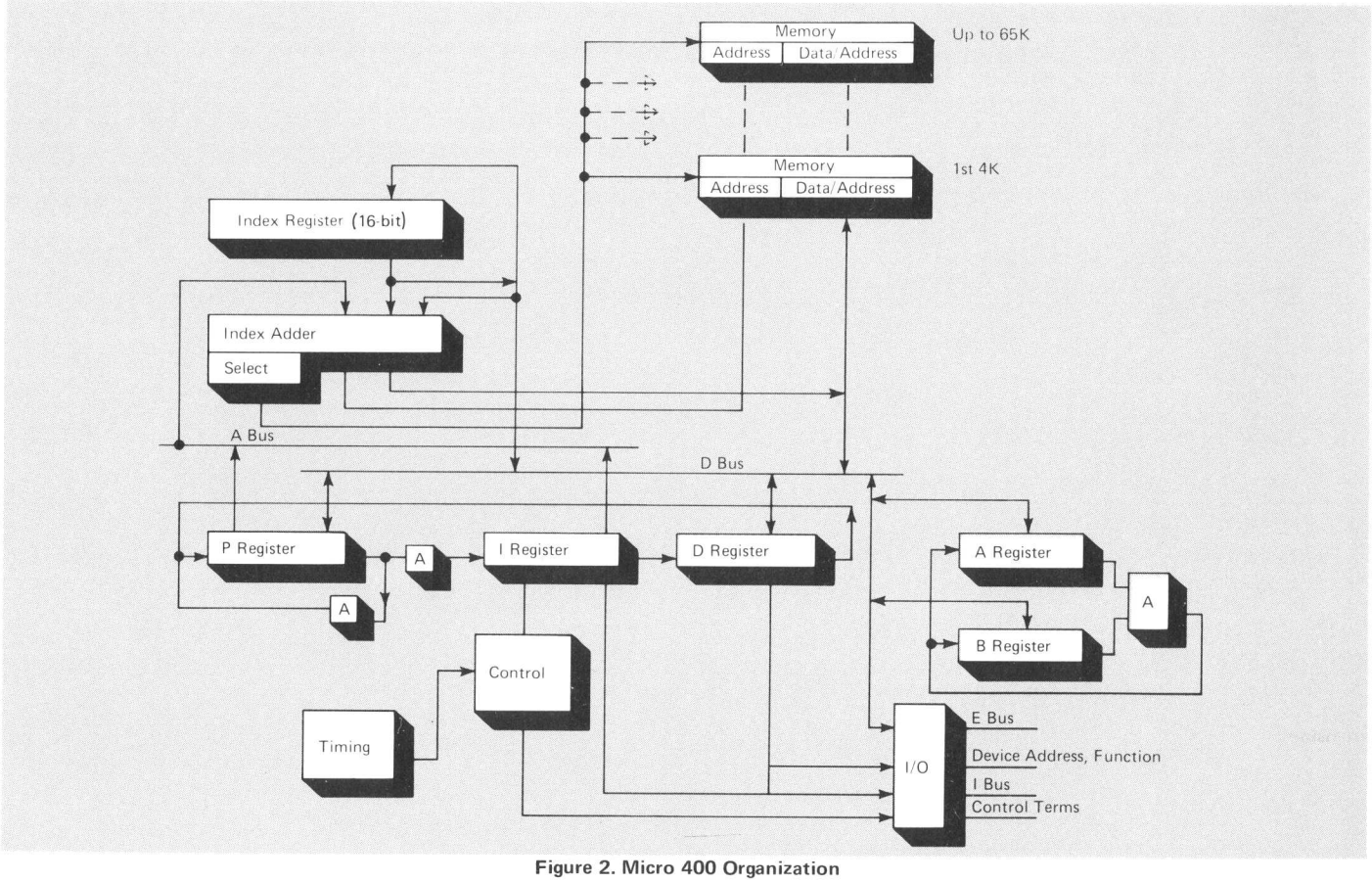


Figure 2. Micro 400 Organization

CONDENSED SPECIFICATIONS

General

A general purpose digital computer designed for controller, control system, data collection, communications, data terminal and stand alone applications.

Memory

Magnetic core, 8-bit word length, 1.6 microseconds full cycle, 400 nanoseconds access. Expandable from 1024 to 65,536 bytes. Each memory module contains data and address registers and 1K or 4K bytes of core memory.

Byte Length

8 bits.

Addressing

Direct to 4096 bytes
Indexed to 65,536 bytes
Base register addressing to 65,536 bytes (optional)

Instructions

118 standard instructions, 49 optional:

Type	Execution Time (cycles)
Load/Store	3
Arithmetic/Logical	1
Memory Modify/Skip	3-4
Register Transfer	1
Jump/Jump Mark	2-4
Skip	2-3
Control	1
Input/Output	2
Load/Store Indexed	3
Index Register Control	2
Base Register Control (optional)	2

Operational Registers

P	Register	program counter, 12 bits
I	Register	instruction register, 8 bits
D	Register	holding, 8 bits
X	Register	index, 16 bits
MA	Register	memory address, 12 bits
MD	Register	memory data, 8 bits

(MA and MD registers are contained within each 1024- or 4096-byte memory block.)

Accumulators

A	Register	accumulator and input/output, 8 bits
B	Register	accumulator and input/output, 8 bits

Input/Output

Programmed Data Transfer:
- Single byte to/from both accumulators
- External control functions, 8 per device
- External sense functions, 8 per device

Automatic Data Transfer (optional):
- Direct Memory Access at 625,000 bytes per second

Priority Interrupt:
- One level, standard
- Eight levels, optional

Control Panel

Twelve display indicators and data entry switches for all operational registers except I, D and X.
Four control indicators (LINK, OVERFLOW, STEP, and RUN)
Two sense switches
Five control switches (INITIALIZE, STEP, RUN, EXECUTE and ON/OFF)

Note: The Micro 400 will operate without the control panel which, if used can be installed up to 2 feet from the processor and is designed for mounting in the OEM user's equipment.

Dimensions

CPU	One PC board 12.5" x 18"
Memory	One PC board 12.5" x 18"
Power Supply	19" deep x 3.5" wide x 3.25" high
Enclosure	3.5" high x 17.5" wide x 21" deep

Weight

Complete Micro 400 with power supply, console, 8192 words memory: 23 pounds
Micro 400 without power supply: 10 pounds

Power

Requirements	2 amps, 105 VAC to 125 VAC, 47 to 63 Hz, single phase (other frequencies available on special order)
Dissipation	170 watts (typical)

Enclosure

The basic Micro 400 enclosure houses the complete computer: CPU board, up to 8192 words of memory, TTY or modem controller, automatic bootstrap loader, MICRObus, base register index module, power fail/restart, priority interrupts, I/O bus, power supply, and operators console. Matching expansion enclosures available for additional memory and I/O controllers.

Installation

Desk or tabletop mountable
Brackets suppled for mounting in standard 19-inch rack

Environmental

Operating Temperature	0°C to 50°C (32°F to 122°F)
Storage Temperature	-40°C to +80°C (-40°F to +176°F)
Relative Humidity	0 to 90 percent, no condensation

INSTRUCTION REPERTOIRE

Control

Mnemonic	Description
HLT	Halt
SOF	Set overflow flip-flop
ROF	Reset overflow flip-flop
EIN	Enable interrupts
DIN	Disable interrupts
NOP	No operation
SSF	Set sense flip-flop
RSF	Reset sense flip-flop

Arithmetic/Logical

The two accumulators are affected; one or both may contain operands. For arithmetic, both are operand sources and one is destination. For logical, only one accumulator is specified.

Mnemonic	Description
ABA	Add B to A
AAB	Add A to B
SBA	Subtract B from A to A
SAA	Subtract A from B to A
NBA	And B with A to A
NAB	And A with B to B
OBA	Inclusive OR B with A to A
OAB	Inclusive OR A with B to B
XBA	Exclusive OR B with A to A
LSA	Left shift A one bit, insert 0
LSB	Left shift B one bit, insert 0
RSA	Right shift A one bit, insert 0
RSB	Right shift B one bit, insert 0
RRA	Right rotate A one bit
RRB	Right rotate B one bit
OCA	One's complement A
OCB	One's complement B
TCA	Two's complement A
TCB	Two's complement B
IAA	Increment A, to A
IAB	Increment A, to B
IBB	Increment B, to B
DAA	Decrement A, to A
DAB	Decrement A, to B
DBB	Decrement B, to B
CAB	Copy A to B
CBA	Copy B to A
CLA	Clear A
CLB	Clear B
POA	Set A to positive one
POB	Set B to positive one
MOA	Set A to minus one
MOB	Set B to minus one
CLL	Clear link bit to zero
LCB	Set link bit and clear B

INSTRUCTION REPERTOIRE *(continued)*

Load/Store

Data is transferred from one memory location or one accumulator. Either may be the source;

Mnemonic	Description
LDA addr	Load A from memory
LDB addr	Load B from memory
STA addr	Store A into memory
STB addr	Store B into memory
LDA bias,x (,m)	Load A from memory indexed
LDB bias,x (,m)	Load B from memory indexed
STA bias,x (,m)	Store A into memory indexed
STB bias,x (,m)	Store B into memory indexed

Jump

With the Jump commands, the contents of the program counter are altered to affect a change in program sequencing. The Jump and Mark commands accomplish the same thing, however the original contents of the program counter are stored in the location specified by the instruction for use when returning to the original program sequence.

Mnemonic	Description
JPC addr	Jump within current 4096-byte page
JPE addr	Jump to or from extended 4096-byte page
JMC addr	Jump and Mark within current 4096-byte page
JME addr	Jump and Mark to or from extended 4096-byte page

Skip

The Skip commands permit various conditions to be tested. If the condition is true, the following two bytes are skipped.

Mnemonic	Description
SAP	Skip if A positive (or zero)
SAE	Skip if A even
SAZ	Skip if A zero
SON	Skip if overflow not set
SBP	Skip if B positive (or zero)
SBE	Skip if B even
SBZ	Skip if B zero
SLN	Skip if link not set
SNZ lit	Skip if all selected N-group conditions are zero
SAM	Skip if A minus
SAO	Skip if A odd
SAN	Skip if A not zero
SOS	Skip if overflow set
SBM	Skip if B minus
SBO	Skip if B odd
SBN	Skip if B not zero
SLS	Skip if link set
SNO lit	Skip if any of selected N-group conditions is one
SIN	Skip if interrupt enable not set
SSN	Skip if sense response not set
SRN	Skip if TTY read ready not set
SWN	Skip if TTY write ready not set
SI1	Skip if X1L=0, increment X1 by 1
SD1	Skip if X1L=0, decrement X1 by 1
SN1	Skip if sense switch 1 not set
SN2	Skip if sense switch 2 not set
SMZ lit	Skip if all selected M-group conditions are zero
SIS	Skip if interrupt-enable set
SSS	Skip if sense response set
SRS	Skip if TTY read ready set
SWS	Skip if TTY write ready set
SI2	Skip if X2L=0, increment X2 by 1
SD2	Skip if X2L=0, decrement X2 by 1
SS1	Skip if sense switch 1 set
SS2	Skip if sense switch 2 set
SMO lit	Skip if any of selected M-group conditions is one

Input/Output

Similar to data transfer except memory is not involved. One accumulator and one I/O device are specified.

Mnemonic	Description
SEN f,d	Sense device
EXC f,d	External control
DIA f,d	Data input to A register
DOA f,d	Data output from A register
DIB f,d	Data input to B register
DOB f,d	Data output from B register

Memory Test/Modify

These instructions operate directly on the contents of memory and do not affect the accumulators. The contents of the location may be shifted, rotated and/or tested for various skip conditions. During the shift, new data may be shifted into the memory location from various sources. The memory area available for these instructions is the first 256 bytes of the current 4K page.

Mnemonic		Description
SER	addr	Skip if memory even, rotate right 1 bit position
SOR	addr	Skip if memory odd, rotate right 1 bit position
SPM	addr	Skip if memory positive
SMM	addr	Skip if memory negative
RCS	addr	Right shift one bit, copy sense status into MSB.
RCZ	addr	Right shift one bit, copy zero into MSB.
RCO	addr	Right shift one bit, copy one into MSB.
RCA	addr	Right shift one bit, copy LSB of A register into MSB.

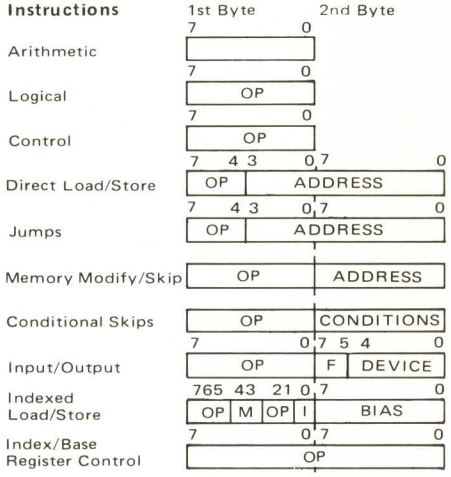
Base Register/Index Instructions

Mnemonic		Description
CLR	B1L	Clear Base 1 lower to zero
CLR	B2L	Clear Base 2 lower to zero
CLR	X1L	Clear Index 1 lower to zero
CLR	X2L	Clear Index 2 lower to zero
CLR	B1U	Clear Base 1 upper to zero
CLR	B2U	Clear Base 2 upper to zero
CLR	X1U	Clear Index 1 upper to zero
CLR	X2U	Clear Index 2 upper to zero
SB1		Set sense if Base 1 not enabled
SLE		Set sense if 'LEB' set
SEL		Set sense if 'EBL' set
SEM		Set sense if in extended memory
LEB		Set 'LEB' flip-flop
EBL		Set 'EBL' flip-flop
TRA	X1L,A	Transfer X1L to A
TRA	X2L,A	Transfer X2L to A
TRA	X1U,A	Transfer X1U to A
TRA	X2U,A	Transfer X2U to A
TRA	A,X1L	Transfer A to X1L
TRA	A,X2L	Transfer A to X2L
TRA	A,X1U	Transfer A to X1U
TRA	A,X2U	Transfer A to X2U
TRA	X1L,B	Transfer X1L to B
TRA	X2L,B	Transfer X2L to B
TRA	X1U,B	Transfer X1U to B
TRA	X2U,B	Transfer X2U to B
TRA	B,X1L	Transfer B to X1L
TRA	B,X2L	Transfer B to X2L
TRA	B,X1U	Transfer B to X1U
TRA	B,X2U	Transfer B to X2U
TRA	B1L,A	Transfer B1L to A
TRA	B2L,A	Transfer B2L to A
TRA	B1U,A	Transfer B1U to A
TRA	B2U,A	Transfer B2U to A
TRA	A,B1L	Transfer A to B1L
TRA	A,B2L	Transfer A to B2L
TRA	A,B1U	Transfer A to B1U
TRA	A,B2U	Transfer A to B2U
TRA	B1L,B	Transfer B1L to B
TRA	B2L,B	Transfer B2L to B
TRA	B1U,B	Transfer B1U to B
TRA	B2U,B	Transfer B2U to B
TRA	B,B1L	Transfer B to B1L
TRA	B,B2L	Transfer B to B2L
TRA	B,B1U	Transfer B to B1U
TRA	B,B2U	Transfer B to B2U

*WHERE:

'bias' is a positive address displacement (0-255)
'x' selects either index register 1 or 2
'm' is an optional modifier to decrement or increment the index after the memory reference
'lit' is the second byte of a two-byte instruction which selects certain specified conditions
'f' is a 3-bit function code
'd' is a 5-bit device address code
'X1L' is lower 8 bits of Index Register 1
'X1U' is upper 8 bits of Index Register 1
'X2L' is lower 8 bits of Index Register 2
'X2U' is upper 8 bits of Index Register 2
'B1L' is lower 8 bits of Base Register 1
'B1U' is upper 8 bits of Base Register 1
'B2L' is lower 8 bits of Base Register 2
'B2U' is upper 8 bits of Base Register 2
'addr' is the second byte of a two-byte instruction which specifies a memory address
'LEB' is lower core-to-extended base F/F.
'EBL' is extended base-to-lower core F/F.

INSTRUCTION/DATA FORMATS



WHERE

OP	- Operation Code
ADDRESS	- Memory Operand Address
BIAS	- Positive Index Displacement
M	- Index Modifier (Increment, Decrement, No Change)
I	- Index Register Selection (X1, X2)
F	- Peripheral Device Function Code
DEVICE	- Peripheral Device Address
CONDITION	- Status Mask for Condition Testing
S	- Sign Bit

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