Milwaukee Computers Inc.

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TECHNICAL DESCRIPTION

MC-1000 SERIES COMPUTER SYSTEMS

Processor : 6502
Reset : On power up. Manual switch also provided.
Clock : 1 MHz
Bus : Internal. Expansion port provided.
Power : +5 volts. +12 volts for disk drives only.

MEMORY

RAM : 64K utilizing 64K x 1 dynamic RAMS
63, 488 bytes usable.
ROM : 1896 bytes devoted to bootstrapping, SBIOS, and diagnostics.
Memory map :

Address (hex)	Function
0000 - F7FF	63,488 bytes RAM
F800 - F87F	128 bytes expansion bus
F880 - F897	24 bytes system I/O
F898 - FFFF	1,896 bytes ROM
	65,536 bytes total (64K)

INPUT/OUTPUT

2 RS-232 serial ports using standard DB-25 connectors. Baud rates switch selectable from 300 - 19,200 baud in multiples of two. Character format 8 bits, no parity, 1 start bit, 1 stop bit (can be altered).

1 Centronics standard parallel port using Centronics compatible connector and printer software.

1 expansion port TTL compatible using 1 DB-25 serial type connector. Lines provided include 8 data lines, 1 clock line, 1 read/write line, 1 port select line, 7 low order address lines, 2 interrupt lines, and 1 data direction line.

Realtime clock accurate within 0.2%. No battery backup provided.

DISK STORAGE

5.25 inch floppy, soft sectored, 512 bytes per sector.
Track format : 5 sectors/track single density (FM)
10 sectors/track double density (MFM)
Data transfer rate : 15,625 characters/sec. (FM)
31,250 characters/sec. (MFM)

Data per disk	Model	Format
102.4 K bytes	**MC-100, MC-1100**	Single sided, 40 tracks, FM
204.8 K bytes	**MC-200, MC-1200**	Single sided, 40 tracks MFM
409.6 K bytes	**MC-300, MC-1300**	Single sided, 80 tracks, MFM
819.2 K bytes	**MC-400, MC-1400**	Double sided, 80 tracks, MFM

UNPACKING AND SET-UP PROCEDURE

The first thing to do when you receive your MC-1000 series computer is to make copies of the disks. Obtain any 5-1/4 inch soft sectored disks (double density disks are recommended for the MC-1200 and MC-1300, and double density - double sided disks for the MC-1400). After following the power-up procedure, the p-System promptline should appear on the terminal. Type 'x'. The following should appear on the screen (your responses are shown after the question marks, and comments are shown in angle brackets). After each response, type a carriage return:

Execute what file ? initdisk

(At this point, remove the disk labeled 'BOOT1' from the disk drive and replace it with a blank disk.)

Unitnumber (4 or 5) ? 4

Starting track number ? 0

Ending track number ? (Your response depends on which model you have; see below)

Done initializing.

MODEL	Ending track#	Approx. time
MC-100 and MC-1100	39	15 sec.
MC-200 and MC-1200	39	15 sec.
MC-300 and MC-1300	79	35 sec.
MC-400 and MC-1400	159	70 sec.

After the disk is initialized, the system promptline should appear. Type 'f' for F)iler. When the Filer promptline appears, type 't' for T)ransfer. The Filer prompts 'Transfer what file ? '. If you have a single drive system, type '#4:, #4:' and put the disk to be copied in the drive. If you have a dual drive system, type '#4:,#5:' and put the disk to be copied in the left hand drive and the blank (initialized) disk in the right hand drive. Now enter a carriage return. On a single drive system, the Filer will occasionally prompt you to exchange disks when necessary.

If you wish to be able to bootstrap the new disk, you must use the 'booter' utility. Q(uit the Filer, then type 'x'. In response to 'Execute what file ?', type 'booter'. On a dual drive system, copy the bootstrap from unit 4 to unit 5. On a single drive system, specify from unit 4 to unit 4. The program will ask you to exchange disks if necessary.

POWER-UP PROCEDURE

(1) Turn on the terminal. Some time may be required for the terminal to warm up, depending on model (note that on some terminals, you must press a key on the keyboard at this point or the system will not bootstrap).

(2) Place a bootstrap diskette (such as the supplied disk labeled "BOOT1") into the left disk drive (drive A).

(3) Turn on the computer. A short message will appear on the terminal, and then the system will begin to bootstrap.

(4) After 45 to 60 seconds, the UCSD p-System welcome message should appear on the terminal. Refer to the UCSD p-System Users Manual for further information on the operating system software.

TEST MODE

The test mode of the MC-1000 series computers is entered by simply turning on the power (or pressing the reset button) when there are no disks in the drives. There are several single key commands available in the test mode:

A - Turns on drive A motor and designates drive A as the current drive.

B - Turns on drive B motor and designates drive B as the current drive.

S - Selects designated drive.

D - Deselects designated drive.

H - Homes drive head to track zero.

O - Steps drive head one step out (toward track zero).

I - Steps drive head one step in (away from track zero).

P - Prints a '*' for each index pulse when this key is held down (provided your terminal has auto-repeat).

W - If disk is write protected, prints 'Y', if not prints 'N'.

M - Performs a thorough memory test. The test takes about 8.5 minutes, and then recycles, printing a '*' on the terminal for each cycle. If an error occurs, a hexadecimal error pattern and address will be displayed on the console. If any error occurs, contact Milwaukee Computers.

E - Exits test mode (same effect as pressing the reset switch).

SOFTWARE

The standard p-System software is discussed in the supplied manuals. This section deals with programs written and supplied by Milwaukee Computers, Inc.

The INITDISK utility allows you to initialize a disk, or a portion of a disk. If you plan to create a new disk, you must initialize it first using the INITDISK utility. INITDISK asks you for the unitnumber of the disk drive containing the blank disk (beware of accidentally destroying already created system disks). Unit 4 is drive A (the left hand drive), and unit 5 is drive B (the right hand drive). The track ranges for different MC-1000 series computers are listed in the unpacking and setup procedures in this manual.

The RS-232 utility is intended to be used when the hardware specifications of your RS-232 compatible device will not allow using an 8 bit data word with 1 stop bit (for example, parity may be required), or when a baud rate of 75 or 150 is required. To achieve a baud rate of 75 or 150, set the baud rate select switch to 300 baud or 600 baud, respectively, and use the RS-232 utility to divide the effective baud rate by 4. Note that a UNITCLEAR on the RS-232 affected will reset it to the default (8 bits, 1 stop bit, baud rate divided by 1).

REALTIME is a Pascal program demonstrating the use of the real time clock. Enter a whole number from 1 to 32000 and the program will report the time required to count from 1 up to the specified value. Enter zero to end the program.

Compatibility: Milwaukee Computers MC-1000 series computers are, of course, completely software compatible with each other and with other computers using the UCSD p-System. Disks intended for the MC-1300 can also be read on the MC-1400. MC-1400 disks can be read on the MC-1300, provided no important information is recorded on the bottom side of the disk (block number greater than 789). In order to transfer files between other MC-1000 series computers, the serial port (REMOUT: and REMIN: under the p-System) may be used.

Note: A text file is included with the supplied software called 'SETUP.INFO.TEXT' which may help you to configure the system for your terminal.

The following is a list of block ranges for different MC-1000 series computers:

MC-100, MC-1100	0 - 194	(195 blocks)
MC-200, MC-1200	0 - 389	(390 blocks)
MC-300, MC-1300	0 - 789	(790 blocks)
MC-400, MC-1400	0 - 1589	(1590 blocks)

Milwaukee Computers MC-1000 Series Computers

Physical Memory Map

Address (hex)	
0000 - F7FF	62K RAM (Random Access Memory)
F800 - F87F	128 bytes expansion I/O
F880 - F881	6850 ACIA for first RS-232 (terminal)
F882 - F883	6850 ACIA for second RS-232 (remote)
F884 - F887	6821 PIA for Centronics parallel port
F888 - F88B	8253 Timer for disk motor delay and real time clock
F88C - F88F	6821 PIA for disk controller
F890 - F891	6852 SSDA for disk I/O
F892 - F897	unused I/O addresses
F898 - FFFF	1,896 bytes EPROM (for bootstrap, SBIOS, and test)

Logical Memory Map

Address (hex)	
0000 - 005F	Zero page memory reserved for SBIOS use
0060 - 007F	Reserved for use by 6502 assembled routines in RAM
0080 - 00FF	Zero page memory used by operating system
0100 - 01FF	6502 stack
0200	address of p-System Interpreter
0200 - F7F9	RAM dedicated to p-System
F7FA	6502 NMI vector points to this location
F7FD	6502 IRQ vector points to this location
F898	Address of ROM-based SBIOS
FFFA	6502 NMI jump vector
FFFC	6502 Reset jump vector (points to ROM bootstrap)
FFFE	6502 IRQ jump vector

Configuration of Parallel Port PIA

A side			B side		
PA0	I	Busy	PB0	O	Data 0
PA1	I	Acknowledge^	PB1	O	Data 1
PA2	I	Paper	PB2	O	Data 2
PA3	I	Select	PB3	O	Data 3
PA4	I	Fault^	PB4	O	Data 4
PA5	O		PB5	O	Data 5
PA6	O	Strobe^	PB6	O	Data 6
PA7	O	Prime	PB7	O	Data 7

Notes: The "I" or "O" stands for Input or Output.
The ^ symbol denotes negative logic.

Timer 0 of the 8253 programmable interval timer is currently unused. It has a 250 KHz input and may be used for any purpose desired.

Pinouts for I/O Board

RS-232 (Terminal)

1.	GND
2.	Rx data
3.	Tx data
4.	CTS^
5.	RTS^
6.	+5V
7.	GND
8.	+5V
9.	NC
10.	NC
11.	NC
12.	NC
13.	NC
14.	NC
15.	NC
16.	NC
17.	NC
18.	NC
19.	NC
20.	NC
21.	NC
22.	NC
23.	NC
24.	NC
25.	NC

2nd RS-232 (Remote)

1.	GND
2.	Tx data
3.	Rx data
4.	RTS^
5.	CTS^
6.	NC
7.	GND
8.	NC
9.	NC
10.	NC
11.	NC
12.	NC
13.	NC
14.	NC
15.	NC
16.	NC
17.	NC
18.	NC
19.	NC
20.	+5V
21.	NC
22.	NC
23.	NC
24.	NC
25.	NC

Parallel Port

1.	STROBE^
2.	D0
3.	D1
4.	D2
5.	D3
6.	D4
7.	D5
8.	D6
9.	D7
10.	ACK^
11.	BUSY
12.	PAPER
13.	SELECT
14.	NC
15.	NC
16.	GND
17.	GND
18.	GND
19.	GND
20.	GND
21.	GND
22.	GND
23.	GND
24.	GND
25.	GND
26.	GND
27.	GND
28.	GND
29.	GND
30.	GND
31.	PRIME^
32.	FAULT^
33.	NC
34.	NC
35.	NC
36.	GND

Expansion Port

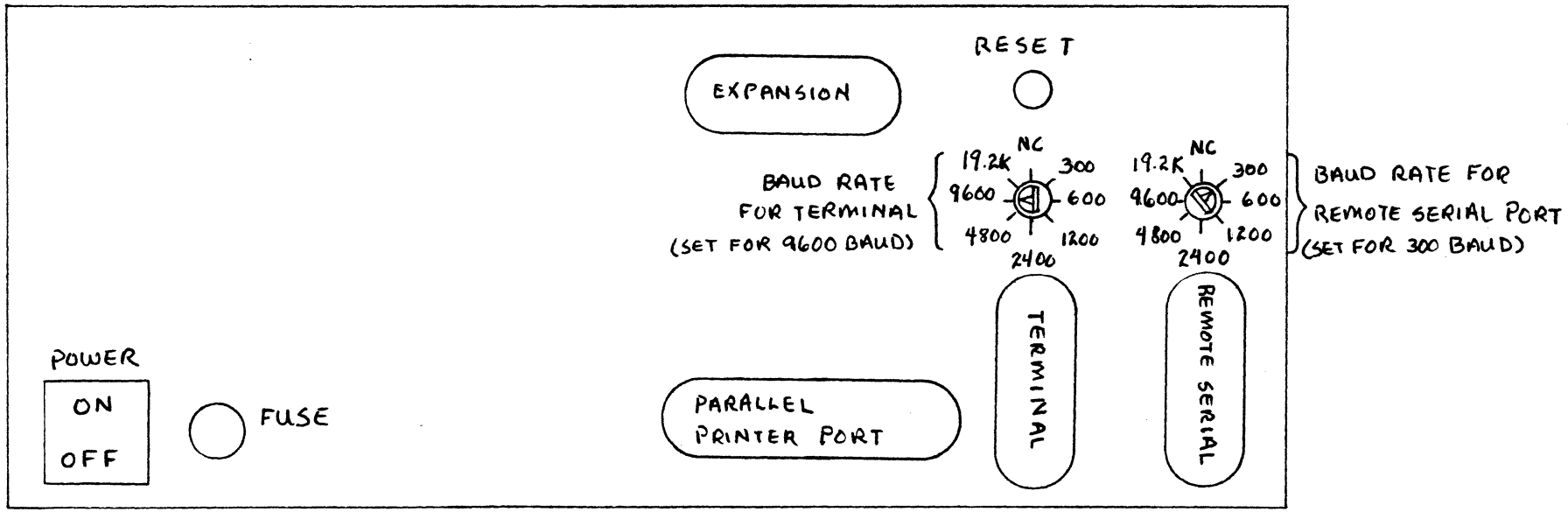
1.	GND
2.	NMI^
3.	IRQ^
4.	Bus Enable
5.	R/W
6.	Ø2 CLK
7.	GND
8.	Data Dir.
9.	D0
10.	D1
11.	D2
12.	D3
13.	D4
14.	D5
15.	D6
16.	D7
17.	NC
18.	A0
19.	A1
20.	A2
21.	A3
22.	A4
23.	A5
24.	A6
25.	NC

Note

The ^ symbol denotes negative logic.

DIAGRAM 'A'

BACK OF MC-1000 SERIES



MC-1200, New Rev (Gold Contacts)
Blank Labled PROM (Near 3242)

```
<K>*=KB000
/99
F880 B000 01 ORA (01,X)
F888 B002 01 ORA (01,X)
F810 B004 01 ORA (01,X)
F818 B006 01 ORA (01,X)
     B008 01 ORA (01,X)
     B00A 01 ORA (01,X)
     B00C 01 ORA (01,X)
     B00E 01 ORA (01,X)
     B010 01 ORA (01,X)
     B012 01 ORA (01,X)
     B014 01 ORA (01,X)
     B016 01 ORA (01,X)
     B018 01 ORA (01,X)
     B01A 01 ORA (01,X)
     B01C 01 ORA (01,X)
F87F B01E 01 ORA (01,X)
F880-F883 B020 02 ???
F884-F887 B021 04 ???
F888-F88B B022 08 PHP
F88C-F88F B023 10 BPL B045(20)
F894-F897 B025 40 RTI
     B026 80 ???
     B027 80 ???
     B028 80 ???
     B029 80 ???
     B02A 80 ???
     B02B 80 ???
     B02C 80 ???
     B02D 80 ???
     B02E 80 ???
     B02F 80 ???
     B030 80 ???
     B031 80 ???
     B032 80 ???
     B033 80 ???
     B034 80 ???
     B035 80 ???
     B036 80 ???
     B037 80 ???
     B038 80 ???
     B039 80 ???
     B03A 80 ???
     B03B 80 ???
     B03C 80 ???
     B03D 80 ???
     B03E 80 ???
     B03F 80 ???
     B040 80 ???
     B041 80 ???
     B042 80 ???
```

01 ≡ I/O EXPANSION
02 ≡ RS232 X2 (6850s)
04 ≡ PIA(6821) for Printer

08 ≡ 8253 (TIMERS)
10 ≡ 6821 PIA for disk
20 ≡ 6852 SSDA disk I/O
40 ≡ ?
80 ≡ EPROM (2716)

```
B043 80 ???
B044 80 ???
B045 80 ???
B046 80 ???
B047 80 ???
B048 80 ???
B049 80 ???
B04A 80 ???
B04B 80 ???
B04C 80 ???
B04D 80 ???
```

↕ 80 ↕

```
B1F5 80 ???
B1F6 80 ???
B1F7 80 ???
B1F8 80 ???
B1F9 80 ???
B1FA 80 ???
B1FB 80 ???
B1FC 80 ???
B1FD 80 ???
B1FE 80 ???
B1FF 80 ???
B200 00 BRK
B201 00 BRK
B202 00 BRK
B203 00 BRK
B204 00 BRK
B205 00 BRK
B206 00 BRK
B207 00 BRK
B208 00 BRK
B209 00 BRK
B20A 00 BRK
B20B 00 BRK
B20C 00 BRK
B20D 00 BRK
```

↕ 00 ↕

```
B3EF 00 BRK
B3F0 00 BRK
B3F1 00 BRK
B3F2 00 BRK
B3F3 00 BRK
B3F4 00 BRK
B3F5 00 BRK
B3F6 00 BRK
B3F7 00 BRK
B3F8 00 BRK
B3F9 00 BRK
B3FA 00 BRK
B3FB 00 BRK
B3FC 00 BRK
B3FD 00 BRK
B3FE 00 BRK
B3FF 00 BRK
B400 FF ???
B401 FF ???
B402 FF ???
B403 FF ???
B404 FF ???
B405 FF ???
B406 FF ???
B407 FF ???
B408 FF ???
B409 FF ???
```

↕ FF ↕

```
B7F5 FF ???
B7F6 FF ???
B7F7 FF ???
B7F8 FF ???
B7F9 FF ???
B7FA FF ???
B7FB FF ???
B7FC FF ???
B7FD FF ???
B7FE FF ???
<K>*=B7FF
/10
B7FF FF ???
```

```
 10;                          RM1MFM
 20;
 30;                          (512 byte sectors)
 40 Q       = $FFFF
 50 *       = $F800
 60         .BYT 'Copyright (C) 1982 '
 70         .BYT 'Milwaukee Computers, Inc.'
 80         .BYT 13,10,'16235 W Ryerson Rd.'
 90         .BYT 13,10,'New Berlin, WI 53151'
100         .BYT 13,10,'414-784-2312',13,10,0
110         .WOR Q,Q,Q,Q,Q,Q,Q,Q,Q,Q,Q,Q
120         .WOR Q,Q,Q,Q,Q,Q,Q,Q,Q,Q,Q,Q
130 *       = $FFFA
140         .WOR $F7FA
150         .WOR ROM1
160         .WOR $F7FD
170 *       = $F898
180; I/O address constants:
190 PIA     = $F884
200 ACIA2   = $F882
210 DPIA    = $F88C
220 SSDA    = $F890             (XC6852)
230 ACIA    = $F880
240 TIMER0  = $F888
250 TIMER1  = $F889
260 TIMER2  = $F88A
270 TIMER   = $F88B             (8253)
280; Numeric constants:
290 SYNC    = $B1               SSDA sync char
300 HIPAGE  = $F7               Highest page of RAM
310 TRAKS   = 160               Tracks per disk
320 SECTR   = 10                Sectors per track
330 STEPRT  = 5                 Stepper rate (ms)
340 HDSETL  = 15                Head settle time (ms)
350 MTRSTR  = 1000              Motor start time (ms)
360; Address constants:
370 AFLAG   = $2A               Motor A timeout flag
380 BFLAG   = $2B               Motor B timeout flag
390 ATMOUT  = $22
400 BTMOUT  = $26
410 MTIME   = $10
420 TRACK   = $3E
430 CURDSK  = $40
440 CURTRK  = $41
450 CURSCT  = $42
460 CURBFR  = $43
470 TOGGLE  = $53
480;
490 SBIOS   JMP SYSINT   98
500 SYSPLT  JMP ($FFFC)  9B     ;6502 RESET
510         JMP CONINT   9E
520         JMP CONSTA   A1
530         JMP CONREA   A4
540         JMP CONWRT   A7
550         JMP SETDSK   AA
560 SETTRK  STA CURTRK   AD
570         RTS
580 SETSCT  STA CURSCT   B0
```

```
 610          JMP DSKREA  B6
 620          JMP DSKWRT  B9
 630          JMP DSKINT  BC
 640          JMP DSKSTR  BF
 650          JMP DSKSTP  C2
 660          JMP PRNSTA  C5
 670          JMP PRNSTA  C8
 680 PRNREA   LDX #9      CB
 690          RTS
 700          JMP PRNWRT  CE
 710          JMP REMINT  D1
 720          JMP REMSTA  D4
 730          JMP REMREA  D7
 740          JMP REMWRT  DA
 750          LDX #9      DD
 760          RTS
 770          LDX #9      E0
 780          RTS
 790          LDX #9      E3
 800          RTS
 810          LDX #9      E6
 820          RTS
 830          JMP CLKREA  E9
 840;
 850 SYSINT   CLD
 860;                              Configure 8253 timer
 870          LDA #%01110100
 880          STA TIMER
 890          LDA #%10110100
 900          STA TIMER
 910          LDA #13
 920          STA TIMER2
 930          LDA #$80
 940          STA TIMER2
 950          LDA #2
 960          STA TIMER1
 970          LDA #0
 980          STA TIMER1
 990          LDX #40
1000          STX $20
1010 TWOSEC   LDY #250
1020          JSR DELAY
1030          DEC $20
1040          BNE TWOSEC
1050;                             Initialize disk PIA
1060          LDY #0
1070          TYA
1080          JSR SETDSK
1090          STY DPIA+1          Select DDRA
1100          LDX #%01000100
1110          STX DPIA
1120          LDA #%0100
1130          STA DPIA+1          Select PA
1140          STX DPIA            VCO off, drive=A
1150          STY DPIA+3          Select DDRB
1160          DEY
1170          STY DPIA+2          All outputs
1180          STA DPIA+3          Select PB
1190          LDY #0
1200          STY DPIA+2          MFM (Double density)
1210          LDX #0
1220          STX TIMER1
1230          LDA #$80
1240          STA TIMER1
              STA PIA+1
```

JMP SETBFR ; B3

LDA #$E0

```
1280          STA PIA
1290          LDY #%0100
1300          STY PIA+1          Select PA
1310          LDA #%11000000
1320          STA PIA            PRIME
1330          LDA #%01000000
1340          STA PIA
1350          STX PIA+3          Select DDRB
1360          DEX
1370          STX PIA+2          All outputs
1380          STY PIA+3          Select PB
1390;                            Initialize ACIA's
1400          JSR REMINT
1410 CONINT   LDA #3
1420          STA ACIA           ACIA reset
1430          LDA #%10110101     8 bits, 1 stop, /16
1440          STA ACIA
1450 CONSTA   JSR MTRCHK
1460          LDX #0
1470          LDY #0
1480          LDA ACIA
1490          LSR A              RDRF?
1500          BCC NOCHAR
1510          DEY
1520 NOCHAR   TYA
1530          RTS
1540 CONREA   LDX #0
1550 INCON    JSR MTRCHK
1560          LDA ACIA
1570          LSR A
1580          BCC INCON
1590          LDA ACIA+1
1600          RTS
1610 OUTCON   STA $1F1A
1620          JMP OUT
1630 CONWRT   LDX #0
1640          STA $1F1A
1650          JSR MTRCHK
1660 OUT      LDA #%0010
1670          BIT ACIA           TDRE?
1680          BEQ OUT
1690          LDA $1F1A
1700          STA ACIA+1
1710          RTS
1720 SETDSK   EOR TOGGLE
1730 NOTAB    STA CURDSK
1740          EOR #$FF
1750          AND #%01
1760          ROR A
1770          ROR A
1780          ROR A
1790          ORA #%0100
1800          STA DPIA
1810          RTS
1820 SETBFR   STA CURBFR
1830          STX CURBFR+1
1840          STX CURBFR+2
1850          RTS
1860 DSKREA   JSR VALID          Is CURDSK valid?
1870          JSR SEEK           Move head to CURTRK
1880 READIP   LDA DPIA
1890          BPL READIP
1900          LDX CURSCT
1910          STX $ED00          TSR SECID
```

```
1530          TXA
1540          BNE ERR
1950          LDY #1
1960          JSR DELAY          .2 ms delay
1970          LDA #%11111011
1980          AND DPIA
1990          STA DPIA           (Enable VCO)
2020          LDA #%10001011
2010          STA SSDA           Clear SSDA sync, Rx
2020          LDA #%10000010
2030          STA SSDA           Enable SSDA sync, Rx
2040          LDY #0
2050          LDX #2
2060          STX $2E 01
2070 DISKIN   LDA DPIA
2080          BPL ERR
2090          LDA SSDA
2100          LSR A              RDA?
2110          BCC DISKIN         No. Keep checking.
2120          LDA SSDA+1         Read 2 bytes at a time
2130          STA (CURBFR),Y
2140          INY
2150          LDX #0
2160          LDA SSDA+1
2170          STA (CURBFR),Y
2180          INY
2190          BNE DISKIN
2200          DEC $2E 01
2210          BEQ OFFVCO
2220          INC CURBFR+1
2230          JMP DISKIN
2240 ERR      LDX #1             Read error status
2250          STX $2D 00
2260 OFFVCO   LDA #%0100
2270          ORA DPIA
2280          STA DPIA           (VCO off)
2290          DEC CURBFR+1
2300          DEC $2D 00
2310          BNE READ2W
2320          LDA CURBFR+2
2330          STA CURBFR+1
2340          RTS
2350 WRERR    LDX #16 10
2360          RTS
2370 DSKWRT   JSR VALID          Is CURDSK valid?
2380          JSR SEEK           Move head to CURTRK
2390          LDA DPIA
2400          AND #%00100000
2410          BEQ WRERR          Write protect?
2420 WRTIP    LDA DPIA           Check for index pulse
2430          BPL WRTIP
2440          LDX CURSCT
2450          DEX
2460          BEQ WRITE
2470          LDA #$FD
2480          STA CURBFR+1       Change buffer to $FDXX
2490          STX $2D 00         Set sector count
2500          JSR READ2W         Get to sector #CURSCT
2510          TXA
2520          BNE WRERR
2530 WRITE    JSR SECTID
2540          TXA
2550          BNE WRERR
2560          LDA #%10001011
2570          STA SSDA           Reset SSDA Tx
```

```
2600          LDA #%11000001
2610          STA SSDA          Select SSDA Tx Data FIFO
2620          LDA #%0001
2630          ORA DPIA+2
2640          STA DPIA+2        Write Enable
2650          LDY #2
2660          JSR DELAY         .4 ms delay
2670          LDA #%0010
2680 SCTDRA   BIT SSDA          TDRA?
2690          BEQ SCTDRA
2700          LDA #SYNC
2710          STA SSDA+1
2720          STA SSDA+1        (2 sync chars out)
2730          LDY #0
2740          LDX #2
2750 DSKOUT   LDA #%0010
2760 TDRA     BIT SSDA          TDRA?
2770          BEQ TDRA
2780          LDA (CURBFR),Y
2790          STA SSDA+1
2800          INY
2810          LDA (CURBFR),Y
2820          STA SSDA+1
2830          INY
2840          BNE DSKOUT
2850          DEX
2860          BEQ FINWRT
2870          INC CURBFR+1
2880          JMP DSKOUT
2890 FINWRT   INY
2900          JSR DELAY
2910          JSR DLY30
2920          JSR DLY30
2930          JSR DLY20
2940          LDA #%11111110
2950          AND DPIA+2
2960          STA DPIA+2        Write enable off
2970          LDA #%10001011
2980          STA SSDA          Inhibit SSDA Tx
2990          LDA #SYNC         SSDA sync char
3000          STA SSDA+1
3010          LDA CURBFR+2
3020          STA CURBFR+1
3030          RTS
3040 SECTID   LDY #3
3050          JSR DELAY
3060          LDA #%11111011
3070          AND DPIA
3080          STA DPIA          Enable VCO
3090          JSR DLY30
3100          JSR DLY30
3110          LDA #%10001011
3120          STA SSDA          Clear SSDA Sync, Rx
3130          LDA #%10000010
3140          STA SSDA          Enable SSDA Sync, Rx
3150 READID   LDA DPIA
3160          BPL IDERR
3170          LDA SSDA
3180          LSR A
3190          BCC READID
3200          LDA SSDA+1
3210          LDY SSDA+1
3220          CMP CURTRK
3230          BNE IDERR
```

LDA #00
STA SSDA+1

IDOFFV LDx #00
LDA #04

```
3260          ORA DPIA
3270          STA DPIA
3280          LDA #%10001011
3290          STA SSDA
3300          RTS
3310 IDERR    LDX #9
3320          BNE IDOFFV
3330 VALID    LDA CURDSK
3340          CMP #2              Is CURDSK > 1 ?
3350          BMI VALDSK
3360 INVAL    PLA
3370          PLA                 Remove sub addr from stack
3380          LDX #9
3390 VALDSK   RTS
3400 DSKINT   JSR VALID
3410          LDA #%0011
3420          STA SSDA            SSDA reset, select C2
3430          LDA #%01011000
3440          STA SSDA+1          8 bits, 2 byte transfer
3450          LDA #%01000011
3460          STA SSDA            Select C3
3470          LDA #%1100
3480          STA SSDA+1          2 sync chars.
3490          LDA #%10001011
3500          STA SSDA            Select sync code register
3510          LDA #SYNC           SSDA Sync char
3520          STA SSDA+1
3530          LDA CURDSK
3540          AND #%0001
3550          TAY
3560          LDA #0
3570          STA TRACK,Y         TRACK=Zero (Y=drive#)
3580          JSR HOME
3590          JSR DSKRDY
3600          RTS
3610 HOME     LDA #%00000100
3620          ORA DPIA+2
3630          STA DPIA+2          Step direction = in
3640          JSR STEP            Take one step in
3650          LDY #88
3660          STY $21 1C
3670          LDA #%11111011
3680          AND DPIA+2
3690          STA DPIA+2          Step direction = in
3700 NXSTEP   JSR WAIT
3710          LDA #%0010
3720          BIT DPIA            Track zero?
3730          BEQ WAIT
3740          JSR STEP            Step out
3750          DEC $21
3760          BNE NXSTEP
3770 WAIT     LDY #30             6 ms delay
3780          JMP DELAY
3790 DSKSTR   JSR VALID
3800          LDA CURDSK
3810          BNE STARTB
3820          STA AFLAG
3830          LDA #%01000000
3840          BIT DPIA+2                    BIT  DPIA+2
3850          BEQ START                     BNE  SELECT
3860          JMP SELECT
3870 STARTB   LDA #0
3880          STA BFLAG
3890          LDA #%10000000
```

```
3920 START  ORA DPIA+2
3930        STA DPIA+2
3940        LDA #MTRSTR/50   Motor start delay
3950        STA $20
3960 MOTRON LDY #250
3970        JSR DELAY
3980        DEC $20
3990        BNE MOTRON
4000 SELECT LDA #%00100000   Select
4010        ORA DPIA+2
4020        STA DPIA+2
4030        RTS
4040 DSKSTP LDA #%11011111
4050        AND DPIA+2
4060        STA DPIA+2       Deselect
4070        JSR CLKREA
4080        LDA CURDSK
4090        BNE TIMEB
4100        LDX #3
4110        STX AFLAG
4120        BNE GETCLK
4130 TIMEB  LDX #7
4140        STX BFLAG
4150 GETCLK LDY #1
4160        PLA   +3
4170        ADC #$68
4180        STA ATMOUT,X
4190        DEX
4200        PLA   +2
4210        ADC #$01
4220        STA ATMOUT,X
4230        DEX
4240 CLKBYT PLA   +1
4250        ADC #0
4260        STA ATMOUT,X
4270        DEX
4280        DEY
4290        BPL CLKBYT
4300        RTS
4310 PRNSTA LDX #0
4320        LDA PIA
4330        LSR A
4340        BCC PREADY
4350        LDX #9
4360 PREADY LDA #0
4370        RTS
4380 PRNWRT PHA
4390 BUSY   LDA PIA
4400        LSR A
4410        BCS BUSY
4420        PLA
4430        STA PIA+2
4440        LDA #0
4450        STA PIA          Pulse PA6 low for STROBE
4460        JSR NULL
4470        LDA #%01000000
4480        STA PIA
4490        LDX #0
4500        RTS
4510 REMINT LDA #3
4520        STA ACIA2
4530        LDA #%10110101   8 bits, 1 stop, /16
4540        STA ACIA2
4550 REMSTA LDX #0
```

```
4580          LSR A
4590          BCC NOCHR2
4600          DEY
4610 NOCHR2   TYA
4620          RTS
4630 REMREA   LDX #0
4640 REMIN    LDA ACIA2
4650          LSR A
4660          BCC REMIN
4670          LDA ACIA2+1
4680          RTS
4690 REMWRT   LDX #0
4700 REMOUT   PHA
4710 OUTREM   LDA #%0010
4720          BIT ACIA2
4730          BEQ OUTREM
4740          PLA
4750          STA ACIA2+1
4760          RTS
4770 SEEK     LDA #%11101111
4780          AND DPIA+2
4790          STA DPIA+2        Top side
4800          LDY CURDSK
4810          LDA CURTRK
4820          CMP #80
4830          BMI SIDE
4840          SEC
4850          SBC #80
4860          TAX
4870          LDA #%0001000
4880          ORA DPIA+2
4890          STA DPIA+2        Bottom side
4900          TXA
4910 SIDE     PHA               Save physical track #
4920          SEC
4930          SBC TRACK,Y       Calculate track offset
4940          STA $30
4950          BEQ NOSTEP
4960          BPL STEPIN
4970          SEC
4980          LDA #0
4990          SBC $30
5000          STA $30           Invert result if (0
5010          LDA #%11111011
5020          AND DPIA+2
5030          STA DPIA+2
5040          BNE ALIGN         (Branch always)
5050 STEPIN   LDA #%0100
5060          ORA DPIA+2
5070          STA DPIA+2
5080 ALIGN    JSR STEP
5090          DEC $30
5100          BNE ALIGN
5110 NOSTEP   LDA CURDSK
5120          AND #%01
5130          TAY
5140          PLA               Get physical track #
5150          STA TRACK,Y
5160          LDY #HDSETL*5
5170          JSR DELAY         Head settle delay
5180;
5190; This routine checks for a floppy in CURDSK
5200; by looking for a transition on INDEX
5210:
```

```
5240          LDX #$0A
5250          STX $52
5260          LDA DPIA
5270          AND #%10000000
5280          STA $50           Save state of INDEX
5290 DISKLK   LDA DPIA
5300          AND #%10000000
5310          CMP $50           Any change?
5320          BNE DETECT
5330          LDY #1
5340          JSR DELAY         .2 ms
5350          DEC $51
5360          BNE DISKLK
5370          DEC $52
5380          BNE DISKLK        Wait 1/2 sec to give up
5390          JMP INVAL         No disk in drive
5400 DETECT   LDA DPIA
5410          BMI DETECT        Wait for index hole
5420          RTS
5430 MTRCHK   PHA
5440          TYA
5450          PHA
5460          TXA
5470          PHA
5480          LDA DPIA+2
5490          AND #%11000000
5500          BEQ NMTRON
5510          JSR CLKREA
5520          LDX #3
5530 CKLOOP   PLA
5540          STA MTIME,X
5550          DEX
5560          BPL CKLOOP
5570          LDX BFLAG
5580          BEQ CHECKA
5590          LDX #0
5600 NEXTMB   LDA BTMOUT,X
5610          CMP MTIME,X
5620          BEQ COMPMB
5630          BCS CHECKA
5640 STOPB    LDA #%01111111
5650          AND DPIA+2
5660          STA DPIA+2
5670          LDA #0
5680          STA BFLAG
5690          JMP CHECKA
5700 COMPMB   INX
5710          CPX #4
5720          BNE NEXTMB
5730 CHECKA   LDX AFLAG
5740          BEQ NMTRON
5750          LDX #0
5760 NEXTMA   LDA ATMOUT,X
5770          CMP MTIME,X
5780          BEQ COMPMA
5790          BCS NMTRON
5800 STOPA    LDA #%10111111
5810          AND DPIA+2
5820          STA DPIA+2
5830          LDA #0
5840          STA AFLAG
5850 NMTRON   PLA
5860          TAX
5870          PLA
```

```
5900          RTS
5910 COMPMA   INX
5920          CPX #4
5930          BNE NEXTMA
5940          BEQ NMTRON
5950 CLKREA   PLA
5960          STA $32
5970          PLA
5980          STA $33
5990          LDA #%01000000
6000          STA TIMER          Latch timer #1
6010          LDA TIMER1         LSBY1
6020          SEC
6030          SBC #1
6040          TAX  +3
6050          LDA TIMER1         MSBY1
6060          SBC #0
6070          AND #$7F
6080          STA $35  +2
6090          LDA #%10000000
6100          STA TIMER
6110          LDA TIMER2         LSBY2
6120          STA $36  +1
6130          LDA TIMER2         MSBY2
6140          LSR A
6150          STA $37  +0
6160          ROR $36  +1
6170          ROR A
6180          AND #%10000000
6190          ORA $35  +2        M1
6200          TAY  +2
6210          LDA $37  +0        M2
6220          EOR #$FF
6230          AND #$3F
6240          PHA  +0
6250          LDA $36  +1        L2
6260          EOR #$FF
6270          PHA
6280          TYA  +2            M1
6290          EOR #$FF
6300          PHA
6310          TXA  +3            L1
6320          EOR #$FF
6330          PHA
6340          LDA $33
6350          PHA
6360          LDA $32
6370          PHA
6380          LDX #0             Clock status
6390 RETRN    RTS
6400 ROM1     LDX #$FF
6410          TXS
6420          JSR SYSINT
6430 RST      LDX #$00
6440          STX AFLAG
6450          STX BFLAG
6460 MENU     LDA LIST,X
6470          BEQ BOOTUP
6480          JSR OUTCON
6490          INX
6500          BNE MENU
6510 BOOTUP   LDA #0
6520          STA TOGGLE
6530          JSR FBSUB
```

```
6560          LDA #1
6570          STA TOGGLE
6580          JSR FBSUB
6590          TXA
6600          BEQ LBOOT
6610          JMP TEST
6620 LBOOT    LDX #$FF
6630          TXS
6640          LDY #25
6650 NXTPM    LDA PARAMS,Y
6660          PHA
6670          DEY
6680          BPL NXTPM
6690          JMP $D200          (Addr of sec bootstrap)
6700 NODISK   LDA #%00011111
6710          AND DPIA+2
6720          STA DPIA+2
6730          LDX #9
6740          RTS
6750 FBSUB    LDA #0
6760          JSR SETDSK
6770          JSR DSKSTR
6780          JSR DSKINT
6790          TXA
6800          BNE NODISK
6810 LOADTR   LDX #$D1
6820          LDA #0
6830          JSR SETBFR
6840          JSR SETTRK
6850          LDA #1
6860          JSR SETSCT
6870 LOAD     JSR DSKREA
6880          TXA
6890          BNE NODISK
6900          LDX CURBFR+1
6910          INX
6920          INX
6930          LDA CURBFR
6940          JSR SETBFR
6950          INC CURSCT
6960          LDA CURSCT
6970          CMP #SECTR+1
6980          BNE LOAD
6990          LDX #0
7000          RTS
7010 DLY20    NOP                20 us time delay
7020          JMP DLY15
7030 DLY30    JSR NULL           30 us time delay
7040 DLY18    CPY #0             18 us entry
7050 DLY15    JMP NULL           15 us entry
7060 LIST     .BYT 7,13,10,13,10
7070          .BYT 'Milwaukee Computers, Inc.    '
7080          .BYT 0
7090 LIST2    .BYT ')Test ',7,0
7100 PARAMS   .WOR $0000,$0200,SBIOS,$0200
7110          .WOR $F7F8,TRAKS,SECTR,$0200
7120          .WOR $0001,$0001,$0000,SECTR,$0200
7130 CRLF     LDA #13
7140          JSR OUTCON
7150          LDA #10
7160          JMP OUTCON
7170 STEP     LDA #%00001000
7180          ORA DPIA+2
7190          STA DPIA+2
```

```
7220          LDY #STEPRT*5
7230 DELAY    LDX #38
7240 TIME     DEX
7250          BNE TIME
7260          EOR $FF,X
7270          DEY
7280          BNE DELAY
7290 NULL     RTS
7300 BY2HEX   PHA
7310          LSR A
7320          LSR A
7330          LSR A
7340          LSR A
7350          JSR NYBBLE
7360          PLA
7370          AND #$0F
7380 NYBBLE   CLC
7390          ADC #$30
7400          CMP #$3A
7410          BCC NUM
7420          ADC #6
7430 NUM      JMP OUTCON
7440 ZERO     LDA #%0010
7450          BIT DPIA
7460          BNE NULL
7470          LDA #8
7480          JSR OUTCON
7490          LDA #'Z
7500          JMP OUTCON
7510 TEST     LDX #0
7520 OUTEST   LDA LIST2,X
7530          BEQ CMD
7540          JSR OUTCON
7550          INX
7560          BNE OUTEST
7570 CMD      JSR INCON
7580          AND #%01011111
7590          CMP #'A
7600          BNE CONT1
7610          JSR OUTCON
7620          LDA #%01000100
7630          STA DPIA+2
7640          STA DPIA
7650          BNE CMD
7660 CONT1    CMP #'B
7670          BNE CONT2
7680          JSR OUTCON
7690          LDA #%10000000
7700          STA DPIA+2
7710          LDA #%00000100
7720          STA DPIA
7730          BNE CMD
7740 CONT2    CMP #'S
7750          BNE CONT3
7760          JSR OUTCON
7770          LDA #%00100000
7780          ORA DPIA+2
7790          STA DPIA+2
7800          BNE CMD
7810 CONT3    CMP #'D
7820          BNE CONT4
7830          JSR OUTCON
7840          LDA #%11011111
7850          AND DPIA+2
```

```
7880 CONT4   CMP #'H
7890         BNE CONT5
7900         JSR OUTCON
7910         JSR HOME
7920         JSR ZERO
7930         BNE CMD
7940 CONT5   CMP #'O
7950         BNE CONT6
7960         JSR OUTCON
7970         LDA #%11111011
7980         AND DPIA+2
7990 INOUT   STA DPIA+2
8000         JSR STEP
8010         JSR ZERO
8020 BCMD    JMP CMD
8030 CONT6   CMP #'I
8040         BNE CONT7
8050         JSR OUTCON
8060         LDA #%0100
8070         ORA DPIA+2
8080         BNE INOUT
8090 CONT7   CMP #'P
8100         BNE CONT8
8110 PULSE   LDA DPIA
8120         BMI PULSE
8130 EDGE    LDA DPIA
8140         BPL EDGE
8150         LDA #'*
8160         JSR OUTCON
8170         JMP CMD
8180 CONT8   CMP #'W
8190         BNE CONT9
8200         LDA DPIA
8210         ASL A
8220         ASL A
8230         BMI NWP
8240         LDA #'Y
8250         BNE WPROT
8260 NWP     LDA #'N
8270 WPROT   JSR OUTCON
8280 JPCMD   JMP CMD
8290 CONT9   CMP #'E
8300         BNE CONT10
8310         JMP ($FFFC)
8320 CONT10  CMP #'M
8330         BEQ MEMTST
8340; 'Q' command sets SSDA to send out zeros
8350; for 1 MHz adjustment
8360         CMP #'Q
8370         BNE JPCMD
8380         JSR OUTCON
8390         LDA #%01000100
8400         STA DPIA
8410         LDA #%00000010
8420         STA DPIA+2        Set to FM
8430         LDA #$0B
8440         STA $F890
8450         LDA #$5C
8460         STA $F891
8470         LDA #$4B
8480         STA $F890
8490         LDA #$0E
8500         STA $F891
8510         LDA #$8B
```

```
8540          STA $F891
8550          LDA #$81
8560          STA $F890
8570          JMP CMD
8580 MEMTST   JSR CRLF
8590 MLOOP    LDA #7
8600          JSR OUTCON
8610          LDA #'*
8620          JSR OUTCON
8630          LDX #0
8640          LDY #0
8650 ZPGW     STY 0,X
8660          INY
8670          INX
8680          BNE ZPGW
8690 ZPGR     TYA
8700          CMP 0,X
8710          BEQ NZPERR
8720          JSR ERRZPG
8730 NZPERR   INY
8740          INX
8750          BNE ZPGR
8760          INY
8770          BNE ZPGW
8780          STX $7E           LOW ADDRESS BYTE
8790          INX
8800          STX $7F           HIGH ADDRESS BYTE
8810          TAX
8820 HIMEM    STA ($7E),Y
8830          DEX
8840          TXA
8850          INY
8860          BNE HIMEM
8870          LDA #HIPAGE
8880          CMP $7F
8890          BEQ READM
8900          TXA
8910          INC $7F
8920          BNE HIMEM
8930 READM    STY $7F
8940 NXTPG    INC $7F
8950 CHKBYT   TXA
8960          CMP ($7E),Y
8970          BEQ NMERR
8980          JSR MEMERR
8990 NMERR    DEX
9000          INY
9010          BNE CHKBYT
9020          LDA #HIPAGE
9030          CMP $7F
9040          BNE NXTPG
9050          LDA #1
9060          STA $7F
9070          DEX
9080          TXA
9090          BNE HIMEM
9100          BEQ MLOOP
9110 ERRZPG   EOR 0,X
9120          JSR BY2HEX
9130          LDA #',
9140          JSR OUTCON
9150          LDA #0
9160          JSR BY2HEX
9170          TXA
```

```
9190          LDA #32
9200          JMP OUTCON
9210 MEMERR   EOR ($7E),Y
9220          JSR BY2HEX
9230          LDA #',
9240          JSR OUTCON
9250          LDA $7F
9260          JSR BY2HEX
9270          TYA
9280          JMP SUBH
```

PROM Listing
MC-1200, New Rev. (Gold Contacts)
MFM 6/29/82, 10 Sector (Near 6502)

```
<K>*=B000 F800
/99
B000 43 ???
B001 6F ???
B002 70 BVS B07D
B004 72 ???
B005 69 ADC #67
B007 68 PLA
B008 74 ???
B009 20 JSR 4328
B00C 29 AND #20
B00E 31 AND (39),Y
B010 38 SEC
B011 32 ???
B012 20 JSR 694D
B015 6C JMP (6177)
B018 75 ADC 6B,X
B01A 65 ADC 65
B01C 20 JSR 6F43
B01F 6D ADC 7570
B022 74 ???
B023 65 ADC 72
B025 73 ???
B026 2C BIT 4920
B029 6E ROR 2E63
B02C 0D ORA 310A
B02F 36 ROL 32,X
B031 33 ???
B032 35 AND 20,X
B034 57 ???
B035 20 JSR 7952
B038 65 ADC 72
B03A 73 ???
B03B 6F ???
B03C 6E ROR 5220
B03F 64 ???
B040 2E ROL 0A0D
B043 4E LSR 7765
B046 20 JSR 6542
B049 72 ???
B04A 6C JMP (6E69)
B04D 2C BIT 5720
B050 49 EOR #20
B052 35 AND 33,X
B054 31 AND (35),Y
B056 31 AND (0D),Y
B058 0A ASL A
B059 34 ???
B05A 31 AND (34),Y
B05C 2D AND 3837
B05F 34 ???
B060 2D AND 3332
B063 31 AND (32),Y
B065 0D ORA 000A
B068 FF ???
B069 FF ???
B06A FF ???
B06B FF ???
B06C FF ???
B06D FF ???
B06E FF ???
B06F FF ???
B070 FF ???
B071 FF ???
B072 FF ???
B073 FF ???
B074 FF ???
B075 FF ???
B076 FF ???
B077 FF ???
B078 FF ???
B079 FF ???
B07A FF ???
B07B FF ???
B07C FF ???
B07D FF ???
B07E FF ???
B07F FF ???
B080 FF ???
B081 FF ???
B082 FF ???
B083 FF ???
B084 FF ???
B085 FF ???
B086 FF ???
B087 FF ???
B088 FF ???
B089 FF ???
B08A FF ???
B08B FF ???
B08C FF ???
B08D FF ???
B08E FF ???
B08F FF ???
B090 FF ???
B091 FF ???
B092 FF ???
B093 FF ???
B094 FF ???
B095 FF ???
B096 FF ???
<K>*=B097
/99
B097 FF ???
SBIOS B098 4C JMP FBEE SYSINT
SYSHLT B09B 6C JMP (FFFC)
B09E 4C JMP FB6B CONINT
B0A1 4C JMP FB75 CONSTA
B0A4 4C JMP FB6B CONREA
B0A7 4C JMP FB99 CONWRT
B0AA 4C JMP FBAD SETDSK
SETTRK B0AD 85 STA 41 CURTRK
B0AF 60 RTS
SETSCT B0B0 85 STA 42 CURSCT
B0B2 60 RTS
B0B3 4C JMP FBBE SETBFR
B0B6 4C JMP FBC5 DSKREA
B0B9 4C JMP FBD5 DSKWRT
B0BC 4C JMP FB1F DSKINT
B0BF 4C JMP FBFE DSKSTA
B0C2 4C JMP FBB8 DSKSTP
B0C5 4C JMP FBE9 PRNSTA
B0C8 4C JMP FBE9 PRNSTA
PRNREA B0CB A2 LDX #09
B0CD 60 RTS
B0CE 4C JMP FBF6 PRNWRT
B0D1 4C JMP FC11 REMINT
B0D4 4C JMP FC1B REMSTA
B0D7 4C JMP FC28 REMREA
B0DA 4C JMP FC34 REMWRT
USRINT B0DD A2 LDX #00 OFFLINE
& B0DF 60 RTS
USRSTA B0E0 A2 LDX #00 OFFLINE
B0E2 60 RTS
USRREA B0E3 A2 LDX #00 OFFLINE
B0E5 60 RTS
USRWRT B0E6 A2 LDX #00 OFFLINE
B0E8 60 RTS
B0E9 4C JMP FB27 CLKREA
SYSINT B0EC D8 CLD
B0ED A9 LDA #74
B0EF 8D STA F00B TIMER
B0F2 A9 LDA #B4
B0F4 8D STA F00B TIMER
B0F7 A9 LDA #0D
B0F9 8D STA F00A TIMER2
B0FC A9 LDA #80
B0FE 8D STA F00A TIMER2
B101 A9 LDA #02
B103 8D STA F009 TIMER1
B106 A9 LDA #00
B108 8D STA F005 TIMER1
B10B A2 LDX #28
```

```
      B10D 86 STX 15
TWOSEC B10F A0 LDY #0D
       B111 20 JSR FE5F
       B114 C6 DEC 1B
       B116 D0 BNE B10F TWOSEC
       B118 A0 LDY #00
       B11A 98 TYA
       B11B 20 JSR F1C5 SETDSK
       B11E 8C STY F80D DPIA+1
       B121 A2 LDX #44
       B123 8E STX F80C DPIA
       B126 A9 LDA #04
       B128 8D STA F80D DPIA+1
       B12B 8E STX F80C DPIA
       B12E 8C STY F80F DPIA+3
       B131 88 DEY
       B132 8C STY F80E DPIA+2
       B135 8D STA F80F DPIA+3
       B138 A0 LDY #00
       B13A 8C STY F80E DPIA+2
       B13D A2 LDX #00
       B13F 8E STX F809 TIMER1
       B142 A9 LDA #80
       B144 8D STA F809 TIMER1
       B147 8E STX F805 PIA+1
       B14A A9 LDA #E0
       B14C 8D STA F804 PIA
       B14F A0 LDY #04
       B151 8C STY F805 PIA+1
       B154 A9 LDA #C0
       B156 8D STA F804 PIA
       B159 A9 LDA #40
       B15B 8D STA F804 PIA
       B15E 8E STX F807 PIA+3
       B161 CA DEX
       B162 8E STX F806 PIA+2
       B165 8C STY F807 PIA+3
       B168 20 JSR F011 REMINT
COINT  B16B A9 LDA #03
       B16D 8D STA F808 ACIA
       B170 A9 LDA #B5
       B172 8D STA F808 ACIA
CONSTA B175 20 JSR F007 MTRCHK
       B178 A2 LDX #00
       B17A A0 LDY #00
       B17C AD LDA F808 ACIA
       B17F 4A LSR .A
       B180 90 BCC B183 NOCHAR
       B182 88 DEY
      <K>*=B183
      /99
```

```
NOCHAR B183 98 TYA
       B184 60 RTS
CONREA B185 A2 LDX #00
INCON  B187 20 JSR F007 MTRCHK
       B18A AD LDA F808 ACIA
       B18D 4A LSR .A
       B18E 90 BCC B187 INCON
       B190 AD LDA F809 ACIA+1
       B193 60 RTS
OUTCON B194 85 STA 1A
       B196 4C JMP F00A OUT
CONWRT B199 A2 LDX #00
       B19B 85 STA 1A
       B19D 20 JSR F007 MTRCHK
OUT    B1A0 A9 LDA #02
       B1A2 2C BIT F808 ACIA
       B1A5 F0 BEQ B1A0 OUT
       B1A7 A5 LDA 1A
       B1A9 8D STA F809 ACIA+1
       B1AC 60 RTS
SETDSK B1AD 45 EOR 55 TOGGLE
NOTAB  B1AF 85 STA 40 CURDSK
       B1B1 49 EOR #FF
       B1B3 29 AND #01
       B1B5 6A ROR .A
       B1B6 6A ROR .A
       B1B7 6A ROR .A
       B1B8 09 ORA #04
       B1BA 8D STA F80C DPIA
       B1BD 60 RTS
SETBFR B1BE 85 STA 43 CURBFR
       B1C0 86 STX 44 CURBFR+1
       B1C2 86 STX 45 CURBFR+2
       B1C4 60 RTS
DSKREA B1C5 20 JSR FB14 VALID
       B1C8 20 JSR F943 SEEK
READIP B1CB AD LDA F80C DPIA
       B1CE 10 BPL B1CB READIP
       B1D0 A6 LDX 42 CURSCT
       B1D2 86 STX 00
READ2W B1D4 20 JSR FACE
       B1D7 8A TXA
       B1D8 D0 BNE B21B ERR
       B1DA A0 LDY #01
       B1DC 20 JSR FE5F DELAY
       B1DF A9 LDA #FB
       B1E1 2D AND F80C DPIA
       B1E4 8D STA F80C DPIA
       B1E7 A9 LDA #8E
       B1E9 8D STA F809 SSDA
```

```
       B1EC A9 LDA #82
       B1EE 8D STA F809 SSDA
       B1F1 A0 LDY #00
       B1F3 A2 LDX #02
       B1F5 86 STX 01
DISKIN B1F7 AD LDA F80C DPIA
       B1FA 10 BPL B21B ERR
       B1FC AD LDA F809 SSDA
       B1FF 4A LSR .A
       B200 90 BCC B1FF DISKIN
       B202 AD LDA F809 SSDA+1
       B205 91 STA (43),Y CURBFR
       B207 C8 INY
       B208 A2 LDX #00
       B20A AD LDA F809 SSDA+1
       B20D 91 STA (43),Y
       B20F C8 INY
       B210 D0 BNE B1FF DISKIN
       B212 C6 DEC 01
       B214 F0 BEQ B21F OFFVCO
       B216 E6 INC 44 CURBFR+1
       B218 4C JMP F0FF DISKIN
ERR    B21B A2 LDX #01
       B21D 86 STX 00
OFFVCO B21F A9 LDA #04
       B221 0D ORA F80C DPIA
       B224 8D STA F80C DPIA
       B227 C6 DEC 44 CURBFR+1
       B229 C6 DEC 00
       B22B D0 BNE B1D4 READ2
       B22D A5 LDA 45 CURBFR+2
       B22F 85 STA 44 CURBFR+1
       B231 60 RTS
WRERR  B232 A2 LDX #10
       B234 60 RTS
DSKWRT B235 20 JSR FB14 VALID
       B238 20 JSR F943 SEEK
       B23B AD LDA F80C DPIA
       B23E 29 AND #20
       B240 F0 BEQ B232 WRERR
WRTIP  B242 AD LDA F80C DPIA
       B245 10 BPL B242 WRTIP
       B247 A6 LDX 42 CURSCT
       B249 CA DEX
       B24A F0 BEQ B250 WRITE
       B24C A9 LDA #FD
       B24E 85 STA 44 CURBFR+1
       B250 86 STX 00
       B252 20 JSR F9D4 READ2
      <K>*=B255
      /99
```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```
B255 8A     TXA
B256 D0     BNE ~~B25C~~ WRERR
WRITE B258 20     JSR ~~FA6E~~ SELTID
      B25B 8A     TXA
      B25C D0     BNE ~~B232~~ :WRERR
      B25E A9     LDA #8B
      B260 8D     STA ~~F890~~ SSDA
      B263 A9     LDA #00
      B265 8D     STA ~~F891~~ SSDA+1
      B268 A9     LDA #C1
      B26A 8D     STA ~~F890~~ SSDA
      B26D A9     LDA #01
      B26F 0D     ORA ~~F88E~~ DPIA+2
      B272 8D     STA ~~F88E~~ DPIA+2
      B275 A0     LDY #02
      B277 20     JSR ~~FE5F~~ DELAY
      B27A A9     LDA #02
SCTDRA B27C 2C     BIT ~~F890~~ SSDA
      B27F F0     BEQ ~~B27C~~ SCTDRA
      B281 A9     LDA #~~01~~ SYNC
      B283 8D     STA ~~F891~~ SSDA+1
      B286 8D     STA ~~F891~~ SSDA+1
      B289 A0     LDY #00
      B28B A2     LDX #02
DSKOUT B28D A9     LDA #02
TDRA  B28F 2C     BIT ~~F890~~ SSDA
      B292 F0     BEQ ~~B28F~~ TDRA
      B294 B1     LDA (~~43~~),Y CURBFR
      B296 8D     STA ~~F891~~ SSDA+1
      B299 C8     INY
      B29A B1     LDA (~~43~~),Y CURBFR
      B29C 8D     STA F891 SSDA+1
      B29F C8     INY
      B2A0 D0     BNE ~~B2AB~~ DSKOUT
      B2A2 CA     DEX
      B2A3 F0     BEQ ~~B2AA~~ FINWRT
      B2A5 E6     INC ~~44~~ CURBFR+1
      B2A7 4C     JMP ~~FA6B~~ DSKOUT
FINWRT B2AA C8     INY
      B2AB 20     JSR ~~FE5F~~ DELAY
SEEKND B2AE 20     JSR ~~FDFA~~ DLY30
      B2B1 20     JSR ~~FDFA~~ DLY30
      B2B4 20     JSR ~~FDF6~~ DLY20
      B2B7 A9     LDA #FE
      B2B9 2D     AND ~~F88E~~ DPIA+2
      B2BC 8D     STA ~~F88E~~ DPIA+2
      B2BF A9     LDA #8B
      B2C1 8D     STA ~~F890~~ SSDA
      B2C4 A9     LDA #~~81~~ SYNC
      B2C6 8D     STA ~~F891~~ SSDA+1

      B2C9 A5     LDA ~~45~~ CURBFR+2
      B2CB 85     STA ~~44~~ CURBFR+1
      B2CD 60     RTS
SELTID B2CE A0     LDY #03
      B2D0 20     JSR ~~FE5F~~ DELAY
      B2D3 A9     LDA #FB
      B2D5 2D     AND ~~F88C~~ DPIA
      B2D8 8D     STA ~~F88C~~ DPIA
      B2DB 20     JSR ~~FDFA~~ DLY30
      B2DE 20     JSR ~~FDFA~~ DLY30
      B2E1 A9     LDA #8B
      B2E3 8D     STA ~~F890~~ SSDA
      B2E6 A9     LDA #82
      B2E8 8D     STA ~~F890~~ SSDA
READID B2EB AD     LDA ~~F88C~~ DPIA
      B2EE 10     BPL ~~B310~~ IDERR
      B2F0 AD     LDA ~~F890~~ SSDA
      B2F3 4A     LSR .A
      B2F4 90     BCC ~~B2EB~~ READID
      B2F6 AD     LDA ~~F891~~ SSDA+1
      B2F9 AC     LDY ~~F891~~ SSDA+1
      B2FC C5     CMP ~~44~~ CURTRK
      B2FE D0     BNE ~~B310~~ IDERR
      B300 A2     LDX #00
IDOFFV B302 A9     LDA #04
      B304 0D     ORA ~~F88C~~ DPIA
      B307 8D     STA ~~F88C~~ DPIA
      B30A A9     LDA #8B
      B30C 8D     STA ~~F890~~ SSDA
      B30F 60     RTS
IDERR B310 A2     LDX #09
      B312 D0     BNE ~~B302~~ IDOFFV
VALID B314 A5     LDA ~~40~~ CURDSK
      B316 C9     CMP #02
      B318 30     BMI ~~B31E~~ VALDSK
INVAL B31A 68     PLA
      B31B 68     PLA
      B31C A2     LDX #09
VALDSK B31E 60     RTS
DSKINT B31F 20     JSR ~~FB14~~ VALID
      B322 A9     LDA #03
      B324 8D     STA ~~F890~~ SSDA
      B327 A9     LDA #58
      B329 8D     STA ~~F891~~ SSDA+1
      B32C A9     LDA #43
      B32E 8D     STA ~~F890~~ SSDA
      B331 A9     LDA #0C
      B333 8D     STA ~~F891~~ SSDA+1
      B336 A9     LDA #8B
<K>*=B338
/00

      B338 8D     STA ~~F890~~ SSDA
      B33B A9     LDA #~~81~~ SYNC
      B33D 8D     STA ~~F891~~ SSDA+1
      B340 A5     LDA ~~40~~ CURDSK
      B342 29     AND #01
      B344 A8     TAY
      B345 A9     LDA #00
      B347 99     STA ~~008E~~,Y TRK
      B34A 20     JSR ~~FD51~~ HOME
      B34D 20     JSR ~~F989~~ DSKRDY
      B350 60     RTS
HOME  B351 A9     LDA #04
      B353 0D     ORA ~~F88E~~ DPIA+2
      B356 8D     STA ~~F88E~~ DPIA+2
      B359 20     JSR ~~FE50~~ STEP
      B35C A0     LDY #58
      B35E 84     STY ~~42~~
      B360 A9     LDA #FB
      B362 2D     AND ~~F88E~~ DPIA+2
      B365 8D     STA ~~F88E~~ DPIA+2
NXSTEP B368 20     JSR ~~FBF9~~ WAIT
      B36B A9     LDA #02
      B36D 2C     BIT ~~F88C~~ DPIA
      B370 F0     BEQ ~~B375~~ WAIT
      B372 20     JSR ~~FE50~~ STEP
      B375 C6     DEC 1C
      B377 D0     BNE ~~B368~~ NXSTEP
WAIT  B379 A0     LDY #1E
      B37B 4C     JMP ~~FE5F~~ DELAY
DSKSTR B37E 20     JSR ~~FB14~~ VALID
      B381 A5     LDA ~~40~~ CURDSK
      B383 D0     BNE ~~B391~~ STARTB
      B385 85     STA ~~56~~ AFLAG
      B387 A9     LDA #40
      B389 2C     BIT ~~F88E~~ DPIA+2
      B38C F0     BEQ ~~B39C~~ START
      B38E 4C     JMP ~~FBAF~~ SELECT
STARTB B391 A9     LDA #00
      B393 85     STA ~~5B~~ BFLAG
      B395 A9     LDA #80
      B397 2C     BIT ~~F88E~~ DPIA+2
      B39A D0     BNE ~~B3AF~~ SELECT
START B39C 0D     ORA F88E
      B39F 8D     STA F88E
      B3A2 A9     LDA #0A
      B3A4 85     STA 1B
      B3A6 A0     LDY #FA
      B3A8 20     JSR FE5F
      B3AB C6     DEC 1B
      B3AD D0     BNE B3A6
```

```
SELECT B3AF A9 LDA #20
       B3B1 0D ORA F88E
       B3B4 8D STA F88E
       B3B7 60 RTS
DSKSTP B3B8 A9 LDA #DF
       B3BA 2D AND F88E
       B3BD 8D STA F88E
       B3C0 20 JSR FD27
       B3C3 A5 LDA 40
       B3C5 D0 BNE B3CD
       B3C7 A2 LDX #03
       B3C9 86 STX 5C
       B3CB D0 BNE B3D1
       B3CD A2 LDX #07
       B3CF 86 STX 5D
       B3D1 A0 LDY #01
       B3D3 68 PLA
       B3D4 69 ADC #68
       B3D6 95 STA 54,X
       B3D8 CA DEX
       B3D9 68 PLA
       B3DA 69 ADC #01
       B3DC 95 STA 54,X
       B3DE CA DEX
       B3DF 68 PLA
       B3E0 69 ADC #00
       B3E2 95 STA 54,X
       B3E4 CA DEX
       B3E5 88 DEY
       B3E6 10 BPL B3DF
       B3E8 60 RTS
PRNSTA B3E9 A2 LDX #00
       B3EB AD LDA F884
       B3EE 4A LSR .A
       B3EF 90 BCC B3F3
       B3F1 A2 LDX #09
       B3F3 A9 LDA #00
       B3F5 60 RTS
PRNWRT B3F6 48 PHA
       B3F7 AD LDA F884
       B3FA 4A LSR .A
       B3FB B0 BCS B3F7
       B3FD 68 PLA
       B3FE 8D STA F886
       B401 A9 LDA #00
       B403 8D STA F884
       B406 20 JSR FE69
       B409 A9 LDA #40
       B40B 8D STA F884
     <K>*=B40E
```

```
       B40E A2 LDX #00
       B410 60 RTS
REMINT B411 A9 LDA #03
       B413 8D STA F882
       B416 A9 LDA #B5
       B418 8D STA F882
REMSTA B41B A2 LDX #00
       B41D A0 LDY #00
       B41F AD LDA F882
       B422 4A LSR .A
       B423 90 BCC B426
       B425 88 DEY
       B426 98 TYA
       B427 60 RTS
REMREA B428 A2 LDX #00
       B42A AD LDA F882
       B42D 4A LSR .A
       B42E 90 BCC B42A
       B430 AD LDA F883
       B433 60 RTS
REMWRT B434 A2 LDX #00
       B436 48 PHA
       B437 A9 LDA #02
       B439 2C BIT F882
       B43C F0 BEQ B437
       B43E 68 PLA
       B43F 8D STA F883
       B442 60 RTS
SEEK   B443 A9 LDA #EF
       B445 2D AND F88E
       B448 8D STA F88E
       B44B A4 LDY 40
       B44D A5 LDA 41
       B44F C9 CMP #50
       B451 30 BMI B460
       B453 38 SEC
       B454 E9 SBC #50
       B456 AA TAX
       B457 A9 LDA #10
       B459 0D ORA F88E
       B45C 8D STA F88E
       B45F 8A TXA
       B460 48 PHA
       B461 38 SEC
       B462 F9 SBC 003E,Y
       B465 85 STA 15
       B467 F0 BEQ B48B
       B469 10 BPL B47C
       B46B 38 SEC
       B46C A9 LDA #00
```

```
       B46E E5 SBC 15
       B470 85 STA 15
       B472 A9 LDA #FB
       B474 2D AND F88E
       B477 8D STA F88E
       B47A D0 BNE B484
       B47C A9 LDA #04
       B47E 0D ORA F88E
       B481 8D STA F88E
       B484 20 JSR FE50
       B487 C6 DEC 15
       B489 D0 BNE B484
       B48B A5 LDA 40
       B48D 29 AND #01
       B48F A8 TAY
       B490 68 PLA
       B491 99 STA 003E,Y
       B494 A0 LDY #4B
       B496 20 JSR FE5F
DSKRDY B499 A2 LDX #FF
       B49B 86 STX 51
       B49D A2 LDX #05
       B49F 86 STX 52
       B4A1 AD LDA F88C
       B4A4 29 AND #80
       B4A6 85 STA 50
       B4A8 AD LDA F88C
       B4AB 29 AND #80
       B4AD C5 CMP 50
       B4AF D0 BNE B4C1
       B4B1 A0 LDY #01
       B4B3 20 JSR FE5F
       B4B6 C6 DEC 51
       B4B8 D0 BNE B4A8
       B4BA C6 DEC 52
       B4BC D0 BNE B4A8
       B4BE 4C JMP FB1A
       B4C1 AD LDA F88C
       B4C4 30 BMI B4C1
       B4C6 60 RTS
MTRCHK B4C7 48 PHA
       B4C8 98 TYA
       B4C9 48 PHA
       B4CA 8A TXA
       B4CB 48 PHA
       B4CC AD LDA F88E
       B4CF 29 AND #C0
       B4D1 F0 BEQ B51A
       B4D3 20 JSR FD27
     <K>*=B4D6
```

```
B4D6 A2 LDX #03
B4D8 68 PLA
B4D9 95 STA 10,X
B4DB CA DEX
B4DC 10 BPL B4D8
B4DE A6 LDX 5D
B4E0 F0 BEQ B500
B4E2 A2 LDX #00
B4E4 B5 LDA 58,X
B4E6 D5 CMP 10,X
B4E8 F0 BEQ B4FB
B4EA B0 BCS B500
B4EC A9 LDA #7F
B4EE 2D AND F88E
B4F1 8D STA F88E
B4F4 A9 LDA #00
B4F6 85 STA 5D
B4F8 4C JMP FD00
B4FB E8 INX
B4FC E0 CPX #04
B4FE D0 BNE B4E4
B500 A6 LDX 5C
B502 F0 BEQ B51A
B504 A2 LDX #00
B506 B5 LDA 54,X
B508 D5 CMP 10,X
B50A F0 BEQ B520
B50C B0 BCS B51A
B50E A9 LDA #BF
B510 2D AND F88E
B513 8D STA F88E
B516 A9 LDA #00
B518 85 STA 5C
B51A 68 PLA
B51B AA TAX
B51C 68 PLA
B51D A8 TAY
B51E 68 PLA
B51F 60 RTS
B520 E8 INX
B521 E0 CPX #04
B523 D0 BNE B506
B525 F0 BEQ B51A
CLKREA B527 68 PLA
B528 85 STA 02
B52A 68 PLA
B52B 85 STA 03
B52D A9 LDA #40
B52F 8D STA F88B
B532 AD LDA F889
B535 38 SEC
B536 E9 SBC #01
B538 AA TAX
B539 AD LDA F889
B53C E9 SBC #00
B53E 29 AND #7F
B540 85 STA 05
B542 A9 LDA #80
B544 8D STA F88B
B547 AD LDA F88A
B54A 85 STA 06
B54C AD LDA F88A
B54F 4A LSR .A
B550 85 STA 07
B552 66 ROR 06
B554 6A ROR .A
B555 29 AND #80
B557 05 ORA 05
B559 A8 TAY
B55A A5 LDA 07
B55C 49 EOR #FF
B55E 29 AND #3F
B560 48 PHA
B561 A5 LDA 06
B563 49 EOR #FF
B565 48 PHA
B566 98 TYA
B567 49 EOR #FF
B569 48 PHA
B56A 8A TXA
B56B 49 EOR #FF
B56D 48 PHA
B56E A5 LDA 03
B570 48 PHA
B571 A5 LDA 02
B573 48 PHA
B574 A2 LDX #00
RETRN B576 60 RTS
ROM1 B577 A2 LDX #FF
B579 9A TXS
B57A 20 JSR F8E0 SYSINT
B57D A2 LDX #00
B57F 86 STX 56 AFLAG
B581 86 STX 57 BFLAG
B583 BD LDA FE02,X LIST
B586 F0 BEQ B58E BOOTUP
B588 20 JSR F994 OUTCON
B58B E8 INX
B58C D0 BNE B563 MENU
<K>*=B58F
BOOTUP B58E A9 LDA #0
B590 85 STA 53 TOGGLE
B592 20 JSR FDBF FBSUB
B595 8A TXA
B596 F0 BEQ B5A5 LBOOT
B598 A9 LDA #01
B59A 85 STA 53 TOGGLE
B59C 20 JSR FDBF FBSUB
B59F 8A TXA
B5A0 F0 BEQ B5A5 LBOOT
B5A2 4C JMP FE92 TEST
LBOOT B5A5 A2 LDX #FF
B5A7 9A TXS
B5A8 A0 LDY #19
NXTPM B5AA B9 LDA FE2C,Y
B5AD 48 PHA
B5AE 88 DEY
B5AF 10 BPL B5AA
B5B1 4C JMP D200
B5B4 A9 LDA #1F
B5B6 2D AND F88E
B5B9 8D STA F88E
B5BC A2 LDX #09
B5BE 60 RTS
B5BF A9 LDA #00
B5C1 20 JSR F9AD
B5C4 20 JSR FB7E
B5C7 20 JSR FB1F
B5CA 8A TXA
B5CB D0 BNE B5B4
B5CD A2 LDX #D1
B5CF A9 LDA #00
B5D1 20 JSR F9BE
B5D4 20 JSR F8AD
B5D7 A9 LDA #01
B5D9 20 JSR F8B0
B5DC 20 JSR F9C5
B5DF 8A TXA
B5E0 D0 BNE B5B4
B5E2 A6 LDX 44
B5E4 E8 INX
B5E5 E8 INX
B5E6 A5 LDA 43
B5E8 20 JSR F9BE
B5EB E6 INC 42
B5ED A5 LDA 42
B5EF C9 CMP #0B
B5F1 D0 BNE B5DC
B5F3 A2 LDX #00
B5F5 60 RTS
```

```
DLY20  B5F6 EA    NOP
       B5F7 4C    JMP FDFF
DLY30  B5FA 20    JSR FE69
       B5FD C0    CPY #00
       B5FF 4C    JMP FE69
       B602 07    ???
       B603 0D    ORA 0D0A
       B606 0A    ASL .A
       B607 4D    EOR 6C69
       B60A 77    ???
       B60B 61    ADC (75,X)
       B60D 6B    ???
       B60E 65    ADC 65
       B610 20    JSR 6F43
       B613 6D    ADC 7570
       B616 74    ???
       B617 65    ADC 72
       B619 73    ???
       B61A 2C    BIT 4920
       B61D 6E    ROR 2E63
       B620 20    JSR 2020
       B623 00    BRK
       B624 3E    ROL 6554,X
       B627 73    ???
       B628 74    ???
       B629 20    JSR 0007
       B62C 00    BRK
       B62D 00    BRK
       B62E 00    BRK
       B62F 02    ???
       B630 98    TYA
       B631 F8    SED
       B632 00    BRK
       B633 02    ???
       B634 F8    SED
       B635 F7    ???
       B636 A0    LDY #00
       B638 0A    ASL .A
       B639 00    BRK
       B63A 00    BRK
       B63B 02    ???
       B63C 01    ORA (00,X)
       B63E 01    ORA (00,X)
       B640 00    BRK
       B641 00    BRK
       B642 0A    ASL .A
       B643 00    BRK
       B644 00    BRK
       B645 02    ???
<K>*=B646
```

```
       B646 A9    LDA #0D
       B648 20    JSR F994
       B64B A9    LDA #0A
       B64D 4C    JMP F994
STEP   B650 A9    LDA #08
       B652 0D    ORA F88E
       B655 8D    STA F88E
       B658 29    AND #F7
       B65A 8D    STA F88E
       B65D A0    LDY #19
DELAY  B65F A2    LDX #26
       B661 CA    DEX
       B662 D0    BNE B661
       B664 55    EOR FF,X
       B666 88    DEY
       B667 D0    BNE B65F
       B669 60    RTS
       B66A 48    PHA
       B66B 4A    LSR .A
       B66C 4A    LSR .A
       B66D 4A    LSR .A
       B66E 4A    LSR .A
       B66F 20    JSR FE75
       B672 68    PLA
       B673 29    AND #0F
       B675 18    CLC
       B676 69    ADC #30
       B678 C9    CMP #3A
       B67A 90    BCC B67E
       B67C 69    ADC #06
       B67E 4C    JMP F994
       B681 A9    LDA #02
       B683 2C    BIT F88C
       B686 D0    BNE B669
       B688 A9    LDA #08
       B68A 20    JSR F994
       B68D A9    LDA #5A
       B68F 4C    JMP F994
       B692 A2    LDX #00
       B694 BD    LDA FE24,X
       B697 F0    BEQ B69F
       B699 20    JSR F994
       B69C E8    INX
       B69D D0    BNE B694
       B69F 20    JSR F987
       B6A2 29    AND #5F
       B6A4 C9    CMP #41
       B6A6 D0    BNE B6B5
       B6A8 20    JSR F994
```

```
       B6AB A9    LDA #44
       B6AD 8D    STA F88E
       B6B0 8D    STA F88C
       B6B3 D0    BNE B69F
       B6B5 C9    CMP #42
       B6B7 D0    BNE B6C8
       B6B9 20    JSR F994
       B6BC A9    LDA #80
       B6BE 8D    STA F88E
       B6C1 A9    LDA #04
       B6C3 8D    STA F88C
       B6C6 D0    BNE B69F
       B6C8 C9    CMP #53
       B6CA D0    BNE B6D9
       B6CC 20    JSR F994
       B6CF A9    LDA #20
       B6D1 0D    ORA F88E
       B6D4 8D    STA F88E
       B6D7 D0    BNE B69F
       B6D9 C9    CMP #44
       B6DB D0    BNE B6EB
       B6DD 20    JSR F994
       B6E0 A9    LDA #DF
       B6E2 2D    AND F88E
       B6E5 8D    STA F88E
       B6E8 4C    JMP FE9F
       B6EB C9    CMP #48
       B6ED D0    BNE B6FA
       B6EF 20    JSR F994
       B6F2 20    JSR FB51
       B6F5 20    JSR FE81
       B6F8 D0    BNE B69F
       B6FA C9    CMP #4F
       B6FC D0    BNE B712
       B6FE 20    JSR F994
       B701 A9    LDA #FB
       B703 2D    AND F88E
       B706 8D    STA F88E
       B709 20    JSR FE50
       B70C 20    JSR FE81
       B70F 4C    JMP FE9F
       B712 C9    CMP #49
       B714 D0    BNE B720
       B716 20    JSR F994
       B719 A9    LDA #04
       B71B 0D    ORA F88E
       B71E D0    BNE B706
       B720 C9    CMP #50
       B722 D0    BNE B736
       B724 AD    LDA F88C
<K>*=B727
```

```
B727 30 BMI B714
B729 AD LDA F88C
B72C 10 BPL B729
B72E A9 LDA #2A
B730 20 JSR F994
B733 4C JMP FE9F
B736 C9 CMP #57
B738 D0 BNE B74D
B73A AD LDA F88C
B73D 0A ASL .A
B73E 0A ASL .A
B73F 30 BMI B745
B741 A9 LDA #59
B743 D0 BNE B747
B745 A9 LDA #4E
B747 20 JSR F994
B74A 4C JMP FE9F
B74D C9 CMP #45
B74F D0 BNE B754
B751 6C JMP (FFFC)
B754 C9 CMP #4D
B756 F0 BEQ B75B
B758 4C JMP FE9F
B75B 20 JSR FE46
B75E A9 LDA #07
B760 20 JSR F994
B763 A9 LDA #2A
B765 20 JSR F994
B768 A2 LDX #00
B76A A0 LDY #00
B76C 94 STY 00,X
B76E C8 INY
B76F E8 INX
B770 D0 BNE B76C
B772 98 TYA
B773 D5 CMP 00,X
B775 F0 BEQ B77A
B777 20 JSR FF89
B77A C8 INY
B77B E8 INX
B77C D0 BNE B772
B77E C8 INY
B77F D0 BNE B76C
B781 86 STX 7E
B783 E8 INX
B784 86 STX 7F
B786 AA TAX
B787 91 STA (7E),Y
B789 CA DEX
B78A 8A TXA
B78B C8 INY
B78C D0 BNE B787
B78E A9 LDA #F7
B790 C5 CMP 7F
B792 F0 BEQ B799
B794 8A TXA
B795 E6 INC 7F
B797 D0 BNE B787
B799 84 STY 7F
B79B E6 INC 7F
B79D 8A TXA
B79E D1 CMP (7E),Y
B7A0 F0 BEQ B7A5
B7A2 20 JSR FFD1
B7A5 CA DEX
B7A6 C8 INY
B7A7 D0 BNE B79D
B7A9 A9 LDA #F7
B7AB C5 CMP 7F
B7AD D0 BNE B79B
B7AF A9 LDA #01
B7B1 85 STA 7F
B7B3 CA DEX
B7B4 8A TXA
B7B5 D0 BNE B787
B7B7 F0 BEQ B75E
B7B9 55 EOR 00,X
B7BB 20 JSR FE6A
B7BE A9 LDA #2C
B7C0 20 JSR F994
B7C3 A9 LDA #00
B7C5 20 JSR FE6A
B7C8 8A TXA
B7C9 20 JSR FE6A
B7CC A9 LDA #20
B7CE 4C JMP F994
B7D1 51 EOR (7E),Y
B7D3 20 JSR FE6A
B7D6 A9 LDA #2C
B7D8 20 JSR F994
B7DB A5 LDA 7F
B7DD 20 JSR FE6A
B7E0 98 TYA
B7E1 4C JMP FFC9
B7E4 FF ???
B7E5 FF ???
B7E6 FF ???
B7E7 FF ???
B7E8 FF ???
<K>*=B7E9
B7E9 FF ???
B7EA FF ???
B7EB FF ???
B7EC FF ???
B7ED FF ???
B7EE FF ???
B7EF FF ???
B7F0 FF ???
B7F1 FF ???
B7F2 FF ???
B7F3 FF ???
B7F4 FF ???
B7F5 FF ???
B7F6 FF ???
B7F7 FF ???
B7F8 FF ???
B7F9 FF ???
B7FA FA ???
B7FB F7 ???
B7FC 77 ???
B7FD FD SBC F7FD,X
```

```
UTIL1:
INITDISK.CODE        3 15-Jun-82
BOOTER.CODE          3  4-Dec-80
SYSTEM.LINKER       26 27-Jan-81
SYSTEM.LIBRARY      20 10-Jun-82
SYSTEM.ASSMBLER     46  2-Dec-80
6500.OPCODES         2 20-Dec-78
6500.ERRORS          7 23-Sep-80
6502.INFO.TEXT       4 31-Aug-79
SETUP.CODE          27 10-Feb-81
SCREENTEST.CODE     13  4-Jun-81
ORIENTER.CODE       12 10-Feb-81
YALOE.CODE          12  2-Dec-80
PATCH.CODE          34  3-Nov-81
COPYDUPDIR.CODE      3  2-Dec-80
MARKDUPDIR.CODE      4  2-Dec-80
DISKSIZE.CODE        3  3-Dec-80
RS-232.CODE          4 10-Jun-82
REALTIME.TEXT        4 10-Jun-82
REALTIME.CODE        2 10-Jun-82
LIBRARY.CODE        13  5-Jun-81
DECODE.CODE         28  5-Mar-81
COMPRESS.CODE       10  3-Dec-80
XREF.CODE           29  3-Dec-80
RECOVER.CODE         8  5-Dec-80
SCREENOPS.CODE      13  1-Apr-81
ADM3A.GOTO.TEXT      4 10-Jun-82
ADM3A.MISCINFO       1 14-Jun-82
ADM3A.GOTO.CODE      3 11-Jun-82
H1500.GOTO.TEXT      4 10-Jun-82
H1500.MISCINFO       1 10-Jun-82
H1500.GOTO.CODE      3 11-Jun-82
ADDS.GOTO.TEXT       4 10-Jun-82
ADDS.GOTO.CODE       3 11-Jun-82
ADDS.MISCINFO        1 10-Jun-82
H1421.MISCINFO       1 11-Jun-82
H19.MISCINFO         1 14-Jun-82
VT52.MISCINFO        1 14-Jun-82
TV950.GOTO.TEXT      4  7-Sep-82
TV950.GOTO.CODE      3  7-Sep-82
TV950.MISCINFO       1  7-Sep-82
SETUP.INFO.TEXT      6  7-Sep-82
41/41 files(listed/in-dir), 377 blocks used, 13 unused, 13 in largest
```

```
WORK01:
SYSTEM.PASCAL     103 27-Sep-82
SYSTEM.INTERP      30 27-Sep-82
SYSTEM.MISCINFO     1 10-Jun-82
SYSTEM.FILER       33 19-Oct-81
SYSTEM.EDITOR      49 30-Jan-81
BOOTER.CODE         3  4-Dec-80
INITDISK.CODE       3 30-Jul-82
COPIER.CODE         3 14-Jun-82
SYSTEM.COMPILER    94 14-May-81
SYSTEM.LIBRARY     20 10-Jun-82
NO                  0  8-Jan-83
PRINTER             1 20-Mar-83
12/12 files<listed/in-dir>, 346 blocks used, 44 unused, 44 in largest
```