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A LOW-COST OUTPUT TERMINAL FOR TIME-SHARED COMPUTERS

by

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Project MAC
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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ABSTRACT

This report describes a low-cost remote terminal to provide switch-form output from a time-shared digital computer. The terminal consists of a modified model 35 KSR teletype and a local memory unit. The unit is independent of any particular computer, and is easy to test and maintain. The states of the memory control and memory words are observable directly by indicator lights.

An application of the memory to automatic set-up and control of an analog computer is described. In this application the results of the analog computation are displayed on an oscilloscope; this makes possible, for example, rapid display of the time response of linear systems, under digital program control.

ACKNOWLEDGMENTS

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The support of Philbrick Researches, Inc., is also gratefully acknowledged.

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SECTION I

INTRODUCTION

1.1 GENERAL PURPOSE OF TERMINAL

The problem of retrieving information from a time-shared digital computer is typically met in several ways; e.g., printers, punched cards, and magnetic tape. For many applications it is desirable to have access to digital information in the form of switch settings (or states). This permits local decisions to be made regarding the use of such information. For example, a terminal which has a keyboard and a bank of switches under digital computer program control, permits symbolic manipulation and control of local hardware, as well as computer analysis of experimental data in the laboratory. It is the purpose of the equipment described in this report to provide such a terminal at low cost. The terminal itself is ultimately connected to an on-line time-shared digital computer.

1.2 PARTICULAR CONSTRAINTS ON TERMINAL DESIGN

Several restrictions were placed on the nature of the terminal, primarily to ensure easy access to components for maintenance, and partly to minimize cost. Among the restrictions were that:

1. The terminal equipment must be entirely local, communicating with the digital computer only by a single telephone line;
2. The memory unit must be compatible with a standard model 35 KSR teletype unit, which provides the keyboard and printer functions, as well as modulating and demodulating equipment for transmission and reception. In particular, this implies that the memory unit must operate at teletype-compatible speeds (as a minimum), and from standard teletype code.

The device which meets the above restrictions is a local, low-speed memory unit that is independent of the type of computer. Teletypes are relatively inexpensive devices that are fairly well-suited to computer keyboard communication. Some indication of the cost of nonstandard parts for the memory is presented in Appendix A.

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SECTION II

TERMINAL SYSTEM

The major components of the terminal system are shown in Figure 1 in terms of the information flow. Between the teletype and the digital computer there is a bilateral channel. The logic unit monitors all teletype communications, either received from the computer or generated by the keyboard, and responds to certain control characters. When the logic unit accepts data, they are used to fill the data memory. The memory contents may be used as required to control auxiliary equipment.

A picture of the terminal is shown in Figure 2. Figure 3 depicts the functional units and their connections. Also shown are components of an analog computer which is described in Section III. Appendix B describes the cable functions, and explains the addressing system built into cable "d".

2.1 TELETYPE UNIT

The teletype is a modified Model 35 Keyboard-Send-and-Receive (KSR) with a set of read-out switches to make available eight bits of coded information per teletype character. Of the eight available bits, the logic and data memory use a subset of six bits, for which a full count (0 to 63 in binary form) exists. The maximum transmission rate for teletype characters is about ten per second.

The input circuit to the logic unit from the teletype is shown in Figure 4. This connection is cable "a" of Figure 3. Detailed information on standard teletype codes and cycle operation is available elsewhere[1]. It is possible to inhibit or enable the printing of information intended for the memory by use of the printer control characters of the teletype. The memory may be loaded directly from the keyboard, which is useful for testing and manipulation purposes (e.g., even if the computer is not operating it is possible to load the memory).

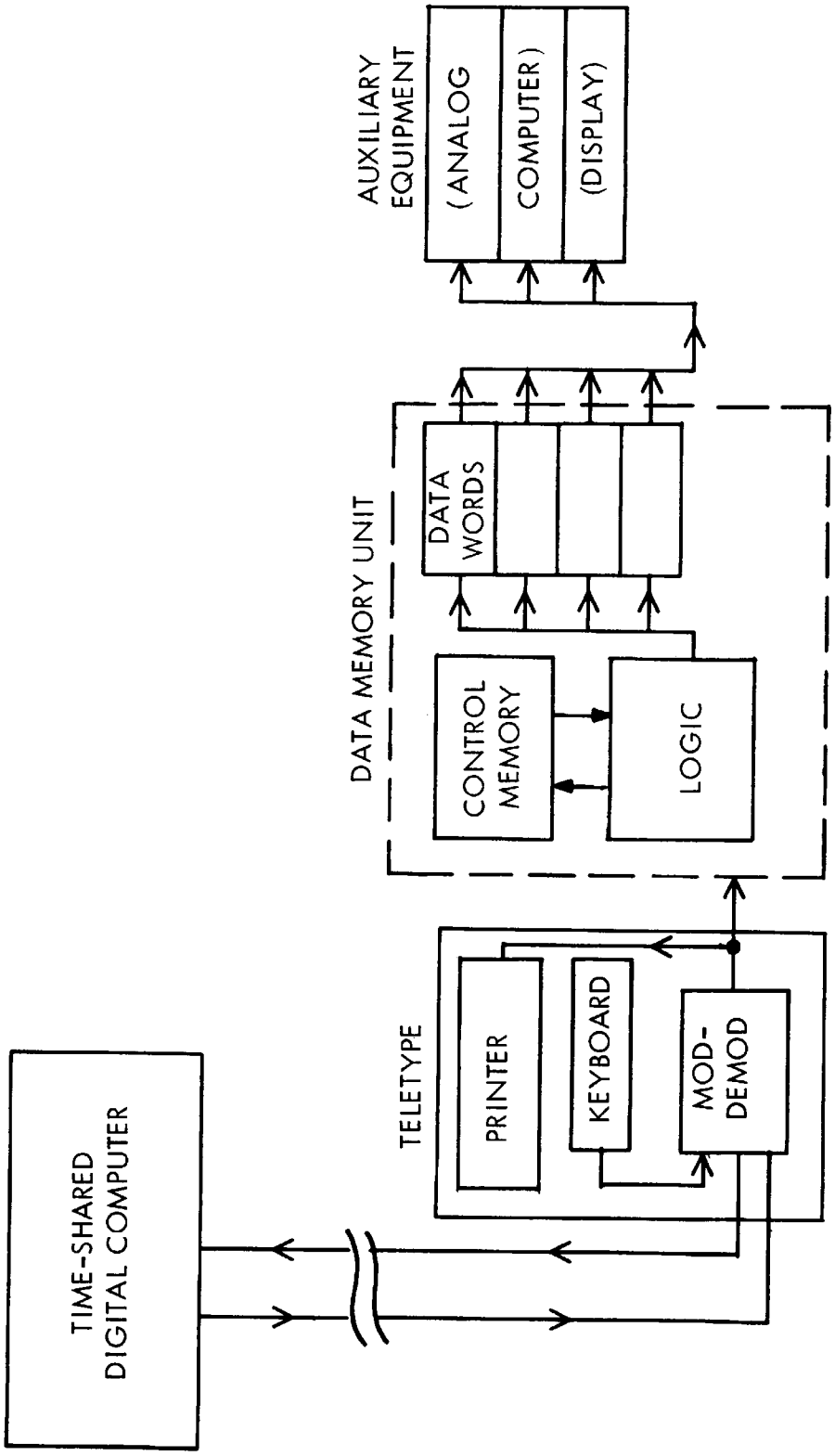

Figure 1. Major Terminal Components, Showing Information Flow

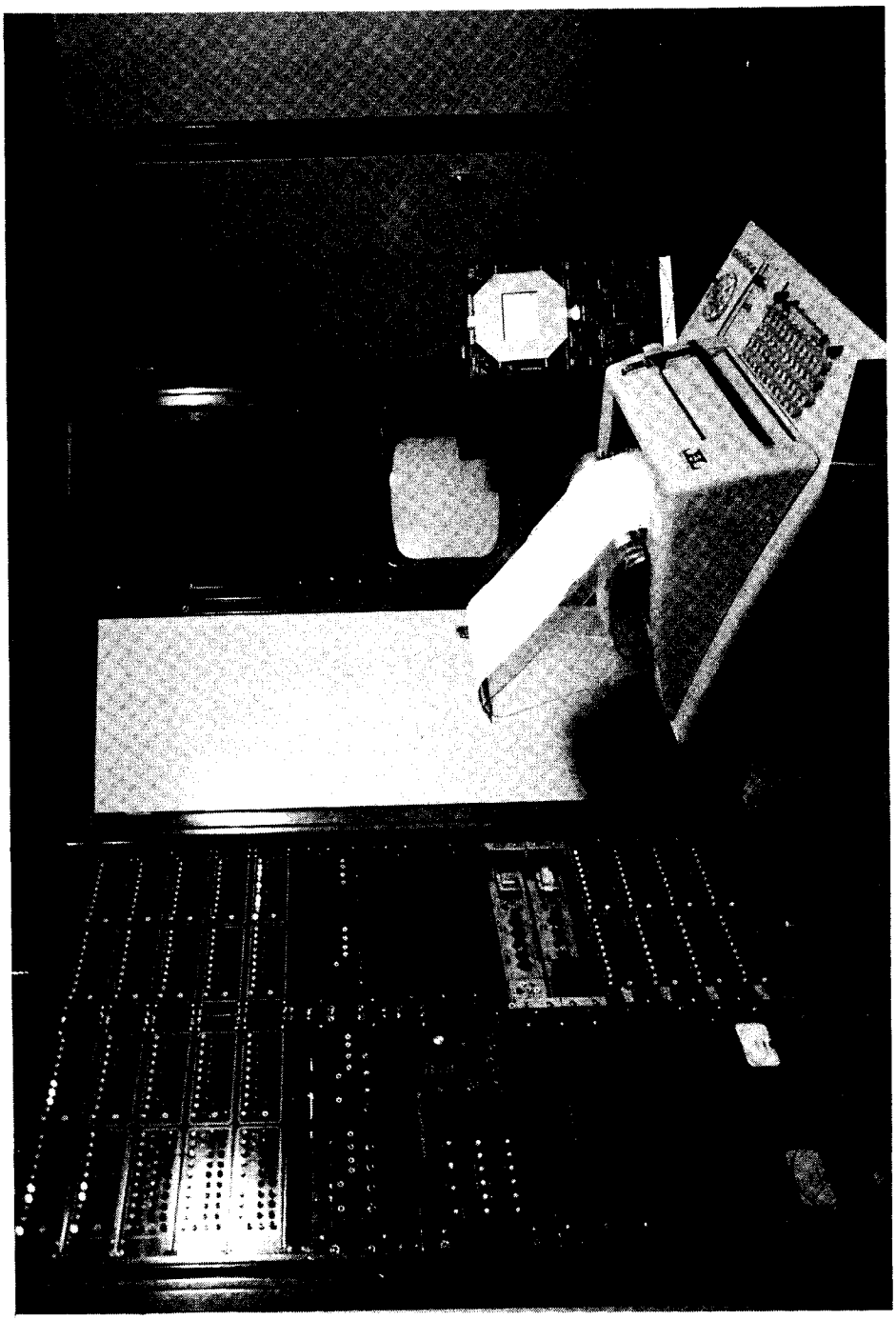

Figure 2. A Remote Terminal Set-up

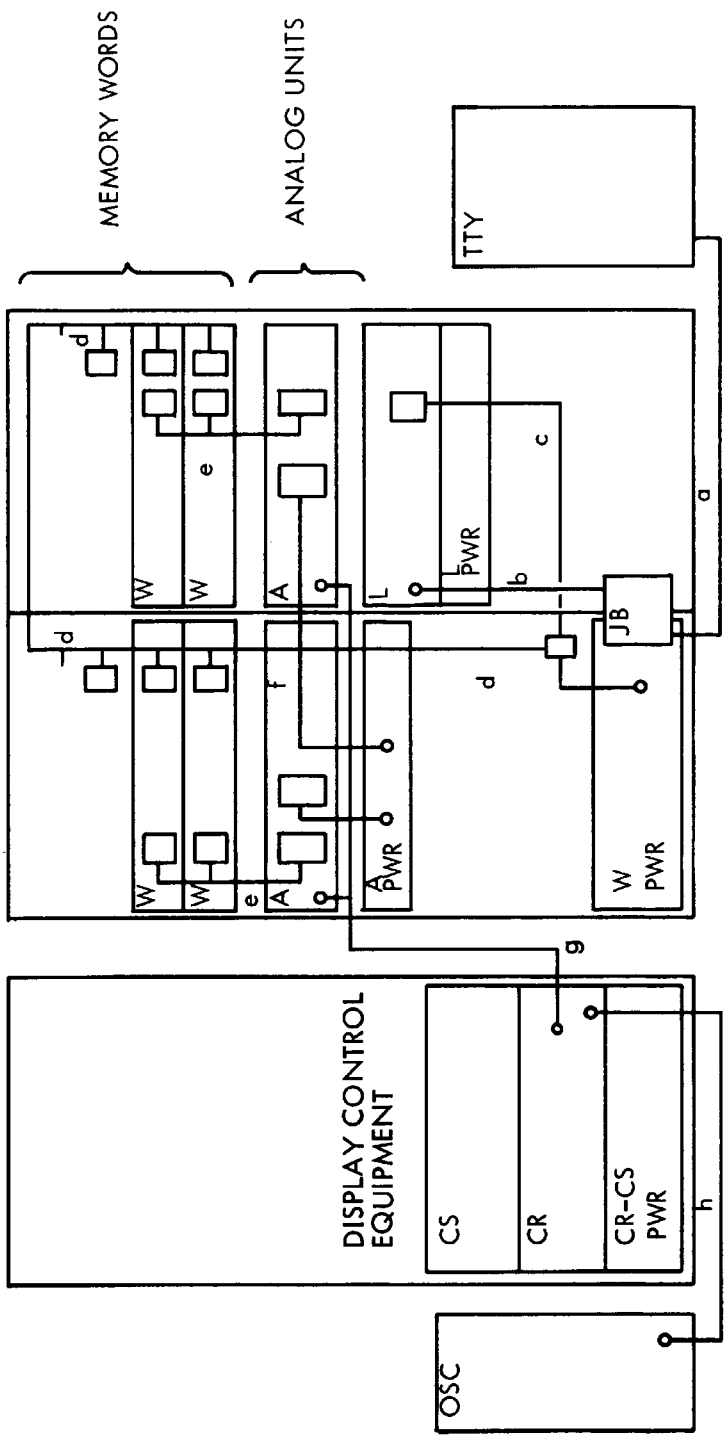

Figure 3. Diagram of Terminal Equipment, Showing Functional Units and Connections

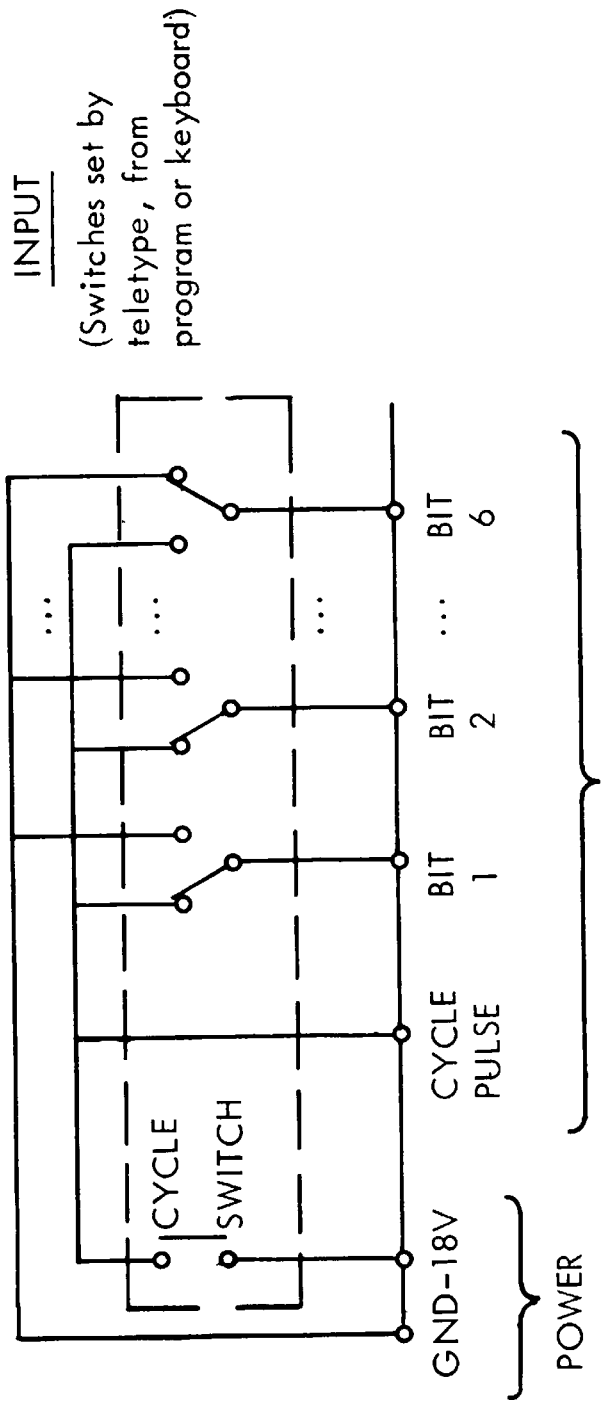

Figure 4. Input Circuit from Teletype to Logic Unit

2.2 LOGIC UNIT

The logic unit receives its information from the teletype. Use of the information depends upon the logic unit state and the reception of several special-purpose machine commands listed below:

Machine Command	Function
START	enables the logic unit to process all subsequent input characters (stable until changed);
ADDRESS	sets the internal counter to interpret the following input character as an address;
STOP	ignores all subsequent input characters except START command (stable until changed).

After a START command has been received, the following internal machine states may exist:

Machine State	Description
ADDRESS	use the next input character to select a data memory word;
LEFT	use the next character to load the left half of the presently addressed word;
RIGHT	use the next character to load the right half of the presently addressed word.

The three machine command characters for the logic unit set the states START and STOP, and reset the cycle counter to ADDRESS. The cycle counter automatically advances the internal state from ADDRESS to LEFT to RIGHT (and so on), one step per set of input data. Figure 5 shows a schematic of the logic unit.

In addition to the teletype (external) input which is normally used, the unit is equipped with a set of toggle and control switches to permit the manual input of data. This feature has proven useful for test and debugging purposes. The front panel also has a set of lights which show the state of the logic unit, and the value of the current data word.

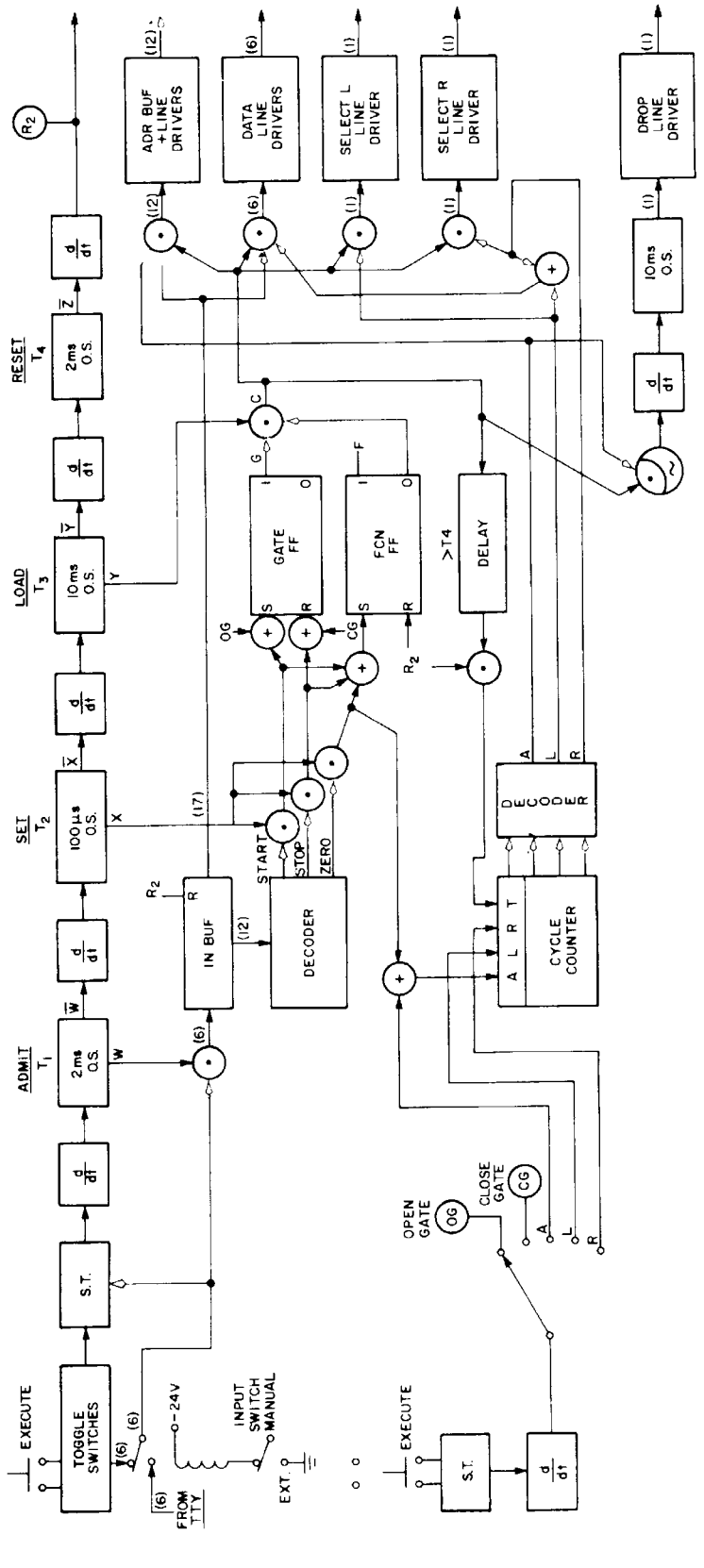

Figure 5. Logic Unit Schematic

2.3 DATA MEMORY

Each data memory word consists of ten bits — nine single-pole and one double-pole (or sign) bit. All bits are self-latching, as may be seen from Figure 6, which is a circuit diagram of a word of memory. When a word is addressed, its present contents are erased or dropped (i.e., the drop line is activated) in preparation for loading the left half (bits S, 1 to 4), and then the right half (bits 5 to 9).

Each memory chassis contains two words, whose addresses differ only in the final bit. All the memory word chassis are interchangeable, because the addressing is done by the wiring in cable "d" (see Figure 3). Although only thirty-two addressable words have been built, the system is designed to allow sixty-one or sixty-four words if the logic control characters are modified suitably. Figure 7 is a photograph of a memory chassis, indicating the common input block for the pair of words. The components are mounted on printed circuit boards.

Output from each word is available at the front panel as sets of terminal pairs, and in the back on a 24-pin connector. The state of each bit is shown by a light. A program written for the Project MAC IBM 7094 computer allows testing of the memory by an easily used set of commands. The author is Stephen Braunstein, an M.I.T. undergraduate student. Instructions for the use of the program are shown on the opposite page as part of an on-line interactive exchange between program and user. Because the basic program was written to operate on the M.I.T. time-sharing system, where certain modifications have been made to the teletype code and FORTRAN Monitor System (FMS), listings are not included here.

Detailed drawings of all circuits, components, and packaged unit for this terminal unit are available as Series 20065 from:

Miss Grace Lynch, Secretary
Rm. 3-150, Engineering Projects, Lab.,
Department of Mechanical Engineering
Massachusetts Institute of Technology
Cambridge, Massachusetts 02139

```
LOADGO MTEST TBIT
W 1008.5
 NEED BR     CLOCK
R 10.033+.833

USE BRCLOK
W 1008.9
EXECUTION.

'MEMORY' WILL LOAD, CLEAR, AND THEN LOAD MEMORY.
'CLEAR' WILL CLEAR MEMORY.
'RAMP12' WILL GENERATE RAMPS WITH INTEGRATORS 1 AND 2.
'RAMP34' WILL GENERATE RAMPS WITH INTEGRATORS 3 AND 4.
'SELF' WILL SET UP A FIRST ORDER SYSTEM FOR EACH INTEGRATOR.
'OSC12' WILL SET UP AN OSCILLATING SYSTEM WITH INTEGRATORS 1 AND 2.
'OSC34' WILL SET UP AN OSCILLATING SYSTEM WITH INTEGRATORS 3 AND 4.
'MEMO', WHERE '0' IS AN INTEGER 1-6, WILL PERFORM THE MEMORY TEST
    ON ONE OF THE SIX VERTICAL WORD BLOCKS.
'CLEARO', WHERE '0' IS AN INTEGER 1-6, WILL CLEAR ONE OF THE
    SIX VERTICAL WORD BLOCKS.


INITIAL CONDITIONS OF INTEGRATORS--
   INTEGRATOR      I.C
        1           +30
        2           +10              (This is reference information
        3           -10              for signals on the analog display.)
        4           -30


GO AHEAD..
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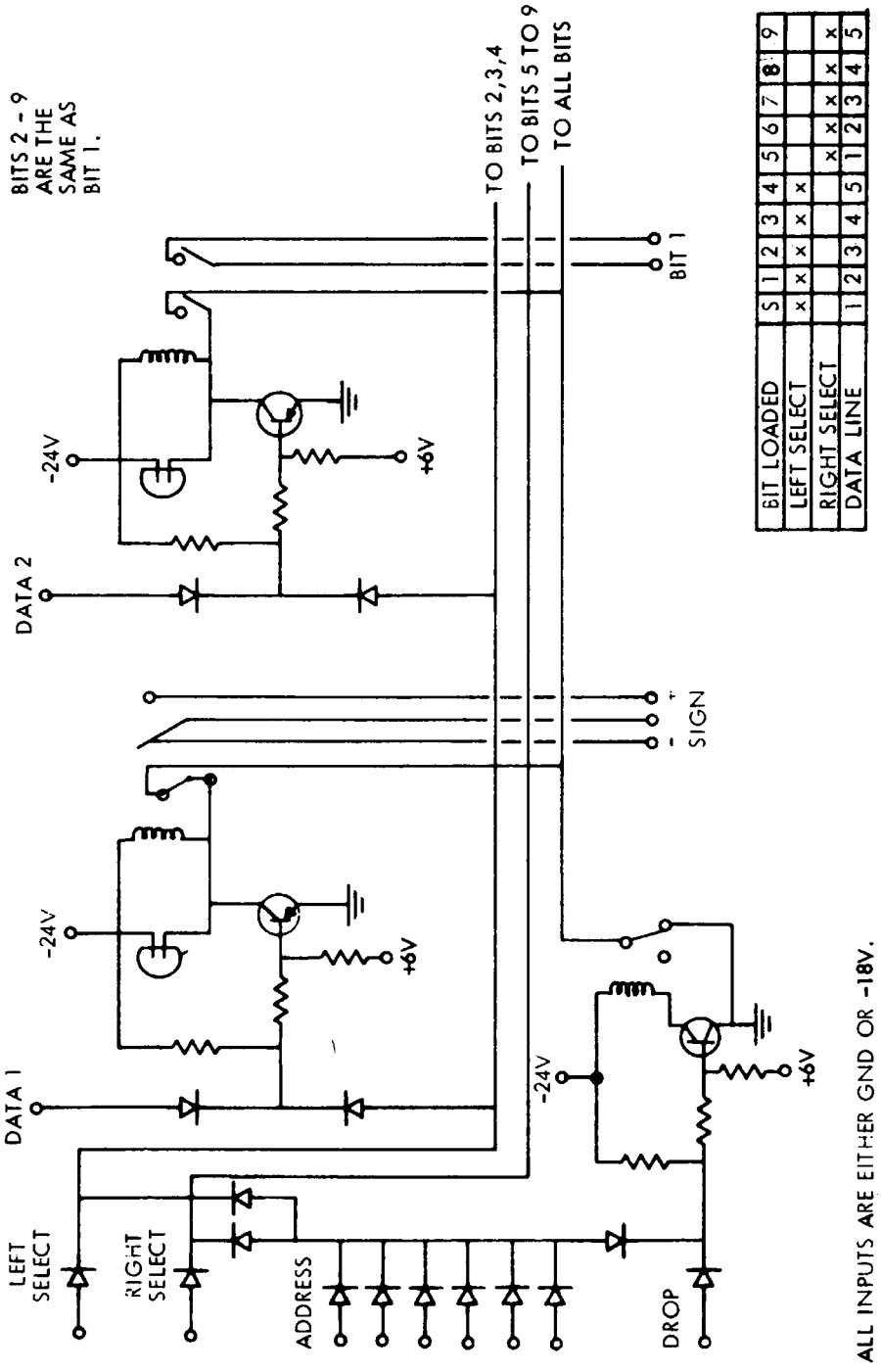

Figure 6. Schematic of a Memory Word Part

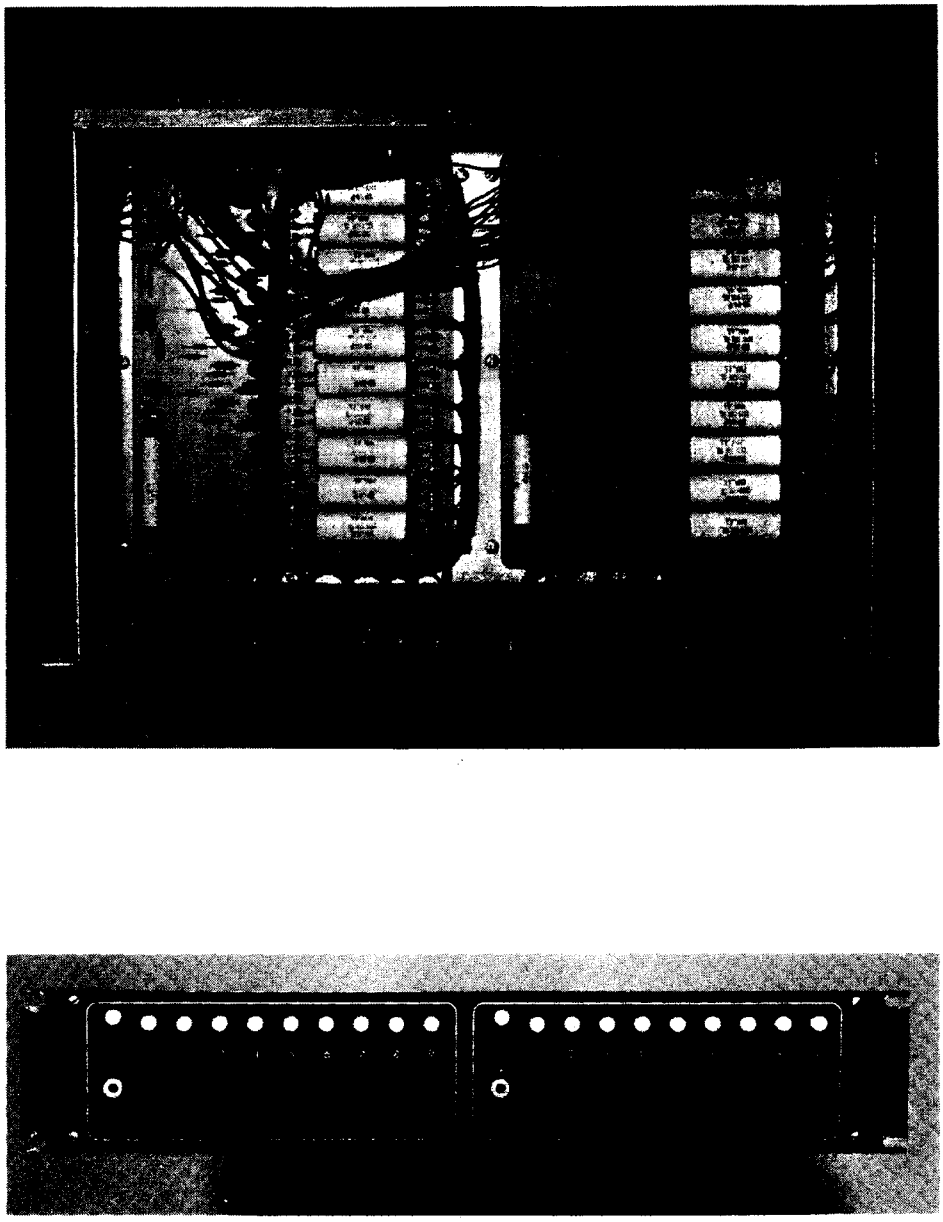

Figure 7. A local Memory Unit

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SECTION III

AN APPLICATION - AUTOMATED ANALOG COMPUTATION

This section describes using part of the memory to set up (program) an analog computer by means of a digital computer. As anyone who has worked with analog computers knows, the problems of set-up (e.g., wiring) and scaling (e.g., adjusting coefficients and integration rates) are not trivial; even when the problem is linear.

3.1 PURPOSE OF ANALOG COMPUTER

The particular analog computer described in this report was used to simulate simple linear dynamic systems. The principal purpose was to display on a screen the wave forms of key variables in a rapid fashion. The remote terminal, equipped with such an automatic display facility, was used in an automated teaching experiment concerned with dynamic system behavior [5].

3.2 ANALOG COMPUTER

The analog computer design was strongly influenced by the organization of the Philbrick K5-U Universal Linear Operator [3]. A fourth-order, completely coupled linear system can be simulated, by the use of four identical summing integrator units, whose coefficients and initial conditions are set by the (digital) program. The analog and display units are shown as terminal system components in Figure 3. In particular, cable "e" provides control data from the memory for the analog units, and cable "g" presents the variables to the display unit. Figure 8 shows an analog integrator unit. Figure 9 shows a block diagram for an integrator unit, and indicates the form of system equations. Figure 10 is the integrator unit schematic, and Figure 11 gives details of a transconductor block, which is the memory-controlled coefficient.

The repetition rate was fixed at twenty cycles per second due to match the display equipment. However this rate may also be brought under program control by providing a switch-controlled set of integrating capacitors; an easy matter with the present equipment. This would extend the dynamic range of systems which could be simulated.

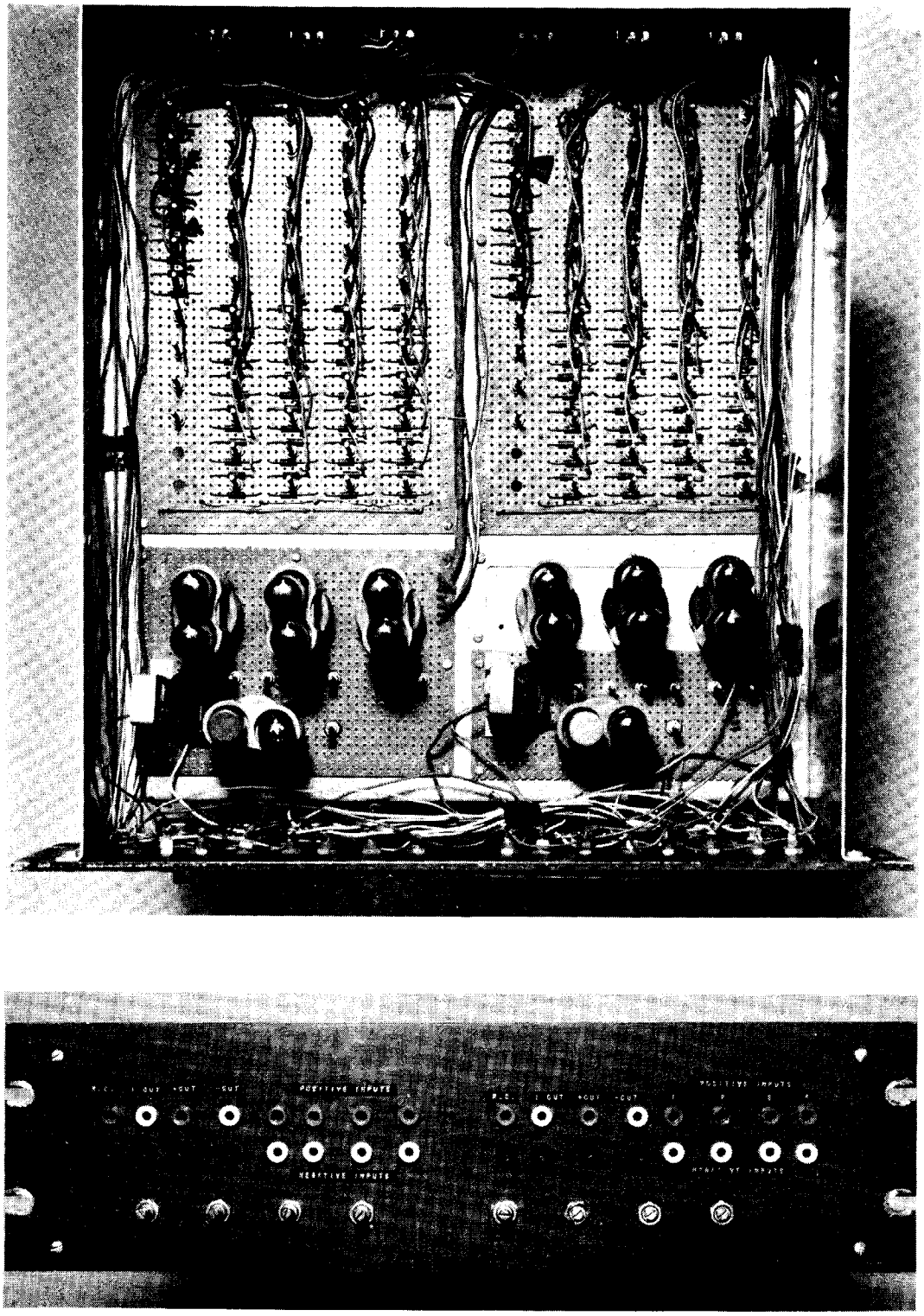
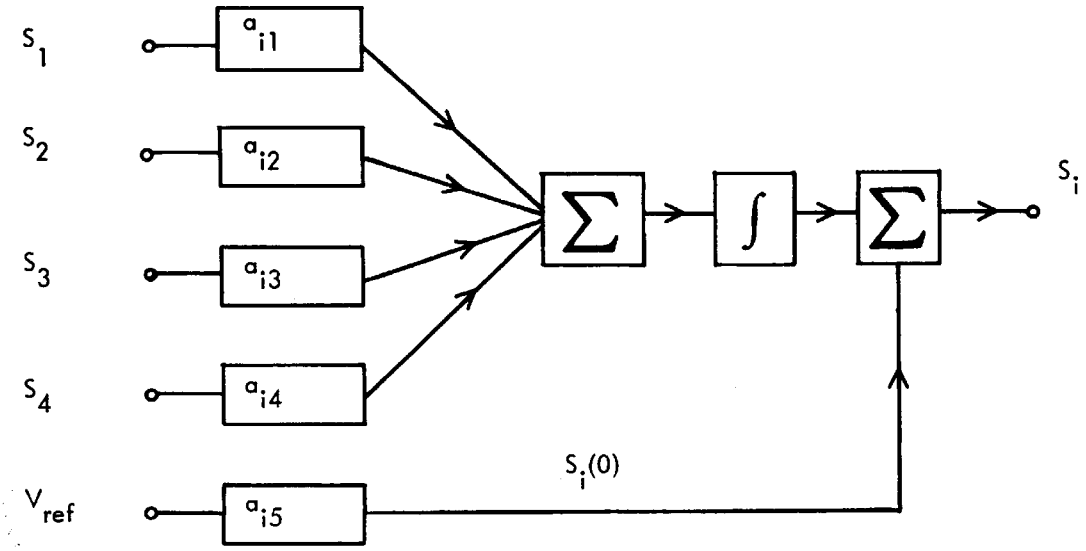


Figure 8. An Analog Integrator Unit

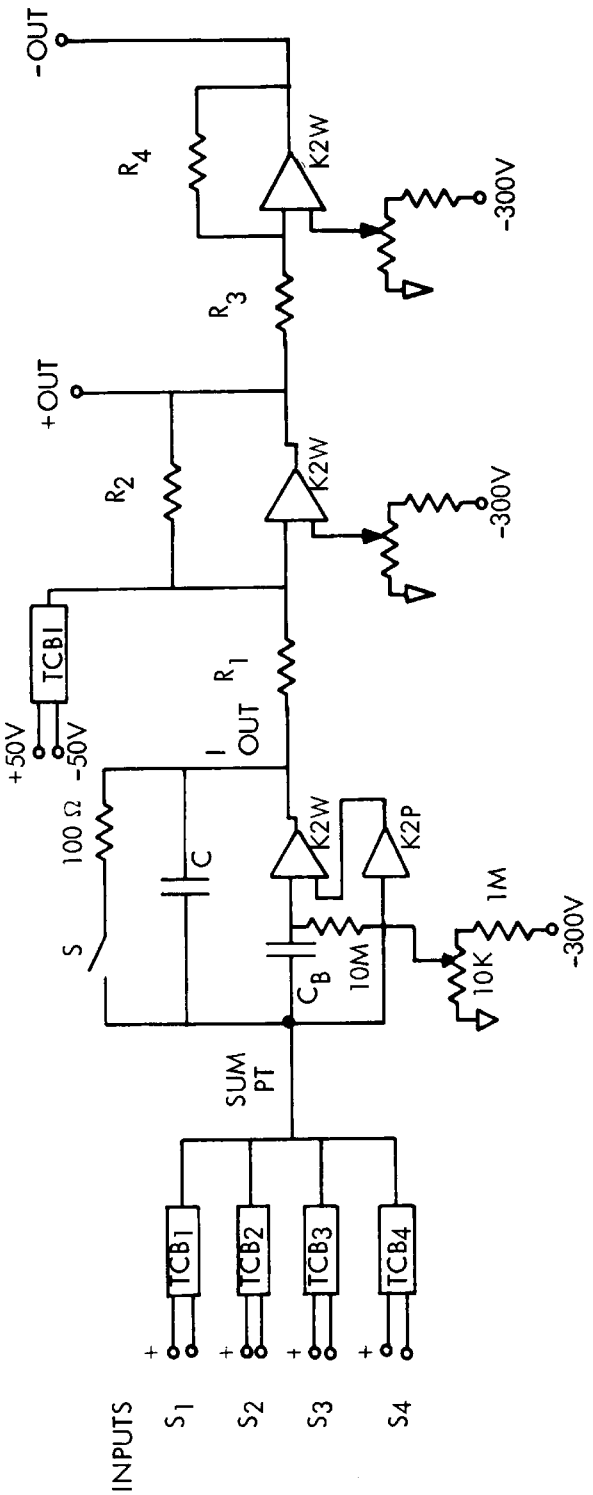


Initial Condition: $S_i(0) = a_{is} * V_{ref}$

Integral Form: $S_i(t) = S_i(0) + \int_0^{t_4} \sum_{j=1} a_{ij} S_j(t) \cdot dt$

Derivative Form: $ds_i/dt\ (t) = \sum_{j=1}^{4} a_{ij} s_j(t)\ _j\ S_i(0)$

Figure 9. Analog Integrator Unit Block Diagram, and Associated System Equations



C - integrating capacitor

C_B - blocking capacitor

R_1 to R_4 - inverter and adder resistors

TCB - transconductor block

TCBI - transconductor block for initial condition

S - the cycle switch (closed is reset to zero)

Amplifier functions:

First stage - integrator (K2P stabilized)

Second stage - adds the initial condition

Third stage - inverts the positive signal

Figure 10. Schematic of an Integrator Unit

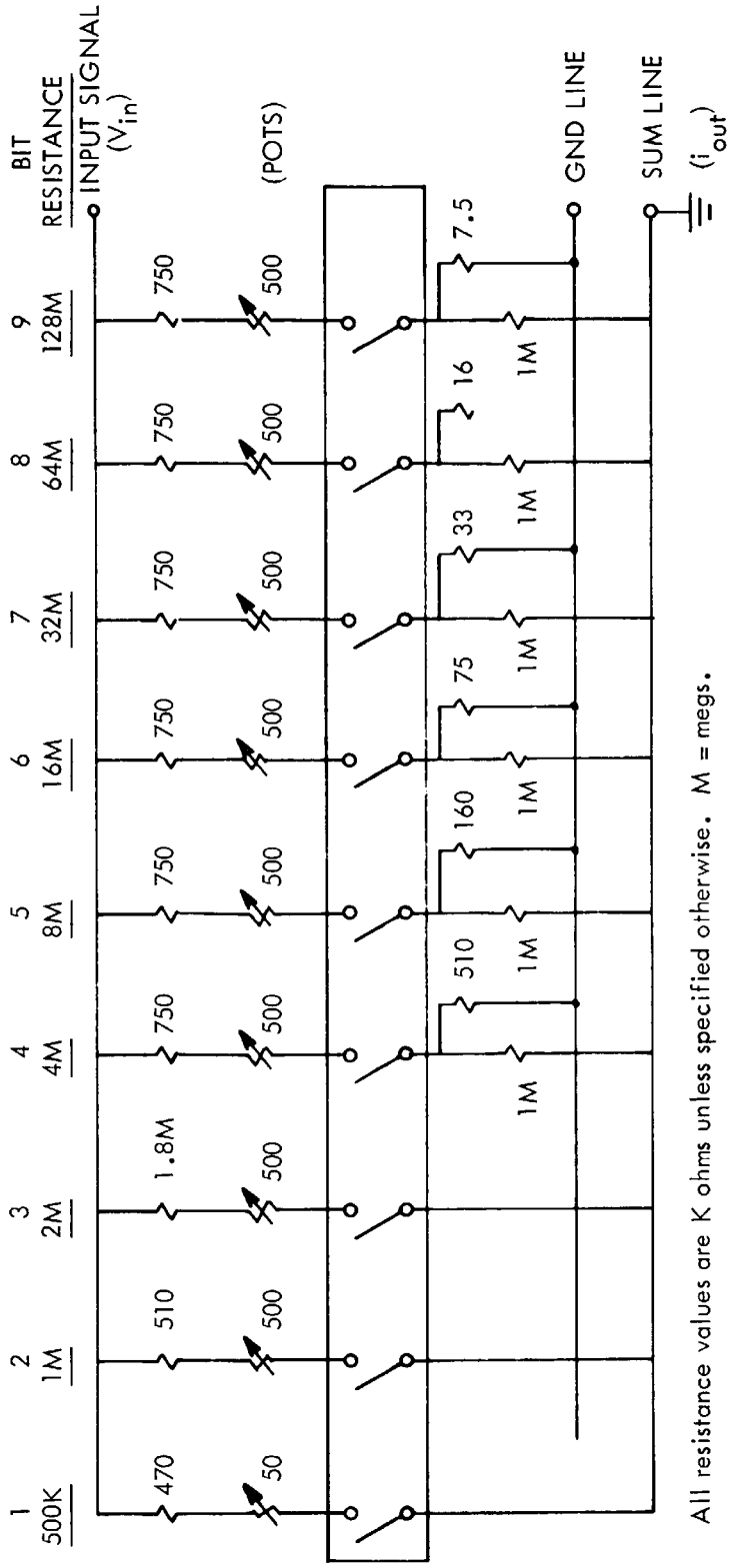


Figure 11. Schematic of a Transconductor

For the particular application described here, the memory words were connected to the analog units in a pattern which allowed direct observation of the analog computer set-up from the memory front panel lights. Each column of memory words contains the four input coefficients and, at the bottom, the weighting factor for an initial condition.

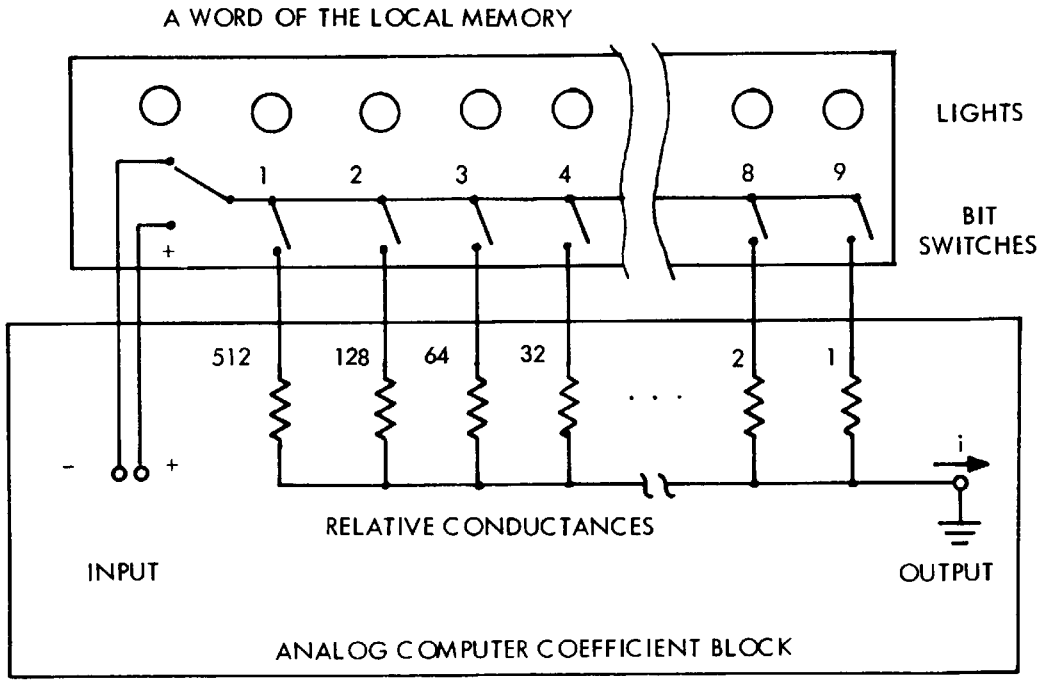
A five-by-four block of memory words was wired as shown below:

Variable	S_1	S_2	S_3	S_4
	A_{11}	A_{21}	A_{31}	A_{41}
	A_{12}	A_{22}	A_{32}	A_{42}
	A_{13}	A_{23}	A_{33}	A_{43}
	A_{14}	A_{24}	A_{34}	A_{44}
Initial Conditions	A_{15}	A_{25}	A_{35}	A_{45}

These coefficients refer to the equation in Figure 9.

The information transmitted by the digital program for display generation was near a minimum, since only structural and parametric data (plus initial conditions) had to be sent. A second-order system might require six data words plus a few control characters, and the computed time response could be displayed in less than four seconds real-time. A closely coupled third-order system might require about seven seconds to set up.

In the present version of the analog unit the memory output is wired directly into the transconductor units, as shown in Figure 12. This introduces wires of some two to three feet in length into the integration circuit. The distributed resistance and capacitance of these conductors is not negligible, and degrades accuracy considerably. Some tests which used the memory to set closely coupled transconductor relays (i.e., relays mounted right in the analog units) have indicated that excellent accuracy can be obtained by this modification.



INPUT	DATA BITS	OUTPUT
VOLTAGE	SWITCH POSITIONS	CURRENT, i
s	0 000 000 000	0 s
s	1 000 000 001	-1 s
s	0 000 000 011	3 s
s	1 110 000 000	-768 s

Figure 12. Technique Used to Set Analog Coefficients

3.3 DISPLAY GENERATION

The equipment used to multiplex the four analog signals for display is a standard Philbrick CR and CS display package[3]. This equipment superimposes the four input signals on a time-voltage grid, generates synchronized computing control signals, and displays the results on an ordinary single-beam oscilloscope.

In the absence of such display equipment it is possible to design one's own computing control and display unit, and feed the results into a standard oscilloscope. In this latter case, the time and voltage line would probably be replaced by the standard scope grid, and some simple manual calibration of the display would be necessary.

REFERENCES

1. Technical Manual, Model 35 Keyboard Send-Receive (KSR) Teletypewriter Set, Bulletin 281B, Vol. 1, Teletype Corporation, Skokie, Illinois, 1963

2. Instruction Manual for 200-KC- S-PAC Digital Modules, Computer Control Company, Inc., Framingham, Massachusetts, August 1963

3. Philbrick Analog Applications Sheets — K5-U, KS-M, RC, CR, CS, R-500, G. A. Philbrick Researches, Inc., Allied Drive, Dedham, Massachusetts

4. Paynter, H.M. and J. Suez, "Automatic Digital Setup and Scaling of Analog Computers," ISA Transactions, January 1964, pages 55-64

5. Rosenberg, R. C., Computer-Aided Teaching of Dynamic System Behavior, PhD. Thesis, M.I.T. Mechanical Engineering Department, September 1965

APPENDIX A

SOME COST INFORMATION FOR NON-STANDARD EQUIPMENT

1. Memory Words - 34 units

Reed switches and coils	$ 813.00	
Lights and clips	264.50	
Circuit components	473.20	
Connectors	266.00	
Fabrication of chasses	271.50	
Printed circuit boards (drilled)	217.30	
Miscellaneous hardware	102.50	
TOTAL		$2,407.50 *
Approximate cost per bit (34 at 10 = 340 bits)	$ 7.06	

2. Logic Unit

Standard CCC components and mounting racks	$1,300.75 *

3. Power Supplies (2) $ 235.04 *

TOTAL $3,943.29 *

* Exclusive of labor for assembly of components.

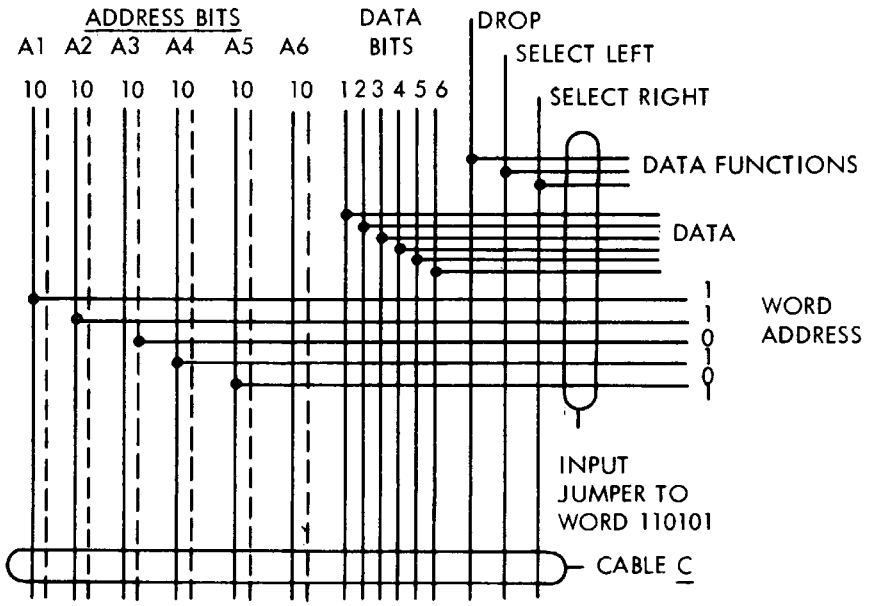
APPENDIX B

LIST OF CABLE FUNCTIONS

CABLE FUNCTION SUMMARY LIST

Cable	No. Lines	Signal Information
A	8	Six input character bits, cycle switch
B	8	Continuation of cable A
C	21	Six address bits; six address complements; six data bits; drop, select left, select right
D	21 + 3	Same signals as C, plus +6V, - 18V gnd
E	12	Common pole connection; + and - sign bits; nine data bits
F	7	Analog unit power (± 30V, ±300V, 6.3 VAC, gnd)
G	5	Four analog output signals; relay control
H	4	Horizontal and vertical sweeps; flyback suppress; ground

DETAIL OF MEMORY CABLE C



* See Figure 3 for reference.

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14. KEY WORDS

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Machine-aided cognition
Multiple-access computers
On-line computers
Real-time computers
Remote terminals
Time-sharing
Time-shared computers

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