PDP-1 COMPUTER
ELECTRICAL ENGINEERING DEPARTMENT
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PDP-32

TX-0/PDP-1 DATA LINK

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A parallel 18-bit, two way data link has been installed between the TX-0 live register and the PDP-1 external register to provide a means of transferring information to and from the two computers. The facilities of both computers are thus made available to a user.

To use this link facility in the PDP-1, external equipment level 1 must be assigned to the user. This link may be requested by the following instructions:

in the source program - law flexo q1
arq
or in ID, before running the program - q1F

If the level is assigned, the instruction following the arq will be skipped (in program) or an extra carriage return will be given (in ID). [See in-out assignment memo 31.]

~~The instructions controlling the link will be illegal if executed in the PDP-1 when the external equipment level 1 is not assigned to the user.~~

Interrupts/branching is determined by the control flip-flop "link" instructions explained on the next page:

TX-0:

opr 17000 (ex7)	set link flip-flop. "1" → FF
opr 1x000 (ex-x)	transfer the contents of the external register of the PDP-1 to the live register of the TX-0. C(ext. reg.)→C(lr)
540000 (tlv)	test link flip-flop. This instruction can be made to skip either on flip-flop set ("1") or cleared ("0") for a faster loop.

PDP-1:

iot 611x *	test the link flip-flop; if it is set, the instruction following the iot 611x is skipped.
iot 621x *	clear the link flip-flop. ("0" → FF)
iot 631x *	transfer the contents of the live register to the external register, if the latter is assigned. Otherwise, the contents of the live register are transferred to the in-out register. C(lr) → C(ext. reg.) / if ext. reg. assigned. C(lr) → C(io) / if ext. reg. not assigned.

* The "x" in the instruction indicated that this digit is not decoded; thus, it can be any number 0-7.

Use with PDP-1 New Mode Sequence Break System:

In new mode sequence break, the link is assigned to channel 1. If channel 2 is enabled when the computer is in sequence break mode and the new mode is one, then when the link flip-flop is set ("1" → FF), a break will occur in the main program to service the link. (See New Mode Sequence Break memo, PDP-26.)