

Division 8 — Lincoln Laboratory  
Massachusetts Institute of Technology  
Lexington 73, Massachusetts

SUBJECT: TX-0 Circuitry

To: K. H. Olsen

From: J. R. Fadiman

Date: October 22, 1956

Approved: K. Olsen  
K. H. Olsen

**Abstract:** The high speed logical circuitry used in the TX-0 transistor computer uses Philco 5122 Surface Barrier transistors. AND and OR gates are formed from inverter or emitter follower combinations. The cascode configuration is used as a power amplifier for fast rise and fall times. Timing pulses are generated by vacuum tubes, and gated on and off by a register driver circuit. Marginal checking is accomplished by varying a positive base bias voltage. The TX-0 flip-flop is a high-speed flip-flop package using 10 SETs and capable of 5 mps operation.

I. Introduction

A. The high speed circuitry for the TX-0 computer uses the Philco 5122 Surface Barrier transistor. The two logical levels are ground and -3 volts. Pulses are negative, with an amplitude of -3 volts and a width of from 80 to 100 mu sec. The supply voltages used for the SBT circuitry are -3, -10 and +10 volts.

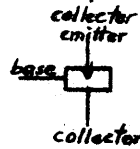
B. Symbols (Note)

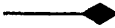
The following symbols are used.


Transistor (in circuit schematics)





Transistor (in block schematics)



-3 volt level 

Ground level 

Negative pulse (ground to -3 volts) 

Positive pulse (-3 volts to ground) 

-3 volt supply 

ground 

-10 volt supply 

+10 volt supply 

Note 1: For detailed considerations of transistor logic and symbology, refer to: 6M-4571, by R. C. Jeffrey.

The logical circuitry for the central machine is constructed out of small plug-in units, each containing one, two, or three transistors and associated components. The types of units and their functions are listed below. The schematic circuit diagrams are in figure 1 and detailed descriptions are in the appendix.

<u>Unit</u>	<u>Transistor</u>	<u>Use</u>
P	1 SBT	Pulse input gate to flip-flop
L	1 SBT	Level input gate and inverter
M	1 SBT	Level input gate with high positive bias
R	1 SBT	Register driver inverter
S	1 SBT	Steering gate
T	1 SBT	Single transistor for single emitter-follower
E	2 SBT	Two emitter followers with separate outputs
A	3 SBT	Three emitter followers with a common output
C	2 SBT	Cascode Circuit
F	1 GE4JDLA17	Ferranti Circuit
F (Mod II)	1 GE4JDLA17	Ferranti Circuit
B	None	Emitter bias for register driver
G	1 GE4JDLA17	Indicator light circuit

## II Logic

### A. "AND" and "OR" Gates

The "AND" and "OR" gates for TX-0 are either emitter followers in parallel or inverters in series or parallel. The AND gate for ground level in, ground level out is emitter followers in parallel as shown in Fig. 2. Because of the restrictions of speed for 5 mcps circuits, a maximum of 10 emitter followers may be placed in parallel in this fashion, providing up to a 10-way AND gate. An inverting AND gate for ground level in, -3 level out is shown in Fig. 3. Because of limitations of speed, only two inverters may be placed in parallel. The capacitance to ground goes up as  $\beta C_c$  where  $C_c$  is the collector capacitance of an off transistor and  $\beta$  is the current gain of the transistor, grounded emitter. The inverting OR gate for ground level in, -3 level out is shown in Fig. 4. Because there is a finite voltage drop across a saturated transistor, (about 0.1 volt), only two inverters may be placed in series in this manner.

### B. Inverter Circuit

For the inverter circuit (Fig. 5) the values of the input resistance and positive bias resistance are so calculated that there is safety margin when the transistor is saturated and when it is cut-off. This insures maximum noise rejection and tolerance to signal variation. It is assumed on the basis of several tests that no transistor will have a  $\beta$  of less than 5 at 5.5 ma. collector current. (Our minimum acceptance  $\beta$  at low current is 15, and 11 at end of life). A larger amount of positive bias is used on inverter input gates to flip-flops when the input is from a distant frame, such as from core memory, toggle switch storage, or the photo-electric tape reader. In these cases the induced noise voltages are apt to be larger than usual, and the input impedance to the flip-flop is sufficiently high to allow the use of the larger positive bias current, and consequently smaller input base current.

This bias is also used in cases where the ground level for the emitter is supplied from an emitter follower gate. Such a level goes

0.3 volt positive and thus it is necessary for the base to be held at about +0.5 volts to provide adequate margins during cut-off.

All of the inverters in TX-0 use a supply voltage of -10 volts. However, the actual voltage at the collector never exceeds -4 volts, since it is clamped, either by an emitter follower following it, or by a voltage divider to ground. A single inverter provides current sufficient for driving three emitter followers or two inverters. It can drive a capacitance of 75 uuf, with a fall time of 0.1  $\mu$  sec.

#### C. Emitter Follower Circuit

The logical circuitry utilizes a combination of inverters and emitter followers which in general are alternated. This ensures that when an emitter follower is turned on, it is always kept in saturation since its base is returned effectively to -10 volts through the load resistor of the previous inverter. The difference in driving capabilities of the saturated and non-saturated emitter follower is shown in the graph of Fig. 6. The load resistance of the emitter follower is returned to +10 volts instead of to ground to shorten the rise time of the emitter follower. This emitter follower will provide 8 ma. of output current at -3 volts and will drive a capacitive load of 120 uuf, with a rise time of 0.1  $\mu$  sec.

#### D. Cascode Circuit

In order to achieve faster rise and fall times and greater driving ability than is possible with either the emitter follower or the inverter, the "cascode" circuit is used. The logical and circuit schematics are shown in Fig. 7. The inputs to  $Q_2$  and  $Q_3$  are always opposite in phase so that in the steady state case only one transistor is conducting.  $Q_3$  acts as an emitter follower which provides the driving current and pulls the input quickly down to -3 volts.  $Q_2$  acts as an inverter whose function is to pull the output quickly up to ground during the transition. Thus, the circuit utilizes the fast rise time of the inverter and the fast fall time of the emitter follower.

This configuration is capable of driving a capacitive load of 420 uuf. with a transition time of 0.1  $\mu$  sec. No power is wasted in load resistances, and this circuit is designed to provide 12 ma. output current at -3 volts. It will drive 12 emitter followers or 8 inverter bases, and one emitter of an inverter. TX-0 uses the cascode as the output stage of all flip-flops, as a power amplifier for driving many transistor bases, and as a cable driver.

Cascode cable drivers are used when sending levels to the memory over 160 ohm coaxial cable. The cable is terminated at the input end by a resistance in series with the cable. This series termination is possible because, unlike the emitter follower or inverter, the cascode circuit looks like a very low impedance (less than 10 ohms) when driving in either direction. Thus, the driven end of the cable is properly terminated at all times.

### III Pulse Circuitry

#### A. Timing Pulses

The timing pulses for the computer are generated by vacuum tubes. Thirty volt positive pulses are sent to the computer through 93 ohm coaxial cables. 7:1 pulse transformers with a one turn secondary are used at the computer to provide approximately 3.4 volt negative pulses. A 1N283 diode is used across the primary in order to damp the overshoot.

#### B. Register Driver

Gated register drivers (Figures 8 and 9) supply the 3 volt negative pulses to the input gates of the flip-flops. The pulse input is at the collector of  $Q_3$  and the output is from the emitter. A pulse is passed when  $Q_3$  is saturated from the negative output of inverters  $Q_1$  and  $Q_2$ . Thus, a ground input to either  $Q_1$  or  $Q_2$  is necessary to pass a pulse through the register driver. The two inverters in series thus give a two-way OR circuit for the pulses. Up to a 10 way OR circuit can be constructed by paralleling register drivers with a common pulse input and output but different gating. In order to form an AND circuit for pulses, emitter follower gates are

placed in parallel to feed the inputs of the inverters. All the inputs must be at ground to pass a pulse. The pulse output of the register driver closely follows the pulse input. The maximum pulse current is 30 ma., sufficient for driving 10 pulses bases, and the pulse voltage drop through the register driver is less than 0.5 volt.

### C. Pulse Inputs to Flip-Flops

In order to set or clear the TX-0 flip-flop the "one" or "zero" input must be brought up to ground by the output of a pulse inverter. Up to 15 such inputs may be tied in parallel to one side of the flip-flop. The negative pulse is inverted and gated by a circuit such as this: Fig. 10. Or, alternately, only one transistor may be used as a gate in this manner: Fig. 11. Here a ground level must be supplied to the emitter in order to pass the pulse. This arrangement requires a level current equal to  $\frac{I_c}{\alpha}$  while the two transistor gate requires a level current equal only to  $\frac{I_c}{\beta} = \frac{I_c}{\alpha} (1-\alpha)$ . In order to complement the flip-flop, the pulse must be steered to the proper side of the flip-flop. The circuit which does this is shown symbolically in Fig. 12.

### IV Marginal Checking

Marginal checking of all TX-0 circuitry is accomplished by varying the +10 voltage on the base of the inverter transistors. Increasing this positive bias supply effectively reduces the negative base current into the transistor and tends to bring it out of saturation. Making the positive bias supply negative tends to allow the transistor to conduct when it should be held cut off. Emitter followers are not directly marginal checked, but their condition can be investigated by marginal checking the inverters which proceed and follow it. For these inverters normal margins are slightly greater than  $\pm 10$  volts either side of the normal +10 volt supply.

### V Flip-Flop

The TX-0 flip-flop is shown in Fig. 13. The circuitry is similar to that already described, with RC coupling between inverters, positive bias, and emitter follower clamping.  $Q_1$  and  $Q_2$  are pulse amplifiers

which are normally conducting and are cut off by the positive input pulse at the "zero" or "one" input.  $Q_3$  and  $Q_4$  are the flip-flop transistors themselves which are arranged in a conventional RC-coupled Eccles-Jordan trigger circuit. When an input pulse cuts off  $Q_1$  or  $Q_2$  this opens the emitter circuit of  $Q_3$  or  $Q_4$ , and changes the state of the flip-flop.  $Q_5$  and  $Q_6$  are inverters which are used to saturate the emitter followers of the output cascode.  $Q_7$  and  $Q_8$ , and  $Q_9$  and  $Q_{10}$  form the cascode circuits on the "one" and "zero" sides respectively. Their operation is the same as that previously described for the cascode circuit, with the opposite phases being obtained from the inverters on opposite sides of the flip-flop.

The output wave form at 10 mcps is shown in Fig. 14, and various marginal checking curves and output characteristics of the flip-flop are shown in Figs. 15 through 22.

J. R. Fadinan  
J. R. Fadinan

Attachments:

Fig. 1: SA-65640-3  
Figs. 2 through 12  
Fig. 13: D-63369  
Fig. 14: A-65366  
Fig. 15: A-67294  
Fig. 16: B-65729  
Fig. 17: B-65721  
Fig. 18: B-65720  
Fig. 19: B-65719  
Fig. 20: B-65727  
Fig. 21: B-65717  
Fig. 22: B-65718

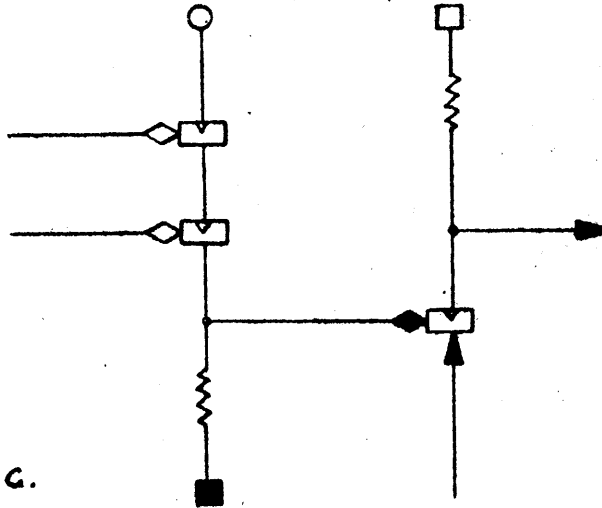
Appendix (15 pages)



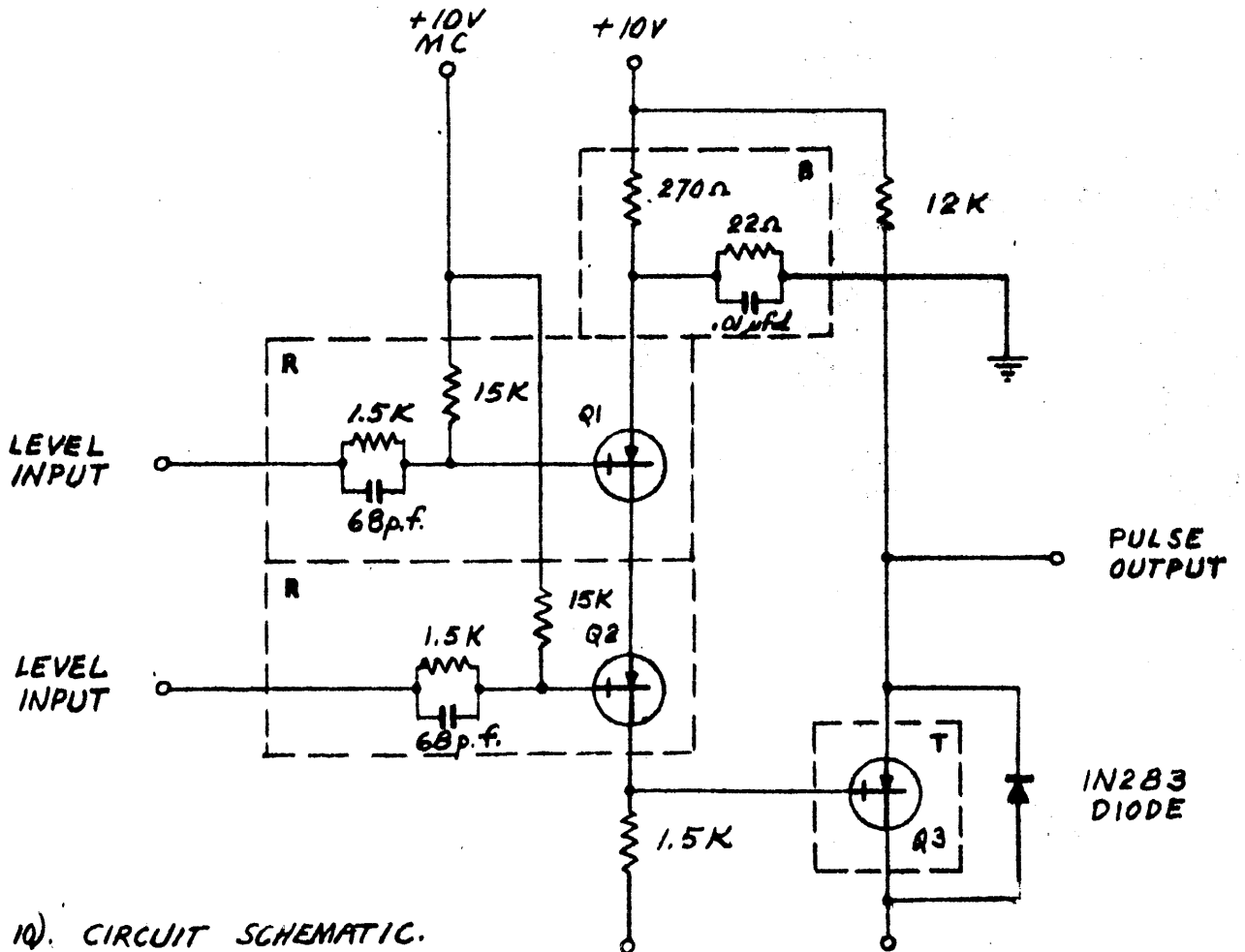
Register Driver

- 1) Use: Gating circuit for pulses for pulse inputs to flip-flops.
- 2) Level input: Ground level for passing pulse. -3 volt level for no pulse output. Level input current required: 2.2 ma.
- 3) Pulse input: -3.4 volt 80 to 100 msec pulse. Input pulse current equal to output pulse current.
- 4) Output: -3 volt 80 to 100 msec. pulse. Pulse amplitude equals input amplitude minus transistor drop. Drop less than 0.5 volt.  
Maximum pulse current: 30 ma. Can drive maximum of 10 pulse bases.  
Set-up delay: about 20 msec.
- 5) Restrictions: Two register drivers driven from the same input gate will drive maximum of 20 bases. Up to 10 register drivers may be placed in parallel with different gating to form a 10-way OR circuit for pulses. Placing up to 10 emitter follower gates in parallel before the register driver gives a 10-way AND circuit for pulses.
- 6) Power required: 6.6 ma. at -10 v.  
35 ma. at +10 v.
- 7) Marginal Checking: Vary +10 volt positive bias on inverter bases.
- 8) Plug-in units used: 1 or 2 R, B, T or E or A.

REGISTER DRIVER.



9). BLOCK SCHEMATIC.

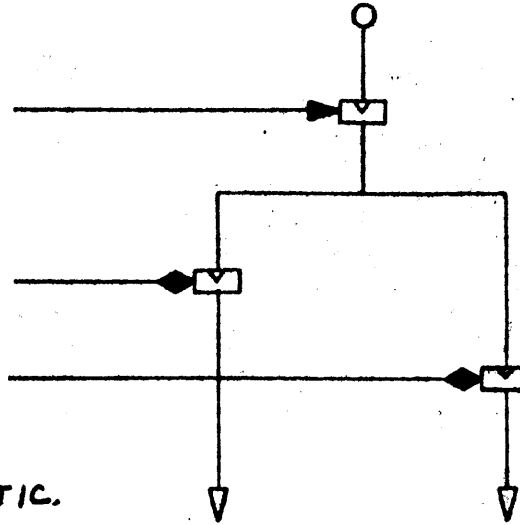


10). CIRCUIT SCHEMATIC.

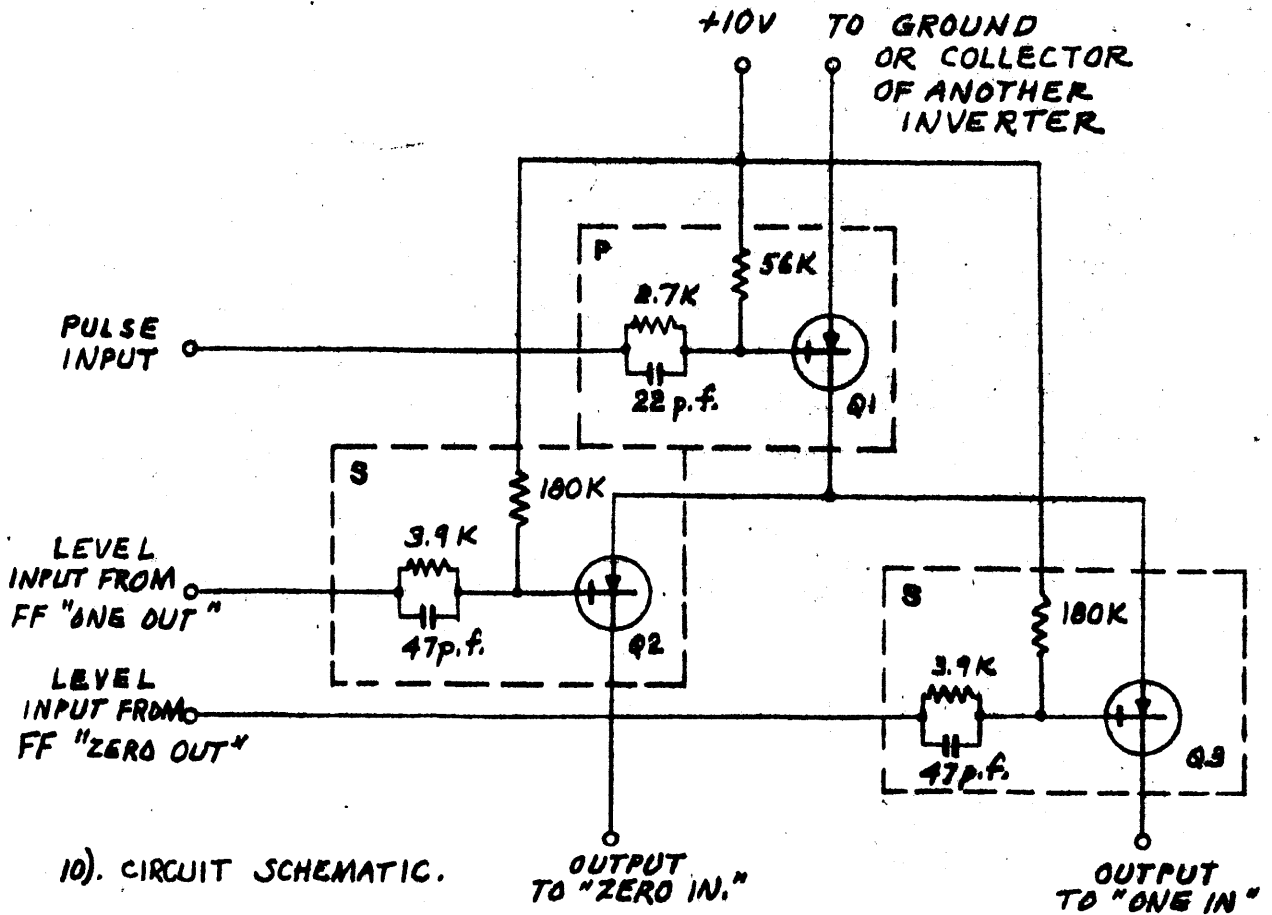
Pulse and Steering Gates

- 1) Use: Provide pulses to complement flip-flop.
- 2) Pulse input: -3 volt 80 to 100 msec. pulse. Pulse current required: Maximum of 3 ma.
- 3) Level inputs: Voltage level at ground on one input, -3 volts on the other, coming from the outputs of the flip-flop to be complemented. Input current required to each base at -3 v.: 0.67 ma.
- 4) Output: Positive pulse up to ground. Will complement one flip-flop.
- 5) Restrictions: There must be no more than 3 transistors in series, including gating level input, pulse input, and steering gate. Up to 15 gates may be placed in parallel on one side of flip-flop input.
- 6) Power required: 0.24 ma. at +10 v.
- 7) Marginal checking: Vary +10 volt positive bias on bases.
- 8) Plug-in units used: 1P, 2S.

PULSE & STEERING GATES.



9). BLOCK SCHEMATIC.



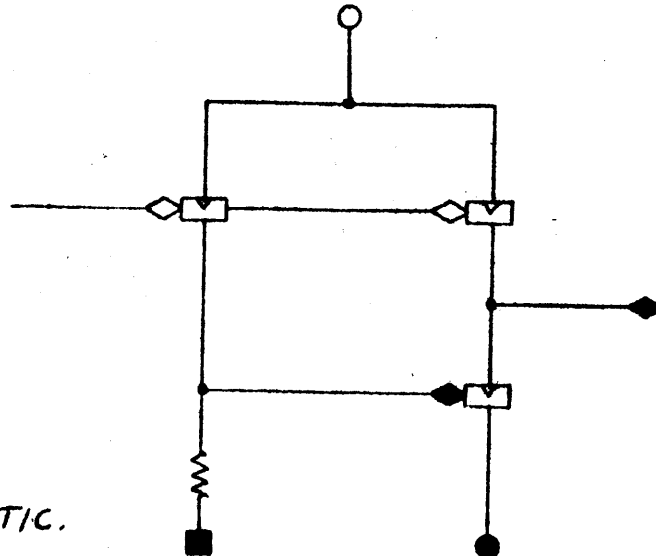
10). CIRCUIT SCHEMATIC.

Inverting Cascode

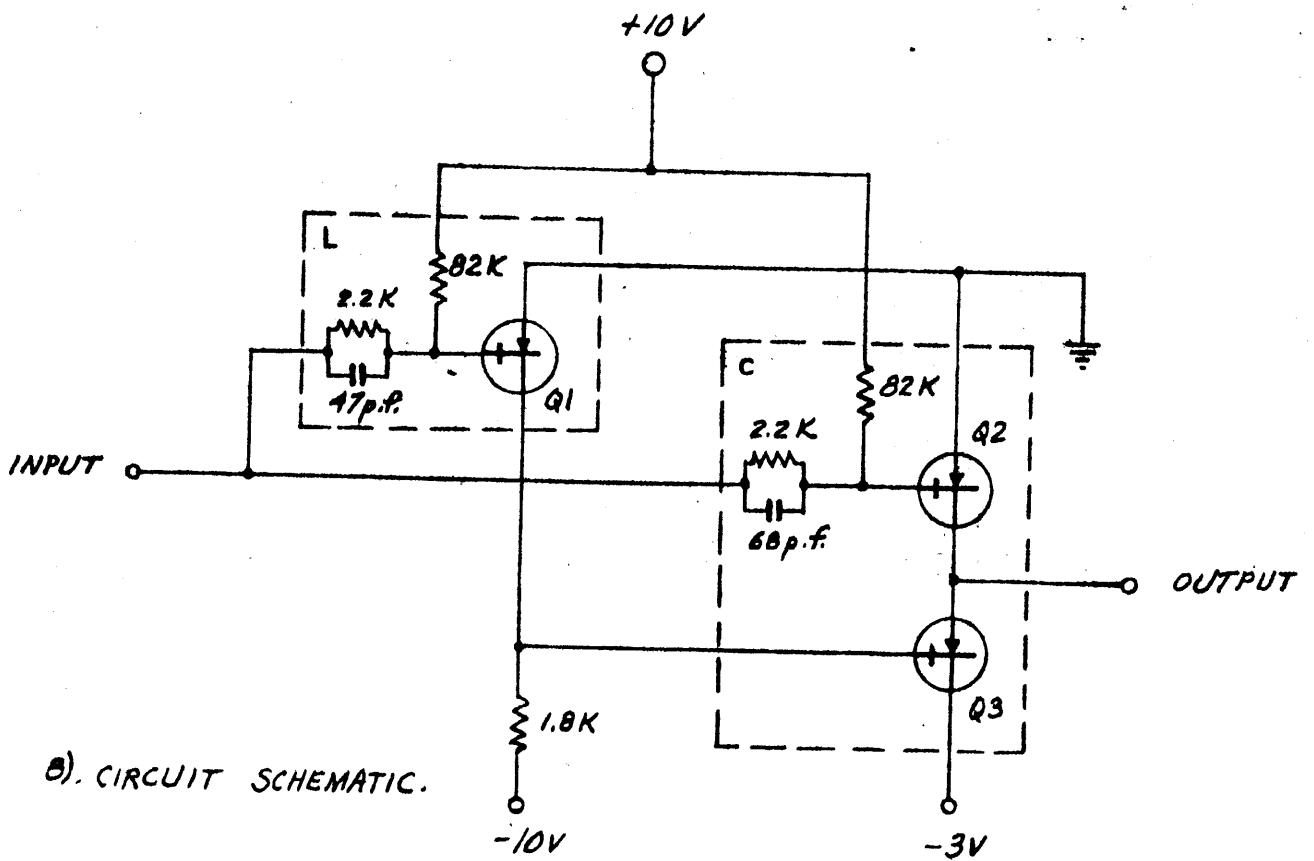
- 1) Uses: Power amplifier and level driver.
- 2) Input: Voltage level at ground or -3 volts. Input current required: 2.2ma.
- 3) Output: Opposite polarity from input. Voltage level at ground or -3 volts. Maximum output current: 12 ma. at -3 v.: 4 ma. at ground level. Can drive maximum of 12 emitter followers or 8 inverters, and one emitter of pulse or level transistor on the same time pulse. Load capacitance for 0.1  $\mu$  sec. rise time: 420 uuf. Delay = 30  $\mu$ sec.
- 4) Power required: 12 ma. at -3 v.  
5.5 ma. at -10v.  
0.24 ma. at +10 v.
- 5) Marginal Checking: Vary +10 volt positive bias on bases.
- 6) Plug-in units used: L,C

INVERTING CASCODE.

7). BLOCK SCHEMATIC.



8). CIRCUIT SCHEMATIC.

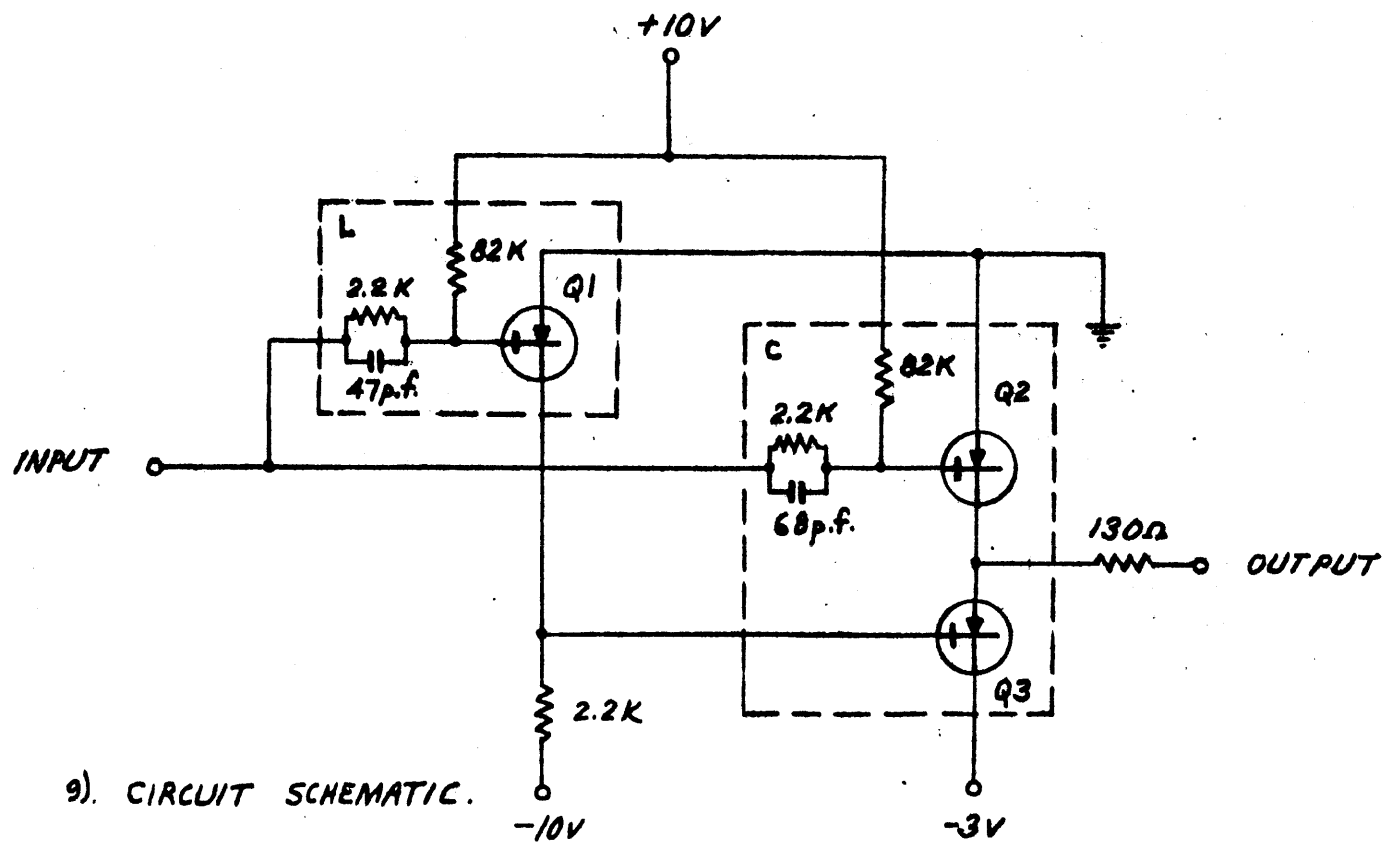
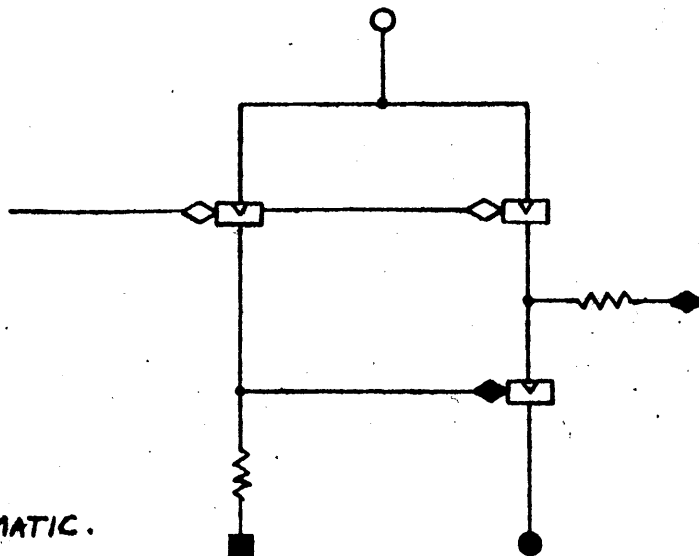


Cable Driver (Inverting Cascode)

- 1) Use: To provide level input into 160 ohm cable, which drives transistor base.
- 2) Input: Voltage level at ground or -3 volts, from emitter follower gate or inverter gate. Input current required: 2.2 ma.
- 3) Output: Opposite polarity from input. Voltage level at ground or negative level less than -3 volts determined by voltage drop through 130 ohm resistor in series with cable. Maximum output current: 12 ma. Will drive maximum of 100 feet of K109 coaxial cable ( $Z_0 = 160$  ohms; D.C. resistance = 0.7 ohms/ft.)
- 4) Restrictions: No termination should be added at end of cable, as cable is terminated in a resistance of 130 ohms in series with the input end at the cable driver.
- 5) Power required: 12 ma at -3 volts.  
5.5 ma. at -10 volts.  
0.24 ma. at +10 v.
- 6) Marginal checking: Vary +10 volt positive bias on bases.
- 7) Plug-in units used: L,C.

### CABLE DRIVER.

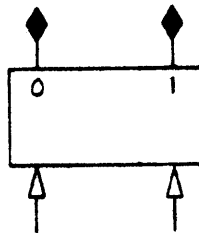
8). BLOCK SCHEMATIC.





Flip-Flop

- 1) Use: To provide logical levels at ground or -3 volts.
- 2) Input: Positive pulse up to ground from output of pulse gate.
- 3) Output: One side at ground: other side at -3 volts.  
Output circuit is inverting cascode. (See Inverting Cascode for specifications) Logical delay before start of rise or fall: 90 to 100 msec.
- 4) Restrictions: Maximum complement rate: 5 mcps.
- 5) Power required: 18 ma. at -3 volts (maximum)  
12 ma. at -10 volts  
1.8 ma. at +10 volts.
- 6) Marginal checking: Vary +10 volt positive bias on inverter bases by varying +10 volt input to "MCA" or "MCB".
- 7) Plug-in unit used: Flip-flop plug-in unit.
- 8) Logical symbol



- 9) Circuit drawing. See Figure 13.

Note on Resistance Values

Inverters

All load resistance to -10 volts are 1.8K, with the following exceptions:

2.2K for inverter in Cable driver cascode, for inverter when followed by two other inverters, and for Accumulator carry chain.

1.5 K for inverters in register drivers.

Normal positive bias resistance for RC input of 2.2 K and 47 uuf is:

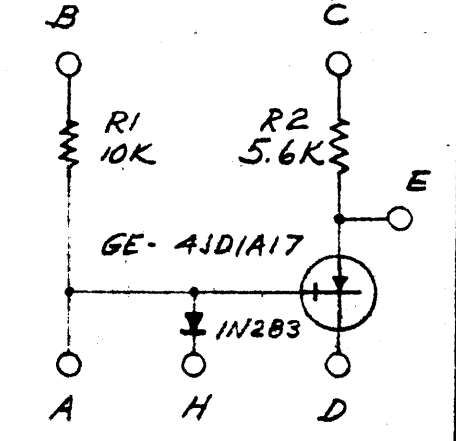
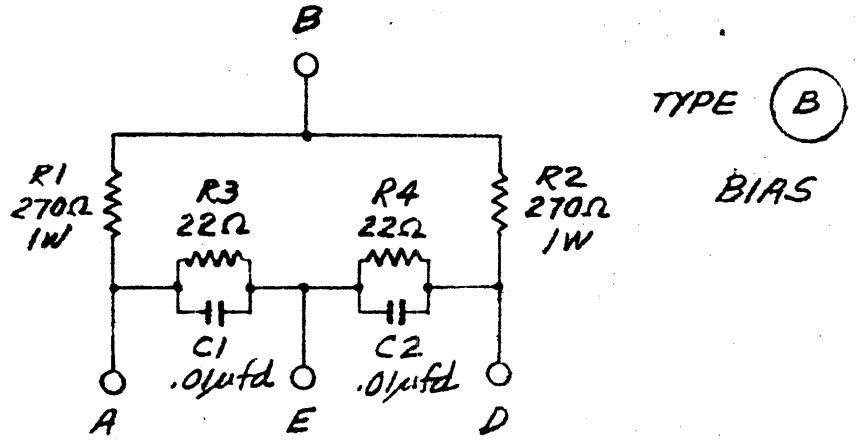
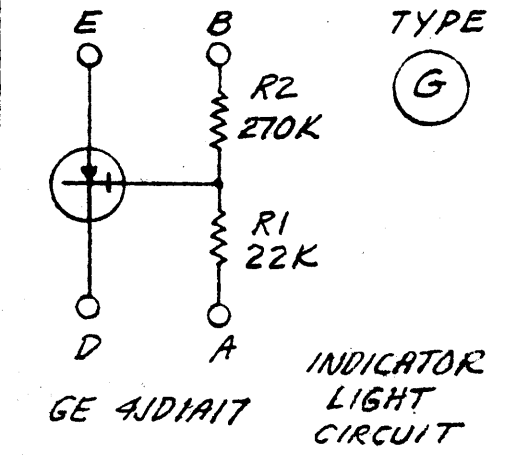
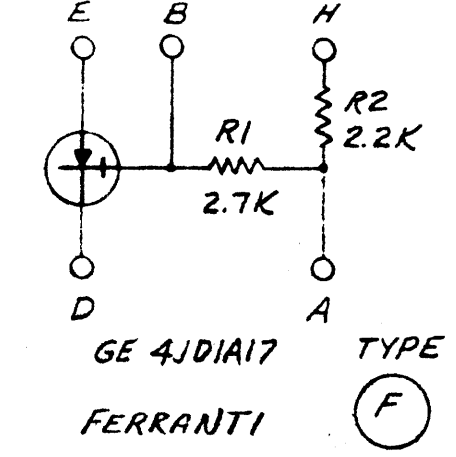
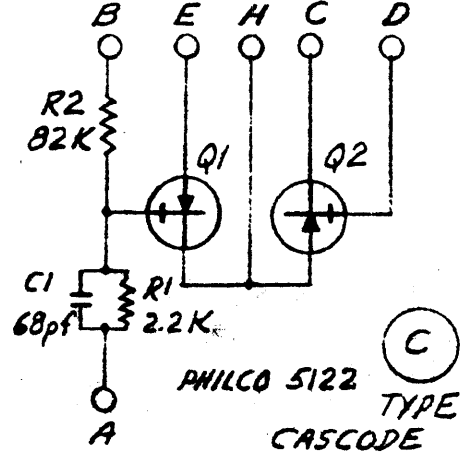
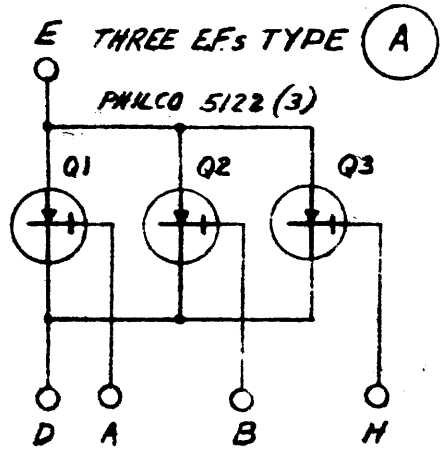
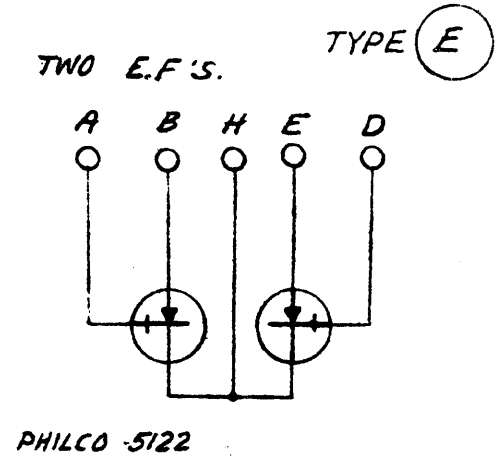
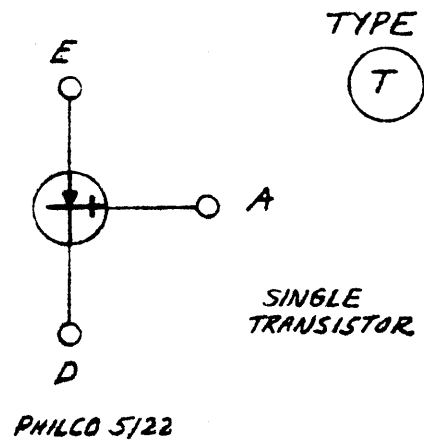
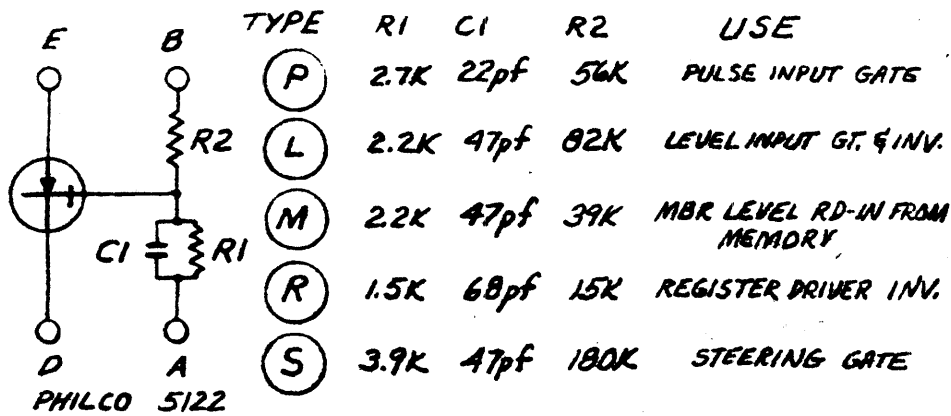
82 K. 39 K is used for level input to MBR from memory frame, toggle switch storage, and PETR, and when the level transistor (L unit) in the Program Counter is driven from emitter followers.

Emitter Followers

All load resistance to +10 volts are 3.9 K with the following exception:

2 K is used when two emitter followers are used in parallel to drive another emitter of a pulse or level transistor. In this case 47 ohm resistors are used in the emitters of the emitter followers as current sharing resistances.

SA 65640-3



"BOTTLED" PLUG-IN UNITS PIN CONNECTIONS. 3-19-56

AND

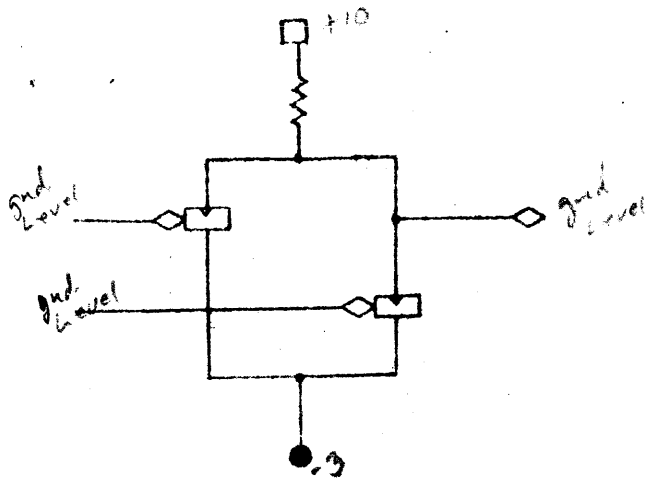


FIG. 2

AND

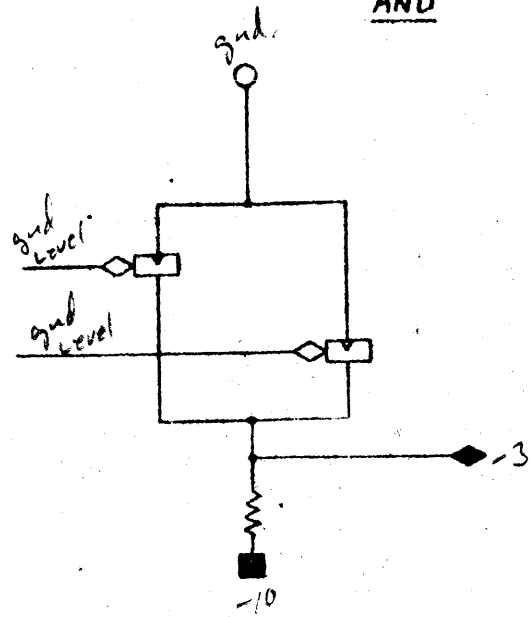


FIG. 3

OR

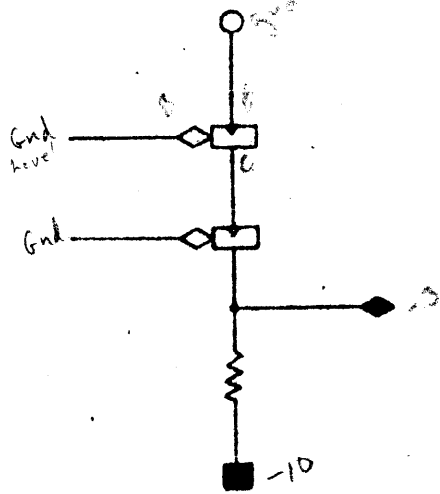


FIG. 4

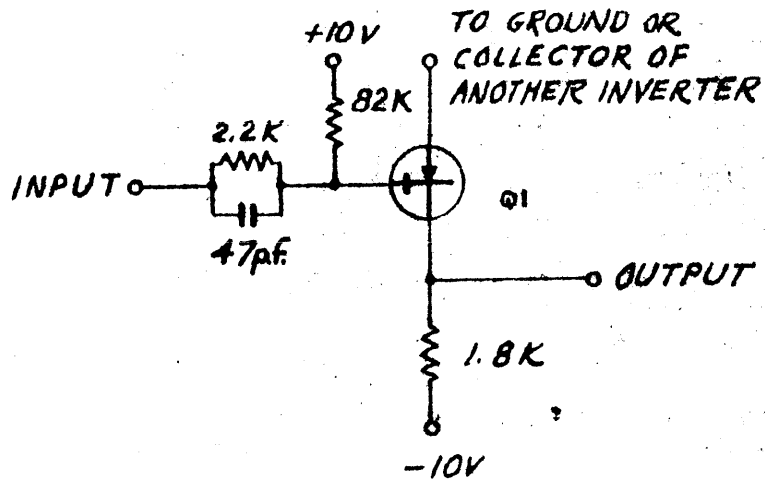
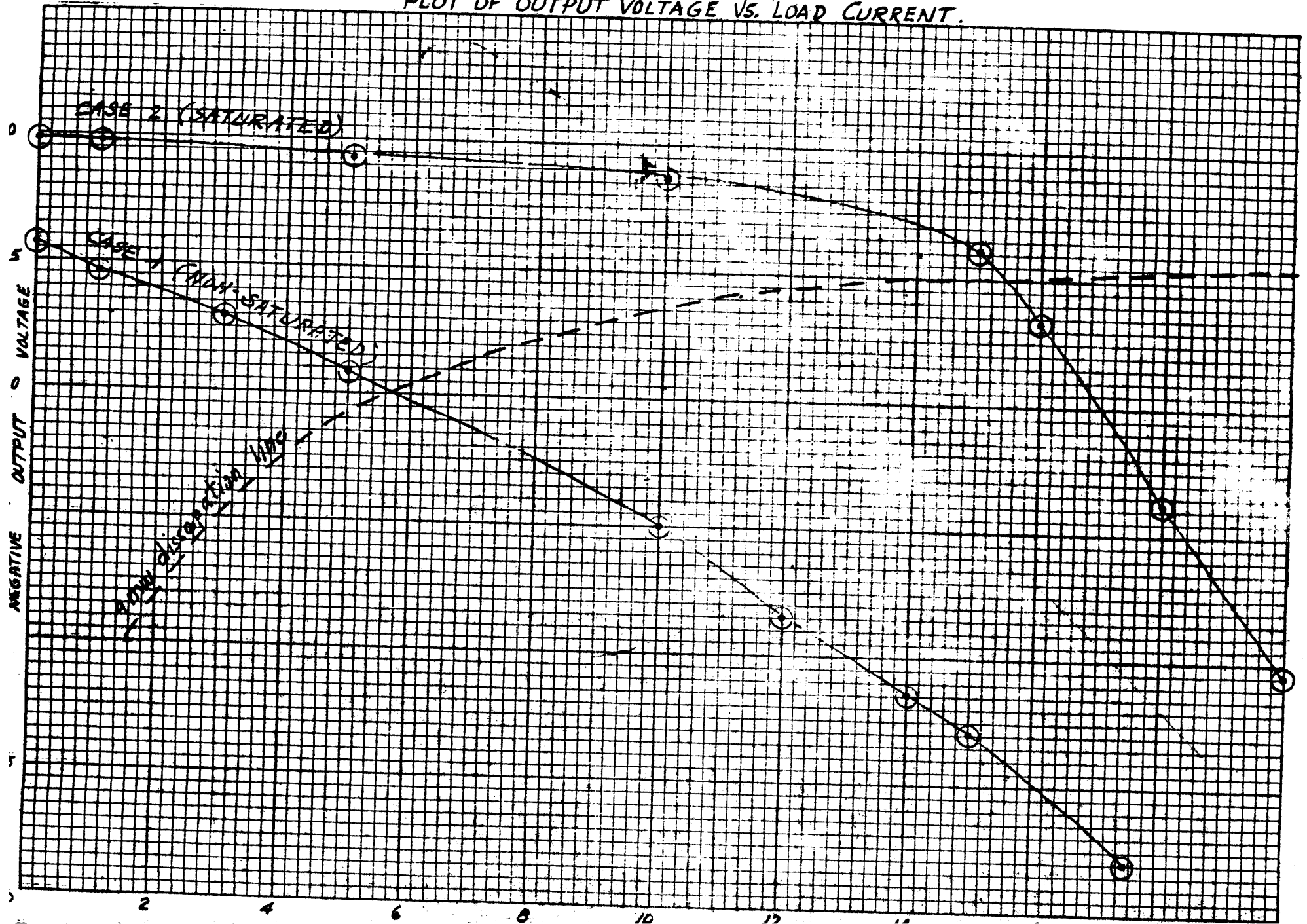
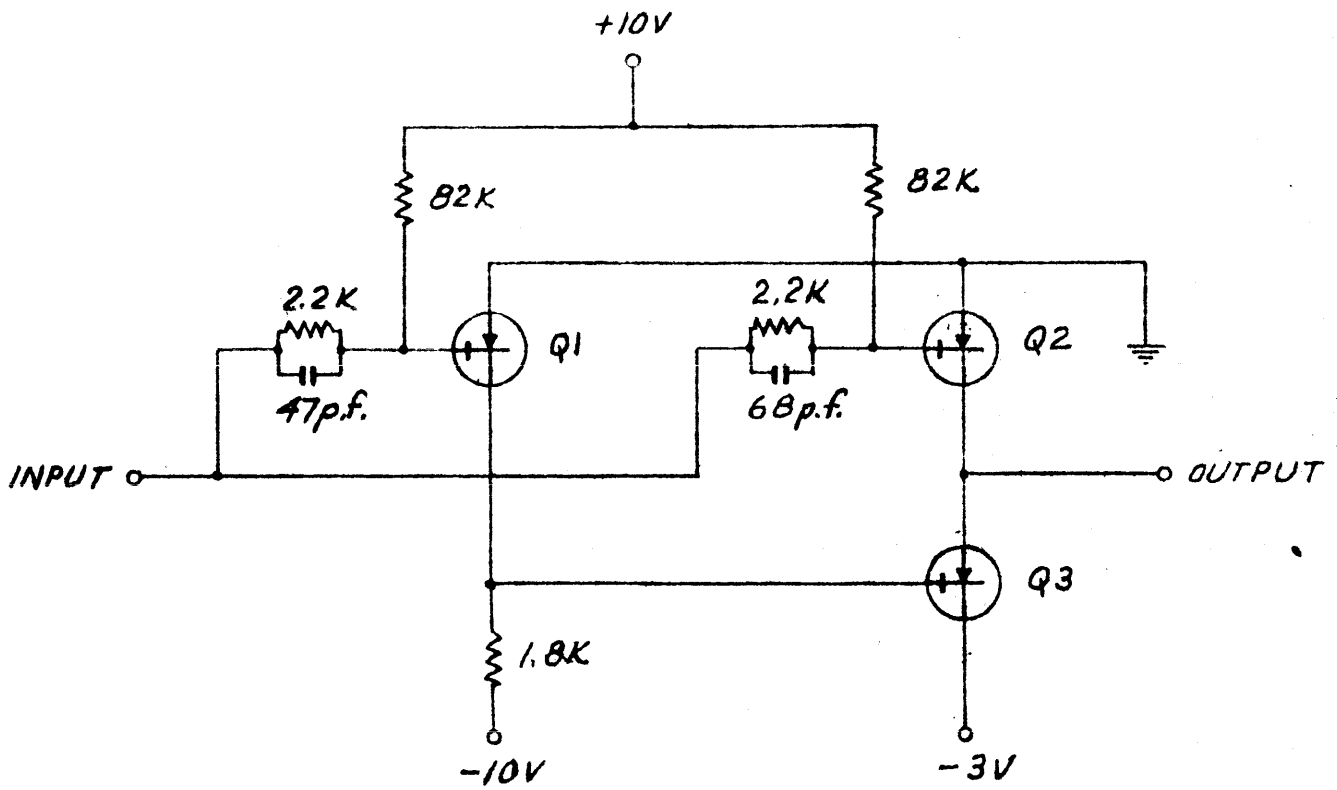
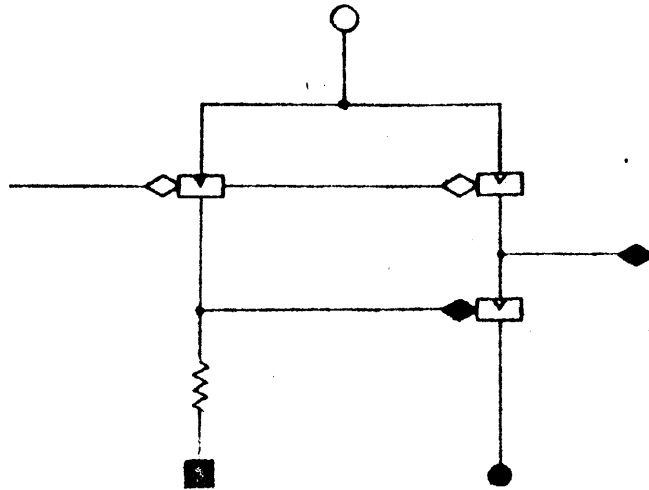


FIG. 5

PLOT OF OUTPUT VOLTAGE VS. LOAD CURRENT.





FIGS. 7

"Cascode" circuit

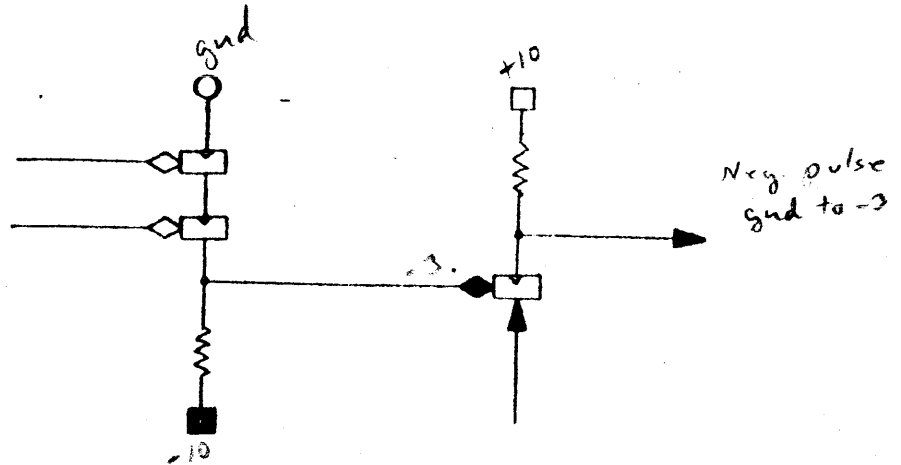


FIG. 8

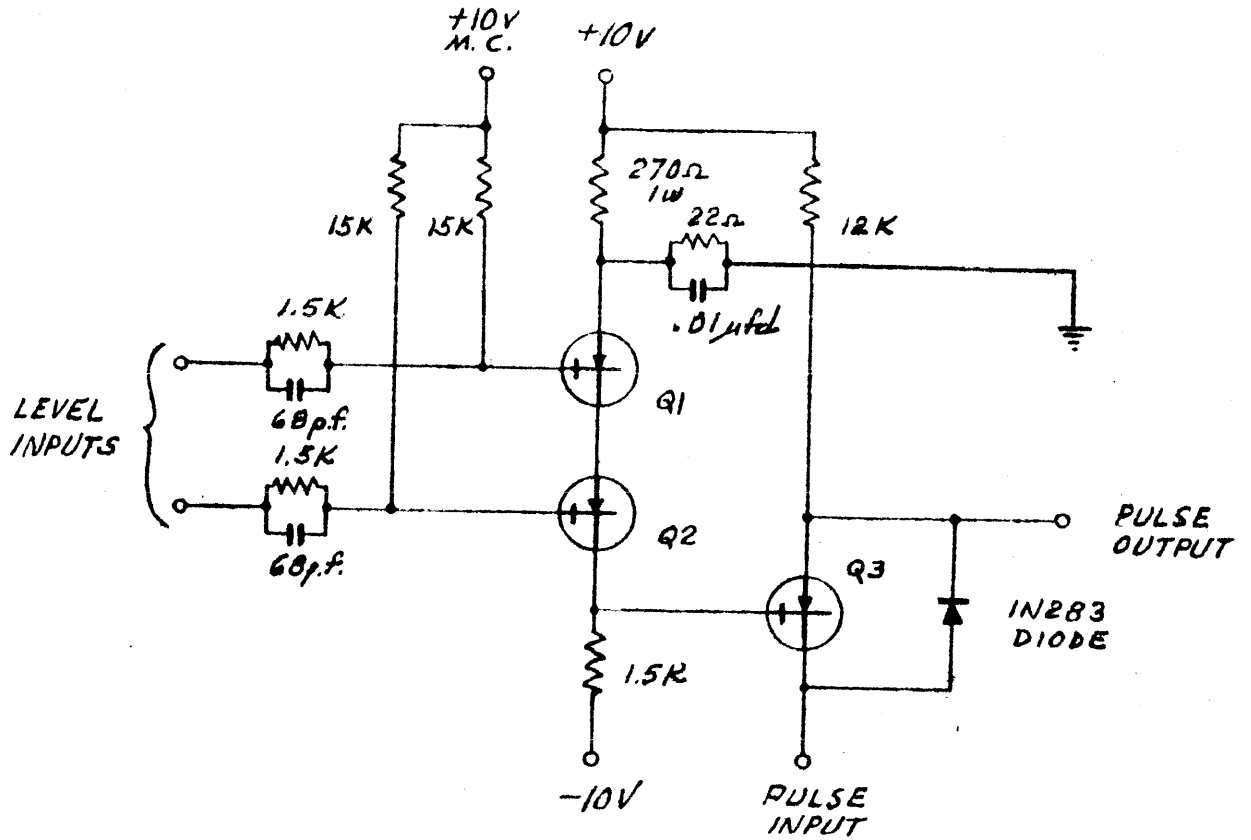


FIG. 9

Register Driver

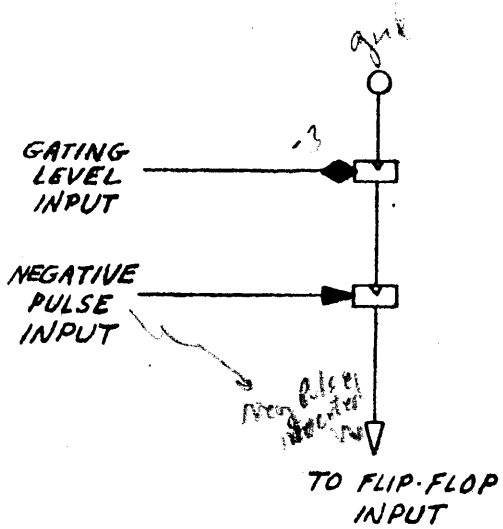


FIG. 10  
Pulse inverter

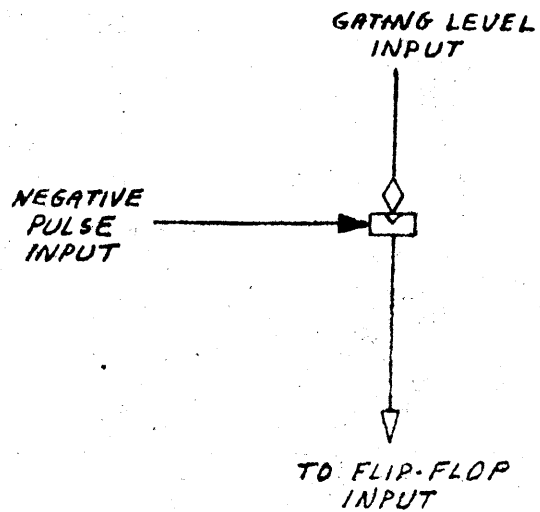


FIG. 11  
Pulse inverter

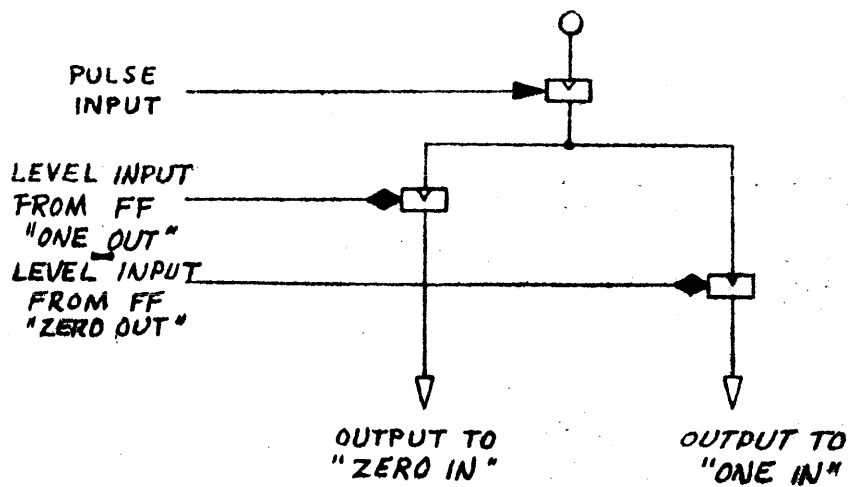


FIG. 12



D-63369  
VG-71  
F-3140  
SN-1328  
F-3181

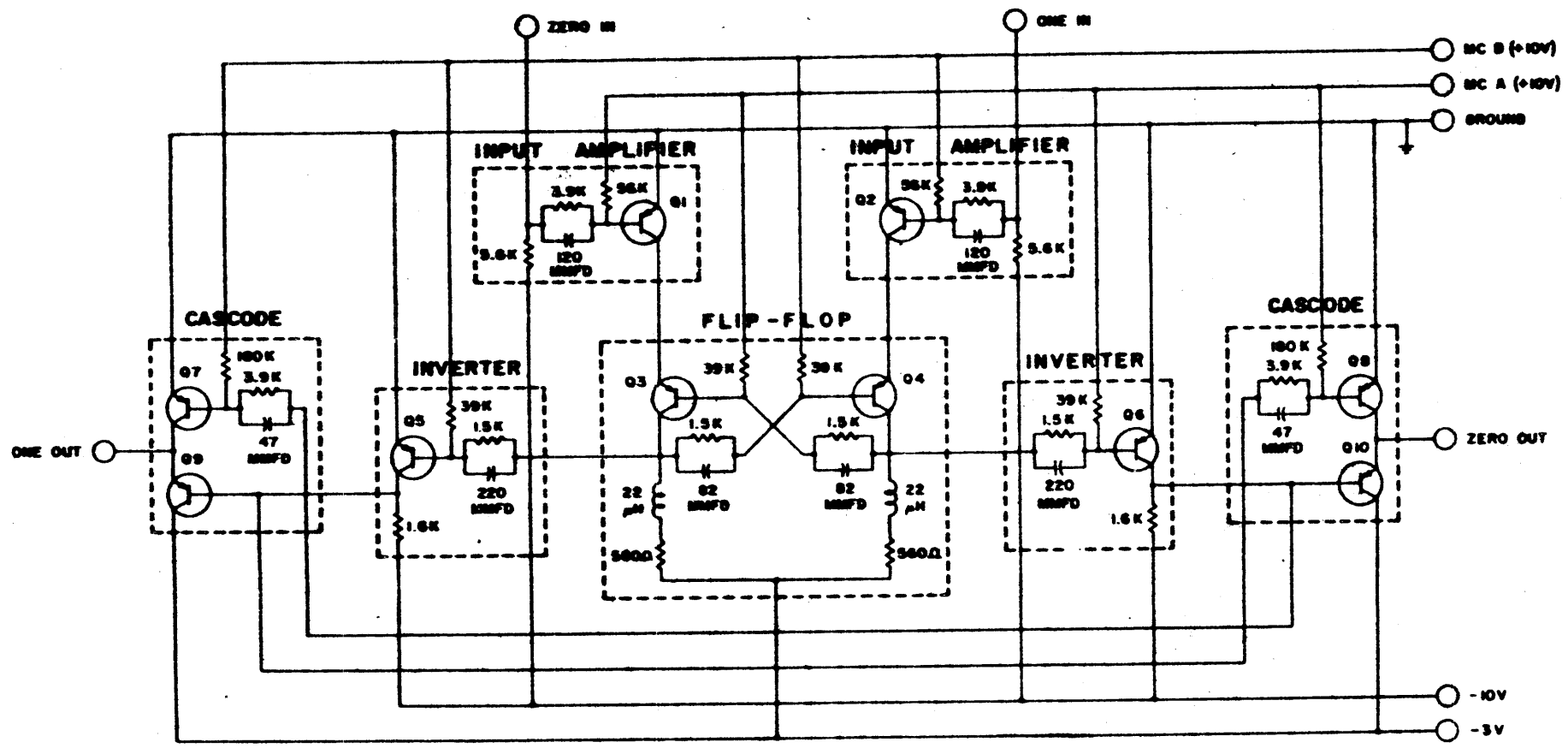
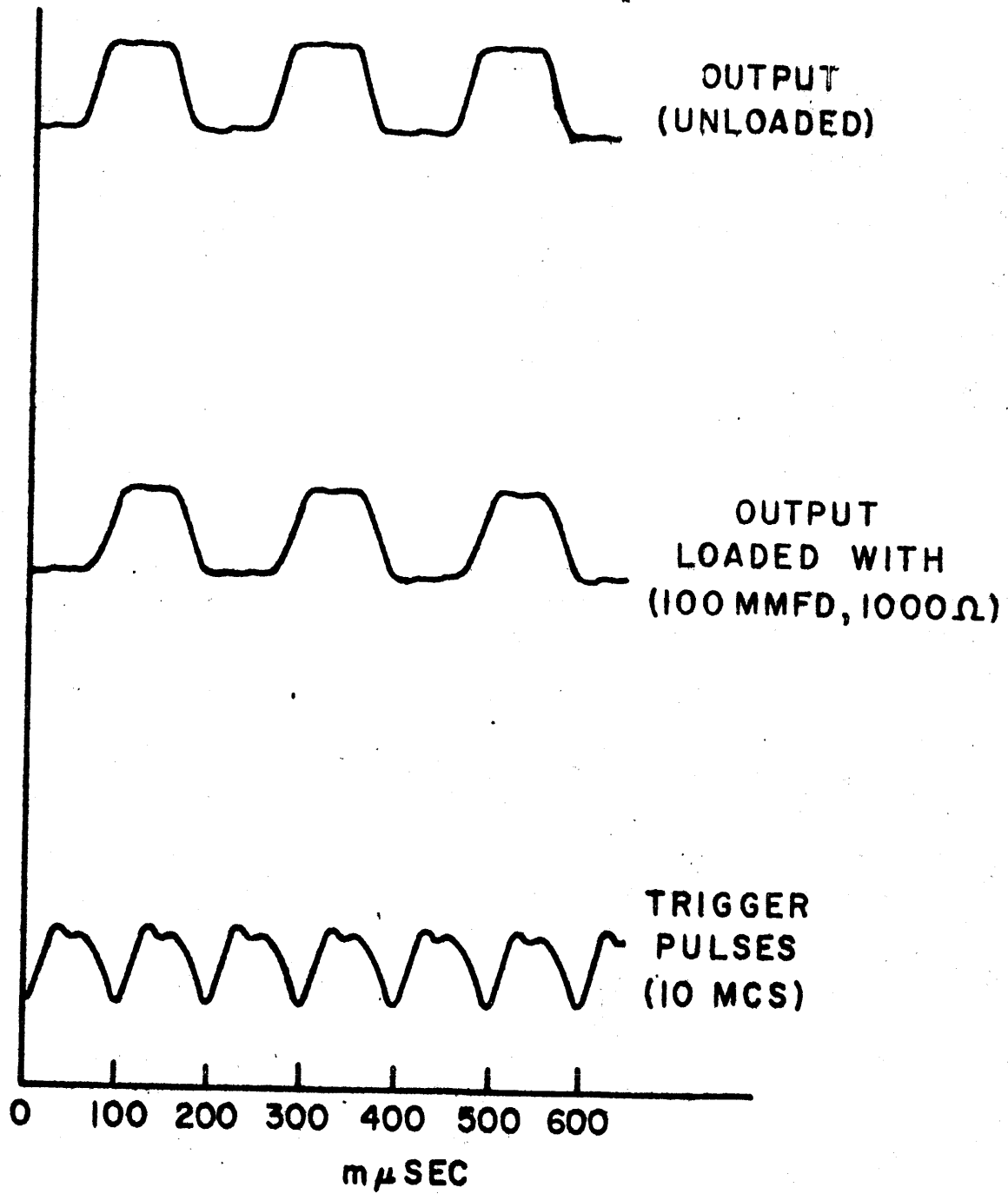


FIG. 13  
TX-0 FLIP-FLOP



TX-0 FLIP-FLOP

A-65366  
VG-82  
SN-1327  
F-3180

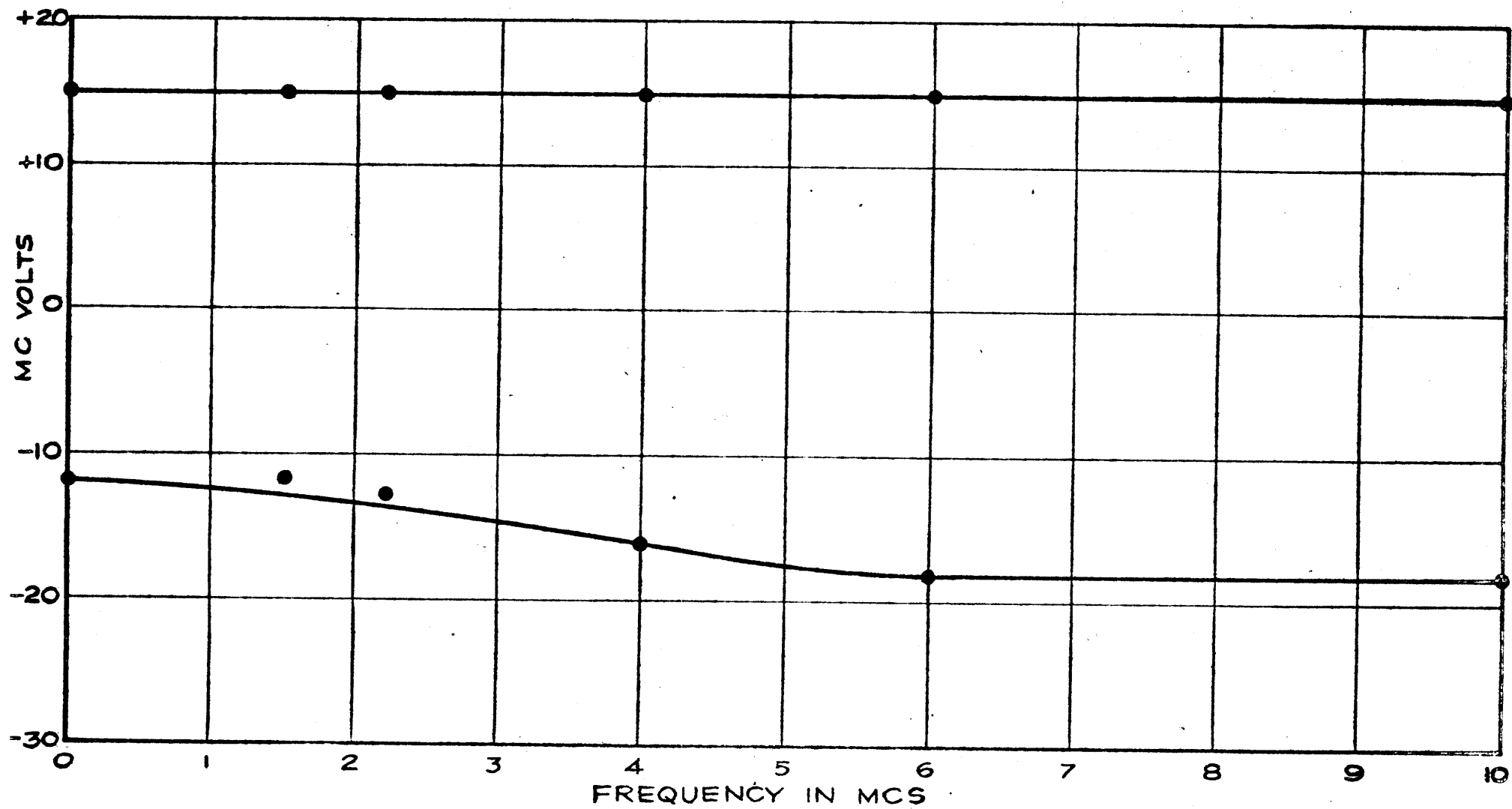
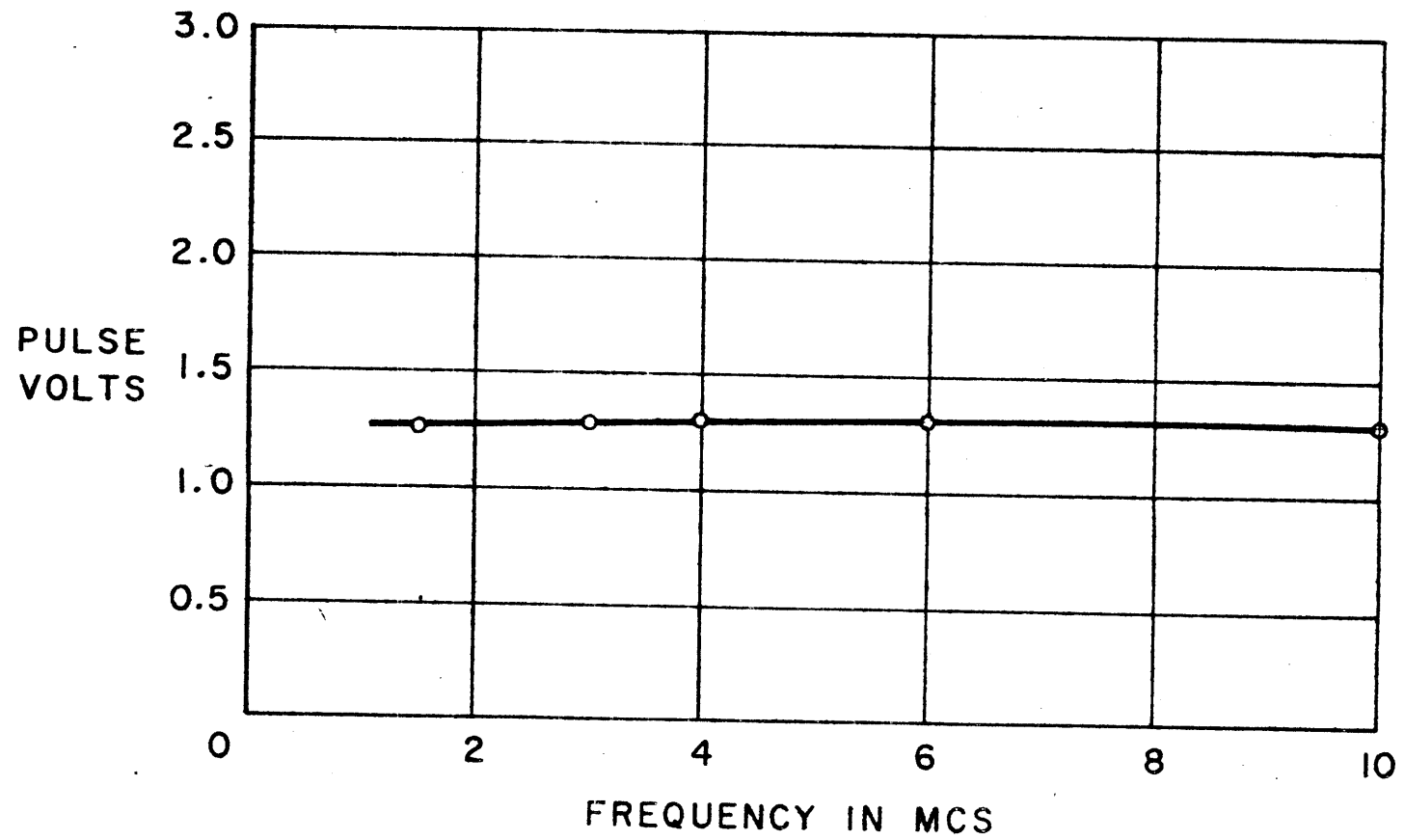


FIG. 15  
FREQUENCY MARGINS

B-65729  
SN-1329  
F-3184



TRIGGER SENSITIVITY