TX-0 COMPUTER
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASSACHUSETTS 02139

M-5001-27-3

THE TX-0 INSTRUCTION CODE

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I. ABBREVIATIONS

AC : ACcumulator
LR : Live Register
PC : Program Counter
PFR : Program Flag Register
PETR: PhotoElectric Tape Reader
TAC : Toggle Switch ACcumulator
TBR : Toggle Switch Buffer Register
LPO : Light Pen FF
LP1 : Light Gun FF

C(AC): "Contents of AC"
$\longrightarrow$: "Replaces"

$\overline{X}$: Complement of X:

X	$\overline{X}$
0	1
1	0

$\supset$: Implies; do y if x is true.
$\wedge$: Intersect; and; logical product.
$\vee$: Union; inclusive or; logical sum.
$\oplus$: Partial add; inequivalence; exclusive or.

mod n: Modulo n ; y = x mod n means x = kn + y for some integer k, $0 \leq k \leq$ n.

x	y	$x \wedge y$	$x \vee y$	$x \oplus y$
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
1	1	1	1	0

INDEX ARITHMETIC

In indexed instructions, the notation "C(y+C(XR))" means: The contents of the register whose address is the sum of y and the contents of the index register. This effective address computation is done with one's complement arithmetic of 14 bit quantities. The address y is a 13 bit number given a zero sign, while the C(XR) is a 14 bit number. Overflows from bit 4 carry into bit 17. The address used is the 13 rightmost bits of the sum.

Examples:

y_{5-17}	$C(XR)_{4-17}$	$z = y+C(XR)_{5-17}$
00002	00001	00003
00002	37776	00001
04000	15000	01000
04000	22000	06000
12345	37777	12345
17777	00001	00000
00001	37777	00001

II. ADDRESSABLE COMMANDS

(A) STORE CLASS

MNEMONIC	OCTAL VALUE	OPERATION	SYMBOLIC DESCRIPTION AND TIMING
STO y	000000 + y	Store	C(AC)→C(y)
Place the contents of AC in register y. The previous contents of y are destroyed. Contents of AC remain unchanged.			2 cycles
STX y	020000 + y	Store AC, Indexed	C(AC)→C(y+C(XR)) 2 cycles
SXA y	040000 + y	Store Index in Address	$C(XR)_{5-17} \rightarrow C(y)_{5-17}$
Store the digits of the index register in the address portion of register y. The sign of XR is ignored. The contents of XR are unchanged. Bits 0 through 4 of register y are unchanged.			3 cycles
ADO y	060000 + y	Add One	C(y) + 1→C(AC)→ C(y)
Add One to the contents of memory register y and leave the results in the accumulator and register y.			3 cycles
SLR y	100000 + y	Store Live Register	C(LR)→C(y)
The contents of LR are placed in register y. The previous contents of y are destroyed. Contents of LR are unchanged.			2 cycles
SLX y	120000 + y	Store LR, Indexed	C(LR)→C(y+C(XR)) 2 cycles
STZ y	140000 + y	Store Zero Clear register y to +0 .	0→C(y) 2 cycles

II. ADDRESSABLE COMMANDS

(B) ADD CLASS

MNEMONIC	OCTAL VALUE	OPERATION	SYMBOLIC DESCRIPTION
ADD y	200000 + y	Add the contents of register y to AC. Contents of y are unchanged.	$C(y) + C(AC) \rightarrow C(AC)$ 2 cycles
ADX y	220000 + y	Add, indexed.	$C(y+C(XR)) + C(AC) \rightarrow C(AC)$ 2 cycles
LDX y	240000 + y	Load Index	$C(y)_{5-17} \rightarrow C(XR)_{5-17}$ $C(y)_0 \rightarrow C(XR)_4$ 2 cycles
Load the index register from bit 0 and bits 5 through 17 of register y. The contents of y are unchanged.			
AUX y	260000 + y	Augment Index	$C(y)_{0,5-17} + C(XR) \rightarrow C(XR)$ 2 cycles
The contents of memory register y are added to XR. The fourteen bit number added consists of bit 0 and bits 5 through 17 of register y. Addition is ones' complement on 14 bit numbers.			
LLR y	300000 + y	Load Live Register	$C(y) \rightarrow C(LR)$ 2 cycles
The contents of register y replace the previous contents of LR. Contents of y are unchanged. Previous contents of LR are destroyed.			
LLX y	320000 + y	Load LR, Indexed	$C(y+C(XR)) \rightarrow C(LR)$ 2 cycles
LDA y	340000 + y	Load Accumulator	$C(y) \rightarrow C(AC)$ 2 cycles
The contents of register y replace the previous contents of the AC. Contents of y are unchanged. Previous contents of the AC are destroyed.			
LAX y	360000 + y	Load Accumulator, Indexed	$C(y+C(XR)) \rightarrow C(AC)$ 2 cycles

II. ADDRESSABLE COMMANDS

(C) TRANSFER CLASS

MNEMONIC	OCTAL VALUE	OPERATION	CONDITIONS AND SYMBOLIC DESCRIPTION	
			$y \rightarrow C(PC)$ Timing: 1 cycle	$C(PC)+1 \rightarrow C(PC)$ Timing: 2 cycles
TRN y	400000 + y	Transfer on Negative AC	$C(AC)_0 = 1$	$C(AC)_0 = 0$
If the AC bit 0 is a one, take next instruction from register y. Otherwise, take next instruction in sequence.				
TZE y	420000 + y	Transfer on Zero	$C(AC) = +0$ or $C(AC) = -0$	$C(AC) \neq +0$, and $C(AC) \neq -0$
If the contents of the accumulator are either plus zero or minus zero, the next instruction is taken from register y. If the accumulator contents are not plus or minus zero, the next instruction in sequence will be executed.				
TSX y	440000 + y	Transfer and Set Index	Always; $C(PC) \rightarrow C(XR)_{5-17}$ $0 \rightarrow C(XR)_4$	Never
The next instruction is taken from register y and the address of the register following the TSX instruction is placed in the index register.				
TIX y	460000	Transfer and Index	$C(XR) \neq +0$ and $C(XR) \neq -0$ If $C(XR)_4 = 1$, $C(XR)+1 \rightarrow C(XR)$; If $C(XR)_4 = 0$, $-[-C(XR)+1] \rightarrow C(XR)$	$C(XR) = +0$ or $C(XR) = -0$
If the index register contains plus or minus zero, perform the next instruction in sequence without changing the contents of the index register. If the index register contains a non-zero positive number, its contents are reduced by one and the next instruction is taken from register y. If the index register contains a non-zero negative number, its contents are increased by one and the next instruction is taken from register y. A zero result will have the same sign as the initial contents of the index register.				

MNEMONIC	OCTAL VALUE	OPERATION	CONDITIONS AND SYMBOLIC DESCRIPTION	
			y→C(PC) Timing: 1 cycle	C(PC)+1→C(PC) Timing: 2 cycles
TRA y	500000 + y	Transfer	Always	Never
The next instruction is taken from register y.				
TRX y	520000 + y	Transfer, indexed.	Always y+C(XR)→C(PC)	Never
TLV y	540000 + y	Transfer on external Level	External level = 0 volts	External level = -3 volts
This instruction provides a means of testing an external condition, provided said condition can provide a 0 or -3 volt level at the in-out panel connection labeled TLV.				

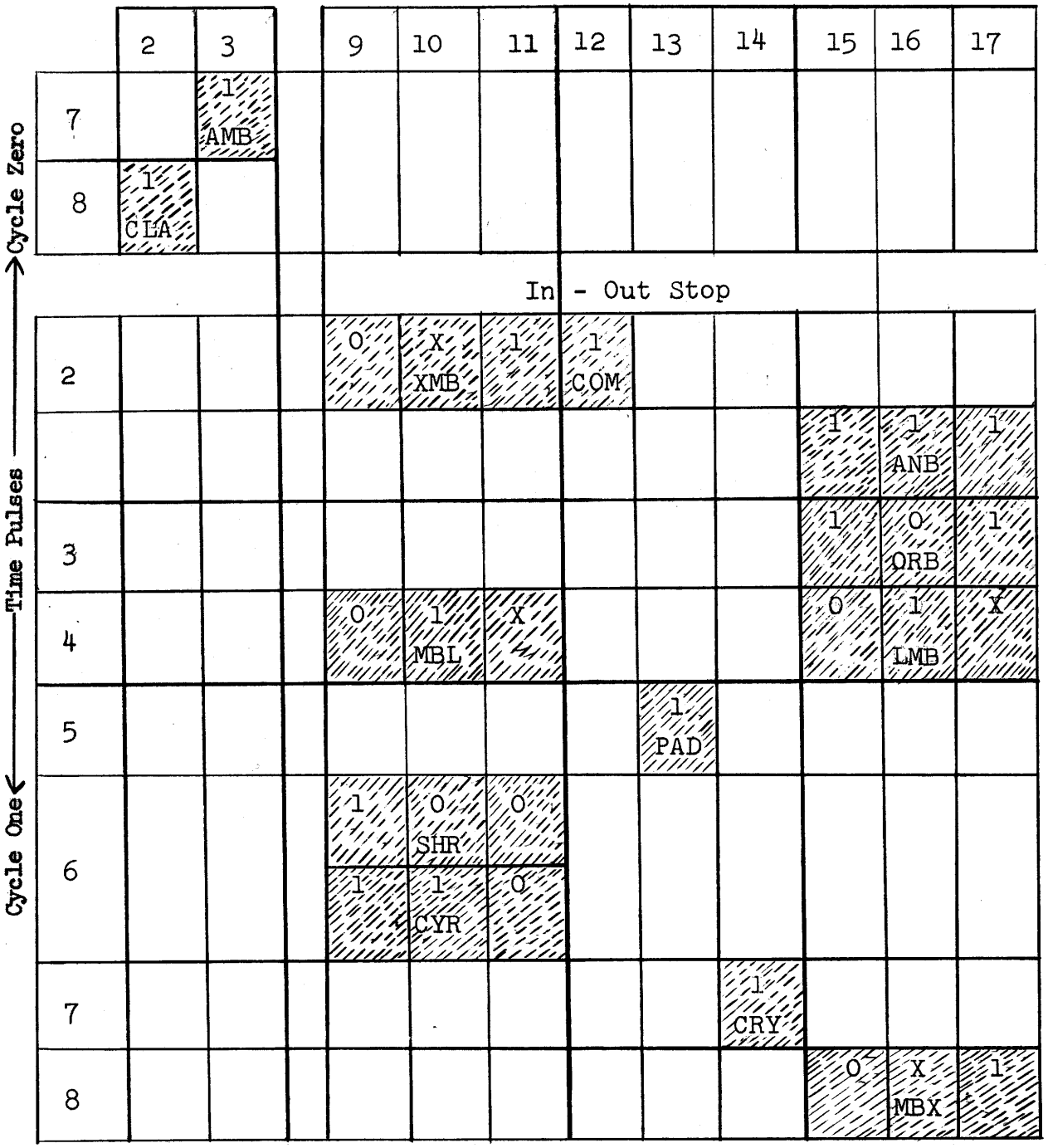
TX-0 ADDRESSABLE INSTRUCTIONS

Bits 0, 1 \ Bits 2, 3, 4	000	001	010	011	100	101	110	111
Store Class 00	sto (AC) → (y) 000000	stx (AC) → (y + (XR)) 020000	sxa $(XR)_{5-17}$ → $(y)_{5-17}$ 040000	ado (y) + 1 → (AC)→(y) 060000	slr (lr) → (y) 100000	slx (LR) → (y + (XR)) 120000	stz 0 → (y) 140000	 160000
Add Class 01	add (y) + (AC) → (AC) 200000	adx (AC) + (y + (XR)) → (AC) 220000	ldx $(y)_{0,\ 5-17}$ → $(XR)_{4-17}$ 240000	aux $(y)_{0,\ 5-17}$ + $(XR)_{4-17}$ → $(XR)_{4-17}$ 260000	llr (y) → (LR) 300000	llx (y + (XR)) → (LR) 320000	lda (y) → (AC) 340000	lax (y +(XR)) → (AC) 360000
Transfer Class 10	trn $(AC)_0$ = 1 ⊃ y→(PC) 400000	tze (AC) = ± 0 ⊃ y→(PC) 420000	tsx (PC)→(XR) y→(PC) 440000	tix (XR) ≠ + 0 ⊃ y→(PC) (XR) < 0 ⊃ (XR)+1→(XR) (XR) > 0 ⊃ (XR)-1→(XR) 460000	tra y→(PC) 500000	trx y + (XR) → (PC) 520000	tlv external level = 0 volts ⊃ y→(PC) 540000	tpl $(LR)_0$ = 0 ⊃ y→(PC) 560000

III. OPERATE CLASS COMMANDS

(A) MICRO ORDER CHART

Instruction Bits



III. OPERATE CLASS COMMANDS

(B) IN OUT GROUP CHART

Instruction bits 6, 7, and 8

Instruction bits 4 and 5

	000	001	010	011	100	101	110	111
00	NOP	1.1 TAC	1.2 TBR	1.1 PEN	SEL	SPARE	1.2 RPF	1.6 SPF
01	IOS EX0	IOS EX1	IOS EX2	IOS EX3	IOS EX4	IOS EX5	IOS EX6	IOS EX7
10	CPY	IOS R1L	IOS DIS	IOS R3L	IOS PRT	IOS TYP	IOS P6H	IOS P7H
11	1.8 HLT	0.6 CLL	0.6 CLR	SPARE	SPARE	SPARE	SPARE	SPARE

Any of the commands enclosed in this border may be used together with the micro commands listed in the preceding chart.

III. OPERATE CLASS COMMANDS

(C) MICRO-ORDERS

MNEMONIC	ACTION	SYMBOLIC DESCRIPTION
CLA	CLear AC	$0 \rightarrow C(AC)$
AMB	transfer AC contents to MBR	$C(AC) \rightarrow C(MBR)$
XMB	transfer XR contents to MBR	$C(XR)$ bits 5-17 $\rightarrow C(MBR)$ bits 5-17. $C(XR)$ bit 4 $\rightarrow C(MBR)$ bits 0-4.
MBL	transfer MBR contents to LR	$C(MBR) \rightarrow C(LR)$
LMB	transfer LR contents to MBR. Note: LMB and MBL, if used simultaneously, interchange C(LR) and C(MBR).	$C(LR) \rightarrow C(MBR)$
MBX	transfer MBR contents to XR	$C(MBR)_{5-17} \rightarrow C(XR)_{5-17}$ $C(MBR)_0 \rightarrow C(XR)_4$
CYR	CYcle AC contents Right one binary position. (AC bit 17 goes to AC bit 0)	$C(AC)_i \rightarrow C(AC)_j$ $i = 0, 1, \ldots, 17$ $j = (i+1) \bmod 18$
SHR	SHift AC contents Right one binary position (AC bit 0 is unchanged, bit 17 is lost)	$C(AC)_i \rightarrow C(AC)_{i+1}$, $i = 0, 1, 2, \ldots 16$
ANB	ANd (logical product) LR MBR.	$C(LR) \wedge C(MBR) \rightarrow C(MBR)$
ORB	OR (logical sum) LR contents into MBR.	$C(LR) \vee C(MBR) \rightarrow C(MBR)$
COM	COMplement AC	$\overline{C(AC)} \rightarrow C(AC)$
PAD	Partial ADd MBR to AC (for each MBR one, complement the corresponding AC bit.)	$C(MBR) \oplus C(AC) \rightarrow C(AC)$

MNEMONIC	ACTION	SYMBOLIC DESCRIPTION
CRY	A CarRY digit is a ONE if in the next least significant digit, either AC = 0 and MBR = 1, or AC = 1 and carry digit = 1. The carry digits so determined are partial added to the AC by CRY. PAD and CRY used together give a full one's complement addition of C(MBR) to C(AC).	$CRY[C(AC), C(MBR)] = C(AC) \oplus C \rightarrow AC.$ $C_i = [C(MBR)_j \wedge \overline{C(AC)_j}]$ $\vee [C_j \wedge C(AC)_j]$ $i = 0, 1, \ldots, 17$ $j = (i+1) \bmod 18.$ $CRY\ [C(AC) \oplus C(MBR), C(MBR)]$ $= C(AC) + C(MBR)$

III. OPERATE CLASS COMMANDS

(D) IN-OUT GROUP COMMANDS WHICH CAN BE USED WITH MICRO-ORDERS SPECIFIED BY FITS 9-17.

OCTAL CODE	MNEMONIC	ACTION	CYCLE AND TIME PULSE
631000	CLL	CLear Left 9 bits of AC	0.6
632000	CLR	CLear Right 9 bits of AC	0.6
607000	SPF	Set Program Flag register from MBR	1.6
606000	RPF	Read Program Flag register into MBR. (inclusive or)	1.2
602000	TBR	transfer TBR contents to MBR (inclusive or)	1.1
601000	TAC	transfer TAC contents to AC (inclusive or)	1.2
603000	PEN	set AC bit 0 from light PEN FF, and AC bit 1 from light gun FF. (FF's contain one if pen or gun saw displayed point). Then clear both light pen and light gun FF's.	1.1
620000	CPY	CoPY synchronizes transmission of information between in-out equipment and computer.	**
621000	R1L	Read ONE Line of tape from PETR into AC bits 0, 3, 6, 9, 12, 15 with CYR before read (inclusive or)	IOS
623000	R3L	Read THREE Lines of tape from PETR AC bits 0, 3, 6, 9, 12, 15, with CYR before each read (inclusive or)	IOS
622000	DIS	DISplay a point on scope (AC bits 0-8 specify X coordinate, AC bits 9-17 specify Y coordinate). The coordinate (0,0) is usually at the lower left hand corner of the scope. A console switch is available to relocate (0,0) to the center.	IOS

OCTAL CODE	MNEMONIC	ACTION	CYCLE AND TIME PULSE
626000	P6H	Punch one SIX-bit line of Flexo tape (without seventh hole) from AC bit 2, 5, 8, 11, 14, 17. Note: Lines without seventh hole are ignored by PETR.	IOS
627000	P7H	same as P6H, but with SEVENTH hole	IOS
610000 through 617000	EX0 through EX7	operate user's EXTernal equipment. Causes signals to appear at corresponding terminals on the in-out panel.	IOS
600000	NOP	Perform No in-out group OPeration	
630000	HLT	HaLT the computer and sound chime	1.8

III. OPERATE CLASS COMMANDS

(E) SELECT CLASS CHART

bits	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	1	1	A	X	0	0	1	0	0	X	X	X	X	B	C	C	D	D

Bits	0	1
A	Does not clear AC	Clears AC
B	Read or write in Binary mode (odd parity)	Read or write in Decimal mode (even parity)
	Decoded as a 2 bit group	
C	00 Backspace tape 01 Read select tape 10 Rewind tape 11 Write select tape	
D	Select one of 4 devices 00 Unused 01 Magnetic Tape unit No. 1 10 Unused 11 Unused	
X	Ignored	

IV. OPERATE CLASS INSTRUCTIONS RECOGNIZED BY MACRO AND FLIT

MNEMONIC	OCTAL VALUE	OPERATION
opr	600000	No operation.
xro	600001	Clear XR to +0.
lro	600200	Clear LR to +0.
cla	700000	Clear entire AC to +0.
com	600040	Complement the AC.
clc	700040	Clear and complement: set AC to -0.
shr	600400	Shift accumulator right one place, bit 0 remains unchanged.
cyr	600600	Cycle AC right one place.
cll	631000	Clear left half of AC to zero.
clr	632000	Clear right half of AC.
cyl	640030	Cycle AC left one place.
amz	640050	Add minus zero to AC.
cal	700200	Clear AC and LR to +0.
alr	640200	Place accumulator contents in live register.
alo	640220	ALR, then set AC to +0.
alc	640260	ALR, then set AC to -0.
all	640230	ALR, then cycle left once.
lac	700022	Place LR in AC.
lad	600032	Add LR to AC.
laz	700072	Add LR to minus zero in AC.
lpd	600022	Logical exclusive or of AC is placed in AC, (partial add)
cry	600012	Carry the contents of AC according to bits of LR. Results of this operation is same as if contents of LR were added to exclusive or of AC and LR. PAD followed by CRY is equivalent to LAD.
lcc	700062	Place complement of LR in AC.

MNEMONIC	OCTAL VALUE	OPERATION
lcd	600072	Contents of LR minus those of AC are placed in AC.
lal	700012	Place LR in AC cycled left once.
lar	700622	Place LR in AC cycled right once.
ana	740027	Logical and of AC and LR is placed in AC.
anl	640207	Logical and of AC and LR is placed in LR.
ano	740207	ANL, then clear AC.
ora	740025	Logical or of AC and LR is placed in AC.
orl	640205	Logical or of AC and LR is placed in LR.
oro	740205	ORL, then clear AC.
ial	740222	Interchange AC and LR.
iad	640232	Interchange and add: AC contents are placed in the LR and the previous contents of the LR are added to AC.
cax	700001	Clear AC and XR to +0.
axr	640001	Place AC contents in XR.
axo	640021	AXR, then set AC to +0.
axc	640061	AXR, then set AC to -0.
alx	640031	AXR, then cycle AC left once.
arx	640601	AXR, then cycle AC right once.
xac	700120	Place index register in accumulator.
xad	600130	Add index register to accumulator.
xcc	700160	Place complement of XR in accumulator.
xcd	600170	Contents of XR minus those of AC are placed in AC.
xal	700110	XAC, then cycle AC left once.
lxr	600003	Place LR in XR.

MNEMONIC	OCTAL VALUE	OPERATION
xlr	600300	Place XR in LR.
ixl	600303	Interchange XR and LR.
rax	640203	Place LR in XR, then place AC in LR.
rxa	700322	Place LR in AC, then place XR in LR.
hlt	630000	Stops computer.
cpf	607000	The program flag register is cleared.
spf	647000	Place AC in program flag register.
rpf	706020	The program flag register is placed in AC.
tac	701000	Contents of test accumulator are placed in AC.
dis	622000	Display point on CRT corresponsing to contents of AC.
dso	662020	DIS, then clear AC.
pen	603000	Contents of light pen and light cannon flip-flops replace contents of AC bits 0 and 1. The flip-flops are cleared.
prt	624000	Print one on-line flexo character from bits 2, 5, etc. of AC.
pnt	624600	PRT, then cycle AC right once to set up another character.
pno	664020	PRT, then clear AC.
pnc	664060	PRT, then clear AC to -0.
p6h	626600	Punch one line of paper tape; 6 holes from bits 2, 5, etc. of AC then cycle right once.
p6o	666020	p6h then clear AC.

MNEMONIC	OCTAL VALUE	OPERATION
p6s	726000	Clear AC and punch a line of blank tape.
p6b	766020	Punch a line of blank tape but save AC.
p7h	627600	Same as p6h, but punch 7th hole.
p7o	667020	p7h then clear AC.
r1c	721000	Read one line paper tape into AC bits 0, 3, etc.
r1r	721600	r1c, then cycle AC right once.
r3c	723000	Read three line of paper tape.
rew	604010	Rewind tape unit.
wrs	604014	Select tape unit for writing a record.
rds	604004	Select tape unit for reading a record.
bsr	604000	Backspace tape unit by one record.
rtb	604004	Read tape binary. (odd parity)
wtb	604014	Write tape binary. (odd parity)
rtd	604024	Read tape decimal. (even parity)
wtd	604034	Write tape decimal. (even parity)
cpy	620000	Transmits information between the live register and selected input-output unit.