TECHNICAL MANUAL
NS11L
MEMORY CARD ASSEMBLY

National Semiconductor
Memory Systems

TECHNICAL MANUAL
NS11L
MEMORY CARD ASSEMBLY

National Semiconductor
Minicomputer Systems

420103841 Rev B
April 1980

TABLE OF CONTENTS

FIGURES

TABLES

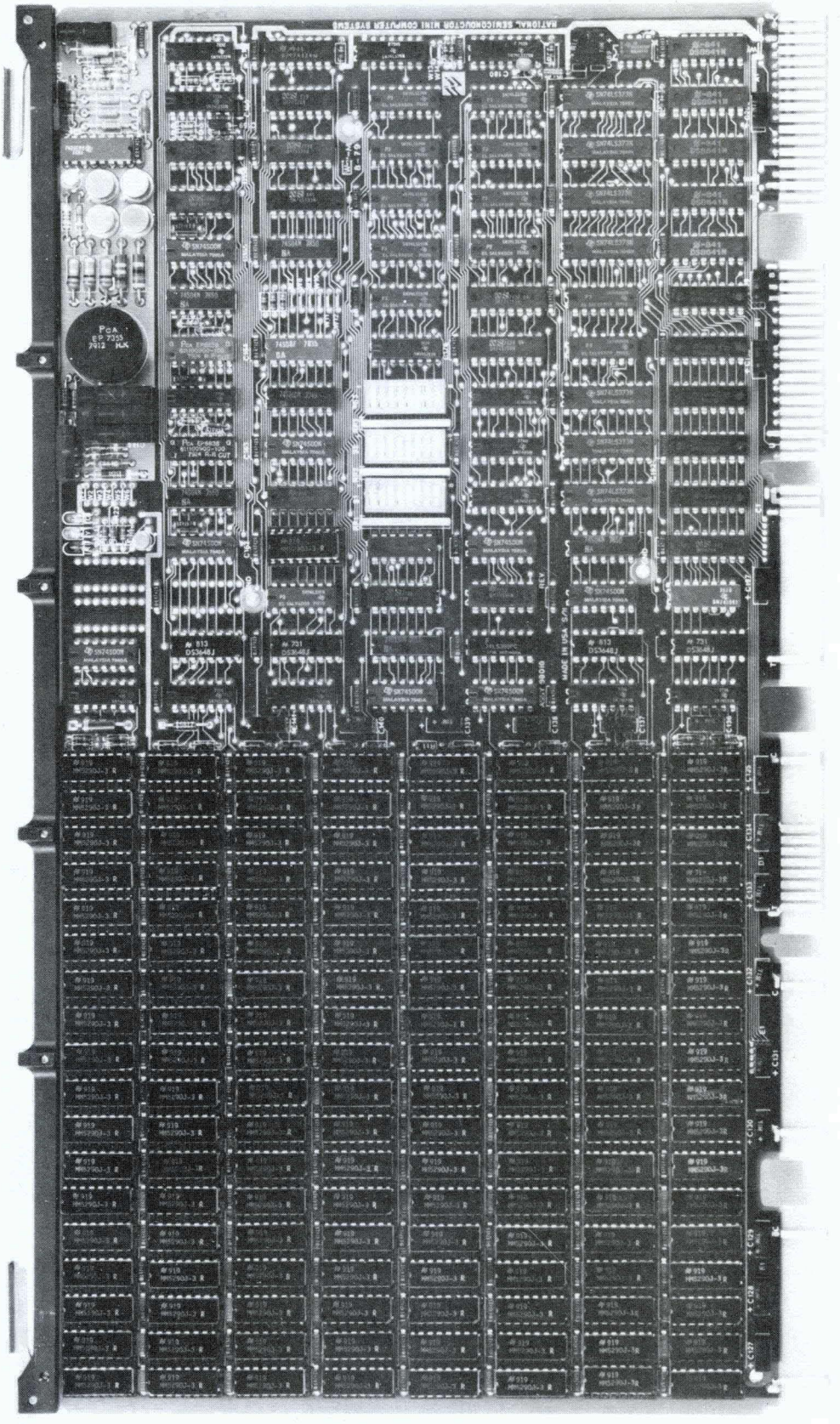


Fig. 1-1

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual contains four sections which describe the NS11L Add-in Memory System. This information includes a general description, an installation and maintenance section, theory of operation, and a section containing assembly drawings, schematics, and bill of materials. Figure 1-1 is a photograph of the NS11L Add-In Memory System.

1.2 PURPOSE

The NS11L, P/N-980103841, is designed for use with DEC * PDP-11 CPU's. The NS11L is directly compatible with any DEC UNIBUS/Modified UNIBUS/SPECIAL UNIBUS type backplane.

1.3 PHYSICAL DESCRIPTION

The NS11L memory is contained on one multilayer printed circuit card. See Table 1-1 for the physical dimensions of the NS11L.

* DEC, UNIBUS, modified UNIBUS, and PDP11 are registered trade marks of Digital Equipment Corp., Maynard Mass.

Table 1-1 NS11L Dimensions

Thickness	.480	inches
Height	8.680	inches
Length	15.687	inches

The NS11L memory is designed to mount on a minimum center-to-center board spacing of 0.50". Two card ejectors permit easy removal of the card.

Figure 1-2 is a connector locator diagram.

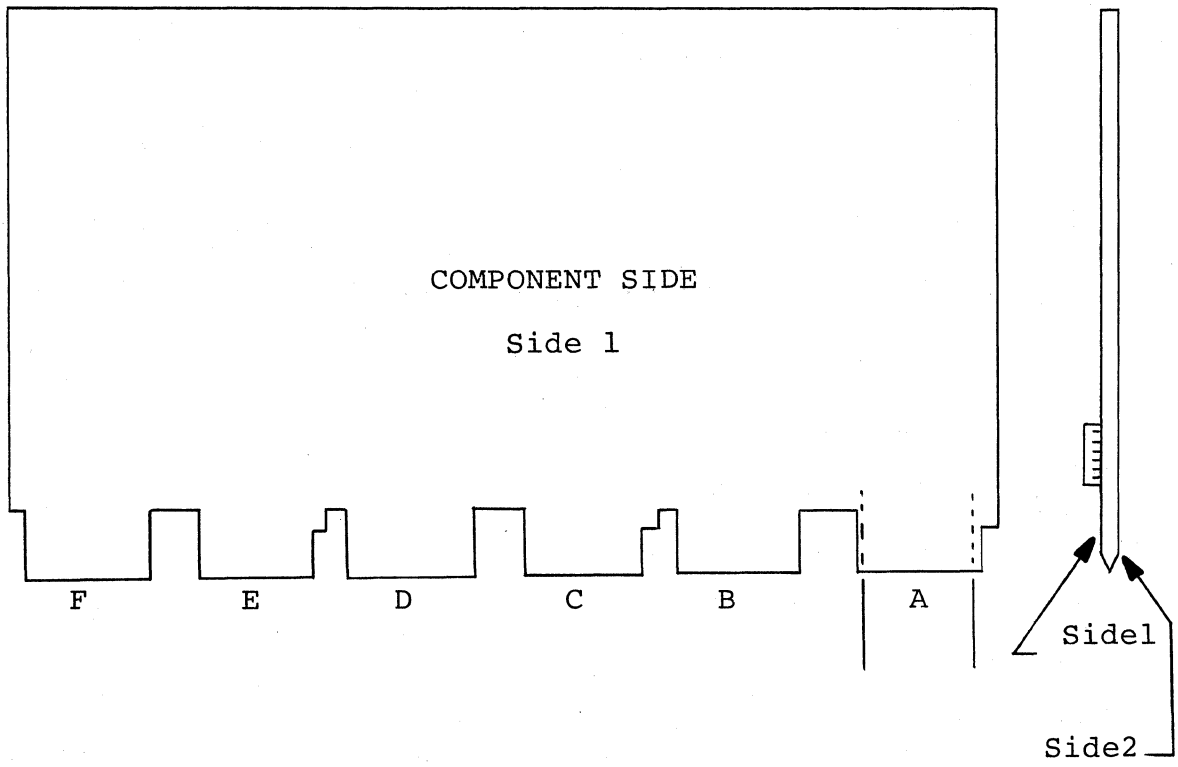


FIGURE 1-2

1.3.1 I/O Connectors

The NS11L Memory is designed to fit mechanically into the following PDP-11 backplanes:

1. DD11-DK slots 2-8
2. DD11-PK slots 3-8
3. DD11-CK slots 2-3

For installation in backplanes not listed above, the backplane connector pin assignments must be compatible with the NS11L pin assignments as listed in Table 3-1.

1.4 FUNCTIONAL DESCRIPTION

The NS11L is a 128Kx18 bit Add-In Memory for the DEC PDP-11 family of minicomputers. The NS11L board requires +5V only and generates +12V and -5V with an on board DC-to-DC converter. The board is designed for maximum reliability and speed. Additionally, the board contains an on-board CSR register, eliminating the need for a DEC M-7850 parity controller. The NS11L is completely hardware and software compatible with all DEC systems as described in paragraph 1.2.

1.5 GENERAL SPECIFICATIONS

The following tables list the general specifications of the NS11L Add-In Memory. Table 1-2 lists the power requirements and Table 1-3 lists access and cycle times.

Table 1-2 NS11L Power Requirements

	Current-Amps					
Supply Voltage	Operational		Standby		Battery Back-up	
	TYP.	MAX.	TYP.	MAX.	TYP.	MAX.
+5V	4.5	5.0	3.7	3.8	Ø	Ø
$+5V_{BB}$	.9	1.0	.9	1.0	.9	1.0

Table 1-3 Access and Cycle Times

READ		
Cycle Time	405ns	MIN
Access Time	300ns	MAX
Parity Access Time	340ns	MAX
CSR ACCESS	100ns	MAX
WRITE		
Cycle Time	405ns	MIN
Access Time (Add/Data Latch)	100ns	MAX
REFRESH		
Cycle Time	405ns	MIN

(Cycle requests made during a refresh will extend the cycle and access time an additional 405ns Max).

NOTE:

1) Cycle time - The interval between memory reception of Bus MSYN L (at reciever input) and the availability of the memory to respond to the next Bus MSYN L.

2) Access Time - The interval between memory reception of Bus MSYN L and the assertion of Bus SSYN L.

1.5.1 Operating Modes

The operating mode of the memory is determined by the state of the C0 and C1 control lines and the A0 address line. These modes are defined in Table 1-4 shown below.

Table 1-4 Operating Modes

A0	C1	C0	COMMAND	OPERATION
X	0	0	DATI	Read
X	0	1	DATIP	Read
X	1	0	DATO	Write Word
0	1	1	DATOB 0	Write Byte 0
1	1	1	DATOB 1	Write Byte 1

NOTE: Logic 1=0 volts (LOW)
Logic 0=+ 3.4 volts (HIGH)

1.6 ENVIRONMENTAL SPECIFICATIONS

The NS11L is designed to operate over a variety of environmental conditions. Listed below are the environmental conditions and specifications.

1.6.1 Operating Specifications

- TEMPERATURE.....Ambient Air temperature range of $0^{\circ}C$ to $+50^{\circ}C$.
- THERMAL SHOCK.....The NS11L Memory can withstand a thermal shock with a maximum rate of change of $30^{\circ}C$ per hour during operation.

- HUMIDITY.....The Memory has been designed to operate in a relative humidity of up to 95% (without condensation).
- ALTITUDE.....The system is capable of operation at altitudes from -1,000 feet msl to +10,000 feet msl.
- COOLING.....Suggested minimum air flow for the NS11L Memory is 25 cfm.

1.6.2 Shipping and Storage Specifications

- TEMPERATURE.....The NS11L Memory can withstand a temperature range of -40°C to +85°C during shipment or storage.
- THERMAL SHOCK.....A thermal rate of change as high as 10°C per minute can be tolerated by the Memory.
- ALTITUDE.....A Shipping Altitude of 40,000 feet can be withstood.
- MECHANICAL SHOCK....The NS11L Memory, housed in its shipping container, can tolerate mechanical shock resulting from drop tests performed in accordance with MIL-STD-810B, Method 516, procedure V, without exhibiting damage or degradation.

1.7 RELIABILITY

This card was designed to the best commercial standards of workmanship. Vigorous testing is conducted (including testing over operating temperature range) to ensure a reliable service of ten years at 24-hours per day usage (exclusive of routine maintenance time). The design is such that catastrophic failure occurrence is minimized and minimal propagation of such failure will be experienced. Calculated MTBF using A+ logic and MIL Handbook 217B (where applicable) is 28,873 hours.

SECTION II

INSTALLATION AND MAINTENANCE

2.1 GENERAL

The NS11L Memory is ready for installation upon receipt; however, the memory size and address switches and the option jumpers must be checked before the card is installed. Refer to paragraphs 2.4 thru 2.7., and Tables 2-1 through 2-7, for switch and jumper information.

The NS11L is completely compatible with DEC's PDP-11 computers and all standard DEC peripheral devices. It can be used in both parity and non-parity systems.

For installation in backplanes not listed below, the subject backplane connector pin assignments must be compatible with the NS11L pin assignments listed in Table 3-1.

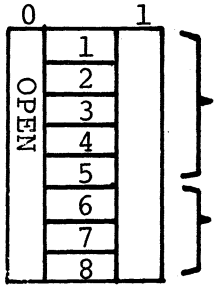
The Memory is directly plug-compatible into the following DEC backplanes:

- DD11-DK (slots 2-8)
- DD11-PK (slots 3-8)
- DD11-CK (slots 2-3)

TABLE 2-1

SWITCH DESIGNATIONS AND SETTINGS

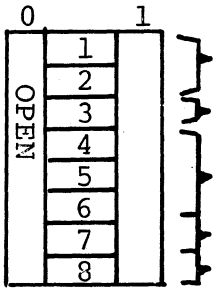
SWITCH 1



1-5, UNIBUS Starting address select. Open=ADDR Ø
See Table 2-2 on page 2-3.

6-8, Special Bus starting address select. Open=ADDR Ø
See Table 2-3 on page 2-3.

SWITCH 2



1-2, I/O space size select. See Table 2-4 on page 2-4.
4K I/O - 1=OPEN, 2=CLOSED.

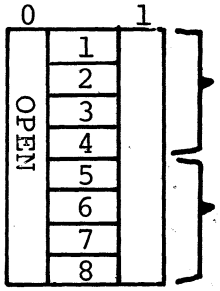
3, CSR/Parity disable. CLOSED=disable.

4-6, Spare.

7, Special Bus operation enable. CLOSED=enable.

8, Special Bus starting address select. OPEN=ADDR Ø
See Table 2-3 on page 2-3.

SWITCH 3



1-4 CSR address select. CLOSED=772100.
See Table 2-5 on page 2-4.

5-8, Memory size select. CLOSED=128K.
See Table 2-6 on page 2-5.

TABLE 2-2

UNIBUS STARTING ADDRESS (OCTAL)	MEMORY STARTING ADDRESS	SWITCH SETTING				
		S1-5	S1-4	S1-3	S1-2	S1-1
000000	0K	0	0	0	0	0
020000	4K	0	0	0	0	1
040000	8K	0	0	0	1	0
060000	12K	0	0	0	1	1
100000	16K	0	0	1	0	0
120000	20K	0	0	1	0	1
140000	24K	0	0	1	1	0
160000	28K	0	0	1	1	1
200000	32K	0	1	0	0	0
220000	36K	0	1	0	0	1
240000	40K	0	1	0	1	0
260000	44K	0	1	0	1	1
300000	48K	0	1	1	0	0
320000	52K	0	1	1	0	1
340000	56K	0	1	1	1	0
360000	60K	0	1	1	1	1
400000	64K	1	0	0	0	0
420000	68K	1	0	0	0	1
440000	72K	1	0	0	1	0
460000	76K	1	0	0	1	1
500000	80K	1	0	1	0	0
520000	84K	1	0	1	0	1
540000	88K	1	0	1	1	0
560000	92K	1	0	1	1	1
600000	96K	1	1	0	0	0
620000	100K	1	1	0	0	1
640000	104K	1	1	0	1	0
660000	108K	1	1	0	1	1
700000	112K	1	1	1	0	0
720000	116K	1	1	1	0	1
740000	120K	1	1	1	1	0
760000	124K	1	1	1	1	1

NOTES

A. 0=OPEN (OFF)
1=CLOSED (ON)

B. For 18 bit addressing, S1-6, S1-7, S1-8 and S2-8 must be open. For 22 Bit addressing, see Table 2-5.

TABLE 2-3

SPECIAL BUS STARTING ADDR (OCTAL)	MEMORY STARTING ADDRESS	SWITCH SETTING			
		S2-8	S1-8	S1-7	S1-6
00000000	0K	0	0	0	0
01000000	128K	0	0	0	1
02000000	256K	0	0	1	0
03000000	384K	0	0	1	1
04000000	512K	0	1	0	0
05000000	640K	0	1	0	1
06000000	769K	0	1	1	0
07000000	896K	0	1	1	1
10000000	1024K	1	0	0	0
11000000	1152K	1	0	0	1
12000000	1280K	1	0	1	0
13000000	1408K	1	0	1	1
14000000	1536K	1	1	0	0
15000000	1664K	1	1	0	1
16000000	1792K	1	1	1	0
17000000	1920K	1	1	1	1

NOTES

A. 0=OPEN (OFF)
1=CLOSED (ON)

B. For 22 bit address operation, S2-7 must be closed.

TABLE 2-4

I/O SPACE SIZE SELECT

I/O SPACE SIZE	SWITCH SETTING	
	S2-2	S2-1
8K	0	0
4K	1	0
2K	1	1

TABLE 2-5

CSR ADDRESS SELECT

CSR ADDRESS SELECTION		SWITCH SETTING			
UNIBUS ADDRESS	SPECIAL BUS ADDRESS	S3-4	S3-3	S3-2	S3-1
772100	17772100	1	1	1	1
772102	17772102	1	1	1	0
772104	17772104	1	1	0	1
772106	17772106	1	1	0	0
772110	17772110	1	0	1	1
772112	17772112	1	0	1	0
772114	17772114	1	0	0	1
772116	17772116	1	0	0	0
772120	17772120	0	1	1	1
772122	17772122	0	1	1	0
772124	17772124	0	1	0	1
772126	17772126	0	1	0	0
772130	17772130	0	0	1	1
772132	17772132	0	0	1	0
772134	17772134	0	0	0	1
772136	17772136	0	0	0	0

0=OPEN (off)
1=CLOSED (on)

TABLE 2-6

MEMORY SIZE SELECTION

ON BOARD MEMORY CAPACITY	SWITCH SETTING			
	S3-8	S3-7	S3-6	S3-5
8K	0	0	0	0
16K	0	0	0	1
24K	0	0	1	0
32K	0	0	1	1
40K	0	1	0	0
48K	0	1	0	1
56K	0	1	1	0
64K	0	1	1	1
72K	1	0	0	0
80K	1	0	0	1
88K	1	0	1	0
96K	1	0	1	1
104K	1	1	0	0
112K	1	1	0	1
120K	1	1	1	0
128K	1	1	1	1

0= OPEN (off)
1= CLOSED (on)

TABLE 2-7

JUMPER PLACEMENT CHART

JUMPER	FUNCTION	INSTALLED	REMOVED
W1	+12V From Convertor to Array	Normal	During Test
W2	+V To Array	During Test	Normal
W3	Not Used	- -	Normal
W4	-5V From Convertor to Array	Normal	During Test
W5	-V To Array	During Test	Normal
W6	Not Used	- -	Normal
W7		Normal	-
W8		- -	Normal
W9		- -	Normal
W10	8K Partial RAM	Normal	-
W11	Configuration (Not Used)	- -	Normal
W12		- -	Normal
W13	Internal Refresh Disable	- -	Normal
W14	External Refresh In	- -	Normal
W15	+20V (AV2) In	- -	Normal
W16	+15V Batt. (AR1) In	During Test	Normal
W17	+5V Batt. (BD1) to +5VB Plane	For Batt. Back up	Normal
W18	+5V to +5VB Plane	Normal	For Batt. Back up
W19	I/O Space Disable	- -	Normal

Memory boards will be shipped with the jumpers in the "NORMAL" configuration.

CAUTION

Do not attempt to install the NS11L Memory board into DEC backplanes listed below or damage to the equipment could result:

- MF11-U
- MF11-W

Maintenance of the NS11L is minimal, enhanced by the use of fixed timing sequences. Refer to paragraph 2.10 for maintenance information.

2.2 SAFETY

The following safety precautions should be observed during installation and maintenance:

WARNING

Proper concern for the safety of all personnel is vital when installing equipment. The following safety practices should always be observed, or injury could occur.

2.2.1 Power

1. Remove all power from the system before installation using the related facility and/or system circuit breakers. Remove the AC power plug from the AC receptacle. (This is particularly important when cards or components are to be removed).

2. Tag all system circuit breakers with WARNING tags to ensure that circuit breakers will not be inadvertently turned on during installation.

3. When it is necessary to work on a system where power is present, never work alone. Two people must always be present when work is being done within a system, or on an interconnecting cable whenever system power is applied.

2.2.2 Fire

1. Good housekeeping is a significant factor in fire and accident prevention. Keep benches and working areas clear of unnecessary articles.

2. Ensure fire extinguishers of the CO_2 type (for electrical fires) are readily available.

2.3 UNPACKING AND INSPECTION

Follow the steps listed below to unpack and inspect the NS11L Memory board.

1. Remove all packing materials. (Failure to do so could result in damage to the equipment and present a fire hazard); store the reusable packing materials for future use.

2. Remove the Memory board from its container.

3. Inspect the board for visual damage, checking for bent stiffener, damaged IC's, broken wires or connectors, dislocated or broken switches or indicators, etc. Certain damage may not be detected until power has been applied and diagnostics performed.

NOTE: Visually damaged or inoperative boards should be returned to: NATIONAL SEMICONDUCTOR
2900 Semiconductor Drive
Santa Clara, California 95051

2.4 ADDRESS AND I/O SWITCH CONFIGURATIONS

2.4.1 Address

The NS11L Memory will accept a full 22 bit address with the least significant bit being used for Byte selection. The address lines to the memory are single rail; the addressing mode may be random. The address lines are identified as A0 through A21.

The NS11L may be used for expansion to 2M words using the 22 bits of address. When this expansion is used, address I/O pin assignments are as follows:

BUS A18-BE2
BUS A19-BE1
BUS A20-AP1
BUS A21-AN1

A0 is used for Byte selection. A1 through A21 are decoded for one of 2,097,152 address locations.

A13 through A21 are 'strappable' on the memory module. These address lines may be strapped to set the initial address for a memory module. Nine switch positions located at S1 and S2 are provided to set the initial address. Five positions are used for initial address selection in the 0-128K address range.

The remaining four positions can be used for expansion to 2M words. See Table 2-2 for 0-128K Select. See Table 2-3 for expansion to 2M word. Address selection is in 128K blocks to 2M word. Addresses A18 thru A21 are switch settable via switches per Table 2-3. Address buffer for A18-A21 must be enabled by closing switch S2-7. For system expansion beyond 128K, Table 2-2 is used in conjunction with Table 2-3 to ascertain required switch settings.

Table 2-1 is a general guide to the address and I/O switch configurations, and lists the pages of this guide for switch selection. (See page 2-2).

2.5 CSR ADDRESS ASSIGNMENT

The NS11L contains an on-board CSR, which contains error information in the event of a parity error. There are 16 possible CSR addresses as listed in Table 2-5. When the NS11L is used in conjunction with DEC parity memory and a DEC M7850 parity controller, or multiple NS11L's, the CSR addresses of the M7850 and NS11L's must not be the same. The CSR can be disabled by closing switch S2-3. See Table 2-5 for CSR address selection.

NOTE: CSR address has no relevance to the memory starting address or storage capacity of the NS11L.

2.6 BATTERY BACK UP

The NS11L can be configured for battery back up by installing jumper W17 and removing jumper W18. See Table 2-7 for a list of jumper configurations.

2.7 I/O CONFIGURATIONS

A. I/O Space Selection

The NS11L has a normal reserved I/O space of 4K but can be selectable to either 8K or 2K. The I/O space normally resides between 124K and 128K for Unibus operation. I/O space will reside at the top of the 2M words for 22-Bit address operation. See Table 2-4 for I/O space size selection switch settings.

B. Memory Size Selection

The NS11L can be configured in 8K increments to 128K. Memory size must be set according to actual board capacity. See Table 2-6 for memory size select switch settings.

2.8 INSTALLATION

Perform the following steps in the order listed to install the NS11L Memory board:

1. Verify that the PDP11 system is performing properly by running the appropriate memory diagnostics before any changes to the CPU configuration are made.
2. Verify that jumper connections (Table 2-7) and switch settings (Tables 2-1 through 2-6) are correct according to the memory starting address, memory size, CSR address,

I/O space, and battery back-up, as per sections 2.4 thru 2.7.

3. Turn off CPU power.

4. Carefully slide the memory into the selected slot. Be sure that the component side faces the correct direction, and that the board is aligned in the card guides. Insert and remove slowly so contact is not made with adjacent boards. When the memory has engaged the connectors, press firmly on the card and seat it by exerting equal pressure on the two ejectors.

5. Replace any cables, covers, panels, etc., which were moved during installation. Turn on CPU power.

6. Perform post-installation checks listed in paragraph 2.9.

2.9 POST INSTALLATION CHECKS

Post installation checks consist primarily of checking the operation of the memory unit as an integral part of the data processing system in which it is installed. Since the functional checks depend upon the data processing system configuration and user application, the test routines to be used are left to the discretion of the user. Owing to the all-electronic nature of the memory unit, there are no mechanical checks or inspections to be performed once the unit is installed.

NOTE: Any unused "modified bus" backplane slot must have a bus grant card in location D, or the CPU will show bus error.

Again verify that the system is performing properly by running the appropriate memory diagnostics.

2.10 MAINTENANCE

The maintainability of the NS11L Memory is enhanced by the use of fixed timing sequences. Since all timing is self-contained on the card, and one card type is used, complete interchangeability is realized. A spare card can be used in place of a failing unit without the need for any timing adjustments.

2.10.1 Pretested Memory Replacement

One pretested memory device is plugged into an on-board socket for spare requirements. This spare memory device can be used to replace any failing memory devices in the field. The spare memory is at location U167.
The memory devices are all mounted in sockets, so that repairs can be effected on-site.

Paragraph 2.10.2 contains a listing of steps to follow prior to troubleshooting at the component level.

2.10.2 Preliminary Checks

If the memory fails, the following preliminary procedure should be followed before component-level troubleshooting:

1. Check the memory installation; it must be installed facing the correct direction. (Memory components are facing the same direction as the CPU board components).

2. Insure that the YELLOW and RED LED's are not lit; the Yellow LED will light if the DC/DC convertor has failed and the Red LED will light if a parity error has occured.
3. Remove memory and visually inspect; wipe edge-connector with clean cloth.
4. Re-check the jumper connections and switch settings.
5. Re-install the Memory, carefully seating module in the chassis connectors.
6. Using the peripheral equipment, interrogate various address areas of the memory. (This will assure the module is fully operational).
7. When possible, switch with another module known to be operating properly. (Use the results to determine whether the problem is in the module or in the processor interface).

Figure 2-1 may be used for locating defective memory devices.

FIGURE 2-1

MEMORY COMPONENT BIT AND ROW ADDRESS LOCATOR

U1																	U18
U19																	U36
U37																	U54
U55																	U72
U73																	U90
U91																	U108
U109																	U126
U127																	U144
BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	BIT 9	BIT 10	BIT 11	BIT 12	BIT 13	BIT 14	BIT 15	BIT P0	BIT P1

RAM IC's	MEMORY SYSTEM ADDRESS RANGE
U1-18	$0-16K(0-077776)_8$
U19-36	$16-32K(100000-177776)_8$
U37-54	$32-48K(200000-277776)_8$
U55-72	$48-64K(300000-377776)_8$
U73-90	$64-80K(400000-477776)_8$
U91-108	$80-96K(500000-577776)_8$
U109-126	$96-112K(600000-677776)_8$
U127-144	$112-128K(700000-777776)_8$

SECTION III

THEORY OF OPERATION

3-1 GENERAL

This section comprises a functional description of the memory card assembly. Description is divided into general discussion and detailed circuit description, each referring to appropriate block diagrams and schematics. The schematic diagram is located in Appendix A.

3-2 INTERFACE

3.2.1 Unibus; Standard, Modified and Special Bus

The DEC PDP-11 Unibus has three configurations. The standard configuration differs slightly from the Modified and Special configuration in pin designation. The Unibus signals are delineated in Table 3-1.

TABLE 3-1 Bus Signals Viewed From The Connector End

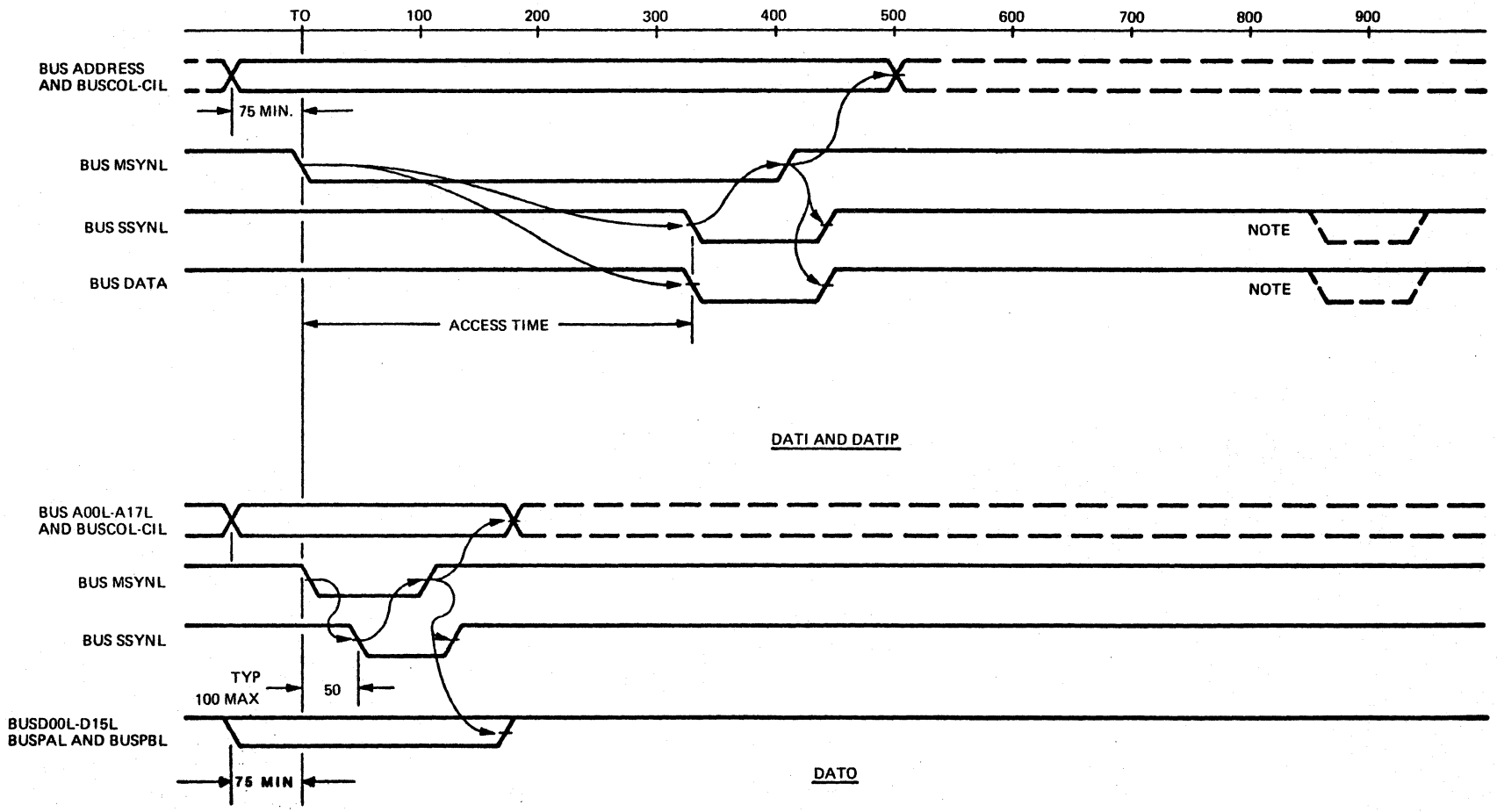
PIN NUMBER	STANDARD	MODIFIED	SPECIAL
AA1	INIT L	INIT L	INIT L
AB1	INTR L*	INTR L*	INTR L*
AC1	DOO L	DOO L	DOO L
AD1	DO2 L	DO2 L	DO2 L
AE1	DO4 L	DO4 L	DO4 L
AF1	DO6 L	DO6 L	DO6 L
AH1	DO8 L	DO8 L	DO8 L
AJ1	D10 L	D10 L	D10 L
AK1	D12 L	D12 L	D12 L
AL1	D14 L	D14 L	D14 L
AM1	PA L*	PA L*	PA L*
AN1	GND*	PAR P1*	A21 L
AP1	GND*	PAR P0	A20 L
AR1	GND*	+15 BATT*	+15 BATT*
AS1	GND*	-15 BATT*	-15 BATT*
AT1	GND*	GND	GND
AU1	NPG H*	+20V (CORE)*	+20V (CORE)*
AV1	BG7 S0*	+20V (CORE)*	+20V (CORE)*
AA2	+5V	+5V	+5V
AB2	GND*	TP*	TP*
AC2	GND	GND	GND
AD2	D01 L	D01 L	D01 L
AE2	D03 L	D03 L	D03 L
AF2	D05 L	D05 L	D05 L
AH2	D07 L	D07 L	D07 L
AJ2	D09 L	D09 L	D09 L
AK2	D11 L	D11 L	D11 L
AL2	D13 L	D13 L	D13 L
AM2	D15 L	D15 L	D15 L
AN2	PB L	PB L	PB L
AP2	BBSY L*	BBSY L*	BBSY L*
AR2	SACK L*	SACK L*	SACK L*
AS2	NPR L*	NPR L*	NPR L*
AT2	BR7 L*	BR7 L*	BR7 L*
AU2	BR6 L*	BR6 L*	BR6 L*
AV2	GND	+20V (CORE)*	+20V (CORE)*

*Pins assigned in Unibus connector but not used by memory.

TABLE 3-1 Bus Signals Viewed From The Connector End (Cont'd)

PIN NUMBER	STANDARD	MODIFIED	SPECIAL
BA1	BG6 H*	RESV*	RESV*
BB1	BG5 H*	RESV*	RESV*
BC1	BR5 L*	BR5 L*	BR5 L*
BD1	GND*	+5 BATT	+5 Batt
BE1	GND*	SSYN INT L*	A19 L
BF1	ACLO L*	ACLO L*	ACLO L*
BH1	A01 L	A01 L	A01 L
BJ1	A03 L	A03 L	A03 L
BK1	A05 L	A05 L	A05 L
BL1	A07 L	A07 L	A07 L
BM1	A09 L	A09 L	A09 L
BN1	A11 L	A11 L	A11 L
BP1	A13 L	A13 L	A13 L
BR1	A15 L	A15 L	A15 L
BS1	A17 L	A17 L	A17 L
BT1	GND	GND	GND
BU1	SSYN L	SSYN L	SSYN L
BV1	MSYN L	MSYN L	MSYN L
BA2	+5V *	+5V *	+5V *
BB2	GND *	TP *	TP *
BC2	GND *	GND *	GND *
BD2	BR4 L*	BR4 L*	BR4 L*
BE2	BG4 L*	PAR DET L*	A18 L
BF2	DC LO L	DC LO L	DC LO L
BH2	A00 L	A00 L	A00 L
BJ2	A02 L	A02 L	A02 L
BK2	A04 L	A04 L	A04 L
BL2	A06 L	A06 L	A06 L
BM2	A08 L	A08 L	A08 L
BN2	A10 L	A10 L	A10 L
BP2	A12 L	A12 L	A12 L
BR2	A14 L	A14 L	A14 L
BS2	A16 L	A16 L	A16 L
BT2	C1 L	C1 L	C1 L
BU2	C0 L	C0 L	C0 L
BV2	GND *	-5V (CORE)*	-5V (CORE)*

*Pins assigned in Unibus connector but not used by memory.



NOTE DATA AND SSYNL MAY BE DLEAYED UP TO 405 ns DUE TO SIMULTANEOUS REFRESH AND MEMORY REQUEST.

FIGURE 3-1

3.2.2 SIGNALS

There are three types of signals; input, output and bidirectional. These signals are received, processed and passed back to the CPU in two logic levels: A high, or logic level one; and a low, or logic level zero. Specifications for these logic levels are as follows:

TYPE OF SIGNAL	LEVEL ONE	LEVEL ZERO
Bus Logic Levels	+0.8V or Less	+2.0V or More
Input Signal Logic Levels	1.3V Maximum 30 microamps typical at 0.8V	1.7V Minimum 80 microamps maximum at 2.5V
Output Signal Logic Levels	0.8V maximum at 70milliamps	2.4V minimum 25 microamps maximum at 3.5V

Memory System Interface Timing is given in figure 3-1. All timing is measured at the card edge connectors and is referenced to the +1.5V level of signal transition.

3.2.3 Types of Signals

There are three types of signals. Input signals, output signals and bi-directional signals.

Input Signals

These signals are address and command signals. A00 through A17 (BH1-BS1,BH2-BS2) are address lines which determine memory location. A0 determines which byte is written when Byte Write (DATOB) is executed.

When addresses A18 - A21 are used the following pin assignments are used (Special Bus Operation): A18 - BE2
A19 - BE1
A20 - AP1
A21 - AN1

C0 and C1 are the signals which determine the cycle mode. C1 selects Read or Write Cycle. C0 selcts Byte Write or Full Write.

Master Sync, MSYN, is the Bus control signal which initiates memory cycle when memory is available (BVI).

Initialize, INIT, is used as a clear signal before MSYN occurs. It clears the Control Status Registers (CSR's) for bits 0, 2, 14, and 15 (AA1).

DC LO, when asserted, causes the memory to perform Refresh only. It also allows data retention should the battery back-up voltage be activated (BF2).

Output Signals

SSYN is the Slave Sync signal. It tells the host system that memory is on line and data is ready for the Read Cycle. During the Write cycle, it indicates that address/data has been accepted by memory for processing (BU1).

PB is the signal which indicates that a parity error has been detected.

Bi-directional Signals

D0 through D15 data lines are bi-directional. These 16 lines are used to communicate data information with the Unibus I/O (AC1 through AK1 and AD2 through AM2).

3.3 ADDRESS (FIGURE 3-2)

The NS11L Memory accepts a full 22-bit address with the least significant bit being used to control Byte Write. The address lines to the memory are single rail and the addressing mode is random. Address signals are identified as A0 through A21 (See Figure 3-2.

A0 is used in the Byte Write mode as the byte selection control bit. A1 through A21 can be decoded across a range of addresses from zero through 2,097,152 locations in memory. The extention of memory addressing through 2 Mega Words is achieved by the setting of Switch S2-7, which enables the buffer for bits A18 through A21 and allows them to be included in the address certification process.

Four Buffer chips receive the address from the bus. The address is stable on the Bus for 75 nsec, prior to receipt of MSYNC, the Master Sync pulse. During this time it is processed through the address selection circuitry (see Figure 3-2). The address buffers receive and pass all inputs from the bus to the

Address Latch, which is transparent until the Selection process is completed.

A0 through A17 are passed through the Address Latch chips. A1 through A14 go directly to the RAS/CAS Address Multiplexer where they select the Row and Column RAM address. This is discussed in greater detail later in this section.

A13 through A21 are presented at the Starting Address Select circuitry and compared with the initial address entered in the nine switch positions located on Switches S1 and S2. These nine switch positions represent the minimum bus address to which the card can respond. When the Starting Address Selection process is complete, one of two conditions has been recognized:

- The bus address is either less than the minimum address configuration set by S1-1 through S1-8, S2-8.
- Or it is equal to, or greater than, the minimum switch settings.

If the address is less than the switch settings, it is rejected and no further action is taken. If, however, the address is found to be equal to or greater than the minimum switch setting, the Starting Address Select function outputs a normalized address. This address is the difference between the bus address and the address set by the switches. If the normalized address (NA14-NA17) is in the range set by the Memory Size Select circuitry (value set by S3-5 thru S3-8), the +ADDR SEL signal

is generated. The +ADDR SEL signal, when enabled by MSYNC, latches the address in the Address Latch and begins a memory cycle.

When the two criteria cited above are met, address bits NA15 and NA16 are presented to the Row Decode circuitry which selects a row of RAM on the card.

A1-A7 are multiplexed with A3-A14 to become -Add 0-6, which transmit row address, then column address, during a normal cycle. During the Refresh Cycle the refresh addresses are provided by a refresh address counter.

The I/O Block is an area in Memory that is usually 4K words in size. It is normally located in the top 4K of Memory, i.e., from 124K words to 128K words, using a Unibus interface. It is located at the top of 2M words when interfacing with the Special Bus (from 1.996M to 2M). In the I/O address space, the Memory does not respond to Bus MSYN L unless the on-board CSR has been addressed. The I/O Block has a Size Select Switch which permits selection of 2K, 4K, or 8K words of I/O space. This switch (S2) is set as a part of the installation procedure. (Table 2-4)

CSR Address Selection is accomplished in the I/O region. The CSR, seen by the CPU as an I/O register, has assigned addresses which can be accessed (one of sixteen) by a Bus

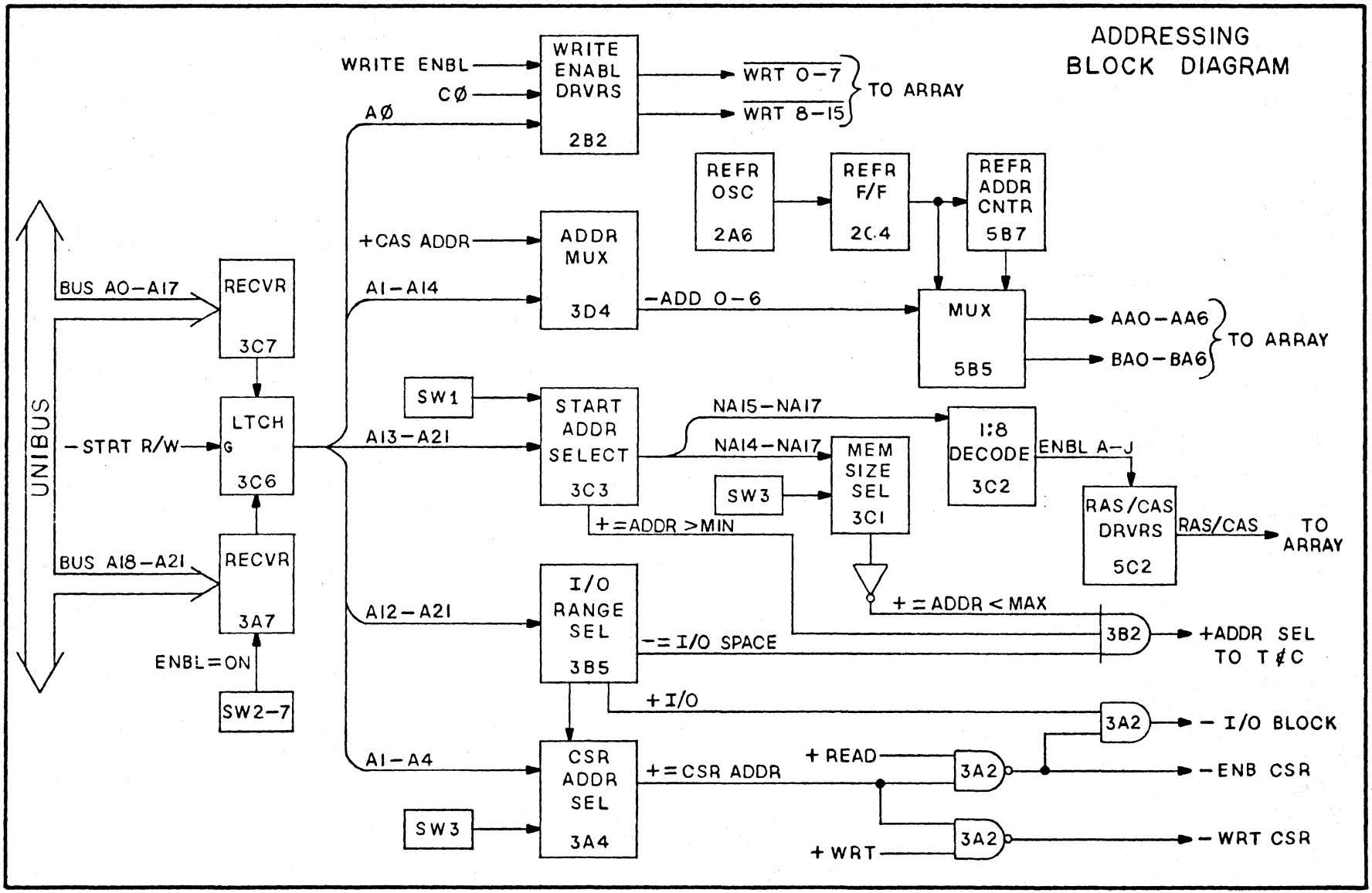

ADDRESSING
BLOCK DIAGRAM
WRITE ENBL
CØ
AØ
WRITE ENABL DRVRS 2B2
WRT 0-7
WRT 8-15
TO ARRAY
REFR OSC 2A6
REFR F/F 2C4
REFR ADDR CNTR 5B7
+CAS ADDR
A1-A14
ADDR MUX 3D4
-ADD 0-6
MUX 5B5
AA0-AA6
BA0-BA6
TO ARRAY
BUS A0-A17
RECVR 3C7
UNIBUS
-STRT R/W
LTCH 3C6
SW1
START ADDR SELECT 3C3
A13-A21
NA15-NA17
NA14-NA17
MEM SIZE SEL 3C1
SW3
1:8 DECODE 3C2
ENBL A-J
RAS/CAS DRVRS 5C2
RAS/CAS
TO ARRAY
+=ADDR >MIN
+=ADDR <MAX
BUS A18-A21
RECVR 3A7
ENBL=ON
SW2-7
A12-A21
I/O RANGE SEL 3B5
-=I/O SPACE
3B2
+ADDR SEL TO T¢C
+I/O
3A2
-I/O BLOCK
A1-A4
CSR ADDR SEL 3A4
+=CSR ADDR
+READ
3A2
-ENB CSR
SW3
+WRT
3A2
-WRT CSR

FIGURE 3-2

Master via the Unibus or Special Bus. This address will contain diagnostic and error information (error address to the nearest 1K) if an error has occured. CSR operation can be disabled by closing S2-3.

The CSR starting address receives an enable from the I/O region (high) and A1-A4. The CSR address select circuitry compares A1-A4 with the CSR Addr switch setting (S3-1,2,3,4). If they are equal, then a +CSR ADDR signal is generated. These inputs combined with +MSYN, +READ or +WRITE produce -WRT CSR or -ENB CSR.

3.4 TIMING AND CONTROL (FIGURE 3-3)

The timing and control circuitry provides the necessary timing and signal control to allow the memory card to run full or refresh cycles. The T and C contains the Refresh arbitration network and refresh oscillator. A bus cycle can be delayed as much as 405ns if the request arrives after a refresh cycle has begun.

The START ENABLE circuit tests the memory card status and is the cycle arbitrator. A memory request from a bus master is initiated only if the following conditions exist: there is no refresh request waiting, there is no cycle presently in progress, the address is in the range of the memory card, and the address is not in the I/O region. If a refresh request had been present, the memory would have done a refresh cycle and then honored the bus request.

If the memory status allows a bus request to be honored, the START ENABLE circuit output is delayed and then sets the START FLIP FLOP. The delay insures that a race condition between a cycle request and a refresh request does not exist. The START F/F sets the FULL CYCLE F/F and enables the read and write SSYN F/F's. The START F/F output also disables the refresh enable circuitry. The FULL CYCLE F/F output enters the delay lines (200ns) which provide the memory card timing.

If a refresh request had occured during a memory cycle, the REFR REQ F/F would have been set. The refresh enable circuitry would have been disabled by the START F/F and the F CYCLE F/F. When both devices have been reset by memory timing at the end of the cycle, the refresh request is allowed to pass through the REFRESH ENABLE circuitry and a refresh cycle is initiated. The REFRESH ENABLE output also blocks any further bus requests until the refresh cycle is terminated.

Refresh of the dynamic RAM's takes place every 15 uSec. The RAM is refreshed to prevent loss of existing DATA. Refresh is accomplished by the selection of a particular Refresh RAS Address, and inhibiting Row Decode so that all rows of RAM are selected. A counter in the Refresh Address Counter and Multiplexer increments once each time a Refresh Cycle is completed. This counter sets up the RAS address selection process for the next Refresh Cycle, thereby stepping the refresh activity completely through the memory every 2 milliseconds.

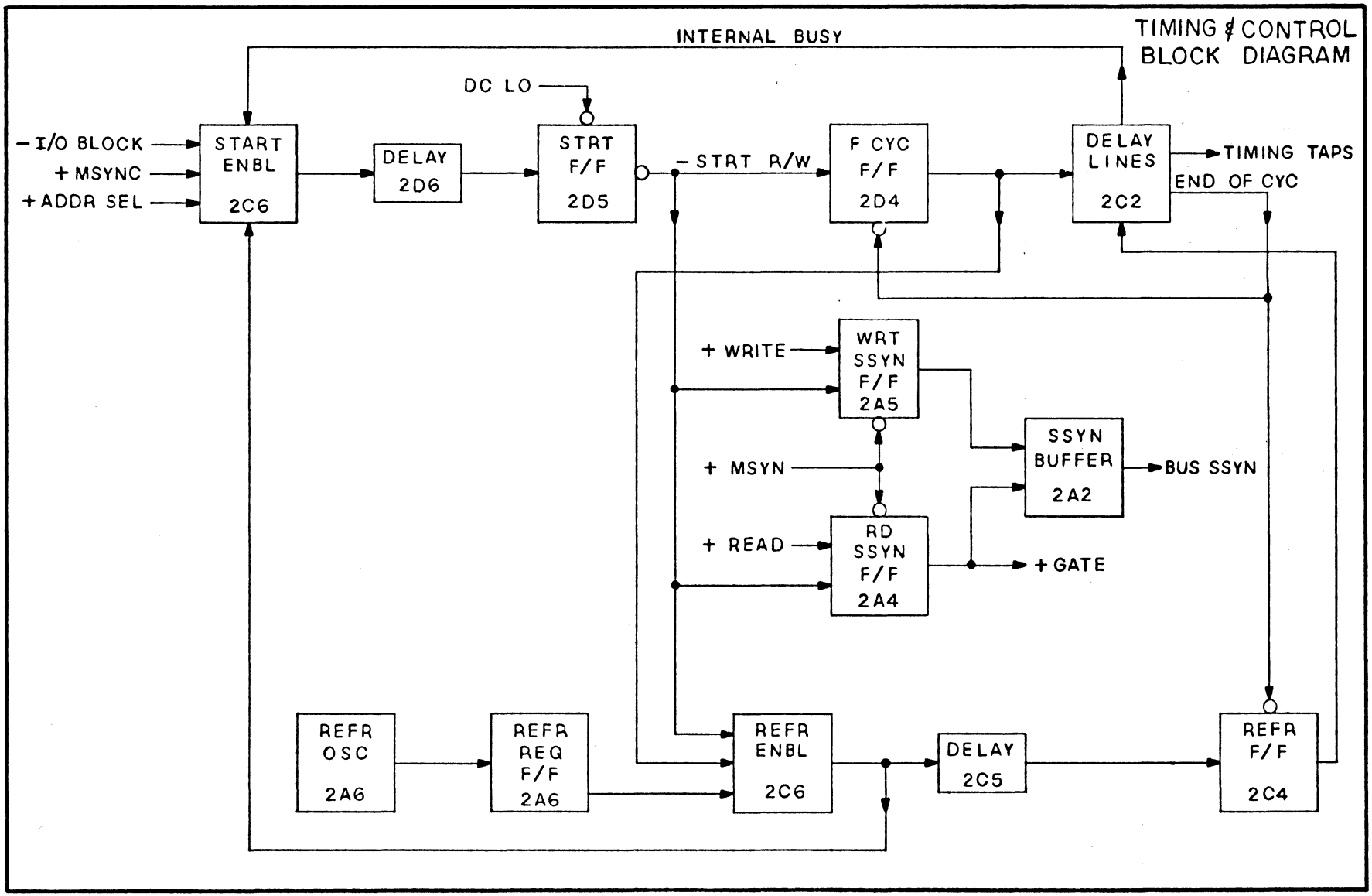

TIMING & CONTROL
BLOCK DIAGRAM
INTERNAL BUSY
DC LO
-I/O BLOCK
+MSYNC
+ADDR SEL
START ENBL 2C6
DELAY 2D6
STRT F/F 2D5
-STRT R/W
F CYC F/F 2D4
DELAY LINES 2C2
TIMING TAPS
END OF CYC
+WRITE
WRT SSYN F/F 2A5
+MSYN
SSYN BUFFER 2A2
BUS SSYN
+READ
RD SSYN F/F 2A4
+GATE
REFR OSC 2A6
REFR REQ F/F 2A6
REFR ENBL 2C6
DELAY 2C5
REFR F/F 2C4

FIGURE 3-3

3.5 MEMORY ARRAY (FIGURE 3-4)

The Memory Array is comprised of 144 16K Dynamic Rams in a 8x18 matrix. Each Byte contains 128Kx9 bits of memory; eight data bits and a parity bit. Addresses AØ thru A6 are common to all Rams. RAS and CAS signals (1 of 8) are common to each row. Basic Array organization is shown in Figure 3-4.

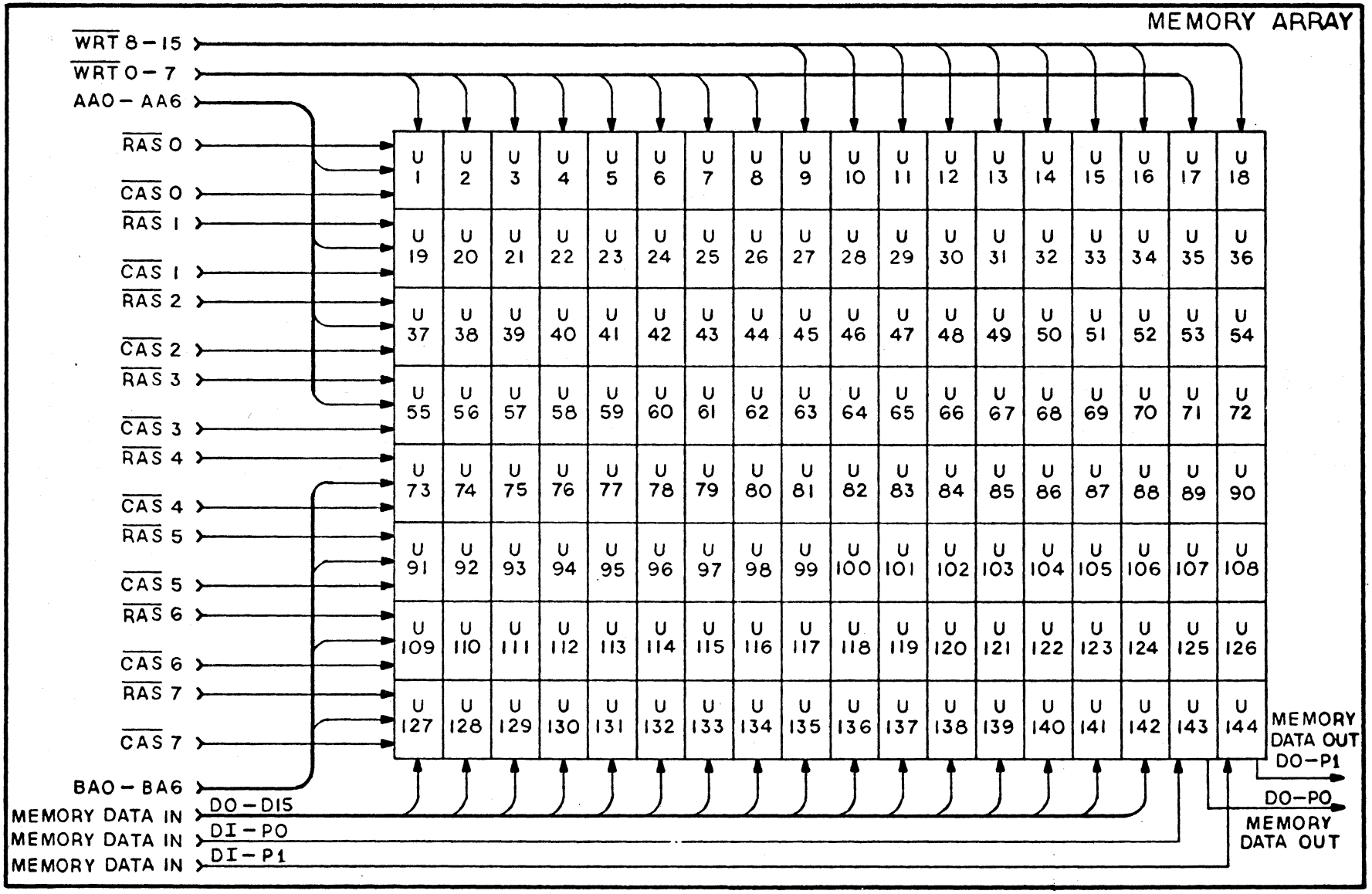

MEMORY ARRAY
WRT 8-15
WRT 0-7
AA0-AA6
RAS 0
CAS 0
RAS 1
CAS 1
RAS 2
CAS 2
RAS 3
CAS 3
RAS 4
CAS 4
RAS 5
CAS 5
RAS 6
CAS 6
RAS 7
CAS 7
BA0-BA6
MEMORY DATA IN
DO-DI5
MEMORY DATA IN
DI-P0
MEMORY DATA IN
DI-P1
U 1 U 2 U 3 U 4 U 5 U 6 U 7 U 8 U 9 U 10 U 11 U 12 U 13 U 14 U 15 U 16 U 17 U 18
U 19 U 20 U 21 U 22 U 23 U 24 U 25 U 26 U 27 U 28 U 29 U 30 U 31 U 32 U 33 U 34 U 35 U 36
U 37 U 38 U 39 U 40 U 41 U 42 U 43 U 44 U 45 U 46 U 47 U 48 U 49 U 50 U 51 U 52 U 53 U 54
U 55 U 56 U 57 U 58 U 59 U 60 U 61 U 62 U 63 U 64 U 65 U 66 U 67 U 68 U 69 U 70 U 71 U 72
U 73 U 74 U 75 U 76 U 77 U 78 U 79 U 80 U 81 U 82 U 83 U 84 U 85 U 86 U 87 U 88 U 89 U 90
U 91 U 92 U 93 U 94 U 95 U 96 U 97 U 98 U 99 U 100 U 101 U 102 U 103 U 104 U 105 U 106 U 107 U 108
U 109 U 110 U 111 U 112 U 113 U 114 U 115 U 116 U 117 U 118 U 119 U 120 U 121 U 122 U 123 U 124 U 125 U 126
U 127 U 128 U 129 U 130 U 131 U 132 U 133 U 134 U 135 U 136 U 137 U 138 U 139 U 140 U 141 U 142 U 143 U 144
MEMORY DATA OUT
DO-P1
DO-P0
MEMORY DATA OUT

FIGURE 3-4

3.6 DATA PATH (FIGURE 3-5)

The read and write data paths are depicted in figure 3-5. During a write cycle, the bus data passes through the transceivers and is latched by the -LTCH and ENBL signal. The data latch outputs are tri-state and are enabled by the -CTRL signal. The data latch outputs are enabled during a WR cycle and for the last half of a RD cycle. The data lines to the array are bi-directional for bits 0-15. The data latch outputs drive the data lines to/from the array and also are tied to the parity generation and check circuit, where the parity bits (DIPØ, DIP1) are generated and sent to the array.

During a read cycle, the data from the array appears on the bi-directional data lines D0-D15. The data goes through the transceiver onto the bus, where it is fed back through the receiver portion of the transceiver and is latched by the data latches after the data stabilizes. The data latch outputs are then enabled, ensuring data on the bus until MSYN is no longer asserted. The data out of the array, along with the parity data outlines (D0PØ, D0P1) is checked by the Parity check circuit for odd parity. If an error is detected, the +error signal is generated and a parity error flag (BUS PB) can be asserted on the bus.

3.7 CSR/Parity Operation (Figure 3-5)

The NS11L memory is capable of performing parity and CSR functions equivalent to the M7850 parity controller. The

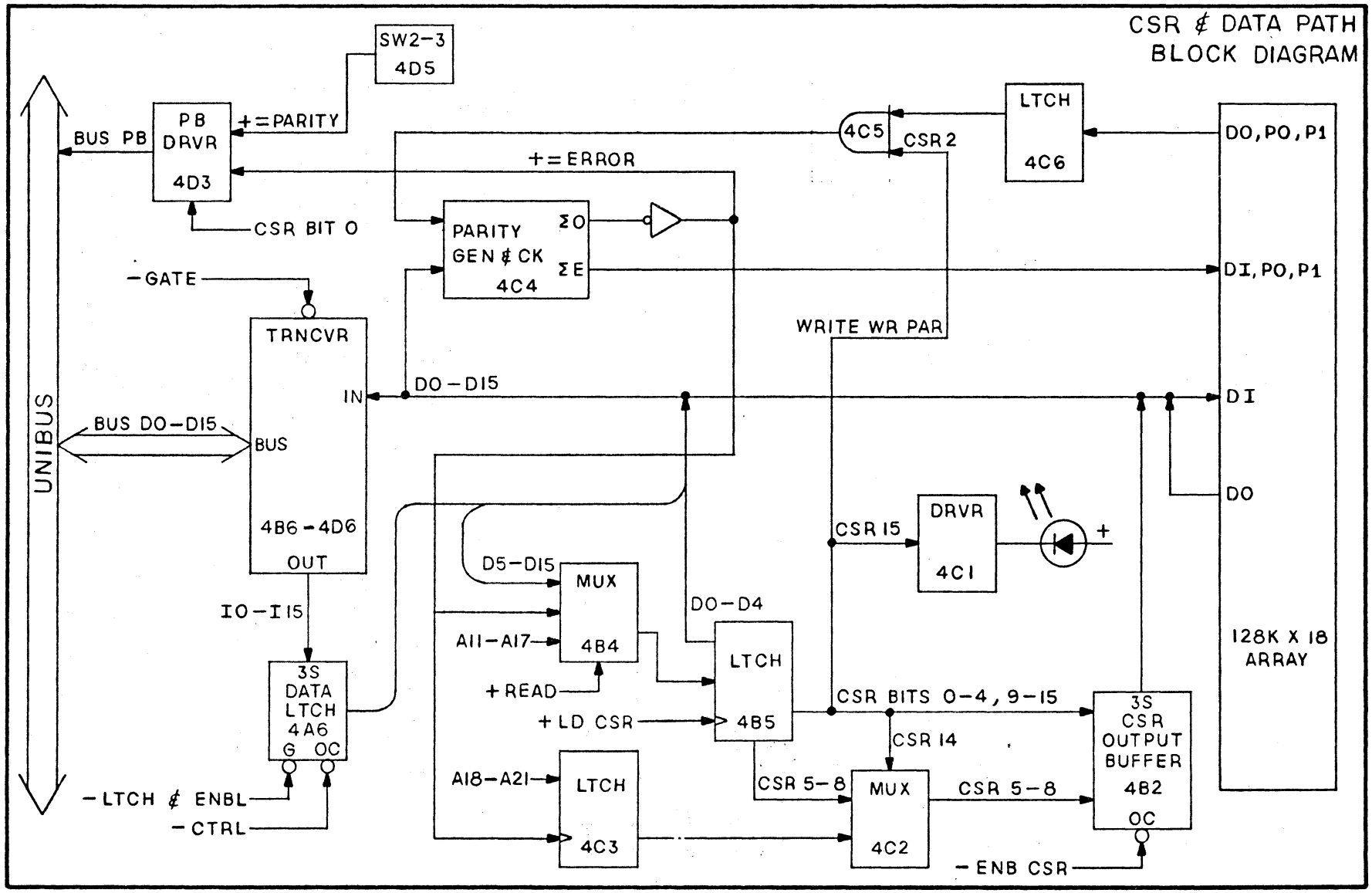
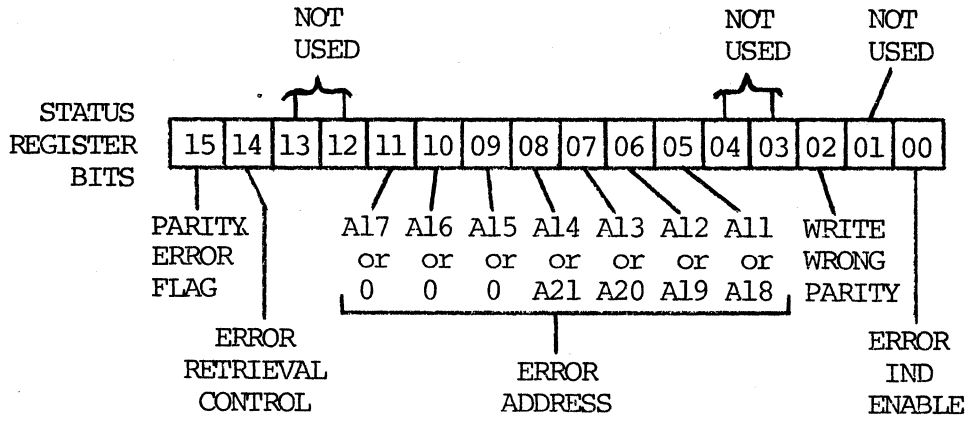

CSR & DATA PATH
BLOCK DIAGRAM
SW2-3
4D5
PB
DRVR
4D3
BUS PB
+=PARITY
+=ERROR
CSR BIT 0
4C5
CSR2
LTCH
4C6
DO,PO,P1
PARITY
GEN & CK
4C4
ΣO
ΣE
DI,PO,P1
-GATE
TRNCVR
IN
DO-D15
WRITE WR PAR
UNIBUS
BUS DO-D15
BUS
4B6-4D6
OUT
DI
DO
CSR 15
DRVR
4C1
D5-D15
MUX
4B4
DO-D4
I0-I15
A11-A17
3S
DATA
LTCH
4A6
G OC
LTCH
4B5
+READ
+LD CSR
CSR BITS 0-4, 9-15
CSR 14
128K X 18
ARRAY
3S
CSR
OUTPUT
BUFFER
4B2
OC
A18-A21
LTCH
4C3
CSR 5-8
MUX
4C2
CSR 5-8
-LTCH & ENBL
-CTRL
-ENB CSR

FIGURE 3-5

memory is compatible with all modified Unibus parity or non-parity memories. The memory does not require an M7850 parity controller; however, an M7850 may be required for other parity memories that may be on the same backplane. The presence of the M7850 does not affect the NS11L.

The control and status register (CSR) in the NS11L allows program control of certain parity functions and contains diagnostic information (error address to nearest 1K) if an error has occurred. The CSR is assigned an address and can be accessed by a bus master via the Unibus or the "special bus". Each NS11L or M7850, in a given backplane, must be assigned a different address. (For address assignment see Table 2-7). Some CSR bits are cleared by the assertion of BUS INIT L as part of the processor power-up sequence. The CSR Bit assignments and operational description are as follows:



BITS 1,3,4,12,13
These Bits are not used and are always read as logical 0's. Writing into these Bits has no effect on the CSR.

BIT 0

Error Indication Enable - This Bit, when set (Logical 1), allows the memory to assert BUS PB L (AN2) when Data is retrieved from memory if a Parity error has been detected. This Bit is a Read/Write Bit and is cleared by BUS INIT L.

BIT 2

Write/Wrong Parity - This Bit, when set, causes the NS11L to Write Wrong Parity (even) when Data is written during a Write cycle (DATO or DATOB). A parity error will then be detected when this Data is read during a Read (DATI or DATIP) cycle. The detection of the parity error causes the parity error flag to be asserted. This Bit is set for diagnostic purposes and is cleared for normal operation. Bit 2 is a Read/Write Bit and is cleared by BUS INIT L.

BITS 5-11

Error Address - Once a parity error has been detected, these Bits contain a partial address of the faulty Data that caused the parity error. In Unibus operation, address Bits A11-A17 are in CSR Bits 5-11 respectively, specifying the faulty Data location to a 1K segment of memory. In special bus operation, the address placed in Bits 5-11 is determined by Bit 14. Bits 5-11 are Read/Write Bits and are not cleared by BUS INIT L.

BIT 14

Special Bus Error Retrieval - This Bit, when set, causes the memory to place A18-A21 of the faulty Data location into CSR Bits 5-8; logical 0's are placed in Bits 9-11. Address Bits A11-A17 are placed in Bits 5-11 when Bit 14 is cleared. In special bus operation, Bit 14 is a Read/Write Bit and is cleared by BUS INIT L. In Unibus operation, Bit 14 is a Read only Bit and is always a logic 0 (clear).

NOTE:

In normal special bus operation, Bit 14 is a logic 0. If a parity error has occured during special Bus operation, the partial address (A11-A21) of the faulty Data is retrieved with the following sequence:

a) Read CSR to obtain A11-A17. Bit 14 should be read as a logical 0.

b) Write a logical 1 in Bit 14 of the CSR.

c) Read CSR to obtain A18-A21. Bit 14 should be read as a logical 1.

BIT 15

Parity Error Bit - This Bit, when set, indicates that a parity error has occurred. Bit 15 is a Read/Write Bit and is cleared by BUS INIT L.

NOTE:

The on-board CSR can be disabled by closing (ON) Switch S2-3.

3.8 DC-TO-DC CONVERTOR (FIGURE 3-6)

The NS11L employs a DC-to-DC convertor switching regulator that operates as flyback convertor in a step-up mode. The basic circuit is shown in Figure 3.6.

When switch S1 closes, the applied voltage drops to almost zero ($V_a=V_x$), and the voltage(Vin-Vs) applied across the inductor, causing the inductor current to increase linearly. Because the applied voltage is less than the output voltage, the diode is reverse-biased and current cannot flow to the output. When the switch opens, the inductor current cannot change instantly and the applied voltage changes to the total of the output voltage plus the diode voltage. At this time current can flow through the diode to the load capacitance and the inductor current decreases at a linear rate, determined by Vout(+ V_D-Vin). Timing adjustments control the average diode current (I_{D1}) so it is equal to the load current. The diode current can only flow during off-time, so the maximum output current is (Ipk/2) ($T_{off}/T_{on}+T_{off}$). If the load current is less than the maximum output current, off-time is increased by a dead time with no current to the output. Input current can flow during both on and off times, so the average input current is always greater than the maximum output current.

In figure 3-6, the designations correspond to schematic reference designations as follows: L=L1, S_1=Q2 thru Q5, D1=CR5, CR6, Co=all capacitance on +12V line.

Main control for the convertor is handled by a pulse width modulator that controls on time, off time, dead time, voltage regulation and soft-start sequence. If the DC-to-DC convertor circuitry should fail, or the convertor input voltage fuse should blow, the amber LED (DS2) will light.

DC TO DC CONVERTOR
BLOCK DIAGRAM

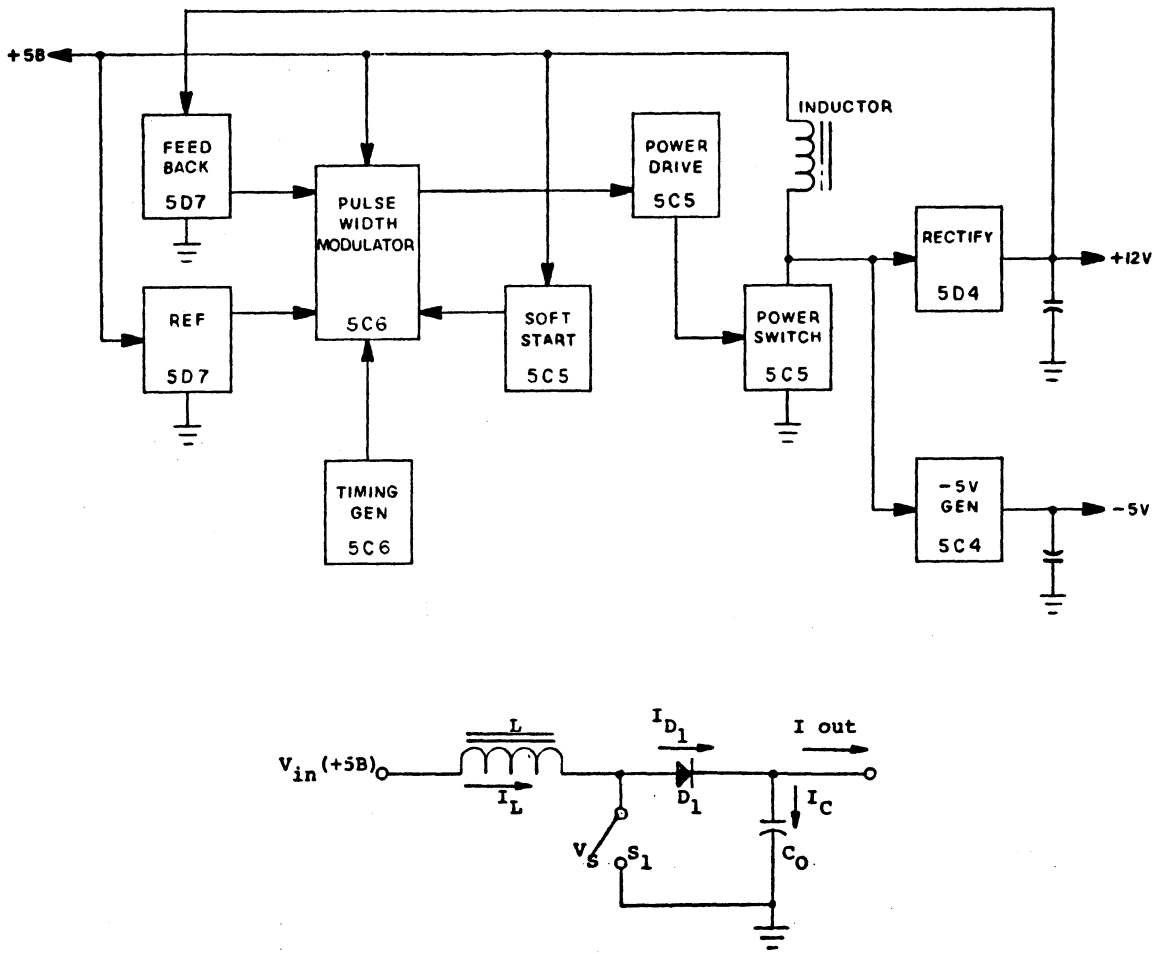


FIGURE 3.6

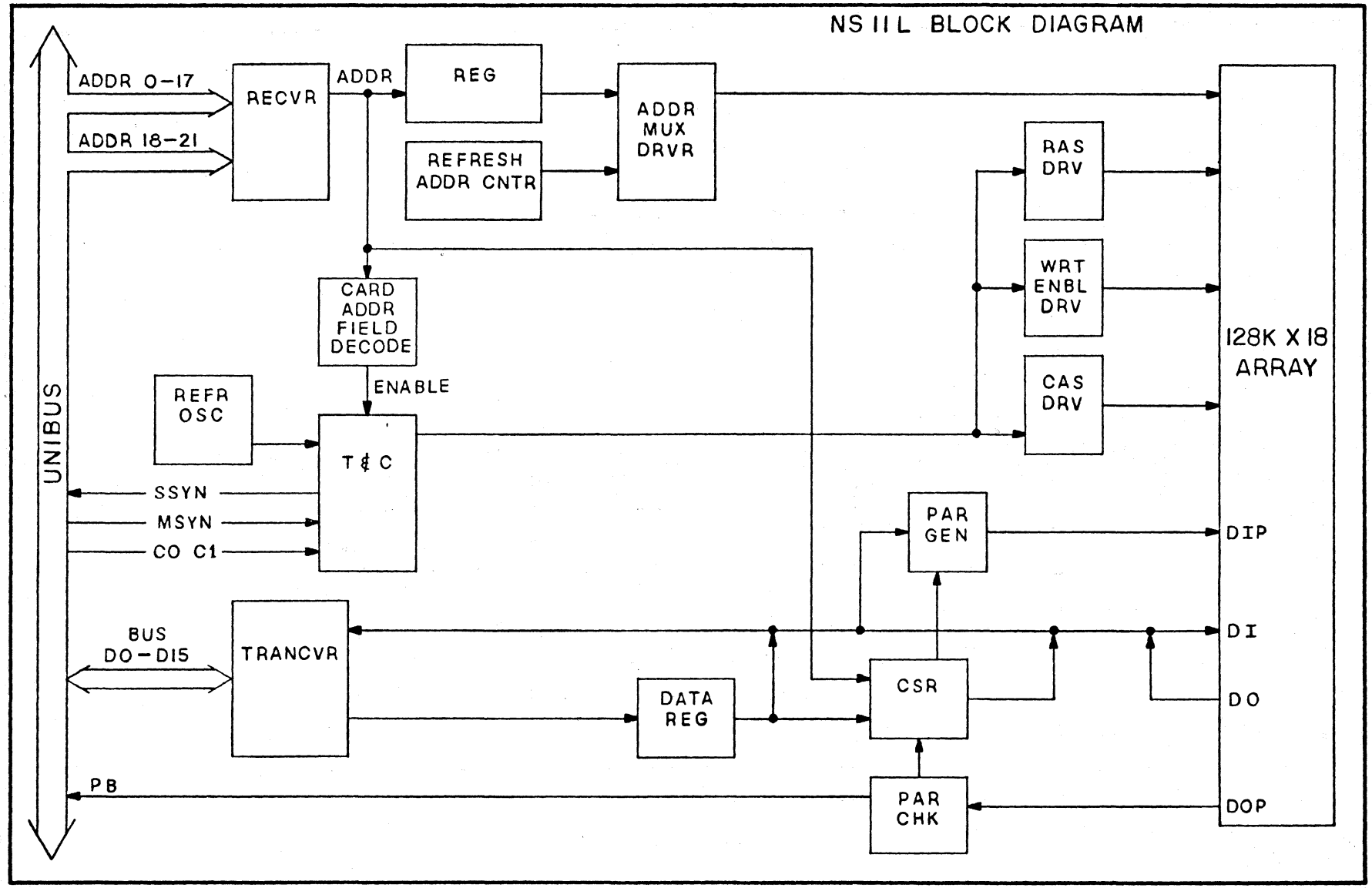

NS11L BLOCK DIAGRAM
UNIBUS
ADDR 0-17
ADDR 18-21
RECVR
ADDR
REG
REFRESH ADDR CNTR
ADDR MUX DRVR
RAS DRV
WRT ENBL DRV
CAS DRV
128K X 18 ARRAY
CARD ADDR FIELD DECODE
ENABLE
REFR OSC
T & C
SSYN
MSYN
CO C1
PAR GEN
DIP
BUS DO-D15
TRANCVR
DI
DO
DATA REG
CSR
PB
PAR CHK
DOP

FIGURE 3-7

SECTION IV

APPENDIX A

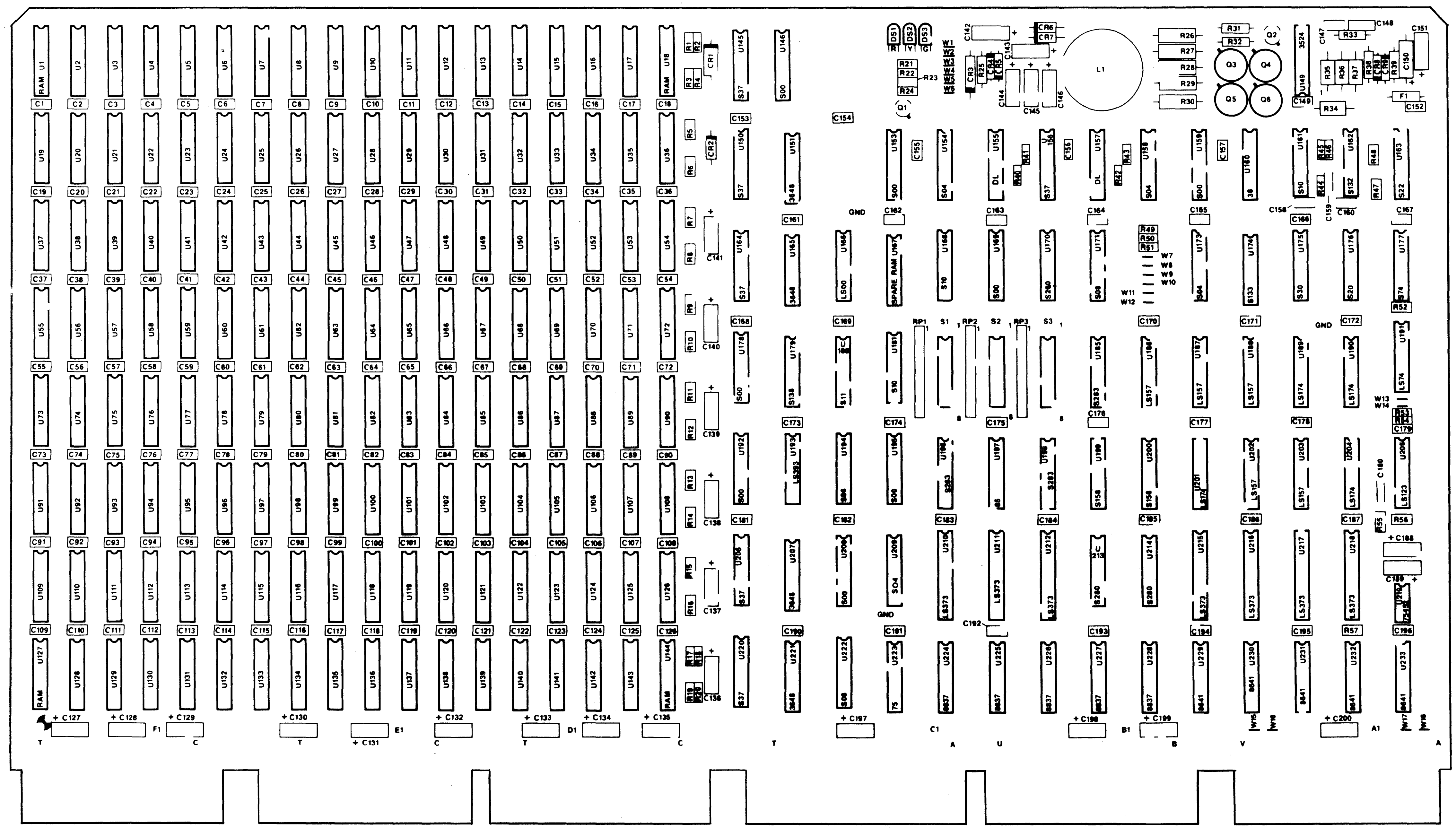
Reference Drawings

This appendix contains the schematic, assembly drawing and bill of material pertaining to the NSllL memory card.

870103841 Schematic

980103841 Assembly and Bill of Materials

REVISIONS			
REV	DATE	ECO NO	APPVD



MATERIAL	DR BY	
FINISH	CHK BY	
	ME	
	EE	
	PE	

NEXT ASSY	USED ON

UNLESS OTHER SPECIFIED

DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES

REMOVE BURRS AND SHARP EDGES BREAK SHARP CORNERS .015 MAX

TOLERANCE		
ANG	2 PL	3 PL

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

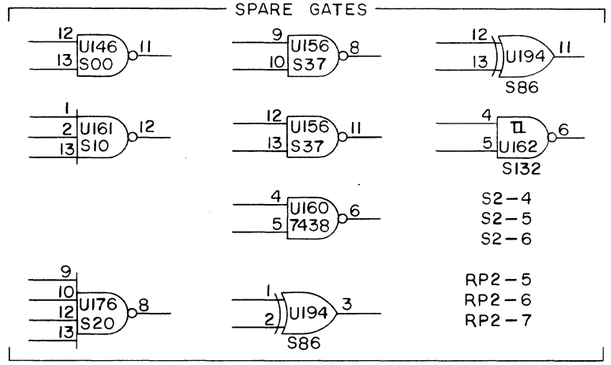
SILKSCREEN LEGEND

SIZE	DR NO	
C	810103841	000

SCALE NONE SHEET ___ OF ___

REVISIONS			
REV	DATE	ECO NO.	APPVD
A	11-3-79	PDD 3564	
B	11-25-79	PCO 23636	

SPARE GATES



S2-4
S2-5
S2-6

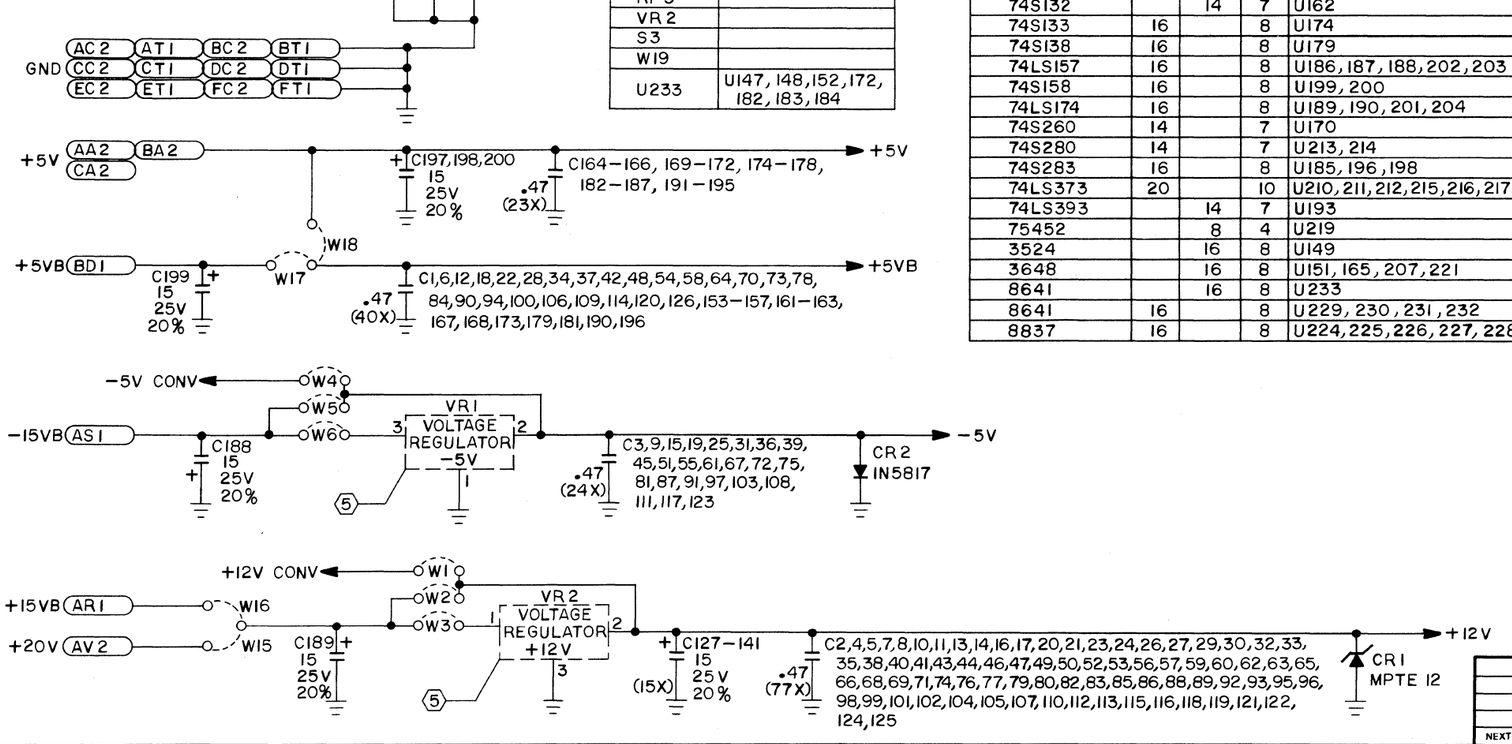
RP2-5
RP2-6
RP2-7

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C200	
CR9	
DS2	
F1	
L1	
Q6	
R57	R21
RP3	
VR2	
S3	
W19	
U233	U147, 148, 152, 172, 182, 183, 184

VOLTAGE TABLE				
DEVICE TYPE	+5V	+5VB	GND	REFERENCE DESIGNATIONS
DELAY LINE 100NS			8,14	U155,157
74S00		14	7	U146,153,159,169,178,192
74S00	14		7	U195,208
74LS00	14		7	U166
74S04		14	7	U154,158
74S04	14		7	U173,209
74S08	14		7	U171,222
74S10		14	7	U161,168
74S10	14		7	U181
74S11	14		7	U180
74S20	14		7	U176
74S22		14	7	U163
74S30	14		7	U175
74S37		14	7	U145,150,156,164,206,220
7438		14	7	U160
74S74		14	7	U177
74LS74		14	7	U191
7475	5		12	U223
7485	16		8	U197
74S86	14		7	U194
74LS123		16	8	U205
74S132		14	7	U162
74S133	16		8	U174
74S138	16		8	U179
74LS157	16		8	U186,187,188,202,203
74S158	16		8	U199,200
74LS174	16		8	U189,190,201,204
74S260	14		7	U170
74S280	14		7	U213,214
74S283	16		8	U185,196,198
74LS373	20		10	U210,211,212,215,216,217,218
74LS393		14	7	U193
75452		8	4	U219
3524		16	8	U149
3648		16	8	U151,165,207,221
8641		16	8	U233
8641	16		8	U229,230,231,232
8837	16		8	U224,225,226,227,228

NOTES: UNLESS OTHERWISE SPECIFIED.

1. CAPACITANCE VALUES IN MICROFARADS, 50V, 10%.
2. RESISTANCE VALUES IN OHMS, 1/8W, 5%.
3. ALL DIODES ARE IN4531.
4. ALL TRANSISTORS ARE 2N3506.
5. FUTURE CIRCUIT CAPABILITY.



MATERIAL		DR. BY J.C. Jacobs	5-2-79
FINISH		CHK. BY	9-5-79
		M.E.	
		E.E.	9-5-79
		P.E.	9-5-79

TOLERANCE: ANG. | 2 PL | 3 PL

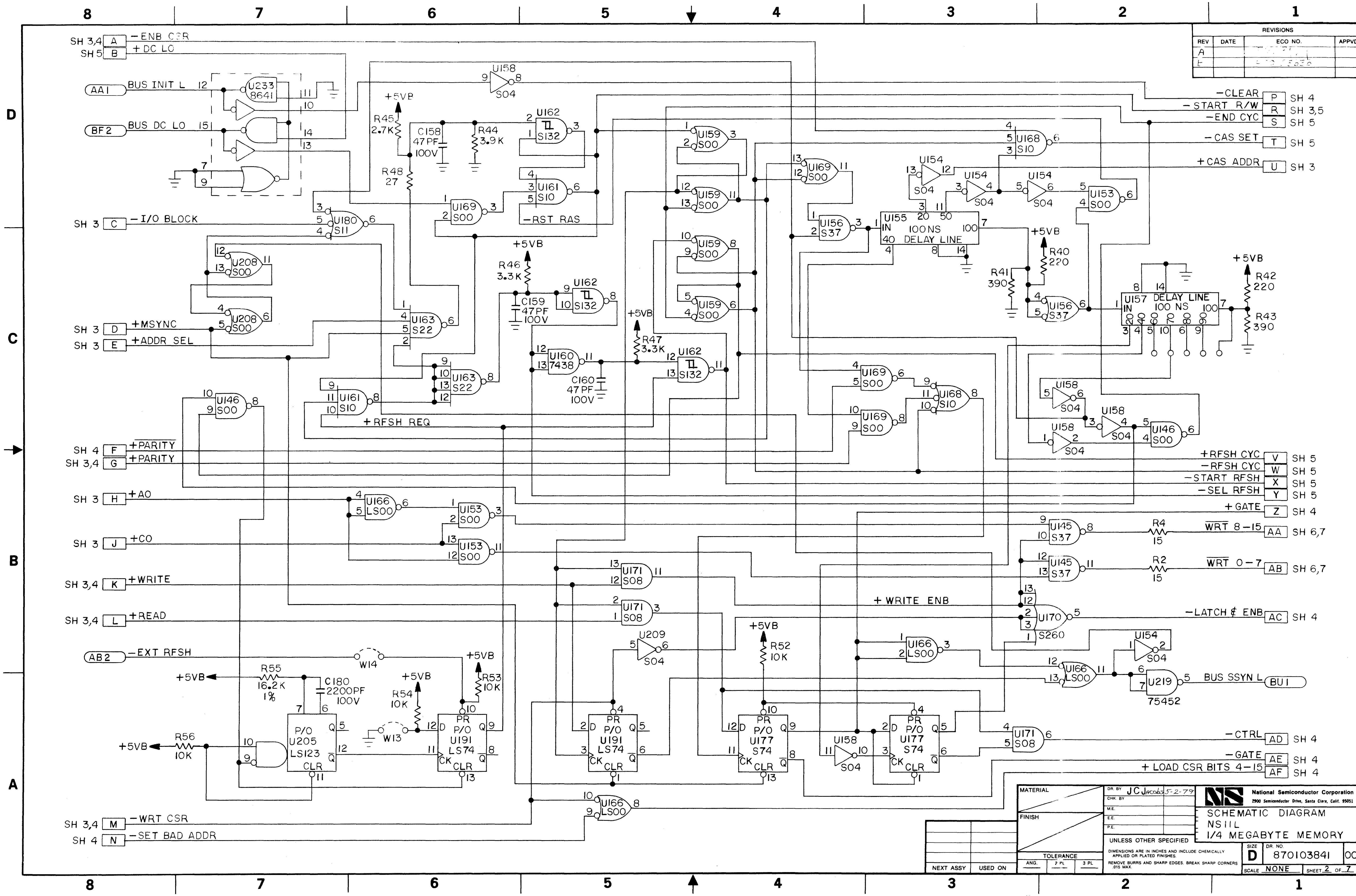
NEXT ASSY | USED ON

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SCHEMATIC DIAGRAM
NS11L
1/4 MEGABYTE MEMORY

SIZE D | DR. NO. 870103841 | 001

SCALE NONE | SHEET 1 OF 7



REVISIONS			
REV	DATE	ECO NO.	APPVD
A			
B			

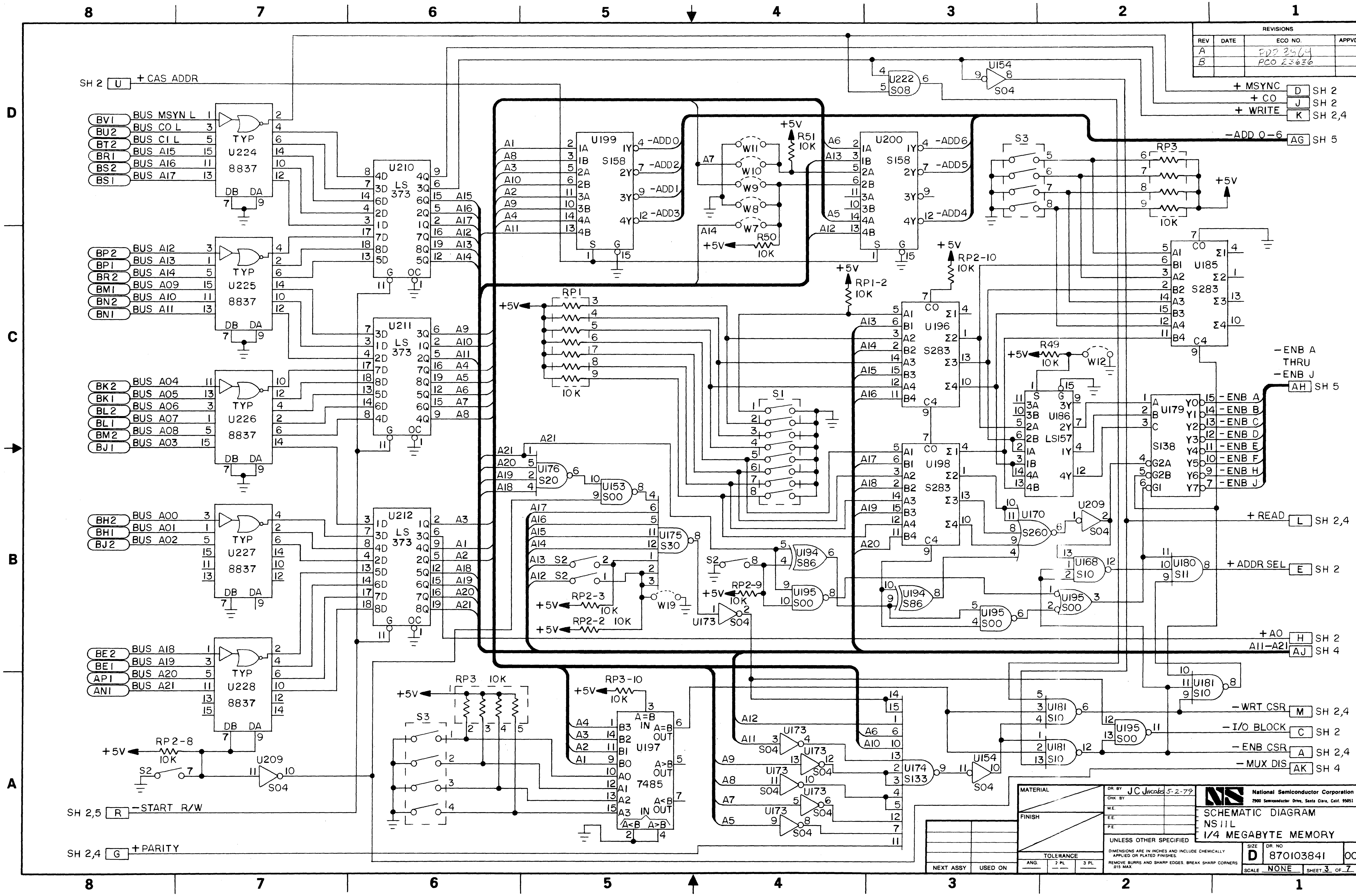
DR BY J C Jacobs 5-2-79

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

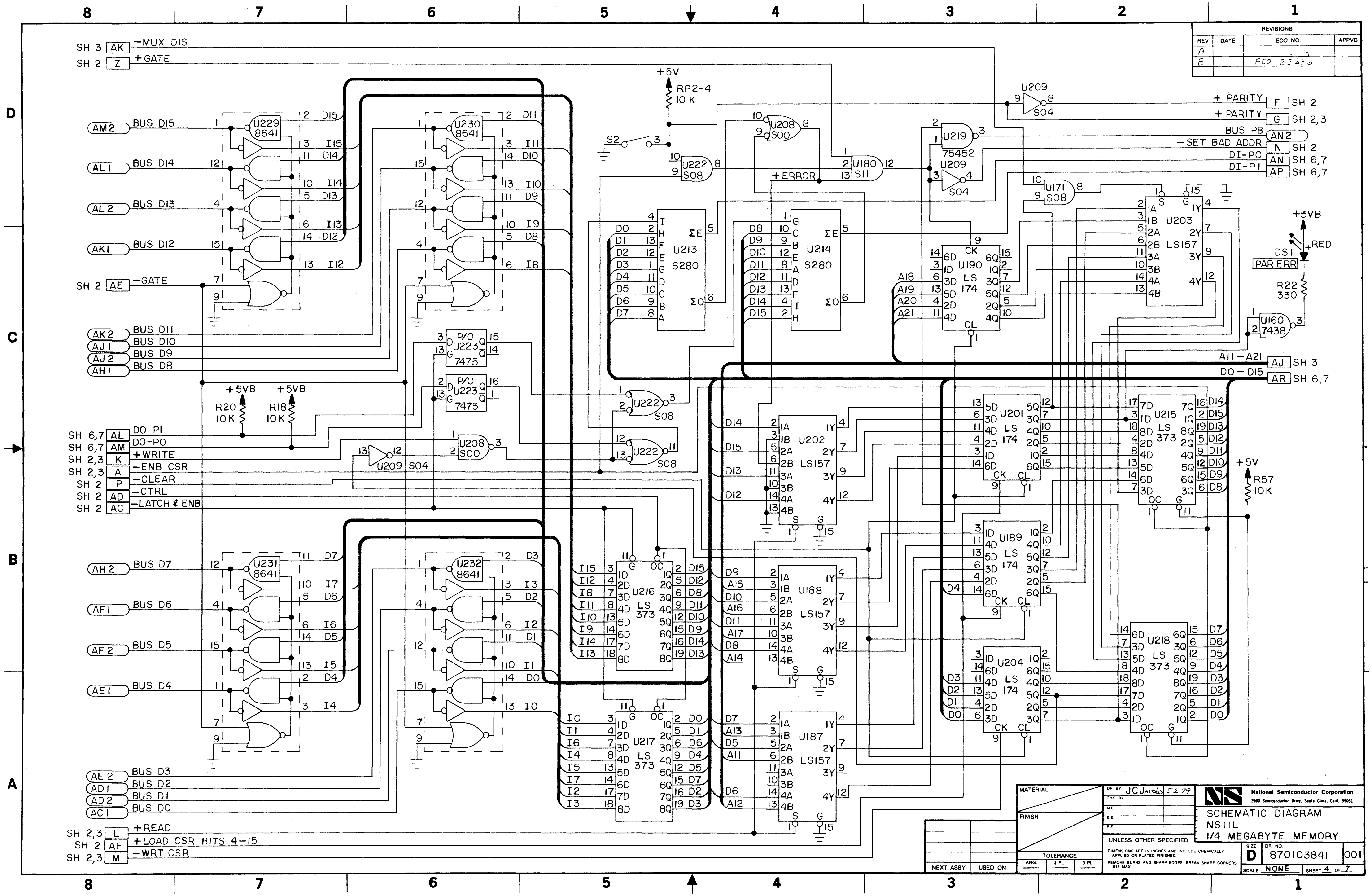
SCHEMATIC DIAGRAM
NS11L
1/4 MEGABYTE MEMORY

UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.

SIZE D DR NO 870103841 001
SCALE NONE SHEET 2 OF 7



REVISIONS
REV | DATE | ECO NO. | APPVD
A | | PDP 3564
B | | PCO 23636
SH 2 U +CAS ADDR
+MSYNC D SH 2
+CO J SH 2
+WRITE K SH 2,4
-ADD 0-6 AG SH 5
-ENB A THRU -ENB J AH SH 5
+READ L SH 2,4
+ADDR SEL E SH 2
+A0 H SH 2
A11-A21 AJ SH 4
-WRT CSR M SH 2,4
-I/O BLOCK C SH 2
-ENB CSR A SH 2,4
-MUX DIS AK SH 4
SH 2,5 R -START R/W
SH 2,4 G +PARITY
BV1 BUS MSYN L
BU2 BUS CO L
BT2 BUS C1 L
BR1 BUS A15
BS2 BUS A16
BS1 BUS A17
BP2 BUS A12
BP1 BUS A13
BR2 BUS A14
BM1 BUS A09
BN2 BUS A10
BN1 BUS A11
BK2 BUS A04
BK1 BUS A05
BL2 BUS A06
BL1 BUS A07
BM2 BUS A08
BJ1 BUS A03
BH2 BUS A00
BH1 BUS A01
BJ2 BUS A02
BE2 BUS A18
BE1 BUS A19
AP1 BUS A20
AN1 BUS A21
TYP U224 8837
TYP U225 8837
TYP U226 8837
TYP U227 8837
TYP U228 8837
U210 LS 373
U211 LS 373
U212 LS 373
U199 S158
U200 S158
U196 S283
U198 S283
U185 S283
U186 LS157
U179 S138
U197 7485
National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051
DR BY JC Jacobs 5-2-79
SCHEMATIC DIAGRAM
NS11L
1/4 MEGABYTE MEMORY
UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.
SIZE D DR. NO 870103841 001
SCALE NONE SHEET 3 OF 7
MATERIAL
FINISH
TOLERANCE
NEXT ASSY USED ON


REVISIONS
REV DATE ECO NO. APPVD
B ECO 23620
SH 3 AK -MUX DIS
SH 2 Z +GATE
+5V
RP2-4 10K
S2
U222 S08
U208 S00
+ERROR
U180 S11
U209 S04
U219 75452
U171 S08
+PARITY F SH 2
+PARITY G SH 2,3
BUS PB AN2
-SET BAD ADDR N SH 2
DI-PO AN SH 6,7
DI-PI AP SH 6,7
AM2 BUS D15
AL1 BUS D14
AL2 BUS D13
AK1 BUS D12
SH 2 AE -GATE
U229 8641
U230 8641
U213 S280
U214 S280
U190 LS 174
U203 LS157
+5VB
DS1 PAR ERR
RED
R22 330
U160 7438
AK2 BUS D11
AJ1 BUS D10
AJ2 BUS D9
AH1 BUS D8
U223 7475
A11-A21 AJ SH 3
D0-D15 AR SH 6,7
R20 10K
R18 10K
SH 6,7 AL DO-PI
SH 6,7 AM DO-PO
SH 2,3 K +WRITE
SH 2,3 A -ENB CSR
SH 2 P -CLEAR
SH 2 AD -CTRL
SH 2 AC -LATCH & ENB
U202 LS157
U201 LS 174
U215 LS 373
R57 10K
AH2 BUS D7
AF1 BUS D6
AF2 BUS D5
AE1 BUS D4
U231 8641
U232 8641
U216 LS 373
U188 LS157
U189 LS 174
U204 LS 174
U218 LS 373
U217 LS 373
U187 LS157
AE2 BUS D3
AD1 BUS D2
AD2 BUS D1
AC1 BUS D0
SH 2,3 L +READ
SH 2 AF +LOAD CSR BITS 4-15
SH 2,3 M -WRT CSR
MATERIAL
FINISH
TOLERANCE
NEXT ASSY USED ON
DR BY JC Jacobs 5-2-79
UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX
National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051
SCHEMATIC DIAGRAM
NS11L
1/4 MEGABYTE MEMORY
SIZE D
DR NO 870103841 001
SCALE NONE
SHEET 4 OF 7

REVISIONS			
REV	DATE	ECO NO.	APPVD
A			
B			

+5VB
F1 4.0 AMP
C151 33 35V 20%
C152 .47
C149 .47
R32 470 1/4W
R30 36 1/2 W
L1 150µH
R31 2.2K 1/4W
C146 33 35V 20%
CR6 IN5817
CR7 IN5817
C144 33 35V,20%
C145 33 35V,20%
+12V CONV
-5V CONV
C143 22 35V,20%
CR5
CR4
C142 33 35V 20%
R25 150 1/4 W
CR3 IN5231B
R24 47K
Q1 2N5434
R23 330
DS2 YELLOW CONV
U158 S04
+DC LO B SH 2

U149 SG3524
VREF VIN C1 C2 NI E1 E2 INV COMP -CL +CL RT CT OV OSC
R36 2.21K 1%
R37 2.21K 1%
R34 8.87K 1%
R35 2.21K 1%
R33 10K 1/4 W
C147 4700PF 100V
C148 1000PF 100V
R38 47K 1/4W
CR9
CR8
R39 1M 1/4W
C150 4.7 10V,20%
Q2 2N4014
Q3
Q4
Q5
Q6
R27 1 1/2W
R26 1 1/2W
R29 1 1/2W
R28 1 1/2W

SH 2 W -RFSH CYC

U165 3648 AI BI A2 B2 A3 B3 A4 B4 S OC YI Y2 Y3 Y4
-ADD 0 -ADD 2 -ADD 1 -ADD 3
AA0 AA2 AA1 AA3

U151 3648 AI BI A2 B2 A3 B3 A4 B4 S OC YI Y2 Y3 Y4
-ADD 6 -ADD 5 -ADD 4
AA6 AA5 AA4

U207 3648 AI BI A2 B2 A3 B3 A4 B4 S OC YI Y2 Y3 Y4
-ADD 0 -ADD 2 -ADD 1 -ADD 3
BA0 BA2 BA1 BA3

U221 3648 AI BI A2 B2 A3 B3 A4 B4 S OC YI Y2 Y3 Y4
-ADD 6 -ADD 5 -ADD 4
BA6 BA5 BA4

+RFSH CYC
SH 2 V
UI93 LS393 2A 1A 2QA 2QB 2QC 2QD 1QA 1QB 1QC 1QD CLR-1 CLR-2

-ENB A
-ENB B
-ENB C
-ENB D
-ENB E
-ENB F
-ENB H
-ENB J
U178 S00
U192 S00

U150 S37
U164 S37
U206 S37
U220 S37
R1 R3 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R19 15
CAS 0 AW SH 6
RAS 0 AX SH 6
CAS 1 AU SH 6
RAS 1 AV SH 6
CAS 2 AY SH 6
RAS 2 AZ SH 6
CAS 3 AS SH 6
RAS 3 AT SH 6
AA0 – AA6
BA0 – BA6 BA SH 6,7
CAS 4 BH SH 7
RAS 4 BJ SH 7
CAS 5 BB SH 7
RAS 5 BC SH 7
CAS 6 BD SH 7
RAS 6 BE SH 7
CAS 7 BF SH 7
RAS 7 BG SH 7

U145 S37
U146 S00
+CAS TIME
+RAS TIME

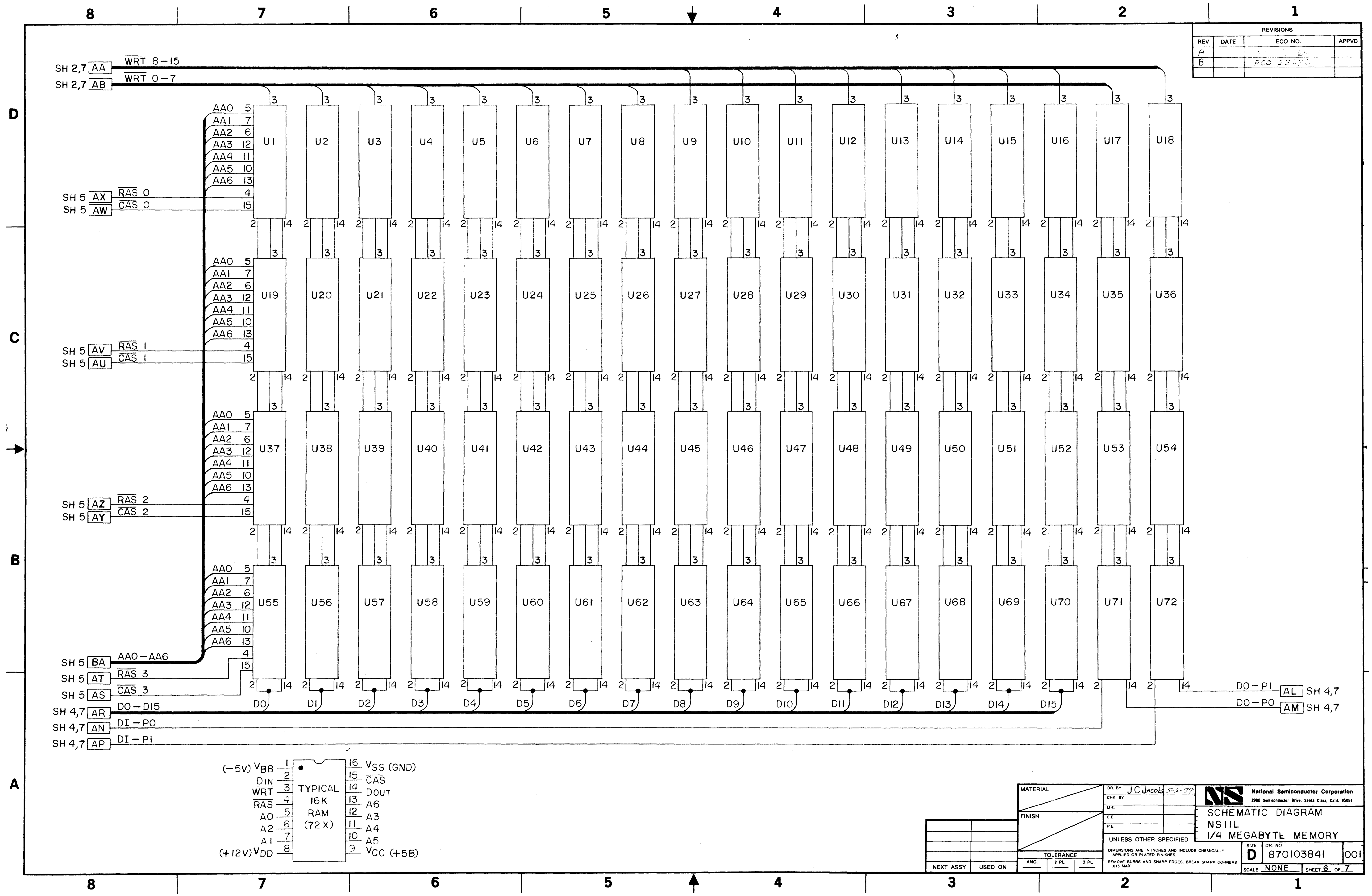
SH 2 Y -SEL RFSH
SH 3 AG -ADD 0-6
SH 3 AH -ENB A-J
SH 2 T -CAS SET
SH 2 S -END CYC
SH 2,3 R -START R/W
SH 2 X -START RFSH

MATERIAL	DR. BY JC Jacobs 5-2-79
FINISH	CHK. BY
	M.E.
	E.E.
	P.E.
UNLESS OTHER SPECIFIED	
TOLERANCE ANG. — 2 PL — 3 PL —	DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES. REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX
NEXT ASSY	USED ON

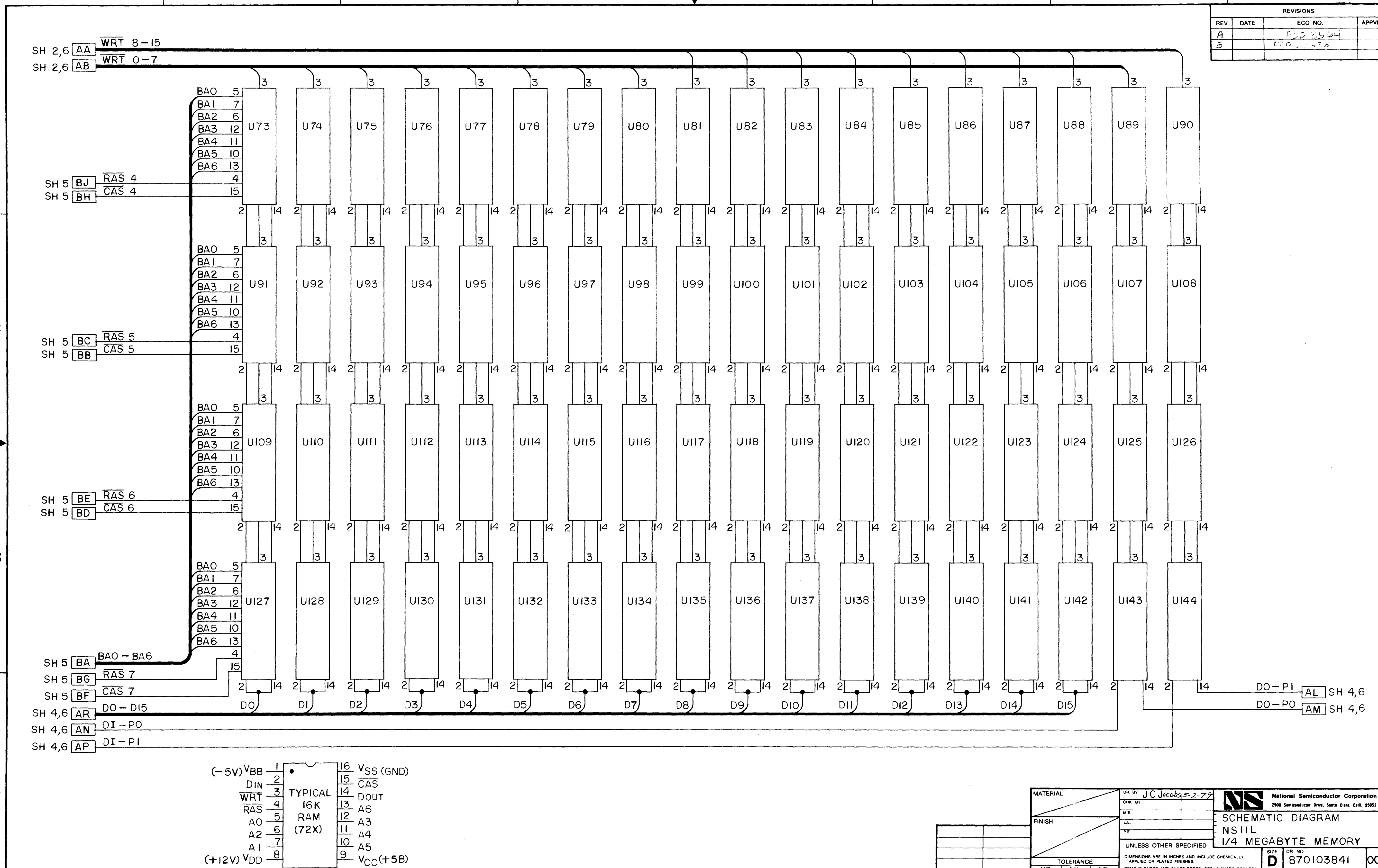
National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SCHEMATIC DIAGRAM
NSIIL
1/4 MEGABYTE MEMORY

SIZE D | DR NO. 870103841 | 001
SCALE NONE | SHEET 5 OF 7



REVISIONS
REV DATE ECO NO. APPVD
A
B
SH 2,7 AA WRT 8-15
SH 2,7 AB WRT 0-7
AA0 5
AA1 7
AA2 6
AA3 12
AA4 11
AA5 10
AA6 13
SH 5 AX RAS 0 4
SH 5 AW CAS 0 15
SH 5 AV RAS 1
SH 5 AU CAS 1
SH 5 AZ RAS 2
SH 5 AY CAS 2
SH 5 BA AA0-AA6
SH 5 AT RAS 3
SH 5 AS CAS 3
SH 4,7 AR D0-D15
SH 4,7 AN DI-P0
SH 4,7 AP DI-P1
D0-P1 AL SH 4,7
D0-P0 AM SH 4,7
U1 U2 U3 U4 U5 U6 U7 U8 U9 U10 U11 U12 U13 U14 U15 U16 U17 U18
U19 U20 U21 U22 U23 U24 U25 U26 U27 U28 U29 U30 U31 U32 U33 U34 U35 U36
U37 U38 U39 U40 U41 U42 U43 U44 U45 U46 U47 U48 U49 U50 U51 U52 U53 U54
U55 U56 U57 U58 U59 U60 U61 U62 U63 U64 U65 U66 U67 U68 U69 U70 U71 U72
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
(-5V) VBB 1
DIN 2
WRT 3
RAS 4
A0 5
A2 6
A1 7
(+12V) VDD 8
TYPICAL 16K RAM (72 X)
16 VSS (GND)
15 CAS
14 DOUT
13 A6
12 A3
11 A4
10 A5
9 VCC (+5B)
MATERIAL
FINISH
NEXT ASSY USED ON
TOLERANCE ANG. 2 PL 3 PL
DR BY J C Jacobs 5-2-79
CHK BY
UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX
National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051
SCHEMATIC DIAGRAM
NS11L
1/4 MEGABYTE MEMORY
SIZE D DR NO 870103841 001
SCALE NONE SHEET 6 OF 7



REVISIONS			
REV	DATE	ECO NO.	APPVD
A		FDD 3564	
5		F.O. ...	

MATERIAL	DR. BY J C Jacobs 5-2-79
FINISH	CHK BY
	M.E.
	E.E.
	P.E.
NEXT ASSY	USED ON
TOLERANCE ANG. 2 PL 3 PL	UNLESS OTHER SPECIFIED

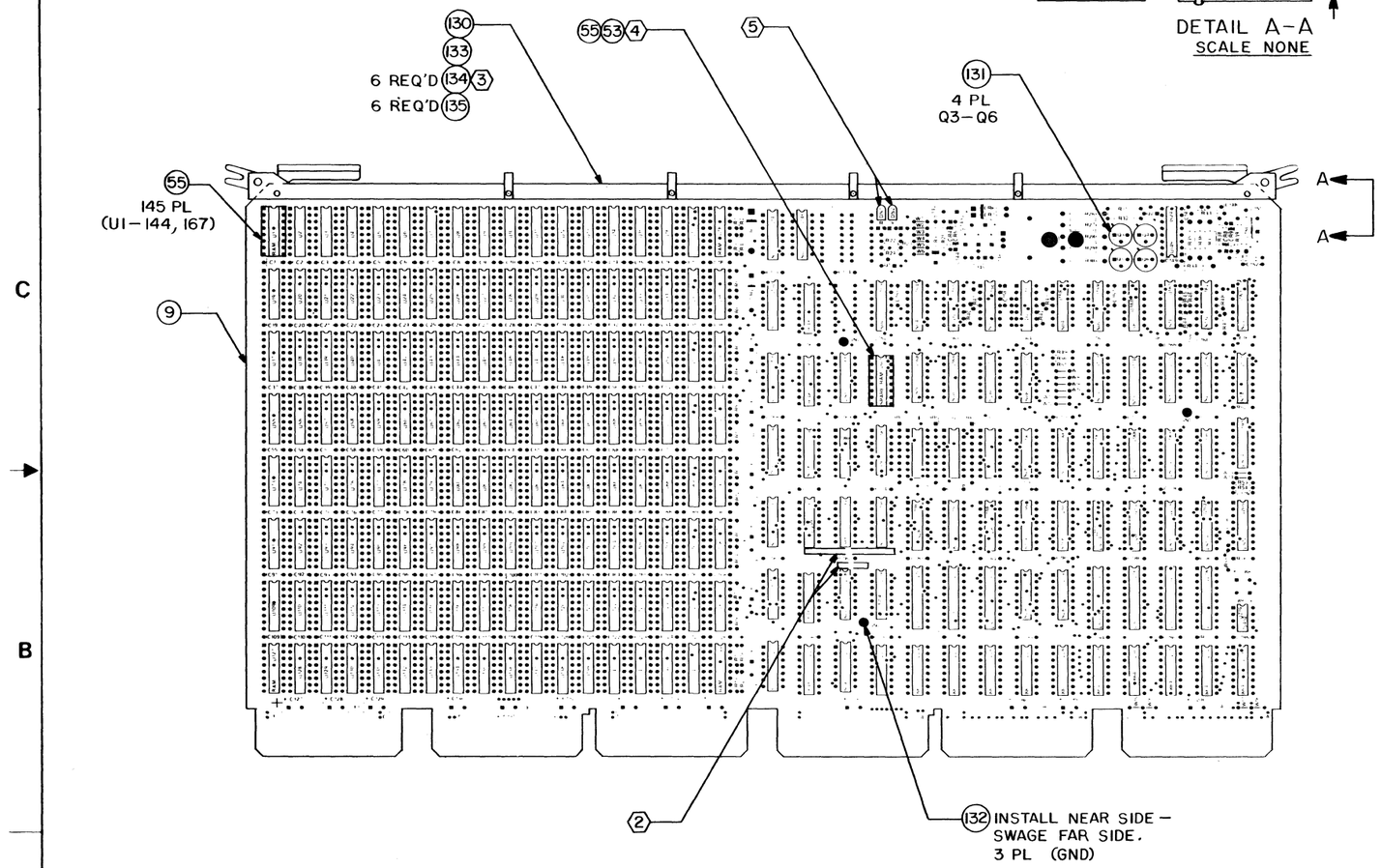
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.

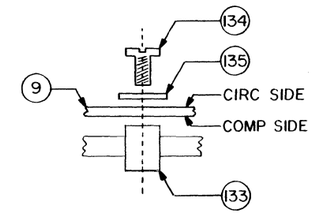
National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

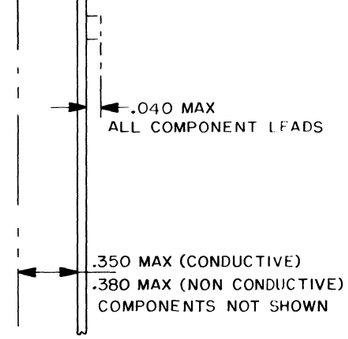
SCHEMATIC DIAGRAM
NS11L
1/4 MEGABYTE MEMORY

SIZE D | DR. NO 870103841 | 001
SCALE NONE | SHEET 7 OF 7

REVISIONS			
REV.	DATE	ECO NO	APPVD
A	11-78	PDD 3564	
B	12-15-78	PCO 23636	
C	12-6-79	PCO 24003	
D	12-7-79	PCO 24005	
E	2-6-80	PCO 24009	







NOTES:

1. ASSEMBLE AND SOLDER PER NSC SPEC. 429101895.
2. MARK ASSY. PART NO. 3841, DASH NO., REV. LEVEL AND S/N WITH .12–.18 HIGH CHARACTERS WHERE SHOWN.
3. APPLY ITEM 130 (LOCTITE) TO TAPPED HOLES IN ITEM 133 (STIFFENER) PRIOR TO INSERTING ITEM 134 (SCREWS).
4. INSTALL ITEM 53 AFTER PRE–TESTING PER TEST SPEC. 425103841.
5. 1. SHORT LEG IS CATHODE.
   2. CATHODE TO SQUARE PAD.
   3. BEND PER DETAIL A–A BEFORE INSTALLATION.
6. ALL JUMPER OPTIONS SHOULD BE INSTALLED USING ITEM 126.
7. INSTALL MEMORY I.C.'s ACCORDING TO THE TABULATED DATA CHART. THE MEMORY ELEMENT P/N IS ASSIGNED IN THE MEMORY ELEMENT P/N CHART.
8. INSTALL JUMPERS ACCORDING TO THE FACTORY INSTALL JUMPER TABLE.
9. AFTER FINAL TEST, INSTALL/REMOVE JUMPERS AS DEFINED BY THE MARKETING CONFIGURATION CODE TABLE.
10. VERSION NUMBERS ARE ESTABLISHED TO THE FOLLOWING CODE: – X,Y,Z.

DR BY J.C. Jurenka 7-16-79
CHK
APPD
MFG

National Semiconductor Corporation

P.C.B. ASSEMBLY DRAWING
NSIIL
1/4 MEGABYTE MEMORY

D 980103841 000

1:1 1 2

REVISIONS			
REV	DATE	ECO NO.	APPVD
A	9-15-77	PDD 3564	
B		PCO 23636	
C	2-6-79	PCO 24003	
D	2-7-79	PCO 24005	
E	2-6-80	PCO 24009	

⑦ TABULATED DATA CHART

VERSION ⑩	QTY	POPULATED MEMORY ELEMENT LOCATIONS REFERENCE DESIGNATIONS	CAPACITY 16K RAM	CAPACITY 8K RAM	OPTION
-X01	144	U1 - U144	128K	64K	PARITY
-X02	126	U1 - U126	112K	56K	
-X03	108	U1 - U108	96K	48K	
-X04	90	U1 - U90	80K	40K	
-X05	72	U1 - U72	64K	32K	
-X06	54	U1 - U54	48K	24K	
-X07	36	U1 - U36	32K	16K	
-X08	18	U1 - U18	16K	8K	
-X11	128	U1-16, U19-34, U37-52, U55-70, U73-88, U91-106, U109-124, U127-142	128K	64K	NON-PARITY
-X12	112	U1-16, U19-34, U37-52, U55-70, U73-88, U91-106, U109-124	112K	56K	
-X13	96	U1-16, U19-34, U37-52, U55-70, U73-86, U91-106	96K	48K	
-X14	80	U1-16, U19-34, U37-52, U55-70, U73-88	80K	40K	
-X15	64	U1-16, U19-34, U37-52, U55-70	64K	32K	
-X16	48	U1-16, U19-34, U37-52	48K	24K	
-X17	32	U1-16, U19-34	32K	16K	
-X18	16	U1-16	16K	8K	

X = MEMORY CHIP TYPE
(SEE MEMORY ELEMENT PART NUMBER CHART)

X = 0 16K
X = 1 8K PARTIAL RH
X = 2 8K PARTIAL LH

Y = OPTION

Y = 0 PARITY
Y = 1 NON-PARITY

Z = MEMORY ROW POPULATION

Z = 1 ROWS 1-8
Z = 2 ROWS 1-7
Z = 3 ROWS 1-6
Z = 4 ROWS 1-5
Z = 5 ROWS 1-4
Z = 6 ROWS 1-3
Z = 7 ROWS 1-2
Z = 8 ROW 1

⑧ FACTORY INSTALLED JUMPER TABLE

⑩ VERSION	JUMPERS INSTALLED	REMARKS
ALL	W1, W4, W18	
-001 THRU -016	W7, W10	16K RAMS
-101 THRU -116	W9, W11, W12	8K PARTIAL, RIGHT HALF
-201 THRU -216	W11, W12	8K PARTIAL, LEFT HALF

⑦ MEMORY ELEMENT PART NUMBER CHART

X ⑩	PART NUMBER	DESCRIPTION
0	482102598-012	16K x 1 DYNAMIC RAM, 200 NS
1	482102989-112	8K x 1 DYN. RAM, PARTIAL RH, 200 NS
2	482103060-112	8K x 1 DYN. RAM, PARTIAL LH, 200 NS

⑨ MARKETING CONFIGURATION CODE TABLE
USER SELECTABLE OPTION JUMPERS

MKTG. CONFIG. CODE	JUMPERS INSTALLED	JUMPERS REMOVED	REMARKS
00	—	—	NO OPTIONS ⑧
01	W17	W18	BATTERY BACKUP

NEXT ASSY	USED ON	MATERIAL	
		FINISH	
		TOLERANCE: ANG. — / PL — 3 PL —	

DR. BY S.C. Jacobs 7-16-79
CHK. BY
M.E.
E.E.
P.E.

UNLESS OTHER SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
REMOVE BURRS AND SHARP EDGES. BREAK SHARP CORNERS .015 MAX.

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

PCB ASSEMBLY DRAWING
NS1IL
1/4 MEGABYTE MEMORY

SIZE D | DR. NO 980103841 | 000
SCALE NONE | SHEET 2 OF 2

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
KEY (1): A = WITH B/M, D = WITHOUT B/M, R = REFERENCE, S = SPECIFICATION
KEY (2)
RELEASED FOR ASSEMBLY
BILL OF MATERIAL NO. 980103841-000

ITEM/ FIND NO	QUANTITY PER ASSEMBLY (000)	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
1								
2								
3	0	04	R		870103841-001	SCHEMATIC DIAGRAM		
4	0	04	R		427103841-001	TEST PROCEDURE		
5	0	04	S		425103841-001	TEST SPEC		
6	0	04	S		426103841-001	PRODUCT SPEC		
7								
8								
9	1	04	D		551103841-002	PC BOARD		
10								
11	1	04			482000354-001	I.C. 74LS00		U166
12	8	04			482000079-001	74S00		U146,153,
13								159,169,178,
14								192,195,208
15	4	04			482000180-001	I.C. 74S04		U154,158,
16								173,209

NOTES:

ENG CHG	REV	A	B	C	D	E
	CHG NO.	POD 3564	PCO 23636	PCO 24003	PCO 24005	PCO 24009
	DATE	7-10-79	10-25-79	12-7-79	12-7-79	2-6-80
	APPR	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

ASSY USAGE REF

WRITTEN BY: D.TAYLOR — DATE — DESIGN — DATE
CHECKED BY — DATE — APPROVED — DATE

TITLE: NS11L ¼ MEGA BYTE MEMORY

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE — BILL OF MATERIAL NO 980103841-000 — SH 1 OF 9

FORM NO. 0011A

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
KEY (1): A = WITH B/M, D = WITHOUT B/M, R = REFERENCE, S = SPECIFICATION
KEY (2)
RELEASED FOR ASSEMBLY
BILL OF MATERIAL NO. 980103841-000

ITEM/ FIND NO	QUANTITY PER ASSEMBLY (000)	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
17	2	04			482100672-001	I.C. 74S08		U171,222
18	3	04			482001344-001	74S10		U161,168,181
19	1	04			482000299-001	74S11		U180
20	1	04			482001345-001	74S20		U176
21	1	04			482000438-001	74S22		U163
22	1	04			482000335-001	74S30		U175
23	6	04			482100777-001	74S37		U145,150,156,
24								164,206,220
25	1	04			482000164-001	7438		U160
26	1	04			482000179-001	74S74		U177
27	1	04			482000365-001	74LS74		U191
28	1	04			482000043-001	7475		U223
29	1	04			482103946-001	7485		U197
30	1	04			482000300-001	74S86		U194
31	1	04			482101175-001	74LS123		U205
32	1	04			482100840-001	I.C. 74S132		U162

NOTES:

ENG CHG	REV	A	B	C	D	E
	CHG NO.	POD 3564	PCO 23636	PCO 24003	24005	PCO 24009
	DATE	—	—	—	—	—
	APPR	—	—	—	—	—

ASSY USAGE REF

WRITTEN BY: D.TAYLOR — DATE — DESIGN — DATE
CHECKED BY — DATE — APPROVED — DATE

TITLE: NS11L ¼ MEGA BYTE MEMORY

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE — BILL OF MATERIAL NO 980103841-000 — SH 2 OF 9

FORM NO. 0011A

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
KEY (1): A = WITH B/M, D = WITHOUT B/M, R = REFERENCE, S = SPECIFICATION
KEY (2)
RELEASED FOR ASSEMBLY
BILL OF MATERIAL NO. 980103841-000

ITEM/ FIND NO	QUANTITY PER ASSEMBLY (000)	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
33	1	04			482000310-001	I.C. 74S133		U174
34	1	04			482000314-001	74S138		U179
35	5	04			482100784-001	74LS157		U186,187,
36								188,202,203
37	2	04			482000312-001	74S158		U199,200
38	4	04			482100835-001	74LS174		U189,190,
39								201,204
40	1	04			482101177-001	74S260		U170
41	2	04			482000342-001	74S280		U213,214
42	3	04			482102505-001	74S283		U185,196,198
43	7	04			482103947-001	74LS373		U210,211,212,
44								215,216,217,218
45	1	04			482102639-001	74LS393		U193
46	1	04			482103971-001	75452		U219
47	1	04			482104567-001	I.C. 3524		U149
48								

NOTES:

ENG CHG	REV	A	B	C	D	E
	CHG NO.	POD 3564	PCO 23636	PCO 24003	24005	PCO 24009
	DATE	—	—	—	—	—
	APPR	—	—	—	—	—

ASSY USAGE REF

WRITTEN BY: D.TAYLOR — DATE — DESIGN — DATE
CHECKED BY — DATE — APPROVED — DATE

TITLE: NS11L ¼ MEGA BYTE MEMORY

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE — BILL OF MATERIAL NO 980103841-000 — SH 3 OF 9

FORM NO. 0011A

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
KEY (1): A = WITH B/M, D = WITHOUT B/M, R = REFERENCE, S = SPECIFICATION
KEY (2)
RELEASED FOR ASSEMBLY
BILL OF MATERIAL NO. 980103841-000

ITEM/ FIND NO	QUANTITY PER ASSEMBLY (000)	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
49	4	04			482102662-001	I.C. 3648		U151, 165,
50								207,221
51	5	04			482103697-001	8641		U229-233
52	5	04			482000248-001	8837		U224-228
53	1	04			482102598-012	RAM 16K		U167
54								
55	145	04			214102685-003	I.C. SOCKET, 16 PIN		U1-144,
56								167
57	2	04			611100900-100	DELAY LINE 100 nS		U155, 157
58								
59								
60	3	04			513100986-008	SWITCH, DIP, 8 POS		S1-3
61								
62	1	04			480105601-001	TRANSIENT SUPPRESSOR	CR1	GENERAL
63								SEMICONDUCT-
64								INDUSTRIES

NOTES:

ENG CHG	REV	A	B	C	D	E
	CHG NO.	POD 3564	PCO 23636	PCO 24003	24005	PCO 24009
	DATE	—	—	—	—	—
	APPR	—	—	—	—	—

ASSY USAGE REF

WRITTEN BY: D.TAYLOR — DATE — DESIGN — DATE
CHECKED BY — DATE — APPROVED — DATE

TITLE: NS11L ¼ MEGA BYTE MEMORY

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE — BILL OF MATERIAL NO 980103841-000 — SH 4 OF 9

FORM NO. 0011A

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
KEY (1): A = WITH B/M, D = WITHOUT B/M, R = REFERENCE, S = SPECIFICATION
KEY (2)
RELEASED FOR ASSEMBLY
BILL OF MATERIAL NO. 980103841-000

ITEM/ FIND NO	QUANTITY PER ASSEMBLY (000)	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
65	3	04			481100853-001	DIODE IN5817		CR2,6,7
66	1	04			481100775-001	DIODE IN5231B		CR3
67	4	04			481101049-001	DIODE IN4531		CR4,5,8,9
68								
69								
70	1	04			394105352-001	LED (RED)		DS1
71	1	04			394105352-002	LED (YELLOW)		DS2
72								
73								
74	1	04			518102113-011	FUSE 4.0 AMP		F1
75	1	04			180105031-001	INDUCTOR 150 µH		L1
76								
77								
78	1	04			480103970-001	TRANSISTOR, FET 2N5434		Q1
79	1	04			480104767-001	TRANSISTOR, 2N4014		Q2
80	4	04			480105342-001	TRANSISTOR, 2N3506		Q3-6

NOTES:

ENG CHG	REV	A	B	C	D	E
	CHG NO.	POD 3564	PCO 23636	PCO 24003	24005	PCO 24009
	DATE	—	—	—	—	—
	APPR	—	—	—	—	—

ASSY USAGE REF

WRITTEN BY: D.TAYLOR — DATE — DESIGN — DATE
CHECKED BY — DATE — APPROVED — DATE

TITLE: NS11L ¼ MEGA BYTE MEMORY

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE — BILL OF MATERIAL NO 980103841-000 — SH 5 OF 9

FORM NO. 0011A

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
KEY (1): A = WITH B/M, D = WITHOUT B/M, R = REFERENCE, S = SPECIFICATION
KEY (2):
RELEASED FOR ASSEMBLY:
BILL OF MATERIAL NO: 980103841-000

ITEM/ FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
81	3	04			474101854-002	RES. MOD 10PIN SIP 10K		RP1-3
82								
83	18	04			470101134-019	RES.CC 15Ω, 1/8W 5%		R1-17,19
84	10	04			470101134-087	RES.CC, 10K, 1/8W 5%		R18,20,
85								49-54,56
86								57
87	3	04			470101134-051	RES.CC, 330Ω 1/8W, 5%		R21,22,23
88	1	04			470101134-103	RES,CC 47K, 1/8W, 5%		R24
89	1	04			470100611-043	RES.CC 150Ω, 1/4W,5%		R25
90	4	04			470101135-001	RES.CC, 1Ω, 1/2W, 5%		R26-29
91	1	04			470101135-038	RES.CC, 36Ω, 1/2W, 5%		R30
92	1	04			470100611-071	RES,CC, 2.2K, 1/4W, 5%		R31
93	1	04			470100611-055	RES,CC, 470, 1/4W, 5%		R32
94	1	04			470100611-087	RES,CC, 10K, 1/4W, 5%		R33
95	1	04			474102565-096	RES.FILM, 8.87K, 1/8W, 1%		R34
96	3	04			474102565-098	RES,FILM, 2.21K, 1/8W, 1%		R35-37

NOTES:

ASSY USAGE REF:

ENG. CHG	REV	A	B	C	D	E
	CHG NO.	PDD 3564	PCO 23636	PCO 24003	24005	PCO 24009
	DATE	—	—	—	—	—
	APPR	—	—	—	—	—

TITLE: NSIIL
1/4 MEGA BYTE MEMORY

WRITTEN BY: DTAYLOR DATE: DESIGN: DATE:
CHECKED BY: DATE: APPROVED: DATE:

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE: BILL OF MATERIAL NO: 980103841-000 SH 6 OF 9

FORM NO. 0011A

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
KEY (1): A = WITH B/M, D = WITHOUT B/M, R = REFERENCE, S = SPECIFICATION
KEY (2):
RELEASED FOR ASSEMBLY:
BILL OF MATERIAL NO: 980103841-000

ITEM/ FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
97	1	04			470100611-103	RES.CC, 47K, 1/4W, 5%		R38
98	1	04			470100611-135	RES.CC, 1MΩ, 1/4W, 5%		R39
99	2	04			470101134-047	RES.CC, 220Ω, 1/8W, 5%		R40,42
100	2	04			470101134-053	RES.CC, 390Ω, 1/8W, 5%		R41, 43
101	1	04			470101134-077	RES.CC, 3.9K, 1/8W, 5%		R44
102	1	04			470101134-073	RES.CC, 2.7K, 1/8W, 5%		R45
103	2	04			470101134-075	RES.CC, 3.3K, 1/8W, 5%		R46, 47
104	1	04			470101134-025	RES.CC, 27Ω, 1/8W, 5%		R48
105	1	04			474102565-120	RES.FILM 16.2K, 1/8W, 1%		R55
106								
107								
108	166	04			151104975-012	CAP.CER, .47UF, 50V, 10%		C1-126, 149,
109								152-157,
110								161-179,
111								181-187,
112								190-196

NOTES:

ASSY USAGE REF:

ENG. CHG	REV	A	B	C	D	E
	CHG NO.	PDD 3564	PCO 23636	PCO 24003	24005	PCO 24009
	DATE	—	—	—	—	—
	APPR	—	—	—	—	—

TITLE: NSIIL
1/4 MEGA BYTE MEMORY

WRITTEN BY: DTAYLOR DATE: DESIGN: DATE:
CHECKED BY: DATE: APPROVED: DATE:

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE: BILL OF MATERIAL NO: 980103841-000 SH 7 OF 9

FORM NO. 0011A

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
KEY (1): A = WITH B/M, D = WITHOUT B/M, R = REFERENCE, S = SPECIFICATION
KEY (2):
RELEASED FOR ASSEMBLY:
BILL OF MATERIAL NO: 980103841-000

ITEM/ FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
113	21	04			155105442-005	CAP.TANT. 15UF, 25V, 20%		C127-141,
114								188, 189,
115								197-200
116								
117	1	04			155104570-003	CAP.TANT. 22UF, 35V, 20%		C143
118	1	04			155100628-017	CAP.TANT. 4.7UF, 10V, 20%		C150
119	3	04			151101308-009	CAP.CER. 47 PF, 100V, 10%		C158-160
120	1	04			151101308-025	CAP.CER. 1000 PF, 100V, 10%		C148
121	1	04			151101308-033	CAP.CER. 4700PF, 100V, 10%		C147
122	1	04			151101308-029	CAP.CER. 2200 PF, 100V, 10%		C180
123	5	04			155104570-004	CAP.TANT. 33 UF, 35V, 20%		C142,
124								144-146,
125								151
126	0	04			600100155-005	WIRE, PVC 24 AWG Solid GRN		
127	0	04			600100158-005	WIRE, PVC 30 AWG Solid GRN		
128								

NOTES:

ASSY USAGE REF:

ENG. CHG	REV	A	B	C	D	E
	CHG NO.	PDD 3564	PCO 23636	PCO 24003	24005	PCO 24009
	DATE	—	—	—	—	—
	APPR	—	—	—	—	—

TITLE: NSIIL
1/4 MEGA BYTE MEMORY

WRITTEN BY: DTAYLOR DATE: DESIGN: DATE:
CHECKED BY: DATE: APPROVED: DATE:

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE: BILL OF MATERIAL NO: 980103841-000 SH 8 OF 9

FORM NO. 0011A

UNIT OF MEAS: 01 = EACH, 02 = INCH, 03 = FEET, 04 = BULK, 05 = AS REQD, 09 = OTHER
KEY (1): A = WITH B/M, D = WITHOUT B/M, R = REFERENCE, S = SPECIFICATION
KEY (2):
RELEASED FOR ASSEMBLY:
BILL OF MATERIAL NO: 980103841-000

ITEM/ FIND NO	QUANTITY PER ASSEMBLY	UNIT OF MEAS	KEY (1)	KEY (2)	PART NUMBER/ REFERENCE DOCUMENT	TITLE/DESCRIPTION	REF DESIG.	REMARKS
129								
130	0	04			160101790-001	LOCTITE		
131	4	04			790002971-001	TRANSISTOR PAD		Q3-6
132	3	04			215100496-003	TERMINAL		
133	1	04			980103847-001	STIFFENER-CAM LOCK		
134	6	04			280100064-005	SCREW, 2-56 X 5/16LG, PH		
135	6	04			282100453-008	WASHER, #2		
136	0	04			482102598-012	16 K RAM, 200 NS		(7)
137	0	04			482102989-112	8K PARTIAL RAM, RIGHT HALF, 200NS		(7)
138	0	04			482103060-112	8K PARTIAL RAM, LEFT HALF, 200NS		(7)
139								
140								
141								
142								
143								
144								

NOTES:

ASSY USAGE REF:

ENG. CHG	REV	A	B	C	D	E
	CHG NO.	PDD 3564	PCO 23636	PCO 24003	24005	PCO 24009
	DATE	—	—	—	—	—
	APPR	—	—	—	—	—

TITLE: NSIIL
1/4 MEGA BYTE MEMORY

WRITTEN BY: DTAYLOR DATE: DESIGN: DATE:
CHECKED BY: DATE: APPROVED: DATE:

National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, Calif. 95051

SIZE: BILL OF MATERIAL NO: 980103841-000 SH 9 OF 9

FORM NO. 0011A