

**TECHNICAL MANUAL**  
**Volume 1**

PBC 1000 Revision 4

**RAYTHEON 250**

**RAYTHEON COMPUTER**

(Formerly Packard Bell Computer)



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2700 SOUTH FAIRVIEW ST., SANTA ANA, CALIFORNIA 92704



July 15, 1961

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## PREFACE

The PB250 Computer Technical Manual is presented in two volumes, and is designed for the use of technical personnel engaged in computer checkout, modification, and field service. It is assumed that such technical personnel are familiar with basic computer technology.

Volume I contains a general description of the computer, together with a detailed description of PB250 Computer logic.

Volume II contains detailed descriptions of installation, operation, power supply, Flexowriter, test points, and maintenance procedures. The appendices contain logic layout, applicable schematics, Flexowriter specifications, and material lists.

The logic equations and logic summary in this manual have been revised to include the "P" change.

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## I. DESCRIPTION

### A. GENERAL

The Packard Bell PB 250 is a high-speed, completely solid-state general purpose digital computer in which both the data and the commands required for computations are stored in an internal memory. The storage medium is a group of magnetostrictive delay lines along which acoustical pulses are propagated. At one end of each of these lines a "writing" device converts electrical pulses into acoustical energy. At the other end of each delay line a "reading" device converts acoustical energy back into electrical pulses.

The PB 250 provides more than 50 commands to permit coding of a broad range of scientific and engineering problems. Double precision commands are provided for operating upon large numbers. Commands for scaling and normalizing numbers permit floating point operation. In addition, square root, and variable length multiplication and division operations are available. Other features include input-output buffering, and a large variety of external optional units such as punched card equipment, paper tape photo-readers, magnetic tape handlers, analog-to-digital and digital-to-analog converters, and magnetic core storage.

The memory of the basic PB 250 contains 10 magnetostrictive delay lines numbered octally from 00 through 11. These delay lines store both data and commands. Each long line, 01 through 11, contains 256 decimal or 400 octal locations. These locations, also called sectors, are numbered

000 through 377. Line 00 is a 16-word fast access line. Since line 00 is 1/16 the length of a long line, any unit of information contained in it is available 16 times during each complete circulation of the 256-word long lines. Fifty-three additional delay lines may be added, each of which may have a total of from 1 to 256 words. These additional lines are numbered from 10 through 36, and 40 through 77. If all of the additional lines are used, and if all lines hold 256 words, the memory capacity of the PB 250 is extended to 15,888 words.

Since the PB 250 memory stores either data or commands, the generic term "word" is used to cover both types of information. Every word stored in the internal memory is in binary form (negative numbers are stored in complementary form). Words stored in the PB 250 memory are represented by a series of pulses which correspond to the digits of a binary number.

Three arithmetic registers, A, B, and C, are provided for arithmetic operations and information manipulation. Each register has the same format as a memory location. Information may be interchanged between the three registers. The contents of a register may be tested for nonpositive values, or compared against the contents of any memory location. A record may be kept in one register of operations performed in the other registers.

## B. LEADING PARTICULARS

Two models of the PB 250 Computer are available : the rack-mounted PB 250 R, and the table-mounted PB 250 T. Both models are identical except for height requirements. Modular construction is used throughout the computer for ease of accessibility and maintenance. All electrical connections are made to a row of connectors at the back of the computer. Additional leading particulars are shown in Table 1-1.

Table 1-1.

LEADING PARTICULARS

Type	Serial, binary, internal program
Command structure	Single address with index register
Number of commands	59
Operation times:	
Add/subtract	12 $\mu$ sec
Multiply	276 $\mu$ sec (max. )
Divide	252 $\mu$ sec (max. )
Square root	252 $\mu$ sec (max. )
Average access time	1536 $\mu$ sec
Average access time to fast memory	96 $\mu$ sec
Maximum operational rate	40,000 instructions per second
Memory capacity	2320 words (Up to 15,888 words internal storage available)
Dimensions:	
PB 250 R (rack-mounted)	78 in. high, 19 in. wide, 24 in. deep
PB 250 T (table-mounted)	63 in. high, 19 in. wide, 24 in. deep
Power requirements	115 v, 60 cps, single phase, 110 watts
Weight	110 pounds (approx. )

## C. STANDARD EQUIPMENT

### 1-1. CONTROL UNIT

A Model FX-1 Flexowriter is supplied as standard equipment, and is used as the control unit for the PB 250 Computer. The Flexowriter is also used to prepare, duplicate, and read paper tapes. The Flexowriter can be used on-line (under control of the computer), or off-line (under control of the operator). The general appearance and operation of the Flexowriter are similar to a standard electric typewriter.

### 1-2. BASIC MODULES

The majority of the logic used in the PB 250 is constructed from four types of plug-in transistorized modules, three of which are diode modules, while the fourth is a high-frequency flip-flop module. Logic for the PB 250 uses low-leakage, high-frequency diodes to permit two-level gating. All logic is of the "true-negative" (PNP) type, in which a -12 v level represents a "true" condition, and a 0 v level represents a "false" condition.

In addition to the logic circuits, plug-in transistorized modular construction is used for the magnetostrictive registers, and the various amplifiers, emitter followers, clock drivers, etc., required for computer operation.

Description and schematics of the basic modules are contained in PB 250 Technical Manual, Volume 2.

## II. PB 250 LOGIC

### A. GENERAL

This section contains a description of the functional logic of the PB 250. The logic is defined by Appendix A, Description of Notation; Appendix B, Glossary of Terms; Appendix C, Complete Logical Equations; and Appendix F, Logic Summary.

The logic equations are presented term-by-term, together with block diagrams which illustrate the application of gating terms.

### B. COMMAND LIST

The list of commands for the PB 250 is given in Table 2-1. These commands are numbered octally from 00 to 77.

The six binary digits (bits) of the command number are stored in pulse positions 9 through 14 of the command. These bits are stored in the operation code register flip-flops and may be defined octally (see Figure 2-1).

Example:

State	O6	$\overline{O5}$	$\overline{O4}$	O3	O2	$\overline{O1}$	
reads	1	0	0	1	1	0	in binary
or	4			6			in octal

Combinations of signals from the operation code register flip-flops are used to

Table 2 - 1. (Sheet 1 of 3)

COMMAND CLASSIFICATIONS

Class 1: Executed Between Command Location and Address Sector Number.

NORMALIZE AND DECREMENT	NAD	(20)*
NORMALIZE	NOR	(20)*
LEFT SHIFT AND DECREMENT	LSD	(21)*
AB LEFT	SLT	(21)*
RIGHT SHIFT AND INCREMENT	RSI	(22)*
AB RIGHT	SRT	(22)*
SCALE RIGHT AND INCREMENT	SAI	(23)
NO OPERATION	NOP	(24)
INTERCHANGE A AND M	IAM	(25)
MOVE LINE X TO LINE 7	MLX	(26)
SQUARE ROOT	SQR	(30)
DIVIDE	DIV	(31)*
DIVIDE REMAINDER	DVR	(31)*
MULTIPLY	MUP	(32)
SHIFT B RIGHT	SBR	(33)*
LOGICAL RIGHT SHIFT	LRS	(33)*
WRITE OUTPUT CHARACTER	WOC	(6X)
PULSE TO SPECIFIED UNIT	PTU	(70)
MOVE COMMAND LINE BLOCK	MCL	(71)
BLOCK SERIAL OUTPUT	BSO	(72)
BLOCK SERIAL INPUT	BSI	(73)

\*Asterisk indicates that the op code has at least two meanings, depending on the address used with the command.

Table 2-1. (Sheet 2 of 3)

Class 2: Executed in Address Sector Number		
INTERCHANGE A AND C	IAC	(01)
INTERCHANGE B AND C	IBC	(02)
LOAD A	LDA	(05)
LOAD B	LDB	(06)
LOAD C	LDC	(04)
STORE A	STA	(11)
STORE B	STB	(12)
STORE C	STC	(10)
ADD	ADD	(14)
SUBTRACT	SUB	(15)
EXTEND BIT PATTERN	EBP	(40)
GRAY TO BINARY	GTB	(41)
AND M & C	AMC	(42)
CLEAR A	CLA	(45)
CLEAR B	CLB	(43)
CLEAR C	CLC	(44)
AND OR COMBINED	AOC	(46)
EXTRACT FIELD	EXF	(47)
DISCONNECT INPUT UNIT	DIU	(50)
READ TYPEWRITER KEYBOARD	RTK	(51)
READ PAPER TAPE	RPT	(52)
READ FAST UNIT	RFU	(53)
LOAD A FROM INPUT BUFFER	LAI	(55)
COMPARE A AND M	CAM	(56)
CLEAR INPUT BUFFER	CIB	(57)
HALT	HLT	(00)*
MERGE A INTO C	MAC	(00)*

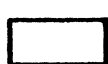
\*Asterisk indicates that the op code has at least two meanings, depending on the address used with the command.



Table 2-1. (Sheet 3 of 3)

Class 3: Executed In Address Sector Number And Following Sector.		
ROTATE	ROT	(03)
LOAD DOUBLE PRECISION	LDP	(07)
STORE DOUBLE PRECISION	STD	(13)
DOUBLE PRECISION ADD	DPA	(16)
DOUBLE PRECISION SUBTRACT	DPS	(17)
Class 4: Executed Between Command Location And Address Sector Number		
TRANSFER UNCONDITIONALLY	TRU	(37)
TRANSFER IF A NEGATIVE	TAN	(35)
TRANSFER IF B NEGATIVE	TBN	(36)
TRANSFER IF C NEGATIVE	TCN	(34)
TRANSFER ON OVERFLOW	TOF	(75)
TRANSFER ON EXTERNAL SIGNAL	TES	(77)

Op Code	Op Code Register Flip-Flops						Op Code	Op Code Register Flip-Flops					
	O6	O5	O4	O3	O2	O1		O6	O5	O4	O3	O2	O1
	Flip-Flop Binary Weights							Flip-Flop Binary Weights					
	40	20	10	4	2	1		40	20	10	4	2	1
00							40						
01							41						
02							42						
03							43						
04							44						
05							45						
06							46						
07							47						
10							50						
11							51						
12							52						
13							53						
14							54						
15							55						
16							56						
17							57						
20							60						
21							61						
22							62						
23							63						
24							64						
25							65						
26							66						
27							67						
30							70						
31							71						
32							72						
33							73						
34							74						
35							75						
36							76						
37							77						
	2nd Octal Digit			1st Octal Digit				2nd Octal Digit			1st Octal Digit		

 Indicates that the flip-flop is in its reset or "false" condition.


 Indicates that the flip-flop is in its set or "true" condition.

Figure 2-1. Command Codes In Operation Code Register

condition many of the logic gates.

## C. TIMING

### 2-1. PULSE COUNTER

Basic pulse timing is provided by a binary five stage counter that serves as the pulse counter ( see Figure 2-2 ). This counter consists of five flip-flops whose states define the pulse counts as shown in Figure 2-3. The pulse counter is similar to a regular 32-pulse counter, except that F 5 is reset at the end of P 23 and F 4 is set only at the end of P 7.

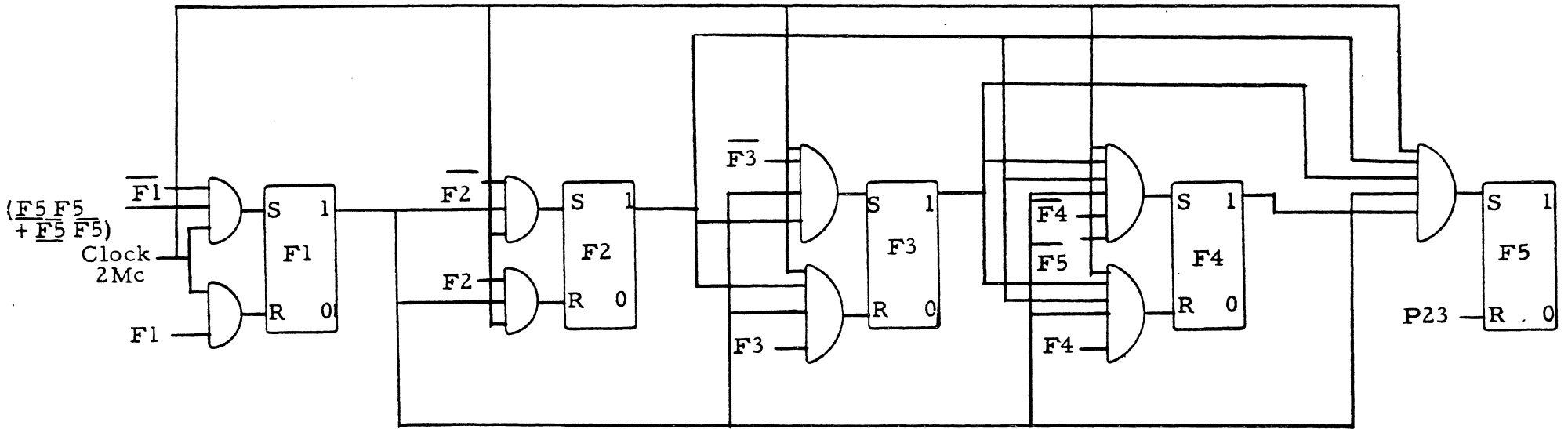
### 2-2. SECTOR COUNTER

For sector number information, a one-word (24-pulse) register is provided as a sector counter (see Figure 2-4). Serial sector numbers are obtained in the pulse intervals (P 8-P 15) and (P16-P23) by setting carry flip-flop, Sc, at P 7 and P 15 (see Figure 2-5).

$$\begin{aligned} sSc &= \overline{F5} F3 F2 F1 \\ rSc &= P23 + \overline{Sr} (\overline{F3} + \overline{F2} + \overline{F1}) \\ sSw &= Sc \overline{Sr} \overline{Qg} + \overline{Sc} Sr \overline{Qg} + \dots \\ rSw &= Sc Sr + \overline{Sc} \overline{Sr} ( ) + Qg ( ) \\ sSr &= (Sw \text{ delayed by } 22 \text{ pulse times}) \\ rSr &= (\overline{Sw} \text{ delayed by } 22 \text{ pulse times}) \end{aligned}$$

The sector counter clear term, Qg, is described in paragraph 2-3. The use of the interval (P24 - P7) as an input buffer is described in paragraph 2-9. This interval is protected by resetting the sector counter carry flip-flop, Sc, at P 23.

The sector counter numbers in (P8 - P15) and (P16-P23) advance from



2-7

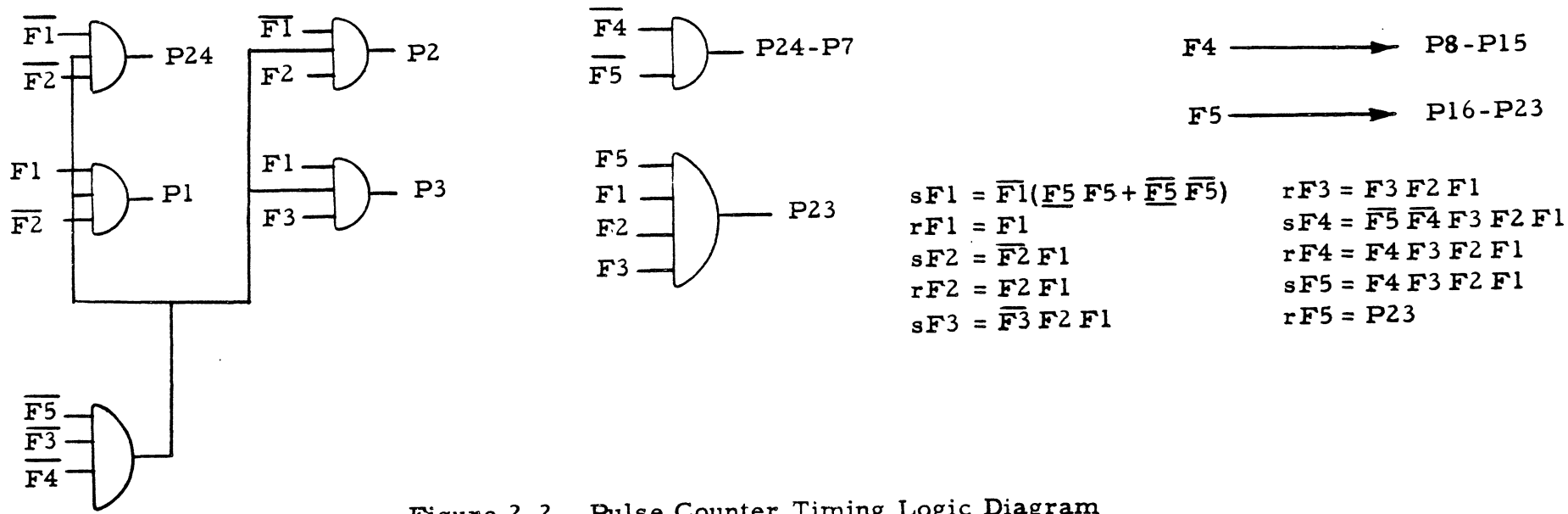
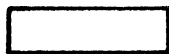


Figure 2-2. Pulse Counter Timing Logic Diagram

Maintenance Timing	F5	F4	F3	F2	F1	Programming Timing
P1					■	*
P2				■		T1
P3				■	■	T2
P4			■			T3
P5			■		■	T4
P6			■	■		T5
P7			■	■	■	T6
P8		■				T7
P9		■			■	T8
P10		■		■		T9
P11		■		■	■	T10
P12		■	■			T11
P13		■	■		■	T12
P14		■	■	■		T13
P15		■	■	■	■	T14
P16	■					T15
P17	■				■	T16
P18	■			■		T17
P19	■			■	■	T18
P20	■		■			T19
P21	■		■		■	T20
P22	■		■	■		T21
P23 <small>sign</small>	■		■	■	■	T22
P24						*



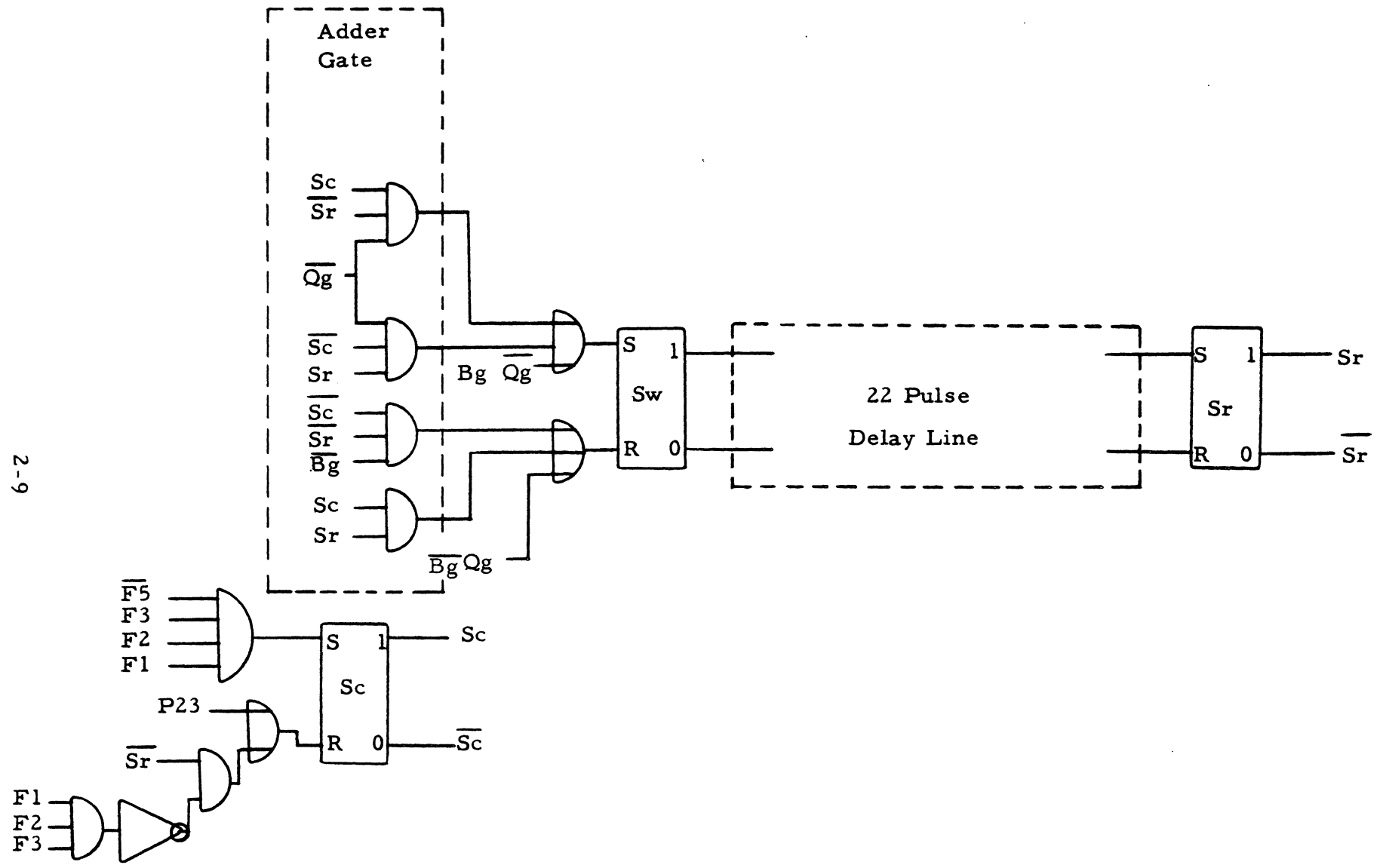
Indicates that the flip-flop is in its reset or "false" condition.



Indicates that the flip-flop is in its set or "true" condition.

\*P1 and P24 are not accessible to the programmer and are not numbered.

Figure 2-3. Pulse Counts



$$\overline{F5} \overline{F3} \overline{F2} \overline{F1} = (P7 + P15)$$

Figure 2-4. Sector Counter Timing Logic Diagram

000 to 255 for each machine cycle. These numbers are used in comparison with the one-word instruction register to define the numbers of the sectors which follow. An example of the numbers presented by the sector counter in memory is shown in Figure 2-6.

### 2-3. MULTIPLE COMPUTER OPERATION

To synchronize the pulse counters of two computers, the F5 signal from the master computer enters the slave computer and is designated F5. With the clock generators operating from a single crystal oscillator, the first stage of the slave computer's pulse counter is controlled by F5.

$$sF1 = \overline{F1} (\underline{F5} F5 + \overline{F5} \overline{F5}).$$

This prevents counting in the slave computer when the most significant stages of the two pulse counters are different, which synchronizes the counters.

To synchronize the sector counter of the slave computer, the master computer executes a command 70 having a line number  $37_g$  during sector 255 ( $377_g$ ). This command is detected in the Qg gate of the slave computer and serves to zero the sector counter.

$$Qg = - - - + \underline{Cpg} \underline{M3g} \underline{N7g} + - - -$$

### D. OPERATION PHASES

The operation phases are controlled with the Ec and Rc flip-flops, based on the successive commands read into the instruction register and into the operation code register flip-flops. The basic timing of the operation phases is provided by comparing sector numbers in the instruction register with the sector counter using the comparison flip-flop, Is.

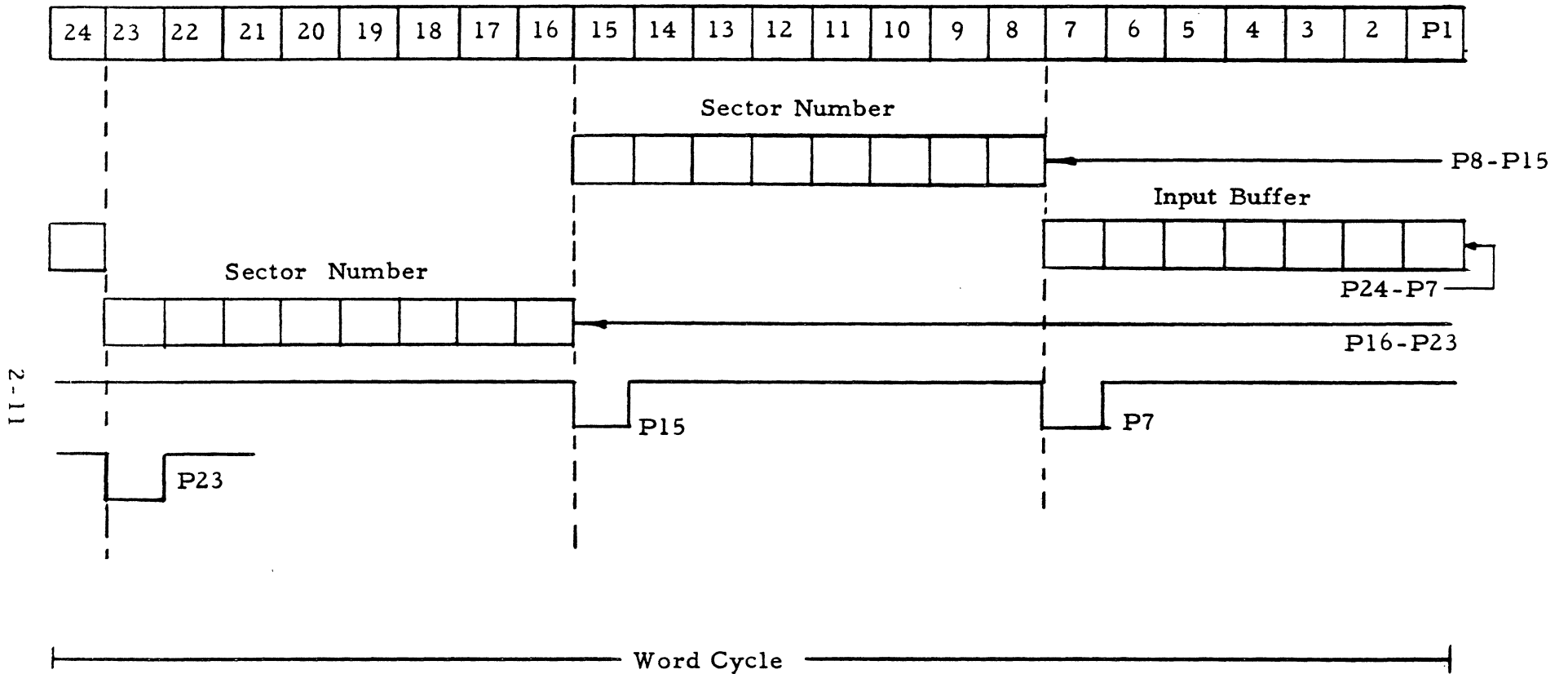
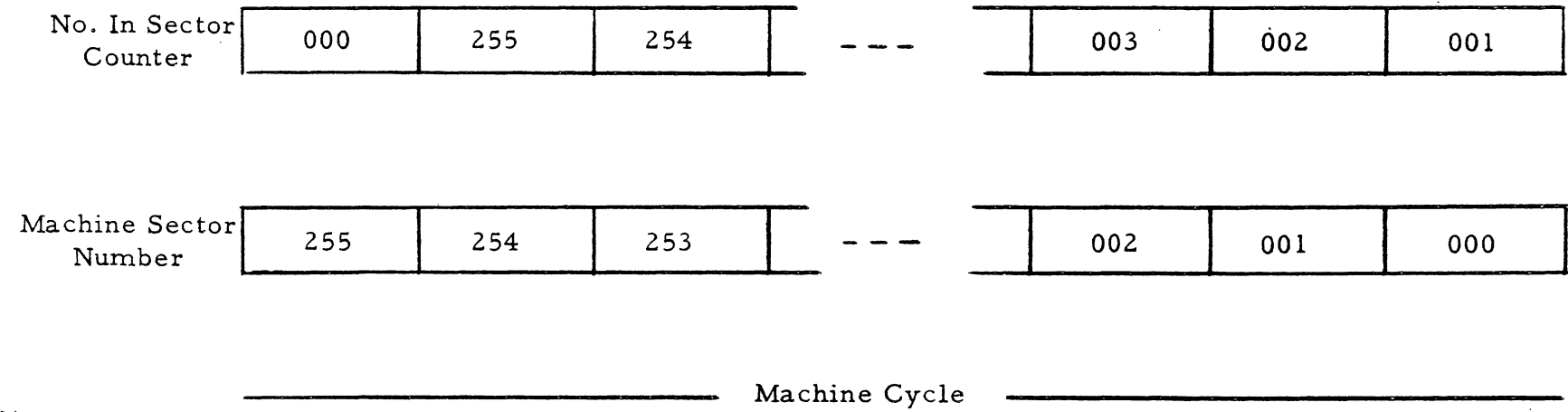


Figure 2-5. Pulse Time Format Timing Diagram





2-12

Figure 2-6. Sector Format Timing Diagram

The four operation phases are:

Phase 1	$\overline{E_c} \overline{R_c}$	Wait to read next command
Phase 2	$\overline{E_c} R_c$	Read command
Phase 3	$E_c R_c$	Wait to execute command
Phase 4	$E_c \overline{R_c}$	Execute command

Depending on the timing, phases 1 or 3 may be skipped if there is no requirement to wait for a command or an execution. When the computer is stopped, it idles in phase 1. The operation code register flip-flops exert some control over the operation phases. For commands 20 through 37, and 60 through 77 (characterized by the O5 flip-flop being "true"), the computer automatically skips from phase 2 to phase 4, and phase 4 is terminated by the address sector number. For all other commands, phase 4 terminates automatically after one or two sectors. In any command, when the operation code flip-flop, Oc, is set, the computer will skip phase 1 at the end of phase 4. In the case of branch commands, 34, 35, 36, 37, 75 and 77, the Oc flip-flop is used to detect the branch control condition. If Oc is set, the computer goes to phase 4. If Oc is reset, the computer skips from phase 2 to phase 4 for one pulse time (P1) and then returns to phase 2 so that the next command in sequence will be read. Indication of the phase changes is presented in Figure 2-7.

#### 2-4. PHASE 1: WAIT TO READ COMMAND

During each sector of phase 1, the Is flip-flop compares the next command sector number in the instruction register with the sector counter to determine when to read the next command.

$$\begin{aligned}
 sIs &= P24 \\
 rIs &= (\overline{S_r} sIw + S_r rIw) \left[ \overline{E_c} \overline{R_c} (P8-P15) + \dots \right]
 \end{aligned}$$

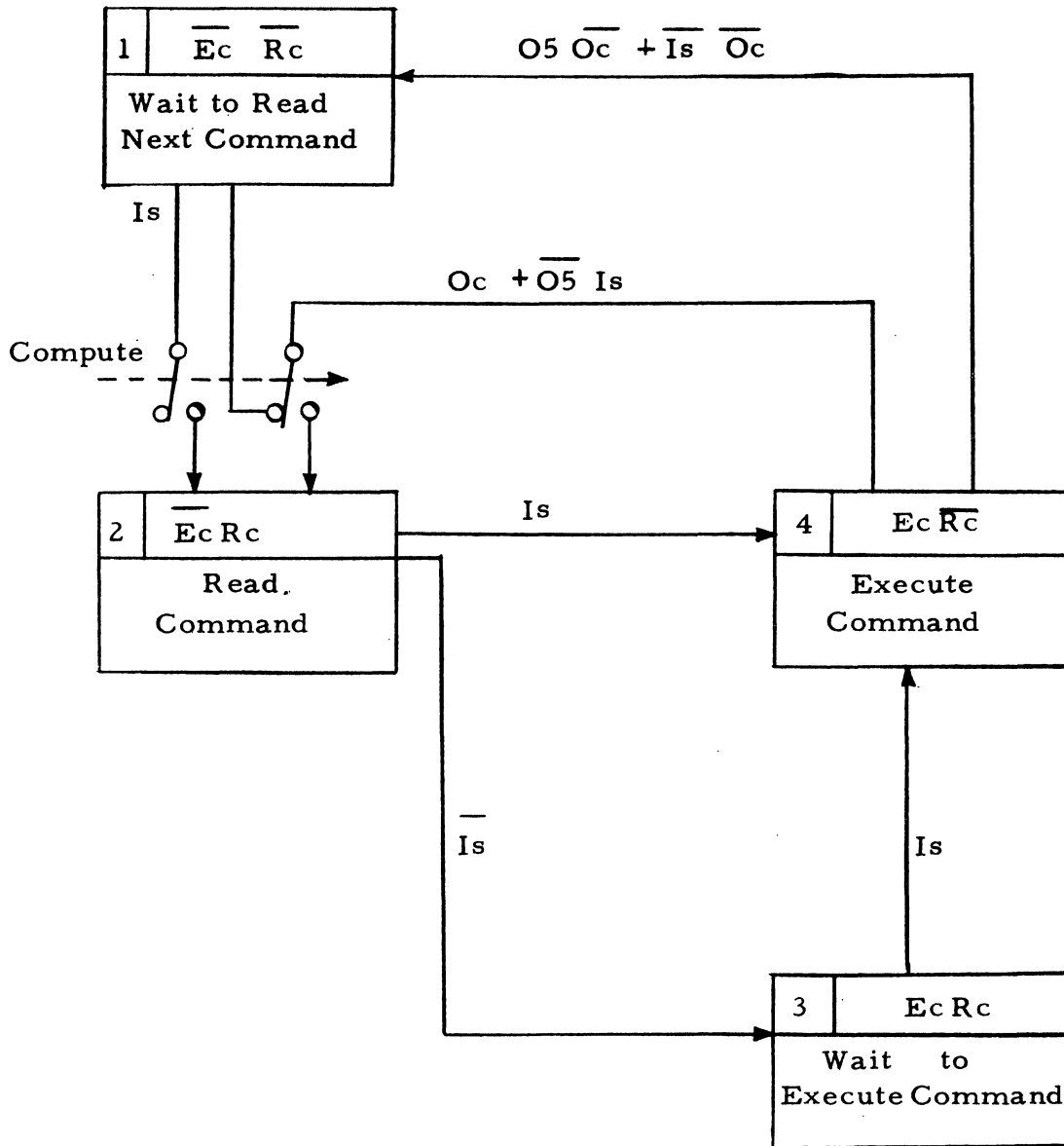


Figure 2-7. Simplified Phase Chart

## 2-5. PHASE 2: READ COMMAND

When the command sector number agrees with the sector counter, the  $I_s$  flip-flop will still be set at the end of the sector, and phase 2 will be initiated ( $R_c$  set).

$$sR_c = P24 \overline{E_c} \overline{R_c} I_s \left( \overline{E_n} + \dots \right) \overline{F_i} + \dots$$

Phase 2 is conditioned by depressing the ENABLE switch, which qualifies all  $sR_c$  terms as a computation interrupt ( $\overline{E_n}$ ). Raising the FILL switch also interrupts computation (see Figure 2-8).

During the single sector of phase 2 the bits of the next command to be executed are read into the proper storage locations. The bit in bit position 2 of each command is temporarily stored in operation code register flip-flop, O2.

$$\begin{aligned} sO2 &= \overline{E_c} R_c P2 V_g + \dots \\ rO2 &= \overline{E_c} R_c P2 \overline{V_g} + \dots \end{aligned}$$

This bit is then used to select the operand line number from either the index portion of the instruction register if the O2 flip-flop is set, or from the line number portion of the command itself if the O2 flip-flop is reset, during bit positions 4 through 8 (see Figure 2-9).

$$\begin{aligned} sL5 &= L_g \overline{O2} V_g + L_g O2 I_w + \dots \\ rL5 &= L_g \overline{O2} \overline{V_g} + L_g O2 \overline{I_w} \\ \\ sL4 &= L_g L5 + \dots \\ rL4 &= L_g \overline{L5} + \dots \\ \\ sL3 &= L_g L4 + \dots \\ rL3 &= L_g \overline{L4} + \dots \\ \\ sL2 &= L_g L3 + \dots \\ rL2 &= L_g \overline{L3} + \dots \end{aligned}$$

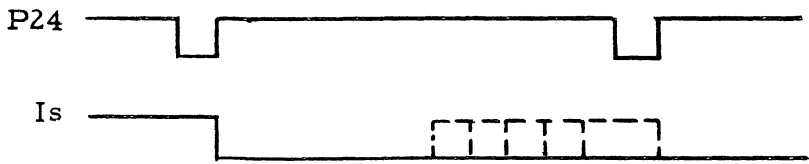
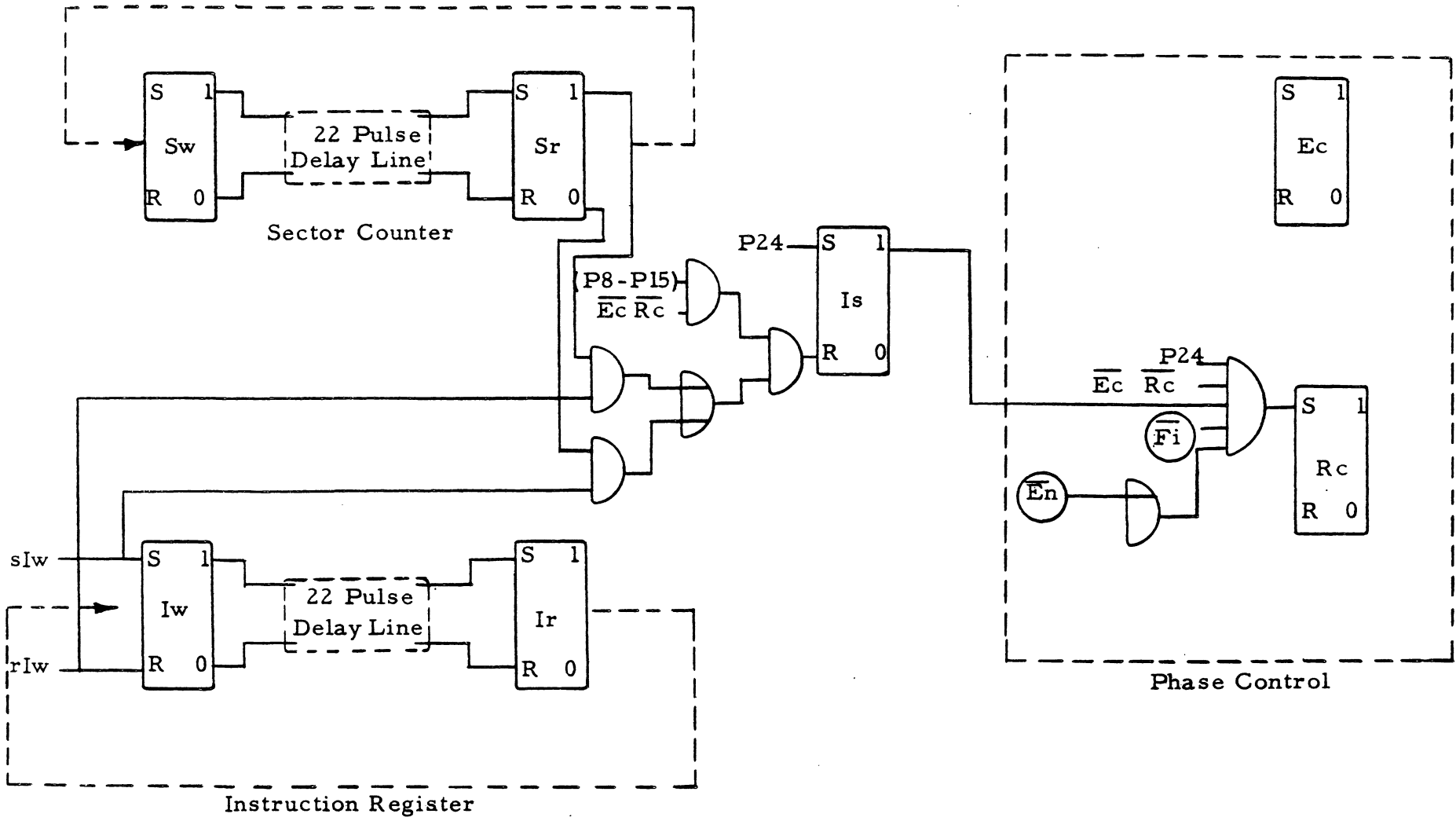


Figure 2-8. Phase Control (Ph 1 to Ph 2) Logic Diagram

$$\begin{aligned}
sL1 &= Lg L2 + - - - \\
rL1 &= Lg \overline{L2} + - - - \\
Lg &= \overline{Ec} R_c \overline{F5} (\overline{F4} + \overline{F3} \overline{F2} \overline{F1}) \overline{P24}
\end{aligned}$$

The bits in bit positions 9 through 15 are shifted into the operation code register flip-flops.

$$\begin{aligned}
sOc &= Og Vg + - - - & sO3 &= Og O4 + - - - \\
rOg &= Og \overline{Vg} + - - - & rO3 &= Og \overline{O4} \\
sO6 &= Og Oc + - - - & sO2 &= Og O3 + - - - \\
rO6 &= Og \overline{Oc} + - - - & rO2 &= Og \overline{O3} + - - - \\
sO5 &= Og O6 + - - - & sO1 &= Og O2 + - - - \\
rO5 &= Og \overline{O6} + - - - & rO1 &= Og \overline{O2} + - - - \\
sO4 &= Og O5 + - - - & Og &= \overline{Ec} R_c F4 \\
rO4 &= Og \overline{O5} + - - -
\end{aligned}$$

During the shift into the operation code register flip-flops, the next command sector number is advanced by writing the new number in the sector counter into the instruction register (see Figure 2-10).

$$sIw = \overline{Ec} R_c (P8-P15) S_r + - - -$$

The address sector number of the command is written into the instruction register following the next command location sector number.

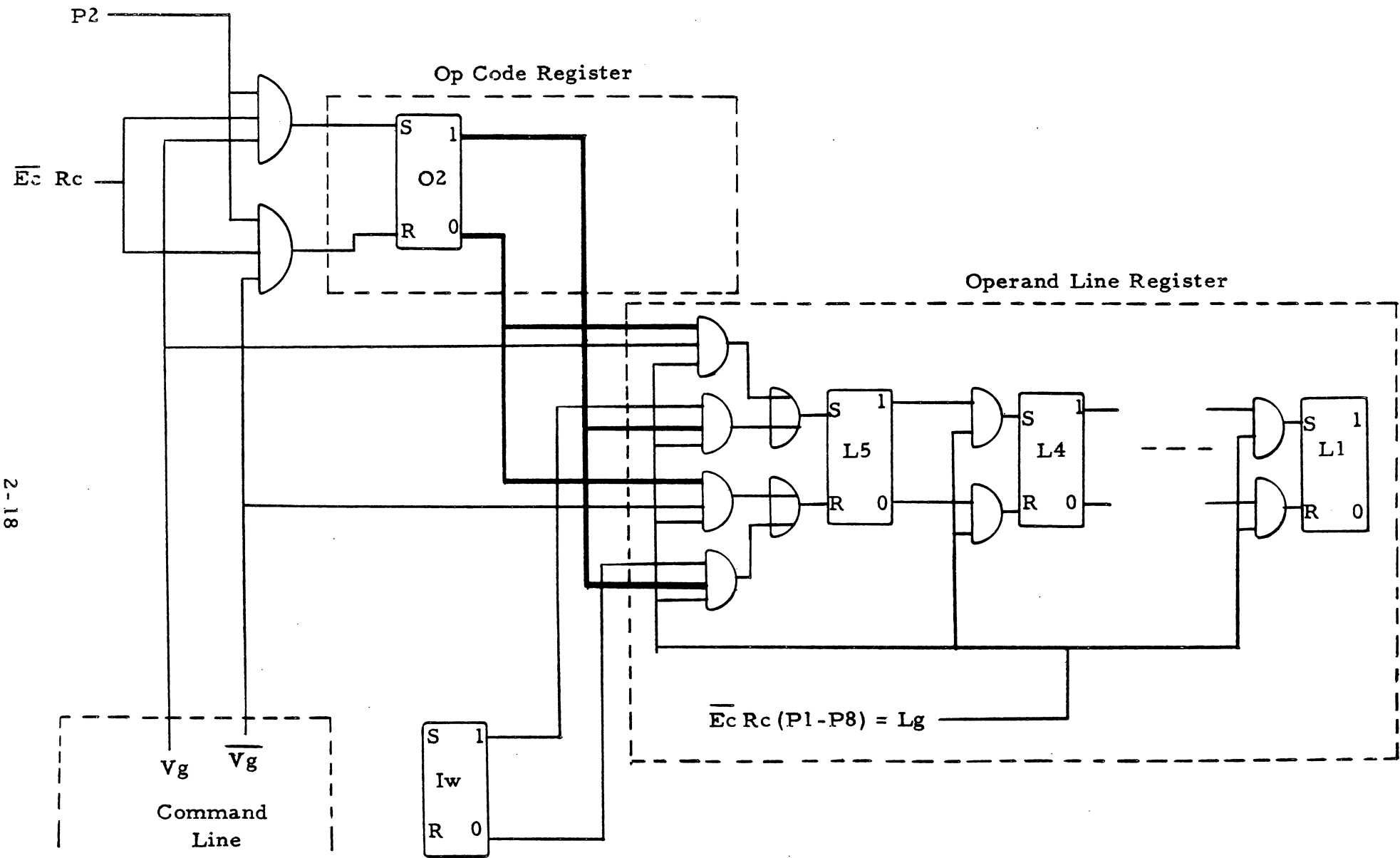
$$sIw = + \overline{Ec} R_c (P16 - P23) Vg + - - -$$

This address sector number of the command is also compared with the sector counter to determine if phase 4 should follow phase 2.

$$rIs = (\overline{Sr} sIw + S_r rIw) \left[ - - - + \overline{O5} R_c (P16-P23) + - - - \right]$$

Phase 2 is always changed to phase 3 or 4 after one sector.

$$sEc = P24 \overline{Ec} R_c$$



2-18

Figure 2-9. Operand Line Selection Logic Diagram





At the end of the read command sector, the flip-flop  $I_s$  will be set and phase 4 will follow phase 2 directly if the command includes  $O_5$  ( $O_5$  in its "true" condition), or if the address sector number agreed with the sector counter in phase 2.

$$rRc = P_{24} R_c I_s + \dots$$

#### 2-6. PHASE 3: WAIT TO EXECUTE COMMAND

If phase 3 is allowed to occur, the address sector number continues to be compared with the sector counter until these two numbers agree, causing phase 4 to be set.

#### 2-7. PHASE 4: EXECUTE COMMAND

During phase 4 the command is executed. The end of the execute phase for commands 00, 01, 02, 04, 05, 06, 10, 11, 12, 14, 15, and 40 through 57, occurs after one sector (see Sheet 1, Figure 2-11).

$$\begin{aligned} E_g &= P_{24} E_c \overline{R_c} (\overline{O_5} \overline{O_2} + \overline{O_5} O_6 + \overline{O_5} \overline{O_3} \overline{O_1} + \overline{O_5} \overline{O_4} \overline{O_1} + \dots) \\ rE_c &= E_g + \dots \end{aligned}$$

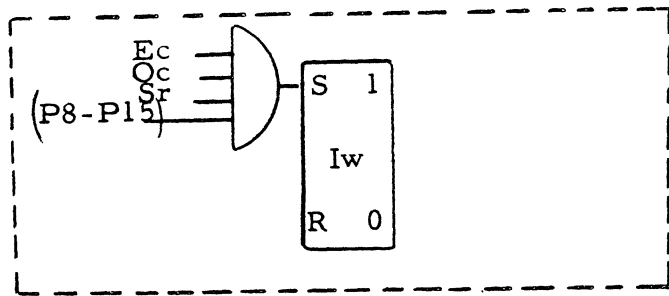
Commands 03, 07, 13, 16, and 17 are effectively changed to commands 01, 05, 11, 14, and 15, respectively, after one sector of execution and, after two sectors, execution is terminated by the  $P_{24} E_c \overline{R_c} \overline{O_5} \overline{O_2}$  term of  $E_g$ .

$$rO_2 = \dots + P_{24} E_c \overline{R_c} \overline{O_6} \overline{O_5} O_1 + P_{24} E_c \overline{R_c} \overline{O_6} \overline{O_5} O_4 O_3$$

For commands 20 through 37, and 60 through 77, phase 4 is terminated by matching the address sector number and the sector number and the sector counter (see Sheet 1, Figure 2-11).

$$\begin{aligned} rI_s &= (\overline{S_r} s_{lw} + S_r r_{lw}) \left[ \dots + E_c O_5 (P_{16} - P_{23}) + \dots \right] \\ E_g &= P_{24} E_c \overline{R_c} \dots + O_5 I_s \end{aligned}$$

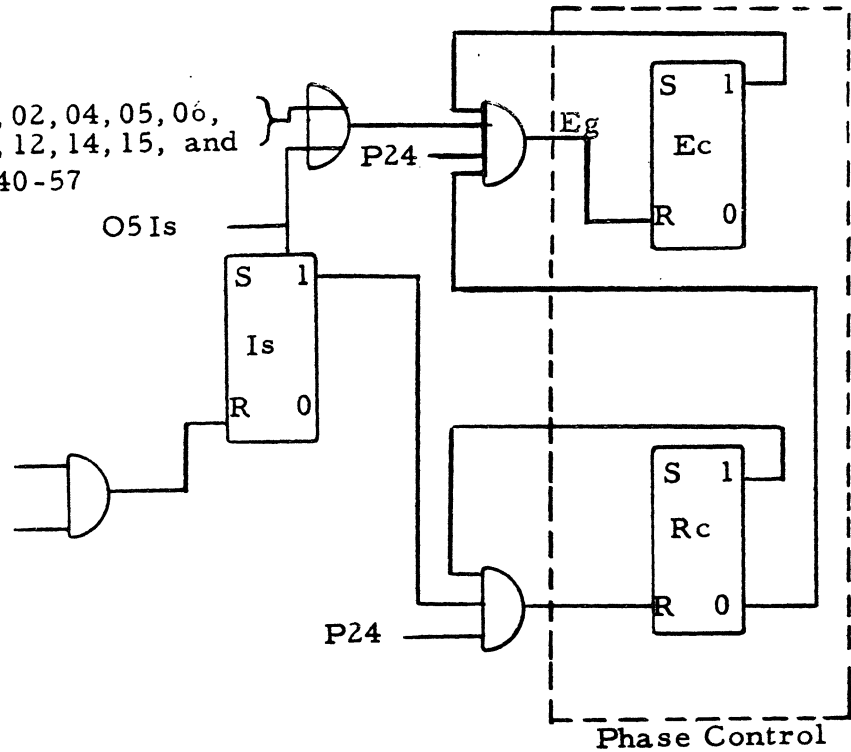
If the  $O_c$  flip-flop is set during phase 4, the next command number in the



Instruction Register

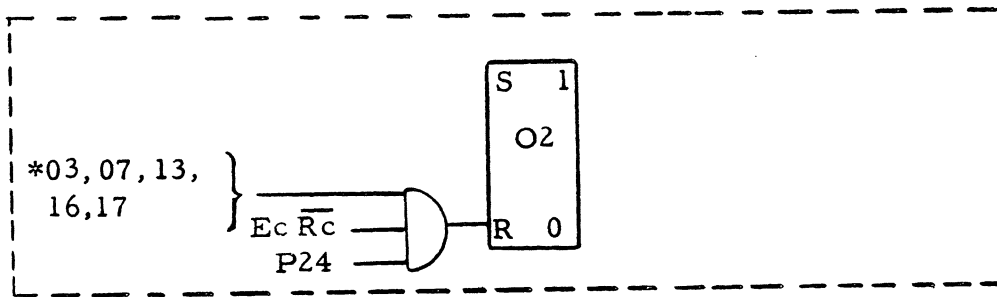
\*00, 01, 02, 04, 05, 06,  
10, 11, 12, 14, 15, and  
40-57

$(\overline{S}r sIw + Sr rIw)$   
Ec 05 (P16-P23)



Phase Control

2-21



Op Code Register

\*Commands

Figure 2-11. Phase 4 Termination Logic Diagram (Sheet 1 of 2)

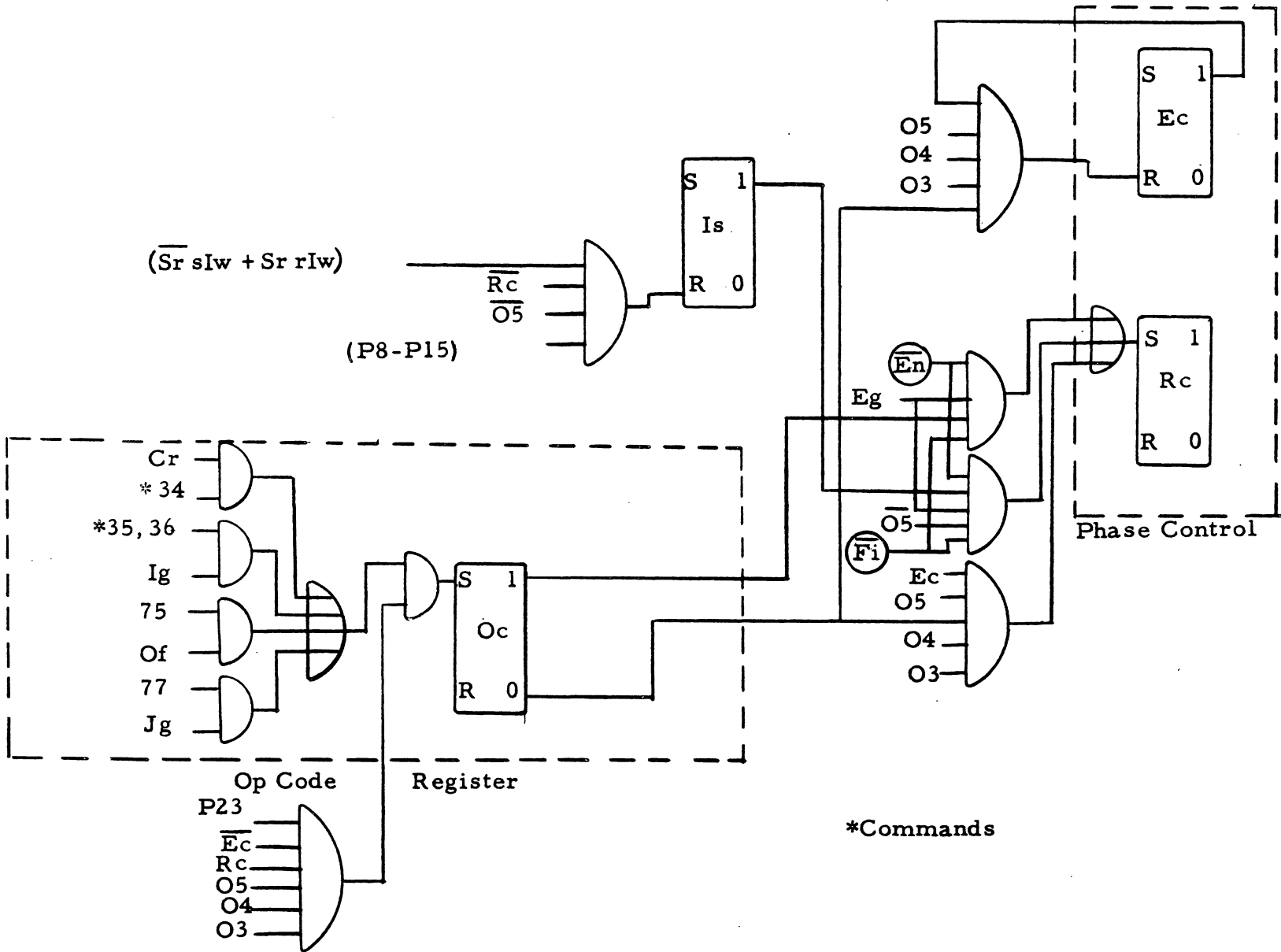


Figure 2-11. Phase 4 Termination Logic Diagram (Sheet 2 of 2)

instruction register is advanced by writing the number in the sector counter into the instruction register.

$$sIw = \dots + Ec Oc (P8-P15) Sr + \dots$$

This next command number is used only if computation is interrupted and then restarted, since Oc in its "true" condition normally causes phase 2 at the end of phase 4 (see paragraph D).

$$sRc = \overline{En} \overline{Fi} Eg Oc + \dots$$

During phase 4 of commands 00 through 17, and 40 through 57, the next command sector number is compared with the sector counter to determine whether phase 2 should be entered when phase 4 is terminated (see Sheet 2, Figure 2-11).

$$\begin{aligned} rIs &= (\overline{Sr} sIw + Sr rIw) [- \dots + \overline{Rc} \overline{O5} (P8-P15)] \\ sRc &= \dots \overline{En} \overline{Fi} Eg \overline{O5} Is + \dots \\ rRc &= P24 Rc Is + \dots \end{aligned}$$

Commands 34, 35, 36, 37, 75, and 77 operate somewhat differently. At the end of reading one of these commands, Oc will be set if the branch condition being tested is set (see Sheet 2, Figure 2-11).

$$\begin{aligned} sOc &= \dots + P23 \overline{Ec} Rc O5 O4 O3 (\overline{O6} Ig + O6 \overline{O2} O1 Of \\ &\quad + O6 O2 O1 Jg + \overline{O2} \overline{O1} Cr) \end{aligned}$$

These terms include Ig for the signs of the A and B registers; Cr for the sign of the C register; Of for overflow; and Jg for a selected branch control input line (see paragraph K for the construction of Jg). Phase 4 will immediately follow phase 2 because of the P24 Rc Is term of rRc but, if Oc is not set, phase 4 will immediately be changed to phase 2.

$$\begin{aligned} rEc &= \dots + Ec O5 O4 O3 \overline{Oc} + \dots \\ sRc &= \dots + Ec O5 O4 O3 \overline{Oc} \end{aligned}$$

If Oc was set, phase 4 will extend until the address sector number agrees with the sector counter, and phase 2 will follow phase 4. When commands 34, 35, 36, 37, and 75 enter phase 4 due to Oc being set, the command line selector flip-flops are changed by the contents of the operand line selector flip-flops.

$$\begin{aligned}
 sK4 &= Kg L4 & sK2 &= Kg L2 \\
 rK4 &= Kg \overline{L4} + \dots & rK2 &= Kg \overline{L2} + \dots \\
 sK3 &= Kg L3 & sK1 &= Kg L1 + \dots \\
 rK3 &= Kg \overline{L3} + \dots & rK1 &= Kg \overline{L1} \\
 Kg &= Ec O5 O4 O3 F4 (\overline{O6} + \overline{O2})
 \end{aligned}$$

## 2-8. MANUAL CONTROLS

A minimum of manual control is included. Depressing the ENABLE switch holds the computer in phase 1 by blocking the sRc terms. If the  $\gamma$  key is depressed while the ENABLE switch is closed, the command line selector register is set to line 01 and the next command sector is reset to zero (see Figure 2-12).

$$\begin{aligned}
 rKs &= \dots + \textcircled{En} \textcircled{T6} \textcircled{T5} \textcircled{T4} \textcircled{T1} (P23) \\
 rK3 &= \dots + \textcircled{En} \textcircled{T6} \textcircled{T5} \textcircled{T4} \textcircled{T1} (P23) \\
 rK2 &= \dots + \textcircled{En} \textcircled{T6} \textcircled{T5} \textcircled{T4} \textcircled{T1} (P23) \\
 sK1 &= \dots + \textcircled{En} \textcircled{T6} \textcircled{T5} \textcircled{T4} \textcircled{T1} (P23) \\
 sIw &= \dots + Ir \left[ \dots + \textcircled{En} \textcircled{T6} \textcircled{T5} \textcircled{T4} \textcircled{T1} (P8-P15) \right] \\
 &\quad \underbrace{\quad \quad \quad}_{+ \dots}
 \end{aligned}$$

If the "C" key is depressed while the ENABLE switch is closed, the computer will read and execute one command. The Oc flip-flop provides the enabling conditions for this one cycle operation.

$$\begin{aligned}
 sOc &= \dots + \textcircled{En} P24 Is \overline{Ec} \overline{Rc} \textcircled{T6} \textcircled{T5} \textcircled{T2} \textcircled{T1} + \dots \\
 rOc &= \dots + Eg \\
 sRc &= \dots + P24 \overline{Ec} \overline{Rc} Is \left( \textcircled{En} + Oc \overline{\textcircled{T6} \textcircled{T5} \textcircled{T2} \textcircled{T1}} \textcircled{F1} \right) \\
 &\quad + \dots
 \end{aligned}$$

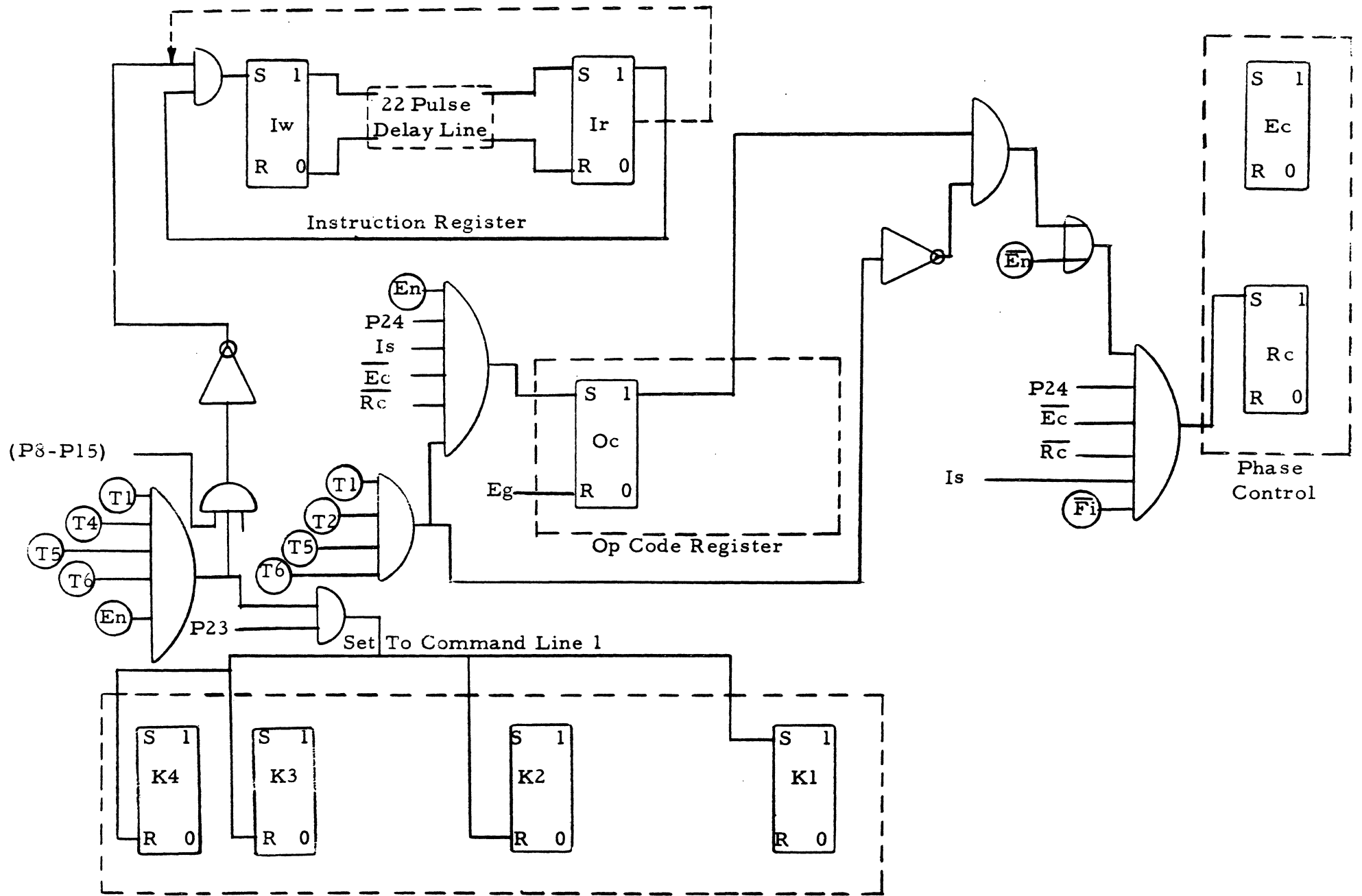


Figure 2-12. "I" and "C" Key Control Logic Diagram

The storage of a line number in the index register is achieved by sending it to line (37)<sub>g</sub>. The useful portion of this number (bit positions 3 through 7) is entered into the instruction register.

$$sIw = \dots + \overline{P24}(P24-P7) M3g N7g Wg Ig + \dots$$

When transferred to the operand line selector register, the number in the instruction register (bit positions 4 through 8) is taken from the instruction register write flip-flop, Iw, rather than from the instruction register read flip-flop, Ir.

Phase 2 or phase 4 can be immediately changed to phase 1 if a parity error is indicated by the Pc flip-flop (see Figure 2-13).

$$rEc = \dots + Ec \overline{Rc} Pc Pi$$

$$rRc = \dots + \overline{Ec} Rc Pc Pi$$

A parity error will halt computation until the Pc flip-flop is cleared by depressing the ENABLE switch and the BREAK POINT switch.

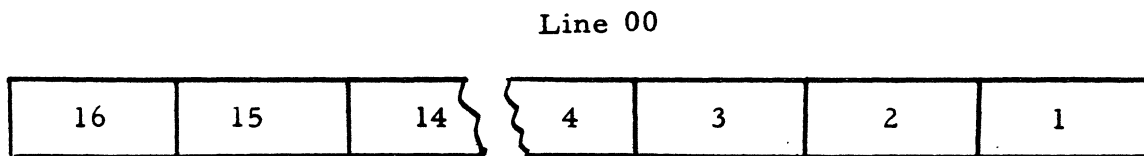
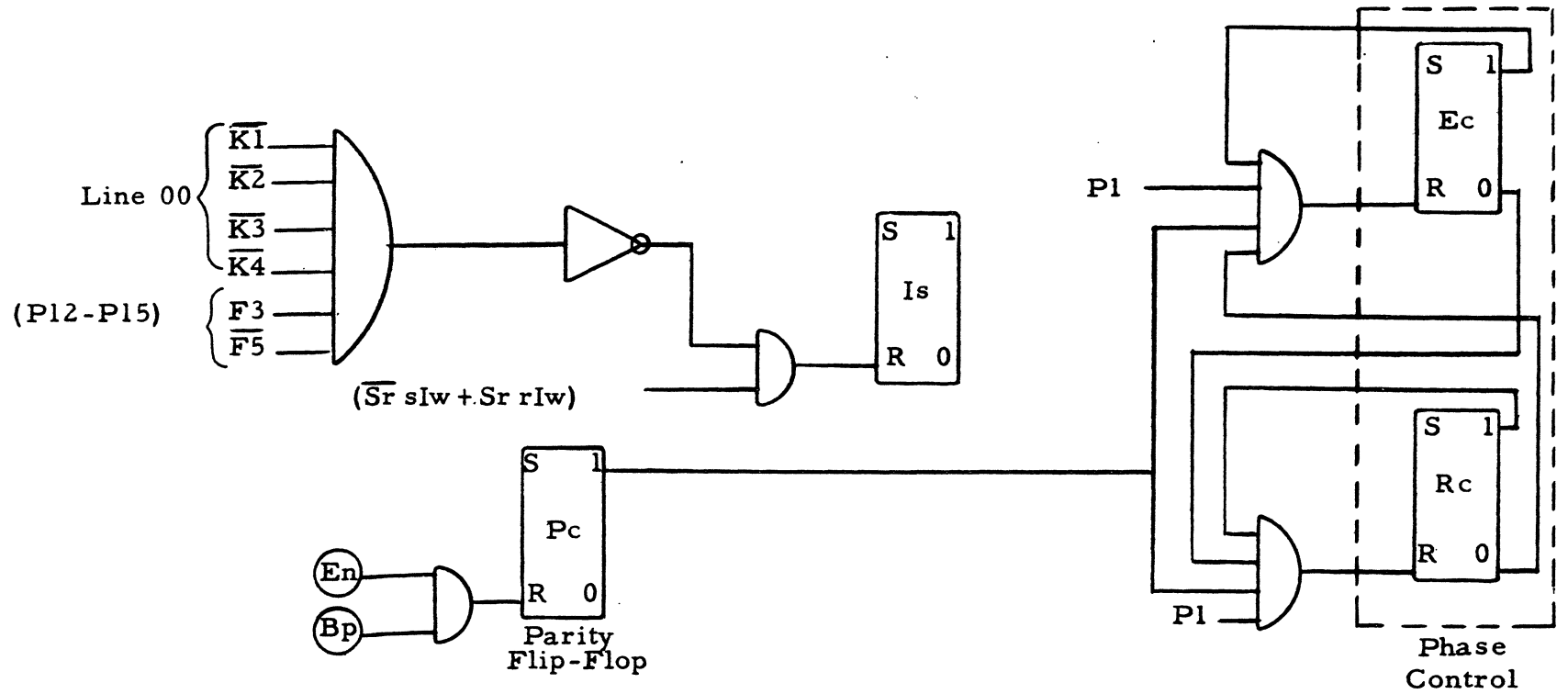
$$rPc = \dots + \textcircled{En} \textcircled{Bp} + \dots$$

To provide modulo 16 operation of the command sequence, when line 00 is the source of commands, pulse positions 12 through 15 are blocked from the comparison in the Is flip-flop (see Figure 2-13).

$$rIs = (\overline{Sr} sIw + Sr rIw) \left[ \dots \right] \left[ \overline{K4} \overline{K3} \overline{K2} \overline{K1} \overline{F5} \overline{F3} \right]$$

## E. DATA TRANSFER

The basic data transfers are "fetches" from the memory lines to the registers, and "stores" from the registers to the memory lines. The data stored is formed by the Ig gate (see Figure 2-14). This gate presents the contents of the C register for command 10, the contents of the A register for commands 01, 11, 41, 25, and 35, and the contents of the B register



Repeats 16 Times Per Machine Cycle

Figure 2-13. Parity Block, Modulo 16 Operation Logic Diagram



2-28

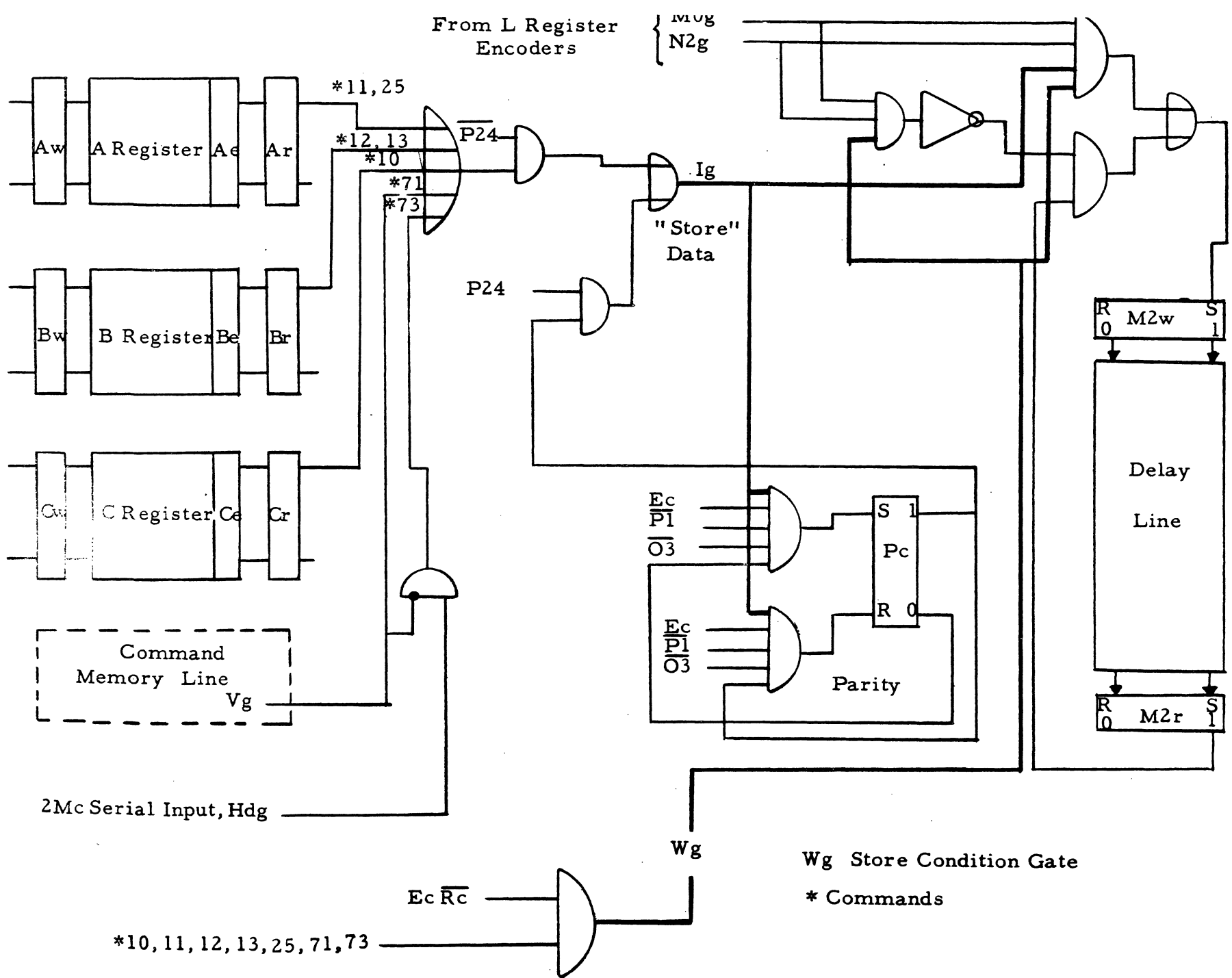


Figure 2-14. Data Transfer-'Stores' Logic Diagram

for commands 02, 03, 12, 13, and 36.

$$I_g = \overline{P24} \overline{O5} \overline{O2} \overline{O1} Cr + \overline{P24} \overline{O6} \overline{O2} O1 Ar + \overline{P24} \overline{O6} O2 Br + \overline{P24} \overline{O4} \overline{O2} Ar + \dots$$

For command 71, the stored data comes from the command line.

$$I_g = \dots + \overline{P24} O6 O5 \overline{O2} Vg + \dots$$

For command 73, the stored data comes from an input signal, Hdg, gated by Vg.

$$I_g = \dots + \overline{P24} O6 O5 O2 Vg Hdg + \dots$$

The last bit of each stored word is a parity bit to produce an even number of "1's" in each word (excluding P1).

$$\begin{aligned} I_g &= \dots + P24 Pc \\ sPc &= Ec \overline{Rc} \overline{P1} \overline{O5} O3 I_g \overline{Pc} + \dots \\ rPc &= Ec \overline{Rc} \overline{P1} \overline{O5} O3 I_g Pc + \dots \end{aligned}$$

Writing into a memory line is conditioned by phase 4 and commands 10, 11, 12, 13, 71, or 25.

$$W_g = \left( \overline{O6} \overline{O5} O4 \overline{O3} + O6 O5 O4 \overline{O3} O1 + \overline{O6} O5 \overline{O4} O3 \overline{O2} O1 \right) Ec \overline{Rc}$$

Writing into a particular memory line is conditioned by the operand line selector. For example, to write in memory line 02

$$\begin{aligned} sM2w &= M0g N2g Wg I_g + \overline{M0g} \overline{N2g} \overline{Wg} \overline{M2r} \\ rM2w &= M0g N2g Wg \overline{I_g} + \overline{M0g} \overline{N2g} \overline{Wg} \overline{M2r} \end{aligned}$$

where

$$\begin{aligned} \left[ \begin{array}{l} M0g = \overline{L0} \overline{L5} \overline{L4} \\ M1g = \overline{L0} \overline{L5} L4 \\ M2g = \overline{L0} L5 \overline{L4} \\ \text{etc.} \end{array} \right] \quad \text{and} \quad \left[ \begin{array}{l} N0g = \overline{L3} \overline{L2} \overline{L1} \\ N1g = \overline{L3} \overline{L2} L1 \\ N2g = \overline{L3} L2 \overline{L1} \\ \text{etc.} \end{array} \right] \end{aligned}$$

To make "fetches" from the memory, the line is selected by the address line selector (see Figure 2-15).

$$\begin{aligned} Fg &= M0g N0g M0r + M0g N1g M1r + \dots + M1g N7g M15r \\ &+ M3g N7g Ir + Nxg \end{aligned}$$

Parity is checked for commands 04, 05, 06, and 07, during phase 4 as well as during phase 2.

$$\begin{aligned} sPc &= \dots + \overline{P1} \overline{Ec} \overline{Rc} \overline{O6} \overline{O5} O3 Fg \overline{Pc} + \overline{P1} \overline{Ec} Rc Vg \overline{Pc} + \dots \\ rPc &= \dots + \overline{P1} \overline{Ec} \overline{Rc} \overline{O6} \overline{O5} O3 Fg Pc + \overline{P1} \overline{Ec} Rc Vg Pc + \dots \end{aligned}$$

If the parity is odd, the Pc flip-flop will block computation. The data selected by the "fetch" command is sent to the proper register. For commands 05 and 25, data is sent to A, for O6 and O7 to B, and for O4 to C.

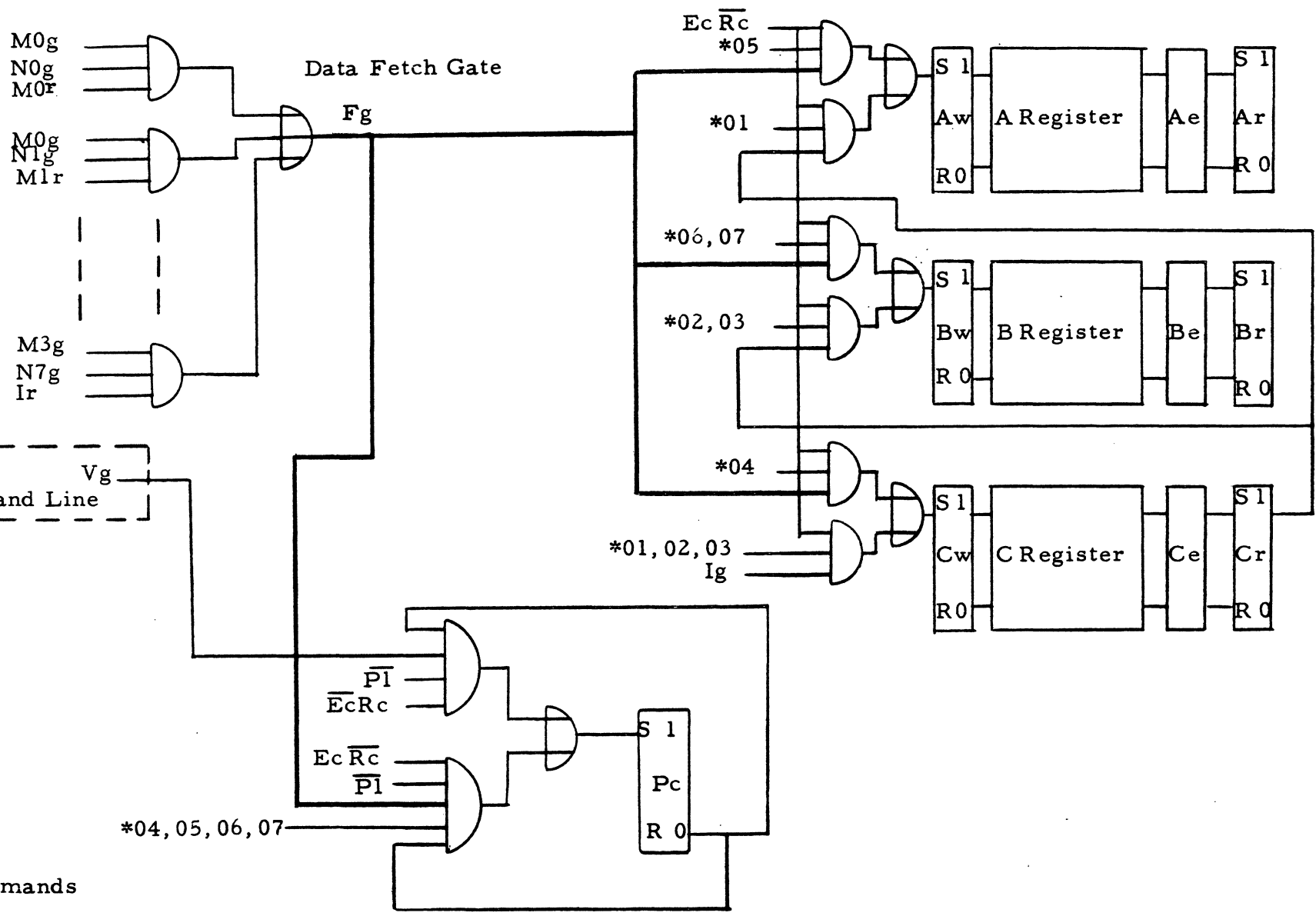
$$\begin{aligned} sAw &= \overline{Ec} \overline{Rc} \overline{O6} \overline{O4} O3 \overline{O2} O1 Fg + \dots \\ sBw &= \overline{Ec} \overline{Rc} \overline{O6} \overline{O5} \overline{O4} O3 O2 Fg + \dots \\ sCw &= \overline{Ec} \overline{Rc} \overline{O6} \overline{O5} \overline{O4} O3 \overline{O2} \overline{O1} Fg + \dots \end{aligned}$$

Command 01 provides an interchange between the A and C registers, and command 02 provides an interchange between the B and C registers.

$$\begin{aligned} sCw &= \dots + \overline{Ec} \overline{Rc} \overline{O6} \overline{O5} \overline{O4} \overline{O3} Ig + \dots \\ sAw &= \dots + \overline{Ec} \overline{Rc} \overline{O6} \overline{O5} \overline{O4} \overline{O3} \overline{O2} O1 Cr + \dots \\ sBw &= \dots + \overline{Ec} \overline{Rc} \overline{O6} \overline{O5} \overline{O4} \overline{O3} O2 Cr + \dots \end{aligned}$$

Command 03 provides a rotation (interchange) of information between the A, B and C registers.

During the first sector of execution of the 03 command the B and C registers interchange. At the end of the first sector of execution, the 03 command is changed to a 01 command by resetting the O2 flip-flop. During the second sector of execution the A and C registers interchange. The results of this command is that the C register is copied into the B register, the



\*Commands

Figure 2-15. "Fetch" Data Transfer Logic Diagram

B register is copied into the A register, and the A register is copied into the C register.

F. ADDITION AND SUBTRACTION

Commands 14, 15, 16, and 17 provide addition and subtraction into the A register and AB register pair (see Figure 2-16). The sum entered into these registers is formed in the adder.

$$Zg = \overline{\overline{Zg}}$$

$$\overline{Zg} = Xg Yg \overline{Ca} + Xg \overline{Yg} Ca + \overline{Xg} Yg Ca + \overline{Xg} \overline{Yg} \overline{Ca}$$

The input term from the memory is entered in "true" form for addition (commands 14 and 16) and inverted for subtraction (commands 15 and 17).

$$Xg = - - - + \overline{O5} \overline{O1} Fg + \overline{O5} O1 \overline{Fg} + - - -$$

The input term from the registers is taken from the B register for commands 16 and 17, and from the A register for commands 14 and 15. For the double precision commands 16 and 17, O2 is reset at the end of the first sector of execution which changes the commands from 16 to 14 and from 17 to 15.

$$Yg = - - - + \overline{O6} O4 \overline{O2} Ar + \overline{O5} O2 Br + - - -$$

The adder carry flip-flop, Ca, is cleared before any execution and set at the start of execution of commands 15 and 17 to add the "true" complement of the input term from the memory.

$$sCa = \overline{P1} \overline{P24} \overline{Ca} \overline{Ec} \overline{Rc} Xg Yg + P24 Rc Is \overline{O6} \overline{O5} O4 O3 O1 + - - -$$

$$rCa = \overline{P1} \overline{P24} Xg \overline{Yg} + Ca Rc + - - -$$

The resulting sum is entered into the B and A registers.

$$sBw = - - - + \overline{Ec} \overline{Rc} \overline{O6} \overline{O5} O4 O3 O2 Zg + - - -$$

$$sAw = - - - + Ec \overline{Rc} \overline{O6} \overline{O5} O4 O3 \overline{O2} Zg + - - -$$

Overflow at the sign position is used to set the Of flip-flop. An overflow occurs when the two adder inputs have the same sign and the result has

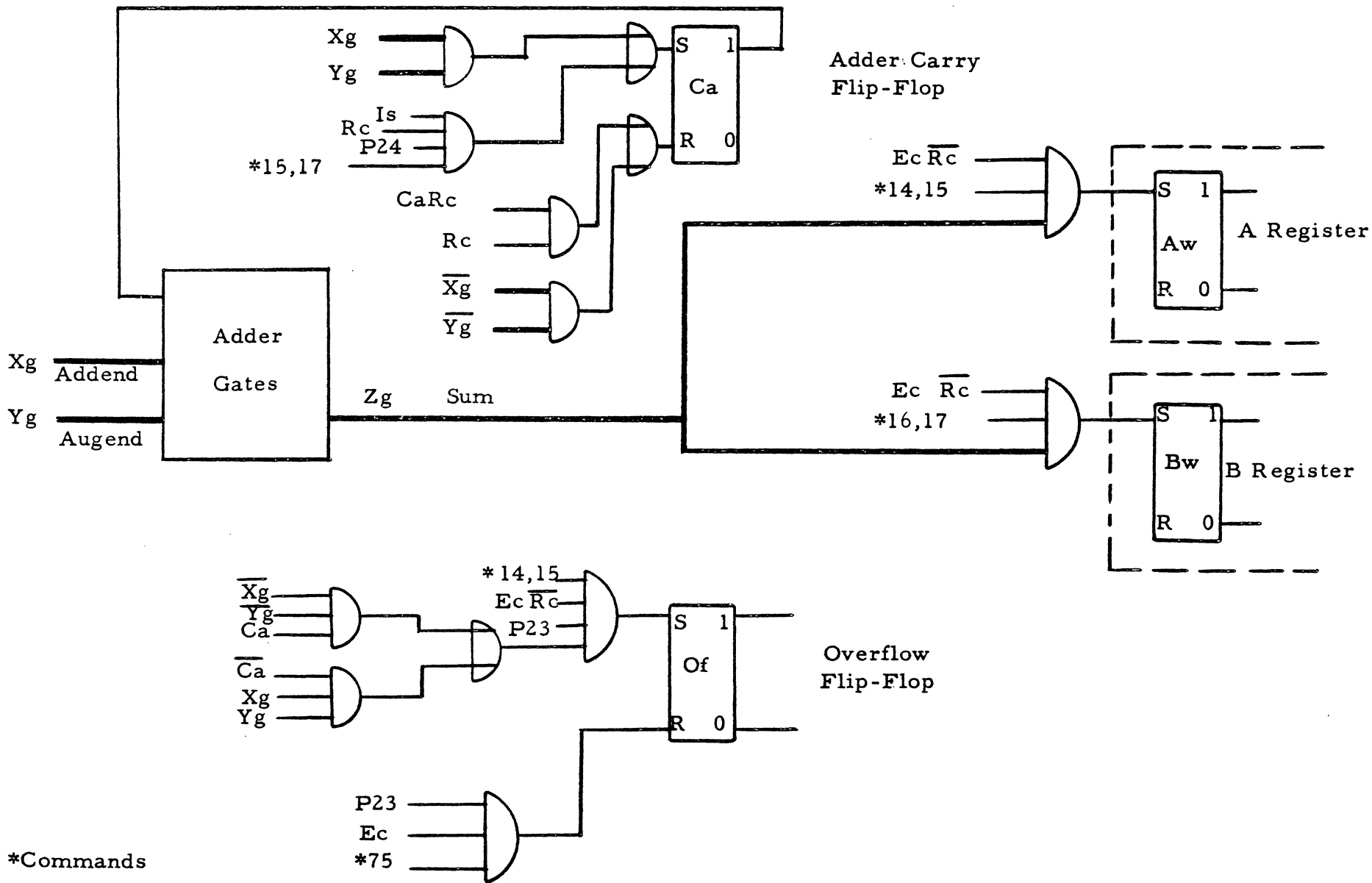


Figure 2-16. Addition and Subtraction Logic Diagram

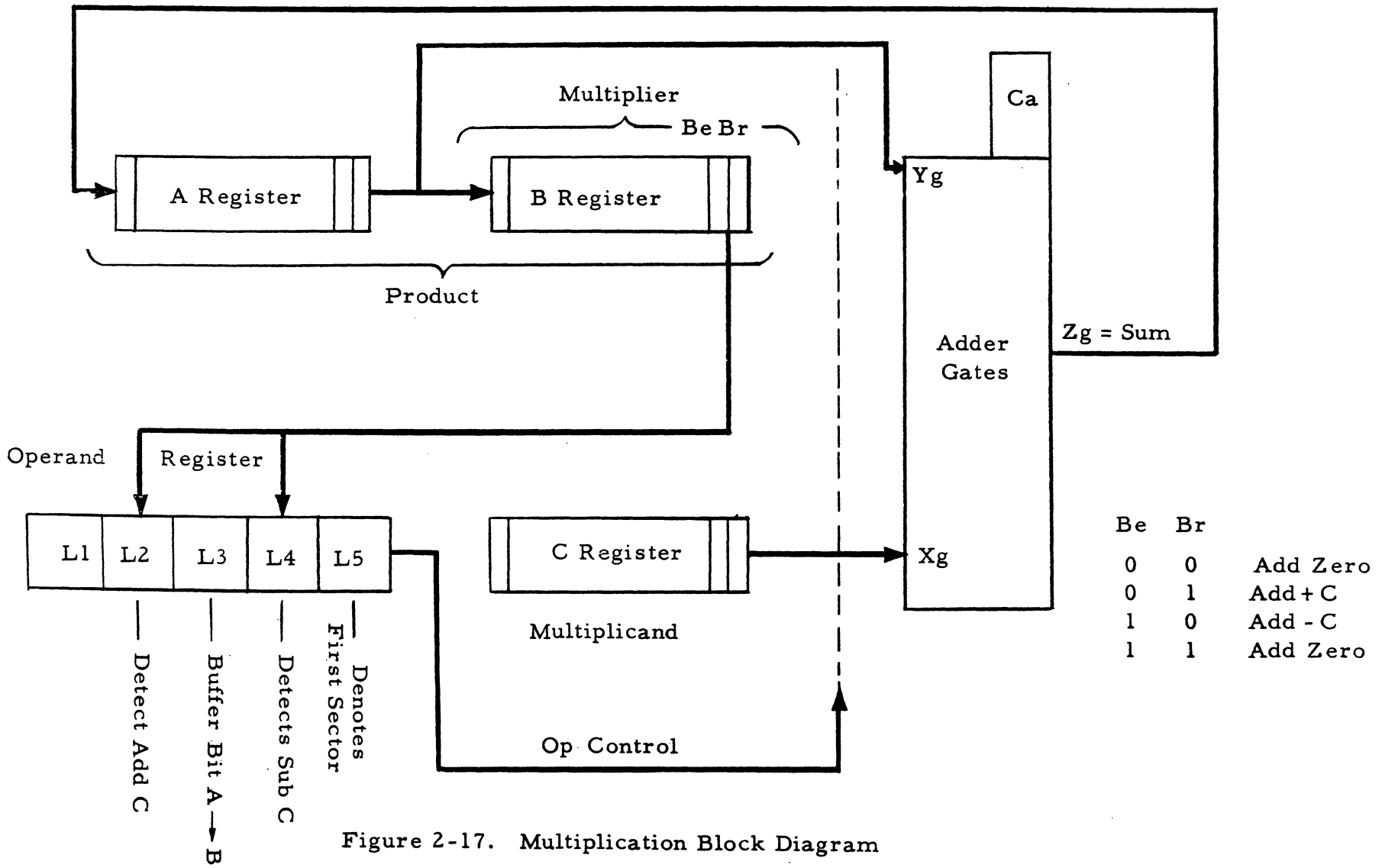


Figure 2-17. Multiplication Block Diagram

a different sign.

$$sOf = P23 Ec \overline{Rc} \overline{O6} \overline{O5} O4 O3 \overline{O2} (\overline{Xg} \overline{Yg} Ca + Xg Yg \overline{Ca}) + \dots$$

Of is reset by the execution of command 75 that tests for overflow.

$$rOf = P23 Ec O6 O5 O4 O3 \overline{O2} O1 + \dots$$

For commands 14, 15, 16, and 17, the parity of the information taken from the memory is checked through the Pc flip-flop.

### G. MULTIPLICATION

During the execution of command 32, the contents of the C register are multiplied by the contents of the B register (see Figure 2-17). The contents of the AB register pair are shifted to the right by one bit position for each sector of the multiplication operation, which placed the multiplier bits at the right end of the B register. Based on these multiplier bits, the A register has the contents of the C register added to it, subtracted from it, or a zero added to it. By this process the most significant bits of the product appear in the A register, and the least significant bits of the product appear in the B register.

The first sector of multiplication operation is marked by L5. At the end of the first sector, L5 is set (see Sheet 1, Figure 2-18).

$$sL5 = \dots + \overline{O6} O5 \overline{O3} P24 Ec$$

The multiplier bit code to add (C) is detected by L2.

$$sL2 = \dots + \overline{O6} O5 O4 \overline{O3} O2 \overline{O1} \overline{Be} Br P1 + \dots$$

$$rL2 = \dots + \overline{O6} O5 O4 \overline{O3} O2 \overline{O1} P24$$

The multiplier bit code to subtract (C) is detected by L4.

$$sL4 = \dots + \overline{O6} O5 O4 \overline{O3} O2 \overline{O1} P1 Be \overline{Br}$$

$$rL4 = \dots + \overline{O6} O5 O4 \overline{O3} O2 \overline{O1} P24$$



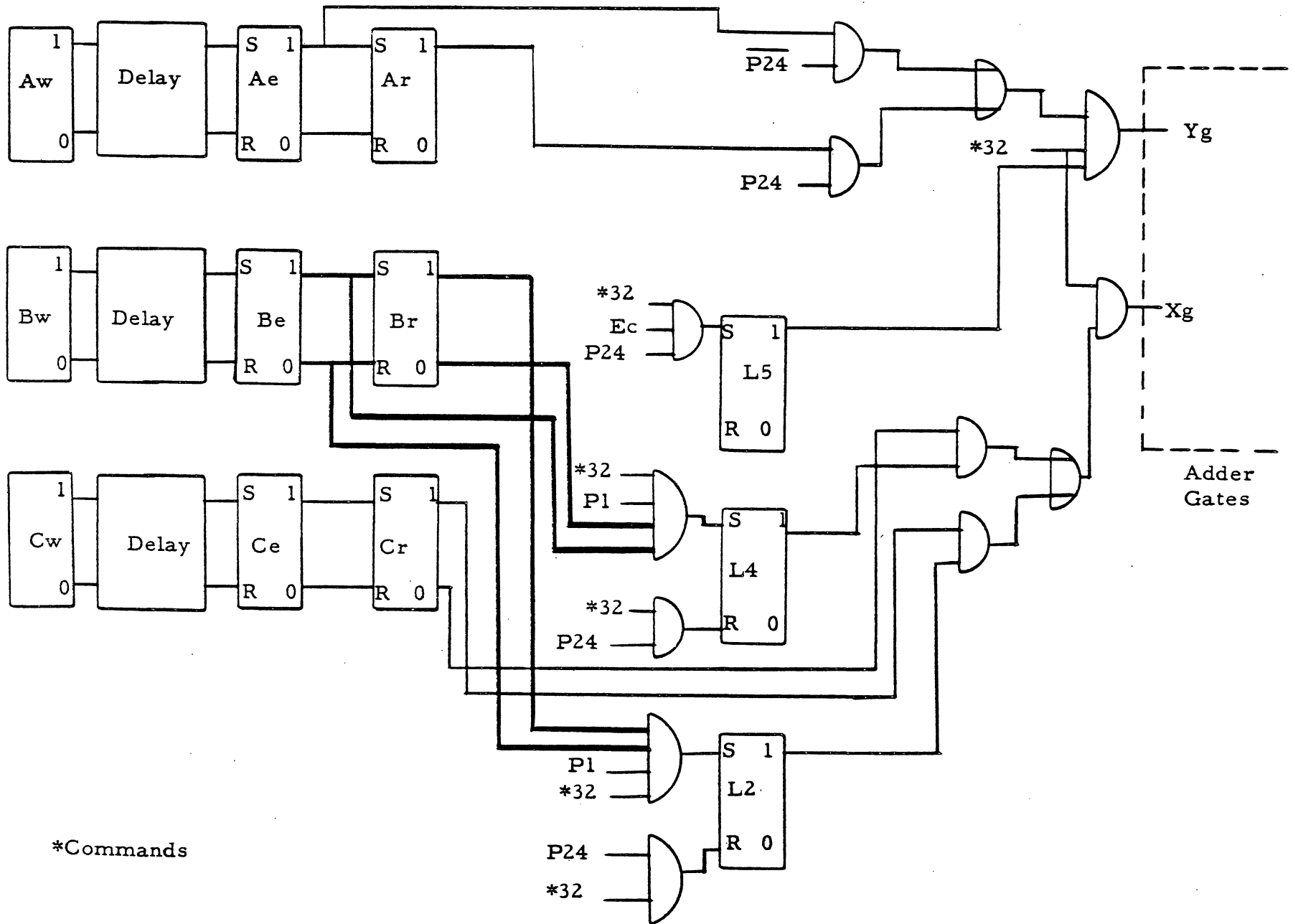


Figure 2-18. Multiplication Logic Diagram (Sheet 1 of 2)

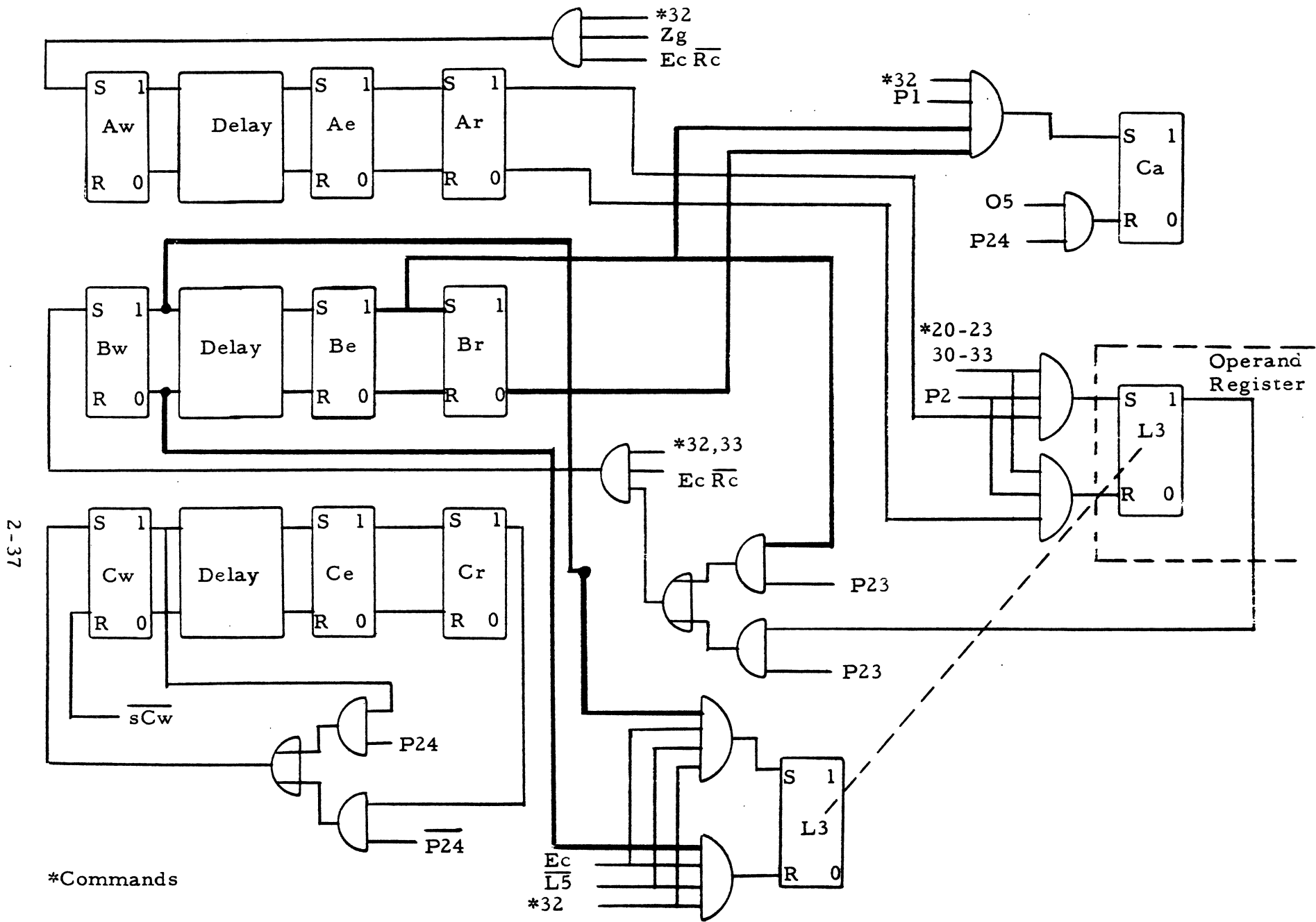


Figure 2-18. Multiplication Logic Diagram (Sheet 2 of 2)

The adder inputs, with the A register shifted to the right through Ae, and the entry of the C register controlled by L2 and L4, are as follows (see Sheet 1, Figure 2-18):

$$\begin{aligned} Xg &= \text{---} + \overline{O6} O5 O4 \overline{O3} O2 \overline{O1} (L2 Cr + L4 \overline{Cr}) + \text{---} \\ Yg &= \text{---} + \overline{O6} O5 O4 \overline{O3} O2 L5 (\overline{P24} Ae + P24 Ar) + \text{---} \\ sCa &= \text{---} + \overline{O6} O5 O4 \overline{O3} O2 \overline{O1} P1 Be \overline{Br} \\ rCa &= \text{---} + O5 P24 \end{aligned}$$

Qualifying Yg by L5 clears the A register during the first sector of operation. When subtracting, the adder carry flip-flop, Ca, is set to obtain the "true" complements of the C register.

The output of the adder, Zg, is recorded in the A register (see Sheet 2, Figure 2-18).

$$sAw = \text{---} + Ec \overline{Rc} \overline{O6} O5 O4 \overline{O3} O2 Zg + \text{---}$$

To start the multiplier bit code properly, the P1 bit position of the B register is kept clear during all recirculation. During multiplication, the B register is shifted to the right, by the B register early flip-flop, Be; and the bits from the A register enter the left end of the B register through the operand line selector register flip-flop, L3.

$$sBw = \text{---} + Ec \overline{Rc} \overline{O6} O5 \overline{O3} O2 (\overline{P23} Be + P23 L3) + \overline{P1} Br (\overline{\quad}) + \text{---}$$

The bits shifted from the right end of the A register are detected and stored in L3 for entry into the left end of the B register.

$$\begin{aligned} sL3 &= \text{---} + \overline{O6} O5 \overline{O3} (\text{---} + P2 Ar) + \text{---} \\ rL3 &= \text{---} + \overline{O6} O5 \overline{O3} (\text{---} + P2 \overline{Ar}) + \text{---} \end{aligned}$$

During the first sector of multiplication, the sign of the B register is retained in P23 of the B register so that the last sector of multiplication will

operate correctly. The  $\overline{L5}$  signal is used to repeat the sign.

$$\begin{aligned} sL3 &= - - - + \overline{O6} O5 O4 \overline{O3} O2 \overline{O1} Ec \overline{L5} Be \\ rL3 &= - - - + \overline{O6} O5 O4 \overline{O3} O2 \overline{O1} Ec \overline{L5} \overline{Be} \end{aligned}$$

For proper operation of the sign of the product in the A register, the sign bit of the C register is extended into P24.

$$sCw = - - - + P24 Cw + \overline{P24} Cr \left[ \text{---} \right] + - - -$$

The following timing chart indicates that process of multiplication for a shortened set of registers. The multiplier has four bits, a sign, and the sign repeated during the first sector of multiplication. The bit pair at the right end of the B register controls the arithmetic operation as follows:

- 00 add zero
- 01 add + (C)
- 10 add - (C)
- 11 add zero

$$(C) = +9/16$$

	0 0. 1 0 0 1 X	
	(A)	(B) = +13/16
	X - - - - X	X 0. 1 1 0 1 0
1)	1 1. 0 1 1 1 X	X 0. 0 1 1 0 1
2)	0 0. 0 1 0 0 X	X 1. 0 0 1 1 0
3)	1 1. 1 0 0 1 X	X 0. 1 0 0 1 1
4)	1 1. 1 1 0 0 X	X 1. 0 1 0 0 1
5)	0 0. 0 1 1 1 X	X 0. 1 0 1 0 0
6)	0 0. 0 0 1 1	X 1. 0 1 0 1 0

$$(AB) = 117/256 (1/2)$$

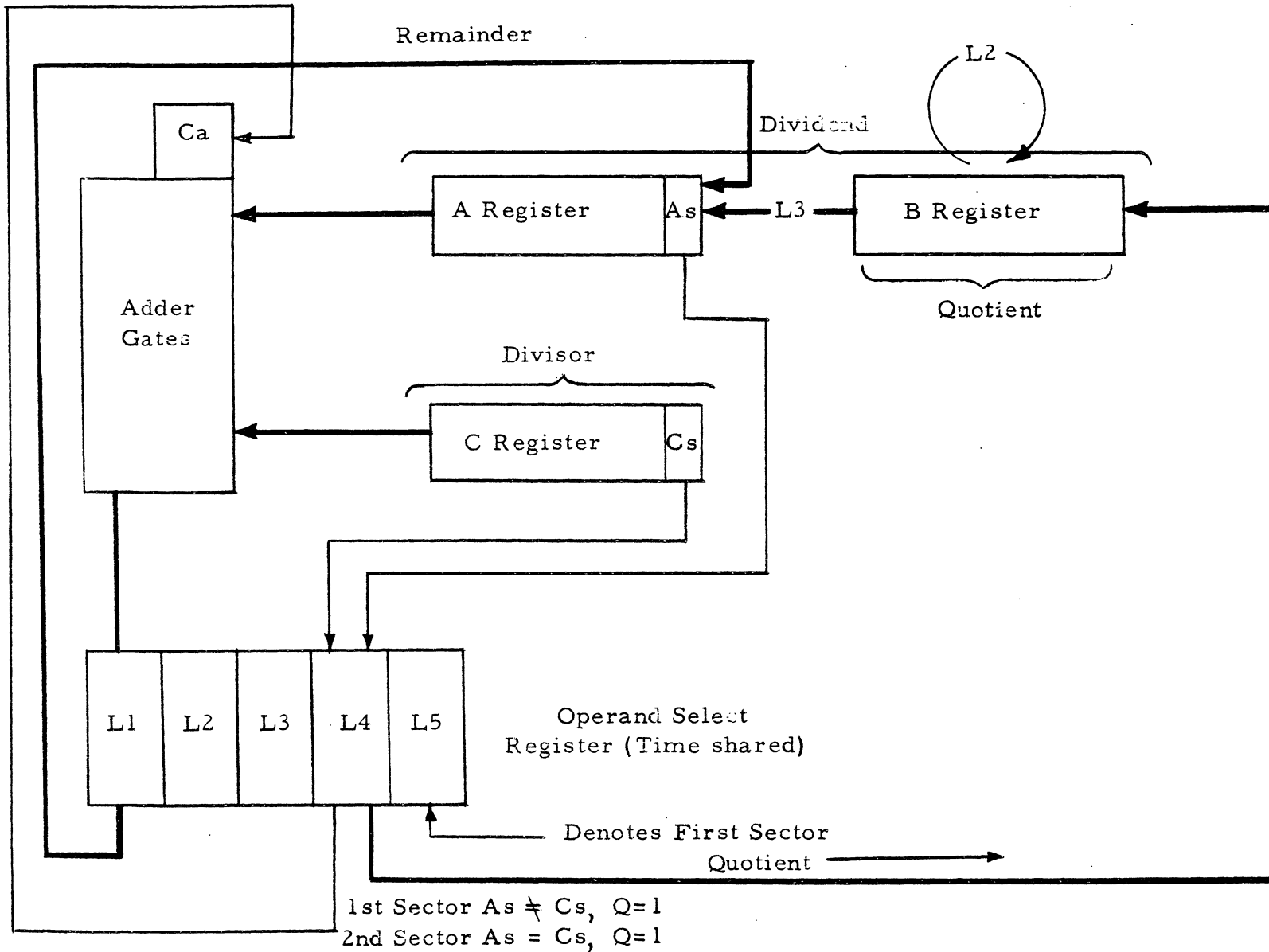


Figure 2-19. Division Block Diagram

For the sixth (last) sector, the sign and the repeated sign are used to provide a shift only, and produce  $1/2 (C) (B)$  in AB. This last step is to ensure the correct product when B and C start as -1, as shown in the following timing chart.

	(C) = -1														
	1 1.0 0 0 0 X														
	(A)						(B) = -1								
	X	-	-	-	-	-	X	X	1.0	0	0	0	0	0	0
1)	0	0.0	0	0	0	0	X	X	1.1	0	0	0	0	0	0
2)	0	0.0	0	0	0	0	X	X	0.1	1	0	0	0	0	0
3)	0	0.0	0	0	0	0	X	X	0.0	1	1	0	0	0	0
4)	0	0.0	0	0	0	0	X	X	0.0	0	1	1	0	0	0
5)	0	1.0	0	0	0	0	X	X	0.0	0	0	1	1	0	0
6)	0	0.1	0	0	0	0	X	X	0.0	0	0	0	0	1	1
	(AB) = 1 (1/2)														

#### H. DIVISION

During the execution of command 31, the contents of the AB register pair are divided by the contents of the C register (see Figure 2-19). During each sector of the division operation, the divisor is added to or subtracted from the remainder, depending on whether the sign of the divisor matches the sign of the remainder. For each sector of operation, the remainder is doubled by shifting the sum of the A and C registers ( $A \pm C$ ) to the left one bit position in the A register, and shifting the B register to the left one bit position. The bits of the quotient are entered into the right end of the B register as a function of the sign of each remainder.

The first sector of division operation is marked by  $\overline{L5}$ . At the end of

the first sector, L5 is set by the same term used for multiplication. The signs of the A and C registers are compared and, if the signs are the same, L4 is set to indicate that subtraction of the C register is required (see Sheet 1, Figure 2-20). This comparison is made while the division command is being read as well as during execution of the division command.

The adder inputs for division are (see Sheet 2, Figure 2-20):

$$\begin{aligned} Xg &= \overline{O6} O5 O4 \overline{O3} \overline{O2} (\overline{L4} Dg + L4 \overline{Dg}) + \dots \\ Yg &= \dots + \overline{O6} O4 \overline{O2} Ar + \dots \\ Dg &= O1 Cr + \dots \\ sCa &= \dots + \overline{O6} O5 O4 \overline{O3} \overline{O2} P1 L4 \\ rCa &= \dots + O5 P24 \end{aligned}$$

When subtracting, the adder carry flip-flop, Ca, is set to obtain the "true" complement of the C register.

The output of the adder, Zg, is delayed through L1 and recorded into the A register (see Sheet 1, Figure 2-20).

$$\begin{aligned} sL1 &= \dots + \overline{O6} O5 O4 \overline{O3} \overline{O2} Ec (Zg O4 + Ar \overline{O4}) + \dots \\ rL1 &= \dots + \overline{O6} O5 O4 \overline{O3} \overline{O2} Ec (\overline{Zg} O4 + \overline{Ar} \overline{O4}) + \dots \\ sAw &= \dots + Ec \overline{Rc} \overline{O6} O5 \overline{O3} \overline{O2} (\overline{P23} \overline{P2} L1 + P2 L3 + P23 O4 L1) \\ &\quad + \dots \end{aligned}$$

The storage of bits shifted from the left end of the B register for entry into the right end of the A register is handled by L3.

$$\begin{aligned} sL3 &= \dots + \overline{O6} O5 \overline{O3} (P24 Bw + \dots) + \dots \\ rL3 &= \dots + \overline{O6} O5 \overline{O3} (P24 \overline{Bw} + \dots) + \dots \end{aligned}$$

The shifting of the contents of the B register is handled through L2.







$$\begin{aligned}
sL2 &= - - - + \overline{O6} O5 \overline{O3} \overline{O2} E_c Br + - - - \\
rL2 &= - - - + \overline{O6} O5 \overline{O3} \overline{O2} E_c \overline{Br} + - - - \\
sBw &= - - - + \overline{O6} O5 O4 \overline{O3} \overline{O2} [E_c \overline{P2} \overline{P3} L2 + - - - ]
\end{aligned}$$

During the division operation, the bits of the quotient are entered into the B register at pulse position P3.

$$sBw = - - - + \overline{O6} O5 O4 \overline{O3} \overline{O2} [E_c P3 (\overline{L5} \overline{L4} + L5 L4) + - - - ]$$

Each quotient bit is a "1" when the remainder and divisor have like signs, except for the first sector of operation, when the sign of the quotient is formed. During the first sector, indicated by  $\overline{L5}$ , unlike signs produce a "1" for a negative quotient.

Immediately after the last sector of division, the last bit of the quotient is entered into bit position P2 of the B register.

$$sBw = - - - + \overline{O6} O5 O4 \overline{O3} \overline{O2} [\overline{E_c} P2 L4 + - - - ]$$

The L4 flip-flop compares the sign of the remainder in the A register with the sign of the divisor in the C register at P24.

$$\begin{aligned}
sL4 &= - - - \overline{O6} O5 O4 \overline{O3} \overline{O2} P24 E_c (L1 Cr + \overline{L1} \overline{Cr}) + - - - \\
rL4 &= - - - \overline{O6} O5 O4 \overline{O3} \overline{O2} P23 L4
\end{aligned}$$

The new sign of the register A is taken from the L1 flip-flop.

The first comparison is made as the division command is read. For normal division, the first signs are taken at P23. For division of a remainder, the first signs are taken at P24 under the control of the code bit in the L1 flip-flop.

$$sL4 = - - - + \overline{O6} O5 O4 \overline{O3} \overline{O2} [- - - P23 R_c \overline{L1} \overline{Zg} + P24 R_c L1 \overline{Zg} ]$$

When the division command is read at P23 and P24, with  $C_a = 0$  and  $L4 = 0$ ,  $\overline{Zg} = Ar Cr + \overline{Ar} \overline{Cr}$ .

The following timing charts show some short register division operations:

$$(C) = 1/2$$

0 0. 1 0 0 0 X		
(AB) = -1		I
⊕	X 1. 0 0 0 0 X	X 0. 0 0 0 0 0
+	1 1. 0 0 0 0 X	X 0. 0 0 1 0 0
+	1 1. 0 0 0 0 X	X 0. 0 1 0 0 0
+	1 1. 0 0 0 0 X	X 0. 1 0 0 0 0
	1 1. 0 0 0 0 X	X 1. 0 0 0 0 0

$$(A) = -1$$

$$(B) = -1$$

$$(C) = +11/16$$

0 0. 1 0 1 1 X		
(AB) = 143/256		II
⊖	X 0. 1 0 0 0 X	X 1. 1 1 1 0 0
+	1 1. 1 0 1 1 X	X 1. 1 1 0 0 0
-	0 0. 1 1 0 1 X	X 1. 1 0 0 1 0
-	0 0. 0 1 0 1 X	X 1. 0 0 1 1 0
	1 1. 0 1 0 1 X	X 0. 0 1 1 0 0

$$(A) = -11/16$$

$$(B) = 6/16$$

$$(C) = 3/4$$

0 0.1 1 0 0 X		
(AB) = 3/4		III
⊖ - + +	X 0.1 1 0 0 X	X 0.0 0 0 0 0
	0 0.0 0 0 0 X	X 0.0 0 0 1 0
	1 0.1 0 0 0 X	X 0.0 0 1 0 0
	1 0.1 0 0 0 X	X 0.0 1 0 0 0
	1 0.1 0 0 0 X	X 0.1 0 0 0 0

$$(A) = -6/4$$

$$(B) = +1/2$$

$$(C) =$$

1 1.1 0 0 0 X		
(AB) = 3/4		IV
⊕ + + -	X 0.1 1 0 0 X	X 0.0 0 0 0 0
	0 0.1 0 0 0 X	X 0.0 0 1 0 0
	0 0.0 0 0 0 X	X 0.0 1 0 0 0
	1 1.0 0 0 0 X	X 0.1 0 0 1 0
	1 1.0 0 0 0 X	X 1.0 0 1 1 0

$$(A) = -1$$

$$(B) = -13/16$$

With four-bit plus sign registers,  $1/2 \frac{(AB)}{(C)}$  is formed in the B register in four sectors of operation. The operation may be programmed for five sectors to give  $\frac{(AB)}{(C)}$  if the quotient is less than one in magnitude. When dividing the non-restored remainder by the C register, the operation should be performed for five sectors to eliminate the quotient's sign. A negative divisor results in a quotient that is a "1's" complement of the desired quotient (see example 4 below).

The relationship between the uncorrected remainder in A and the true remainder, R, can be defined as follows:

$$R = 1/2 (A) \quad \text{if the sign of (A) is the same as the sign of (C)}$$

$$R = 1/2 (A) + (C) \quad \text{if the sign of (A) differs from the sign of (C)}$$

The fractional remainders for the four examples are as follows:

$$\text{I. } \frac{R}{C} = \frac{1/2 (-1) + (1/2)}{(1/2)} = 0$$

$$\text{II. } \frac{R}{(C)} = \frac{1/2 (-11/16) + (11/16)}{(11/16)} = 1/2$$

$$\text{III. } \frac{R}{(C)} = \frac{1/2 (-6/4) + (3/4)}{(3/4)} = 0$$

$$\text{IV. } \frac{R}{(C)} = \frac{1/2 (-1)}{(-1/2)} = 1$$

This fractional remainder,  $\frac{R}{(C)}$ , represents the correction which must be made to the least significant bit position in the B register. For example, in equation IV above;  $(3/4) (-1/2) = 2 (-13/16) + (11/16) = 2 (-12/16) = 1 \ 1/2$

## I. SQUARE ROOT

During the execution of command 30, the square root of the contents of the AB register pair is extracted (see Figure 2-21). In the first sector of operation, a trial subtraction of  $(0.1)^2$  is made into the A register. In the second sector, the  $(0.1)^2$  is added back into the A register and, either  $(0.11)^2$  is trial subtracted, if the  $(0.1)^2$  will go (remainder in A register positive), or  $(0.01)^2$  is trial subtracted, if the  $(0.1)^2$  will not go (remainder in A register negative). For example, in the fifth sector,  $(0.pqr 1)^2$  is on whether the "1" in  $(0.pqr 1)^2$  goes or not. The value of p is a "1" if the first remainder is

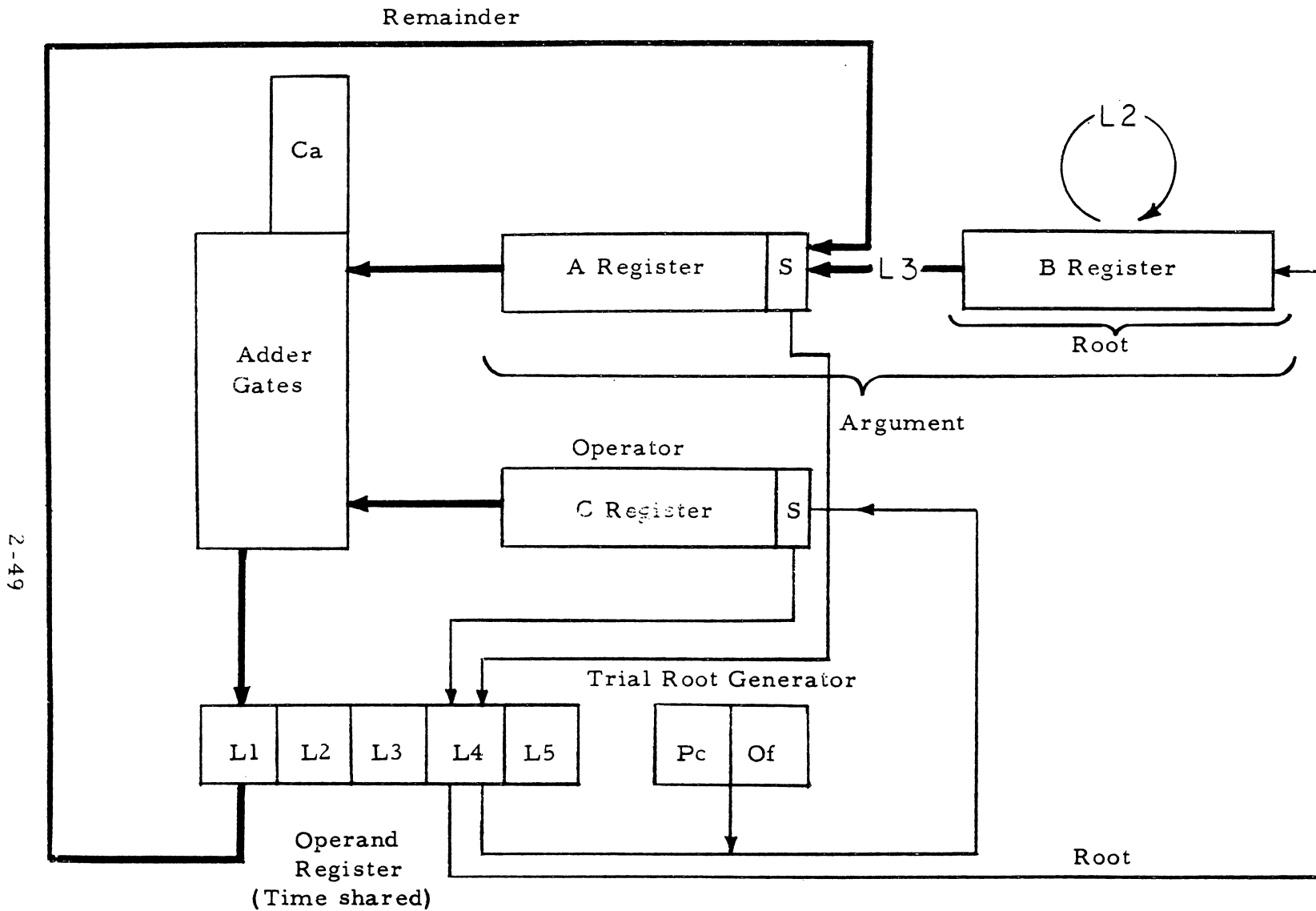


Figure 2-21. Square Root Block Diagram

positive; q is a "1" if the second remainder is positive; etc. Table 2-2 shows the values added into the A register for successive sectors.

Table 2-2.

SQUARE ROOT OPERATION

Sector No.	If Remainder in A Positive	If Remainder in A Negative
1	-0.0 1 -	- - -
2	-0.0 1 0 1 p = 1	p = 0 + 0.0 0 1 1
3	-0.0 0 p 1 0 1 q = 1	q = 0 + 0.0 0 p 0 1 1
4	-0.0 0 0 p q 1 0 1 r = 1	r = 0 + 0.0 0 0 p q 0 1 1
5	-0.0 0 0 0 p q r 1 0 1 s = 1	s = 0 + 0.0 0 0 0 p q r 0 1 1

These values follow from the arithmetic, since

$$(A) : (0.pq1)^2 - (0.pq11)^2 = -(0.000pq101),$$

Rule

$$(B) : (0.pq1)^2 - (0.pq01)^2 = +(0.000pq011), \text{ etc.}$$

The data handling procedure is similar to that of division; the remainder in the AB register pair is shifted to the left by one position for each sector of operation and the sign of each remainder is used to enter each bit of the answer into the right end of the B register. This allows the bits of the root, p, q, r, etc., to be inserted and retained in bit positions 22, 21, 20, etc., of the C register as they are determined during the basic division process.

The information of the new C register number is synchronized by the parity flip-flop, Pc, and the overflow flip-flop, Of, (see Figures

2-22 and 2-23).

$$sPc = - - - + P24 Ec \overline{O6} O5 O4 \overline{O3} \overline{O2} \overline{O1} \overline{Of} Dg + - - -$$

$$rPc = - - - + Ec \overline{O6} O5 O4 \overline{O3} \overline{O2} \overline{O1} Of Pc$$

$$sOf = - - - + \overline{Of} Ec \overline{O6} O5 O4 \overline{O3} \overline{O2} \overline{O1} Pc + - - -$$

$$rOf = - - - + \overline{P23} \overline{O6} O5 O4 \overline{O3} \overline{O2} \overline{O1} + - - -$$

The new value for the C register is formed as

$$Dg = - - - + \overline{O1} L5 (Of \overline{Pc} Cr + Of Pc L4 + \overline{Of} Pc \overline{L4} + \overline{Of} \overline{Pc} Ce)$$

$$+ \overline{O1} \overline{L5} F5 F3 \overline{F2} F1$$

$$sCw = - - - + Ec \overline{Rc} \overline{O6} O5 O4 \overline{O3} \overline{O2} \overline{O1} Dg + - - -$$

The L5 flip-flop in its "false" condition ( $\overline{L5}$ ) blocks the normal terms and enters a "1" bit in P21, permitting the starting value of  $(0.01)^2$  to be entered in the C register during the first sector of operation. This bit is shifted by the  $\overline{Of} \overline{Pc} Ce$  term in each succeeding sector. After the bit has been shifted, the sign of each previous remainder and its inverse are entered in the C register by the L4 flip-flop. The balance of the C register is retained after the inverted sign. The new value for the C register is added to, or subtracted from, the A register as described on page 2-48. An example is shown in the following chart, using a set of shortened registers.



$$(C) = 1/2$$

Initial	0 0, 1 0 0 0 X	
	X 0. 1 0 1 0 X	X 1.0 0 1 0 0
(AB) = 169/256		
Sector 1	0 0. 0 1 0 0 X	
	0 0. 1 1 0 1 X	X 0.0 1 0 1 0
(AB) = 105/128		
Sector 2	0 0. 1 0 1 0 X	
	0 0. 0 1 1 0 X	X 0.1 0 1 1 0
(AB) = 25/64		
Sector 3	0 0. 1 1 0 1 X	
	1 1. 0 0 1 0 X	X 1.0 1 1 0 0
(AB) = -27/32		
Sector 4	0 0. 1 1 0 1 1	
	1 1. 1 1 1 1 X	X 0.1 1 0 0 0

$$(A) = -1/16$$

$$(B) = 12/16$$

A minor error is produced in the last sector since the "1" shifted into P1 of the C register is not used to compute the final remainder. The A register should have been zero and the answer in the B register should have been 13/16.

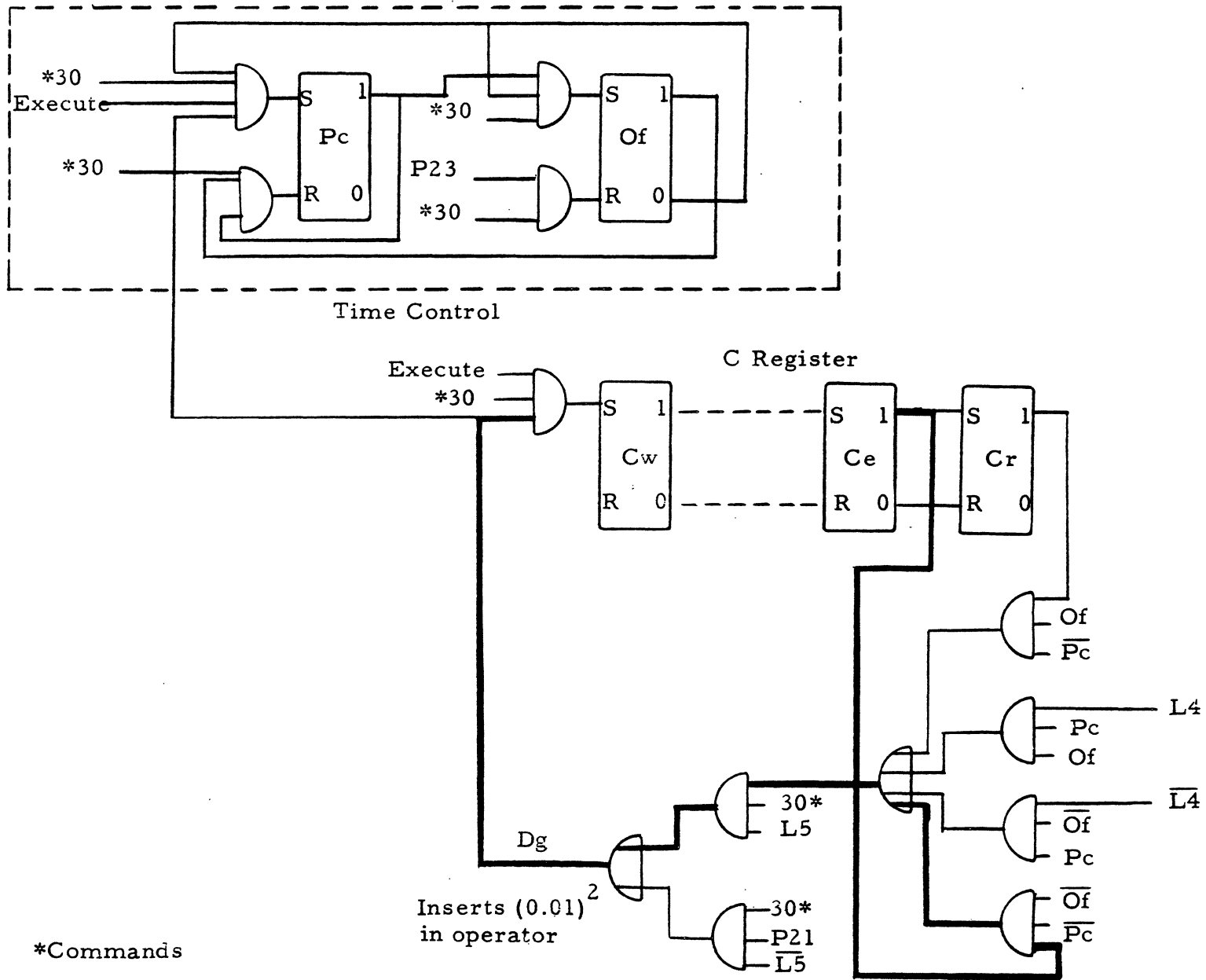


Figure 2-22. Square Root, Logic Diagram

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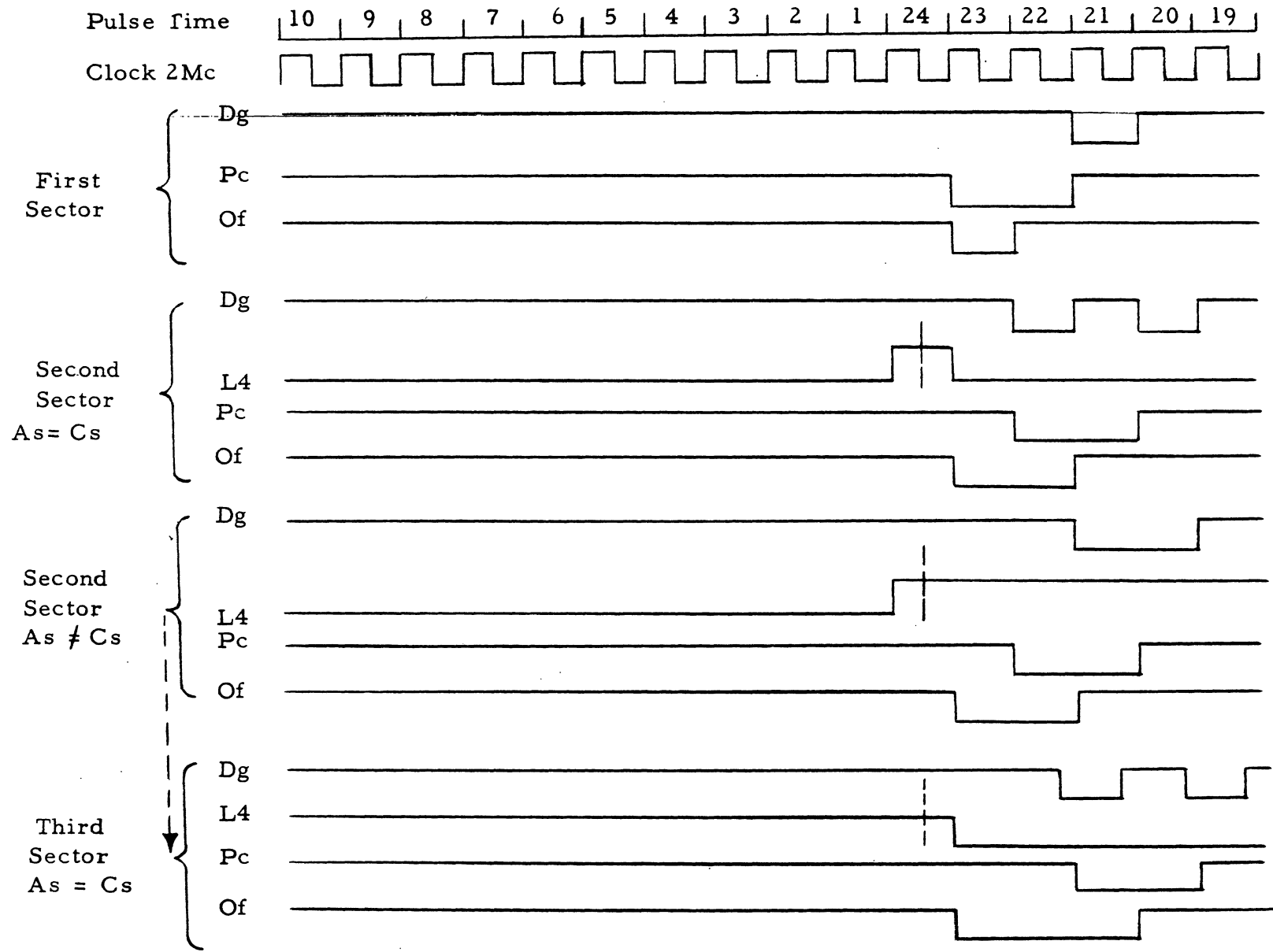


Figure 2-23. Square Root, Timing Diagram

J. SHIFT COMMANDS

Commands 20 and 21 initiate a shift left of the AB register pair (see Figure 2-24).

The A register is shifted left through L1,

$$\begin{aligned} sL1 &= - - - + \overline{O6} O5 \overline{O3} \overline{O2} E_c (Z_g O4 + A_r \overline{O4}) + - - - \\ rL1 &= - - - + \overline{O6} O5 \overline{O3} \overline{O2} E_c (\overline{Z_g} O4 + \overline{A_r} \overline{O4}) + - - - \\ sAw &= - - - + E_c \overline{R_c} \overline{O6} O5 \overline{O3} \overline{O2} (\overline{P23} \overline{P2} L1 + - - -) + - - - \\ &\quad + \overline{O6} O5 \overline{O4} \overline{O3} P23 A_r + - - - \end{aligned}$$

the B register is shifted left through L2,

$$\begin{aligned} sL2 &= - - - + \overline{O6} O5 \overline{O3} \overline{O2} E_c B_r + - - - \\ rL2 &= - - - + \overline{O6} O5 \overline{O3} \overline{O2} E_c \overline{B_r} + - - - \\ sBw &= - - - + E_c \overline{R_c} \overline{O6} O5 \overline{O4} \overline{O3} \overline{O2} \overline{P2} L2 + - - - \end{aligned}$$

while the shift left from B to A is handled through L3.

$$\begin{aligned} sL3 &= - - - + \overline{O6} O5 \overline{O3} (P24 B_w + - - -) + - - - \\ rL3 &= - - - + \overline{O6} O5 \overline{O3} (P24 \overline{B_w} + - - -) + - - - \\ sAw &= - - - + E_c \overline{R_c} \overline{O6} O5 \overline{O3} \overline{O2} (- - - + P2 L3 + - - -) + - - - \end{aligned}$$

Commands 22 and 23 initiate a shift right of the AB register pair (see Figure 2-25). The A register is shifted right through Ae,

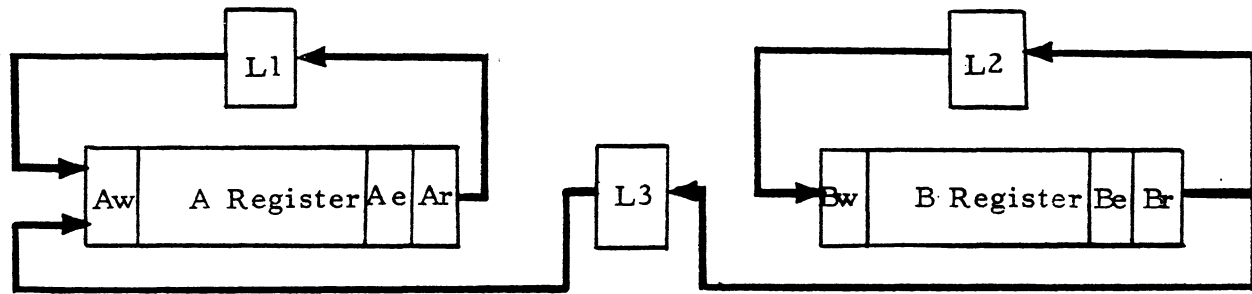
$$\begin{aligned} sAw &= - - - + E_c \overline{R_c} \overline{O6} O5 \overline{O4} \overline{O3} O2 \overline{P23} A_e + \overline{O6} O5 \overline{O4} \overline{O3} P23 A_r \\ &\quad + - - - \end{aligned}$$

the B register is shifted right through Be,

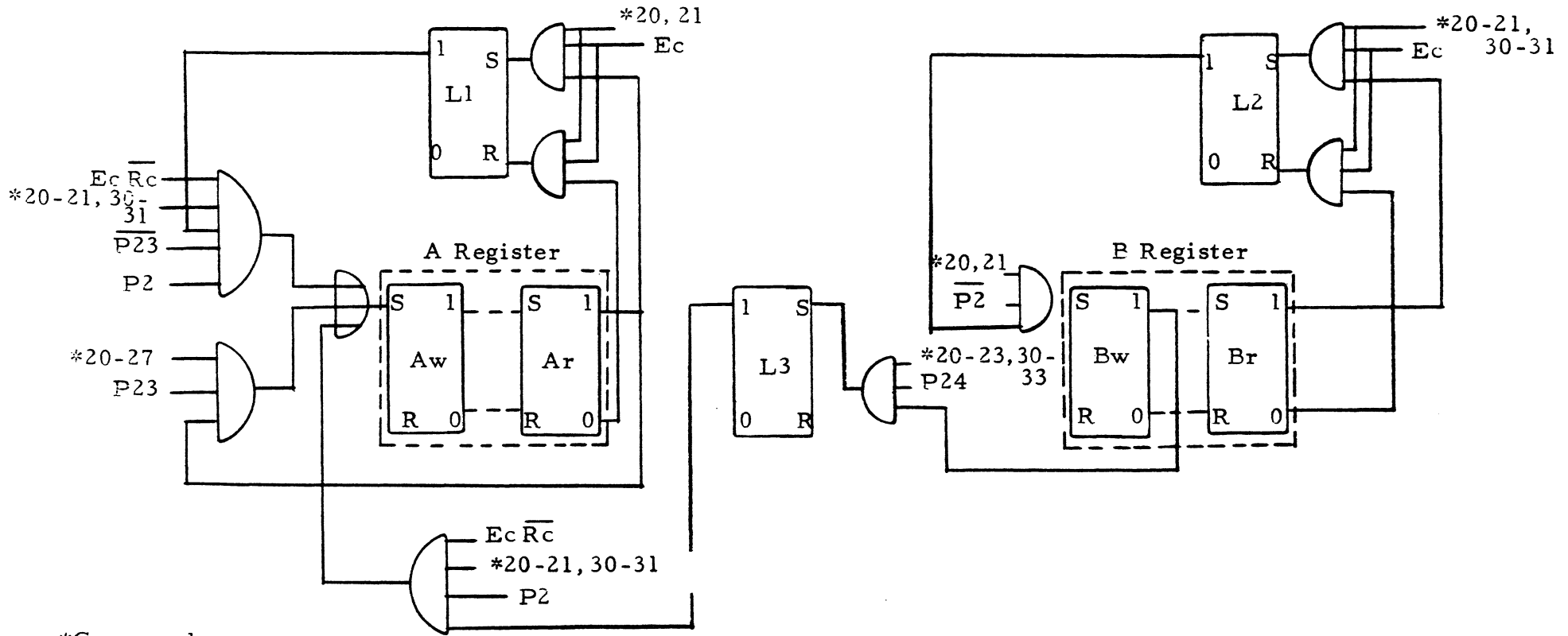
$$sBw = - - - + E_c \overline{R_c} \overline{O6} O5 \overline{O3} O2 (\overline{P23} B_e + - - -) + - - -$$

while the shift right from A to B is handled through L3,

$$\begin{aligned} sL3 &= - - - + \overline{O6} O5 \overline{O3} (- - - + P2 A_r) + - - - \\ rL3 &= - - - + \overline{O6} O5 \overline{O3} (- - - + P2 \overline{A_r}) + - - - \\ sBw &= - - - + E_c \overline{R_c} \overline{O6} O5 \overline{O3} O2 (- - - + P23 L3) + - - - \end{aligned}$$

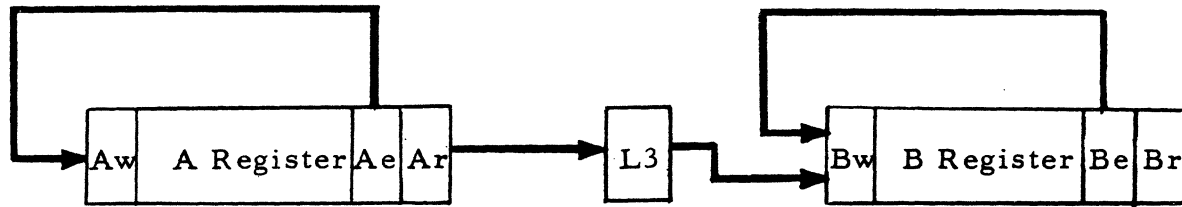


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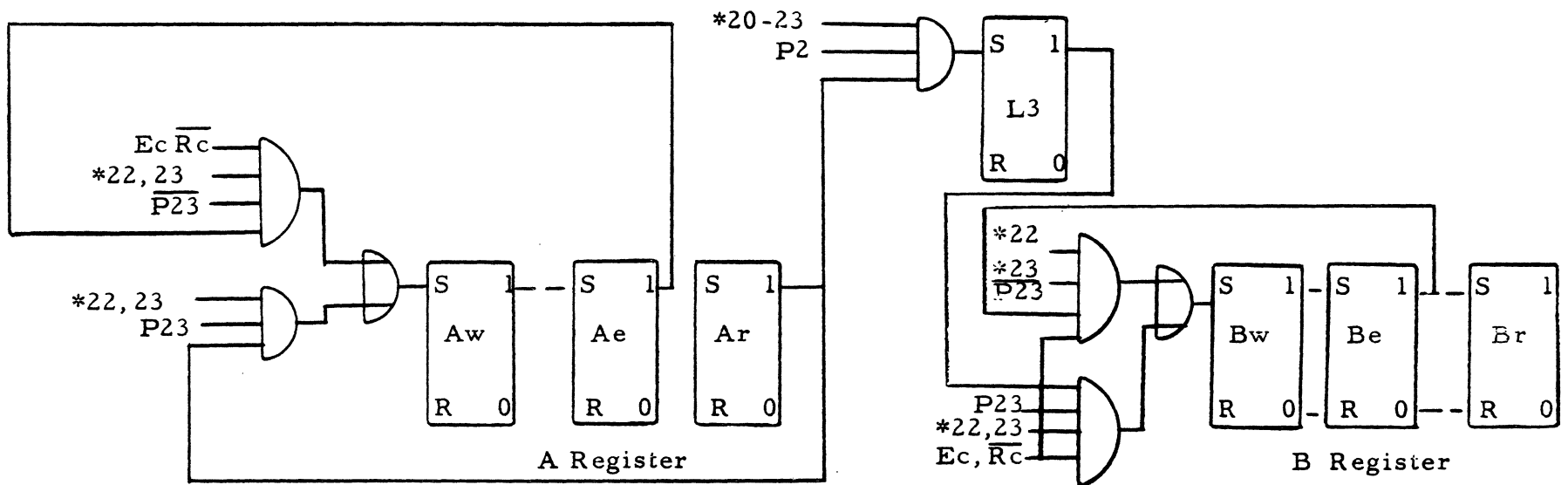


\*Commands

Figure 2-24. AB Shift Left Logic Diagram



2-57



\*Commands

Figure 2-25. AB Shift Right Logic Diagram

During left shifts the C register is incremented by "-1's," while during right shifts, the C register is incremented by "+1's" (see Figure 2-26).

$$\begin{aligned}
 sCw &= \text{---} + E_c \overline{R_c} O_5 \overline{O_4} Z_g + \text{---} \\
 X_g &= \text{---} + O_5 \overline{O_4} \overline{O_3} \overline{L_4} (\overline{O_2} + P_2) \\
 Y_g &= \text{---} + O_5 \overline{O_4} C_r \\
 rCa &= \text{---} + O_5 P_2
 \end{aligned}$$

All shift commands are terminated by the sector number of the command, except that shifting stops when the sign and most significant digit of A become different (command 20 is changed to 24), or when C becomes positive (command 23 is changed to 27).

$$\begin{aligned}
 sO_3 &= \text{---} + P_2 \overline{O_6} O_5 \overline{O_4} \overline{O_3} \overline{O_2} \overline{O_1} (A_w \overline{A_r} + \overline{A_w} A_r) \\
 &\quad + P_2 \overline{O_6} O_5 \overline{O_4} \overline{O_3} O_2 O_1 \overline{C_w} + \text{---}
 \end{aligned}$$

#### K. MISCELLANEOUS COMMANDS

The halt command, 00, is used to set the parity flip-flop, P<sub>c</sub>, during phase 3 (wait to execute).

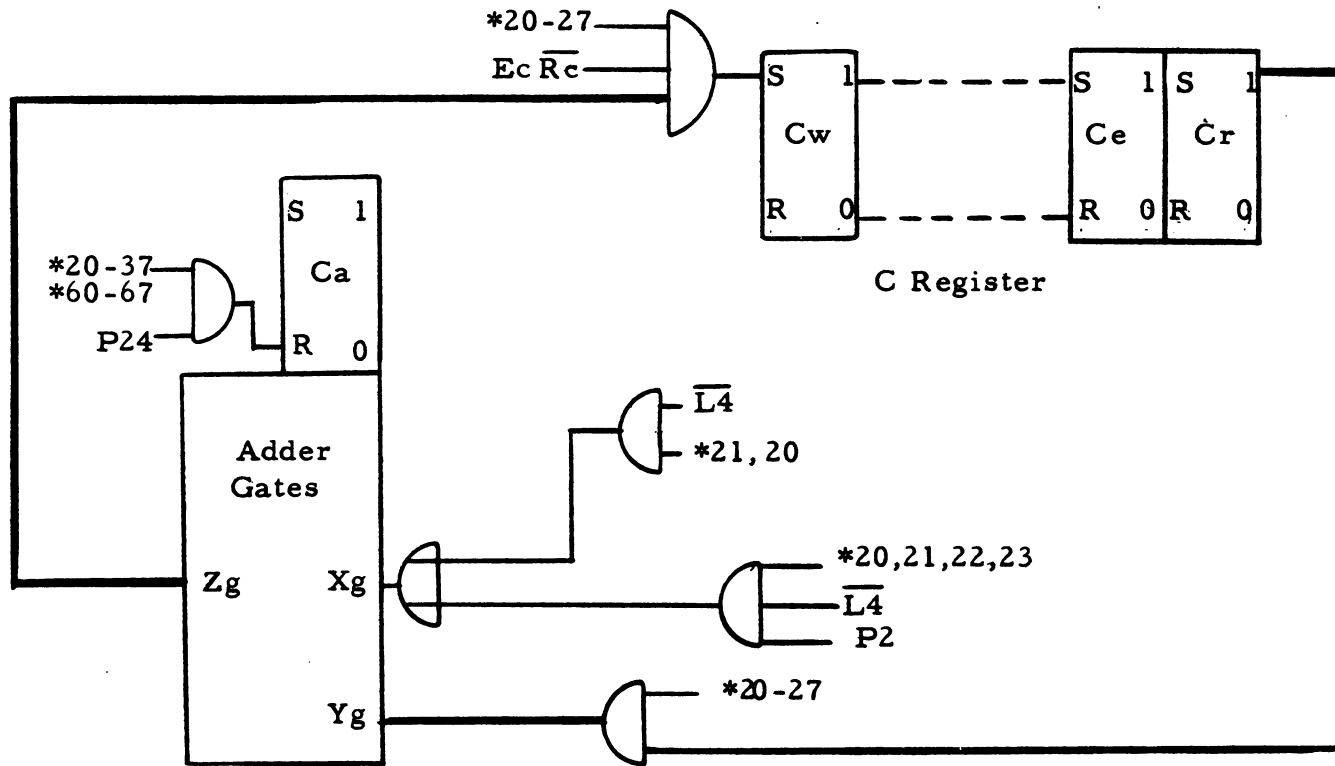
$$sP_c = \text{---} + E_c R_c \overline{O_6} \overline{O_5} \overline{O_4} \overline{O_3} \overline{O_2} \overline{O_1}$$

This locks the computer in phase 1 (wait to read next command), until the parity flip-flop is cleared with the BREAK POINT switch.

Command 26 is used to transfer data from the memory line to line 7.

$$\begin{aligned}
 sM_{7w} &= \text{---} + \overline{[M_{0g} N_{7g} W_g]} \left[ \overline{M_{7r}} (\overline{O_6} O_5 \overline{O_4} O_3 O_2 \overline{O_1} E_c) \right. \\
 &\quad \left. + (\overline{O_6} O_5 \overline{O_4} O_3 O_2 \overline{O_1} E_c) F_g \right] \\
 rM_{7w} &= \text{---} + \overline{[M_{0g} N_{7g} W_g]} \left[ \overline{M_{7r}} (\overline{O_6} O_5 \overline{O_4} O_3 O_2 \overline{O_1} E_c) \right. \\
 &\quad \left. + (\overline{O_6} O_5 \overline{O_4} O_3 O_2 \overline{O_1} E_c) \overline{F_g} \right]
 \end{aligned}$$

Command 40 extends the bit pattern in the A register where there are



\*Commands

Figure 2-26. Incrementing C Register Logic Diagram



corresponding "1's" in memory.

$$sAw = \text{---} + Ec \overline{Rc} O6 \overline{O5} \overline{O4} \overline{O3} \overline{O2} \overline{O1} Fg Aw + \text{---} \\ + Ar \left[ \overline{Ec} \overline{Rc} (O6 \overline{O5} \overline{O4} \overline{O3} \overline{O2} \overline{O1} Fg + \text{---}) \right]$$

Command 41 records the signal from the parity flip-flop, Pc, into the A register while Pc is generating the parity signal for the data in the A register.

$$Ig = \text{---} + \overline{P24} \overline{O6} \overline{O2} O1 Ar + \text{---} \\ sPc = Ec \overline{Rc} \overline{P1} \overline{O5} \overline{O3} Ig \overline{Pc} + \text{---} \\ rPc = Ec \overline{Rc} \overline{P1} \overline{O5} \overline{O3} Ig Pc + \text{---} \\ sAw = \text{---} + Ec \overline{Rc} O6 \overline{O5} \overline{O4} \overline{O3} \overline{O2} O1 Pc + \text{---}$$

Commands 42, 46, and 47 perform logical operations on the contents of the B register. For both command 42 and 46, the contents of the C register are gated into the B register where there are corresponding "1" bits in memory.

$$sBw = \text{---} + Ec \overline{Rc} O6 \overline{O5} \overline{O4} O2 \overline{O1} Fg Cr + \text{---}$$

For both commands 46 and 47, each B register bit is cleared where there is a corresponding "1" bit in memory.

$$sBw = \text{---} + \overline{P1} Br \left[ \overline{Ec} \overline{Rc} (O6 \overline{O5} \overline{O4} O3 O2 Fg + \text{---}) \right]$$

The remaining clearing terms for B are interpreted as follows:

$$sBw = \text{---} + \overline{P1} Br \left[ \overline{Ec} \overline{Rc} (\overline{O6} \overline{O5} O3 O2 + \overline{O6} O5 \overline{O3} + \text{---} + \overline{O5} \overline{O4} \overline{O3} O2) \right]$$

	↓	↓	↓
	06	20	02
Clear (B)	07	21	03
for these	16	22	42
commands	17	23	43
		30	
		31	
		32	
		33	

The clearing terms for the A register are as follows:

$$sAw = \dots + Ar \left[ \overline{Ec} \overline{Rc} (\overline{O5} \overline{O4} \overline{O2} O1 + \overline{O5} O4 O3 \overline{O2} + \overline{O6} O5 \overline{O3} \dots +) \right]$$

	↓	↓	↓
	01	14	20
Clear (A) for	05	15	21
these	41	54	22
commands.	45	55	23
			30
			31
			32
			33

The clearing terms for the C register are as follows:

$$sCw = \dots + \overline{P24} Cr \left[ \overline{Ec} \overline{Rc} (\overline{O5} \overline{O4} O3 \overline{O2} \overline{O1} + \overline{O6} \overline{O5} \overline{O4} \overline{O3} \dots +) \right]$$

	↓	↓
	04	00
Clear (C) for	44	01
these		02
commands.		03

	↓	↓
	20,60	30
	21,61	
	22,62	
Clear (C) for	23,63	
these	24,64	
commands.	25,65	
	26,66	
	27,67	

The justification for clearing the contents of these registers for the indicated commands can be found by referring to the command list in Table 2-1. In the case of the C register, the indicated clearing for commands 24, 25, 26, and 27 is prevented by recirculation through the adder.

$$sCw = \dots + \overline{Ec} \overline{Rc} O5 \overline{O4} Zg + \dots$$

$$Xg = \dots + O6 O5 \overline{O4} + O5 \overline{O4} \overline{O3} \overline{L4} (\overline{O2} + P2)$$

$$Yg = \dots + O5 \overline{O4} Cr$$

Command 56 is used to set the overflow flip-flop, Of, and then reset it if there is any difference between the A register and memory.

$$\begin{aligned} \text{sOf} &= \text{---} + \text{P24 Rc O6 } \overline{\text{O5}} \text{ O4 O3 O2 } \overline{\text{O1}} \\ \text{rOf} &= \text{---} + \overline{\text{P1}} \overline{\text{P24}} \text{ Ec } \overline{\text{Rc}} \text{ O6 } \overline{\text{O5}} \text{ O4 O3 O2 } \overline{\text{O1}} (\text{Fg } \overline{\text{Ar}} + \overline{\text{Fg}} \text{ Ar}) \end{aligned}$$

Command 70 generates a signal to pulse a unit external to the computer. The control pulse execution signal is as follows:

$$\text{Cpg} = \text{Ec O6 O5 O4 } \overline{\text{O3}} \overline{\text{O2}} \overline{\text{O1}}$$

The transmitted output code is taken from L1, L2, L3, L4, and L5.

Command 72 generates a serial output from the memory line. The format mask is taken from the same command line from which command 72 is read.

$$\begin{aligned} \text{Gsg} &= \text{Ec O6 O5 O4 } \overline{\text{O3}} \text{ O2 } \overline{\text{O1}} \text{ Vg } \overline{\text{P1}} \overline{\text{P24}} \\ \text{Gdg} &= \text{Fg} \end{aligned}$$

Command 73 provides a serial input to the memory line. The format mask is taken from the same command line from which command 73 is read.

$$\begin{aligned} \text{Hsg} &= \text{Ec O6 O5 O4 } \overline{\text{O3}} \text{ O2 O1 Vg } \overline{\text{P1}} \overline{\text{P24}} \\ \text{Ig} &= \text{---} + \overline{\text{P24}} \text{ O6 O5 O2 Vg Hdg } + \text{---} \end{aligned}$$

Command 77 is used for testing a number of external signals. The memory line number of the command is used to select 1 of 32 inputs.

$$\begin{aligned} \text{Jg} &= \text{M0g N0g } \textcircled{\text{J0}} + \text{---} + \text{M3g N0g } \textcircled{\text{J24}} \\ &+ \text{M0g N1g } \textcircled{\text{J1}} + \text{---} + \text{M3g N1g } \textcircled{\text{J25}} \\ &+ \text{---} \\ &+ \text{M0g N4g } \textcircled{\text{J4}} + \text{---} + \text{M3g N4g } \textcircled{\text{J28}} \\ &+ \text{M0g N5g } \textcircled{\text{J5}} + \text{---} + \text{M3g N5g } \textcircled{\text{Bp}} \\ &+ \text{M0g N6g } \textcircled{\text{J6}} + \text{---} + \text{M3g N6g } \overline{\text{Rf}} \overline{\text{Tf}} \\ &+ \text{M0g N7g } \textcircled{\text{J7}} + \text{---} + \text{M3g N7g } \textcircled{\text{Tb}} \end{aligned}$$

The  $\textcircled{J27}$  signal is connected to the magnetic tape clock signal,  $\textcircled{Uc}$  and the  $\textcircled{J28}$  signal is jumpered to the photo tape reader sprocket signal,  $\textcircled{Sc}$ .

#### L. INPUT AND OUTPUT

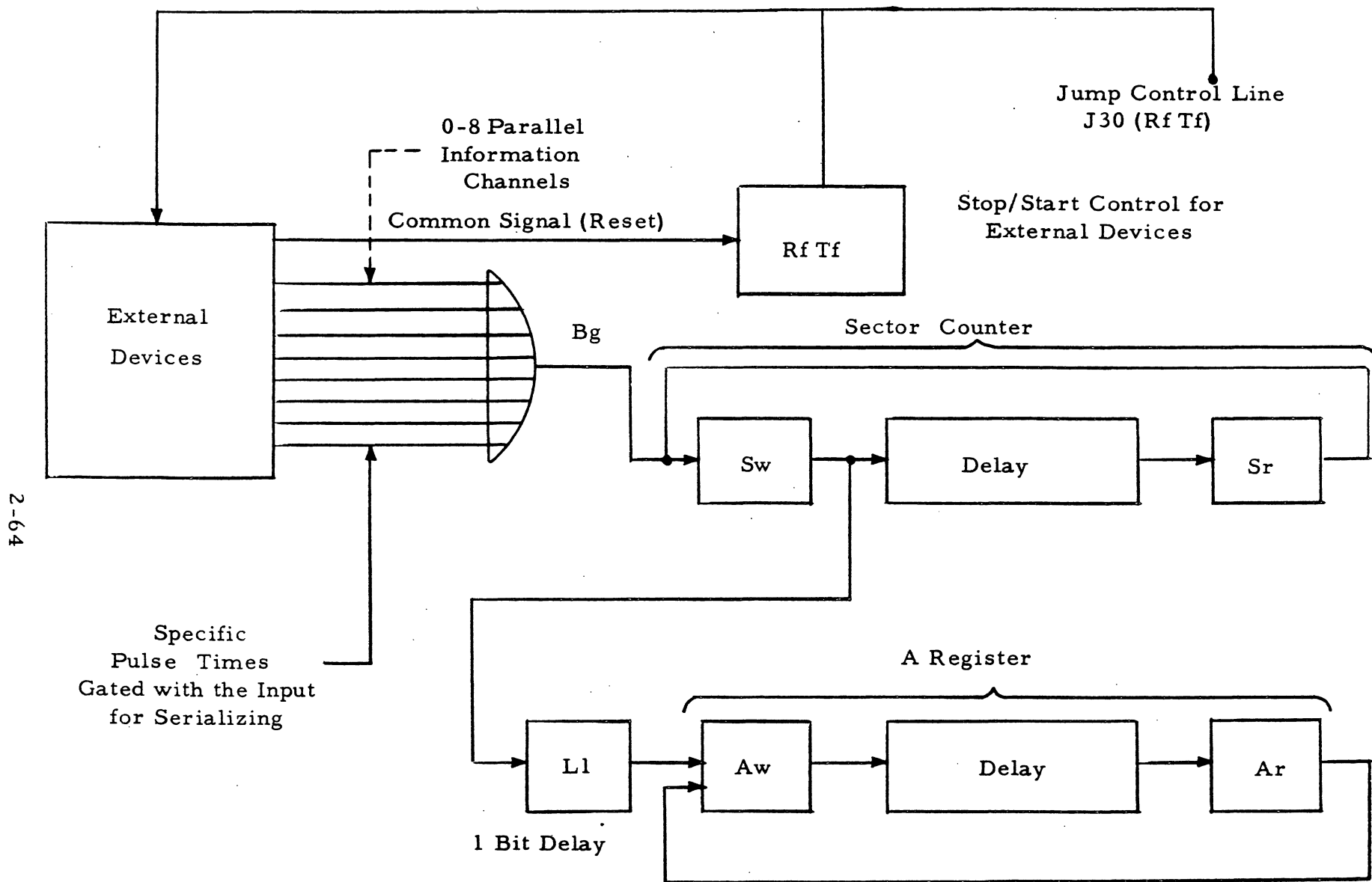
The input operation on the PB250 is shown in Figure 2-27. Input and output is handled on an individual character basis. Each 8-bit input character is entered into the buffer section of the sector counter. Each 8-bit output character is transmitted by a character output command and is presented by the operand line selector register flip-flops, L5, L4, L3, L2, and L1, and the operation code register flip-flops, O3, O2, and O1.

For character input control, the Rf and Tf flip-flops are controlled by commands 50, 51, 52, and 53.

$$\begin{aligned} sRf &= Ec O6 \overline{O5} O4 \overline{O3} O2 + - - - \\ rRf &= Ec O6 \overline{O5} O4 \overline{O3} \overline{O2} + - - - \\ sTf &= Ec O6 \overline{O5} O4 \overline{O3} O1 \\ rTf &= Ec O6 \overline{O5} O4 \overline{O3} \overline{O1} + - - - \end{aligned}$$

The function of these flip-flops is to control the input devices. The condition  $Rf \overline{Tf}$  is used to energize the reader release magnet, LR, and to energize the reader contacts return. The condition  $\overline{Rf} Tf$  is used to energize the "type light" and the typewriter contacts return. A gate line for the fast readers is energized by the condition  $Rf Tf$ . The signals from the reader common,  $\textcircled{Rc}$  and the signals from the typewriter common,  $\textcircled{Tc}$ , are used to reset Rf and Tf, respectively.

$$\begin{aligned} rRf &= - - - + \textcircled{Fi} \textcircled{Mr} (P8 - P15) + \textcircled{Rc} \overline{Ec} \\ rTf &= - - - + \textcircled{Tc} Ec \dagger \textcircled{Fi} (P8 - P15) \end{aligned}$$



2-64

Figure 2-27. Buffer Input

The input code signals are

(R1), (R2), (R3), (R4), (R5), (R6), (R7), and (R8) from the mechanical tape reader,

(T1), (T2), (T3), (T4), (T5), and (T6), from the typewriter.

(S1), (S2), (S3), (S4), (S5), (S6), (S7), and (S8) from the photo tape reader.

(U1), (U2), (U3), (U4), (U5), (U6), (U7), and (U8) from the magnetic tape reader.

These parallel codes are serialized in pulse positions P24, P1, P2 - - - P6, and P7, and entered into the buffer section of the sector counter.

$$\begin{aligned}
 Bg &= P24 \left( (R1) + (S1) + (T1) + (U1) \right) \\
 &+ P1 \left( (R2) + (S2) + (T2) + (U2) \right) \\
 &+ P2 \left( (R3) + (S3) + (T3) + (U3) \right) \\
 &+ P3 \left( (R4) + (S4) + (T4) + (U4) \right) \\
 &+ (P24-P7) F3 \overline{F2} \overline{F1} \left( (R5) + (S5) + (T5) + (U5) \right) \\
 &+ (P24-P7) F3 \overline{F2} F1 \left( (R6) + (S6) + (T6) + (U6) \right) \\
 &+ (P24-P7) F3 F2 \overline{F1} \left( (R7) + (S7) + (U7) \right) \\
 &+ (P24-P7) F3 F2 F1 \left( (R8) + (S8) + (U8) \right)
 \end{aligned}$$

$$sSw = - - - + Bg \overline{Qg}$$

$$rSw = - - - + \overline{Sc} \overline{Sr} \overline{Bg} + Qg \overline{Bg}$$

Each eight-bit code from the mechanical tape reader and from the typewriter is entered into the buffer before the corresponding common signal sets the condition  $\overline{Rf} \overline{Tf}$ . This entry is made for the "1's" of the code to prevent dropouts due to contact chatter. When the state  $\overline{Rf} \overline{Tf}$  is set, the reader and typewriter contact returns are deenergized to terminate the input signals to the buffer. The code is then cleared from the buffer and loaded into the A register with command 55.

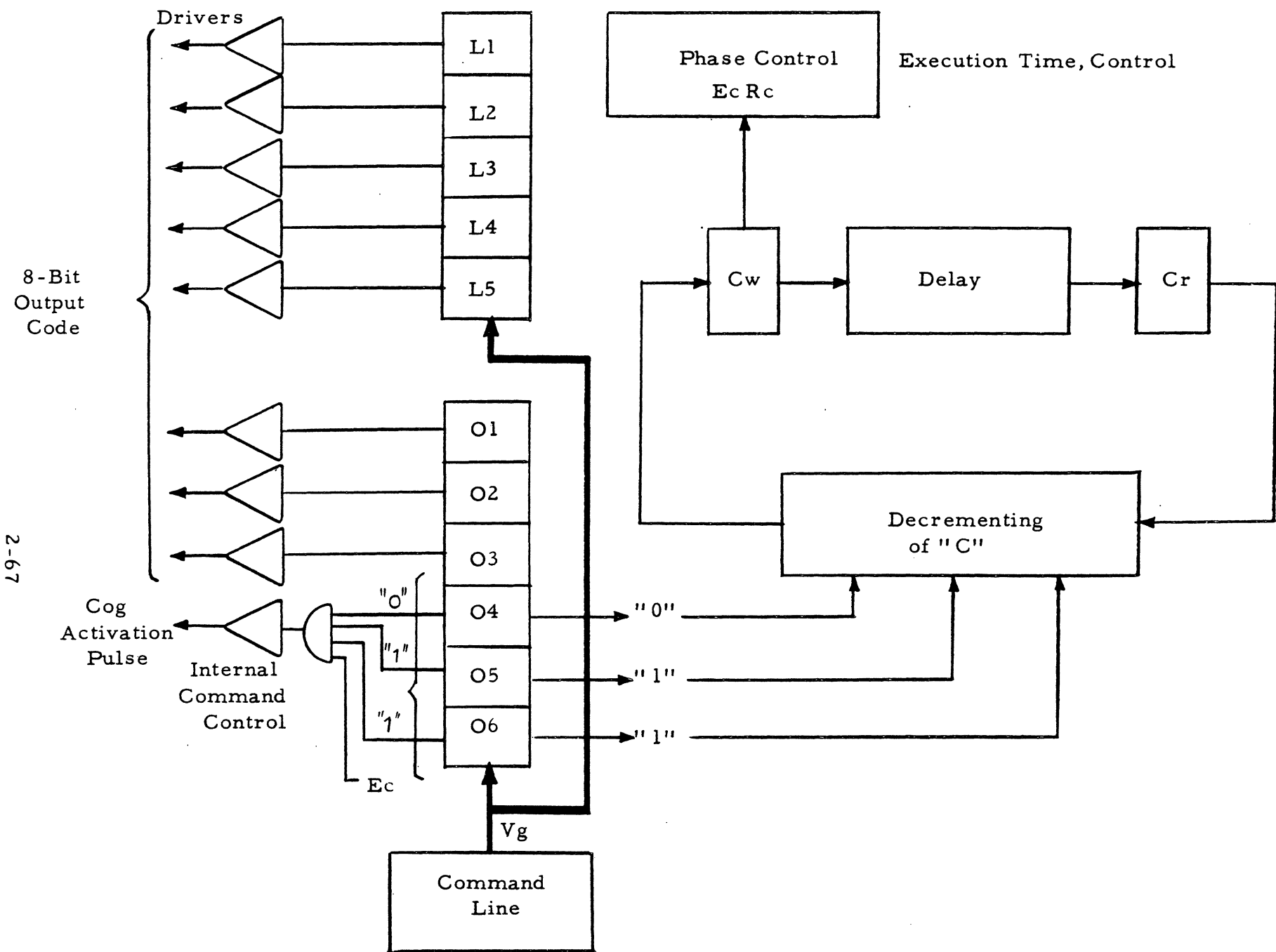
$$\begin{aligned}
Qg &= \overline{Ec} O6 \overline{O5} O4 O3 O1 \overline{P24} (P24-P7) + \dots \\
&\quad + Ec \overline{Rc} O6 \overline{O5} O4 O3 O1 P24 \\
sSw &= \dots + \overline{Sc} Sr \overline{Qg} + \dots \\
rSw &= \dots + Qg \overline{Bg} \\
sL1 &= \dots + O6 \overline{O5} O4 \overline{O2} Ec Sw \\
rL1 &= \dots + O6 \overline{O5} O4 \overline{O2} Ec \overline{Sw} \\
sAw &= \dots + Ec \overline{Rc} O6 \overline{O5} O4 O3 \overline{O2} O1 (L1 Vg + Ar \overline{Vg}) + \dots
\end{aligned}$$

## 2-9. BUFFER CLEARING

The bits from the buffer are delayed through Sw and L1 flip-flops to place the first code bit in P2 of the A register. The number of code bits entered into the A register is controlled by a format word in the command line and by the L1 Vg term. The Ar  $\overline{Vg}$  term preserves the balance of the A register. For the buffer clearing term, Qg, the P24 position is cleared as the command is executed, while positions P1 through P7 are cleared in the first sector after execution. This first sector after execution may be phase 1 or phase 2; therefore O2 which changes at P2 of phase 2, must be omitted from the clearing term. This requirement results in command 57 being a buffer clearing command also.

If commands 51 or 52 are repeated while the input contacts are still closed, the same input code will be entered into the buffer and the same common contact signal will again reset the condition  $\overline{Rf} \overline{Tf}$ . In the case of fast tape readers, the computer program must phase the use of commands 55 and 57, based on sensing an input clock signal with command 77.

The output operation of the PB 250 is shown in Figure 2-28. An 8-bit character output code is presented by O3, O2, O1, L5, L4, L3, L2, and L1 when commands 60 through 67 are executed. The destination is coded by



2-67

Figure 2-28. Character Output Operation



the command line selector register flip-flops, K3, K2, K1. The output character execute signal is Cog.

$$\text{Cog} = \text{Ec O6 O5 } \overline{\text{O4}}$$

The duration of execution of a character output command is controlled by decreasing a control number in the C register by one count for each sector of execution.

$$\begin{aligned} \text{Xg} &= \text{---} + \text{O6 O5 } \overline{\text{O4}} + \text{---} \\ \text{Yg} &= \text{---} + \text{O5 } \overline{\text{O4}} \text{ Cr} \\ \text{sCw} &= \text{---} + \text{Ec } \overline{\text{Rc}} \text{ O5 } \overline{\text{O4}} \text{ Zg} + \text{---} \end{aligned}$$

While the register remains positive, the Is flip-flop is prevented from indicating a sector comparison to terminate phase 4.

$$\text{rIs} = \text{---} + \text{P23 Ec Rc O6 O5 } \overline{\text{O4}} \overline{\text{Cr}}$$

If the C register starts with a large positive number, the execution phase may extend to 25 seconds. If the C register is zero or negative, the execution duration will be controlled entirely by the memory sector number of the command

The "type output character" and "punch output character" execute signals are provided as follows:

$$\begin{aligned} \text{Tg} &= \text{Ec O6 O5 } \overline{\text{O4}} \text{ K3 } \overline{\text{K2}} \text{ K1} \\ \text{Pg} &= \text{Ec O6 O5 } \overline{\text{O4}} \text{ K3 K2 } \overline{\text{K1}} \end{aligned}$$

The code selector signals are also provided for the typewriter and punch.

LT1 = L1 Tg  
 LT2 = L2 Tg  
 LT3 = L3 Tg  
 LT4 = L4 Tg  
 LT5 = L5 Tg  
 LT6 = O1 Tg

LP1 = L1 Pg  
 LP2 = L2 Pg  
 LP3 = L3 Pg  
 LP4 = L4 Pg  
 LP5 = L5 Pg  
 LP6 = O1 Pg  
 LP7 = O2 Pg  
 LP8 = O3 Pg

M. BOOTSTRAP INPUT

Figure 2-29 illustrates the bootstrap input. Bootstrap is an input means for loading line 01 from a special tape without the use of a program in the computer. The special tape format is indicated as follows:

(B6)	(B5)	(B4)	(B3)	(B2)	(B1)	
1	0	1	1	1	0	Carriage Return
1	0	0	0	0	0	Zero for 0's
1	0	1	0	0	0	H for 1's
0	1	0	0	0	0	Space Code
0	0	1	0	1	1	Stop Code
0	0	0	0	0	0	Feed Code
C	C	"1"				S
O	O					T
M	M					O
M	M					P
O	O					
N	N					

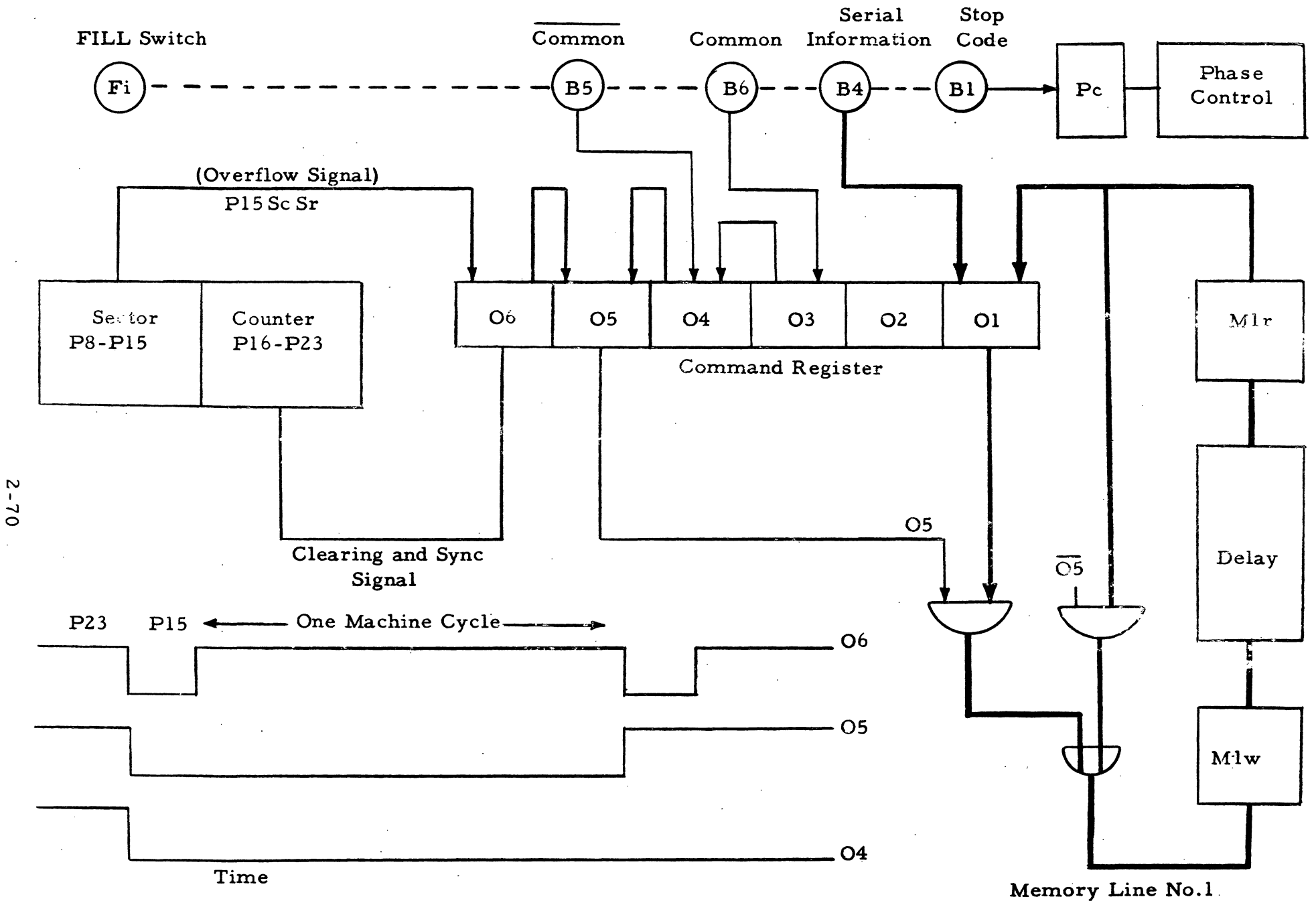


Figure 2-29. Bootstrap Input

2-70

Channel 4 provides the binary input data, while channel 1 provides the stop code. In the case of a photo tape reader or a magnetic tape reader, channel 6 provides an input common signal and channel 5 provides an input common signal. These signals are provided by  $\textcircled{Rc}$  and  $\textcircled{\overline{Rc}}$  in the case of a mechanical reader.

The input is started by closing the FILL switch and resetting the parity flip-flop if it is set. If a mechanical reader is used,  $\textcircled{Mr}$  is "true" and  $Rf \overline{Tf}$  is set to release the reader. Otherwise,  $Rf \overline{Tf}$  is set.

$$\begin{aligned} sRf &= \text{---} + \textcircled{Fi} \overline{Pc} (P8-P15) \textcircled{Mr} \\ rRf &= \text{---} + \textcircled{Fi} \textcircled{\overline{Mr}} (P8-P15) + \textcircled{Rc} \overline{Ec} \\ rTf &= \text{---} + \textcircled{Fi} (P8-P15) \end{aligned}$$

To start a photo tape reader or a magnetic tape reader, start and stop signals are generated from the parity flip-flop.

$$\begin{aligned} \text{BootstrapStart} &= \textcircled{Fi} \overline{Pc} \\ \text{BootstrapStop} &= \textcircled{Fi} Pc \end{aligned}$$

The input process is stopped by setting the parity flip-flop as soon as the first "1" bit in channel 1 is detected.

$$sPc = \text{---} + \textcircled{Fi} \textcircled{B1} + \text{---}$$

While the FILL switch is depressed, computation is blocked by the  $\textcircled{\overline{Fi}}$  term in  $sRc$ . When the FILL switch is released, computation will still be blocked by the  $\overline{Ec} Rc Pc P1$  term of  $rRc$ . If it is necessary to put a new tape in the reader, the "I" key of the typewriter must be depressed while the ENABLE switch is depressed, to allow computation to start at memory word zero. At this time the BREAK POINT switch can be depressed to reset the  $Pc$  flip-flop.

While the bootstrap input is in operation, each "common" signal is

detected by the O3 flip-flop. The "common" signal that follows is then detected by the O4 flip-flop.

$$sO3 = - - - + \textcircled{Fi} \textcircled{B6}$$

$$sO4 = - - - + \textcircled{Fi} \textcircled{B5} \overline{O4} O3$$

After O4 is set, O5 is set for one machine cycle, synchronized by O6; then O3, O4, and O5 are reset simultaneously.

$$sO5 = - - - + \textcircled{Fi} P23 O6 \overline{O5} O4$$

$$rO5 = - - - + \textcircled{Fi} P23 O6 O5$$

$$rO4 = - - - + \textcircled{Fi} P23 O6 O5 + - - -$$

$$rO3 = - - - + \textcircled{Fi} P23 O6 O5$$

$$sO6 = - - - + \textcircled{Fi} F4 F3 F2 F1 Sr Sc$$

$$rO6 = \textcircled{Fi} P23 + - - -$$

While the "common" signals are detected by O3, the "1" bits in channel 4 are entered into the O1 flip-flop.

$$sO1 = - - - + \textcircled{Fi} \textcircled{B4} \overline{O5} + - - -$$

$$rO1 = - - - + \textcircled{Fi} \overline{O3} + - - -$$

Before each input character, O1 is cleared by the  $\textcircled{Fi} \overline{O3}$  term.

With the FILL switch depressed, O6 is set once per machine cycle when all "1's" are read in Sr during the interval (P8-P15). This marks each machine cycle and serves to synchronize the second number in the sector counter.

$$Qg = - - - + \textcircled{Fi} O6 + - - -$$

While O5 is set, the contents of line O1 are shifted by one bit through the O1 flip-flop. This enters each bit from the O1 flip-flop into line O1.

$$\begin{aligned}
sO1 &= - - - + \textcircled{Fi} \ O5 \ M1r \\
rO1 &= - - - + \textcircled{Fi} \ O5 \ \overline{M1r} \\
sM1w &= - - - + [M0g \ N1g \ Wg] [M1r \ (\overline{\textcircled{Fi} \ O5})] + \textcircled{Fi} \ O5 \ O1 \\
rM1w &= - - - + [M0g \ N1g \ Wg] [\overline{M1r} \ (\textcircled{Fi} \ O5)] + \textcircled{Fi} \ O5 \ \overline{O1}
\end{aligned}$$

The following chart indicates signal sources for various readers.

	$\textcircled{B6}$	$\textcircled{B5}$	$\textcircled{B4}$	$\textcircled{B1}$	$\textcircled{Mr}$
Mechanical Reader	$\textcircled{Rc}$	$\textcircled{Rc}$	$\textcircled{R4}$	$\textcircled{R1}$	1
Photo Reader	$\textcircled{S6}$	$\textcircled{S5}$	$\textcircled{S4}$	$\textcircled{S1}$	0
Mag. Tape Reader	$\textcircled{U6}$	$\textcircled{U5}$	$\textcircled{U4}$	$\textcircled{U1}$	0

The Bootstrap input connector selects the source of  $\textcircled{B6}$ ,  $\textcircled{B5}$ ,  $\textcircled{B4}$ ,  $\textcircled{B1}$ , and  $\textcircled{Mr}$ .

The input bits are entered at P24 of word  $(376)_8$  of line 01 and precess into words  $(377)_8$ , 00, 01, 02, 03, etc. The input rate is limited by the rate of precessing bits into line 01. A tape for use with the mechanical reader should be prepared as follows:

0 0 0 0 H 0 0 H 0 0 0 0 0 0 0 0 0 H H 0 0 0 0 0	C	←	for 01-001
H 0 0 0 0 0 0 0 0 H 0 0 0 0 H H 0 0 0 0 0 0 0	C	←	for 01-000
0 0	C	←	for 01-255
0	S	←	for 01-254
	T		

A tape for use with the photo reader should be prepared as in the preceding example, but with two-space codes before each code shown. A magnetic tape for use as a bootstrap should have 14-space codes between each code shown. These space codes are to allow two machine cycles between input characters.

## N. MAGNETIC TAPE

With six bits per character and three or four characters per word, a 2 kc input rate can result in an input rate as high as 667 words per second, or two words per machine cycle. The program presented here allows for this rate, with blocks of up to 272 words or 816 characters. The end-of-block will be detected by the tape handler, using either code or gap detection.

The program assembles words in the A register with LSD commands, assembles 16-word groups in L0 with IAM commands, and precesses the 16-word groups into L4 through a 16-word buffer register, L15, with DUMP operations. The first group is precessed into memory locations 04-255 through 04-014, then into memory locations 04-015 through 04-030, etc.

The input program is a cyclic set of 16 commands in one line. The tape reader is started by a PTU command and control is immediately switched to the input program. While waiting for input characters, the program tests the input clock every 192  $\mu$ sec. When a character is detected, it is transferred to the A register and shifted left. If the character completes a word in the A register, the shift is replaced by an IAM transfer to L0. When a clock signal is detected, the input clock is tested after 384  $\mu$ sec rather than 192  $\mu$ sec. This limits the signal width between 232  $\mu$ sec and 384  $\mu$ sec, and the peak input rate is limited to 2600 characters per second.

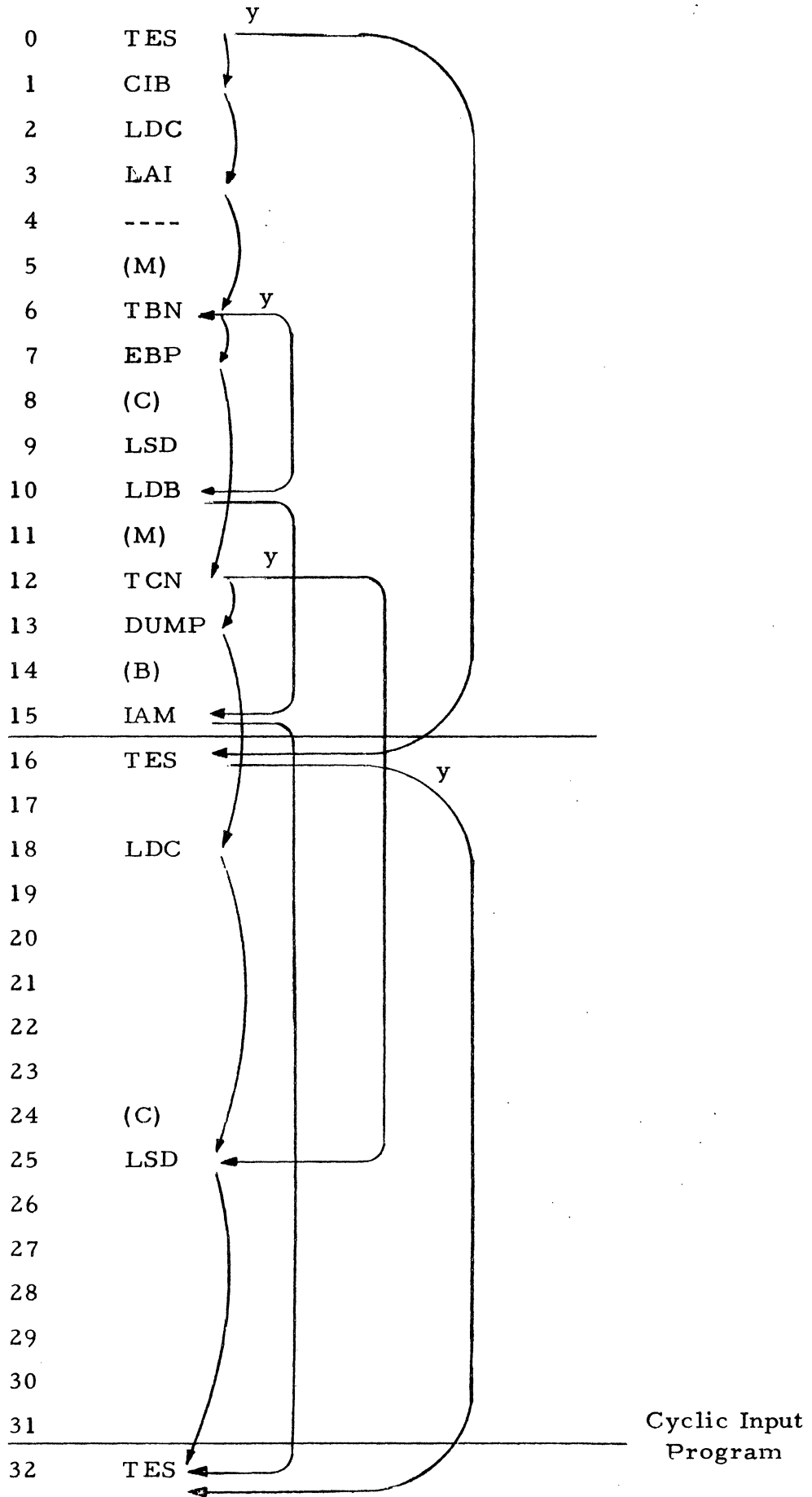
The detailed commands are listed in Table 2-3.

Table 2-3.

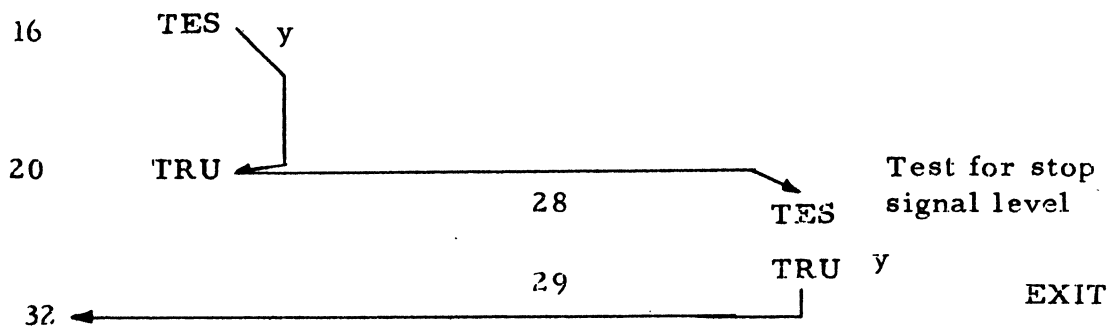
MAGNETIC TAPE INPUT COMMAND LIST

Word	Command	Function
0	TES	Tests input clock. "No" equals an input signal.
1	CIB	Clears input buffer immediately before each character is accepted.
3	LAI	Loads input character.
5	(M)	Input mask for LAI.
6	TBN	Tests for a "one-bit" shifted into sign of B register to indicate completed word in A register.
7	EBP	Stretches bit into sign position of A register.
11	(M)	Mask for EBP.
10	LDB	Restores B register after each word is formed in A register.
14	(B)	Marker bit for B register.
15	IAM	Precesses A register into L0 for 16 sectors.
12	TCN	Tests for completion of 16 new words in L0. C register starts out negative and counts down to positive with LSD commands.
13	DUMP	Starts transfer of 16 words in L0 to long line 04.
2	LDC	Restores count to C register after each 16 words in L0.
8	(C)	Number for LDC.
9	LSD	Shifts A register left. The LSD command may be placed in position 10 and LDB in position 9 for 5-bit input.



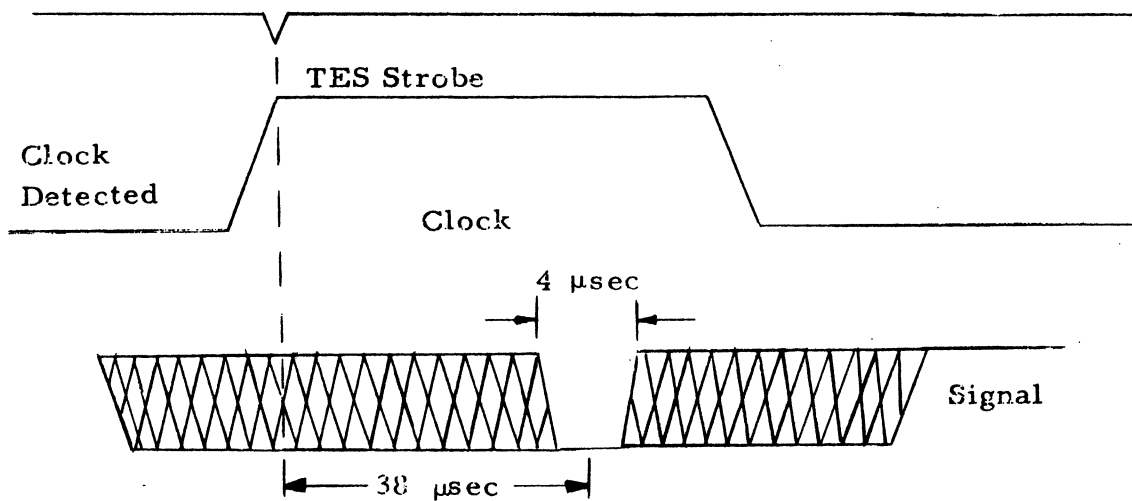


The program exit is not indicated. The tape handler detects its own end-of-block and signals the computer with a dc level. One 16-word program block can branch out to another command line to test for the stop signal. For example:

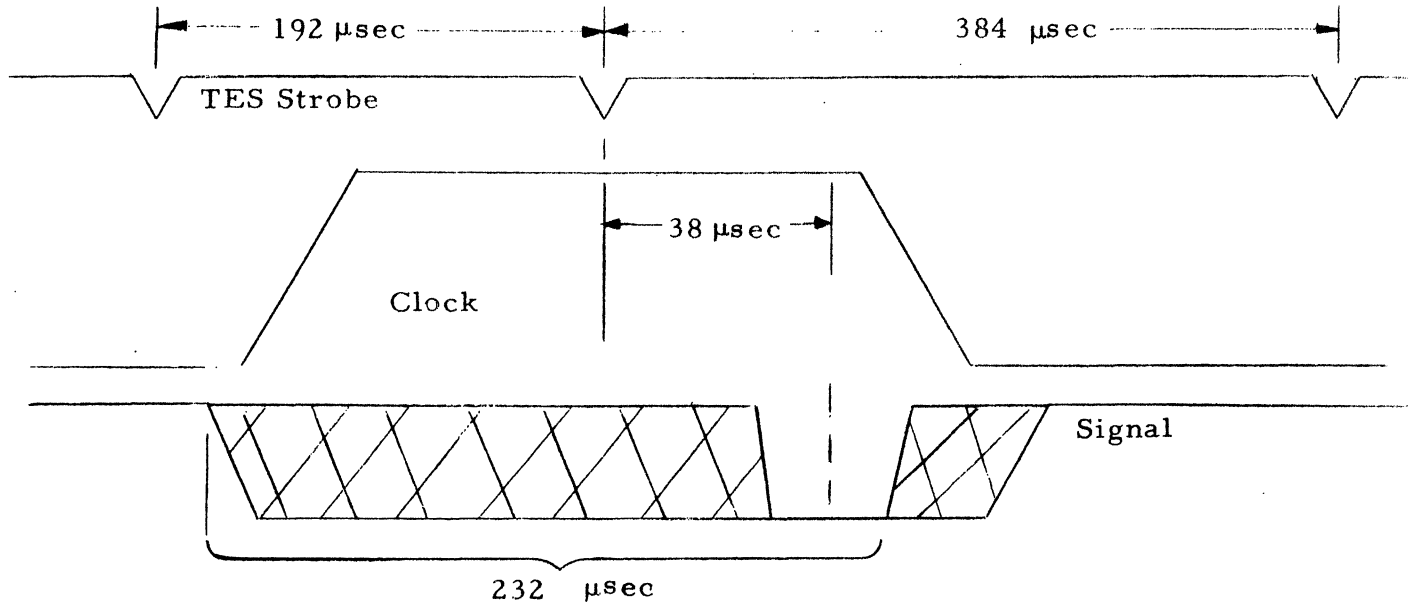


#### 2-10. SIGNAL TOLERANCES

The input signals are accepted following the detection of a clock signal. This allows a tape skew of up to 36  $\mu$ sec, i. e., a signal need not occur until 36  $\mu$ sec following the clock.



The minimum duration of signals is also influenced by this 38  $\mu$ sec, i. e., each signal must be present from 36  $\mu$ sec following the clock to 232  $\mu$ sec following the clock.



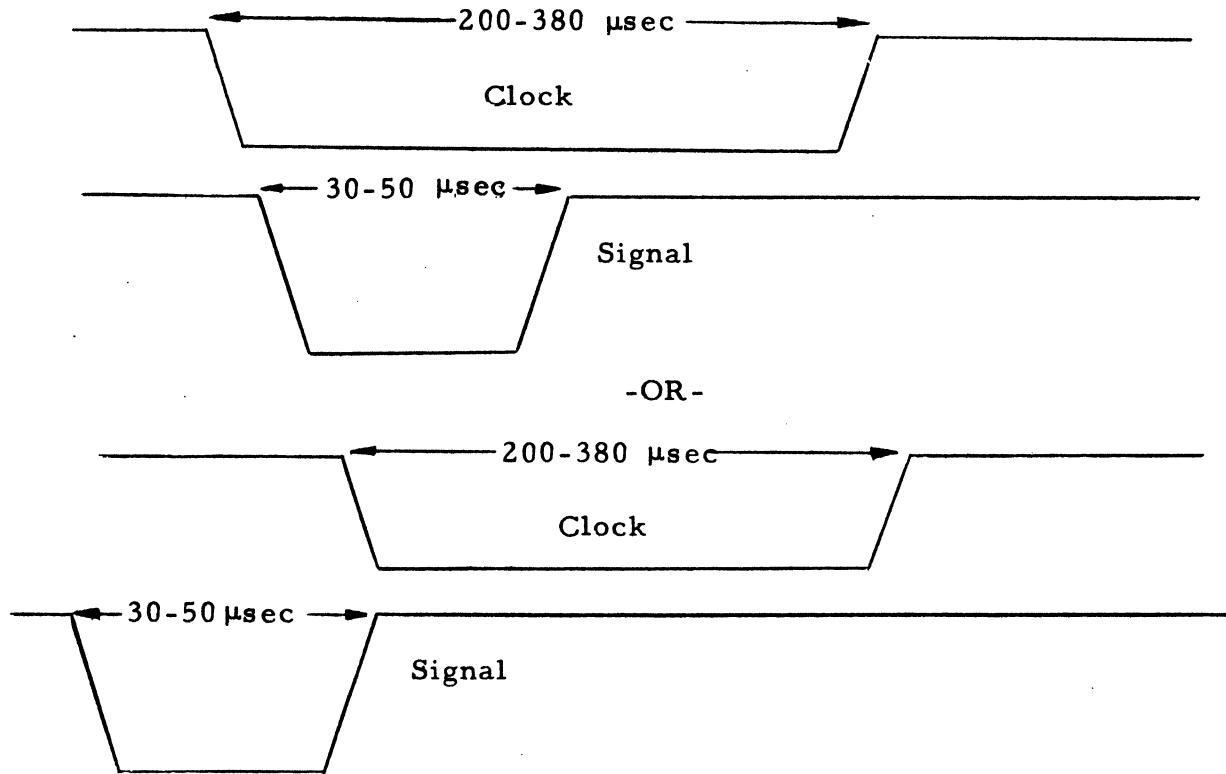
The DUMP command is a PTU command with an assigned line number. It sets in motion a sequence of data handling operations. The phases of operation are controlled by flip-flops.

Phase 2	Phase 1	
0	0	Idle, wait for DUMP command.
0	1	During IAM to L0, send shifted data from L0 → L15 and send data from L15 → L0.
1	1	Idle and wait for start of machine cycle.
1	0	Precess L4 through L15 for one machine cycle.

The DUMP command is useful for taking data from L4 for recording on magnetic tape as well as storing data in L4 when reading from magnetic tape.

## 2-11. ALTERNATE PROGRAMS

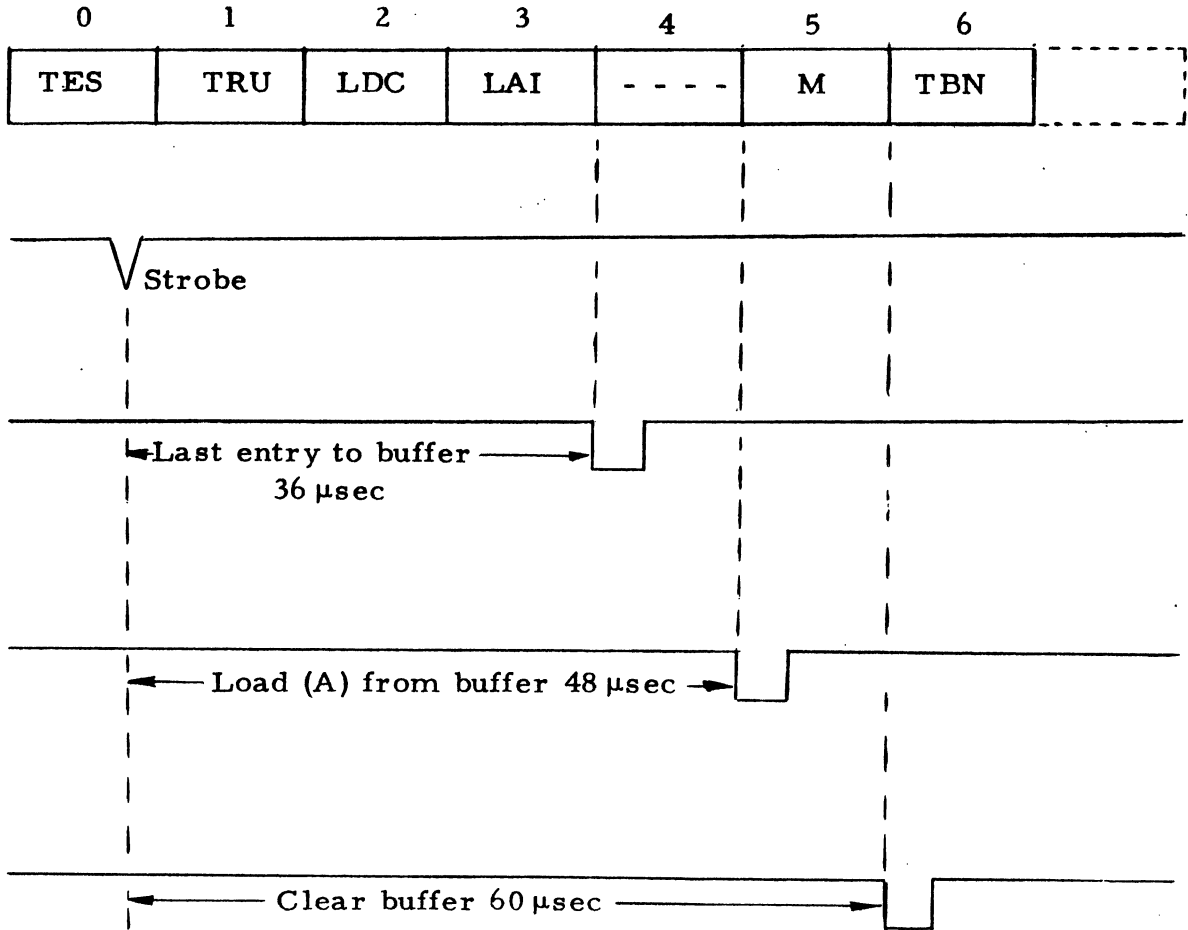
If the input signals are different, the input program may require some alteration. Two other possible input signals are shown below.



For the two types of signals shown above, the following program can be used. The LAI command clears the buffer.

0	TES	↘	y
1	TRU	↘	
2	LDC	↘	
3	LAI	↘	
4	----	↘	
5	(M)	↘	
6	TBN	↘	
	etc.	↘	

The timing of the preceding program is as follows:



## A. DESCRIPTION OF NOTATION

$$\left[ \begin{array}{l} \text{sF2} \\ \text{F2} \\ \text{rF2} \end{array} \right. \quad \begin{array}{l} = \overline{\text{F2}} \text{ F1} \\ \\ = \text{F2} \text{ F1} \end{array}$$

This notation signifies a high frequency flip-flop, F2, with its set input identified by sF2 and its reset input identified by rF2. The set and reset inputs have clock input signals implied.

$$\left[ \text{Lg} \right. \quad = \overline{\text{Ec} + \overline{\text{Rc}} + \text{F5} + \text{F4} \text{ F3} + \text{F4} \text{ F2} + \text{F4} \text{ F1} + \text{P24}_3 + \text{P1}}$$

This notation signifies a high frequency gate signal generated through an inverter for flip-flop input gates. No clock input signal is involved.

$$\left[ \text{N0g} \right. \quad = \overline{\text{L3}} \overline{\text{L2}} \overline{\text{L1}}$$

This notation signifies a low frequency gate signal generated with emitter followers. No clock input signal is involved.

$$\left[ \begin{array}{l} \text{Vg} \\ \overline{\text{Vg}} \end{array} \right. \quad \begin{array}{l} = \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \overline{\text{K1}} \text{ M0r} + \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \text{ K1} \text{ M1r} + \dots \\ = (\overline{\text{Vg}}) \end{array}$$

This notation signifies a high frequency gate signal pair generated through a double inverter.

$$\left[ \begin{array}{l} \text{slr} \\ \text{rlr} \end{array} \right. \begin{array}{l} = (\text{Iw delayed by 22 pulse times}) \\ = \overline{(\text{Iw delayed by 22 pulse times})} \end{array}$$

$$\left[ \begin{array}{l} \text{slw} \\ \text{rlw} \end{array} \right. \begin{array}{l} = \overline{\text{Ec}} \text{ Rc (P16-P23) Vg + - - - + Ir} \left[ \overline{\text{Ec}} \text{ Rc (P16-P23) + - -} \right] \\ = \overline{(\text{sIw})} \end{array}$$

These notations signify a flip-flop, Ir, that receives set and reset inputs from another flip-flop, Iw, through a 22 pulse-time delay time. The clock, as shown before, is implied for these high frequency flip-flops.

$$\left[ \begin{array}{l} \text{LTc} \\ \text{LT1} \\ \text{LT2} \\ \text{LT6} \end{array} \right. \begin{array}{l} = \text{Tg} \\ = \text{L1 Tg} \\ = \text{L2 Tg} \\ = \text{O1 Tg} \end{array}$$

These notations signify power driver output stages which operate magnet coils that are returned to -48v. No clock is used.

(A), (B), (C)

These notations signify, respectively, the contents of the A Register, the contents of the B Register, and the contents of the C Register.

## B. GLOSSARY OF TERMS

Ae, Ar, Aw:	A register flip-flops, early, read, write.
(B6), (B5), (B4), (B1):	Bootstrap input character signals.
Be, Br, Bw:	B register flip-flops, early, read, write.
(Bp):	BREAK POINT switch.
Bg:	Eight-bit character scanning buffer gate.
Ce, Cr, Cw:	C register flip-flops, early, read, write.
Ca:	Adder carry flip-flop.
Cog:	Output character gate signal (Commands 60-67).
Cpg:	Control pulse output signal for command 70.
Dg:	Denominator gate signal.
Ec:	Control flip-flop indicating waiting to execute or execute command.
Eg:	End of execute gate.
(En):	ENABLE switch signal.
F5, F4, F3, F2, F1:	Pulse-time counter flip-flops.
Fg:	"Fetch" gate information from line selected by L5, L4, L3, L2, L1.
(F):	FILL switch signal.
Fxg:	"Fetch" gate information, from lines 16 and higher in accessory memory expansion.
Gdg:	Output data signal for command 72.
Gsg:	Output shift signal for command 72.



Hdg:	Input data signal for command 73.
Hsg:	Input shift signal for command 73.
Ig:	Information gate signal from (A), (B), (C), Vg, Hdg, and parity.
Ir, Iw:	Instruction register flip-flops, read, write.
Is:	Instruction and sector registers comparison flip-flop.
(J28) -- (J0):	Branch control input signals.
Jg:	Branch control input selector gate signal.
K3, K2, K1; k4:	Command line selector register flip-flops.
Kg:	Command line register gate signal.
L5, L4, L3, L2, L1:	Operand line selector register flip-flops.
Lg:	Operand line selector register shift signal.
LP1, LP2, --- LP8:	Punch code magnet signals.
LPC:	Punch clutch magnet signal.
LR:	Reader release magnet.
LT1, LT2, ---LT6:	Typewriter translator code magnet signals.
LTC:	Typewriter translator clutch magnet signal.
M3g, M2g, M1g, M0g:	Line selector signals decoded from L5 and L4.
M0r, M1r --- :	Memory line read flip-flops.
M0w, M1w, --- :	Memory line write flip-flops.
(Mr) (Mr):	Mechanical reader bootstrap input control levels.
N7g, -- N0g:	Line selector signals decoded from L3, L2 and L1.
Oc, O6, O5, O4, O3, O2, O1:	Operation code register flip-flops.
Of:	Overflow flip-flop.
Og:	Operation code register shift signal.
P1, P2, P3, P23, P24:	Pulse times decoded from F5, F4, F3, F2, F1.

(P24-P7) (P8-P15) (P16-P23):	Pulse time intervals decoded from F5, F4, F3, F2, F1.
Pc:	Parity check flip-flop.
Pg:	Punch gate signal (commands 60-67 command line 6).
Qg:	Clear signal for input character buffer.
(R8) -- (R1):	Eight-bit character signals from mechanical reader.
(Rc):	Reader common signal.
Rc:	Control flip-flop indicating read command or wait to execute.
Rf:	Input control flip-flop, indicates reader input.
(S8) -- (S1):	Eight-bit character input signals (photo reader).
Sc:	Carry flip-flop for sector counter register.
Sr, Sw:	Sector counter register flip-flops, read, write.
(T6) -- (T1):	Six-bit typewriter character signals.
(Tb):	Typewriter busy signal.
(Tc):	Typewriter common signal.
Tf:	Input control flip-flop, indicating typewriter input or fast reader input.
Tg:	Typewriter gate signal (Commands 60-67 command line 5).
(U8) -- (U1):	Eight-bit character input signals (magnetic tape reader).
Vg:	Next command gate signal, selected by K3, K2, K1, K4.
Wg:	Gate signal for the control of writing into the memory.
Xg:	Input term for adder (addend).

**Yg:** Input term for adder (augend).  
**Zg:** Adder output signal.

## C. COMPLETE LOGICAL EQUATIONS

### C-1. PULSE AND SECTOR COUNTERS

$\left[ \begin{array}{l} \text{F1} \\ \text{F1} \end{array} \right.$	$\text{sF1} = \overline{\text{F1}} (\overline{\text{F5}} \text{F5} + \overline{\text{F5}} \overline{\text{F5}}) *$	$\text{rF1} = \text{F1}$	$\left[ \begin{array}{l} \text{P1} \\ \text{P1} \end{array} \right.$	$= \overline{\text{F5}} \overline{\text{F4}} \overline{\text{F3}} \overline{\text{F2}} \text{F1}$	$= \overline{(\text{P1})}$	
$\left[ \begin{array}{l} \text{F2} \\ \text{F2} \end{array} \right.$	$\text{sF2} = \overline{\text{F2}} \text{F1}$	$\text{rF2} = \text{F2} \text{F1}$	$\left[ \begin{array}{l} \text{P2} \\ \text{P2} \end{array} \right.$	$= \overline{\text{F5}} \overline{\text{F4}} \overline{\text{F3}} \text{F2} \overline{\text{F1}}$	$= \overline{(\text{P2})}$	
$\left[ \begin{array}{l} \text{F3} \\ \text{F3} \end{array} \right.$	$\text{sF3} = \overline{\text{F3}} \text{F2} \text{F1}$	$\text{rF3} = \text{F3} \text{F2} \text{F1}$	$\left[ \begin{array}{l} \text{P3} \\ \text{P3} \end{array} \right.$	$= \overline{\text{F5}} \overline{\text{F4}} \overline{\text{F3}} \text{F2} \text{F1}$	$= \overline{(\text{P3})}$	
$\left[ \begin{array}{l} \text{F4} \\ \text{F4} \end{array} \right.$	$\text{sF4} = \overline{\text{F5}} \overline{\text{F4}} \text{F3} \text{F2} \text{F1}$	$\text{rF4} = \text{F4} \text{F3} \text{F2} \text{F1}$	$\left[ \begin{array}{l} \text{P23} \\ \text{P23} \end{array} \right.$	$= \text{F5} \text{F3} \text{F2} \text{F1}$	$= \overline{(\text{P23})}$	
$\left[ \begin{array}{l} \text{F5} \\ \text{F5} \end{array} \right.$	$\text{sF5} = \text{F4} \text{F3} \text{F2} \text{F1}$	$\text{rF5} = \text{P23}$	$\left[ \begin{array}{l} \text{P24} \\ \text{P24} \end{array} \right.$	$= \overline{\text{F5}} \overline{\text{F4}} \overline{\text{F3}} \overline{\text{F2}} \overline{\text{F1}}$	$= \overline{(\text{P24})}$	
$\left[ \begin{array}{l} \text{Sc} \\ \text{Sc} \end{array} \right.$	$\text{sSc} = \overline{\text{F5}} \text{F3} \text{F2} \text{F1}$	$\text{rSc} = \text{P23} + \overline{\text{Sr}} (\overline{\text{F3}} + \overline{\text{F2}} + \overline{\text{F1}})$	$\left[ \begin{array}{l} (\text{P8-P15}) \\ (\text{P16-P23}) \\ (\text{P24-P7}) \end{array} \right.$	$= \text{F4}$	$= \text{F5}$	$= \overline{\text{F5}} \overline{\text{F4}}$

$$\left[ \begin{array}{l} \text{Sw} \\ \text{Sr} \end{array} \right. \begin{array}{l} \text{sSw} = \overline{\text{Sc}} \overline{\text{Sr}} \overline{\text{Qg}} + \overline{\text{Sc}} \text{Sr} \overline{\text{Qg}} + \text{Bg} \overline{\text{Qg}} \\ \text{rSw} = \overline{\text{Sc}} \text{Sr} + \overline{\text{Sc}} \overline{\text{Sr}} \overline{\text{Bg}} + \text{Qg} \overline{\text{Bg}} \end{array}$$

$$\left[ \begin{array}{l} \text{Sr} \\ \text{rSr} \end{array} \right. \begin{array}{l} \text{sSr} = (\text{Sw delayed by 22 pulse times}) \\ \text{rSr} = (\overline{\text{Sw}} \text{ delayed by 22 pulse times}) \end{array}$$

$$\begin{aligned} \text{Qg} &= \overline{\text{Ec}} \text{O6} \overline{\text{O5}} \text{O4} \text{O3} \text{O1} \overline{\text{P24}} (\text{P24-P7}) + \text{(Fi)} \text{O6} \\ &\quad + \underline{\text{Cpg}} \underline{\text{M3g}} \underline{\text{N7g}} * + \text{Ec} \overline{\text{Rc}} \text{O6} \overline{\text{O5}} \text{O4} \text{O3} \text{O1} \text{P24} \\ \overline{\text{Qg}} &= \overline{(\text{Qg})} \end{aligned}$$

### C-2. INSTRUCTION REGISTER AND CONTROL

$$\left[ \begin{array}{l} \text{Ec} \\ \text{rEc} \end{array} \right. \begin{array}{l} \text{sEc} = \text{P24} \overline{\text{Ec}} \text{Rc} \\ \text{rEc} = \text{Eg} + \text{Ec} \text{O5} \text{O4} \text{O3} \overline{\text{Oc}} + \text{Ec} \overline{\text{Rc}} \text{Pc} \text{P1} \end{array}$$

$$\left[ \begin{array}{l} \text{Rc} \\ \text{rRc} \end{array} \right. \begin{array}{l} \text{sRc} = \text{(En)} \text{(Fi)} \text{Eg} \text{Oc} + \text{(En)} \text{(Fi)} \text{Eg} \overline{\text{O5}} \text{Is} + \text{P24} \overline{\text{Ec}} \overline{\text{Rc}} \text{Is} \left( \text{(En)} \right. \\ \quad \left. + \text{Oc} \text{(T6)} \text{(T5)} \text{(T2)} \text{(T1)} \right) \text{(Fi)} + \text{Ec} \text{O5} \text{O4} \text{O3} \overline{\text{Oc}} \\ \text{rRc} = \text{P24} \text{Rc} \text{Is} + \overline{\text{Ec}} \text{Rc} \text{Pc} \text{P1} \end{array}$$

$$\left[ \text{Eg} \right. = \text{P24} \text{Ec} \overline{\text{Rc}} ( \overline{\text{O5}} \overline{\text{O2}} + \overline{\text{O5}} \text{O6} + \overline{\text{O5}} \overline{\text{O3}} \text{O1} + \overline{\text{O5}} \overline{\text{O4}} \text{O1} + \text{O5} \text{Is} )$$

$$\left[ \begin{array}{l} \text{Is} \\ \text{rIs} \end{array} \right. \begin{array}{l} \text{sIs} = \text{P24} \\ \text{rIs} = (\overline{\text{Sr}} \text{sIw} + \text{Sr} \text{rIw}) \left[ \overline{\text{Ec}} \overline{\text{Rc}} (\text{P8-P15}) + \overline{\text{O5}} \text{Rc} (\text{P16-P23}) \right. \\ \quad \left. + \overline{\text{Rc}} \overline{\text{O5}} (\text{P8-P15}) + \text{Ec} \text{O5} (\text{P16-P23}) \right] \left[ \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \overline{\text{K1}} \overline{\text{F5}} \overline{\text{F3}} \right] \\ \quad + \text{P23} \text{Ec} \overline{\text{Rc}} \text{O6} \text{O5} \overline{\text{O4}} \overline{\text{Cr}} \end{array}$$

\* Optional sync terms for multiple computer operation.

$$\begin{array}{l}
 \left[ \begin{array}{l}
 \text{Iw} \\
 \text{rIw}
 \end{array} \right. \begin{array}{l}
 \text{sIw} = \overline{\text{Ec}} \text{ Rc (P8-P15) Sr} + \overline{\text{Ec}} \text{ Rc (P16-P23) Vg} + \text{Ec Oc (P8-P15)} \\
 \text{Sr} + \overline{\text{P24}} \text{ (P24-P7) M3g N7g Wg Ig} \\
 + \text{Ir} \left[ \overline{\text{Ec}} \text{ Rc (P8-P15)} + \overline{\text{Ec}} \text{ Rc (P16-P23)} + \text{Ec Oc (P8-P15)} \right. \\
 \left. + \text{(P24-P7) M3g N7g Wg} + \text{(En) (T6) (T5) (T4) (T1) (P8-P15)} \right] \\
 \text{rIw} = \overline{\text{(sIw)}}
 \end{array}
 \end{array}$$

$$\begin{array}{l}
 \left[ \begin{array}{l}
 \text{Ir} \\
 \text{rIr}
 \end{array} \right. \begin{array}{l}
 \text{sIr} = \text{(Iw delayed by 22 pulse times)} \\
 \text{rIr} = \overline{\text{(Iw delayed by 22 pulse times)}}
 \end{array}
 \end{array}$$

### C-3. OP CODE REGISTER

$$\begin{array}{l}
 \left[ \begin{array}{l}
 \text{Oc} \\
 \text{rOc}
 \end{array} \right. \begin{array}{l}
 \text{sOc} = \text{Og Vg} + \text{(En) P24 Is} \overline{\text{Ec}} \overline{\text{Rc}} \text{(T6) (T5) (T2) (T1)} \\
 + \text{P23} \overline{\text{Ec}} \text{ Rc O5 O4 O3 (} \overline{\text{O6}} \text{ Ig} + \overline{\text{O2}} \overline{\text{O1}} \text{ Cr} + \text{O6} \overline{\text{O2}} \text{ O1 Of} \\
 + \text{O6 O2 O1 Jg)} \\
 \text{rOc} = \text{Og} \overline{\text{Vg}} + \text{Eg}
 \end{array}
 \end{array}$$

$$\begin{array}{l}
 \left[ \begin{array}{l}
 \text{O6} \\
 \text{rO6}
 \end{array} \right. \begin{array}{l}
 \text{sO6} = \text{Og Oc} + \text{(Fi) F4 F3 F2 F1 Sr Sc} \\
 \text{rO6} = \text{Og} \overline{\text{Oc}} + \text{(Fi) P23}
 \end{array}
 \end{array}$$

$$\begin{array}{l}
 \left[ \begin{array}{l}
 \text{O5} \\
 \text{rO5}
 \end{array} \right. \begin{array}{l}
 \text{sO5} = \text{Og O6} + \text{(Fi) P23 O6} \overline{\text{O5}} \text{ O4} \\
 \text{rO5} = \text{Og} \overline{\text{O6}} + \text{(Fi) P23 O6 O5}
 \end{array}
 \end{array}$$

$$\begin{array}{l}
 \left[ \begin{array}{l}
 \text{O4} \\
 \text{rO4}
 \end{array} \right. \begin{array}{l}
 \text{sO4} = \text{Og O5} + \text{(Fi) (B5) } \overline{\text{O4}} \text{ O3} \\
 \text{rO4} = \text{Og} \overline{\text{O5}} + \text{(Fi) P23 O6 O5}
 \end{array}
 \end{array}$$

$$\begin{array}{l}
 \left[ \begin{array}{l}
 \text{O3} \\
 \text{rO3}
 \end{array} \right. \begin{array}{l}
 \text{sO3} = \text{Og O4} + \text{P23} \overline{\text{O6}} \text{ O5} \overline{\text{O4}} \overline{\text{O3}} \overline{\text{O2}} \overline{\text{O1}} \text{ (Aw} \overline{\text{Ar}} + \overline{\text{Aw}} \text{ Ar)} \\
 + \text{P24} \overline{\text{O6}} \text{ O5} \overline{\text{O4}} \overline{\text{O3}} \text{ O2 O1} \overline{\text{Cw}} + \text{(Fi) (B6)} \\
 \text{rO3} = \text{Og} \overline{\text{O4}} + \text{(Fi) P23 O6 O5}
 \end{array}
 \end{array}$$

$$\left[ \begin{array}{l} \text{O2} \\ \text{O2} \end{array} \right. \begin{array}{l} \text{sO2} = \text{Og O3} + \overline{\text{Ec}} \text{ Rc P2 Vg} \\ \text{rO2} = \text{Og } \overline{\text{O3}} + \text{P24 Ec } \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O1}} + \text{P24 Ec } \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \text{O4 } \overline{\text{O3}} \\ \quad + \overline{\text{Ec}} \text{ Rc P2 } \overline{\text{Vg}} \end{array}$$

$$\left[ \begin{array}{l} \text{O1} \\ \text{O1} \end{array} \right. \begin{array}{l} \text{sO1} = \text{Og O2} + \text{(Fi)} \text{(B4)} \overline{\text{O5}} + \text{(Fi)} \text{O5 M1r} \\ \text{rO1} = \text{Og } \overline{\text{O2}} + \text{(Fi)} \overline{\text{O3}} + \text{(Fi)} \text{O5 } \overline{\text{M1r}} \end{array}$$

$$\text{Og} = \overline{\text{Ec}} \text{ Rc F4}$$

#### C-4. OPERAND LINE SELECTOR

$$\left[ \begin{array}{l} \text{L5} \\ \text{L5} \end{array} \right. \begin{array}{l} \text{sL5} = \text{Lg } \overline{\text{O2}} \text{ Vg} + \text{Lg O2 Iw} + \overline{\text{O6}} \text{O5 } \overline{\text{O3}} \text{P24 Ec} \\ \text{rL5} = \text{Lg } \overline{\text{O2}} \overline{\text{Vg}} + \text{Lg O2 } \overline{\text{Iw}} \end{array}$$

$$\left[ \begin{array}{l} \text{L4} \\ \text{L4} \end{array} \right. \begin{array}{l} \text{sL4} = \text{Lg L5} + \overline{\text{O6}} \text{O5 O4 } \overline{\text{O3}} \overline{\text{O2}} \left[ \text{P24 Ec (L1 Cr} + \overline{\text{L1}} \overline{\text{Cr}}) + \text{P23} \right. \\ \quad \left. \text{Rc } \overline{\text{L1}} \overline{\text{Zg}} + \text{P24 Rc L1 } \overline{\text{Zg}} \right] + \overline{\text{O6}} \text{O5 O4 } \overline{\text{O3}} \text{O2 } \overline{\text{O1}} \text{P1 Be } \overline{\text{Br}} \\ \text{rL4} = \text{Lg } \overline{\text{L5}} + \overline{\text{O6}} \text{O5 O4 } \overline{\text{O3}} \overline{\text{O2}} \text{P23 L4} + \overline{\text{O6}} \text{O5 O4 } \overline{\text{O3}} \text{O2 } \overline{\text{O1}} \text{P24} \end{array}$$

$$\left[ \begin{array}{l} \text{L3} \\ \text{L3} \end{array} \right. \begin{array}{l} \text{sL3} = \text{Lg L4} + \overline{\text{O6}} \text{O5 } \overline{\text{O3}} (\text{P24 Bw} + \text{P2 Ar}) \\ \quad + \overline{\text{O6}} \text{O5 O4 } \overline{\text{O3}} \text{O2 } \overline{\text{O1}} \text{Ec } \overline{\text{L5}} \text{Be} \\ \text{rL3} = \text{Lg } \overline{\text{L4}} + \overline{\text{O6}} \text{O5 } \overline{\text{O3}} (\text{P24 } \overline{\text{Bw}} + \text{P2 } \overline{\text{Ar}}) \\ \quad + \overline{\text{O6}} \text{O5 O4 } \overline{\text{O3}} \text{O2 } \overline{\text{O1}} \text{Ec } \overline{\text{L5}} \text{Be} \end{array}$$

$$\left[ \begin{array}{l} \text{L2} \\ \text{L2} \end{array} \right. \begin{array}{l} \text{sL2} = \text{Lg L3} + \overline{\text{O6}} \text{O5 } \overline{\text{O3}} \overline{\text{O2}} \text{Ec Br} + \overline{\text{O6}} \text{O5 O4 } \overline{\text{O3}} \text{O2 } \overline{\text{O1}} \text{P1 } \overline{\text{Be}} \text{Br} \\ \text{rL2} = \text{Lg } \overline{\text{L3}} + \overline{\text{O6}} \text{O5 } \overline{\text{O3}} \overline{\text{O2}} \text{Ec } \overline{\text{Br}} + \overline{\text{O6}} \text{O5 O4 } \overline{\text{O3}} \text{O2 } \overline{\text{O1}} \text{P24} \end{array}$$

$$\begin{array}{l}
\text{L1} \left[ \begin{array}{l}
\text{sL1} = \text{Lg L2} + \overline{\text{O6}} \text{O5} \overline{\text{O3}} \overline{\text{O2}} \text{Ec} (\text{Zg O4} + \overline{\text{Ar O4}}) + \text{O6} \overline{\text{O5}} \text{O4} \overline{\text{O2}} \text{Ec Sw} \\
\text{rL1} = \text{Lg} \overline{\text{L2}} + \overline{\text{O6}} \text{O5} \overline{\text{O3}} \overline{\text{O2}} \text{Ec} (\overline{\text{Zg O4}} + \overline{\text{Ar O4}}) + \text{O6} \overline{\text{O5}} \text{O4} \overline{\text{O2}} \text{Ec} \overline{\text{Sw}}
\end{array} \right. \\
\\
*\text{L0} \left[ \begin{array}{l}
\text{sL0} = \text{Lg L1} \\
\text{rL0} = \text{Lg} \overline{\text{L1}}
\end{array} \right. \\
\\
\text{Lg} = \overline{\text{Ec} + \overline{\text{Rc}} + \text{F5} + \text{F4 F3} + \text{F4 F2} + \text{F4 F1} + \text{P24} + \text{P1}} \\
\\
\left[ \begin{array}{l}
\text{M0g} = *\overline{\text{L0}} \overline{\text{L5}} \overline{\text{L4}} \\
\text{M1g} = \overline{\text{L0}} \overline{\text{L5}} \text{L4} \\
\text{M2g} = \overline{\text{L0}} \text{L5} \overline{\text{L4}} \\
\text{M3g} = \overline{\text{L0}} \text{L5} \text{L4} \\
*\text{M4g} = \text{L0} \overline{\text{L5}} \overline{\text{L4}} \\
*\text{M5g} = \text{L0} \overline{\text{L5}} \text{L4} \\
*\text{M6g} = \text{L0} \text{L5} \overline{\text{L4}} \\
*\text{M7g} = \text{L0} \text{L5} \text{L4}
\end{array} \right. \left[ \begin{array}{l}
\text{N0g} = \overline{\text{L3}} \overline{\text{L2}} \overline{\text{L1}} \\
\text{N1g} = \overline{\text{L3}} \overline{\text{L2}} \text{L1} \\
\text{N2g} = \overline{\text{L3}} \text{L2} \overline{\text{L1}} \\
\text{N3g} = \overline{\text{L3}} \text{L2} \text{L1} \\
\text{N4g} = \text{L3} \overline{\text{L2}} \overline{\text{L1}} \\
\text{N5g} = \text{L3} \overline{\text{L2}} \text{L1} \\
\text{N6g} = \text{L3} \text{L2} \overline{\text{L1}} \\
\text{N7g} = \text{L3} \text{L2} \text{L1}
\end{array} \right.
\end{array}$$

C-5. COMMAND LINE SELECTOR

$$\begin{array}{l}
\text{K4} \left[ \begin{array}{l}
\text{sK4} = \text{Kg L4} \\
\text{rK4} = \text{Kg} \overline{\text{L4}} \quad (\text{En}) \quad (\text{T6}) \quad (\text{T5}) \quad (\text{T4}) \quad (\text{T1}) \quad \text{P23}
\end{array} \right. \\
\\
\text{K3} \left[ \begin{array}{l}
\text{sK3} = \text{Kg L3} \\
\text{rK3} = \text{Kg} \overline{\text{L3}} + \quad (\text{En}) \quad (\text{T6}) \quad (\text{T5}) \quad (\text{T4}) \quad (\text{T1}) \quad \text{P23}
\end{array} \right. \\
\\
\text{K2} \left[ \begin{array}{l}
\text{sK2} = \text{Kg L2} \\
\text{rK2} = \text{Kg} \overline{\text{L2}} + \quad (\text{En}) \quad (\text{T6}) \quad (\text{T5}) \quad (\text{T4}) \quad (\text{T1}) \quad \text{P23}
\end{array} \right. \\
\\
\text{K1} \left[ \begin{array}{l}
\text{sK1} = \text{Kg L1} + \quad (\text{En}) \quad (\text{T6}) \quad (\text{T5}) \quad (\text{T4}) \quad (\text{T1}) \quad \text{P23} \\
\text{rK1} = \text{Kg} \overline{\text{L1}}
\end{array} \right. \\
\\
\text{Kg} = \text{Ec O5 O4 O3 F4} (\overline{\text{O6}} + \overline{\text{O2}})
\end{array}$$

\*L0 and M4g thru M7g are options for memory expansion.



$$\begin{aligned}
 \left[ \begin{array}{l} \text{Vg} \\ \overline{\text{Vg}} \end{array} \right. &= \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \overline{\text{K1}} \text{M0r} + \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \overline{\text{K1}} \text{M1r} + \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \overline{\text{K1}} \text{M2r} \\
 &+ \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \overline{\text{K1}} \text{M3r} + \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \overline{\text{K1}} \text{M4r} + \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \overline{\text{K1}} \text{M5r} \\
 &+ \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \overline{\text{K1}} \text{M6r} + \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \overline{\text{K1}} \text{M7r} + \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \overline{\text{K1}} \text{M10r} \\
 &+ \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \overline{\text{K1}} \text{M11r} + \dots + \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \overline{\text{K1}} \text{M16r} + \overline{\text{K4}} \overline{\text{K3}} \overline{\text{K2}} \\
 &\text{K1 M17r} \\
 \overline{\text{Vg}} &= (\overline{\text{Vg}})
 \end{aligned}$$

C-6. A REGISTER

$$\begin{aligned}
 \left[ \begin{array}{l} \text{sAw} \\ \text{Aw} \\ \text{rAw} \end{array} \right. &= \text{Ec} \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O4}} \text{O3} \overline{\text{O2}} \text{O1} \text{Fg} \\
 &+ \text{Ec} \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \text{O3} \overline{\text{O2}} \text{Zg} \\
 &+ \text{Ec} \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \overline{\text{O3}} \overline{\text{O2}} \text{O1} \text{Pc} \\
 &+ \text{Ec} \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \text{O3} \overline{\text{O2}} \text{O1} (\text{L1} \text{Vg} + \text{Ar} \overline{\text{Vg}}) \\
 &+ \text{Ec} \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O3}} \overline{\text{O2}} (\overline{\text{P23}} \overline{\text{P2}} \text{L1} + \text{P2} \text{L3} + \overline{\text{P23}} \text{O4} \text{L1}) \\
 &+ \text{Ec} \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \overline{\text{O3}} \text{O2} \overline{\text{P23}} \text{Ae} \\
 &+ \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \overline{\text{O3}} \text{P23} \text{Ar} \\
 &+ \text{Ec} \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \overline{\text{O3}} \overline{\text{O2}} \overline{\text{O1}} \text{Fg} \text{Aw} \\
 &+ \text{Ec} \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \overline{\text{O3}} \overline{\text{O2}} \text{O1} \text{Cr} \\
 &+ \text{Ec} \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \overline{\text{O3}} \text{O2} \text{Zg} \\
 &+ \text{Ar} \left[ \overline{\text{Ec} \overline{\text{Rc}} (\overline{\text{O5}} \overline{\text{O4}} \overline{\text{O2}} \text{O1} + \overline{\text{O5}} \text{O4} \text{O3} \overline{\text{O2}} + \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O3}} \right. \\
 &\quad \left. + \overline{\text{O6}} \overline{\text{O4}} \overline{\text{O2}} \text{O1} + \text{O6} \overline{\text{O5}} \overline{\text{O4}} \overline{\text{O3}} \overline{\text{O2}} \overline{\text{O1}} \text{Fg}) \right] \\
 \text{rAw} &= (\overline{\text{sAw}})
 \end{aligned}$$

$$\left[ \begin{array}{l} \text{Ar} \end{array} \right. \left[ \begin{array}{l} \text{sAr} \\ \text{rAr} \end{array} \right. = \text{Ae} \\
 \phantom{\left[ \begin{array}{l} \text{Ar} \end{array} \right.} \phantom{\left[ \begin{array}{l} \text{sAr} \\ \text{rAr} \end{array} \right.} = \overline{\text{Ae}}
 \end{array}$$

$$\left[ \begin{array}{l} \text{Ae} \end{array} \right. \left[ \begin{array}{l} \text{sAe} \\ \text{rAe} \end{array} \right. = (\text{Aw delayed by 21 pulse times}) \\
 \phantom{\left[ \begin{array}{l} \text{Ae} \end{array} \right.} \phantom{\left[ \begin{array}{l} \text{sAe} \\ \text{rAe} \end{array} \right.} = (\overline{\text{Aw}} \text{ delayed by 21 pulse times})
 \end{array}$$

C-7. B, REGISTER

$$\begin{aligned}
 \text{Bw} \quad \text{sBw} &= \overline{\text{Ec}} \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \text{O3} \text{O2} \text{Fg} \\
 &+ \overline{\text{Ec}} \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \text{O4} \text{O3} \text{O2} \text{Zg} \\
 &+ \overline{\text{Ec}} \overline{\text{Rc}} \text{O6} \overline{\text{O5}} \overline{\text{O4}} \text{O2} \overline{\text{O1}} \text{Fg} \text{Cr} \\
 &+ \overline{\text{Ec}} \overline{\text{Rc}} \overline{\text{O6}} \text{O5} \overline{\text{O4}} \overline{\text{O3}} \overline{\text{O2}} \overline{\text{P2}} \text{L2} \\
 &+ \overline{\text{Ec}} \overline{\text{Rc}} \overline{\text{O6}} \text{O5} \overline{\text{O3}} \text{O2} (\overline{\text{P23}} \text{Be} + \text{P23} \text{L3}) \\
 &+ \overline{\text{Ec}} \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \overline{\text{O3}} \text{O2} \text{Cr} \\
 &+ \overline{\text{O6}} \text{O5} \text{O4} \overline{\text{O3}} \overline{\text{O2}} (\overline{\text{Ec}} \overline{\text{P2}} \overline{\text{P3}} \text{L2} + \overline{\text{Ec}} \text{P3} \overline{\text{L5}} \overline{\text{L4}} \\
 &+ \overline{\text{Ec}} \text{P3} \text{L5} \text{L4} + \overline{\text{Ec}} \overline{\text{P2}} \text{L4}) \\
 &+ \overline{\text{P1}} \text{Br} \left[ \overline{\text{Ec}} \overline{\text{Rc}} (\overline{\text{O6}} \overline{\text{O5}} \text{O3} \text{O2} + \overline{\text{O6}} \text{O5} \overline{\text{O3}} + \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \text{O2} \text{Fg} \right. \\
 &\left. + \overline{\text{O5}} \overline{\text{O4}} \overline{\text{O3}} \text{O2} \right) ] \\
 \text{rBw} &= \overline{(\text{sBw})}
 \end{aligned}$$

$$\begin{aligned}
 \text{Br} \quad \text{sBr} &= \text{Be} \\
 \text{rBr} &= \overline{\text{Be}}
 \end{aligned}$$

$$\begin{aligned}
 \text{Be} \quad \text{sBe} &= (\text{Bw} \text{ delayed by } 21 \text{ pulse times}) \\
 \text{rBe} &= \overline{(\text{Bw} \text{ delayed by } 21 \text{ pulse times})}
 \end{aligned}$$

C-8. C REGISTER

$$\begin{aligned}
 \text{Cw} \quad \text{sCw} &= \overline{\text{Ec}} \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \text{O3} \overline{\text{O2}} \overline{\text{O1}} \text{Fg} \\
 &+ \overline{\text{Ec}} \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \overline{\text{O3}} \text{Ig} \\
 &+ \text{P24} \text{Cw} \\
 &+ \overline{\text{Ec}} \overline{\text{Rc}} \text{O5} \overline{\text{O4}} \text{Zg} \\
 &+ \overline{\text{Ec}} \overline{\text{Rc}} \overline{\text{O6}} \text{O5} \text{O4} \overline{\text{O3}} \overline{\text{O2}} \overline{\text{O1}} \text{Dg} \\
 &+ \overline{\text{P24}} \text{Cr} \left[ \overline{\text{Ec}} \overline{\text{Rc}} (\overline{\text{O5}} \overline{\text{O4}} \text{O3} \overline{\text{O2}} \overline{\text{O1}} + \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \overline{\text{O3}} \right. \\
 &\left. + \overline{\text{O5}} \overline{\text{O4}} + \overline{\text{O6}} \text{O5} \text{O4} \overline{\text{O3}} \overline{\text{O2}} \overline{\text{O1}} \right) ] \\
 \text{rCw} &= \overline{(\text{sCw})}
 \end{aligned}$$

$$\left[ \begin{array}{l} \text{Cr} \\ \text{Cr} \end{array} \right. \begin{array}{l} \text{sCr} \\ \text{rCr} \end{array} = \begin{array}{l} \text{Ce} \\ \overline{\text{Ce}} \end{array}$$

$$\left[ \begin{array}{l} \text{Ce} \\ \text{Ce} \end{array} \right. \begin{array}{l} \text{sCe} \\ \text{rCe} \end{array} = \begin{array}{l} (\text{Cw delayed by 21 pulse times}) \\ (\overline{\text{Cw}} \text{ delayed by 21 pulse times}) \end{array}$$

C-9. ADDER

$$\left[ \begin{array}{l} \text{Zg} \\ \overline{\text{Zg}} \end{array} \right. = \begin{array}{l} (\overline{\text{Zg}}) \\ \text{Xg Yg } \overline{\text{Ca}} + \text{Xg } \overline{\text{Yg}} \text{ Ca} + \overline{\text{Xg}} \text{ Yg Ca} + \overline{\text{Xg}} \overline{\text{Yg}} \overline{\text{Ca}} \end{array}$$

$$\left[ \begin{array}{l} \text{Xg} \\ \overline{\text{Xg}} \end{array} \right. = \begin{array}{l} \overline{\text{O6}} \text{ O5 O4 } \overline{\text{O3}} \overline{\text{O2}} (\overline{\text{L4}} \text{ Dg} + \text{L4 } \overline{\text{Dg}}) \\ + \overline{\text{O6}} \text{ O5 O4 } \overline{\text{O3}} \text{ O2 } \overline{\text{O1}} (\text{L2 Cr} + \text{L4 } \overline{\text{Cr}}) \\ + \overline{\text{O5}} \overline{\text{O1}} \text{ Fg} + \overline{\text{O5}} \text{ O1 } \overline{\text{Fg}} + \text{O6 O5 } \overline{\text{O4}} + \text{O5 } \overline{\text{O4}} \overline{\text{O3}} \overline{\text{L4}} (\overline{\text{O2}} + \text{P2}) \\ \overline{\text{Xg}} = (\overline{\text{Xg}}) \end{array}$$

$$\left[ \begin{array}{l} \text{Yg} \\ \overline{\text{Yg}} \end{array} \right. = \begin{array}{l} \overline{\text{O6}} \text{ O5 O4 } \overline{\text{O3}} \text{ O2 L5 } (\overline{\text{P24}} \text{ Ae} + \text{P24 Ar}) \\ + \overline{\text{O6}} \text{ O4 } \overline{\text{O2}} \text{ Ar} + \overline{\text{O5}} \text{ O2 Br} + \text{O5 } \overline{\text{O4}} \text{ Cr} \\ \overline{\text{Yg}} = (\overline{\text{Yg}}) \end{array}$$

$$\left[ \begin{array}{l} \text{Ca} \\ \text{Ca} \end{array} \right. \begin{array}{l} \text{sCa} \\ \text{rCa} \end{array} = \begin{array}{l} \overline{\text{P1}} \overline{\text{P24}} \text{ Ec } \overline{\text{Rc}} \text{ Xg Yg } \overline{\text{Ca}} + \text{P24 Rc Is } \overline{\text{O6}} \overline{\text{O5}} \text{ O4 O3 O1} \\ + \overline{\text{O6}} \text{ O5 O4 } \overline{\text{O3}} \overline{\text{O2}} \text{ P1 L4} + \overline{\text{O6}} \text{ O5 O4 } \overline{\text{O3}} \text{ O2 } \overline{\text{O1}} \text{ P1 B} \overline{\text{Br}} \\ \text{rCa} = \overline{\text{P1}} \overline{\text{P24}} \overline{\text{Xg}} \overline{\text{Yg}} + \text{Ca Rc} + \text{O5 P24} \end{array}$$

$$\left[ \begin{array}{l} \text{Dg} \\ \overline{\text{Dg}} \end{array} \right. = \begin{array}{l} \text{O1 Cr} + \overline{\text{O1}} \text{ L5 } (\text{Of } \overline{\text{Pc}} \text{ Cr} + \text{Of Pc L4} + \overline{\text{Of}} \text{ Pc } \overline{\text{L4}} + \overline{\text{Of}} \overline{\text{Pc}} \text{ Ce}) \\ + \overline{\text{O1}} \overline{\text{L5}} \text{ F5 F3 } \overline{\text{F2}} \text{ F1} \\ \overline{\text{Dg}} = (\overline{\text{Dg}}) \end{array}$$

$$\begin{aligned}
 \left[ \begin{array}{l} \text{sOf} \\ \text{Of} \\ \text{rOf} \end{array} \right. &= P23 \text{ Ec } \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \text{O4 O3 } \overline{\text{O2}} (\overline{\text{Xg}} \overline{\text{Yg}} \text{Ca} + \text{Xg Yg } \overline{\text{Ca}}) \\
 &+ \overline{\text{Of}} \text{Ec } \overline{\text{O6}} \text{O5 O4 } \overline{\text{O3}} \overline{\text{O2}} \overline{\text{O1}} \text{Pc} + P24 \text{ Rc O6 } \overline{\text{O5}} \text{O4 O3 O2 } \overline{\text{O1}} \\
 &= P23 \text{ Ec O6 O5 O4 O3 } \overline{\text{O2}} \text{O1} + P23 \overline{\text{O6}} \text{O5 O4 } \overline{\text{O3}} \overline{\text{O2}} \overline{\text{O1}} \\
 &+ \overline{\text{P1}} \overline{\text{P24}} \text{Ec } \overline{\text{Rc}} \text{O6 } \overline{\text{O5}} \text{O4 O3 O2 } \overline{\text{O1}} (\text{Fg } \overline{\text{Ar}} + \overline{\text{Fg}} \text{Ar})
 \end{aligned}$$

C-10. DATA TRANSFER GATES

$$\begin{aligned}
 \left[ \begin{array}{l} \text{Fg} \\ \overline{\text{Fg}} \end{array} \right. &= \text{M0g N0g M0r} + \text{M0g N1g M1r} + \dots + \text{M1g N7g M15r} \\
 &+ \text{M3g N7g Ir} + \text{F} \times \text{g} \\
 &= (\overline{\text{Fg}})
 \end{aligned}$$

$$\left[ \begin{array}{l} \text{Wg} \end{array} \right. = ( \overline{\text{O6}} \overline{\text{O5}} \text{O4 } \overline{\text{O3}} + \text{O6 O5 O4 } \overline{\text{O3}} \text{O1} + \overline{\text{O6}} \text{O5 } \overline{\text{O4}} \text{O3 } \overline{\text{O2}} \text{O1} ) \Gamma_c \overline{\text{Rc}}$$

$\begin{matrix} 10, 11, 12, 13 & 71, 73 & 25 \\ 54 & 03, 01 & \\ 07, 00 & 12, 11 & \\ 44, 46 & 25, 27 & \\ 14, 16 & 20, 21 & \end{matrix}$

$$\begin{aligned}
 \left[ \begin{array}{l} \text{Ig} \\ \overline{\text{Ig}} \end{array} \right. &= \overline{\text{P24}} \overline{\text{O5}} \overline{\text{O2}} \overline{\text{O1}} \text{Cr} + \overline{\text{P24}} \overline{\text{O6}} \overline{\text{O2}} \text{O1 Ar} \\
 &+ \overline{\text{P24}} \overline{\text{O4}} \overline{\text{O2}} \text{Ar} + \overline{\text{P24}} \overline{\text{O6}} \text{O2 Br} + \overline{\text{P24}} \text{O6 O5 } \overline{\text{O2}} \text{Vg} \\
 &+ \overline{\text{P24}} \text{O6 O5 O2 Vg Hdg} + \text{P24 Pc} \\
 &= (\overline{\text{Ig}})
 \end{aligned}$$

$$\begin{aligned}
 \left[ \begin{array}{l} \text{sPc} \\ \text{Pc} \\ \text{rPc} \end{array} \right. &= \text{Ec } \overline{\text{Rc}} \overline{\text{P1}} \overline{\text{O5}} \text{O3 } \overline{\text{Ig}} \overline{\text{Pc}} + \overline{\text{P1}} \text{Ec } \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \text{O3 Fg } \overline{\text{Pc}} \\
 &+ \overline{\text{P1}} \overline{\text{Ec}} \text{Rc Vg } \overline{\text{Pc}} + \overline{\text{P24}} \text{Ec } \overline{\text{O6}} \text{O5 O4 } \overline{\text{O3}} \overline{\text{O2}} \overline{\text{O1}} \overline{\text{Of}} \text{Dg} \\
 &+ (\text{Fi}) (\text{B1}) + \text{Ec Rc } \overline{\text{O6}} \overline{\text{O5}} \overline{\text{O4}} \overline{\text{O3}} \overline{\text{O2}} \overline{\text{O1}} \\
 &= \text{Ec } \overline{\text{Rc}} \overline{\text{P1}} \overline{\text{O5}} \text{O3 } \overline{\text{Ig}} \overline{\text{Pc}} + \overline{\text{P1}} \text{Ec } \overline{\text{Rc}} \overline{\text{O6}} \overline{\text{O5}} \text{O3 Fg } \overline{\text{Pc}} \\
 &+ \text{M3g N7g Ec } \overline{\text{Rc}} \text{O3} + \overline{\text{P1}} \overline{\text{Ec}} \text{Rc Vg } \overline{\text{Pc}} + (\text{En}) (\text{Bp}) \\
 &+ \text{Ec } \overline{\text{O6}} \text{O5 O4 } \overline{\text{O3}} \overline{\text{O2}} \overline{\text{O1}} \text{Of Pc}
 \end{aligned}$$

C-11. MEMORY LINES

[	M0w	$sM0w = M0g N0g Wg [ \overline{\phi 2} \overline{\phi 1} (\overline{O6} O5 \overline{O4} O3 \overline{O2} O1) M15r$ $+ Wg \overline{\phi 2} \overline{\phi 1} (\overline{O6} O5 \overline{O4} O3 \overline{O2} O1 \overline{I}g) ] + - - -$
		$rM0w = M0g N0g Wg [ (\overline{\phi 2} \overline{\phi 1} (\overline{O6} O5 \overline{O4} O3 \overline{O2} O1) \overline{M15r}$ $+ Wg \overline{\phi 2} \overline{\phi 1} (\overline{O6} O5 \overline{O4} O3 \overline{O2} O1) \overline{I}g) ] + - - -$
[	M0r	$sM0r = (M0w \text{ delayed by } 382 \text{ pulse times})$
		$rM0r = (\overline{M0w} \text{ delayed by } 382 \text{ pulse times})$
[	M1w	$sM1w = M0g N1g Wg I_g + \overline{[M0g N1g Wg]} [M1r ( \textcircled{Fi} O5)$ $+ \textcircled{Fi} O5 O1 ]$
		$rM1w = M0g N1g Wg \overline{I_g} + \overline{[M0g N1g Wg]} [M1r ( \textcircled{Fi} O5)$ $+ \textcircled{Fi} O5 O1 ]$
[	M1r	$sM1r = (M1w \text{ delayed by } 6142 \text{ pulse times})$
		$rM1r = (\overline{M1w} \text{ delayed by } 6142 \text{ pulse times})$
[	M2w	$sM2w = M0g N2g Wg I_g + \overline{[M0g N2g Wg]} [M2r]$
		$rM2w = M0g N2g Wg \overline{I_g} + \overline{[M0g N2g Wg]} [\overline{M2r}]$
[	M2r	$sM2r = (M2w \text{ delayed by } 6142 \text{ pulse times})$
		$rM2r = (\overline{M2w} \text{ delayed by } 6142 \text{ pulse times})$
[	M4w	$sM4w = - - - + \overline{[M0g N4g Wg]} [ \overline{\phi 2} \overline{\phi 1} M15r + (\overline{\phi 2} + \phi 1) M4r ]$
		$rM4w = - - - + \overline{[M0g N4g Wg]} [ \overline{\phi 2} \overline{\phi 1} \overline{M15r} + (\overline{\phi 2} + \phi 1) \overline{M4r} ]$

Line 2, typical of lines 3, 5, 6, 7, 8, 9, 10, 11, - - -29 and 30.

$$\begin{array}{l}
 \left[ \begin{array}{l}
 \text{sM7w} \\
 \text{M7w} \\
 \text{rM7w}
 \end{array} \right.
 \begin{array}{l}
 = M0g N7g Wg Ig + \overline{[M0g N7g Wg]} [M7r (\overline{O6} O5 \overline{O4} O3 O2 \overline{O1} Ec) \\
 + (\overline{O6} O5 \overline{O4} O3 O2 \overline{O1} Ec) Fg] \\
 \\
 = M0g N7g Wg \overline{Ig} + \overline{[M0g N7g Wg]} [\overline{M7r} (\overline{O6} O5 \overline{O4} O3 O2 \overline{O1} Ec) \\
 + (\overline{O6} O5 \overline{O4} O3 O2 \overline{O1} Ec) \overline{Fg}]
 \end{array}
 \end{array}$$

### C-12. CHARACTER INPUT

$$\left[ \begin{array}{l}
 \text{Rf} \\
 \text{rRf}
 \end{array} \right.
 \begin{array}{l}
 \text{sRf} = Ec O6 \overline{O5} O4 \overline{O3} O2 + (Fi) \overline{Pc} (P8-P15) (Mr) \\
 \text{rRf} = Ec O6 \overline{O5} O4 \overline{O3} \overline{O2} + (Fi) (Mr) (P8-P15) + (Rc) \overline{Ec}
 \end{array}$$

$$\left[ \begin{array}{l}
 \text{Tf} \\
 \text{rTf}
 \end{array} \right.
 \begin{array}{l}
 \text{sTf} = Ec O6 \overline{O5} O4 \overline{O3} O1 \\
 \text{rTf} = Ec O6 \overline{O5} O4 \overline{O3} \overline{O1} + (Tc) \overline{Ec} + (Fi) (P8-P15)
 \end{array}$$

$$\left[ \begin{array}{l}
 \text{Reader Contacts Return} \\
 \text{Type Light}
 \end{array} \right.
 \begin{array}{l}
 = Rf \overline{Tf} \\
 = \overline{Rf} Tf
 \end{array}$$

$$\left[ \begin{array}{l}
 \text{Typewriter Contacts Return} \\
 \text{LR Reader Release Magnet}
 \end{array} \right.
 \begin{array}{l}
 = (En) + \overline{Rf} Tf \\
 = Rf \overline{Tf}
 \end{array}$$

$$\left[ \begin{array}{l}
 \text{LR Reader Release Magnet} \\
 \text{Type Light}
 \end{array} \right.
 \begin{array}{l}
 = Rf \overline{Tf} \\
 = \overline{Rf} Tf
 \end{array}$$

$$\left[ \begin{array}{l}
 \text{Type Light} \\
 \text{Bootstrap Start}
 \end{array} \right.
 \begin{array}{l}
 = \overline{Rf} Tf \\
 = (Fi) \overline{Pc}
 \end{array}$$

$$\left[ \begin{array}{l}
 \text{Bootstrap Start} \\
 \text{Bootstrap Stop}
 \end{array} \right.
 \begin{array}{l}
 = (Fi) \overline{Pc} \\
 = (Fi) Pc
 \end{array}$$

$$\left[ \begin{array}{l}
 \text{Bootstrap Stop} \\
 \text{Gate Line for Fast Readers}
 \end{array} \right.
 \begin{array}{l}
 = (Fi) Pc \\
 = Rf Tf
 \end{array}$$

$$\begin{aligned}
 \left[ \begin{array}{l} Bg \\ \overline{Bg} \end{array} \right. &= P24 ( \textcircled{R1} + \textcircled{S1} + \textcircled{T1} + \textcircled{U1} ) \\
 &+ P1 ( \textcircled{R2} + \textcircled{S2} + \textcircled{T2} + \textcircled{U2} ) \\
 &+ P2 ( \textcircled{R3} + \textcircled{S3} + \textcircled{T3} + \textcircled{U3} ) \\
 &+ P3 ( \textcircled{R4} + \textcircled{S4} + \textcircled{T4} + \textcircled{U4} ) \\
 &+ (P24-P7) F3 \overline{F2} \overline{F1} ( \textcircled{R5} + \textcircled{S5} + \textcircled{T5} + \textcircled{U5} ) \\
 &+ (P24-P7) F3 \overline{F2} F1 ( \textcircled{R6} + \textcircled{S6} + \textcircled{T6} + \textcircled{U6} ) \\
 &+ (P24-P7) F3 F2 \overline{F1} ( \textcircled{R7} + \textcircled{S7} + \textcircled{U7} ) \\
 &+ (P24-P7) F3 F2 F1 ( \textcircled{R8} + \textcircled{S8} + \textcircled{U8} ) \\
 &= \overline{(Bg)}
 \end{aligned}$$

C-13. CHARACTER OUTPUT AND CONTROL PULSE OUTPUT

$$\left[ \left[ \begin{array}{l} Cog \end{array} \right. \right. = Ec O6 O5 \overline{O4} - \text{output character execute}$$

$$\left[ \begin{array}{l} K3 \\ K2 \\ K1 \\ L1 \\ L2 \\ L3 \\ L4 \\ L5 \\ O1 \\ O2 \\ O3 \end{array} \right. = \left. \begin{array}{l} K3 \\ K2 \\ K1 \\ L1 \\ L2 \\ L3 \\ L4 \\ L5 \\ O1 \\ O2 \\ O3 \end{array} \right\} \begin{array}{l} \text{Destination code for character and control pulse outputs} \\ \\ \\ \text{Code output for character and control pulse outputs} \end{array}$$

$$\left[ \left[ \begin{array}{l} Cpg \end{array} \right. \right. = Ec O6 O5 O4 \overline{O3} \overline{O2} \overline{O1} \text{ (Control pulse execute)}$$

$$\left[ \left[ \begin{array}{l} Tg \end{array} \right. \right. = Ec O6 O5 \overline{O4} K3 \overline{K2} K1 \overline{K4} \text{ (Typewriter gate signal)}$$

LTC	= Tg	(Execute to typewriter translator clutch)
LT1	= L1 Tg	} (Code to translator magnets)
LT2	= L2 Tg	
LT3	= L3 Tg	
LT4	= L4 Tg	
LT5	= L5 Tg	
LT6	= O1 Tg	

[Pg = Ec O6 O5  $\overline{O4}$  K3 K2  $\overline{K1}$   $\overline{K4}$  (Punch gate signal)]

LPC	= Pg	(Execute to tape punch clutch)
LP1	= L1 Pg	} (Code to punch magnets)
LP2	= L2 Pg	
LP3	= L3 Pg	
LP4	= L4 Pg	
LP5	= L5 Pg	
LP6	= O1 Pg	
LP7	= O2 Pg	
LP8	= O3 Pg	

C-14. JUMP CONTROL INPUT GATE

[Jg	= M0g N0g (J0) +-----+ M3g N0g (J24)
	M0g N1g (J1) +-----+ M3g N1g (J25)
	-----
	M0g N4g (J4) -----+ M3g N4g (J28)
	M0g N5g (J5) -----+ M3g N5g (Bp)
	M0g N6g (J6) -----+ M3g N6g $\overline{Rf}$ $\overline{Tf}$
	M0g N7g (J7) -----+ M3g N7g (Tb)



C-15. SERIAL INPUT

$$[Hsg = E_c O_6 O_5 O_4 \overline{O_3} O_2 O_1 V_g \overline{P_1} \overline{P_2}$$

(Hdg = data input to Ig gate)

C-16. SERIAL OUTPUT

$$[Gsg = E_c O_6 O_5 O_4 \overline{O_3} O_2 \overline{O_1} V_g \overline{P_1} \overline{P_2}$$

$$[Gdg = F_g$$

## D. INPUT/OUTPUT CONNECTORS

### D-1. FLEXOWRITER INPUT (ONE CONNECTOR)

1. Type inputs:  $\textcircled{T1}$   $\textcircled{T2}$   $\textcircled{T3}$   $\textcircled{T4}$   $\textcircled{T5}$   $\textcircled{T6}$   $\textcircled{Tc}$
2. Reader inputs:  $\textcircled{R1}$   $\textcircled{R2}$   $\textcircled{R3}$   $\textcircled{R4}$   $\textcircled{R5}$   $\textcircled{R6}$   $\textcircled{R7}$   $\textcircled{R8}$   $\textcircled{Rc}$   $\textcircled{\overline{Rc}}$
3. Return for T's: (  $\textcircled{En}$  +  $\overline{Rf}$   $\overline{Tf}$  )
4. Return for R's: (  $Rf$   $\overline{Tf}$  )
5. Typewriter busy signal:  $\textcircled{Tb}$
6. ENABLE switch:  $\textcircled{En}$   $\textcircled{\overline{En}}$
7. BREAK POINT switch:  $\textcircled{Bp}$
8. Signal ground

### D-2. FLEXOWRITER OUTPUT (ONE CONNECTOR)

1. Translator drivers:  $LTC = Tg$   
 $LT1 = L1 Tg$   
 $LT2 = L2 Tg$   
 $LT3 = L3 Tg$   
 $LT4 = L4 Tg$   
 $LT5 = L5 Tg$   
 $LT6 = O1 Tg$
2. Punch drivers:  $LPC = Pg$   
 $LP1 = L1 Pg$   
 $LP2 = L2 Pg$   
 $LP3 = L3 Pg$   
 $LP4 = L4 Pg$

LP5 = L5 Pg

LP6 = O1 Pg

LP7 = O2 Pg

LP8 = O3 Pg

3. Reader release magnet: LR = Rf  $\overline{Tf}$
4. Type light:  $\overline{Rf Tf}$
5. -48v

D-3. CHARACTER INPUT PHOTO READER (ONE CONNECTOR)

1. Input signal: (S1) (S2) (S3) (S4) (S5) (S6) (S7) (S8)
2. Sprocket signal: (Sc) to be connected to jump input, (J28)
3. Start and Stop control: K3, K2, K1, L1, L2, L3, L4, L5, Cpg.
4. Gate signal: (Rf Tf).
5. + 6v, 0v, -12v.

D-4. CHARACTER INPUT MAGNETIC TAPE READER (ONE CONNECTOR)

1. Input signal: (U1) (U2) (U3) (U4) (U5) (U6) (U7) (U8)
2. Clock signal: (Uc) to be connected to jump input, (J27)
3. Start and Stop control: K3, K2, K1, L1, L2, L3, L4, L5, Cpg
4. Gate signal: (Rf Tf).
5. + 6v, 0v, -12v.

D-5. CHARACTER OUTPUT (TWO CONNECTORS)

1. Destination: K3, K2, K1
2. Code: L1, L2, L3, L4, L5, O1 O2 O3
3. Execute: Cog
4. Gnd, + 6v, -12v

D-6. CONTROL PULSE OUTPUT (TWO CONNECTORS)

1. Destination: K3, K2, K1
2. Code: L1, L2, L3, L4, L5
3. Gnd, +6v, -12v
4. Execute: Cpg

D-7. SERIAL INPUT/OUTPUT (ONE CONNECTOR)

1. Source code: K3, K2, K1
2. Input shift signal: Hsg
3. Input data signal: Hdg
4. Clock signal, ground
5. Output shift signal: Gsg
6. Output data signal: Gdg

D-8. MEMORY ACCESSORY (ONE CONNECTOR)

1. Selector signals: M2g, M3g, (M4g, M5g, M6g, M7g optional)  
N0g, N1g, N2g, N3g, N4g, N5g, N6g, N7g
2. Write command: Wg
3. Write data: Ig,  $\overline{\text{Ig}}$
4. Read data: Fxg
5. Sync signals (optional): Cpg, M0g, N0g, F5
6. Clock signal: + 6v, 0v, -12v

D-9. JUMP CONTROL INPUTS (FOUR CONNECTORS)

- Connector 1: (J0), (J1), (J2), (J3), (J4), (J5), (J6), (J7), gnd
- Connector 2: (J8), (J9), (J10), (J11), (J12), (J13), (J14), (J15), gnd
- Connector 3: (J16), (J17), (J18), (J19), (J20), (J21), (J22), (J23), gnd
- Connector 4: (J24), (J25), (J26), (J27), (J28), gnd

D-10. BOOTSTRAP INPUT CONNECTOR (ONE CONNECTOR)

1. Input Character:  $\textcircled{B6}$  ,  $\textcircled{B5}$  ,  $\textcircled{B4}$  ,  $\textcircled{B1}$  .
2. Mechanical reader control levels:  $\textcircled{Mr}$  ,  $\textcircled{\overline{Mr}}$  .
3. Bootstrap Start, Bootstrap Stop.
4. Gnd, - 12v.
5.  $\textcircled{R1}$  ,  $\textcircled{R4}$  ,  $\textcircled{\overline{Rc}}$  ,  $\textcircled{Rc}$  .
6.  $\textcircled{S1}$  ,  $\textcircled{S4}$  ,  $\textcircled{S5}$  ,  $\textcircled{S6}$  , Photo Start, Photo Stop.
7.  $\textcircled{U1}$  ,  $\textcircled{U4}$  ,  $\textcircled{U5}$  ,  $\textcircled{U6}$  , Mag Start, Mag Stop.

## E. INDICATOR PANEL

### E-1. SWITCHES

- a. Power : on-off
- b. TEST : TEST 1 - TEST 2
- c. FILL : FILL on  $\textcircled{\text{Fi}}$  FILL off  $\textcircled{\overline{\text{Fi}}}$

### E-2. INDICATORS

- a. POWER : light on
- b. COMMAND Line : K3, K2, K1
- c. OPERAND Line : L5, L4, L3, L2, L1
- d. OPERATION Code : O6, O5, O4, O3, O2, O1
- e. PARITY : Pc
- f. O'FLOW : Of

$\left. \begin{aligned} sSw &= \overline{S_c} S_r \overline{Q_g} \\ rSw &= \overline{S_c} \overline{S_r} \overline{B_g} \end{aligned} \right\}$	Recirculates buffer section (P7-P24) of sector counter.
$sSc = \overline{F_5} F_3 F_2 F_1$	Sets carry flip-flop (Sc) to increment Nc section of sector counter (P7 time)
$\left. \begin{aligned} sSw &= S_c \overline{S_r} \overline{Q_g} \\ rSw &= S_c S_r \end{aligned} \right\}$	Counts Nc section (P15-P8) of sector counter.
$rSc = \overline{S_r} (\overline{F_3} + \overline{F_2} + \overline{F_1})$	Resets carry flip-flop when Sr flip-flop contains a zero (P8-P14 time if Sr).
$\left. \begin{aligned} sSw &= \overline{S_c} S_r \overline{Q_g} \\ rSw &= \overline{S_c} \overline{S_r} \overline{B_g} \end{aligned} \right\}$	Recirculates Nc section (after it is incremented).
$sSc = \overline{F_5} F_3 F_2 F_1$	Sets carry flip-flop (Sc) to increment No section of sector counter (P15 time).
$\left. \begin{aligned} sSw &= S_c \overline{S_r} \overline{Q_g} \\ rSw &= S_c S_r \end{aligned} \right\}$	Counts No section (P23-P16) of sector counter.
$rSc = \overline{S_r} (\overline{F_3} + \overline{F_2} + \overline{F_1})$	Resets carry flip-flop (Sc) when Sr flip-flop contains a zero (P14-P22 time if Sr).
$\left. \begin{aligned} sSw &= \overline{S_c} S_r \overline{Q_g} \\ rSw &= \overline{S_c} \overline{S_r} \overline{B_g} \end{aligned} \right\}$	Recirculates No section (after it is incremented)
$rSc = P23$	Preserves existing information, if any, in the buffer section (P7-P24) by resetting the carry flip-flop at P23. Generally, the Sc flip-flop will be reset before P23 time by the alternate equation; however, it is possible for the Sc flip-flop <u>not</u> to be reset before this time. This situation would occur when the sector counter sections were to be incremented from sector $(377)_8$ to $(000)_8$ . (The last sector-count back to the first.)
$sIs = P24$	

The preceding equations apply in all phases (1, 2, 3 and 4) for the specific functions outlined.

$$rIs = (\overline{Sr} sIw + Sr rIw) [\overline{Ec} \overline{Rc} (P8-P15) + \dots] [\overline{K4} \overline{K3} \overline{K2} \overline{K1} \overline{F5} \overline{F3}]$$

$$sRc = P24 \overline{Ec} \overline{Rc} Is (\overline{En}) + \dots$$

Compares Nc section (P8-P15) of sector counter with the sector address of next command word. This address is contained in the Nc section (P8-P15) of the instruction register.

$$sIw = Ir [\overline{Ec} \overline{Rc} (P8-P15) + \overline{Ec} \overline{Rc} (P16 - P23) + Ec Oc (P8-P15) +$$

Recirculates the Instruction Register during Phase I.

$$(P24-P7) M3g N7g Wg + (\overline{En}) (\overline{T6}) (\overline{T5}) (\overline{T4}) (\overline{T1}) (P8-P15)]$$

$$rIw = (\overline{sIw})$$

$$sIw = Ir (\overline{Ec} + \overline{Rc} + \overline{P8-P15}) (\overline{Ec} + \overline{Rc} + \overline{P16-P23}) (\overline{Ec} + \overline{Oc} + \overline{P8-P15}) (\overline{P24-P7} + \overline{M3g} + \overline{N7g} + \overline{Wg}) (\overline{En}) + (\overline{T6}) + (\overline{T5}) + (\overline{T4}) + (\overline{T1}) + \overline{P8-P15}$$

This represents the equation after it has been through an inverter as indicated by the "overbar" over the original bracketed quantity. The asterisk indicates which terms will have - 12 volts present during Phase I.



$$V_g = \left. \begin{aligned} &\overline{K_4} \overline{K_3} \overline{K_2} \overline{K_1} M_{0r} + \overline{K_4} K_3 \overline{K_2} \overline{K_1} M_{4r} \\ &+ \overline{K_4} \overline{K_3} \overline{K_2} K_1 M_{1r} + \overline{K_4} K_3 \overline{K_2} K_1 M_{5r} \\ &+ \overline{K_4} \overline{K_3} K_2 \overline{K_1} M_{2r} + \overline{K_4} K_3 K_2 \overline{K_1} M_{6r} \\ &+ \overline{K_4} \overline{K_3} K_2 K_1 M_{3r} + \overline{K_4} K_3 K_2 K_1 M_{7r} \end{aligned} \right\} \text{Information from memory Command Word.}$$

$$V_g = (\overline{V_g}) + K_4 K_3 K_2 K_1, M_{10r} + K_4 K_3 K_2 K_1 M_{11r} + \dots + K_4 K_3 K_2 K_1 M_{17r}$$

$$L_g = \overline{E_c} R_c \overline{F_5} (\overline{F_4} + \overline{F_3} \overline{F_2} \overline{F_1}) \overline{P_{24}} \overline{P_1} \quad \text{Shift control gate (P2-P8) for operand line select flip-flops.}$$

$$\left. \begin{aligned} sO_2 &= \overline{E_c} R_c P_2 V_g \\ rO_2 &= \overline{E_c} R_c P_2 \overline{V_g} \end{aligned} \right\} \text{Set by index tag configuration of incoming command word.}$$

$$\left. \begin{aligned} sL_5 &= L_g \overline{O_2} V_g + L_g O_2 I_w \\ rL_5 &= L_g \overline{O_2} \overline{V_g} + L_g O_2 \overline{I_w} \end{aligned} \right\} \text{Receives line number from incoming command word (}\overline{O_2}\text{ flip-flop "false") or index section of instruction register (}O_2\text{ flip-flop "true").}$$

$$\left. \begin{aligned} sL_4 &= L_g L_5 \\ rL_4 &= L_g \overline{L_5} \\ sL_3 &= L_g L_4 \\ rL_3 &= L_g \overline{L_4} \\ sL_2 &= L_g L_3 \\ rL_2 &= L_g \overline{L_3} \\ sL_1 &= L_g L_2 \\ rL_1 &= L_g \overline{L_2} \end{aligned} \right\} \text{Serially shifts line number into operand line select flip-flops during (P2-P8).}$$

$$O_g = \overline{E_c} R_c F_4 \quad \text{Shift control gate (P8-P15) for operation code flip-flops.}$$

$$sO_c = O_g V_g$$

$$rO_c = O_g \overline{V_g}$$

$$sO_6 = O_g O_c$$

$$rO_6 = O_g \overline{O_c}$$

$$sO_5 = O_g O_6$$

$$rO_5 = O_g \overline{O_6}$$

$$sO_4 = O_g O_5$$

$$rO_4 = O_g \overline{O_5}$$

$$sO_3 = O_g O_4$$

$$rO_3 = O_g \overline{O_4}$$

$$sO_2 = O_g O_3$$

$$rO_2 = O_g \overline{O_3}$$

$$sO_1 = O_g O_2$$

$$rO_1 = O_g \overline{O_2}$$

Serially shifts operation code into operand code flip-flops during (P8-P15).

$$sI_w = \overline{E_c} R_c (P15-P8) S_r$$

$$rI_w = (\overline{sI_w})$$

Serially shifts the next instruction address from the Nc section (P8-P15) of the sector counter into the Nc section (P8-P15) of the instruction register.

$$sI_w = \overline{E_c} R_c (P23-P16) V_g$$

$$rI_w = (\overline{sI_w})$$

Serially shifts the operand sector number into the memory section (P16-P23) of the instruction register.

sIs	=	P24	Compares incoming Operand sector number (Vg, which is setting and re-setting Iw during P16-P23) with No section of sector counter (Sr during P16-P23). This will determine whether phase 4 follows phase 2.
rIs	=	( $\overline{S}r$ sIw + Sr rIw)	
		$\left[ \overline{O}5 R_c (P16-P23) + - - - \right]$ $\left[ \overline{K}4 \overline{K}3 \overline{K}2 \overline{K}1 \overline{F}5 F3 \right]$	
sEc	=	P24 $\overline{E}c R_c$	To phase 3
rRc	=	P24 R_c Is	To phase 4

$\overline{E_c} R_c$ 

PARITY ERROR

Detected in phase 2

$$sP_c = \overline{E_c} R_c V_g \overline{P_c} \overline{P_1}$$

$$rP_c = \overline{E_c} R_c V_g P_c \overline{P_1}$$

$$sE_c = \overline{E_c} R_c P_{24}$$

Possibility of phase 3:

$$rR_c = P_{24} R_c I_s$$

$$rE_c = E_c \overline{R_c} P_c P_1$$

To phase 1 only (no  $sR_c$  equation at  $P_1$  of phase 4)

$$sR_c = P_{24} \overline{E_c} \overline{R_c} I_s (\overline{E_n}) + \dots$$

$$rR_c = \overline{E_c} R_c P_1 P_c$$

$$rP_c = (\overline{E_n}) (\overline{B_p})$$

From phase 2 to phase 3 or phase 4, then in phase 4 for one pulse and back to phase 1 until  $I_s$  ( $N_c = N_c$ ) then into phase 2 for one pulse and back to phase 1. If a parity error is detected in this phase and the  $P_c$  flip-flop is reset by the BREAK POINT and ENABLE switches, the command is not executed and is effectively lost because the next command in sequence is picked up for execution.

$E_c \overline{R_c}$ 

PARITY ERROR

Detected in phase 4

$$sP_c = \overline{P_1} E_c \overline{R_c} \overline{O_6} \overline{O_5} O_3 F_g \overline{P_c}$$

$$rP_c = \overline{P_1} E_c \overline{R_c} \overline{O_6} \overline{O_5} O_3 F_g P_c$$

$$E_g = P_{24} E_c \overline{R_c} (\overline{O_5} \overline{O_2} + \overline{O_5} \overline{O_4} \overline{O_1})$$

$$rE_c = E_g$$

Possibility of phase 1 ( $\overline{E_c} \overline{R_c}$ )

$$sR_c = \textcircled{\overline{E_n}} \textcircled{\overline{F_1}} E_g O_c$$

$$+ \textcircled{\overline{E_n}} \textcircled{\overline{F_1}} E_g \overline{O_5} I_s$$

$$sR_c = P_{24} \overline{E_c} \overline{R_c} I_s ( \textcircled{\overline{E_n}} + - - - )$$

Possibility of phase 2

When phase 2 is reached ( $\overline{E_c} R_c$ )

$$rR_c = \overline{E_c} R_c P_c P_1$$

$$rP_c = \textcircled{E_n} \textcircled{B_p}$$

In phase 4 the error is detected, and at the completion of this phase the computer sequences to phase 1 or phase 2. At this point a loop between phase 1 and 2 begins until the  $P_c$  flip-flop is reset by the **BREAK POINT** and **ENABLE** switches. The command has been executed.

 $E_c \overline{R_c}$ 

PARITY GENERATION EQUATIONS

$$I_g = \overline{P_{24}} - - - C_r + \overline{P_{24}} - - - A_r + \overline{P_{24}} - - - B_r \\ + \overline{P_{24}} - - - A_r + \overline{P_{24}} - - - V_g + \overline{P_{24}} - - - V_g H_d g + P_{24} P_c$$

$$sP_c = E_c \overline{R_c} \overline{P_1} \overline{O_5} O_3 I_g \overline{P_c}$$

$$rP_c = E_c \overline{R_c} \overline{P_1} \overline{O_5} O_3 I_g P_c$$

$$E_g = P_{24} E_c \overline{R_c} ( - - - + - - - + - - - )$$

$$rE_c = E_g$$

## MEMORY LINE SELECTION

$M0g = *L0 \overline{L5} \overline{L4}$	$N0g = \overline{L3} \overline{L2} \overline{L1}$
$M1g = \overline{L0} \overline{L5} L4$	$N1g = \overline{L3} \overline{L2} L1$
$M2g = \overline{L0} L5 \overline{L4}$	$N2g = \overline{L3} L2 \overline{L1}$
$M3g = \overline{L0} L5 L4$	$N3g = \overline{L3} L2 L1$
$*M4g = L0 \overline{L5} \overline{L4}$	$N4g = L3 \overline{L2} \overline{L1}$
$*M5g = L0 \overline{L5} L4$	$N5g = L3 \overline{L2} L1$
$*M6g = L0 L5 \overline{L4}$	$N6g = L3 L2 \overline{L1}$
$*M7g = L0 L5 L4$	$N7g = L3 L2 L1$

$$Fg = M0g N0g M0r + M0g N1g M1r + M0g N2g M2r + M0g N3g M3r$$

$$+ M0g N4g M4r + M0g N5g M5r + M0g N6g M6r + M0g N7g M7r$$

$$+ M1g N0g M8r + M1g N1g M9r + (\text{etc. , except for line 31}) + M7g N7g M6 3r$$

$$+ M3g N7g Ir (\text{Index line}) + Fxg$$
  

$$\overline{Fg} = (\overline{Fg})$$

The following notation appears in the summary:

$$Fg = Mig Nig Mir$$

This notation is used to indicate the selected memory line which is feeding the Fg (Fetch) Gate. The (i) indicates the particular gate or component number that is being used.

---

\*L0 and M4g through M7g are options for memory expansion.

$\overline{E}c R_c$

00\* HALT

(HLT)

$sE_c = P24 \overline{E}c R_c$

$sP_c = E_c R_c \overline{O6} \overline{O5} \overline{O4} \overline{O3} \overline{O2} \overline{O1} \longrightarrow$  Phase 3

$rR_c = P24 R_c I_s \longrightarrow$  Phase 3

$rE_c = E_c \overline{R}c P_c P1 \longrightarrow$  Phase 4

$sR_c = P24 \overline{E}c \overline{R}c I_s ( \textcircled{\overline{E}n} + - - - ) \longrightarrow$  Phase 1

$rR_c = \overline{E}c R_c P_c P1 \longrightarrow$  Phase 2

$rP_c = \textcircled{\overline{E}n} \textcircled{Bp}$

Limitation: Ms number associated with halt command must be other than a + 1 address.

Definition. Computer goes from phase 2 to phase 3 until  $I_s$  ( $M_s = N_o$ ) ( $P_c$  flip-flop is being set) then into phase 4 for one pulse. Phase 1 is next and continues until  $I_s$  ( $N_c = N_c$ ) then into phase 2 for one pulse and back to phase 1 - - loops between phase 1 and 2.

---

\*Indicates that operation code has at least two meanings, depending on the address used with the command.

$\overline{E}c R_c$

00\* MERGE ( $M_s = a + 1$ )

(MAC)

$$sE_c = P24 \overline{E}c R_c$$

No possibility of phase 3 ( $M_s = a + 1$ )

$$rR_c = P24 R_c I_s$$

$$I_g = \overline{P24} \overline{O5} \overline{O2} \overline{O1} C_r + \dots + \overline{P24} \overline{O4} \overline{O2} A_r + \dots$$

$$sC_w = E_c \overline{R_c} \overline{O6} \overline{O5} \overline{O4} \overline{O3} I_g$$

$$rC_w = (\overline{sC_w})$$

$$E_g = P24 E_c \overline{R_c} (\overline{O5} \overline{O2} + \overline{O5} \overline{O3} \overline{O1} + \overline{O5} \overline{O4} \overline{O1}) + \dots$$

$$rE_c = E_g$$

Limitation:  $M_s$  number associated with halt command must be  $a + 1$  address.

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\*Indicates that operation code has at least two meanings, depending on the address used with the command.



$\overline{Ec} R_c$ 

01 INTERCHANGE A AND C

(IAC)

$$sEc = P24 \overline{Ec} R_c$$

Possibility of phase 3:

$$rRc = P24 R_c Is$$

$$I_g = - - - + \overline{P24 O6 O2 O1 Ar} + - - - + \overline{P24 O4 O2} Ar + P24 Pc$$

$$\overline{I_g} = (\overline{I_g})$$

$$sCw = Ec \overline{Rc O6 O5 O4 O3} I_g$$

$$rCw = (\overline{sCw})$$

$$sAw = - - - + Ec \overline{Rc O6 O5 O4 O3 O2 O1 Cr}$$

$$rAw = (\overline{sAw})$$

$$Eg = P24 Ec \overline{Rc (O5 O2 + - - -)}$$

$$rEc = Eg$$

$\overline{Ec} R_c$ 

02 INTERCHANGE B AND C

(IBC)

$$sEc = P24 \overline{Ec} R_c$$

Possibility of phase 3:

$$rRc = P24 R_c Is$$

$$Ig = \overline{P24} \overline{O6} O2 Br + P24 Pc$$

$$\overline{Ig} = (\overline{Ig})$$

$$sCw = Ec \overline{Rc} \overline{O6} \overline{O5} \overline{O4} \overline{O3} Ig$$

$$rCw = (\overline{sCw})$$

$$sBw = Ec \overline{Rc} \overline{O6} \overline{O5} \overline{O4} \overline{O3} O2 Cr$$

$$rBw = (\overline{sBw})$$

$$Eg = P24 Ec \overline{Rc} (\overline{O5} \overline{O3} \overline{O1} + \overline{O5} \overline{O4} \overline{O1} + \dots)$$

$$rEc = Eg$$

$\overline{Ec} R_c$ 

03 → 01 ROTATE

(ROT)

$$sEc = P24 \overline{Ec} R_c$$

Possibility of phase 3:

$$rRc = P24 R_c Is$$

$$I_g = \overline{P24} \overline{O6} O2 Br + P24 Pc$$

$$\overline{I_g} = (\overline{I_g})$$

$$sCw = Ec \overline{Rc} \overline{O6} \overline{O5} \overline{O4} \overline{O3} I_g$$

$$rCw = (\overline{sCw})$$

$$sBw = Ec \overline{Rc} \overline{O6} \overline{O5} \overline{O4} \overline{O3} O2 Cr$$

$$rBw = (\overline{sBw})$$

$$rO2 = P24 Ec \overline{Rc} \overline{O6} \overline{O5} O1$$

$$I_g = (\overline{P24} \overline{O6} \overline{O2} O1 + \overline{P24} \overline{O4} \overline{O2}) Ar + - - + P24 Pc$$

$$\overline{I_g} = (\overline{I_g})$$

$$sCw = Ec \overline{Rc} \overline{O6} \overline{O5} \overline{O4} \overline{O3} I_g$$

$$rCw = (\overline{sCw})$$

$$sAw = Ec \overline{Rc} \overline{O6} \overline{O5} \overline{O4} \overline{O3} \overline{O2} O1 Cr + - - -$$

$$rAw = (\overline{sAw})$$

$$Eg = P24 Ec \overline{Rc} (\overline{O5} \overline{O2} + - - -)$$

$$rEc = Eg$$

$\overline{E_c} R_c$

04 LOAD C

(LDC)

$$sE_c = P24 \overline{E_c} R_c$$

Possibility of phase 3:

$$rR_c = P24 R_c I_s$$

$$F_g = M_{ig} N_{ig} M_{ir}$$

$$\overline{F_g} = (\overline{F_g})$$

$$sC_w = E_c \overline{R_c} \overline{O_6} \overline{O_5} \overline{O_4} \overline{O_3} \overline{O_2} \overline{O_1} F_g$$

$$rC_w = (\overline{sC_w})$$

$$E_g = P24 E_c \overline{R_c} (\overline{O_5} \overline{O_2} + \overline{O_5} \overline{O_4} \overline{O_1} + \dots)$$

$$rE_c = E_g$$

$\overline{Ec} R_c$

05 LOAD A

(LDA)

$$sEc = P24 \overline{Ec} R_c$$

Possibility of phase 3:

$$rRc = P24 R_c Is$$

$$Fg = Mig Nig Mir$$

$$\overline{Fg} = (\overline{Fg})$$

$$sAw = Ec \overline{Rc} \overline{O6} \overline{O4} O3 \overline{O2} O1 Fg$$

$$rAw = (\overline{sAw})$$

$$Eg = P24 Ec \overline{Rc} (\overline{O5} \overline{O2} + \dots)$$

$$rEc = Fg$$

$\overline{E_c R_c}$

06 LOAD B

(LDB)

$$sE_c = P24 \overline{E_c R_c}$$

Possibility of phase 3:

$$R_c = P24 R_c I_s$$

$$F_g = \text{Mig Nig Mir}$$

$$\overline{F_g} = (\overline{F_g})$$

$$sB_w = E_c \overline{R_c} \overline{O_6} \overline{O_5} \overline{O_4} \overline{O_3} \overline{O_2} F_g$$

$$rB_w = (\overline{sB_w})$$

$$E_g = P24 E_c \overline{R_c} (\overline{O_5} \overline{O_4} \overline{O_1} + - - -)$$

$$rE_c = E_g$$

$\overline{E}c Rc$

07 → 05 LOAD DOUBLE PRECISION

(LDP)

$$sEc = P24 \overline{E}c Rc$$

Possibility of phase 3:

$$rRc = P24 Rc Is$$

$$Fg = Mig Nig Mir$$

$$\overline{Fg} = (\overline{Fg})$$

$$sBw = Ec \overline{Rc} \overline{O6} \overline{O5} \overline{O4} O3 O2 Fg + - - -$$

$$rBw = (\overline{sBw})$$

$$rO2 = P24 Ec \overline{Rc} \overline{O6} \overline{O5} O1 + - - -$$

$$sAw = Ec \overline{Rc} \overline{O6} \overline{O4} O3 \overline{O2} O1 Fg$$

$$rAw = (\overline{sAw})$$

$$Eg = P24 Ec \overline{Rc} (\overline{O5} \overline{O2} + - - -)$$

$$rEc = Eg$$

$\overline{E}c R_c$

10 STORE C

(STC)

$$sEc = P24 \overline{E}c R_c$$

Possibility of phase 3:

$$rRc = P24 R_c I_s$$

$$I_g = \overline{P24} \overline{O5} \overline{O2} \overline{O1} Cr + - - - + P24 Pc$$

$$\overline{I}g = (\overline{I}g)$$

$$Wg = Ec \overline{R}c (\overline{O6} \overline{O5} O4 \overline{O3} + - - -)$$

$$sMiw = Mig Nig Wg I_g + \boxed{Mig Nig Wg} \boxed{Mir}$$

$$rMiw = Mig Nig Wg \overline{I}g + \boxed{Mig Nig Wg} \boxed{Mir}$$

$$Eg = P24 Ec \overline{R}c (\overline{O5} \overline{O2} + \overline{O5} \overline{O3} \overline{O1} + - - -)$$

$$rEc = Eg$$



$\overline{E}c R_c$ 

11 STORE A

(STA)

$$sEc = P24 \overline{E}c R_c$$

Possibility of phase 3:

$$rRc = P24 R_c Is$$

$$I_g = \overline{P24} \overline{O6} \overline{O2} O1 Ar + \overline{P24} \overline{O4} \overline{O2} Ar + \dots + P24 Pc$$

$$\overline{I}g = (\overline{I}g)$$

$$Wg = Ec \overline{R}c (\overline{O6} \overline{O5} O4 \overline{O3} + \dots)$$

$$sMiw = Mig Nig Wg Ig + \boxed{Mig Nig Wg} \boxed{Mir}$$

$$rMiw = Mig Nig Wg \overline{I}g + \boxed{Mig Nig Wg} \boxed{Mir}$$

$$Eg = P24 Ec \overline{R}c (\overline{O5} \overline{O2} + \dots)$$

$$rEc = Eg$$

$\overline{E_c} R_c$ 

12 STORE B

(STB)

$$sE_c = P24 \overline{E_c} R_c$$

Possibility of phase 3:

$$rR_c = P24 R_c I_s$$

$$I_g = \overline{P24} \overline{O_6} O_2 B_r + \dots + P24 P_c$$

$$\overline{I_g} = (\overline{I_g})$$

$$W_g = E_c \overline{R_c} (\overline{O_6} \overline{O_5} O_4 \overline{O_3} + \dots)$$

$$sM_{iw} = Mig Nig W_g I_g + \boxed{\overline{Mig Nig W_g}} \boxed{Mir}$$

$$rM_{iw} = Mig Nig W_g \overline{I_g} + \boxed{\overline{Mig Nig W_g}} \boxed{\overline{Mir}}$$

$$E_g = P24 E_c \overline{R_c} (\overline{O_5} \overline{O_3} \overline{O_1} + \dots)$$

$$rE_c = E_g$$

$$sEc = P24 \overline{Ec} R_c$$

Possibility of phase 3:

$$rRc = P24 R_c I_s$$

$$I_g = \overline{P24} \overline{O6} O2 Br + - - - + P24 Pc$$

$$\overline{I_g} = (\overline{I_g})$$

$$W_g = Ec \overline{Rc} (\overline{O6} \overline{O5} O4 \overline{O3} + - - -)$$

$$sMiw = Mig Nig Wg I_g + \boxed{Mig Nig Wg} \boxed{Mir}$$

$$rMiw = Mig Nig Wg \overline{I_g} + \boxed{Mig Nig Wg} \boxed{\overline{Mir}}$$

$$rO2 = P24 Ec \overline{Rc} \overline{O6} \overline{O5} O1$$

$$I_g = \overline{P24} \overline{O6} \overline{O2} O1 Ar + - - - + P24 Pc$$

$$\overline{I_g} = (\overline{I_g})$$

$$sMiw = Mig Nig Wg I_g + \boxed{Mig Nig Wg} \boxed{Mir}$$

$$rMiw = Mig Nig Wg \overline{I_g} + \boxed{Mig Nig Wg} \boxed{\overline{Mir}}$$

$$Eg = P24 Ec \overline{Rc} (\overline{O5} \overline{O2} + - - -)$$

$$rEc = Eg$$

$\overline{\text{Ec}} \text{ Rc}$

14 ADD

(ADD)

$\text{Fg} = \text{Mig Nig Mir}$

$\overline{\text{Fg}} = (\overline{\text{Fg}})$

$\text{Xg} = \overline{\text{O5 O1}} \text{ Fg}$

$\overline{\text{Xg}} = (\overline{\text{Xg}})$

$\text{Yg} = \overline{\text{O6 O4 O2}} \text{ Ar}$

$\overline{\text{Yg}} = (\overline{\text{Yg}})$

$\text{sEc} = \text{P24 } \overline{\text{Ec}} \text{ Rc}$

Possibility of phase 3:

$\text{rCa} = \text{Ca Rc}$

$\text{rRc} = \text{P24 Rc Is}$

$\text{Zg} = (\overline{\overline{\text{Zg}}})$

$\overline{\text{Zg}} = \text{Xg Yg } \overline{\text{Ca}} + \text{Xg } \overline{\text{Yg}} \text{ Ca} + \overline{\text{Xg}} \text{ Yg Ca} + \overline{\text{Xg}} \overline{\text{Yg}} \overline{\text{Ca}}$

$\text{sCa} = \overline{\text{P1 P24 Ec Rc Xg Yg } \overline{\text{Ca}}}$

$\text{rCa} = \overline{\text{P1 P24 Xg Yg}}$

$\text{sOf} = \text{P23 Ec } \overline{\text{Rc}} \overline{\text{O6 O5 O4 O3 O2}} (\overline{\text{Xg}} \overline{\text{Yg}} \text{ Ca} + \text{Xg Yg } \overline{\text{Ca}})$

$\text{sAw} = \text{Ec } \overline{\text{Rc}} \overline{\text{O6 O5 O4 O3 O2}} \text{ Zg}$

$\text{rAw} = (\overline{\text{sAw}})$

$\text{Eg} = \text{P24 Ec } \overline{\text{Rc}} (\overline{\text{O5 O2}} + - - -)$

$\text{rEc} = \text{Eg}$

$\overline{E}c R_c$ 

15 SUBTRACT

(SUB)

 $Fg = Mig Nig Mir$  $\overline{F}g = (\overline{F}g)$  $Xg = \overline{O5} O1 \overline{F}g$  $\overline{X}g = (\overline{X}g)$  $Yg = \overline{O6} O4 \overline{O2} Ar$  $\overline{Y}g = (\overline{Y}g)$  $sEc = P24 \overline{E}c R_c$ 

Possibility of phase 3:

 $rCa = Ca R_c$  $sCa = P24 R_c Is \overline{O6} \overline{O5} O4 O3 O1$  $rRc = P24 R_c Is$  $Zg = (\overline{Z}g)$  $\overline{Z}g = Xg Yg \overline{Ca} + Xg \overline{Y}g Ca + \overline{X}g Yg Ca + \overline{X}g \overline{Y}g \overline{Ca}$  $sCa = \overline{P1} \overline{P24} Ec \overline{Rc} Xg Yg \overline{Ca}$  $rCa = \overline{P1} \overline{P24} \overline{X}g \overline{Y}g$  $sOf = P23 Ec \overline{Rc} \overline{O6} \overline{O5} O4 O3 \overline{O2} (\overline{X}g \overline{Y}g Ca + Xg Yg \overline{Ca})$  $sAw = Ec \overline{Rc} \overline{O6} \overline{O5} O4 O3 \overline{O2} Zg$  $rAw = (\overline{sAw})$  $Eg = P24 Ec \overline{Rc} (\overline{O5} \overline{O2} + - - -)$

$\overline{E}c R_c$ 16  $\longrightarrow$  14 DOUBLE PRECISION ADD

(DPA)

 $F_g = \text{Mig Nig Mir}$  $\overline{F}_g = (\overline{F}_g)$  $X_g = \overline{O5} \overline{O1} F_g$  $\overline{X}_g = (\overline{X}_g)$  $Y_g = \overline{O5} O2 Br$  $\overline{Y}_g = (\overline{Y}_g)$  $sEc = P24 \overline{E}c R_c$ 

Possibility of phase 3:

 $rCa = Ca R_c$  $rRc = P24 R_c Is$  $Z_g = (\overline{Z}_g)$  $Z_g = X_g Y_g \overline{Ca} + X_g \overline{Y}_g Ca + \overline{X}_g Y_g Ca + \overline{X}_g \overline{Y}_g \overline{Ca}$  $sCa = \overline{P1} \overline{P24} Ec \overline{Rc} X_g Y_g \overline{Ca}$  $rCa = \overline{P1} \overline{P24} \overline{X}_g \overline{Y}_g$  $sBw = Ec \overline{Rc} \overline{O6} \overline{O5} O4 O3 O2 Z_g$  $rBw = (\overline{sBw})$  $rO2 = P24 Ec \overline{Rc} \overline{O6} \overline{O5} O4 O3$  $Y_g = \overline{O6} O4 \overline{O2} Ar$  $\overline{Y}_g = (\overline{Y}_g)$  $sAw = Ec \overline{Rc} \overline{O6} \overline{O5} O4 O3 \overline{O2} Z_g$  $rAw = (\overline{sAw})$  $sOf = P23 Ec \overline{Rc} \overline{O6} \overline{O5} O4 O3 \overline{O2} (\overline{X}_g \overline{Y}_g Ca + X_g Y_g \overline{Ca})$  $Eg = P24 Ec \overline{Rc} (\overline{O5} \overline{O2} + \dots)$  $rEc = Eg$

$\text{Fg} = \text{Mig Nig Mir}$

$\overline{\text{Fg}} = (\overline{\text{Fg}})$

$\text{Xg} = \overline{\text{O5 O1 Fg}}$

$\overline{\text{Xg}} = (\overline{\text{Xg}})$

$\text{Yg} = \overline{\text{O5 O2 Br}}$

$\overline{\text{Yg}} = (\overline{\text{Yg}})$

$\text{sEc} = \text{P24 } \overline{\text{Ec}} \text{ Rc}$

Possibility of phase 3:

$\text{rCa} = \text{Ca Rc}$

$\text{sCa} = \text{P24 Rc Is } \overline{\text{O6 O5 O4 O3 O1}}$

$\text{rRc} = \text{P24 Rc Is}$

$\text{Zg} = (\overline{\overline{\text{Zg}}})$

$\overline{\text{Zg}} = \text{Xg Yg } \overline{\text{Ca}} + \text{Xg } \overline{\text{Yg}} \text{ Ca} + \overline{\text{Xg}} \text{ Yg Ca} + \overline{\text{Xg}} \overline{\text{Yg}} \overline{\text{Ca}}$

$\text{sCa} = \overline{\text{P1 P24 Ec Rc Xg Yg } \overline{\text{Ca}}}$

$\text{rCa} = \overline{\text{P1 P24 } \overline{\text{Xg Yg}}}$

$\text{sBw} = \text{Ec } \overline{\text{Rc O6 O5 O4 O3 O2 Zg}}$

$\text{rBw} = (\overline{\text{sBw}})$

$\text{rO2} = \text{P24 Ec } \overline{\text{Rc O6 O5 O4 O3}} + \text{P24 Ec } \overline{\text{Rc O6 O5 O1}}$

$\text{Yg} = \overline{\text{O6 O4 O2 Ar}}$

$\overline{\text{Yg}} = (\overline{\text{Yg}})$

$\text{sAw} = \text{Ec } \overline{\text{Rc O6 O5 O4 O3 O2 Zg}}$

$\text{rAw} = (\overline{\text{sAw}})$

$\text{sOf} = \text{P23 Ec } \overline{\text{Rc O6 O5 O4 O3 O2}} (\overline{\text{Xg Yg Ca}} + \text{Xg Yg } \overline{\text{Ca}})$

$\text{Eg} = \text{P24 Ec } \overline{\text{Rc}} (\overline{\text{O5 O2}} + \dots)$

$\text{rEc} = \text{Eg}$

$\overline{E}c R_c$ 

## 20\* NORMALIZE AND DECREMENT

(NAD)

$$\left. \begin{aligned} sL3 &= \overline{O6} O5 \overline{O3} P24 Bw \\ rL3 &= \overline{O6} O5 \overline{O3} P24 \overline{Bw} \end{aligned} \right\}$$

Coupling flip-flops between P23 of B register and P2 of A register.

$$sEc = P24 \overline{E}c R_c$$

$$rRc = P24 R_c Is$$

No possibility of phase 3: (O5 Command)

$$\left. \begin{aligned} sL2 &= \overline{O6} O5 \overline{O3} \overline{O2} Ec Br \\ rL2 &= \overline{O6} O5 \overline{O3} \overline{O2} Ec \overline{Br} \end{aligned} \right\}$$

Delay flip-flop for B register.

$$\left. \begin{aligned} sBw &= Ec \overline{Rc} \overline{O6} O5 \overline{O4} \overline{O3} \overline{O2} \overline{P2} L2 \\ &+ \overline{P1} Br \left[ Ec \overline{Rc} (\overline{O6} O5 \overline{O3} + - - -) \right] \end{aligned} \right\}$$

Left shifts B register.

$$rBw = (\overline{sBw})$$

$$\left. \begin{aligned} sL1 &= \overline{O6} O5 \overline{O4} \overline{O3} \overline{O2} Ec Ar \\ rL1 &= \overline{O6} O5 \overline{O4} \overline{O3} \overline{O2} Ec \overline{Ar} \end{aligned} \right\}$$

Delay flip-flop for A register.

$$sAw = Ec \overline{Rc} \overline{O6} O5 \overline{O3} \overline{O2} P2 L3$$

Transfers P23 bit configuration of B register to P2 position of A register.

$$+ Ec \overline{Rc} \overline{O6} O5 \overline{O3} \overline{O2} \overline{P23} \overline{P2} L1$$

Left shifts A register.

$$+ P23 \overline{O6} O5 \overline{O4} \overline{O3} Ar$$

Recirculates sign of A register.

$$+ Ar \left[ Ec \overline{Rc} (\overline{O6} O5 \overline{O3} + - - -) \right]$$

Recirculates A register if shifting stops.

$$rAw = (\overline{sAw})$$

$$rCa = O5 P24$$

$$Xg = O5 \overline{O4} \overline{O3} (\overline{O2} + P2) \overline{L4}$$

$$\overline{Xg} = (\overline{Xg})$$

\*Indicates that operation code has at least two meanings, depending on address used with the command.



$$Yg = O5 \overline{O4} Cr$$

$$\overline{Yg} = (\overline{Yg})$$

$$Zg = (\overline{Zg})$$

$$\overline{Zg} = Xg Yg \overline{Ca} + Xg \overline{Yg} Ca + \overline{Xg} Yg Ca + \overline{Xg} \overline{Yg} \overline{Ca}$$

$$sCa = \overline{P1} \overline{P24} Ec \overline{Rc} Xg Yg \overline{Ca}$$

$$rCa = \overline{P1} \overline{P24} \overline{Xg} \overline{Yg}$$

$$sCw = Ec \overline{Rc} O5 \overline{O4} Zg$$

$$rCw = (\overline{sCw})$$

$$sO3 = P23 \overline{O6} O5 \overline{O4} \overline{O3} \overline{O2} \overline{O1} (Aw \overline{Ar} + \overline{Aw} Ar)$$

If these conditions occur, O3 is set. This stops the shifting operation and C register logic in phase 4; the computer remains in phase 4 until Is (Ms = No) with the A and B registers recirculating normally and the C register recirculating normally through the adder gates.

$$sIs = P24$$

$$rIs = (\overline{Sr} sIw + Sr rIw) \left[ Ec O5 (P23-P16) + - - - \right] \overline{\left[ \overline{K4} \overline{K3} \overline{K2} \overline{K1} \overline{F5} \overline{F3} \right]}$$

$$Eg = P24 Ec Rc (O5 Is + - - -)$$

$$rEc = Eg$$

#### 20\* NORMALIZE

Whether the C register is decremented or not is a function of the line number used with the command. If the line number has a zero in the position corresponding to the L4 flip-flops' configuration, the C register is decremented. If the C register has a one in the position corresponding to the L4 flip-flops' configuration, the C register is recirculated normally via the adder.

\*Indicates that operation code has at least two meanings, depending on address used with the command.

$\overline{E_c} R_c$ 

## 21\* LEFT SHIFT AND DECREMENT

(LSD)

$$\left. \begin{aligned} sL3 &= \overline{O_6} O_5 \overline{O_3} P_{24} B_w \\ rL3 &= \overline{O_6} O_5 \overline{O_3} P_{24} \overline{B_w} \end{aligned} \right\}$$

Coupling flip-flop between P23 of B register and P2 of A register.

$$sE_c = P_{24} \overline{E_c} R_c$$

$$rR_c = P_{24} R_c I_s$$

No possibility of phase 3: (O5 Command)

$$\left. \begin{aligned} sL2 &= \overline{O_6} O_5 \overline{O_3} \overline{O_2} E_c B_r \\ rL2 &= \overline{O_6} O_5 \overline{O_3} \overline{O_2} E_c \overline{B_r} \end{aligned} \right\}$$

Delay flip-flop for B register.

$$\left. \begin{aligned} sB_w &= E_c \overline{R_c} \overline{O_6} O_5 \overline{O_4} \overline{O_3} \overline{O_2} \overline{P_2} L_2 \\ rB_w &= (\overline{sB_w}) \end{aligned} \right\}$$

Left shifts B register.

$$\left. \begin{aligned} sL1 &= \overline{O_6} O_5 \overline{O_4} \overline{O_3} \overline{O_2} E_c A_r \\ rL1 &= \overline{O_6} O_5 \overline{O_4} \overline{O_3} \overline{O_2} E_c \overline{A_r} \end{aligned} \right\}$$

Delay flip-flop for A register.

$$sA_w = E_c \overline{R_c} \overline{O_6} O_5 \overline{O_3} \overline{O_2} P_2 L_3 \longrightarrow \text{Transfers P23 bit configuration of B register to P2 position of A register.}$$

$$+ E_c \overline{R_c} \overline{O_6} O_5 \overline{O_3} \overline{O_2} \overline{P_2} \overline{P_2} L_1 \longrightarrow \text{Left shifts A register.}$$

$$+ P_2 \overline{O_6} O_5 \overline{O_4} \overline{O_3} A_r \longrightarrow \text{Recirculates sign of A register.}$$

$$rA_w = (\overline{sA_w})$$

$$rC_a = O_5 P_{24}$$

$$X_g = O_5 \overline{O_4} \overline{O_3} (\overline{O_2} + P_2) \overline{L_4}$$

$$\overline{X_g} = (\overline{X_g})$$

$$Y_g = O_5 \overline{O_4} C_r$$

$$\overline{Y_g} = (\overline{Y_g})$$

\*Indicates that the operation code has at least two meanings, depending on the address used with the command.

$\overline{E_c R_c}$                       21\* LEFT SHIFT AND DECREMENT (continued)                      (LSD)

$$Z_g = \overline{Z_g}$$

$$\overline{Z_g} = X_g Y_g \overline{C_a} + X_g \overline{Y_g} C_a + \overline{X_g} Y_g C_a + \overline{X_g} \overline{Y_g} \overline{C_a}$$

$$sC_a = \overline{P_1} \overline{P_{24}} \overline{E_c} \overline{R_c} X_g Y_g \overline{C_a}$$

$$rC_a = \overline{P_1} \overline{P_{24}} \overline{X_g} \overline{Y_g}$$

$$sC_w = E_c \overline{R_c} O_5 \overline{O_4} Z_g$$

$$rC_w = \overline{sC_w}$$

$$sI_s = P_{24}$$

$$rI_s = (\overline{S_r} sI_w + S_r rI_w) \left[ E_c O_5 (P_{23}-P_{16}) + - \right] \overline{[K_4 K_3 K_2 K_1 F_5 F_3]}$$

$$E_g = P_{24} \overline{E_c} \overline{R_c} (O_5 I_s + - - -)$$

$$rE_c = E_g$$

$\overline{E_c} R_c$                       21\* SHIFT LEFT (AB LEFT)                      (SLT)

The equations used for left shift and decrement (LSD) and shift left (SLT) are the same. Whether the C register is decremented or not is a function of the line number used with the command. If the line number has a zero in the position corresponding to the L4 flip-flops' configuration, the C register is decremented. If the line number has a one in the position corresponding to the L4 flip-flops' configuration, the C register is recirculated normally via the adder.

---

\*Indicates that the operation code has least two meanings, depending on the address used with the command.

$\overline{E}c R_c$ 

## 22 \* RIGHT SHIFT AND INCREMENT

(RSI)

$$sEc = P24 \overline{E}c R_c$$

$$rRc = P24 R_c Is$$

No possibility of phase 3: ( O5 Command )

$$sL3 = \overline{O6} O5 \overline{O3} P2 Ar$$

$$rL3 = \overline{O6} O5 \overline{O3} P2 \overline{Ar}$$

$$sBw = Ec \overline{Rc} \overline{O6} O5 \overline{O3} O2 \overline{P23} Be + Ec \overline{Rc} \overline{O6} O5 \overline{O3} O2 P23 L3$$

$$rBw = ( \overline{sBw} )$$

$$sAw = Ec \overline{Rc} \overline{O6} O5 \overline{O4} \overline{O3} O2 \overline{P23} Ae + \overline{O6} O5 \overline{O4} \overline{O3} P23 Ar$$

$$rAw = ( \overline{sAw} )$$

$$rCa = O5 P24$$

$$Xg = O5 \overline{O4} \overline{O3} (\overline{O2} + P2) \overline{L4}$$

$$\overline{Xg} = (\overline{Xg})$$

$$Yg = O5 \overline{O4} Cr$$

$$\overline{Yg} = (\overline{Yg})$$

$$Zg = (\overline{\overline{Zg}})$$

$$Zg = Xg Yg \overline{Ca} + Xg \overline{Yg} Ca + \overline{Xg} Yg Ca + \overline{Xg} \overline{Yg} \overline{Ca}$$

$$sCa = \overline{P1} \overline{P24} Ec \overline{Rc} Xg Yg \overline{Ca}$$

$$rCa = \overline{P1} \overline{P24} \overline{Xg} \overline{Yg}$$

$$sCw = Ec \overline{Rc} O5 \overline{O4} Zg$$

$$rCw = ( \overline{sCw} )$$

\* Indicates that the operation code has at least two meanings, depending on the address used with the command.

$\overline{Ec} \overline{Rc}$ 

## 22 RIGHT SHIFT AND INCREMENT (continued)

(RSI)

$$sIs = P24$$

$$rIs = (\overline{Sr} sIw + Sr rIw) \left[ \overline{Ec} O5 (P23-P16) + - - \right] \overline{[K4 K3 K2 K1 F5 F3]}$$

$$Eg = P24 \overline{Ec} \overline{Rc} (O5 Is + - - -)$$

$$rEc = Eg$$

 $\overline{Ec} \overline{Rc}$ 

## 22\* SHIFT RIGHT (AB RIGHT)

(SRT)

The equation used for right shift and increment (RSI) and shift right (SRT) are the same. Whether the C register is incremented or not is a function of the line number used with the command. If the line number has zero in the position corresponding to the L4 flip-flops' configuration, the C register is incremented. If the line number has a one in the position corresponding to the L4 flip-flops' configuration, the C register is recirculated normally via the adder.

---

\*Indicates that the operation code has at least two meanings, depending on the address used with the command.

$\overline{Ec} R_c$ 

## 2 3 SCALE RIGHT AND INCREMENT

(SAI)

$$sEc = P24 \overline{Ec} R_c$$

$$rRc = P24 R_c Is$$

No possibility of phase 3: (O5 Command)

$$sL3 = \overline{O6} O5 \overline{O3} P2 Ar$$

$$rL3 = \overline{O6} O5 \overline{O3} P2 \overline{Ar}$$

$$sBw = \overline{Ec} \overline{Rc} \overline{O6} O5 \overline{O3} O2 \overline{P23} Be + \overline{Ec} \overline{Rc} \overline{O6} O5 \overline{O3} O2 P23 L3 \\ + \overline{P1} Br \left[ \overline{Ec} \overline{Rc} (\overline{O6} O5 \overline{O3} + - - -) \right]$$

$$rBw = (\overline{sBw})$$

$$sAw = \overline{Ec} \overline{Rc} \overline{O6} O5 \overline{O4} \overline{O3} O2 \overline{P23} Ae + \overline{O6} O5 \overline{O4} \overline{O3} P23 Ar \\ + Ar \left[ \overline{Ec} \overline{Rc} (\overline{O6} O5 \overline{O3} + - - -) \right]$$

$$rAw = (\overline{sAw})$$

$$rCa = O5 P24$$

$$Xg = O5 \overline{O4} \overline{O3} (\overline{O2} + P2) \overline{L4}$$

$$\overline{Xg} = (\overline{Xg})$$

$$Yg = O5 \overline{O4} Cr$$

$$\overline{Yg} = (\overline{Yg})$$

$$Zg = (\overline{Zg})$$

$$\overline{Zg} = Xg Yg \overline{Ca} + Xg \overline{Yg} Ca + \overline{Xg} Yg Ca + \overline{Xg} \overline{Yg} \overline{Ca}$$

$$sCa = \overline{P1} \overline{P24} \overline{Ec} \overline{Rc} Xg Yg \overline{Ca}$$

$$rCa = \overline{P1} \overline{P24} \overline{Xg} \overline{Yg}$$

$$sCw = \overline{Ec} \overline{Rc} O5 \overline{O4} Zg$$

$$rCw = (\overline{sCw})$$

$E_c \overline{R_c}$

23 SCALE RIGHT AND INCREMENT ( continued)

(SAI)

$$sO3 = P24 \overline{O6} O5 \overline{O4} \overline{O3} O2 O1 \overline{Cw}$$

$$sIs = P24$$

$$rIs = (\overline{Sr} sIw + Sr rIw) [ E_c O5 (P23-P16) + - ] \overline{[K4 K3 K2 K1 F5 F3]}$$

$$Eg = P24 E_c \overline{R_c} (O5 Is + - - -)$$

$$rEc = Eg$$

$\overline{E}c R_c$

24 NO OPERATION

(NOP)

$$sE_c = P24 \overline{E}c R_c$$

$$rR_c = P24 R_c I_s$$

No possibility of phase 3: (O5 Command)

$$sI_s = P24$$

$$rI_s = (\overline{S}r sI_w + S_r rI_w) \left[ E_c O5 (P16 - P23) + - - - \right] \left[ \overline{K4} \overline{K3} \overline{K2} \overline{K1} \overline{F5} F3 \right]$$

$$E_g = P24 E_c \overline{R}c (O5 I_s + - - -)$$

$$rE_c = E_g$$



$\overline{Ec} Rc$ 

## 25 INTERCHANGE A AND M

(IAM)

$sEc = P24 \overline{Ec} Rc$

$rRc = P24 Rc Is$

No possibility of phase 3: (O5 Command)

$Fg = Mig Nig Mir$

$\overline{Fg} = (\overline{Fg})$

$Ig = (\overline{P24 O4 O2} + \overline{P24 O6 O2 O1}) Ar + P24 Pc$

$\overline{Ig} = (\overline{Ig})$

$Wg = Ec \overline{Rc} (\overline{O6 O5 O4 O3 O2 O1} + - - -)$

$sAw = Ec \overline{Rc} \overline{O6 O4 O3 O2 O1} Fg$

$rAw = (\overline{sAw})$

$sMiw = Mig Nig Wg Ig + \boxed{Mig Nig Wg} \boxed{Mir}$

$rMiw = Mig Nig Wg \overline{Ig} + \boxed{Mig Nig Wg} \boxed{\overline{Mir}}$

$sIs = P24$

$rIs = (\overline{Sr} sIw + Sr rIw) \boxed{Ec O5 (P23-P16) + - - -} \boxed{\overline{K4 K3 K2 K1 F5 F3}}$

$Eg = P24 Ec \overline{Rc} (O5 Is + - - -)$

$rEc = Eg$

$\overline{\text{Ec}} \text{ Rc}$

26 MOVE LINE X TO LINE 7

(MLX)

$\text{sEc} = \text{P24 } \overline{\text{Ec}} \text{ Rc}$

$\text{rRc} = \text{P24 Rc Is}$

No possibility of phase 3: (O5 Command)

$\text{Fg} = \text{Mig Nig Mir}$

$\overline{\text{Fg}} = (\overline{\text{Fg}})$

$\text{sM7w} = \overline{\text{Mig Nig Wg}} \left[ \overline{\text{M7r}} (\overline{\text{O6 O5 O4 O3 O2 O1 Ec}}) + (\overline{\text{O6 O5 O4 O3 O2 O1 Ec}}) \text{Fg} \right]$

$\text{rM7w} = \overline{\text{Mig Nig Wg}} \left[ \overline{\text{M7r}} (\overline{\text{O6 O5 O4 O3 O2 O1 Ec}}) + (\overline{\text{O6 O5 O4 O3 O2 O1 Ec}}) \overline{\text{Fg}} \right]$

$\text{sIs} = \text{P24}$

$\text{rIs} = (\overline{\text{Sr}} \text{ sIw} + \text{Sr rIw}) \left[ \overline{\text{Ec O5 (P23-P16) + - - -}} \right] \left[ \overline{\text{K4K3 K2K1 F5 F3}} \right]$

$\text{Eg} = \text{P24 Ec } \overline{\text{Rc}} (\text{O5 Is} + - - -)$

$\text{rEc} = \text{Eg}$

$\overline{E}c R_c$ 

31\* DIVIDE

(DIV)

$$sL4 = \overline{O6} O5 O4 \overline{O3} \overline{O2} [P23 R_c \overline{L1} \overline{Zg} + P24 R_c L1 \overline{Zg} + \dots]$$

$$sEc = P24 \overline{E}c R_c$$

$$rRc = P24 R_c Is$$

$$rCa = Ca R_c + O5 P24$$

No possibility of phase 3: (O5 Command)

$$Dg = O1 Cr$$

$$\overline{Dg} = (\overline{Dg})$$

$$Xg = \overline{O6} O5 O4 \overline{O3} \overline{O2} (\overline{L4} Dg + L4 \overline{Dg})$$

$$\overline{Xg} = (\overline{Xg})$$

$$Yg = \overline{O6} O4 \overline{O2} Ar$$

$$\overline{Yg} = (\overline{Yg})$$

$$Zg = (\overline{Zg})$$

$$Zg = Xg Yg \overline{Ca} + Xg \overline{Yg} Ca + \overline{Xg} Yg Ca + \overline{Xg} \overline{Yg} \overline{Ca}$$

$$sCa = \overline{O6} O5 O4 \overline{O3} \overline{O2} P1 L4 + \overline{P1} \overline{P24} \overline{E}c \overline{R}c Xg Yg \overline{Ca}$$

$$rCa = \overline{P1} \overline{P24} \overline{Xg} \overline{Yg} + O5 P24$$

$$sL1 = \overline{O6} O5 O4 \overline{O3} \overline{O2} \overline{E}c Zg$$

$$rL1 = \overline{O6} O5 O4 \overline{O3} \overline{O2} \overline{E}c \overline{Zg}$$

$$sL2 = \overline{O6} O5 \overline{O3} \overline{O2} \overline{E}c Br$$

$$rL2 = \overline{O6} O5 \overline{O3} \overline{O2} \overline{E}c \overline{Br}$$

$$sL3 = \overline{O6} O5 \overline{O3} (P24 Bw + \dots)$$

$$rL3 = \overline{O6} O5 \overline{O3} (P24 \overline{Bw} + \dots)$$

\*Indicates that the operation code has at least two meanings, depending on the address used with the command.

$\overline{Ec} \overline{Rc}$ 

31\* DIVIDE (continued)

(DIV)

$$sL4 = \overline{O6} O5 O4 \overline{O3} \overline{O2} [P24 Ec (L1 Cr + \overline{L1} \overline{Cr}) + - - -]$$

$$rL4 = \overline{O6} O5 O4 \overline{O3} \overline{O2} P23 L4$$

$$sL5 = \overline{O6} O5 \overline{O3} P24 Ec$$

$$sAw = Ec \overline{Rc} \overline{O6} O5 \overline{O3} \overline{O2} [\overline{P23} \overline{P2} L1 + P2 L3 + P23 O4 L1]$$

$$rAw = (\overline{sAw})$$

$$sBw = \overline{O6} O5 O4 \overline{O3} \overline{O2} [Ec \overline{P2} \overline{P3} L2 + Ec P3 (\overline{L5} \overline{L4} + L5 L4) + \overline{Ec} P2 L4]$$

$$rBw = (\overline{sBw})$$

Cw = Normal recirculation

$$sIs = P24$$

$$rIs = (\overline{Sr} sIw + Sr rIw) [Ec O5 (P23 - P16) + - - -] [\overline{K4} \overline{K3} \overline{K2} \overline{K1} \overline{F5} \overline{F3}]$$

$$Eg = P24 Ec \overline{Rc} (O5 Is + - - -)$$

$$rEc = Eg$$

 $\overline{Ec} \overline{Rc}$ 

31\* DIVIDE REMAINDER

(DVR)

The equations used for divide (DIV) and divide remainder (DVR) are the same. The line number must have a one in the position corresponding to the L1 flip-flops' configuration and a zero in the position corresponding to the L5 flip-flops' configuration.

\*Indicates that the operation code has at least two meanings, depending on the address used with the command.

$$sB_w = \overline{P1} Br \text{ (Recirculation equation)} \longrightarrow \text{P1 of B register is always cleared.}$$

$$rL_2 = \overline{O6} O_5 O_4 O_3 O_2 O_1 P_{24}$$

$$rL_4 = \overline{O6} O_5 O_4 \overline{O3} O_2 \overline{O1} P_{24}$$

$$sE_c = P_{24} \overline{Ec} R_c$$

$$rR_c = P_{24} R_c I_s$$

$$rC_a = O_5 P_{24}$$

No possibility of phase 3: (O5 Command)

$$sL_2 = \overline{O6} O_5 O_4 \overline{O3} O_2 \overline{O1} P_1 \overline{Be} Br$$

$$sL_4 = \overline{O6} O_5 O_4 \overline{O3} O_2 \overline{O1} P_1 Be \overline{Br}$$

$$sC_a = \overline{O6} O_5 O_4 \overline{O3} O_2 \overline{O1} P_1 Be \overline{Br}$$

$$X_g = \overline{O6} O_5 O_4 \overline{O3} O_2 \overline{O1} (L_2 Cr + L_4 \overline{Cr})$$

$$\overline{X_g} = (\overline{X_g})$$

$$Y_g = \overline{O6} O_5 O_4 \overline{O3} O_2 L_5 (\overline{P_{24}} Ae + P_{24} Ar) \text{ Repeats P23 bit to P24 bit position for addition.}$$

$$\overline{Y_g} = (\overline{Y_g})$$

$$Z_g = (\overline{Z_g})$$

$$\overline{Z_g} = X_g Y_g \overline{C_a} + X_g \overline{Y_g} C_a + \overline{X_g} Y_g C_a + \overline{X_g} \overline{Y_g} \overline{C_a}$$

$$sC_a = \overline{O6} O_5 O_4 \overline{O3} O_2 \overline{O1} P_1 Be \overline{Br}$$

$$+ \overline{P1} \overline{P_{24}} \overline{Ec} \overline{Rc} X_g Y_g \overline{C_a}$$

$$rC_a = \overline{P1} \overline{P_{24}} \overline{X_g} \overline{Y_g} + O_5 P_{24}$$

$$sL_5 = \overline{O6} O_5 \overline{O3} P_{24} Ec$$

$$sA_w = Ec \overline{Rc} \overline{O6} O_5 O_4 \overline{O3} O_2 Z_g$$

$$rA_w = (\overline{sA_w})$$

$$sL3 = \overline{O6} O5 \overline{O3} (P2 A_r + - - -) \\ + \overline{O6} O5 O4 \overline{O3} O2 \overline{O1} Ec \overline{L5} Be \left. \vphantom{\overline{O6} O5 \overline{O3} (P2 A_r + - - -)} \right\}$$

Transfers P2 of A register to  
P23 of B register.

$$rL3 = \overline{O6} O5 \overline{O3} (P2 \overline{A_r} + - - -) \\ + \overline{O6} O5 O4 \overline{O3} O2 \overline{O1} Ec \overline{L5} Be \left. \vphantom{\overline{O6} O5 \overline{O3} (P2 \overline{A_r} + - - -)} \right\}$$

Recirculates B register during  
the first sector.

$$sBw = Ec \overline{Rc} \overline{O6} O5 \overline{O3} O2 (\overline{P23} Be + P23 L3)$$

$$rBw = (\overline{sBw})$$

$$sCw = \overline{P24} Cr \left[ \overline{Ec \overline{Rc} (O5 \overline{O4} O3 \overline{O2} \overline{O1} + \overline{O6} \overline{O5} \overline{O4} \overline{O3} + O5 \overline{O4} + \overline{O6} O5 O4 \overline{O3} \overline{O2} \overline{O1})} \right] + P24 Cw$$

$$rCw = (\overline{sCw})$$

$$sIs = P24$$

$$rIs = (\overline{Sr} sIw + Sr rIw) \left[ \overline{Ec O5 (P23 - P16) + - - -} \right] \left[ \overline{K4 \overline{K3} \overline{K2} \overline{K1} \overline{F5} \overline{F3}} \right]$$

$$Eg = P24 Ec \overline{Rc} (O5 Is + - - -)$$

$$rEc = Eg$$

$\overline{E}c R_c$ 

33\* LOGICAL RIGHT SHIFT (ML = 20)

(LRS)

$$sEc = P24 \overline{E}c R_c$$

$$sL3 = \overline{O}6 O5 \overline{O}3 P2 Ar$$

$$rL3 = \overline{O}6 O5 \overline{O}3 P2 \overline{Ar}$$

$$rRc = P24 R_c Is$$

$$rCa = O5 P24$$

No possibility of phase 3: (O5 Command)

$$sBw = Ec \overline{R}c \overline{O}6 O5 \overline{O}3 O2 \overline{P}23 Be + Ec \overline{R}c \overline{O}6 O5 \overline{O}3 O2 P23 L3$$

$$rBw = (\overline{sBw})$$

$$Yg = \overline{O}6 O5 O4 \overline{O}3 O2 L5 (\overline{P}24 Ae + P24 Ar)$$

$$\overline{Y}g = (\overline{Yg})$$

$$Xg = (\text{No equation to activate this term})$$

$$Xg = (\overline{Xg})$$

$$Zg = (\overline{Zg})$$

$$\overline{Z}g = \overline{X}g \overline{Y}g \overline{C}a + \dots$$

$$sAw = Ec \overline{R}c \overline{O}6 O5 O4 \overline{O}3 O2 Zg$$

$$rAw = (\overline{sAw})$$

$$sIs = P24$$

$$rIs = (\overline{S}r sIw + S_r rIw) [Ec O5 (P23-P16) + \dots] [\overline{K}4 \overline{K}3 \overline{K}2 \overline{K}1 \overline{F}5 \overline{F}3]$$

$$Eg = P24 Ec \overline{R}c (O5 Is + \dots)$$

$$rEc = Eg$$

\*Indicates that the operation code has at least two meanings, depending on the address used with the command.

The equations used for logical right shift (LRS) and shift B right (SBR) are the same. Whether logical right shift (LRS) or shift B right (SBR) occurs or not is a function of the line number used with the command. If the line number has a one in the position corresponding to the L5 flip-flops' configuration, the A register recirculates normally via the adder (L5 permits the Yg equation to operate). If the line number has a zero in the position corresponding to the L5 flip-flops' configuration, the A register is cleared during the first sector of execution (L5 does not permit the Yg equation to operate). The L3 flip-flop transfers the P2 bit configuration (one or zero) of the A register to the P23 position of the B register during the first sector time. After the first sector of execution, the L3 flip-flop transfers only zeroes from P2 of the A register to P23 of the B register.

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\*Indicates that the operation code has at least two meanings, depending on the address used with the command.



$\overline{E_c} R_c$

34 TRANSFER IF C NEGATIVE

(TCN)

$sO_c = P_{23} \overline{E_c} R_c O_5 O_4 O_3 [\overline{O_2} \overline{O_1} Cr + - - -]$  If sign were negative

$sE_c = P_{24} \overline{E_c} R_c$

$rR_c = P_{24} R_c I_s$

No possibility of phase 3: (O5 Command)

$rE_c = E_c O_5 O_4 O_3 \overline{O_c}$

$sR_c = E_c O_5 O_4 O_3 \overline{O_c}$   $\longrightarrow$  If sign "+" go to phase 4 for one pulse and then back to phase 2.

$K_g = E_c O_5 O_4 O_3 (\overline{O_6} + \overline{O_2}) F_4$

$sK_1 = K_g L_1$

$rK_1 = K_g \overline{L_1}$

$sK_2 = K_g L_2$

$rK_2 = K_g \overline{L_2}$

$sK_3 = K_g L_3$

$rK_3 = K_g \overline{L_3}$

$sK_4 = K_g L_4$

$rK_4 = K_g \overline{L_4}$

$sI_s = P_{24}$

$rI_s = (\overline{S_r} s_{lw} + S_r r_{lw}) [E_c O_5 (P_{23} - P_{16}) + - - -] [\overline{K_4} \overline{K_3} \overline{K_2} \overline{K_1} \overline{F_5} \overline{F_3}]$

$E_g = P_{24} E_c \overline{R_c} (O_5 I_s + - - -) \longrightarrow$  Remain in phase 4 until  $I_s$  ( $M_s = No$ ), indicating which sector next command word is located.

$rE_c = E_g$

$sR_c = \overline{E_n} \overline{F_i} E_g O_c$

$\overline{Ec} R_c$

35 TRANSFER IF A NEGATIVE

(TAN)

$$I_g = (\overline{P24} \overline{O6} \overline{O2} O1 + - - -) A_r + P24 P_c$$

$$sO_c = P23 \overline{Ec} R_c O5 O4 O3 [\overline{O6} I_g + - - -]$$

$$sE_c = P24 \overline{Ec} R_c$$

$$rR_c = P24 R_c I_s$$

No possibility of phase 3: (O5 Command)

$$rE_c = E_c O5 O4 O3 \overline{O_c}$$

$$sR_c = E_c O5 O4 O3 \overline{O_c}$$

$$K_g = E_c O5 O4 O3 (\overline{O6} + \overline{O2}) F4$$

$$sK1 = K_g L1$$

$$rK1 = K_g \overline{L1}$$

$$sK2 = K_g L2$$

$$rK2 = K_g \overline{L2}$$

$$sK3 = K_g L3$$

$$rK3 = K_g \overline{L3}$$

$$sK4 = K_g L4$$

$$rK4 = K_g \overline{L4}$$

$$sI_s = P24$$

$$rI_s = (\overline{S_r} sI_w + S_r rI_w) [\overline{Ec} O5 (P23-P16) + - - -] [\overline{K4} \overline{K3} \overline{K2} \overline{K1} \overline{F5} \overline{F3}]$$

$$E_g = P24 E_c \overline{R_c} (O5 I_s + - - -)$$

$$rE_c = E_g$$

$$sR_c = \overline{E_n} \overline{F_i} E_g O_c$$

$$I_g = \overline{P24} \overline{O6} O2 Br + P24 Pc$$

$$sOc = P23 \overline{Ec} R_c O5 O4 O3 [\overline{O6} I_g + - - -]$$

$$sEc = P24 \overline{Ec} R_c$$

$$rRc = P24 R_c Is$$

No possibility of phase 3: (O5 Command)

$$rEc = Ec O5 O4 O3 \overline{Oc}$$

$$sRc = Ec O5 O4 O3 \overline{Oc}$$

$$Kg = Ec O5 O4 O3 (\overline{O6} + \overline{O2}) F4$$

$$sK1 = Kg L1$$

$$rK1 = Kg \overline{L1}$$

$$sK2 = Kg L2$$

$$rK2 = Kg \overline{L2}$$

$$sK3 = Kg L3$$

$$rK3 = Kg \overline{L3}$$

$$sK4 = Kg L4$$

$$rK4 = Kg \overline{L4}$$

$$sIs = P24$$

$$rIs = (\overline{Sr} sIw + Sr rIw) [Ec O5 (P23-P16) + - - -] [\overline{K4} \overline{K3} \overline{K2} \overline{K1} \overline{F5} F3]$$

$$Eg = P24 Ec \overline{Rc} (O5 Is + - - -)$$

$$rEc = Eg$$

$$sRc = \overline{En} \overline{Fi} Eg Oc$$

Oc flip-flop will be set because this command must have an optimum code bit.\*

$$sEc = P24 \overline{Ec} R_c$$

$$rRc = P24 R_c Is$$

No possibility of phase 3: (O5 Command)

$$Kg = Ec O5 O4 O3 (\overline{O6} + \overline{O2}) F4$$

$$sK1 = Kg L1$$

$$rK1 = Kg \overline{L1}$$

$$sK2 = Kg L2$$

$$rK2 = Kg \overline{L2}$$

$$sK3 = Kg L3$$

$$rK3 = Kg \overline{L3}$$

$$sK4 = Kg L4$$

$$rK4 = Kg \overline{L4}$$

$$sIs = P24$$

$$rIs = (\overline{Sr} sIw + Sr rIw) [Ec O5 (P16-P23) + - - -] \overline{[K4 K3 K2 K1 F5 F3]}$$

$$Eg = P24 Ec \overline{Rc} (O5 Is + - - -)$$

$$rEc = Eg$$

$$sRc = \overline{(En)} \overline{(Fi)} Eg Oc$$

---

\*Due to the similarity in logic mechanization if a TRU command is given with no optimum code bit, the operation takes on the aspect of a TBN command and will act accordingly.

$\overline{E}c Rc$ 

## 40 EXTEND BIT PATTERN

(EBP)

$$sEc = P24 \overline{E}c Rc$$

Possibility of phase 3:

$$rRc = P24 Rc Is$$

$$Fg = Mig Nig Mir$$

$$\overline{F}g = (\overline{F}g)$$

$$sAw = Ec \overline{Rc} O6 \overline{O5} \overline{O4} \overline{O3} \overline{O2} \overline{O1} Fg Aw$$

$$+ Ar \left[ \overline{Ec} \overline{Rc} (O6 \overline{O5} \overline{O4} \overline{O3} \overline{O2} \overline{O1} Fg) \right]$$

$$+ \text{---}]$$

When memory has a "1," the previously written bit configuration in A register is repeated.

When memory has a "0," the A register is recirculated.

$$rAw = (\overline{sAw})$$

$$Eg = P24 Ec \overline{Rc} (\overline{O5} \overline{O2} + \overline{O5} O6 + \overline{O5} \overline{O3} \overline{O1}$$

$$+ \overline{O5} \overline{O4} \overline{O1} + \text{---})$$

$$rEc = Eg$$

$\overline{E}c R_c$ 

## 41 GRAY-TO-BINARY

(GTB)

$$sE_c = P24 \overline{E}c R_c$$

Possibility of phase 3:

$$rR_c = P24 R_c I_s$$

$$I_g = (\overline{P24} \overline{O6} \overline{O2} \overline{O1} + \overline{P24} \overline{O4} \overline{O2}) A_r + P24 P_c$$

$$\overline{I}_g = (\overline{I}_g)$$

$$sP_c = E_c \overline{R}_c \overline{P1} \overline{O5} \overline{O3} I_g \overline{P}_c$$

$$rP_c = E_c \overline{R}_c \overline{P1} \overline{O5} \overline{O3} I_g P_c$$

$$sA_w = E_c \overline{R}_c O_6 \overline{O5} \overline{O4} \overline{O3} \overline{O2} O_1 P_c$$

$$rA_w = (\overline{sA_w})$$

$$E_g = P24 E_c \overline{R}_c (\overline{O5} \overline{O2} + \overline{O5} O_6 + \dots)$$

$$rE_c = E_g$$

$\overline{E}c R_c$

42 AND M & C

(AMC)

$$sEc = P24 \overline{E}c R_c$$

Possibility of phase 3:

$$rRc = P24 R_c Is$$

$$Fg = Mig Nig Mir$$

$$\overline{F}g = (\overline{F}g)$$

$$sBw = Ec \overline{R}c O6 \overline{O}5 \overline{O}4 O2 \overline{O}1 Fg Cr$$

$$rBw = (\overline{sBw})$$

$$Eg = P24 Ec \overline{R}c (\overline{O}5 O6 + \overline{O}5 \overline{O}3 \overline{O}1 + \overline{O}5 \overline{O}4 \overline{O}1 + \dots)$$

$$rEc = Eg$$

$\overline{E}c R_c$

43 CLEAR B

(CLB)

$$sEc = P24 \overline{E}c R_c$$

Possibility of phase 3:

$$rRc = P24 R_c Is$$

$$sBw = P1 Br \left[ \overline{E}c \overline{R}c (\overline{O}5 \overline{O}4 \overline{O}3 \overline{O}2) + - - - \right] \quad \text{This will not be true}$$

$$rBw = (\overline{sBw})$$

$$Eg = P24 E_c \overline{R}c (\overline{O}5 O6 + - - -)$$

$$rEc = Eg$$



$\overline{E_c R_c}$

44 CLEAR C

(CLC)

$$sE_c = P24 \overline{E_c R_c}$$

Possibility of phase 3:

$$rR_c = P24 R_c I_s$$

$$sC_w = \overline{P24 C_r} \left[ \overline{E_c R_c} (\overline{O_5 O_4 O_3 O_2 O_1}) + - - - \right] \quad \text{This will not be true.}$$

$$rC_w = (\overline{sC_w})$$

$$E_g = P24 E_c \overline{R_c} (\overline{O_5 O_2} + \overline{O_5 O_6} + \overline{O_5 O_4 O_1} + - - -)$$

$$rE_c = E_g$$

$\overline{E}c R_c$

45 CLEAR A

(CLA)

$$sEc = P24 \overline{E}c R_c$$

Possibility of phase 3:

$$rRc = P24 R_c I_s$$

$$sAw = Ar \left[ \overline{E}c \overline{R}c (\overline{O}5 \overline{O}4 \overline{O}2 O1) + - - - \right]$$

This will not be true.

$$rAw = (sAw)$$

$$Eg = P24 E_c \overline{R}c (\overline{O}5 \overline{O}2 + \overline{O}5 O6 + - - -)$$

$$rEc = Eg$$

$\overline{E}c R_c$ 

46 AND OR COMBINED

(AOC)

$$sEc = P24 \overline{E}c R_c$$

Possibility of phase 3:

$$rRc = P24 R_c I_s$$

$$Fg = Mig Nig Mir$$

$$\overline{F}g = (\overline{F}g)$$

$$sBw = Ec \overline{R}c O_6 \overline{O}_5 \overline{O}_4 O_2 \overline{O}_1 Fg Cr$$

$$+ \overline{P}1 Br \left[ \overline{Ec \overline{R}c (O_6 \overline{O}_5 \overline{O}_4 O_2 Fg)} \right]$$

$$rBw = (\overline{sBw})$$

$$Eg = P24 Ec \overline{R}c (\overline{O}_5 O_6 + \overline{O}_5 \overline{O}_4 O_1 + \dots)$$

$$rEc = Eg$$

If memory has a "1," C register is copied to B register.

If memory has a "0," B register is recirculated.

$\overline{E}c R_c$

47 EXTRACT FIELD

(EXF)

$$sEc = P24 \overline{E}c R_c$$

Possibility of phase 3:

$$rRc = P24 R_c Is$$

$$Fg = Mig Nig Mir$$

$$\overline{F}g = (\overline{F}g)$$

$$sBw = \overline{P}1 Br \left[ \overline{E}c \overline{R}c (O6 \overline{O}5 \overline{O}4 O2 Fg) + \dots \right]$$

If memory has a "0," B register is recirculated.

If memory has a "1," B register receives a "0."

$$rBw = (\overline{sBw})$$

$$Eg = P24 Ec \overline{R}c (\overline{O}5 O6 + \dots)$$

$$rEc = Eg$$

$\overline{E_c} R_c$

50 DISCONNECT INPUT UNIT

(DIU)

$$sE_c = P24 \overline{E_c} R_c$$

Possibility of phase 3:

$$rR_c = P24 R_c I_s$$

$$rR_f = E_c \overline{R_c} O_6 \overline{O_5} O_4 \overline{O_3} \overline{O_2}$$

$$rT_f = E_c \overline{R_c} O_6 \overline{O_5} O_4 \overline{O_3} \overline{O_1}$$

$$E_g = P24 E_c \overline{R_c} (\overline{O_5} \overline{O_2} + \overline{O_5} O_6 + \overline{O_5} \overline{O_3} \overline{O_1} + \dots)$$

$$rE_c = E_g$$

$\overline{E}c R_c$

51 READ TYPEWRITER KEYBOARD

(RTK)

$sEc = P24 \overline{E}c R_c$

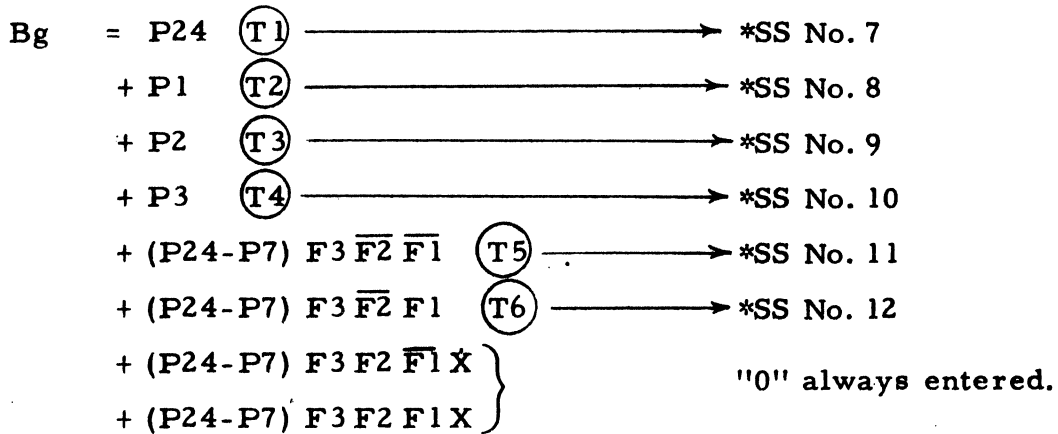
Possibility of phase 3:

$rRc = P24 R_c I_s$

$rRf = E_c \overline{R}c O_6 \overline{O}5 O_4 \overline{O}3 \overline{O}2$

$sTf = E_c \overline{R}c O_6 \overline{O}5 O_4 \overline{O}3 O_1$

$Eg = P24 E_c \overline{R}c (\overline{O}5 \overline{O}2 + \overline{O}5 O_6 + - - -)$



$\overline{B}g = (\overline{B}g)$

$sSw = Bg \overline{Q}g + Sr \overline{S}c \overline{Q}g$

$rSw = \overline{S}c \overline{S}r \overline{B}g$

$rTf = (Tc) \overline{E}c$

\*Selector slides in Flexowriter.

$\overline{Ec} R_c$

52 READ PAPER TAPE

(RPT)

$sEc = P24 \overline{Ec} R_c$

Possibility of phase 3:

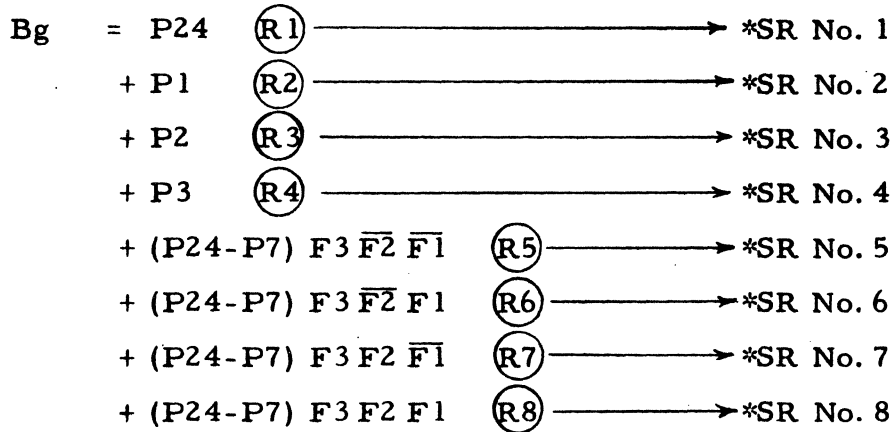
$rRc = P24 R_c I_s$

$sRf = Ec \overline{Rc} O_6 \overline{O_5} O_4 O_3 O_2$

$rTf = Ec \overline{Rc} O_6 \overline{O_5} O_4 \overline{O_3} \overline{O_1}$

$Eg = P24 Ec \overline{Rc} (\overline{O_5} O_6 + \overline{O_5} \overline{O_3} \overline{O_1} + \dots)$

$LR = Rf \overline{Tf}$  (Reader clutch)



$\overline{Bg} = (\overline{Bg})$

$sSw = Bg \overline{Qg} + Sr \overline{Sc} \overline{Qg}$

$rSw = \overline{Sc} \overline{Sr} \overline{Bg}$

$rRf = (Rc) \overline{Ec}$

\*Reader contacts in the Flexowriter.

$\overline{E_c} R_c$ 

## 53 READ FAST UNIT

(RFU)

$$sE_c = P24 \overline{E_c} R_c$$

Possibility of phase 3:

$$sR_c = P24 R_c I_s$$

$$sR_f = E_c \overline{R_c} O_6 \overline{O_5} O_4 \overline{O_3} O_2$$

$$sT_f = E_c \overline{R_c} O_6 \overline{O_5} O_4 \overline{O_3} O_1$$

$$E_g = P24 E_c \overline{R_c} (\overline{O_5} O_6 + - - -)$$

$$\begin{aligned}
B_g &= P24 \left( \textcircled{U1} + \textcircled{S1} \right) \\
&+ P1 \left( \textcircled{U2} + \textcircled{S2} \right) \\
&+ P2 \left( \textcircled{U3} + \textcircled{S3} \right) \\
&+ P3 \left( \textcircled{U4} + \textcircled{S4} \right) \\
&+ (P7-P24) F3 \overline{F2} \overline{F1} \left( \textcircled{U5} + \textcircled{S5} \right) \\
&+ (P7-P24) F3 \overline{F2} F1 \left( \textcircled{U6} + \textcircled{S6} \right) \\
&+ (P7-P24) F3 F2 \overline{F1} \left( \textcircled{U7} + \textcircled{S7} \right) \\
&+ (P7-P24) F3 F2 F1 \left( \textcircled{U8} + \textcircled{S8} \right)
\end{aligned}$$

$$\overline{B_g} = (\overline{B_g})$$

$$sS_w = B_g \overline{Q_g} + S_r \overline{S_c} \overline{Q_g}$$

$$rS_w = \overline{S_c} \overline{S_r} \overline{B_g}$$

Note:  $\textcircled{U}$  indicates magnetic tape. $\textcircled{S}$  indicates photo reader.



$\overline{E}c R_c$ 

55 LOAD A FROM INPUT BUFFER

(LAI)

$$sEc = P24 \overline{E}c R_c$$

$$rRc = P24 R_c I_s$$

Possibility of phase 3:

$$sL1 = O6 \overline{O5} O4 \overline{O2} E_c S_w$$

$$rL1 = O6 \overline{O5} O4 \overline{O2} E_c \overline{S_w}$$

$$sAw = E_c \overline{R_c} O6 \overline{O5} O4 O3 \overline{O2} O1 (L1 V_g + A_r \overline{V_g})$$

$$rAw = (\overline{sAw})$$

$$Q_g = E_c \overline{R_c} O6 \overline{O5} O4 O3 O1 P24 \\ + \overline{E}c O6 \overline{O5} O4 O3 O1 (P7 - P24) \overline{P24}$$

$$sSw = \overline{S_c} S_r \overline{Q_g}$$

$$rSw = Q_g \overline{B_g}$$

$$E_g = P24 E_c \overline{R_c} (\overline{O5} \overline{O2} + \overline{O5} O6 + \dots)$$

$$rEc = E_g$$

$\overline{E}c R_c$

56 COMPARE A AND M

(CAM)

$$sEc = P24 \overline{E}c R_c$$

Possibility of phase 3:

$$rRc = P24 R_c I_s$$

$$Fg = Mig Nig Mir$$

$$\overline{F}g = (\overline{F}g)$$

$$sOf = P24 R_c O_6 \overline{O}_5 O_4 O_3 O_2 \overline{O}_1$$

$$rOf = \overline{P}_1 \overline{P}_2 \overline{P}_4 E_c \overline{R}_c O_6 \overline{O}_5 O_4 O_3 O_2 \overline{O}_1 (Fg \overline{A}r + \overline{F}g Ar)$$

$$Eg = P24 E_c \overline{R}_c (\overline{O}_5 O_6 + - - -)$$

$$rEc = Eg$$

$\overline{E_c} R_c$

57 CLEAR INPUT BUFFER

(CIB)

$$sE_c = P_{24} \overline{E_c} R_c$$

Possibility of phase 3:

$$rR_c = P_{24} R_c I_s$$

$$Q_g = E_c \overline{R_c} O_6 \overline{O_5} O_4 O_3 O_1 P_{24} \\ + \overline{E_c} O_6 \overline{O_5} O_4 O_3 O_1 (P_7 - P_{24}) \overline{P_{24}}$$

$$sS_w = \overline{S_c} S_r \overline{Q_g}$$

$$rS_w = Q_g \overline{B_g}$$

$$E_g = P_{24} E_c \overline{R_c} (\overline{O_5} O_6 + \dots)$$

$$rE_c = E_g$$

$\overline{E_c} R_c$

6X WRITE OUTPUT CHARACTER

(WOC)

$$sE_c = P24 \overline{E_c} R_c$$

$$rR_c = P24 R_c I_s$$

No possibility of phase 3: (O5 Command)

$$T_g = E_c O_6 O_5 \overline{O_4} K_3 \overline{K_2} K_1 \overline{K_4} \text{-----} \text{Designates output to type (Line O5)}$$

$$P_g = E_c O_6 O_5 \overline{O_4} K_3 K_2 K_1 \overline{K_4} \text{-----} \text{Designates output to punch (Line O6)}$$

LTC =  $T_g$  (type translator clutch)

LPC =  $P_g$  (tape punch clutch)

$$LT1 = L1 T_g$$

$$LP1 = L1 P_g$$

$$LT2 = L2 T_g$$

$$LP2 = L2 P_g$$

$$LT3 = L3 T_g$$

$$LP3 = L3 P_g$$

$$LP7 = O2 P_g$$

$$LT4 = L4 T_g$$

$$LP4 = L4 P_g$$

$$LP8 = O3 P_g$$

$$LT5 = L5 T_g$$

$$LP5 = L5 P_g$$

$$LT6 = O1 T_g$$

$$LP6 = O1 P_g$$

$$rC_a = O5 P24$$

$$X_g = O6 O5 \overline{O_4}$$

$$\overline{X_g} = (\overline{X_g})$$

$$Y_g = O5 \overline{O_4} C_r$$

$$\overline{Y_g} = (\overline{Y_g})$$

$$Z_g = (\overline{Z_g})$$

$$\overline{Z_g} = X_g Y_g \overline{C_a} + X_g \overline{Y_g} C_a + \overline{X_g} Y_g C_a + \overline{X_g} \overline{Y_g} \overline{C_a}$$

$$sC_a = \overline{P1} \overline{P24} E_c \overline{R_c} X_g Y_g \overline{C_a}$$

$E_c \overline{R_c}$

6X WRITE OUTPUT CHARACTER (continued)

(WOC)

$$rCa = \overline{P1} \overline{P24} \overline{Xg} \overline{Yg} + O5 P24$$

$$sCw = E_c \overline{R_c} O5 \overline{O4} Zg$$

$$rCw = (\overline{sCw})$$

$$sIs = P24$$

$$rIs = (\overline{Sr} sIw + Sr rIw) [E_c O5 (P16-P23) + - - -] \overline{[K4 K3 K2 K1 F5 F3]} \\ + P23 E_c \overline{R_c} O6 O5 \overline{O4} \overline{Cr}$$

$$Eg = P24 E_c \overline{R_c} (O5 Is + - - -)$$

$$rEc = .Eg$$

$\overline{E}c R_c$

70 PULSE TO SPECIFIED UNIT

(PTU)

$$sEc = P24 \overline{E}c R_c$$

$$rRc = P24 R_c Is$$

No possibility of phase 3: (O5 Command)

$$Cpg = Ec O6 O5 O4 \overline{O3} \overline{O2} \overline{O1}$$

$$sIs = P24$$

$$rIs = (\overline{S}r sIw + Sr rIw) [Ec O5 (P16-P23) + - - -] \boxed{\overline{K4} \overline{K3} \overline{K2} \overline{K1} \overline{F5} F3}$$

$$Eg = P24 Ec \overline{R}c (O5 Is + - - -)$$

$$rEc = Eg$$

$\overline{Ec} R_c$ 

## 71 MOVE COMMAND LINE BLOCK

(MCL)

$$sEc = P24 \overline{Ec} R_c$$

$$rRc = P24 R_c Is$$

No possibility of phase 3: (O5 Command)

$$I_g = \overline{P24} O_6 O_5 \overline{O2} V_g + P24 P_c$$

$$\overline{I_g} = (\overline{I_g})$$

$$W_g = Ec \overline{Rc} (O_6 O_5 O_4 \overline{O3} O_1)$$

$$sMiw = Mig Nig W_g I_g + \boxed{Mig Nig W_g} \boxed{Mir}$$

$$rMiw = Mig Nig W_g \overline{I_g} + \boxed{Mig Nig W_g} \boxed{Mir}$$

$$sIs = P24$$

$$rIs = (\overline{Sr} sIw + Sr rIw) \boxed{Ec O_5 (P23-P16) + - - -} \boxed{\overline{K4} \overline{K3} \overline{K2} \overline{K1} \overline{F5} \overline{F3}}$$

$$Eg = P24 Ec \overline{Rc} (O_5 Is + - - -)$$

$$rEc = Eg$$

$\overline{E}c R_c$

72 BLOCK SERIAL OUTPUT

(BSO)

$$sEc = P24 \overline{E}c R_c$$

$$rRc = P24 R_c Is$$

No possibility of phase 3: (O5 Command)

$$Fg = Mig Nig Mir$$

$$\overline{F}g = (\overline{F}g)$$

$$Gdg = Fg$$

$$Gsg = Ec O6 O5 O4 \overline{O3} O2 \overline{O1} Vg \overline{P1} \overline{P24}$$

$$sIs = P24$$

$$rIs = (\overline{S}r sIw + Sr rIw) [Ec O5 (P16 - P23) + - - -] \boxed{\overline{K4} \overline{K3} \overline{K2} \overline{K1} \overline{F5} F3}$$

$$Eg = P24 Ec \overline{R}c (O5 Is + - - -)$$

$$rEc = Eg$$



$$sEc = P24 \overline{Ec} R_c$$

$$rRc = P24 R_c Is$$

No possibility of phase 3: (O5 Command)

$$Hdg = \text{data input to Ig gate}$$

$$Ig = \overline{P24} O_6 O_5 O_2 V_g Hdg + P24 P_c$$

$$Ig = (\overline{Ig})$$

$$Hsg = Ec O_6 O_5 O_4 \overline{O_3} O_2 O_1 V_g \overline{P_1} \overline{P24}$$

$$Wg = Ec \overline{R_c} (O_6 O_5 O_4 \overline{O_3} O_1 + - - -)$$

$$sMiw = Mig Nig Wg Ig + \boxed{Mig Nig Wg} \boxed{Mir}$$

$$rMiw = Mig Nig Wg \overline{Ig} + \boxed{Mig Nig Wg} \boxed{\overline{Mir}}$$

$$Sis = P24$$

$$rIs = (\overline{Sr} sIw + Sr rIw) \left[ Ec O_5 (P16-P23 + - - -) \boxed{\overline{K_4} \overline{K_3} \overline{K_2} \overline{K_1} \overline{F_5} \overline{F_3}} \right]$$

$$Eg = P24 Ec \overline{R_c} (O_5 Is + - - -)$$

$$rEc = Eg$$

$$sOc = P23 \overline{Ec} R_c O5 O4 O3 [O6 \overline{O2} O1 Of + - - -]$$

$$sEc = P24 \overline{Ec} R_c$$

$$rRc = P24 R_c Is$$

No possibility of phase 3: (O5 Command)

$$rEc = Ec O5 O4 O3 \overline{Oc}$$

$$sRc = Ec O5 O4 O3 \overline{Oc}$$

$$sK1 = Kg L1$$

$$rK1 = Kg \overline{L1}$$

$$sK2 = Kg L2$$

$$rK2 = Kg \overline{L2}$$

$$sK3 = Kg L3$$

$$rK3 = Kg \overline{L3}$$

$$sK4 = Kg L4$$

$$rK4 = Kg \overline{L4}$$

$$rOf = P23 Ec O6 O5 O4 O3 \overline{O2} O1$$

$$sIs = P24$$

$$rIs = (\overline{Sr} sIw + Sr rIw) [Ec O5 (P16-P23 + - - -)] [\overline{K4} \overline{K3} \overline{K2} \overline{K1} \overline{F5} \overline{F3}]$$

$$Eg = P24 Ec \overline{Rc} (O5 Is + - - -)$$

$$rEc = Eg$$

$$sRc = \overline{En} \overline{Fi} Eg Oc$$

$\overline{E_c} R_c$

77 TRANSFER ON EXTERNAL SIGNAL

(TES)

$J_g = M_{ig} N_{ig} \textcircled{J_i}$  (Selected external signal line)

$s_{O_c} = P_{23} \overline{E_c} R_c O_5 O_4 O_3 [O_6 O_2 O_1 J_g + - -]$

$s_{E_c} = P_{24} \overline{E_c} R_c$

$r_{R_c} = P_{24} R_c I_s$

No possibility of phase 3: (O5 Command)

$r_{E_c} = E_c O_5 O_4 O_3 \overline{O_c}$

$s_{R_c} = E_c O_5 O_4 O_3 \overline{O_c}$

$s_{I_s} = P_{24}$

$r_{I_s} = (\overline{S_r} s_{I_w} + S_r r_{I_w}) [E_c O_5 (P_{16} - P_{23}) + - - -] [\overline{K_4 K_3 K_2 K_1 F_5 F_3}]$

$E_g = P_{24} E_c \overline{R_c} (O_5 I_s + - -)$

$r_{E_c} = E_g$

$s_{R_c} = \textcircled{E_n} \textcircled{F_i} E_g O_c$