REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
—	REL FOR PROD PER ERO 500626	10-3-75	AB

APPLICATION

NEXT ASSY	USED ON

PRODUCTION RELEASE

REV STATUS OF SHEETS																					
	REV LTR																				
	SHEET																				
	REV LTR	—	—	—	—	—	—	—	—												
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21

DO NOT SCALE DRAWING

SCREW THREADS PER HANDBOOK H-28

COUNTERBORE AND SPOTFACE FILLET RADII TO BE .010 MAXIMUM

REMOVE ALL BURRS AND BREAK SHARP EDGES EQUIVALENT TO .010R

ROUGHNESS OF MACHINED SURFACES 125 PER USAS B46.1.

STANDARD HOLE TOLERANCE PER AND 10387

TOLERANCES ON: .XX = ± .03 .XXX = ± .010 ANGLES = ± 0° 30'

INTERPRET DIMENSIONS AND TOLERANCES PER USAS Y14.5

DIMENSIONS ARE IN INCHES AND APPLY AFTER HEAT TREAT AND FINISH

UNLESS OTHERWISE SPECIFIED

CONTRACT NO.

DRAWN	T. Githens	10-3-75
CHECK	Bose	10-3-75
DESIGN		
PROJ. ENGR.	D. Andersen	10-3-75
OTHER APPROVALS		

Plessey Memories Incorporated
Santa Ana, California

DWG TITLE
PRODUCT PERFORMANCE SPECIFICATION
PM-DC/8
DISC CONTROLLER

SIZE	CODE IDENT NO.	DWG NO.
A	52648	PS700655

SCALE:

SHEET 1 OF 8

DISTR NO.

FORM 000020

1.0 FEATURES

The Plessey PM-DC/8 disc controller is designed as a direct replacement for the Digital Equipment Corporation RK8-E disc controller. The PM-DC/8 is completely hardware and software compatible with the RK8-E disc controller and plugs directly into the OMNIBUS* without the requirement for additional cabling or rack space.

The Plessey PM-DC/8 is capable of controlling up to 2 Plessey PM-DD/8 dual disc drives or up to 4 DEC* RK05 disc drives in a daisy chain configuration forming a system capable of nearly 5 million words of data storage.

2.0 SYSTEM DESCRIPTION

The PM-DC/8 disc controller consists of three printed circuit modules which are inserted into the OMNIBUS in a fashion indentical to the DEC RK8-E disc controller. The three printed circuit modules include the Major Registers Module, Control Module, and Data Buffer and Status Module. The three printed circuit modules are connected together at the top by means of edge connectors. Connection to the disc drive is made by means of a drive interface cable. The controller is connected only to the first disc drive with the signals to or from succeeding drives supplied by means of an interconnecting signal cable between each drive.

3.0 DATA RECORDING AND FORMAT

3.1 Data is transferred to the disc drive at a rate of 1440 KHz per second or 8.32 usec. per 12 bit word. Data is transferred serially to the drive using the double frequency recording method.

During a write operation the controller generates timing pulses called data clock pulses. The time between the data clock pulses is called the bit-cell time. In order to write a "1" data bit the controller inserts a pulse in the bit-cell time. An absence of a pulse in the bit-cell time indicates a "Ø" data bit. During a write operation the controller transmits data and clock pulses serially to the disc drive over the Write Data line.

* DEC, OMNIBUS, and PDP are registered trademarks of the Digital Equipment Corporation.

3.1 (Continued)

During a read operation the disc drive separates the clock and data pulses and transmits them on separate lines called the Read Clock line and Read Data line. The disc controller utilizes the Read Clock pulses for timing purposes to determine whether the Read Data line contains a data "1" or data "Ø".

The data stored on the disc is divided into 16 sectors per track. Each sector contains 256 data words. The sector is divided into 6 sections: Preamble (140 us of "Ø" data bits), Sync Bit (a single data "1" bit), Header (a 16-bit word containing the cylinder address), Data (256 12-bit words), CRC (16-bit cycle redundancy check word), and Postamble (25 us erase delay zone).

SECTOR FORMAT

Preamble	Sync Bit	Header	Data Field	CRC	Postamble
140us zeros	Single "1" bit	16-bit word	256 12-bit words	16-bit word	25us erase zone

4.0 CONTROL AND STATUS REGISTERS

Software control of the PM-DC/8 disc controller is provided through the implementation of four major registers including the Command Register, Current Address Register, Disc Address Register, and Status Register. These registers are loaded by software or are read by software to control and monitor disc operations.

4.1 Command Register

0 1 2	3	4	5	6	7	8	9 10	11
Function	IDE flag	Enable interrupt on seek done	Xfer 128 word block	EMA2	EMA1	EMAØ	Drive Address	CYL Add

BITS 0, 1, 2 Function; these bits are used to indicate drive operations as follows:

Bit Ø	Bit 1	Bit 2	Operation
0	0	0	Read Data - Read Header and 1 sector
0	0	1	Read All - Read 1 sector
0	1	0	Set Write Protect
0	1	1	Seek
1	0	0	Write Data - Check Header and Write
1	0	1	Write All - Write only.

Bit 3 Interrupt on Done Enable; this bit enables interrupt on Error flag or Transfer Done.

Bit 4 Enable Interrupt on Seek Done; this bit causes Transfer Done to be set when Seek Complete occurs.

Bit 5 Transfer 128 word Block; this bit causes the controller to read 128 words in a sector instead of 256.

Bits 6, 7, 8

Extended Memory - these bits are used to select extended memory as follows:

Bit 6	Bit 7	Bit 8	Field
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Bits 9, 10 — Drive address; these bits select a disc drive as follows:

Bit 9	Bit 10	Unit
0	0	0
0	1	1
1	0	2
1	1	3

Bit 11 — Cylinder Address 128; this bit is used in conjunction with the Cylinder Address Register bits to select a track address.

4.2 Current Address Register

The contents of the Current Address Register and bits 6, 7 and 8 of the Command Register are transmitted to the OMNIBUS to select the first memory location to which data is to be transferred. Before each succeding data transfer, the contents of the Current Address Register are incremented to select the next sequential memory location. Bits 6, 7, and 8 of the Command Register are not incremented and must be changed by means of the program.

4.3 Disc Address Register

0	1	2	3	4	5	6	7	8	9	10	11
Add 64	Add 32	Add 16	Add 8	Add 4	Add 2	Add 1	SUR	Sector 8	Sector 4	Sector 2	Sector 1

Bits 0-6 — Cylinder Address - These bits are loaded with the track address for a data transfer operation.

Bit 7 — Surface - This bit indicates on which disc surface, upper or lower, a data transfer is to occur.

Bits 8-11 — Sector Address - These bits define, in binary form, the address of the sector to or from data is to be transferred.

4.4 Status Register

0	1	2	3	4	5
Control Done	R/W/S Ready	Not Used	Seek Fail	Not Ready	Busy Error

4.4 (Continued)

6	7	8	9	10	11
Time Out Error	WLO Error	CRC Error	Data Request Late	Drive Status Error	CYL Address Error

Bit 0 Control Done - this bit is set at the end of a data transfer, when an error occurs, at the end of a Seek Only operation, or at the completion of a recalibrate operation.

Bit 1 R/W/S Ready - this bit indicates that the selected disc drive has completed a seek operation.

Bit 2 Unused

Bit 3 Seek Fail - this bit indicates that the selected disc drive failed to complete a seek operation.

Bit 4 File Not Ready - this bit indicates that the selected disc drive is not ready.

Bit 5 Busy Error - this bit is set if an operation is started when Control Busy is set.

Bit 6 Time Out Error - this bit is set if the control is busy for more than 280ms.

Bit 7 Write Lock Out Error - this bit indicates that the program tried to write on a write protected disc drive.

Bit 8 CRC Error - this bit indicates that the CRC character calculated by the control did not compare with the CRC read from the disc.

Bit 9 Data Request Late - this bit is set if the processor does not respond to a break request within 22.5 us.

Bit 10 Drive Status Error - this bit is set if a command is issued to a not ready drive or the drive responds with Write Check Error.

Bit 11 Cylinder Address Error - this bit is set if a seek has been completed and the header read indicates that the cylinder address is not correct.

5.0 INTERNAL REGISTERS

The PM-DC/11 contains 5 major registers that are not visible to software. These registers include the Data Buffer Register, CRC Register, Major State Register, Bit Count Registers and Word Count Register.

5.1 Data Buffer Register

During data transfer operations data is assembled in the Data Buffer Register which is capable of storing four data words and transferring the data words, on request, to memory. This 4-word register increases the time that the controller can wait for access to the computer from 6.2 us with a single serial register and one data buffer to 22.5 us with 4 Data Buffer Registers.

5.2 CRC Register

The CRC Register calculates the CRC word to be written on the disc after the data field. In addition, during a read operation the CRC Register calculates the CRC word from the serial data read and does a comparison of the calculated CRC word with the CRC word read from the disc.

The CRC Register is also loaded with the cylinder address by the Load Address and Go instructions. The CRC Register then performs a comparison of the Header word to insure that the drive has seeked to the correct cylinder.

5.3 Major State Register

The sequences of operations within the PM-DC/8 are monitored and controlled by the Major State Register. The Major State Register determines in which area or state the read/write head is located within the sector such as Header area or Data Field. The Major State Register also performs other housekeeping functions and is stepped to control disc drive sequences throughout an operation.

5.4 Bit Count Registers

The Bit Count Registers consist of a 12-bit counter and a 16-bit counter. The 12-bit counter determines the boundries of the PM-DC/8 data word and the 16-bit counter determines that a CRC word or Header is being read to enable the control to know when to check the CRC or Header.

5.5 Word Counter Registers

The Word Count Register Monitors the output of the 12-bit counter to determine that the correct number of data words has been transferred. The Word Counter normally is set to overflow when 256 words have been read but if the Transfer 128-word block in the Command Register is set the Word Counter will overflow at 128 words.

6.0 SPECIFICATIONS

Characteristic	Specification
Data Format	12 bit data word
Sector Capacity	256 data words
Transfer Rate	8.32 us/word
Recording Method	double frequency encoded
Operating Temperature	50° to 100°F
Power Requirements	+5VDC at 3 Amps