PRIAM

OEM MANUAL

Model 3350
Model 6650
Model 15450

FOURTEEN INCH WINCHESTER DISC DRIVES

January 1984 P/N 308002 Rev B EC 2052

PRIAM

Fourteen-Inch Winchester Disc Drives
OEM MANUAL

JANUARY, 1984

SHEET AND REVISION TABLE									
EC 2052									
SHT	i	ii	iii	1	2	3	4	5	6
REV	B	B	B	B	B	B	B	B	B
SHT	7	8	9	10	11	12	13	14	15
REV	B	B	B	B	B	B	B	B	B
SHT	16	17	18	19	20	21	22	23	24
REV	B	B	B	B	B	B	B	B	B
SHT	25	26	27	28	29	30	31	32	33
REV	B	B	B	B	B	B	B	B	B
SHT	34	35	36	37	38	39	40	41	42
REV	B	B	B	B	B	B	B	B	B
SHT	43	44	45	46	47	48	49	50	
REV	B	B	B	B	B	B	B	B	

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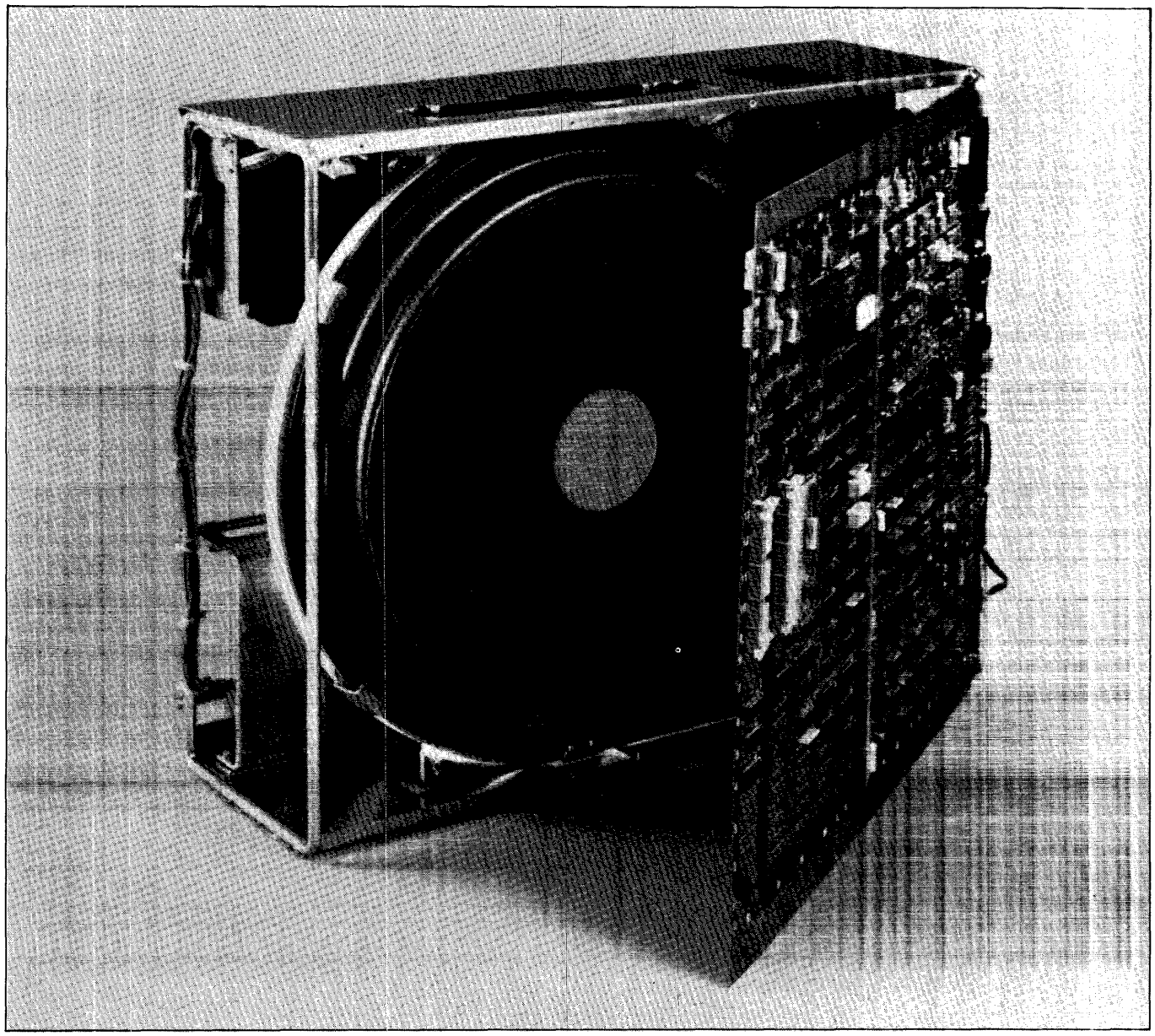


Figure 1-1. DISKOS 3350, 6650 and 15450

1. GENERAL INFORMATION

1.1 Introduction. The DISKOS 3350, 6650 and 15450 use advanced Winchester and microprocessor technologies to provide users with low-cost disc drives having high capacity, fast access, and long-term reliability. Linear motor voice coil positioners with track following servos enable the DISKOS 3350, 6650 and 15450 to position Winchester type heads quickly and precisely. These low-force heads assure high data reliability.

Advanced 14-inch Winchester-technology discs are driven by an outer-rotor, brushless DC motor. The head positioner coil and carriage, heads and discs are enclosed in a sealed, contamination-resistant chamber to assure high reliability.

Two heads serve each disc surface, with one head and data band dedicated to servo information for fully servoed track following, head positioning and write timing. One disc recorded at 480 tracks per inch with three data bands is used in the DISKOS 3350 to provide a capacity of 34 megabytes of unformatted data. In the DISKOS 6650, one disc is recorded at 960 tracks per inch with three data bands to provide a capacity of 68 megabytes of unformatted data. In the DISKOS 15450, two discs are recorded at 960 tracks per inch with seven data bands to provide a capacity of 158 megabytes of unformatted data.

Microprocessors are used in the disc drive electronics to provide interface flexibility and to monitor drive operation. For example, they control

power up and down sequencing, and a self-test program checks drive performance during each power-up sequence. Any malfunction detected by these tests will prevent drive start-up, reducing the chance of loss of data or damage to the drive.

PRIAM disc drives are constructed in a modular fashion so that defective assemblies can be easily replaced. This greatly reduces down time due to servicing. The six assemblies are:

Head Disc Assembly
Main PCB Assembly
Motor Control PCB Assembly
Power Supply Module (Optional)
Photocell Assembly
Frame Assembly

The Head Disc Assembly (HDA) is a sealed enclosure. It contains the drive spindle assembly, drive motor, voice coil motor, head carriage assembly, read/write heads, magnetic discs, and air filter assembly.

The Main PCB Assembly contains all the circuitry associated with read/write control, command execution, information transfers through the user interface, processing servo signals from the servo read head, and controlling the position of the head carriage.

The Motor Control PCB Assembly contains the circuitry associated with driving the spindle motor. This circuitry receives an ON/OFF command from the main PCB, and spindle rotation feedback from the Photocell Assembly.

If the PRIAM power supply option is chosen, the power supply is mounted within the Frame Assembly. The PRIAM power supply can operate from 50 or 60 HZ, with input voltage (selectable) of 100, 120, 220, or 240 VAC.

The Photocell Assembly contains the photo-detectors which sense the DC Motor position. This information is used to control the electrical commutating required for brushless DC motors.

The Frame Assembly is constructed to accommodate all optional assemblies of the disc drive. Its open steel rod and sheet metal design provides improved air circulation and makes the drive lighter, lower in cost and easier to install.

1.2 Options

1.2.1 Interface Types. The PRIAM 14-inch disc drives are available with a variety of interface options. All interfaces available from PRIAM include on-board data separation.

The standard PRIAM interface is designed for low cost and efficient use with micro-processor-based systems. Up to four drives may be daisy-chained when this interface is used. The PRIAM interface provides a basic 8-bit bidirectional bus, which may be used with the popular 8-bit and 16-bit microprocessors. It also provides bit-serial NRZ data exchange. No elaborate handshaking protocols are required. The PRIAM interface is built into the disc drive's main PCB. A 50-conductor flat ribbon cable is used between the PRIAM interface and the host system.

The SMD interface permits a PRIAM 14-inch drive to be used with existing Storage Module Drive (SMD) controllers. The SMD interface is embedded in the main PCB assembly and can be connected directly to an SMD controller. The line drivers and line receivers in the SMD interface are matched to those of typical SMD controllers. There are two interface cables between the host system and the drive interface — a 60-conductor twisted-pair flat cable ("A" cable) and a 26-conductor flat ribbon cable ("B"cable).

An ANSI interface adapter is also available. Characteristics of the ANSI interface include variable and fixed sector sizes,data transfer rates up to 10 megabits per second, and radial attention and select capability. Up to eight drives may be daisy-chained on a single 50-conductor flat ribbon cable.

1.2.2 Interface Cables and Terminators. I/O cables are available from PRIAM for connecting daisy-chained drives to one another.

Terminators are available for I/O signal lines to minimize reflections and to ensure maximum data integrity. One terminator is required for a single drive or for the last drive in a daisy chain. Each drive is shipped with a terminator installed.

1.2.3 Power Supplies. PRIAM's optional power supply allows PRIAM disc drives to operate from 100, 120, 220, and 240 VAC, 50 or 60 Hz power. The optional power supply is delivered already mounted within the drive frame. No extra space or interconnection is required.

1.2.4 Mounting Hardware. Optional slides are available from PRIAM. These slides allow easy access to drives mounted in standard 19" racks and cabinets.

2. SPECIFICATIONS SUMMARY

2.1 General Specifications. Table 2.1 provides functional specifications for the PRIAM 14-inch series of disc drives. Table 2.2 provides operational and non-operational environmental specifications for the disc drives.

Table 2-1. Functional Specifications

	DISKOS 3350	DISKOS 6650	DISKOS 15450
Capacity			
Unformatted			
Per Drive (bytes)	33,929,280	67,798,080	158,195,520
Per R/W Head (bytes)	11,309,760	22,599,360	22,599,360
Per Track (bytes)	20,160	20,160	20,160
Formatted (128 bytes/sector; 111 sectors/track)			
Per Drive (bytes)	23,912,064	47,781,504	111,490,176
Per R/W Head (bytes)	7,970,688	15,927,168	15,927,168
Per Track (bytes)	14,208	14,208	14,208
Formatted (256 bytes/sector; 65 sectors/track)			
Per Drive (bytes)	28,005,120	55,960,320	130,574,080
Per R/W Head (bytes)	9,335,040	18,653,440	18,653,440
Per Track (bytes)	16,640	16,640	16,640
Formatted (512 bytes/sector; 35 sectors/track)			
Per Drive (bytes)	30,159,360	60,264,960	140,618,240
Per R/W Head (bytes)	10,053,120	20,088,320	20,088,320
Per Track (bytes)	17,920	17,920	17,920
Formatted (1024 bytes/sector 18 sectors/track)			
Per Drive (bytes)	31,021,056	61,986,816	144,635,904
Per R/W Head (bytes)	10,340,352	20,662,272	20,662,272
Per Track (bytes)	18,432	18,432	18,432
Transfer Rate (Mbytes/sec)	1.04	1.04	1.04
Rotational Latency (Average)	9.7 msec	9.7 msec	9.7 msec
Access Times (max)			
Track to Track	10 msec	10 msec	12 msec
Average	48 msec	48 msec	48 msec
Longest Seek	86 msec	86 msec	86 msec
Disc Surfaces	2	2	4
Data Heads	3	3	7
Cylinders	561	1121	1121
Track Density (TPI)	480	960	960
Nominal RPM	3100	3100	3100

Table 2-1. Functional Specifications (cont'd.)

	DISKOS 3350	DISKOS 6650	DISKOS 15450
Recording Characteristics:			
Maximum Density (BPI)	6430	6430	6430
Recording Code	MFM	MFM	MFM
Start Time (max)	45 sec	45 sec	90 sec
Stop Time (max) (With Dynamic Brake)	45 sec	45 sec	90 sec

Table 2-2. Environmental Specifications **

	Equipment Operational	Equipment Non-Operational
Ambient Temperature	15°C/hr max rate of change 10° to 40°C* (50° to 104°F)	30°C/hr max rate of change +5° to 60°C (41° to 140°F)
Relative Humidity	8% to 80% without condensation.	8% to 90% without condensation.
Altitude	From 1000 feet below sea level to 12,000 feet above sea level. Derate maximum temperature linearly to 35°C from 7,000 to 12,000 feet.	From 1000 feet below sea level to 40,000 feet above sea level.
Vibration	Drives are capable of sustained exposure to vibrations as specified during normal operation and exhibit no non-recoverable error conditions.	Drives are capable of exposure to vibration as specified while non-operational with mechanical locks set and exhibit no damage or operational performance degradation.
	0.3 g's from 100 to 300 Hz.	2.0 g's from 45 to 300 Hz.
	0.0003 inch 0 to peak from 60 to 100 Hz.	
	0.1 g's from 14 to 60 Hz	
	0.005 inch 0 to peak from 2 to 14 Hz	0.010 inch 0 to peak from 2 to 45 Hz
Shock	Drives are capable of sustained exposure to vibrations as specified during normal operation and exhibit no non-recoverable error conditions.	Drives are capable of exposure to shock as specified while non-operational with mechanical locks set and exhibit no damage or operational performance degradation.
	The shocks will be a half sine wave with peak level of 1 g and have a duration of 11 msec.	The shocks will be a half sine wave with peak level of 25 g's and have a duration of 11 msec.

* 100 CFM air flow should be supplied to the drive end to end to maintain temperature within these limits.

** Refer to Appendix B for Environmental Specifications of drive packaged in PRIAM shipping container or equivalent shipping container.

2.2 Reliability Specifications

MTBF: 10,000 power on hours.

MTTR: 30 minutes.

Component Life: 5 years

Acoustic Noise Level: 60 db at 1 meter

Error Rates:

Seek Errors < 1 per 10^6 seeks
Soft Read Errors < 1 per 10^{10} bits transferred
Hard Read Errors < 1 per 10^{13} bits transferred

2.2.1 Defects. Defects are hard errors found in the disc during disc drive manufacture. Defects are identified by PRIAM to the user when disc drives are delivered. A defect is a media flaw which is 3 bytes or less in length. Any track containing more than 3 defects is considered "bad" by PRIAM. Each bad track is considered one defect for purposes of the specification. The maximum number of defects and bad tracks for each of the DISKOS 14-inch products is shown below.

	3350	6650	15450
Defects (max.)	40	100	230
Bad Tracks (max.)	15	35	82

(Cylinder zero is guaranteed to be defect free)

2.2.2 Preventive Maintenance. No preventive maintenance is required.

2.3 Power Requirements.

AC Power (Optional)

PRIAM's optional power supply provides all of the specified DC requirements. The power supply requires a minimum of 425 watts at 47-63 Hz and one of the following voltages:

100 VAC ± 10%
120 VAC ± 10%
220 VAC ± 10%
240 VAC ± 10%

The power consumption drops to 350 watts max following startup.

DC Power

All PRIAM 14-inch disc drives require power from four DC voltages: +24, +5, −5, and −12 volts. DC power is supplied via a 6-pin connector (AMP 1-480270-0 socket and 6 AMP PINS 60617-1, or equivalent).

Table 2-3. − DC Power Requirements

VOLTAGE	TOL.	PIN NUMBER	CURRENT AMPS MAXIMUM	CURRENT AMPS TYPICAL	RIPPLE (MV P-P MAX)	
+24	±5% (−15% while starting)	2	7.0 ** (while starting)	—	48	(*500)
			—	5.5 (seeking)		
			—	4.0 (not seeking)		
+5	±5%	5	4.0	1.5	10	(*100)
−5	±5%	3	2.0	1.0	10	(*100)
−12	±5%	4	0.7	0.5	24	(*200)
GND		1	8.7	—	—	
24 volt return		6	7.0	—	—	

** Peak current may exceed this number for 5ms.

*Allowed for power systems with + or −3% tolerance including line and load regulation and ripple frequency components under 1 MHz. Ripple frequency components greater than 1 MHz must be less than 5 MV P-P.

Power Dissipation: 1190 BTU/H maximum (350 watts)

2.4 Mounting/Weight Specifications.

Outline drawings of DISKOS 14-inch products are provided in Figure 2-1.

2.4.1 Weight. Weights of PRIAM 14-inch disc drives are shown below:

	3350	6650	15450
Basic disc drive (lbs.)	34	34	40
Power Supply Option (lbs.)	18	18	18
Slide Option (lbs.)	6	6	6

2.4.2 Mounting. The recommended mounting orientations are (i) horizontally, with PCB up for cooling, or (ii) vertically, with the power supply side of the rack frame down and positioner motion horizontal. The exact locations of the drives' mounting pads are shown in Figure 2-1. All PRIAM 14-inch drives can be mounted in a standard 19-inch rack. PRIAM offers an optional slide mounting kit for use with the 14-inch drive models.

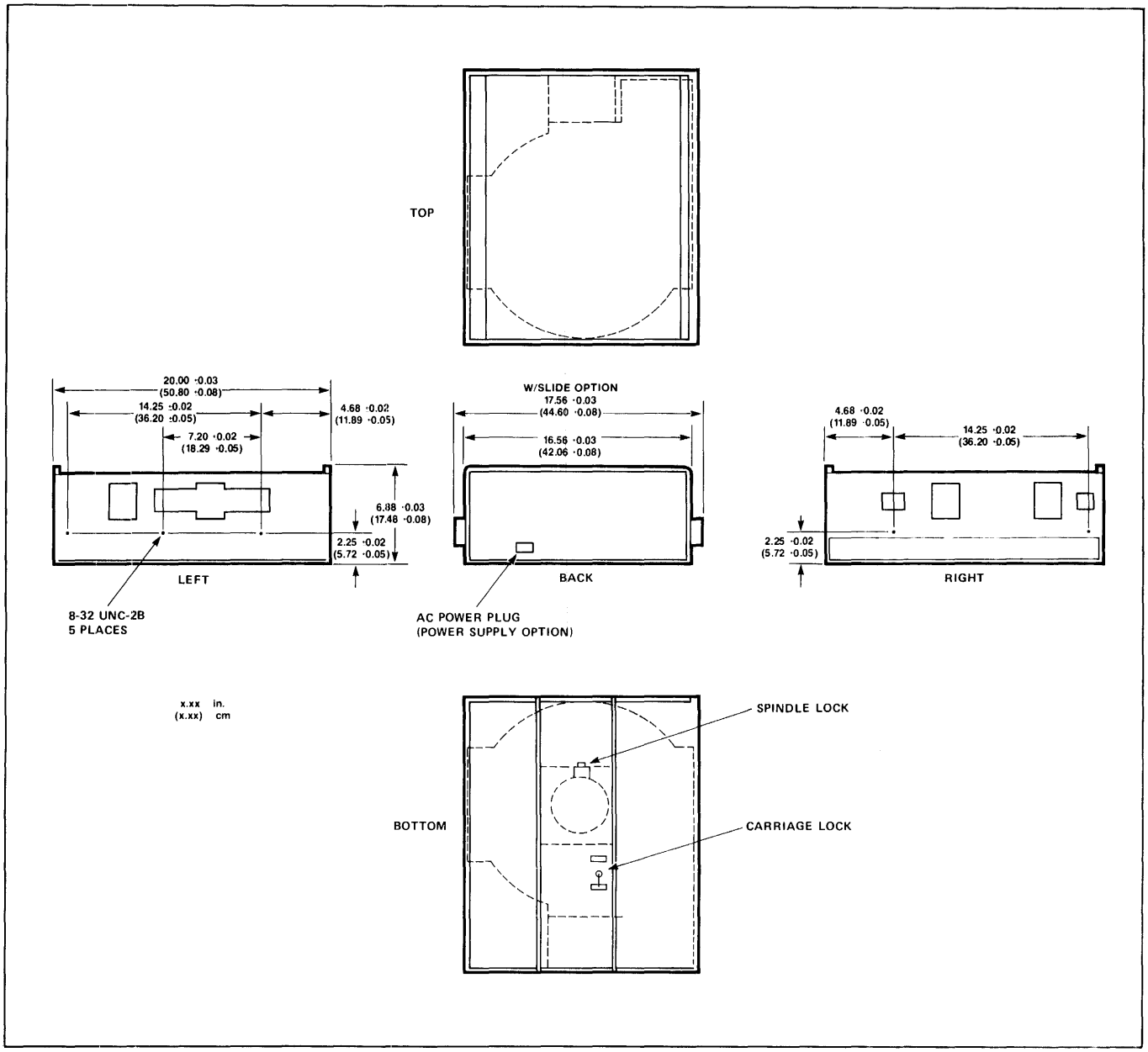


Figure 2-1. PRIAM 14-Inch Disc Drive Dimensions and Mounting

3. RECEIVING, INSTALLATION AND SHIPPING

3.1 Introduction. This section contains procedures for installing all PRIAM 14-inch drives. Included are instructions for unpacking and inspecting, handling guidelines, and shipping instructions.

3.2 Unpackaging the Drive.

3.2.1 Shipping Damage Inspection. The disc drive is packaged to withstand normal handling in a reusable shipping container. It is the customer's responsibility to notify the carrier if shipping damage should occur to the drive.

When the shipment is received, the shipping container should be examined for obvious signs of shipping damage. Most insurance adjusters require inspection of the damaged container. Notify the carrier and PRIAM Customer Service immediately if shipping damage is discovered.

NOTE: When handling the drive while in the shiping container, insure that the container remains in the upright position as indicated by the attached labels.

3.2.2 Removing Drive From Shipping Container. The drive shipping container consists of an outer and inner carton. (See Figure 3-1.) Open

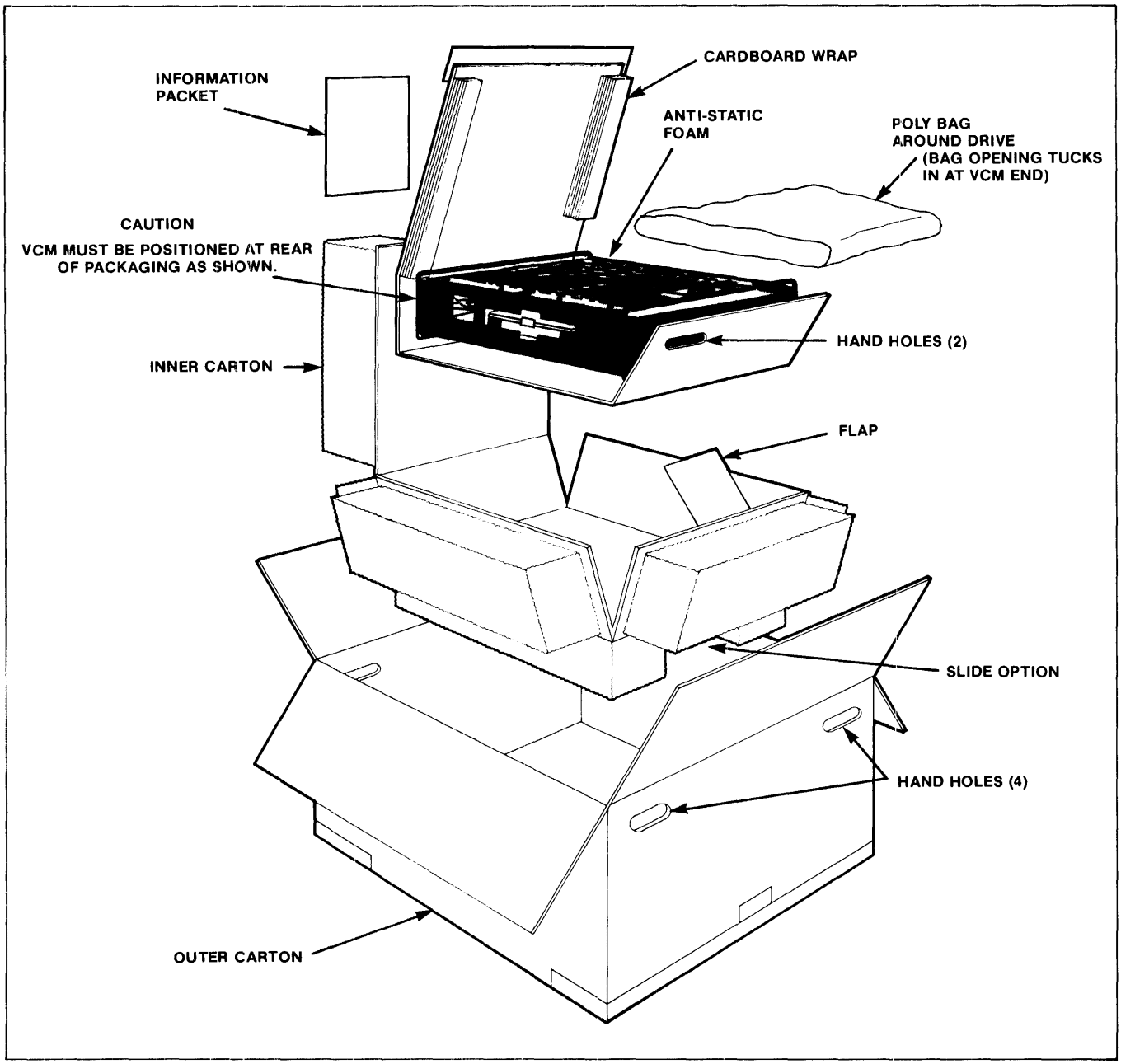


Figure 3-1. Shipping Package

the outer carton by cutting the tape securing the top flaps. Next, cut the tape on the tongue of the inner carton. Fold back the top of the inner carton. Grasp the hand holes at each end of the drive's cardboard wrapping and carefully lift drive out of the inner carton.

CAUTION

The weight of the drive is substantial and if dropped can cause severe damage to the Head/Disk Assembly, which will not be covered under warranty.

Place the drive on a clean, flat surface and remove the protective cardboard and polyethylene wrap. Retain the shipping container for any future shipments of the drive.

3.2.3 Inspection Procedures. After unpacking the disc drive, inspect it thoroughly for damage hidden by the packaging and for loose components or fittings, as follows:

a. Inspect the interior for shipping damage.
b. Examine internally mounted components for loose or missing hardware.
c. Tighten all loose hardware.
d. Clean the frame interior by removing loose debris.
e. Check that head and spindle locks are secure.

3.3 Handling Procedures

3.3.1 Shock and Vibration Precautions. The drives must be handled in a manner as not to exceed the Non-Operational Shock and Vibration limits specified in Table 2.2.

3.3.2 Spindle and Head Locks. Both the drive spindle and the head carriage are locked at the factory prior to shipment. After the drive has been positioned for bench testing or installed in the final system, the spindle and head carriage locks must be set in the "Unlock" position to allow normal operation. Both locks are located on the bottom of the HDA (Head Disc Assembly). See Figure 3-2.

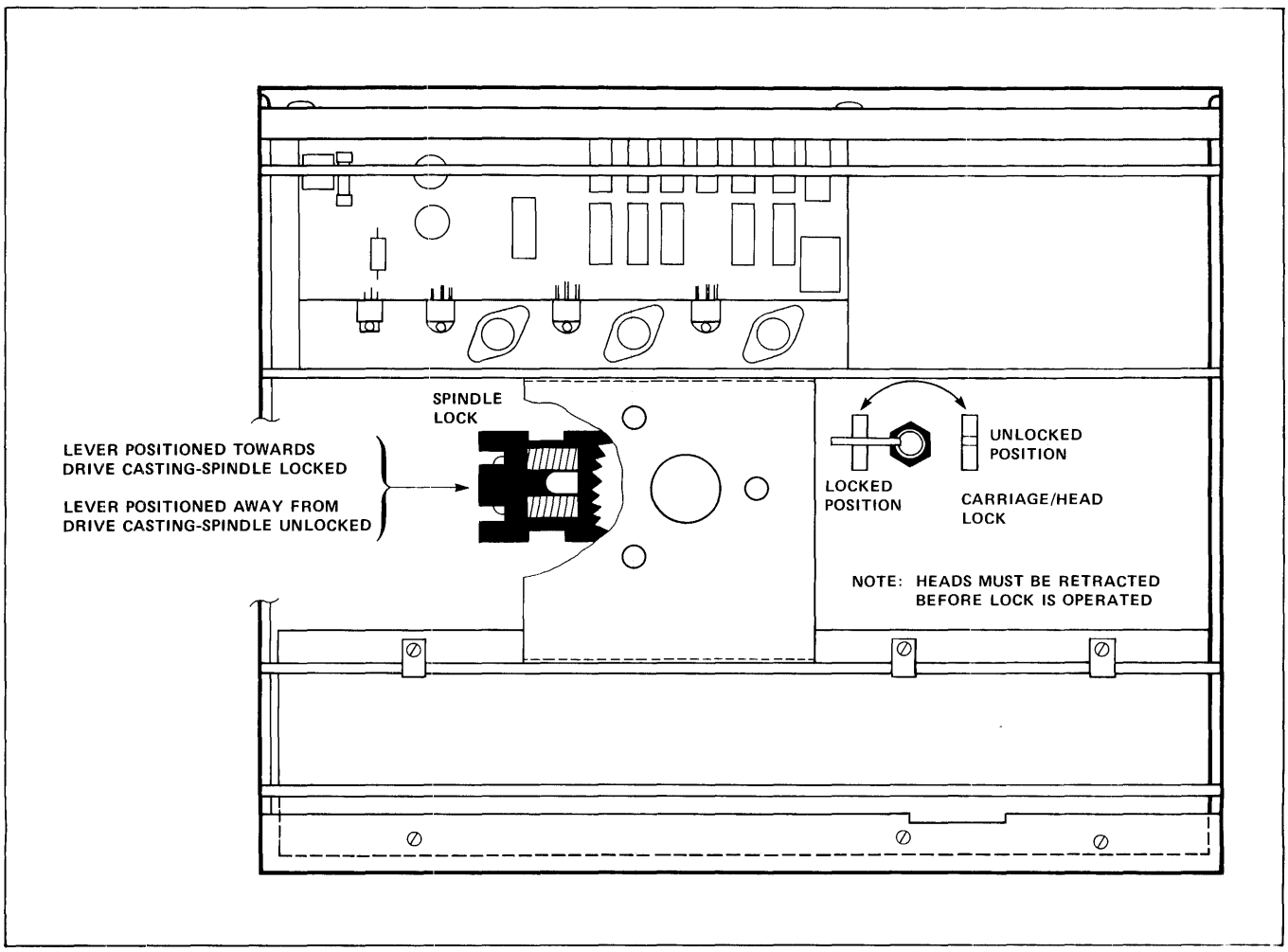


Figure 3-2. Spindle and Head Carriage Locks

3.3.3 Drive Handling Guidelines. Adhere to the steps outlined in Table 3-1 when handling drives.

Table 3-1. Winchester Disk Drive Handling Guidelines (unpacked)

- Always lock spindle/carriage whenever drive is moved. (Do *not* try to lock while drive is spinning.)
- Do *not* drop drive from any height. Drive should be laid down carefully.
- Carts used for transporting drives should have soft rubber wheels to absorb shock.
- Drive should be stored or transported in a vertical position with long dimension horizontal or flat, top up, and drive motor down. Drive must be on a flat surface. Do *not* put papers, etc. under drive.
- Only unlock spindle when drive is in normal operating attitude.
- Do *not* apply power when spindle is locked.
- Do *not* dress or re-position components, wires or cables.
- Do *not* place drives in vertical position closer than 2-3 inches apart to avoid hitting and breaking components.
- Avoid manual rotation of the spindle or movement of the carriage. Damage to the disc surface may occur if the heads are moved across a non-rotating disc surface.
- Do *not* remove plugs from HDA assembly. This may result in contamination which may affect drive operation. Do *not* attempt to disassemble HDA.
- Do *not* lay objects on top of drive, especially metallic objects.

3.4 Shipping Requirements.

3.4.1 Spindle and Carriage Locks. Before packaging a drive for shipment, it is necessary to secure the spindle and carriage locks. (See Figure 3.2.) A sequence down operation must be performed before the drive can be removed from the system and the locks are engaged. After the spindle has come to a complete stop, engage the spindle lock to clamp the fan blades. Also, move the head carriage lock to the "Locked" position since the heads should be retracted into the landing zone by the previous sequence down operation. If the head lock lever cannot be engaged fully *Do Not Force.* Instead, return the lever to the unlocked position, tilt the drive so that the round VCM assembly points downward and then return the carriage lock to the locked position.

3.4.2 Shipping A Stand-Alone Unit. After the drive is removed from the system (with the spindle and carriage locks secure), the drive must be packaged to withstand the environmental extremes specified in Table 2-2. Use of the original PRIAM shipping container is recommended. A user designed shipping container may be substituted if it meets or exceeds the PRIAM non-operating environmental specifications.

NOTE: Failure to ship the drive in a proper container will void its warranty.

Important! Remove slides, brackets, parts of enclosures and cables from the drive before placing it in the shipping container.

3.4.3 Shipping Drive Mounted in an Enclosure. When shipping the drive while it is installed in a system, all environmental specifications in Table 2-2 must be adhered to. Vibrations around 50 Hz should be carefully checked when shipping drives in large mainframe systems, as they can cause the drive to resonate on its protective shock mounts. If the system or enclosure cannot be packaged for shipment so that the drives will meet the specifications in Section 2.2, it is recommended that the drive(s) be removed from the system or enclosure prior to shipment and shipped as a stand-alone unit. (See Section 3.4.2.)

3.5 Functional Testing. The following functional test is a recommended test for incoming receiving inspection to insure that the drive is operational and that no shipping damage has occurred.

	Time	Test
1.	1 min.	Power up drive and get RDY.
2.	15 sec.	Perform max. length seeks.
3.	15 sec.	Perform random seeks.
4.	*	Format, if applicable.
5.	1-3 min.	Sequentially write all cylinders and all heads with worst case pattern. (924..., 249..., 492...)
6.	1-3 min.	Sequentially read what was written.
7.	1 min.	Random Write and Read.

* Time dependent on size of drive and formatter used.

4. PRIAM INTERFACE OPERATION

This section provides information for setting up all 14-inch drives having a PRIAM Interface for use in an OEM system. This includes power selection, jumper and switch settings, interface signal definitions and other information to insure proper system operation.

4.1 Mounting. All PRIAM 14-inch drives can be mounted in a standard 19-inch rack. PRIAM offers an optional slide mounting kit for use with the 14-inch drive models. See Figure 2-1 for mounting dimensions.

4.2 Power Supply Setup. If a PRIAM optional power supply is used, check the AC voltage selection circuit board prior to applying power. This board is adjacent to the AC input plug, and is an integral part of the power supply. To select a voltage, remove the selection circuit board and reinsert it so that the proper AC voltage designation (100, 120, 220, or 240) is visible. Also check the fuse value. A 5-amp fuse is used with 100 or 120 VAC operation, while a 2.5-amp fuse is used with 220 or 240 VAC operation. No modification is required for changing between 60 Hz and 50 Hz power.

4.3 Switch Settings. The drive address, write protect parameters, and sector size are all switch selectable. The switches are located on the main PCB. Referring to Table 4-1, set the switches according to the desired operating conditions for the applicable Model Drive. See Figures 4-1, 4-2 and 4-5 for the locations of the applicable DIP switches.

Table 4-1. DIP Switch Selection

		DRIVE MODEL NUMBER			
		3350-01	6650-10/3350-10	15450-10	
DIP SWITCH LOCATION ON PCB		16R	10K	1J	
SWITCH NUMBER/ FUNCTION	1	DEVICE SELECT 1	DEVICE SELECT 1	DEVICE SELECT 1	
	2	DEVICE SELECT 2	DEVICE SELECT 2	DEVICE SELECT 2	
	3	DEVICE SELECT 3	DEVICE SELECT 3	DEVICE SELECT 3	
	4	DEVICE SELECT 4	DEVICE SELECT 4	DEVICE SELECT 4	
	5	OFF-SKIP DEFECT RECORD PROTECTED	ON-SKIP DEFECT RECORD PROTECTED		
	6	WRITE ENABLE HD 0	ON-WRITE ENABLE		
	7	WRITE ENABLE HD 1	WRITE CLOCK OFF-OPEN LOOP ON-CLOSED LOOP (normal)		
	8	WRITE ENABLE HD 2	ON-INVERTED ø OFF-NORMAL ø		
DIP SWITCH LOCATION ON PCB		23N	11K	9F	
			SECTORS / BYTES	SECTORS / BYTES	
SWITCH NUMBER/ FUNCTION	1	2048 BYTES/SECTOR	1 / 16	1 / 16	
	2	1024 BYTES/SECTOR	2 / 32	2 / 32	
	3	512 BYTES/SECTOR	4 / 64	4 / 64	
	4	256 BYTES/SECTOR	8 / 128	8 / 128	
	5	128 BYTES/SECTOR	16 / 256	16 / 256	
	6	64 BYTES/SECTOR	32 / 512	32 / 512	
	7	32 BYTES/SECTOR	64 / 1024	64 / 1024	
	8	16 BYTES/SECTOR	OFF-SECTOR/TRACK ON-BYTES/SECTOR	OFF-SECTOR/TRACK ON-BYTES/SECTOR	

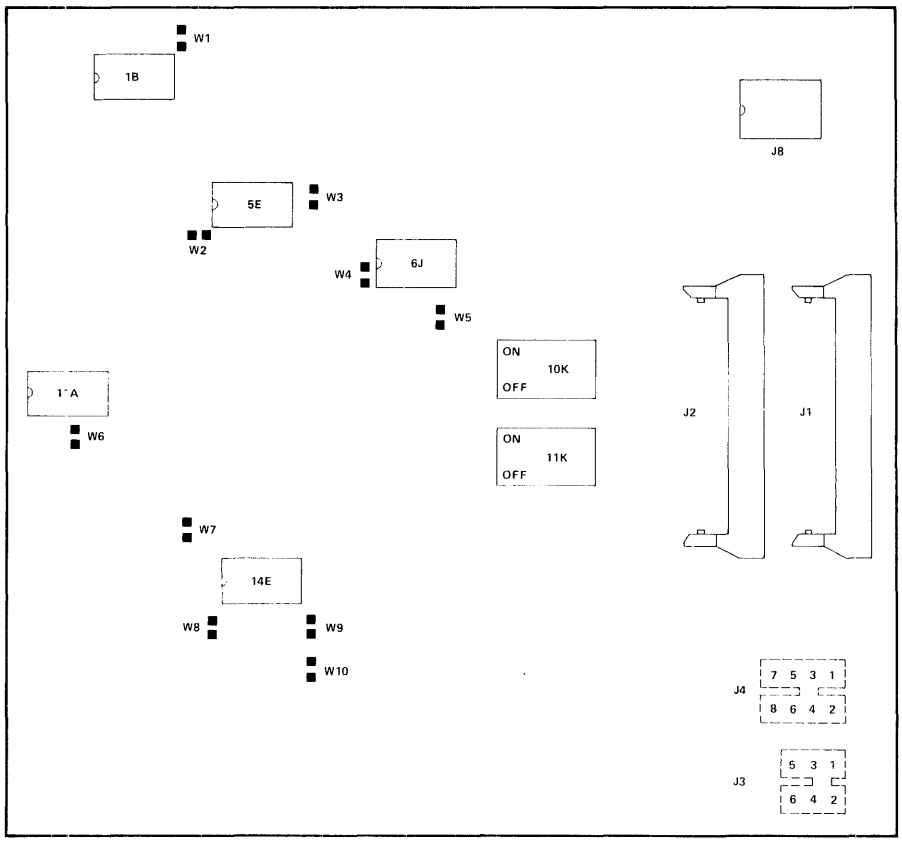


Figure 4-1. Jumper and DIP Switch Locations for Assembly P/N 200113

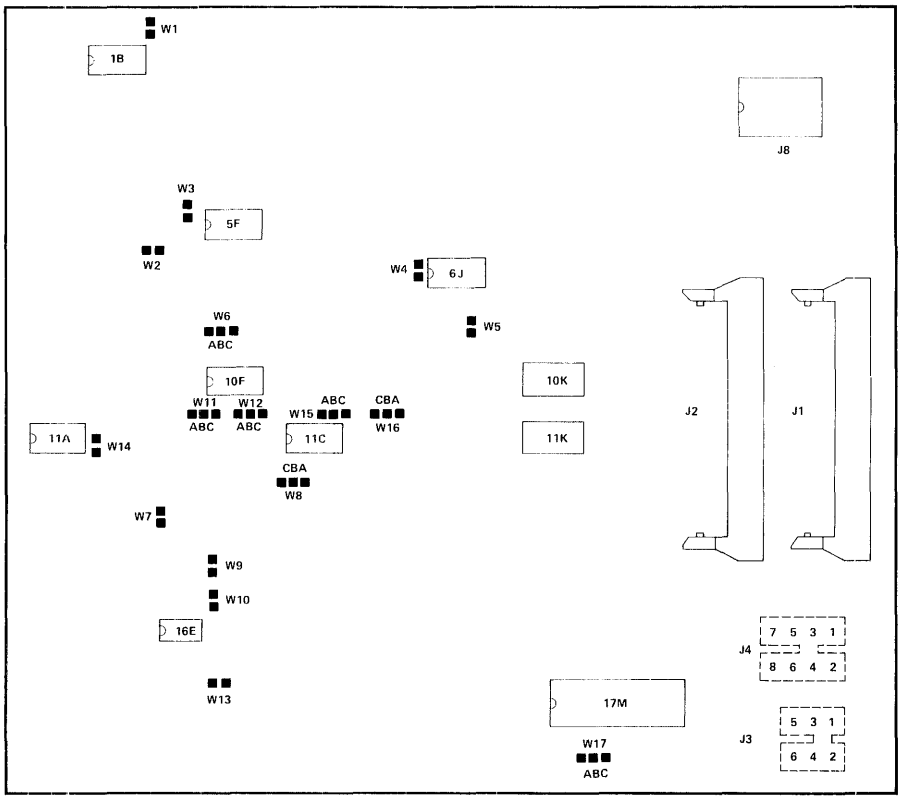


Figure 4-2. Jumper and DIP Switch Locations for Assembly P/N 200173

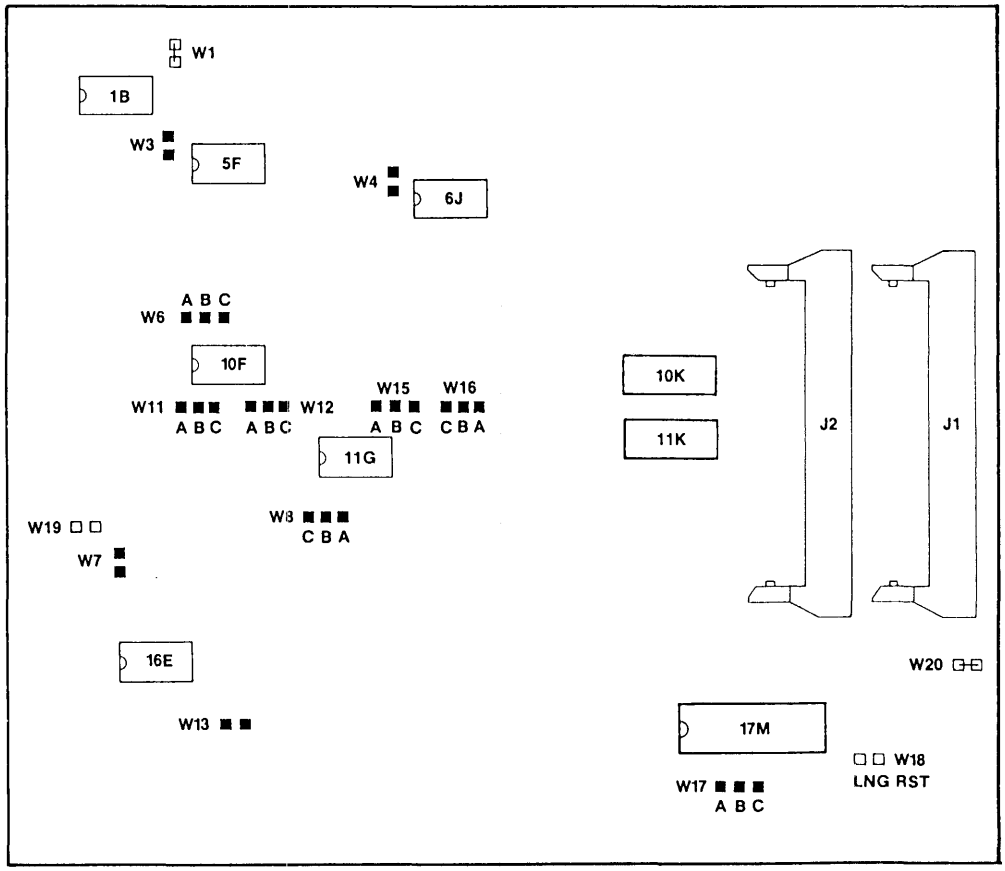


Figure 4-3. Jumper Locations for PCB Assembly 200248-01/02

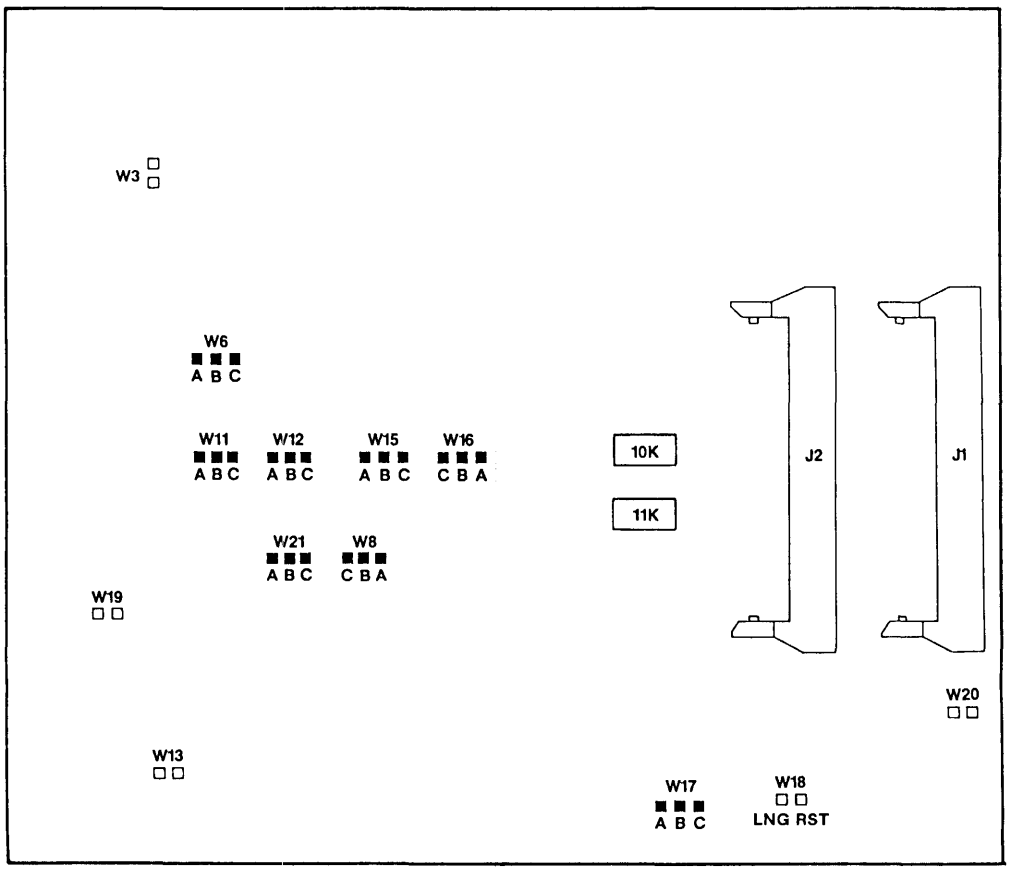


Figure 4-4. Jumper Locations for PCB Assembly 200248-21/22

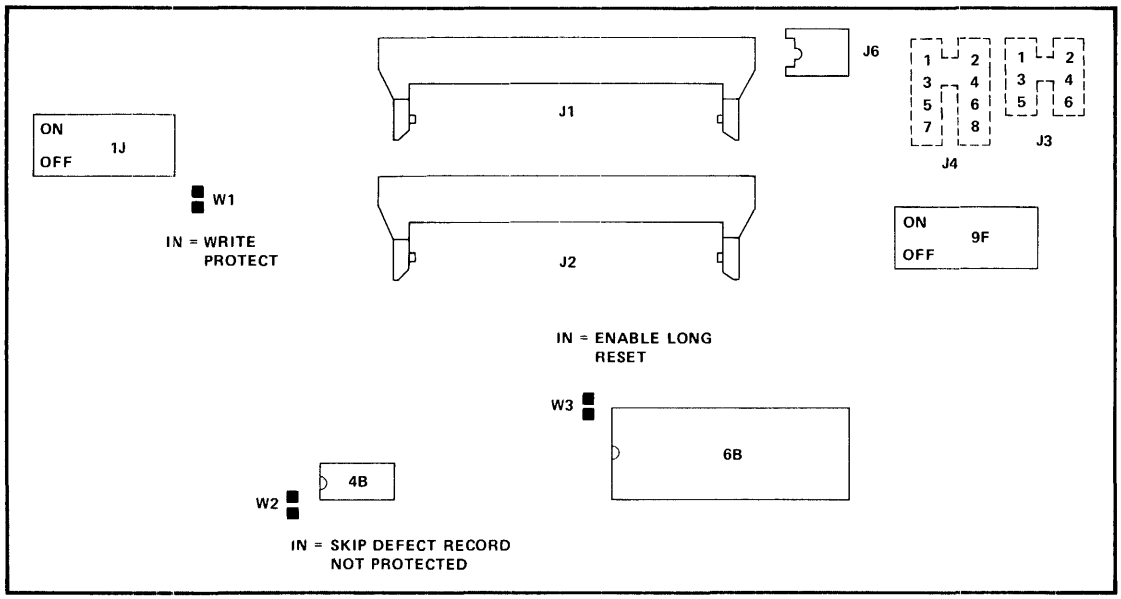


Figure 4-5. Jumper Definitions and Locations and DIP Switch Locations for PCB Assembly 200208/200398

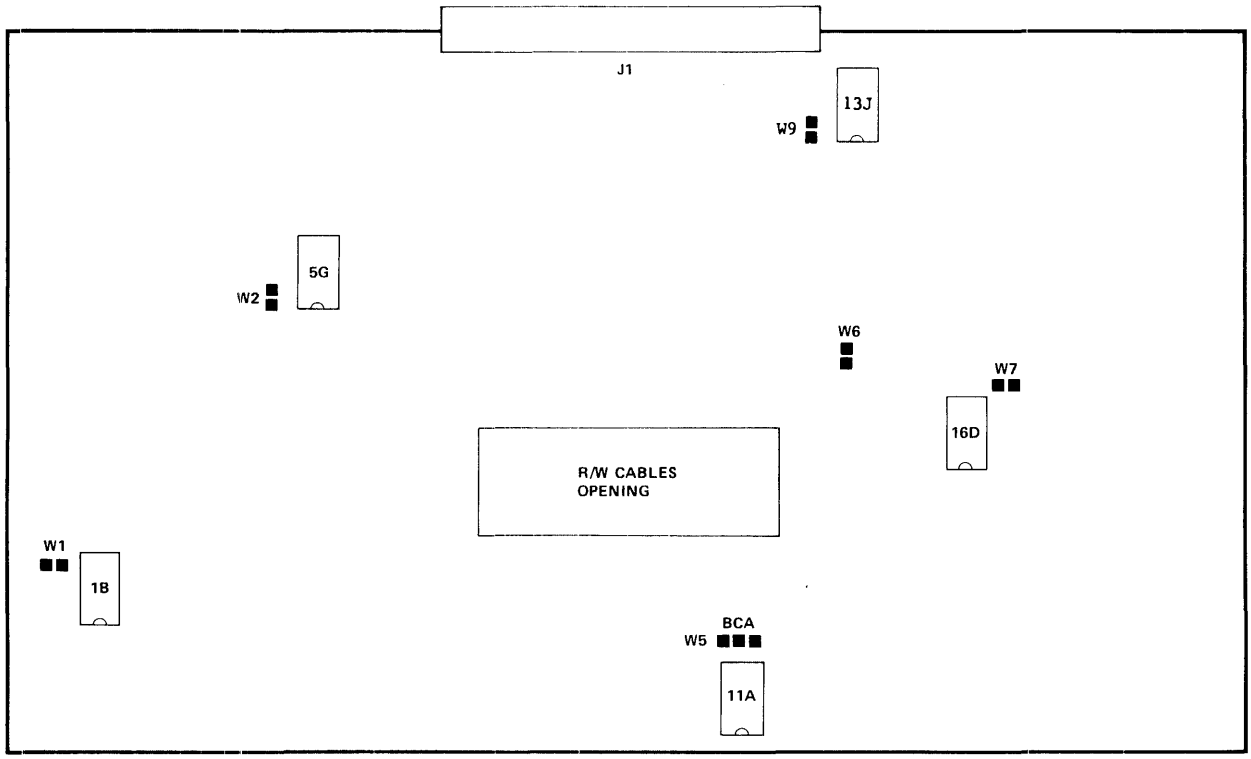


Figure 4-6. Jumper Locations for PCB Assembly 200213

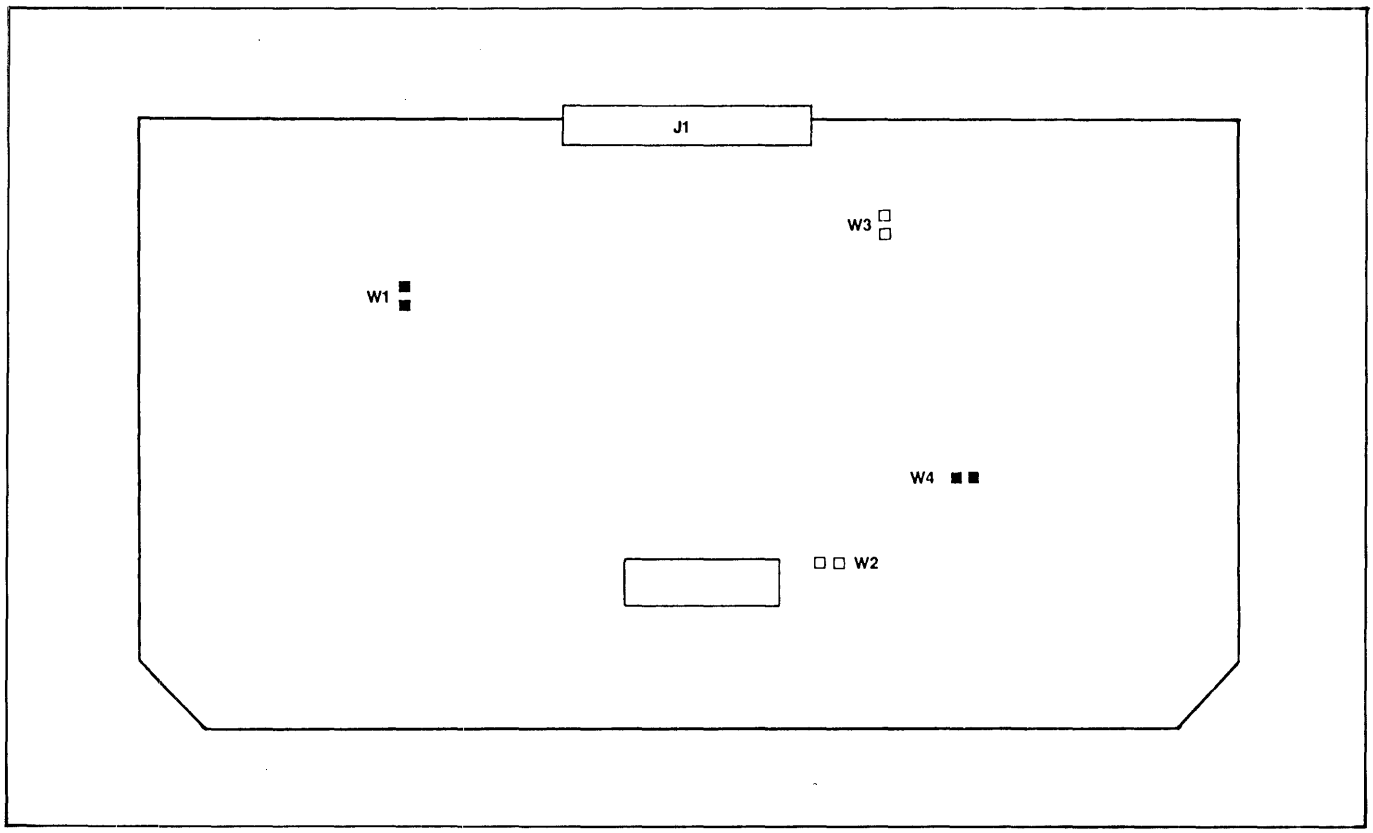


Figure 4-7. Jumper Locations for PCB Assembly 200514-1/200515-1

4.4 Jumper Settings. Jumpers are black conductive tabs that can be inserted on board pins to complete a particular circuit. Although most of these are used only at the factory to facilitate testing, some have user selectable functions. It is important that all jumpers be installed in their proper locations. See Figures 4-1 to 4-6.

Refer to Table 4.2 for jumper position to enable the correct operating conditions for the application.

4.5 Cabling Requirements. All drive signal connections are made via a single 50-pin ribbon cable connector. A second 50-pin connector is available on the main PCB for daisy chaining to another drive or for a terminator for the last drive in the string. Up to four drives may be daisy chained.

A separate connector for DC power is provided. If the optional power supply is installed, then its output is connected to this DC power connector and AC power must be supplied to the optional power supply.

An 8 pin DIP socket for remote write protect control, fault clearing and drive status is also provided on the Main PCB.

4.5.1 Interface Connectors. The interface cables and connectors are defined as follows:

1. Interface Connectors

The interface connectors are 50-pin ribbon cable connectors and provide for interface cable and terminator connections. The pins are numbered 1 through 50. A recommended mating connector is 3M 3425-0000. The pins are defined in Figure 4-9.

2. DC Power Connector

This connector is used to supply DC power to the drive. It is a 6-pin AMP MATE-N-LOK connector, and the recommended mating connector is an AMP 1-480270-0 socket with AMP 60619-1 pins.

Table 4-2. Jumper Selection

Model	3350-10				6650-10			15450-10			
Jumper Number	200113	200173-01	200248-01	200248-21	200173-02	200248-02	200248-22	200208	200213	200514-1	200515-1
W1	IN	IN	IN	X	IN	IN	X	USO	IN	IN	IN
W2	IN	IN	X	X	IN	X	X	USO	IN	OUT	OUT
W3	IN	IN	IN	IN	IN	IN	IN	USO	X	OUT	IN
W4	IN	IN	IN	X	IN	IN	X	X	X	IN	IN
W5	IN	IN	X	X	IN	X	X	X	BC	X	X
W6	IN	AB	AB	AB	BC	BC	BC	X	IN	X	X
W7	IN	IN	IN	X	IN	IN	X	X	IN	X	X
W8	IN	AB	AB	AB	BC	BC	BC	X	X	X	X
W9	IN	IN	X	X	IN	X	X	X	NOTE 2	X	X
W10	IN	IN	X	X	IN	X	X	X	X	X	X
W11	X	AB	AB	AB	BC	BC	BC	X	X	X	X
W12	X	BC	BC	BC	AB	AB	AB	X	X	X	X
W13	X	IN	IN	IN	IN	IN	IN	X	X	X	X
W14	X	IN	X	X	IN	X	X	X	X	X	X
W15	X	AB	AB	AB	BC	BC	BC	X	X	X	X
W16	X	AB	AB	AB	BC	BC	BC	X	X	X	X
W17	X	AB	AB	AB	BC	BC	BC	X	X	X	X
W18	X	X	USO	USO	X	USO	USO	X	X	X	X
W19	X	X	OUT	OUT	X	OUT	OUT	X	X	X	X
W20	X	X	USO	USO	X	USO	USO	X	X	X	X
W21	X	X	X	BC	X	X	BC	X	X	X	X

1. X = Jumper does not exist.
2. For -03 (MIS), jumper must be installed.
3. USO = User Selected Option (See Figure 4-3).

Table 4-3. DC POWER CONNECTOR

PIN	VOLTAGE
1	Ground
2	+24 VDC
3	−5 VDC
4	−12 VDC
5	+5 VDC
6	Ground (+24V Return)

3. AC Power Connector

This is a 3-pin connector used to supply AC power to the disc drive when the PRIAM optional power supply is used. The mating connector is a Belden 5PH-386 or equivalent.

Table 4-4 AC POWER CONNECTOR

PIN	VOLTAGE
L	100 to 240 VAC (HOT)
E	Frame Ground
N	100 to 240 VAC (COMMON)

4. Remote Panel Connector

This is an 8-pin DIP socket connector. It provides limited remote status sensing and control as described in Table 4-5.

Table 4-5 Remote Panel Connector

PIN	SIGNAL NAME
1	− WRITE PROTECT (CONTROL)
2	− FAULT RESET (CONTROL)
3	− READY (STATUS)
4	Ground
5	− BUSY (STATUS)
6	− DRIVE FAULT (STATUS)
7	Reserved
8	+5 VDC (POWER)

Table 4-6. Remote Write Protect Function
(Front Panel Switch Write Protects when Closed)

3350-10 6650-10	Open Switch 10K-6 to enable Remote Write Protect Switch
15450-10	Remove Jumper W1 to enable Remote Write Protect Switch

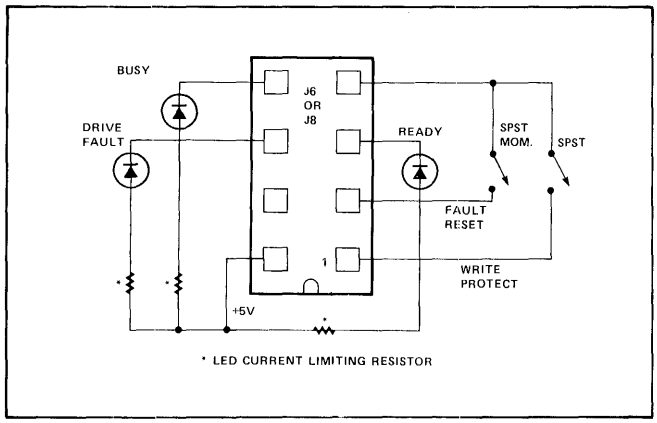


Figure 4-8. Typical Test Panel Schematic

4.5.2 Interface Cable Characteristics

1. Interface Cable

Type:	Flat Ribbon
Impedance:	105 ohms
Wire Size:	28 AWG
Propagation Time:	1.37 nsec/ft.
Maximum Cable Length:	25 ft.

2. DC Power Cable

Type:	6 conductor Vinyl
Wire Size:	18 AWG Stranded

3. AC Power Cable

Type:	SVT Vinyl
Power:	1250 watts, 10 amps

4.6 Signal Functional Requirements. The interface signal names of the PRIAM 14-inch disk drives are listed in Figure 4-9.

Pin	Signal Name	Line Type
1	Ground	Ground
2	+ DBUS 0	Bidirectional/Single
3	+ DBUS 1	Bidirectional/Single
4	+ DBUS 2	Bidirectional/Single
5	+ DBUS 3	Bidirectional/Single
6	+ DBUS 4	Bidirectional/Single
7	+ DBUS 5	Bidirectional/Single
8	+ DBUS 6	Bidirectional/Single
9	+ DBUS 7	Bidirectional/Single
10	Ground	Ground
11	– READ GATE	Received/Single
12	Ground	Ground
13	– RESET	Received/Single
14	Ground	Ground
15	– WRITE GATE	Received/Single
16	Ground	Ground
17	– RD	Received/Single
18	– WR	Received/Single
19	+ AD 1	Received/Single
20	+ AD 0	Received/Single
21	Ground	Ground
22	– DRIVE SELECT 1	Received/Single
23	– DRIVE SELECT 2	Received/Single
24	– DRIVE SELECT 3	Received/Single
25	– DRIVE SELECT 4	Received/Single
26	Ground	Ground
27	Ground	Ground
28	+5 VDC (Terminator Power)	Diode OR'ed/Single*
29	– HEAD SELECT 4	Received/Single
30	– HEAD SELECT 2	Received/Single
31	– HEAD SELECT 1	Received/Single
32	Ground	Ground
33	– INDEX	Transmitted/Single
34	Ground	Ground
35	– READY	Transmitted/Single
36	Ground	Ground
37	– SECTOR MARK	Transmitted/Single
38	Ground	Ground
39	+ WRITE DATA	Received/DIFF
40	– WRITE DATA	Received/DIFF
41	Ground	Ground
42	+ WRITE CLOCK	Received or Transmitted/DIFF
43	– WRITE CLOCK	Received or Transmitted/DIFF
44	Ground	Ground
45	+ READ/REFERENCE CLOCK	Received or Transmitted/DIFF
46	– READ/REFERENCE CLOCK	Received or Transmitted/DIFF
47	Ground	Ground
48	+ READ DATA	Transmitted/DIFF
49	+ READ DATA	Transmitted/DIFF
50	Ground	Ground

*Supplied by drive. NOT used by host.

Figure 4-9. PRIAM Interface Connector

4.6.1 Interface Signal Descriptions. This section gives a functional description and DC characteristics for the signals on the 50-pin connector.

1. + *DBUS 0-7.* This high-active 8-bit wide bus is used to transfer commands and status (head carriage control and interface) between the disc drive and the controller. These lines connect directly to an 8304B bus transceiver, as shown in Figure 4-10. DC characteristics are listed in Table 4-7. These lines should be terminated at each end.

Table 4-7. DBUS Transceiver DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OL}	Output Low Level		0.5	V	I_{OL} = 48 mA
V_{OH}	Output High Level	2.4		V	I_{OH} = −5 mA
I_{OFF}	Output Off Current		−0.2	mA	V_{OFF} = 0.45 V
			+0.2	mA	V_{OFF} = 5.25 V
V_{IL}	Input Low Level		0.9	V	
V_{IH}	Input High Level	2.0		V	

2. + *AD 0-1.* This high-active 2-bit wide address bus is used to select one of three registers into which data can be stored, or one of three registers from which data can be read. These lines connect directly to a 74LS244 Schmit-triggered receiver gated by DRIVE SELECTED, as shown in Figure 4-11. The DC characteristics are listed in Table 4-8. These lines should be terminated at the drive end.

3. - *RD.* This low-active signal is used to gate the contents of the selected register (decode of AD1 and AD0) onto the DBUS. This line is connected to a 74LS2244, gated by DRIVE SELECTED, as shown in Figure 4-11. The DC characteristics are listed in Table 4-8. This line should be terminated at the drive end.

4. - *WR.* This low-active signal is used to gate the DBUS into the selected register (decode of AD1 and AD0). This line is connected to a 74LS244, gated by DRIVE SELECTED, as shown in Figure 4-11. The DC characteristics are listed in Table 4-8. This line should be terminated at the drive end.

5. - *RESET.* This low-active signal resets the drive logic. If the drive is sequenced down when RESET occurs, it will remain sequenced down. If the drive is sequenced up, it will remain sequenced up and the head carriage will restore to cylinder zero. This line is connected to a 74LS244, gated by DRIVE SELECTED, as shown in Figure 4-11. The DC characteristics are listed in Table 4-8. This line should be terminated at the drive end.

6. - *WRITE GATE.* This low-active signal enables the writing of data by a selected head. This line is connected to a 74LS244, as shown in Figure 4-11. The DC characteristics are listed in Table 4-8. This line should be terminated at the drive end.

7. - *READ GATE.* This low-active signal initiates synchronization of the drive's variable frequency oscillator for data separation. READ GATE must be enabled during a gap. This line is connected to a 74LS244, as shown in Figure 4-11. The DC characteristics are listed in Table 4-8. This line should be terminated at the drive end.

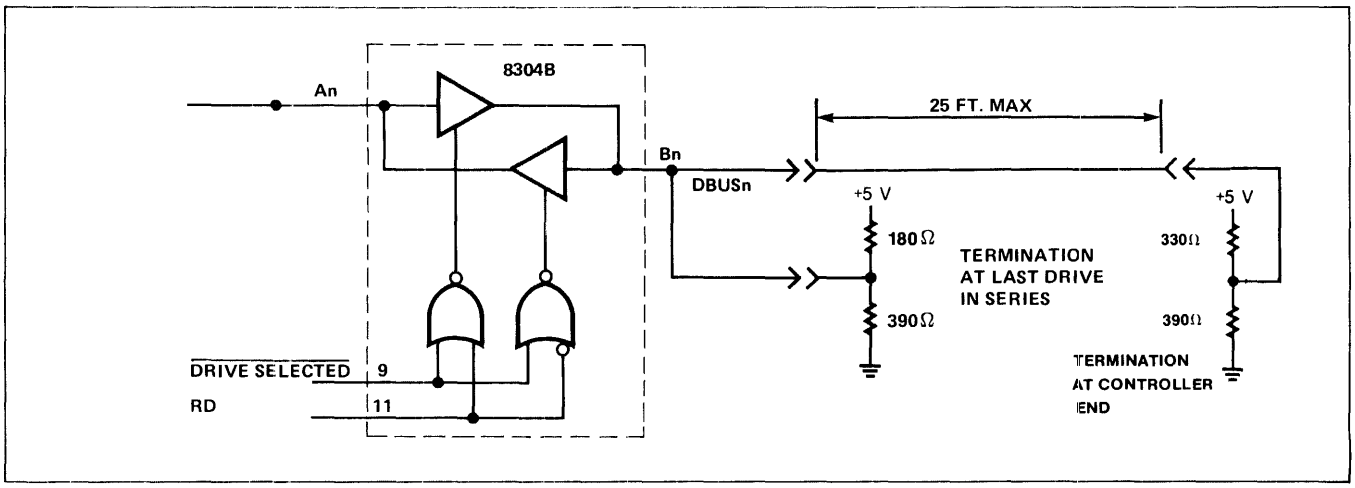


Figure 4-10. DBUS Transceiver

Table 4-8. Single End Line Receiver Gated by DRIVE SELECTED Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IH}	Input High Level	2.0		V	
V_{IL}	Input Low Level		0.8	V	
I_{IH}	High Level Input Current		0.02	mA	$V_I = 2.7$ V
I_{IL}	Low Level Input Current		−0.2	mA	$V_I = 0.4$ V

8. - *DRIVE SELECT 1-4.* These low-active signals (decoded) enable drive selection. No reading, writing, register selection, or command response will occur unless the drive is selected. These lines are connected to single-ended receivers, as shown in Figure 4-12. The DC characteristics are listed in Table 4-9. These lines should be terminated at the drive end.

9. - *HEAD SELECT 1, 2, and 4.* These low-active signals are used to select the desired data head for reading or writing. Head selection decoding is shown in Table 4-13. These lines are connected to single-ended receivers, as shown in Figure 4-12. The DC characteristics are listed in Table 4-9. These lines should be terminated at the drive end.

Table 4-9. Single End Line Receiver DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{T+}	Positive-going Threshold	1.4	1.9	V	
V_{T-}	Negative-going Threshold	0.5	1.0	V	
I_{IH}	High Level Input Current		0.02	mA	$V_I = 2.7$ V
I_{IL}	Low Level Input Current		−0.4	mA	$V_I = 0.4$ V

Cable connections should be terminated at the last drive.

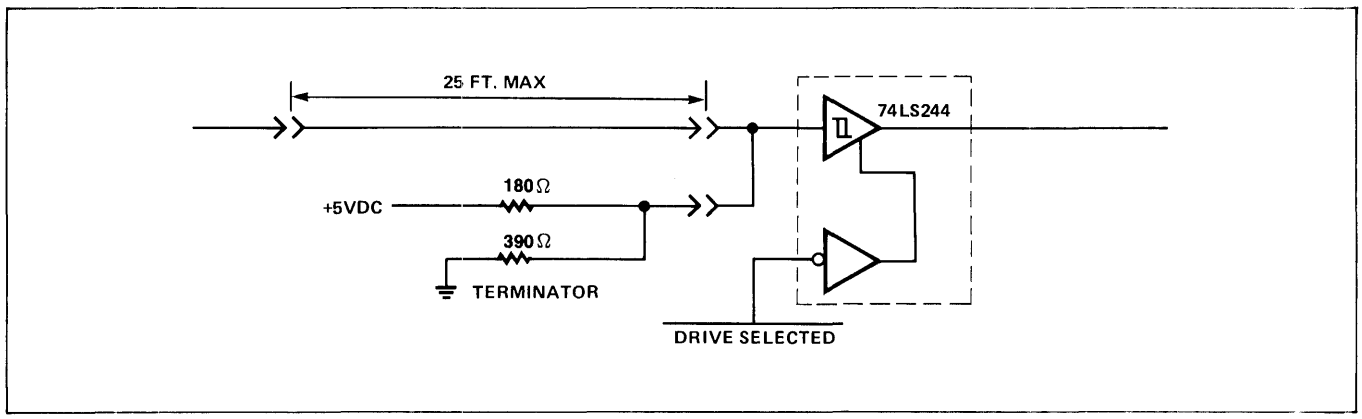


Figure 4-11. Single End Line Receiver Gated by DRIVE SELECT

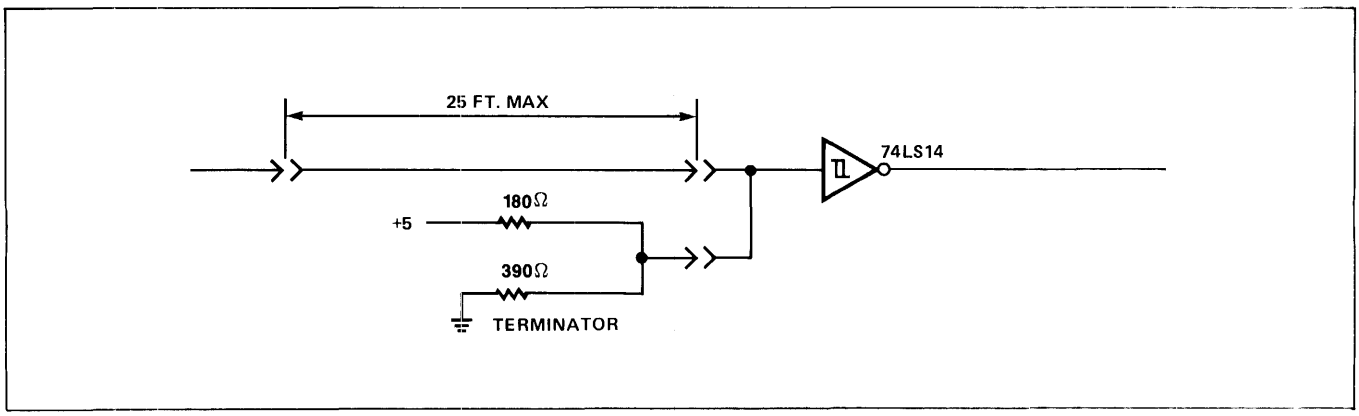


Figure 4-12. Single End Line Receiver

10. - *READY.* This low-active signal from the drive indicates that the drive is up to speed and ready to read, write, or seek. This line is driven by a 75462 open collector driver, as shown in Figure 4-13. The DC characteristics are listed in Table 4-10. This line should be terminated at the controller end.

11. - *INDEX.* This low-active signal occurs once per revolution and indicates the beginning of a track. This line is driven by a 75462 open collector driver, as shown in Figure 4-13. The DC characteristics are listed in Table 4-10. This line must be terminated at the controller end.

12. - *SECTOR MARK.* This low-active signal indicates the beginning of a sector. This line is driven by a 75462 open collector driver, as shown in Figure 4-13. The DC characteristics are listed in Table 4-10. This line must be terminated at the controller end.

Table 4-10. Single End Line Driver DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{OH}	High Level Output Current		0.1	mA	
I_{OL}	Low Level Output Current	300		mA	
V_{OH}	High Level Output Voltage	2.4		V	
V_{OL}	Low Level Output Voltage		0.8	V	$I_{OL} = 300$ mA

This line must be terminated at the controller end.

13. +, - *WRITE DATA.* WRITE DATA is a NRZ serial data signal synchronous with WRITE CLOCK. WRITE DATA is received by an RS422 type differential line receiver as shown in Figure 4-14. The DC characteristics are listed in Table 4-11. This line should be terminated at the drive end.

14. +, - *WRITE CLOCK.* This signal is switch selectable. It can be a square wave signal from the controller which is phase locked to the WRITE DATA, or if the switch is enabled, it can be a reference signal from the drive to the controller to provide clocking and synchronization for WRITE DATA. The controller should be designed so that WRITE DATA is stable at the drive connector during the negative transition of WRITE CLOCK. WRITE CLOCK is received by an RS422 type differential line receiver, as shown in Figure 4-14. The DC characteristics are listed in Table 4-11. These lines should be terminated at the drive end. If long cables are used, cable delays must be considered.

15. +, - READ/*REFERENCE CLOCK.* This square wave signal provides clocking and synchronization for reading and writing data. It is derived from either the servo clock or the VFO synchronized to the READ DATA signal. It is driven by an RS422 type differential driver, as shown in Figure 4-14. The DC characteristics are listed in Table 4-12. These lines should be terminated at the controller end.

16. +, - *READ DATA.* This serial NRZ signal is used to transmit data from the drive to the controller. This output is valid 10 microseconds after READ GATE is enabled. It is driven by an RS422 type differential driver, as shown in Figure 4-14. The DC characteristics are listed in Table 4-12. These lines should be terminated at the controller end.

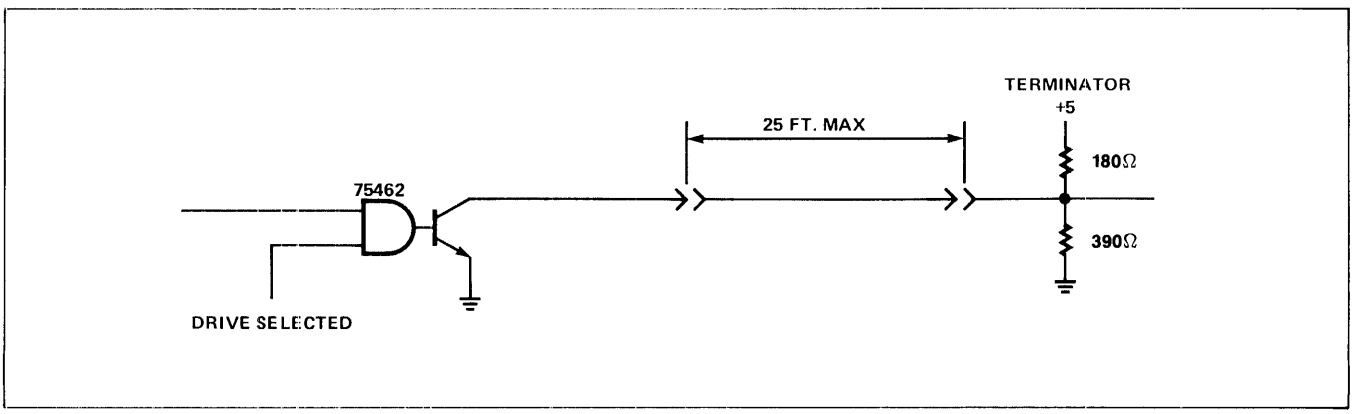


Figure 4-13. Single End Line Driver

Table 4-11. Differential Line Receiver DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{TH}	Differential Input High Threshold		0.2	V	
V_{ICR}	Common Mode Input Range	± 15		V	
$I_{I(REC)}$	Receiver Input Current		2.3	mA	

Table 4-12. Differential Line Driver DC Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}	High Level Output Voltage	2.5		V	$I_{OH} = -20$ mA
V_{OL}	Low Level Output Voltage		0.32	V	$I_{OL} = 20$ mA
I_{OZ}	Output Off Current		± 0.02	mA	
I_{OH}	High Level Output Current		− 20	mA	
I_{OL}	Low Level Output Current		+ 20	mA	
I_{OS}	Short Circuit Output Current	− 30	− 150	mA	

Note: The last drive in a string should be terminated.

4.6.2 Serial Data Transfer Control Signals. Of the interface signals described in Section 4.6.1, there are several that are used specifically to facilitate serial data transfer between the disc drive and the controller. These are described below, with additional details.

1. *INDEX*—The INDEX pulse occurs whenever the servo track index mark is detected, to indicate the beginning of a track.

2. *READY*—The READY signal indicates that the selected drive is ready to read, write, or seek. When READY is false, the controller should not initiate WRITE, READ, or SEEK commands. However, READY will go false when a SEEK command is initiated. READY will later go true when the head carriage is positioned on the specified cylinder, if no fault condition exists.

3. *SECTOR MARK*—The SECTOR MARK pulse occurs at the beginning of each sector (sector size is selectable by setting the appropriate DIP switches on the Main PCB).

4. *HEAD SELECT 1, 2, and 4*—These low-active signals are used to select the data head, as shown in Table 4-13.

Table 4-13. Head Selection.

Head Select 1	Head Select 2	Head Select 4	Selected Head 3350 6650	15450
High	High	High	Zero	Zero
Low	High	High	One	One
High	Low	High	Two	Two
Low	Low	High	Zero*	Three
High	High	Low	Zero*	Four
Low	High	Low	One*	Five
High	Low	Low	Two*	Six
Low	Low	Low	Zero*	Zero*†

*Selected by default because of the number of heads available.
†On drives with the Main PCB below EC1719 a drive fault will occur.

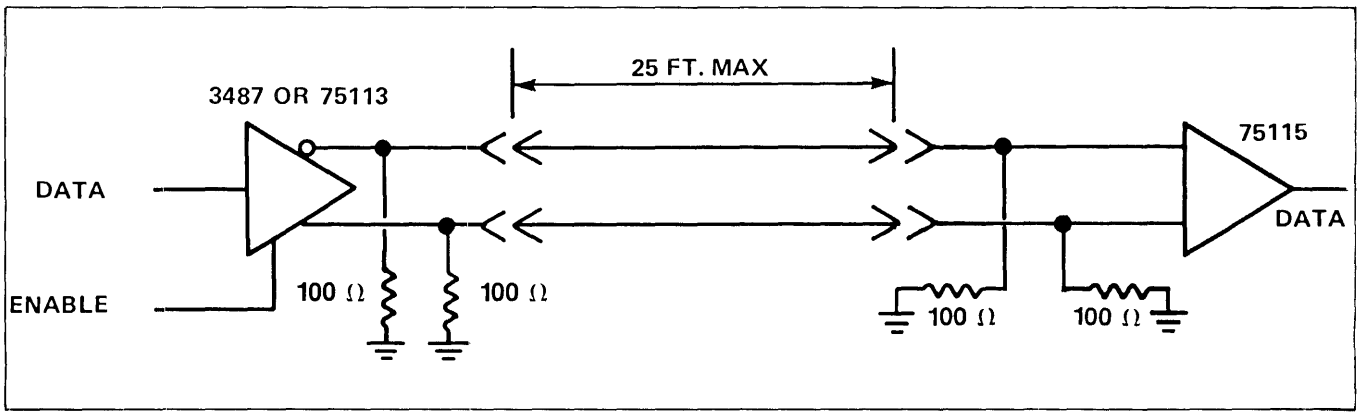


Figure 4-14. Differential Line Drivers and Receivers

5. *WRITE GATE*—WRITE GATE when active, enables data to be written on the disc. READY must be true before write gate is activated.

Table 4-14. Drive Fault Conditions

1. WRITE GATE without write current at the head.
2. Write current at the head without WRITE GATE.
3. WRITE GATE without READY.
4. WRITE GATE with WRITE PROTECT.
5. WRITE GATE occuring between INDEX and the first SECTOR MARK when the Skip Defect Record is protected.
6. More than one head selected.
7. No transitions during write.
8. Spindle speed error.
9. RESET while drive is Sequenced Up.
10. Off-Track condition when track following. (READY true)
11. Failure to Restore.
12. Software Error (time-out of watch dog timer).

6. *WRITE CLOCK*—WRITE CLOCK provides clocking and synchronization for WRITE DATA. The controller generates WRITE CLOCK by echoing the READ/REFERENCE CLOCK signal back to the drive, with suitable phase delay relative to WRITE DATA.

7. *WRITE DATA*—WRITE DATA provides the data to be stored on the disc. NRZ (non-return-to-zero) data is required for WRITE DATA. READ/REFERENCE CLOCK (received from the drive) is used by the controller to clock WRITE DATA on the positive edge. READ/REFERENCE CLOCK is then retransmitted to the drive as WRITE CLOCK. The negative edge of WRITE CLOCK is used to strobe WRITE DATA into the drive's encoder circuitry.

8. *READ GATE*—READ GATE must be enabled in a gap area (all 0s recorded), and at least 9 microseconds before the sync byte. READ GATE enables the VFO clock to synchronize with the information from the read head. Activating READ GATE during a data record may cause the VFO to spuriously lock in an incorrect phase relationship for decoding the recorded information.

   8.6 microseconds after the leading edge of READ GATE, the internal READ CLOCK signal is enabled to the READ/REFERENCE CLOCK interface signal lines.

9. *READ/REFERENCE CLOCK*—READ/REFERENCE CLOCK provides clocking and synchronization for reading and writing data. When READ GATE is not active, READ/REFERENCE CLOCK is switched to the PLO clock, which is phased locked to the servo signal. A change in the phase of READ/REFERENCE CLOCK will occur when it is switched between the servo and VFO clocks.

10. *READ DATA*—Data from the drive is in serial NRZ (non-return-to-zero) form, and is synchronized with READ/REFERENCE CLOCK after a 10 microsecond delay from the leading edge of READ GATE. READ DATA may not be valid for the first 10 microseconds after READ GATE is enabled.

4.6.3 User-Accessible Registers. The user's controller sends control commands and target cylinder addresses to the disc drive via the eight bidirectional bus lines DBUS 0-7. The disc drive sends status information and current cylinder address information to the controller via these same eight lines. DBUS 0-7 is a tri-state bus, and thus these lines present an open circuit to the controller's data bus unless they have been activated by DRIVE SELECT. An active DRIVE SELECT combined with an active WR enables the drive's line receivers on DBUS 0-7, so that the information on the bus can be written into the drive's three control registers. An active DRIVE SELECT combined with an active RD enables the drive's line drivers on DBUS 0-7, so that the information in the drive's three status-like registers can be returned to the controller. The following six registers are involved:

The COMMAND REGISTER receives and stores commands from the controller.

The TARGET ADDRESS REGISTER—UPPER BYTE receives and stores the two or three most significant bits of the desired cylinder address.

The TARGET ADDRESS REGISTER—LOWER BYTE receives and stores the eight least significant bits of the desired cylinder address.

The STATUS REGISTER holds current drive status information.

The CURRENT ADDRESS REGISTER—UPPER BYTE holds the two or three most significant bits of the current cylinder address.

The CURRENT ADDRESS REGISTER—LOWER BYTE holds the eight least significant bits of the current cylinder address.

The registers are accessed by activating the ap-

propriate combinations of address lines A1 and A0, and the WR or RD signal as shown in Table 4-15. Note that the command and target address registers are write-only, while the status and current address registers are read-only.

4.6.4 Commands. Table 4-16 lists the command codes for the valid commands. The commands are discussed individually following Table 4-16.

Table 4-15. Register Selection

RD	WR	A1	A0	Selected Register
0	1	0	0	Command Register
0	1	0	1	Target Address — Upper Byte
0	1	1	0	Target Address — Lower Byte
1	0	0	0	Status Register
1	0	0	1	Current Address — Upper Byte
1	0	1	0	Current Address — Lower Byte

Note: 1 = Active, 0 = Inactive.

Table 4-16. Command Code Summary

	DBUS							
Command Name	7	6	5	4	3	2	1	0
Sequence Up	0	0	0	0	0	0	0	1
Sequence Down	0	0	0	0	0	0	1	0
Restore	0	0	0	0	0	0	1	1
Seek	0	0	0	0	0	1	0	0
Fault Reset	0	0	0	0	0	1	0	1
Read Drive ID	0	0	0	1	0	0	0	0
Read Bytes/Sector	0	0	0	1	0	0	0	1

1. *Sequence Up* The Sequence Up command causes the disc drive spindle motor to power up. The rotational speed of the disc is monitored, and after the drive is up to speed, the heads are positioned to cylinder zero. The drive presents BUSY status (BUSY bit set in the status register) while Sequence Up is in process. At the successful completion of Sequence Up, BUSY is cleared and CYLINDER ZERO, SEEK COMPLETE, and READY are set. If Sequence Up is unsuccessful, WRITE PROTECT and DRIVE FAULT are set.

2. *Sequence Down* The Sequence Down command causes the heads to be positioned to the landing zone, and the spindle motor to be stopped. WRITE PROTECT status is set at the completion of Sequence Down.

3. *Restore* The Restore command causes the head carriage to be positioned to cylinder zero. The drive Restores automatically on Sequence Up, or when a SEEK FAULT is detected. If the Restore command is unsuccessful, the heads will be positioned to the landing zone, and DRIVE FAULT status will be set. If the drive is not sequenced up, the Restore command will function as a Sequence Up Command.

4. *Seek* The Seek command causes the drive to seek to a specified cylinder. Prior to issuing the Seek command, the controller must place the desired cylinder address in the target address registers. Upon receipt of the Seek command, the drive clears READY status and sets BUSY, while moving the head carriage to the correct cylinder. When this has been done, the drive sets READY and also sets SEEK COMPLETE status. If the Seek command is unsuccessful, the drive Restores to cylinder zero, and sets CYLINDER ZERO and SEEK FAULT status.

5. *Fault Reset* The Fault Reset command clears the two fault conditions — SEEK FAULT and DRIVE FAULT.

6. *Read Drive ID* The Read Drive ID command loads the drive ID into the lower byte of the current address register, and clears READY status. The controller may then retrieve the information by reading the lower byte of the current address register. The values of the ID code for various PRIAM disc drives are given in Table 4-17.

   After the DRIVE ID Information has been read by the controller, a Sequence Up or Restore command must be issued to bring the drive back to the READY state. In general, the current address registers contain the current cylinder address if the drive is READY, and the last requested parameter information if the drive is not READY.

7. *Read Bytes per Sector* The Read Bytes per Sector command loads the number of bytes per sector into the current address registers, and clears READY status.

   As with the Read Drive ID command, a Sequence Up or Restore command must be issued to bring the drive back to the READY state.

Table 4-17. Drive ID Assignments

ID Code (Hex)	Drive Designation	
00	Not Valid	
01	DISKOS 3350-01 or 3350-10	(20, 160 bytes/track)
02	DISKOS 3350-01	(19,960 bytes/track)
03	DISKOS 3450	(12,960 bytes/track)
04	DISKOS 3450	(13,440 bytes/track)
05	DISKOS 7050	(13,440 bytes/track)
06	DISKOS 6650	
07	DISKOS 15450	
08-OF	Reserved	
10	Reserved	
11	DISKOS 1070-1	
12	CD8005	
13	CD8010	
14	Reserved	
15	DISKOS 1070-2	
16	DISKOS 1070-3	
17-FF	Reserved	

4.6.5 Register Bit Definitions. Register Bit Definitions are presented in Table 4-18 and Table 4-19.

Table 4-18. Status Register Bit Definitions

Bit	Name	Description
0	READY	The drive is up to speed, the servo system is locked onto a servo track, and the drive is able to read, write or seek.
1	SEEK COMPLETE	A seek operation has been completed. This bit is not valid when the BUSY bit is set.
2	SEEK FAULT	A fault was detected during a seek operation. This bit is not valid when the BUSY bit is set.
3	CYLINDER ZERO	The head carriage is at cylinder zero. This bit is not valid when the BUSY bit is set.
4	BUSY	The drive is in the process of executing a command.

Table 4-18. Status Register Bit Definitions (cont'd.)

Bit	Name	Description
5	DRIVE FAULT	A fault was detected during a write operation, or a drive unsafe condition was detected.
6	WRITE PROTECT	The selected head is write protected. WRITE PROTECT is set by switches on the main PCB. The entire drive is write protected when it is not sequenced up.
7	COMMAND REJECT	The controller attempted to write to a register when the drive was not READY, or an invalid command was received by the drive. This bit is not valid when the BUSY bit is set.

Table 4-19. Target and Current Cylinder Address Register Bit Definitions

	Bit Number							
Byte	7	6	5	4	3	2	1	0
Upper Byte	0	0	0	0	0	C_{10}	C_9	C_8
Lower Byte	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

As indicated in Table 4-19, up to eleven bits of information can be stored in the address registers. This information may be the target cylinder address, the current cylinder address, or the requested parametric information, such as bytes per sector or drive ID. C_{10} is the most significant bit, and C_0 is the least significant bit.

4.6.6 Interface Timing. This section discusses the timing requirements for the various operations performed on the drive interface.

1. *Register Load Timing* Register load timing is shown in Figure 4-15. The AC characteristics are listed in Table 4-20.

Table 4-20. Register Load AC Characteristics

Symbol	Parameter	Min	Max	Units
t_{AW}	Address stable before WR	60		ns
t_{WA}	Address hold time for WR	30		ns
t_{WW}	WR pulse width	100		ns
t_{DW}	Data set up time for WR	60		ns
t_{WD}	Data hold time for WR	30		ns
t_{RV}	Recovery time between WR	200		ns

2. *Register Read Timing* Register read timing is shown in Figure 4-16. The AC characteristics are listed in Table 4-21.

Table 4-21. Register Read AC Characteristics

Symbol	Parameter	Min	Max	Units
t_{AR}	Address stable before RD	60		ns
t_{RA}	Address hold time for RD	30		ns
t_{RR}	RD pulse width	100		ns
t_{RD}	Data delay from RD		60	ns
t_{DF}	RD to data floating	10	40	ns

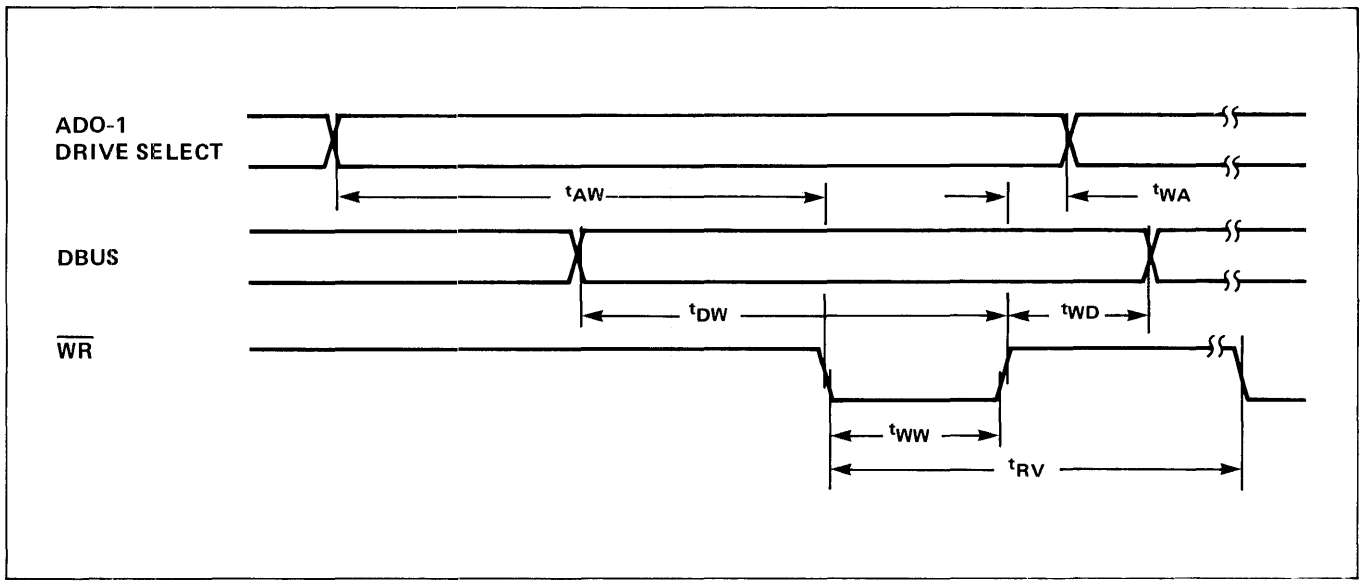


Figure 4-15. Register Load Timing

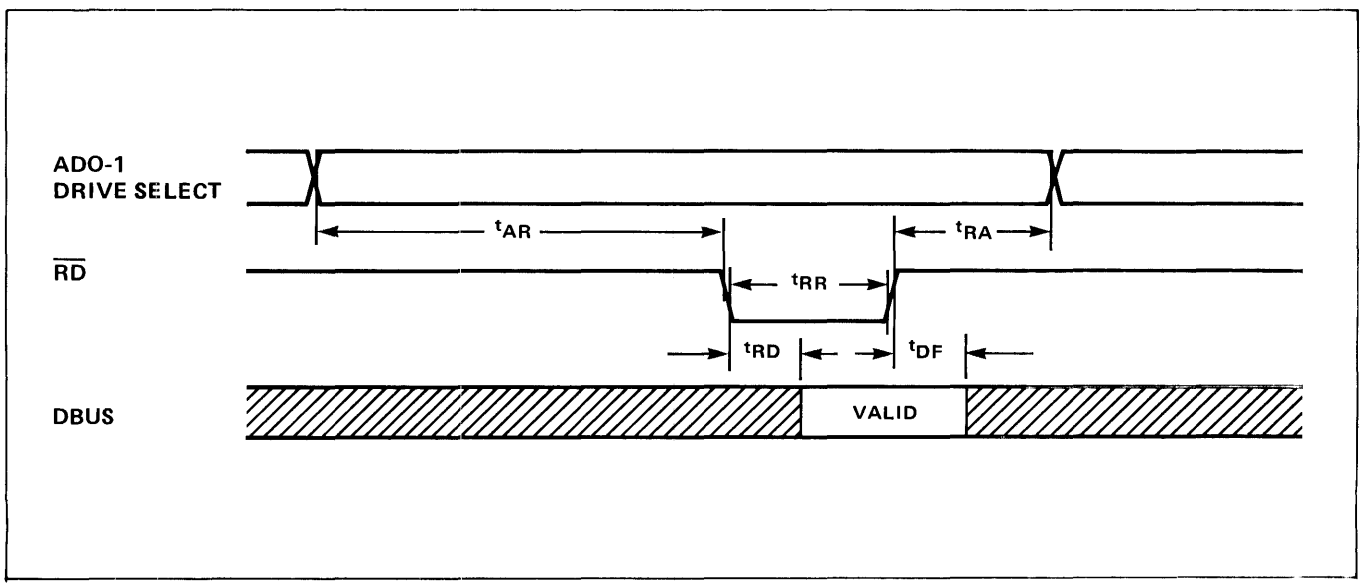


Figure 4-16. Register Read Timing

3. *Reset Timing* Reset timing is shown in Figure 4-17. The AC characteristics are listed in Table 4-22.

Table 4-22. Reset AC Characteristics

Symbol	Parameter	Min	Max	Units
t_{RST}	RESET pulse width	500		ns
t_{SR}	DRIVE SELECT TO RESET	0		ns

4. *INDEX AND SECTOR MARK timing* INDEX and SECTOR MARK timing is shown in Figure 4-18. The AC characteristics are listed in Table 4-23.

Table 4-23. INDEX and SECTOR MARK AC Characteristics

Symbol	Parameter	Timing	Units
t_{IW}	INDEX pulse width	1.92 ±.19	μs
t_{IR}	INDEX period	19.35 ±.5	ms
t_{SW}	SECTOR MARK pulse width	960 ± 140	ns
t_{IS}	INDEX to first SECTOR	34.5 ±5.2	μs
t_{BYTE}	Byte period	960 ±144	ns

t_{SR} = Sector width = (Sector size in bytes)x(t_{BYTE} in nsec) ± 10%

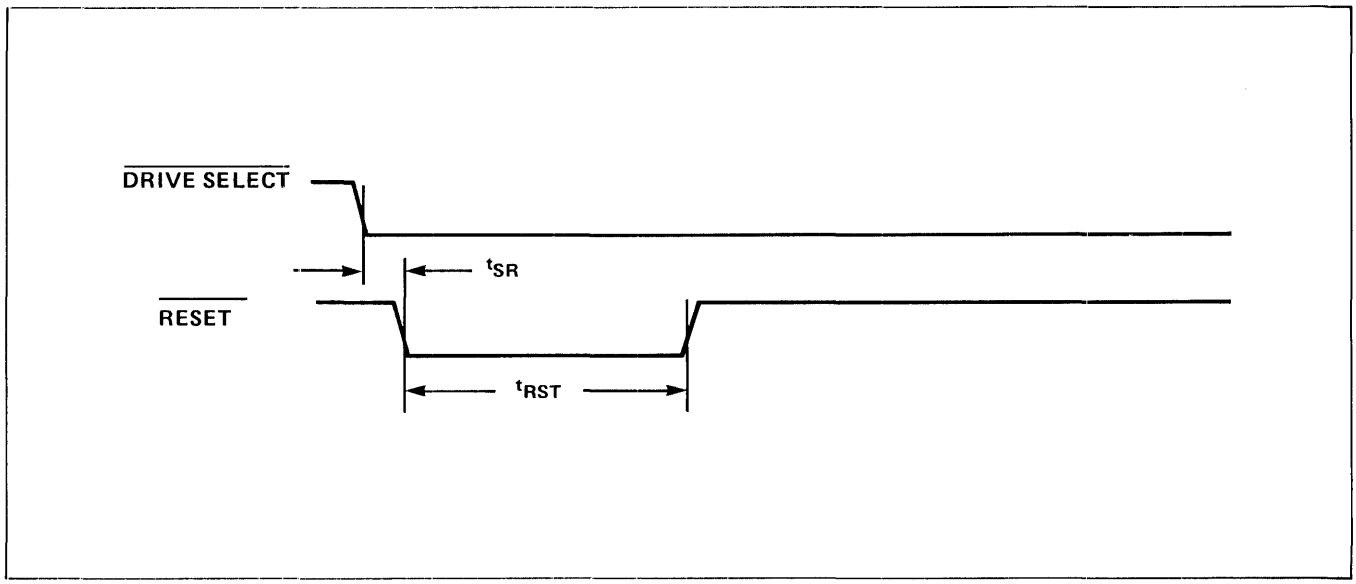


Figure 4-17. Reset Timing

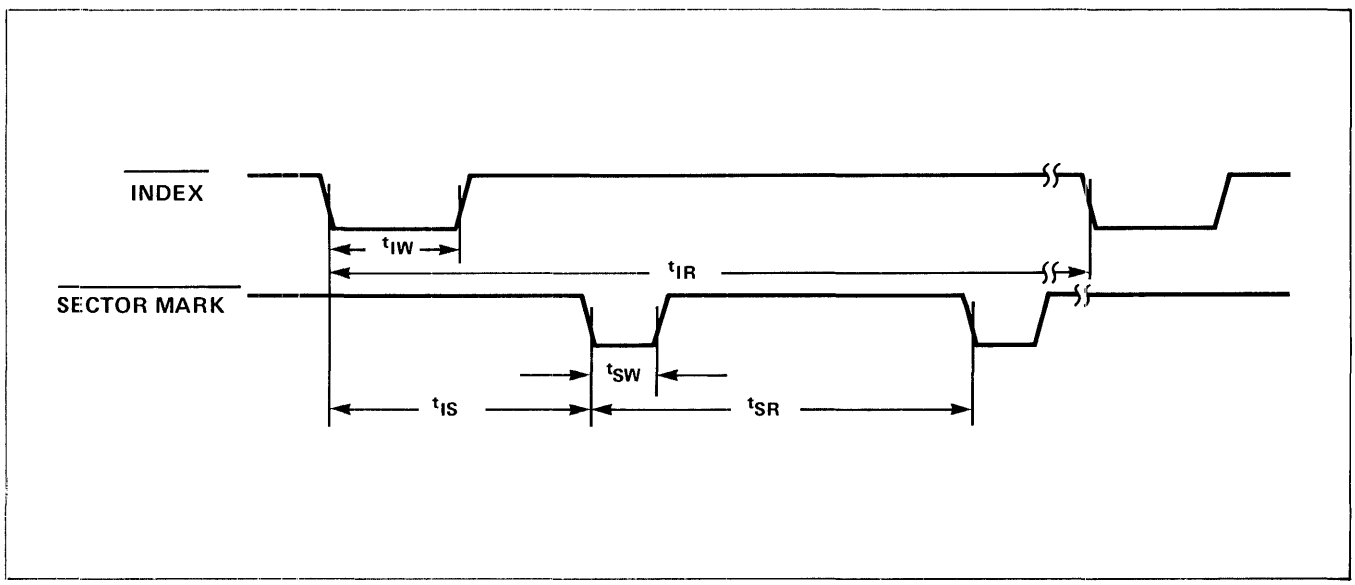


Figure 4-18. INDEX and SECTOR MARK Timing

5. *WRITE DATA and WRITE CLOCK timing* WRITE DATA and WRITE CLOCK timing is shown in Figure 4-19. The AC characteristics are listed in Table 4-24.

6. *READ DATA and READ CLOCK Timing* READ DATA and READ CLOCK timing is shown in Figure 4-20. The AC characteristics are listed in Table 4-25.

Table 4-24. WRITE DATA and WRITE CLOCK AC Characteristics

Symbol	Parameter	Timing	Units
t_{CLK}	WRITE CLOCK period	120 ± 18	ns
t_{WH}	WRITE CLOCK high pulse width	60 ± 9	ns
t_{WL}	WRITE CLOCK low pulse width	60 ± 9	ns
t_{BIT}	WRITE DATA bit period	120 ± 18	ns
t_{DC}	WRITE DATA setup time	20*	ns min
t_{CD}	WRITE DATA hold time	20*	ns min
t_{BYTE}	Byte period	960 ± 144	ns
	*60 ns typical		

Table 4-25. READ DATA and READ CLOCK AC Characteristics

Symbol	Parameter	Timing	Units
t_{CLK}	READ CLOCK period	120 ± 18	ns
t_{WH}	READ CLOCK high pulse width	60 ± 9	ns
t_{WL}	READ CLOCK low pulse width	60 ± 9	ns
t_{BIT}	READ DATA bit period	120 ± 18	ns
t_{DC}	READ DATA setup time	40*	ns min
t_{CD}	READ DATA hold time	40*	ns min
t_{BYTE}	Byte period	960 ± 144	ns
	*60 ns typical		

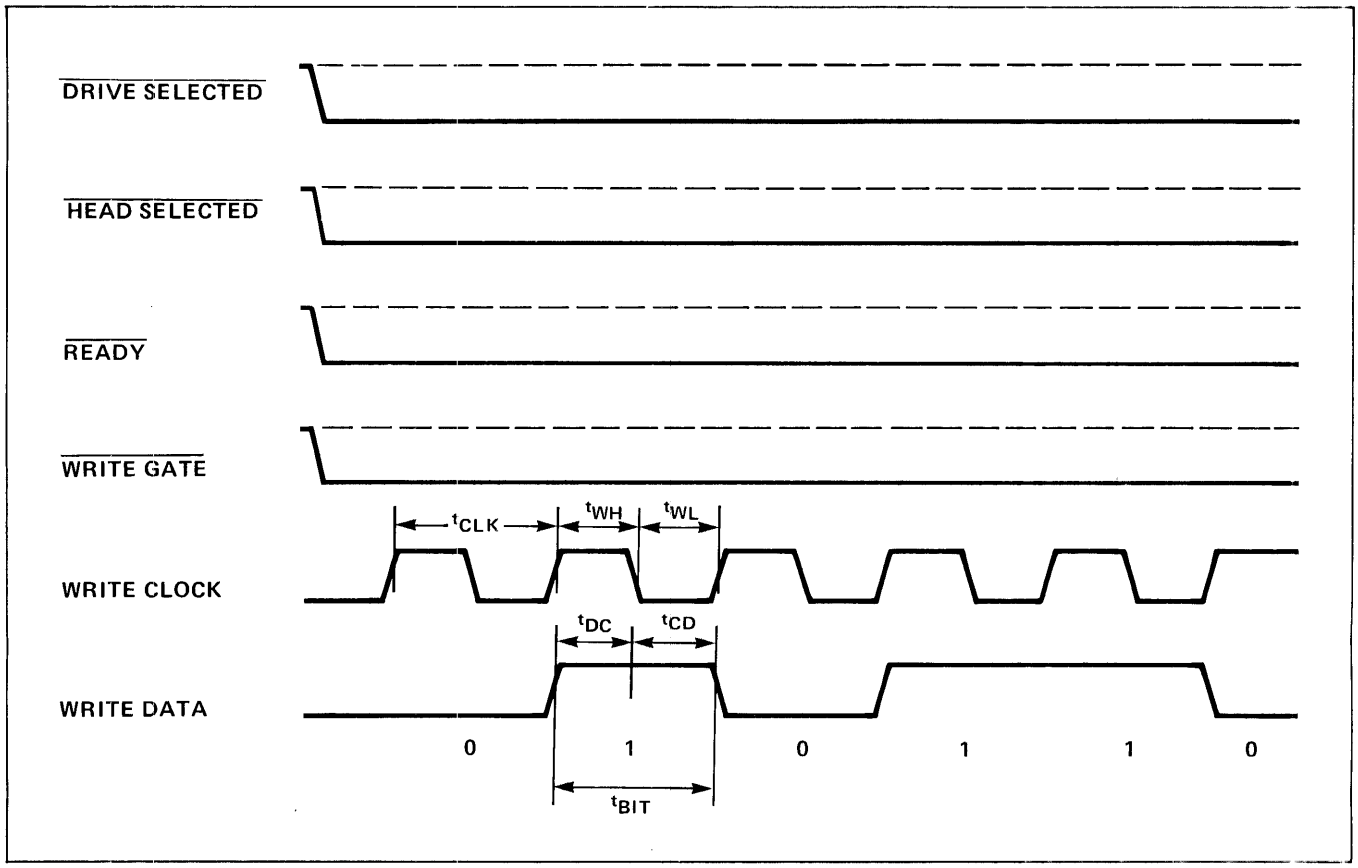


Figure 4-19. WRITE DATA and WRITE CLOCK Timing

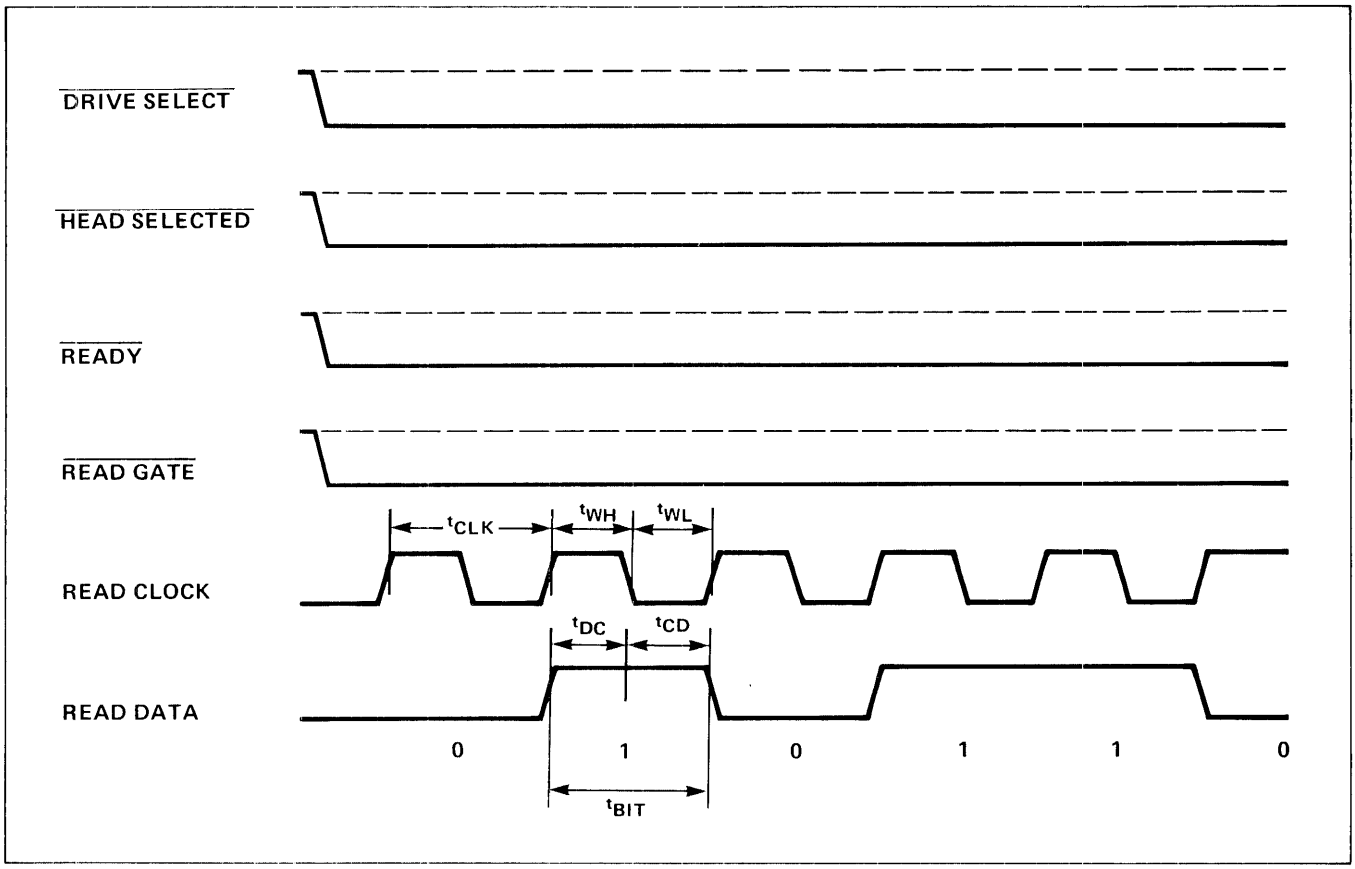


Figure 4-20. READ DATA and READ CLOCK Timing

7. *Record Writing* Figure 4-21 shows the timing requirement for writing full sectors (ID and data fields) and also writing data field only. The AC characteristics are listed in Table 4-26.

8. *Record Reading* Figure 4-22 shows the timing requirements for reading full sectors (ID and data fields) and also for reading data fields only. The AC characteristics are listed in Table 4-27.

The combined operations are shown in Figure 4-23.

Table 4-26. Record Writing Control AC Characteristics

Symbol	Parameter	Timing	Units
t_{SH}	DRIVE SELECTED to HEAD SELECTED	20	μs min
t_{SR}	DRIVE SELECTED to READY	100	ns min
t_{SG}	SECTOR MARK to WRITE GATE	0 ± 1	μs
t_{IDG}	ID gap timing	24	bytes min
t_{IDF}	ID fill	2	bytes min
t_{DG}	Data gap (no write-to-read transitions)	12	bytes min
t_{DF}	Data fill	2	bytes min
t_{HW}	HEAD SELECTED TO WRITE GATE	100	ns
t_{BYTE}	Byte period	960 ± 144	ns

Table 4-27. Record Reading Control AC Characteristics

Symbol	Parameter	Timing	Units
t_{SH}	DRIVE SELECTED to HEAD SELECTED	20	μs
t_{SR}	DRIVE SELECTED to READY	100	ns min
t_{RDLW}	READ GATE delay for gaps allowing write-to read transitions	13	μs min
t_{RDLR}	READ GATE delay for gaps limited to read-to-read or read-to-write transitions	1.9	μs min
t_{SYN}	Read VFO synchronization (data not valid during this period)	9	μs min
t_{HR}	HEAD SELECTED to READ GATE	25	μs min
t_{BYTE}	Byte period	960 ± 144	ns

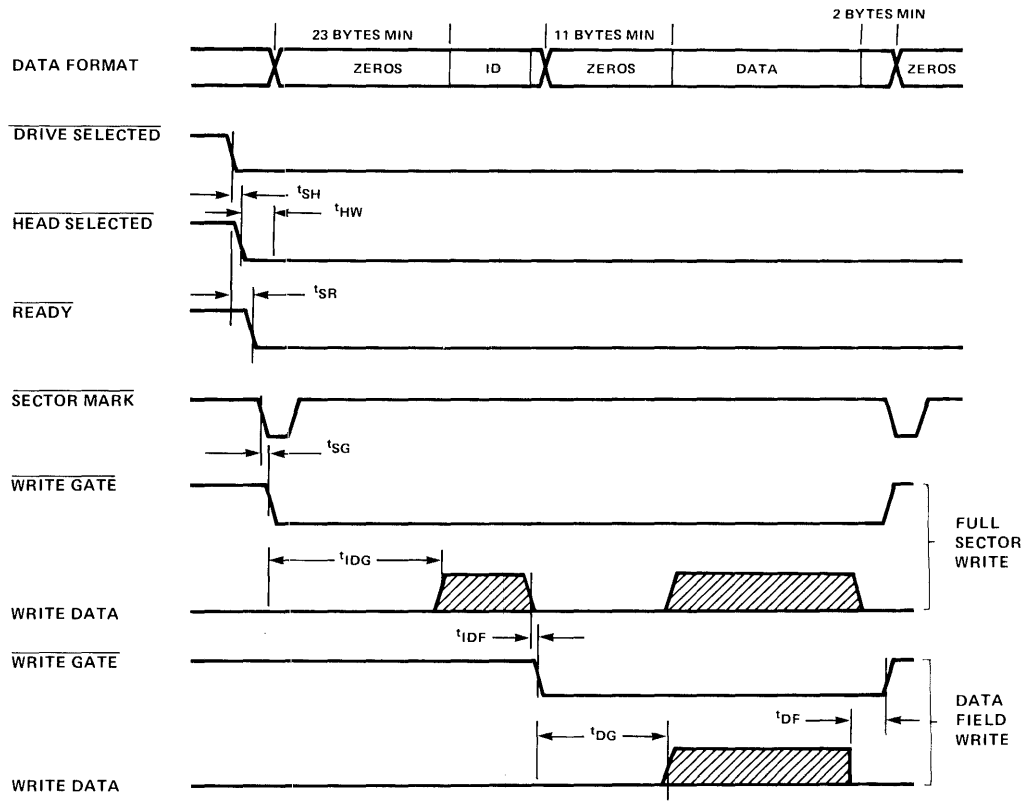


Figure 4-21. Record Writing Timing

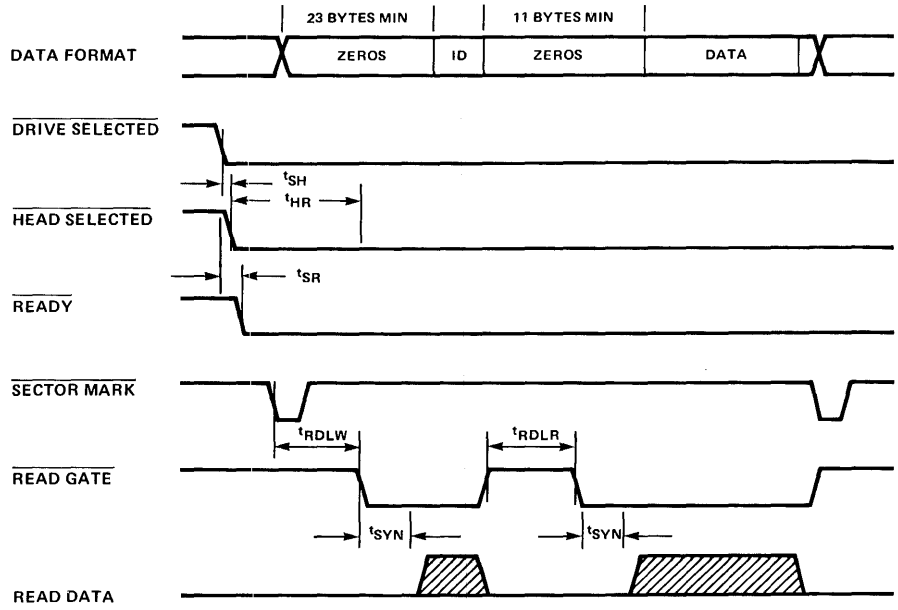


Figure 4-22. Record Reading Timing

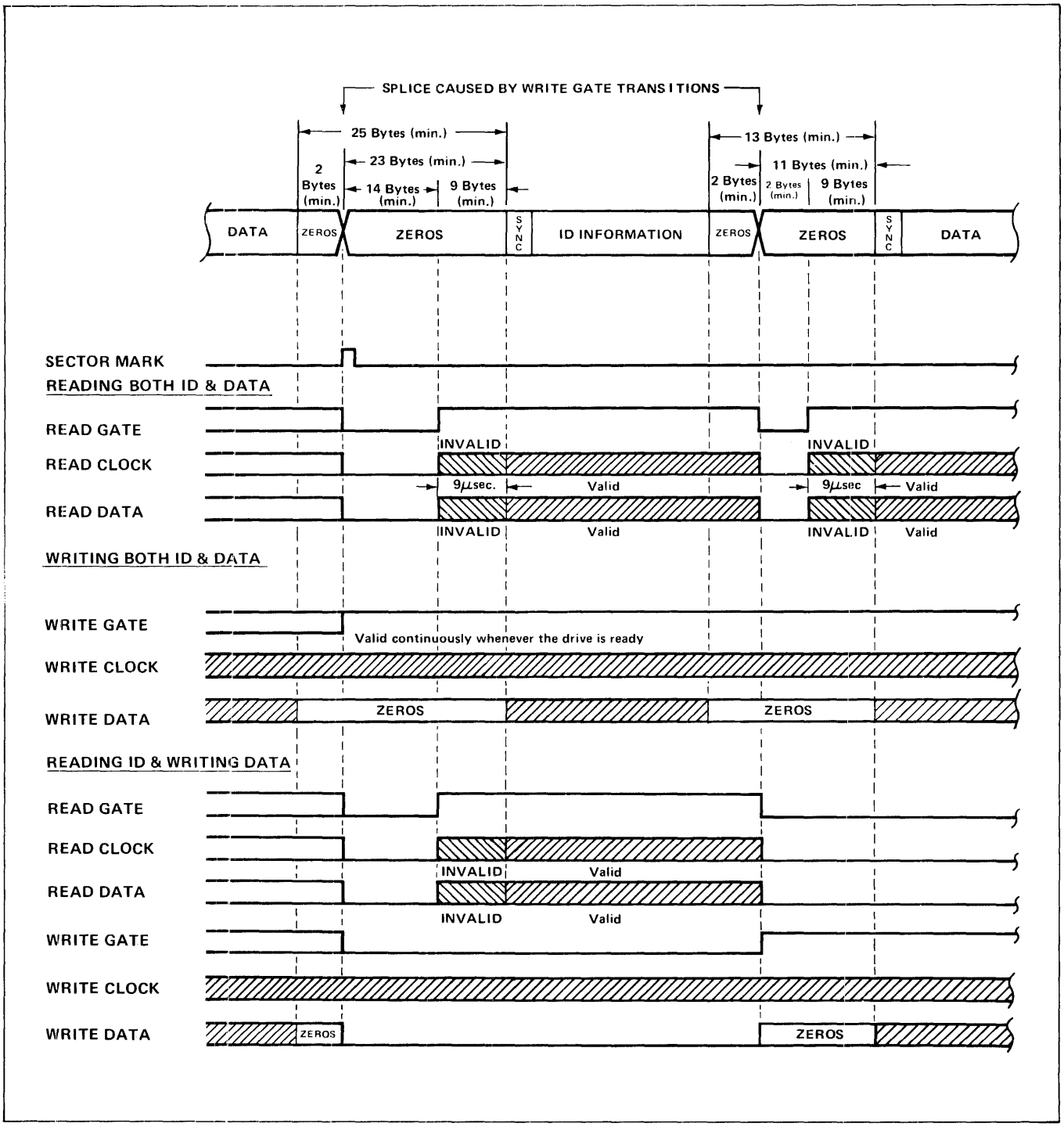


Figure 4-23. Read and Write Transitions During Gaps

4.7 Track Format Considerations. Some hardware constraints must be observed when designing a track format. The following sections discuss these design characteristics and other important related details to be considered in the design of the track format.

4.7.1 Write/Read Timing Constraints (See Figure 4-23).

1. *Head Selection Time* Between the selection of a head and the assertion of READ GATE, there should be a delay of approximately 25 microseconds. Since head selection normally occurs at the index mark, the defect field supplies a sufficient delay for circuit stabilization prior to reading the first ID field.

2. *Write-To-Read Recovery Time* Approximately 13 microseconds are required for read amplifier stabilization after WRITE GATE is turned off. READ GATE should be off during this time. This time is included in the 14 bytes after SECTOR MARK as shown in Figure 4-23.

3. *Read Data VFO Synchronization* A 9 byte delay occuring after the READ GATE is asserted is required to allow the Variable Frequency Oscillator (VFO) to synchronize to the data being read from the disc. This 9 byte area precedes the sync bytes of the ID and the data fields.

4. *Sync Pattern* The sync pattern, indicating the beginning of the address or data area, is 1 byte in length.

5. *Write Driver Turn On* The write driver turn on time is about 960 nanoseconds (one byte time). This time is accounted for in the 2 bytes after the write splice.

4.7.2 Control Timing Constraints (See Figure 4-23).

1. *Read Data Field* READ GATE is the control line associated with a read operation.

   The leading edge of READ GATE allows the VFO to synchronize on an all-zeros pattern. READ GATE (delayed) also enables the output of the data separator onto the I/O lines. There may be invalid data transitions on these lines during the synchronization period. READ GATE must be dropped and raised again after going through a write splice area. READ GATE may be enabled a minimum of 13 microseconds after the leading edge of INDEX or SECTOR. The sync pattern search may begin 72 read clock periods (9 byte times) after the leading edge of READ GATE.

   Read Data and Read Clock may not be valid until 10 microseconds after the leading edge of Read Gate, due to the VFO synchronizing time.

2. *Write Data Field* WRITE GATE is the control line associated with a write operation.

   The sector address must always be read and verified, prior to writing the data field, except while formatting.

   Writing the data field must always be preceded by writing the VFO sync field and data sync pattern.

   Writing the data field must always be followed by writing the data checkword and at least an eight-bit gap of zeros at the end of the checkword.

   During formatting, WRITE GATE is raised upon detecting INDEX or SECTOR. During a record update, WRITE GATE is raised two byte times after the last bit of the ID field.

4.7.3 Suggested Data Format (See Figure 4-24).

All PRIAM Disc Drives are programmable hard sectored drives. Index and sector marks are derived from the servo clocks generated from the servo data. The number of sectors per track is programmed by the user by setting the appropriate sector DIP switches located on the drive's Main PCB. Once these switches are set and the drive is formatted, the sector count is fixed. If the sector count is changed in the sector switches, then the drive has to be reformatted.

To insure reliable recording and retrieval of data on PRIAM drives, the following track format is recommended:

PRIAM RECOMMENDED TRACK FORMAT

Each track begins with an INDEX Pulse which is generated by information from the servo tracks. Also, the servo tracks provide clocking information for generation of sector pulses. A sector pulse occurs at the beginning of each data record area. Each data record consists of several gaps, an ID (Identification) field and data field (See Figure 4-24).

1. *Pre-Record Gap (Gap 1)* The Pre-Record Gap, or Gap 1, appears at the beginning of every rec-

ord. It consists of 23 bytes of zeros. The length of Gap 1 never varies. The first Gap 1 (after INDEX), is followed by the Skip Defect Record. All other Gap 1's (after SECTOR MARKS), are followed by ID records.

2. *Skip Defect Record* The Skip Defect Record (SDR) is written within the 36 bytes following the leading edge of Index on every track of every head on all PRIAM disc drives. The purpose of the SDR is to allow (during a format operation) automatic alternate sector allocation. This can be accomplished through system software or by the action of an intelligent controller such as in all models of the PRIAM SMART drive controllers.

   The Skip Defect Record consists of 13 bytes: a Data Sync using the hexadecimal pattern, FB, the physical address of the first defect using two bytes, the physical address of the second defect using two bytes, the physical address of the third defect using two bytes, a checksum across the previous six bytes using two bytes, and fill characters of zeros using four bytes.

3. *ID Record* This Identification Field uses 9 or 11 bytes as follows:

   a. An ID sync byte using a unique hexadecimal pattern such as F9.

   b. Head address and high order cylinder address of one byte.

   c. The low order cylinder address of one byte.

   d. The sector number of one byte.

   e. A sector length and flag byte (ID control byte).

   f. Two CRC (Cyclic Redundancy Check) bytes or

   g. Four ECC (Error Correction Code) bytes.

   h. Two bytes of zeros for filling.

   The cylinder and head address, along with the sector number, can be used to verify that the drive has addressed the correct track and sector. This insures that no seek errors have occurred.

4. *ID Gap (Gap 2)* The ID Gap, or Gap 2, separates each successive Identification Record from its Data Record. It contains 11 bytes of zeros. The Write Splice is located at the beginning of this Gap.

5. *Data Record* Following Gap 2, the Data Record consists of:

   a. First byte is the data sync byte (hexadecimal FD).

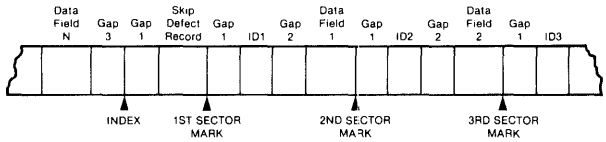
   b. Between 64 and 2031 bytes of data as selected by the sector switches on the drive main PCB.

   c. The last bytes consist of 2 bytes of CRC (Cyclic Redundancy Check) and 2 bytes of zeros for filling, or 4 bytes of ECC (Error Correction Code) and 2 bytes of zeros for filling.

6. *Pre-Index Gap (Gap 3)* The Pre-Index Gap, or Gap 3, is used only once per track. It starts at the end of the last data field and ends at the leading edge of Index pulse. Its size depends on the data record size and contains all zeros.

Table 4-28. Sector Format Examples Using ECC

Sector Logical Size (bytes)	Sector Physical Size (bytes)	Sectors Per Track	Gap 1 (bytes)	Gap 2 (bytes)	Gap 3 (bytes)	Data Per Track (bytes)	Percent Utilization (bytes)
128	181	111	23	11	33	14,208	70.6%
256	309	65	23	11	39	16,640	82.7%
512	574	35	23	11	34	17,920	89.0%
1024	1118	18	23	11	0	18,432	91.6%



Index:	Derived from servo track	
Gap 1:	Zeros	23 Bytes
Skip Defect Record:	Data Sync, FB Hex	1 Byte
	1st defect address	2 Bytes
	2nd defect address	2 Bytes
	3rd defect address	2 Bytes
	Checksum	2 Bytes
	Fill characters (zeros)	2 Bytes
Sector Mark:	Derived from INDEX and servo clock	
Gap 1:	Zeros	23 Bytes
ID Field:	ID Sync	1 Byte
	Sector address	1 Byte
	Head and cylinder address MSB	1 Byte
	Cylinder address LSB	1 Byte
	ID Control	1 Byte
	CRC/ECC	2/4 Bytes
	Fill characters (zeros)	2 Bytes
Gap 2:	Zeros	11 Bytes
Data Field:	Data Sync	1 Byte
	Data Between 64 and	2031 Bytes
	CRC/ECC	2/4 Bytes
	Fill characters (zeros)	2 Bytes
Gap 3:	Zeros (Size depends on data field size)	

Figure 4-24. Format Definition

4.8 System Grounding. PRIAM recommends an AC grounding scheme as shown in Figure 4-25.

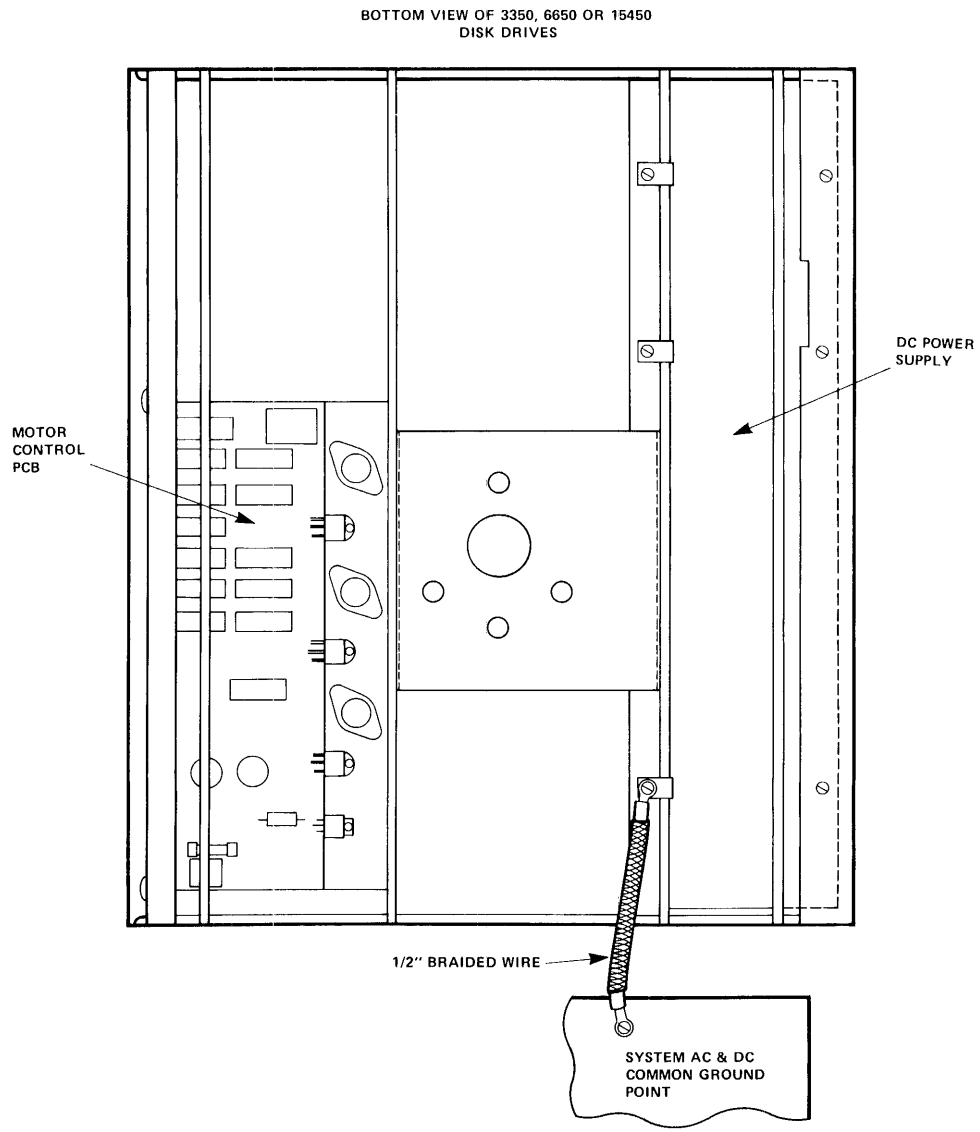


Figure 4-25. Recommended System Grounding

5. SMD Interface Operation

This section provides information for setting up all 14-inch drives having an embedded SMD (Storage Module Device) Interface. This includes power selection, jumper and switch settings, interface signal definitions and other information to insure proper system operation.

There are two SMD drive characteristics that are not supported on PRIAM drives. These are address marks and dual porting. Also, PRIAM uses pin numbers 59 and 60 ("A" cable spare pins) to allow a user optional 11 bit cylinder address. Ten bit cylinder addresses (1024 cylinders) are the SMD standard.

5.1 Mounting. All PRIAM 14-inch drives can be mounted in a standard 19-inch rack. PRIAM offers an optional slide mounting kit for use with all 14-inch drive models. See Figure 2-1 for mounting dimensions.

5.2 AC Power Set-Up. If a PRIAM optional power supply is present, check the AC voltage selection circuit board prior to applying power. This board is adjacent to the AC input plug, and is an integral part of the power supply. To change the AC voltage, remove the selection circuit board, and re-insert it so that the proper AC voltage designation (100, 120, 220, or 240) is visible. Also check the fuse value. A five ampere fuse is used with 100 or 120 VAC operation, while a 2.5 ampere fuse is used with 220 or 240 VAC operation. No modification is required for changing between 60 Hz and 50 Hz power.

5.3 Switch Settings. The drive address, write protect status and sector size are all switch selectable. The switches are located on the main PCB. Referring to Table 5-1, set the switches ac-

Table 5-1. DIP Switch Selection

		DRIVE MODEL NUMBER			
		6650-20/3350-20		15450-20	
DIP SWITCH LOCATION ON PCB		10N		2E	
SWITCH NUMBER/ FUNCTION	1	DEVICE SELECT 1		DEVICE SELECT 1	
	2	DEVICE SELECT 2		DEVICE SELECT 2	
	3	DEVICE SELECT 4		DEVICE SELECT 4	
	4	DEVICE SELECT 8		DEVICE SELECT 8	
	5				
	6				
	7				
	8	ON-WRITE PROTECT		ON-WRITE PROTECT	
DIP SWITCH LOCATION ON PCB		12K		10E	
SWITCH NUMBER/ FUNCTION		SECTORS	BYTES	SECTORS	BYTES
	1	1	16	1	16
	2	2	32	2	32
	3	4	64	4	64
	4	8	128	8	128
	5	16	256	16	256
	6	32	512	32	512
	7	64	1024	64	1024
	8	OFF-SECTOR/TRACK ON-BYTES/SECTOR		OFF-SECTOR/TRACK ON-BYTES/SECTOR	

cording to the desired operating conditions for the applicable Model Drive. See Figures 5-1 to 5-3 for the locations of the applicable DIP switches.

5.4 Jumper Settings. Jumpers are black conductive tabs that can be inserted on board pins to complete a particular circuit. Although most of these are used only at the factory to facilitate testing, some have user selectable functions. It is important that all jumpers be installed in their proper locations. See Figures 5-1 to 5-6.

Refer to Table 5-2 for jumper positions to enable the correct operating conditions for the applicable model drive and controller.

Table 5-2. Jumper Selection

Model	3350-20			6650-20		15450-20			
Jumper Number	200088	20148-01	200403-01	200148-02	200403-02	200263 200218	200213-01	200514-1	200515-1
W1	IN	BC	BC	AB	AB	USO	IN	IN	IN
W2	IN	IN	X	IN	X	OUT	IN	OUT	OUT
W3	IN	IN	X	IN	X	USO	X	OUT	IN
W4	IN	IN	IN	IN	IN	USO	X	IN	IN
W5	IN	BC	X	BC	X	X	BC	X	X
W6	IN	IN	X	IN	X	X	IN	X	X
W7	IN	IN	X	IN	X	X	X	X	X
W8	IN	IN	X	IN	X	X	X	X	X
W9	IN	IN	X	IN	X	X	NOTE 4	X	X
W10	IN	IN	X	IN	X	X	X	X	X
W11	X	AB	AB	BC	BC	X	X	X	X
W12	X	BC	BC	AB	AB	X	X	X	X
W13	X	AB	AB	BC	BC	X	X	X	X
W14	X	AB	AB	BC	BC	X	X	X	X
W15	X	AB	AB	BC	BC	X	X	X	X
W16	X	BC	BC	AB	NOTE 2	X	X	X	X
W17	X	IN	IN	OUT	OUT	X	X	X	X

1. X = Jumper does not exist.
2. Normally, AB. This jumper enables bit 10 for addressing cylinders greater than CYL 1023.
3. For -03 (MIS), jumper must be installed.
4. USO = User Selected Option (See Figure 5-3).

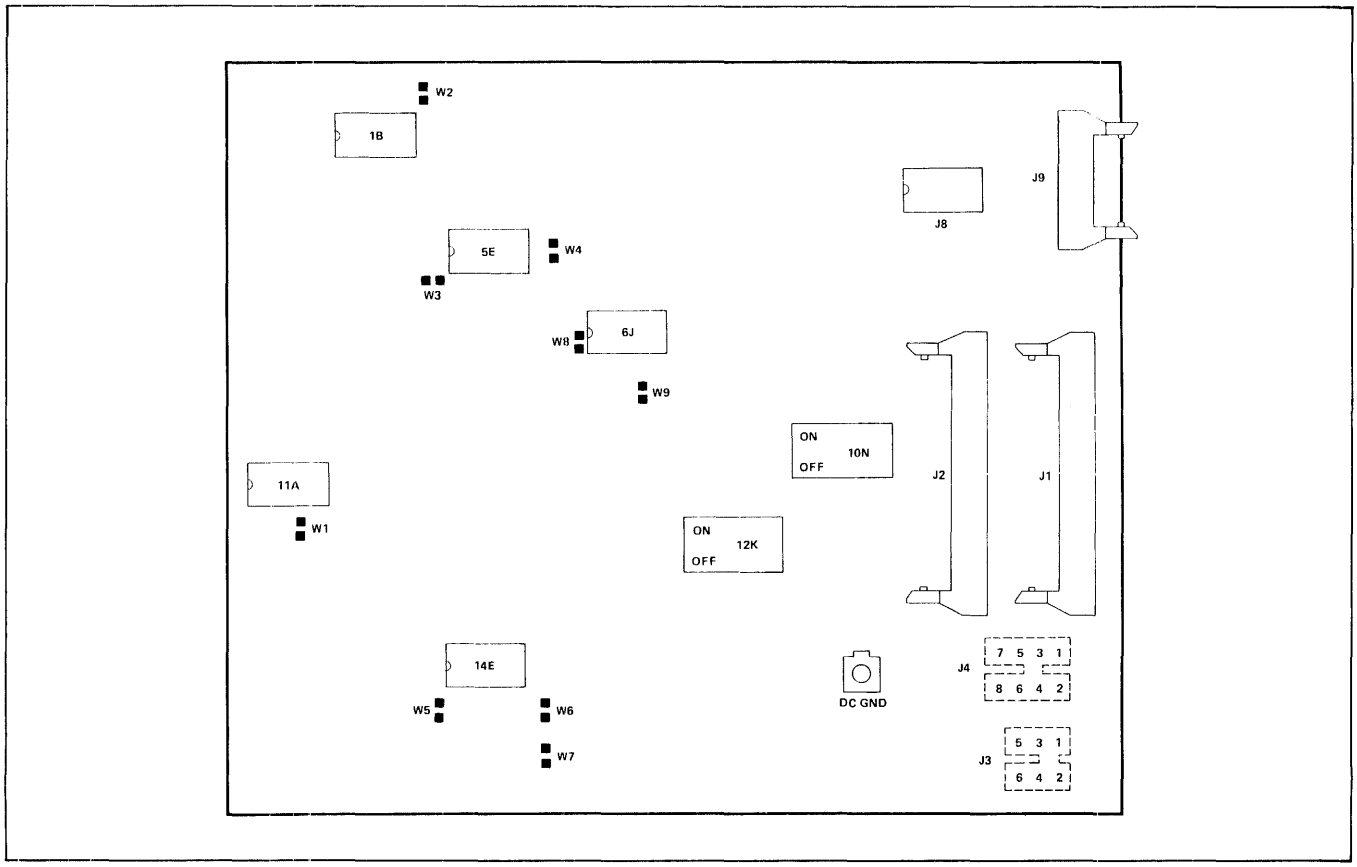
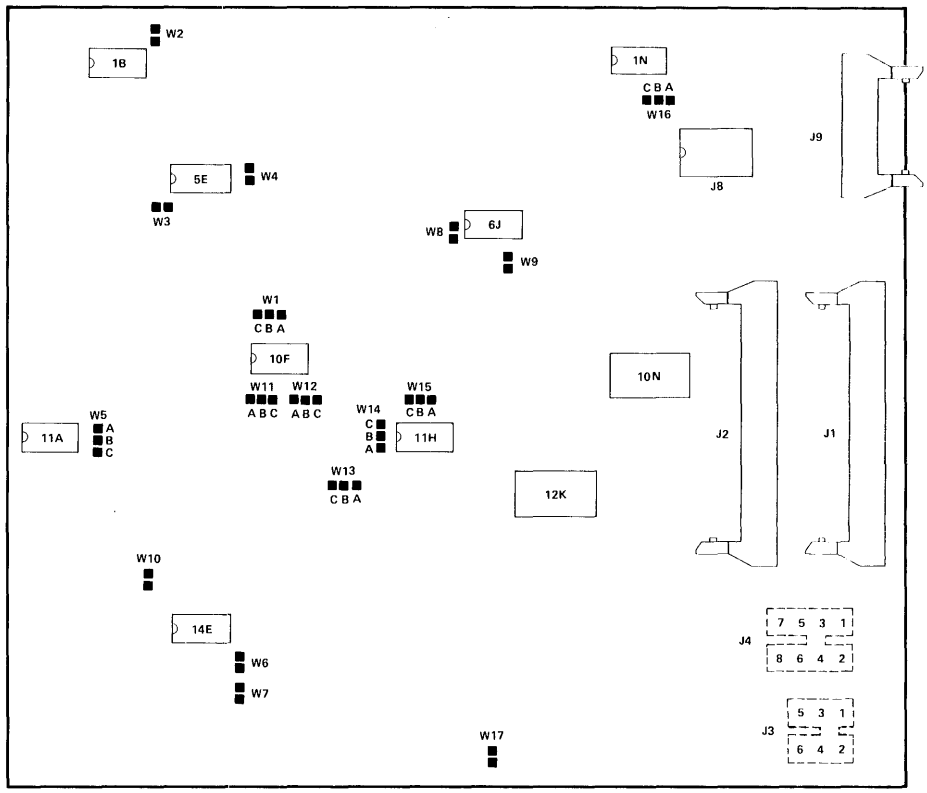
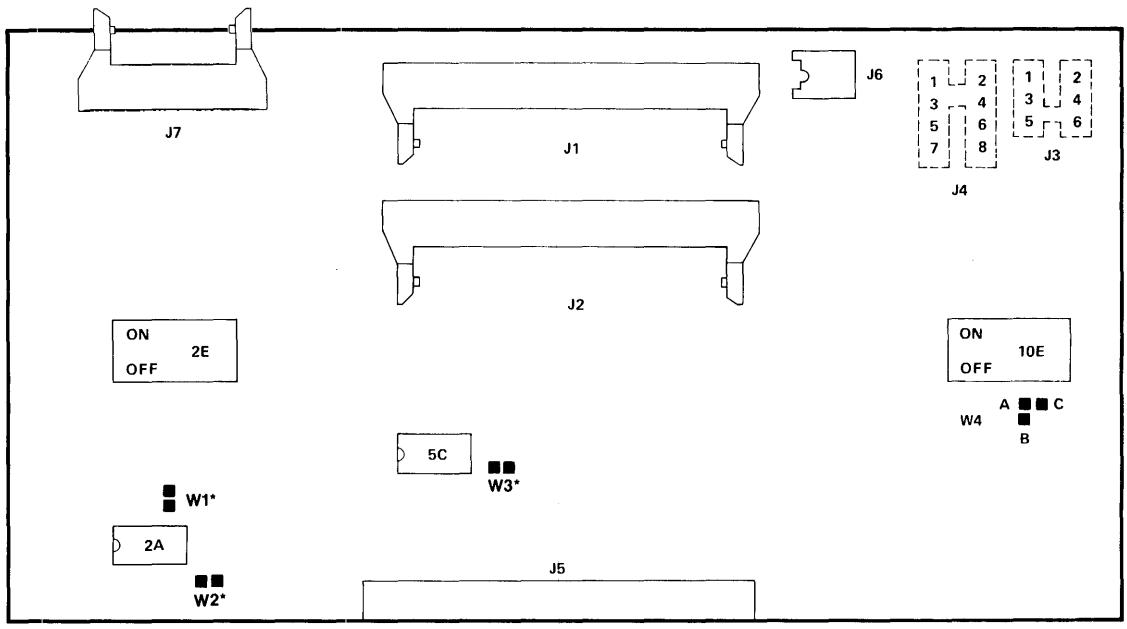


Figure 5-1. DIP Switch and Jumper Locations for PCB Assembly 200088



NOTE: PCB Assembly is used on Model 3350-20 and 6650-20 drives.

Figure 5-2. DIP Switch and Jumper Locations for PCB Assembly 200148-01/02



* Jumper is installed to enable function:
W1 = READ GATE GATED BY INDEX SECTOR.
W2 = NOT USED.
W3 = AUTO SEQUENCE UP.

Figure 5-3. DIP Switch and Jumper Locations for PCB Assembly 200218/200263

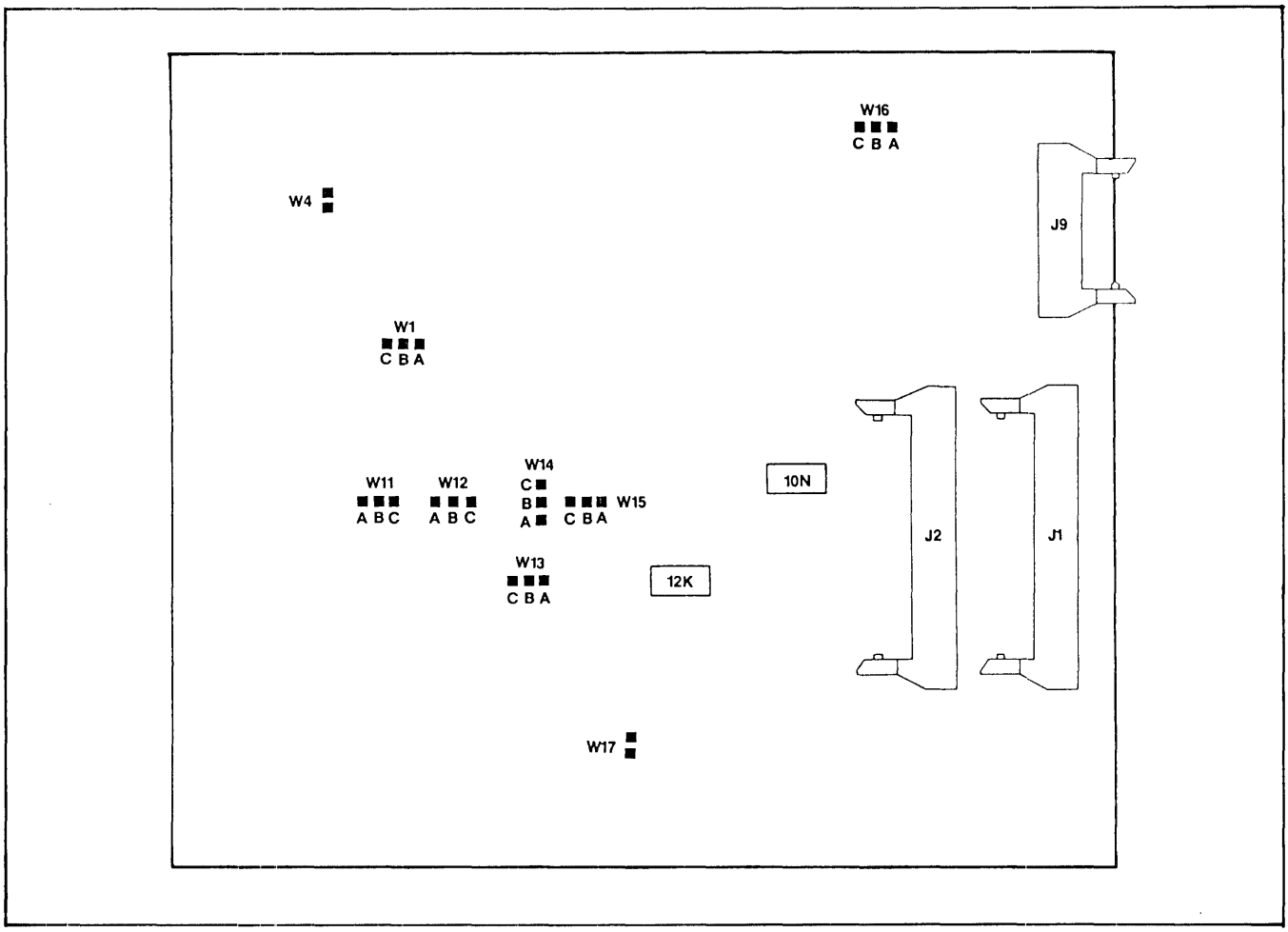


Figure 5-4. Jumper Locations for PCB Assembly 200403-01/02

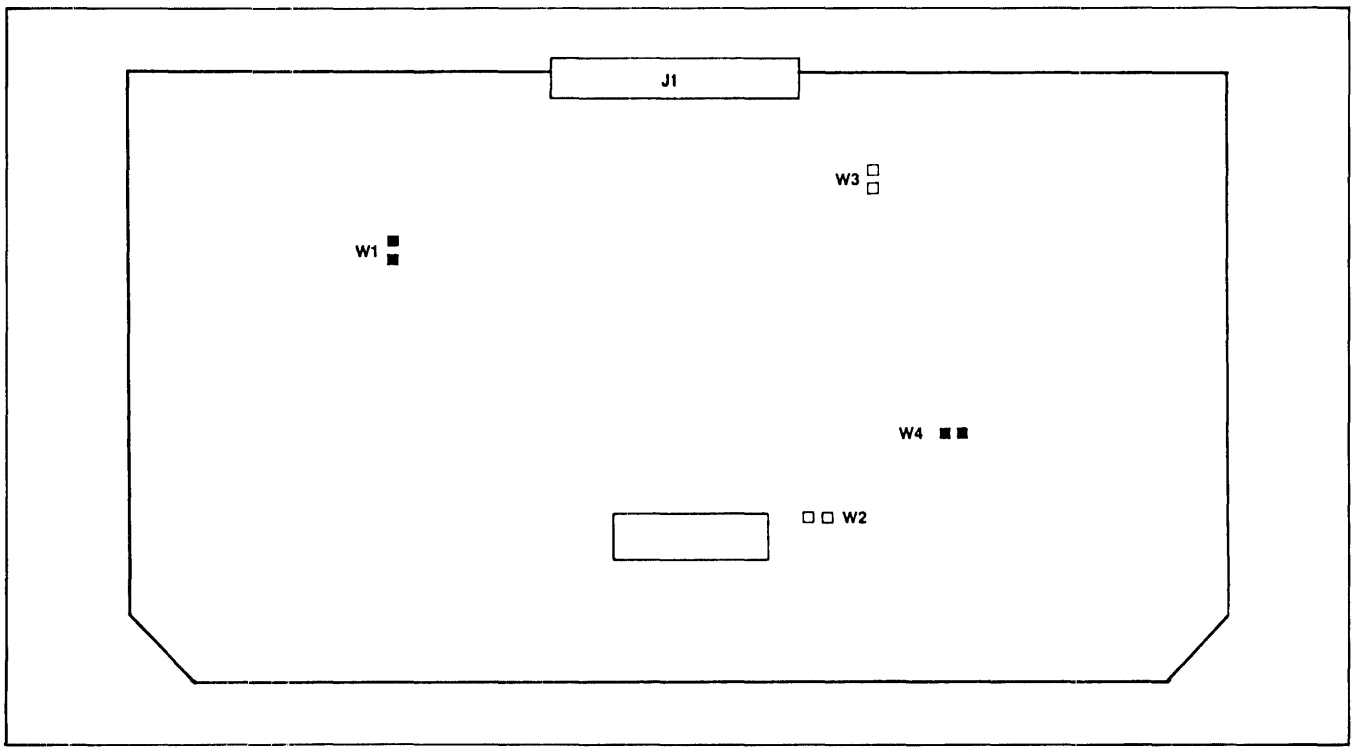


Figure 5-5. Jumper Locations for PCB Assembly 200514-1/200515-1

Table 5-3. Jumper Definitions for PCB Assembly 200218/200263

W1	In:	Read Gate gated by INDEX or SECTOR
W2	In:	Enable Address Mark (Not Used)
W3	In:	Auto Squence Up
W4	A-B:	Enables Cylinder Address Bit 10
	B-C:	Disables Bit 10

5.5 Cabling Requirements. Two cables are used for transmitting data and control signals between the disc drive and the controller. One (the "A" cable) contains parallel data, status, Unit Select and control signals. The other ("B" cable) contains serial data, clocking and sync signals.

A termination resistance is required at the transmitter and receiver end of each transmission line in the "A" cable. This resistance is provided on the drive by a terminator assembly which is shipped with each drive. A standard SMD termination resistance is required at the controller end of each "A" cable line, except for the Open Cable Detect Line.

A termination resistance (as shown in Section 5.6.2) is required at the receiver end of each transmission line in the "B" cable. At the disc drive end, this resistance is provided.

A separate connector for DC power is provided. However, if the optional power supply is installed, its output is connected to this DC power connector and AC power must be supplied to the optional power supply.

An 8 pin DIP socket for remote write protect control, fault clearing and drive status is also provided on the Main PCB.

5.5.1 Interface Cables and Connectors. The I/O interface cables and connectors are as follows:

1. "A" Cable (Shielded)

Description	Berg P/N	Brand-Rex P/N
Connector (60 pos.)	65043-007	
Contact, insert	75691-007	
Cable, miniature 30 twisted pair		T-8649

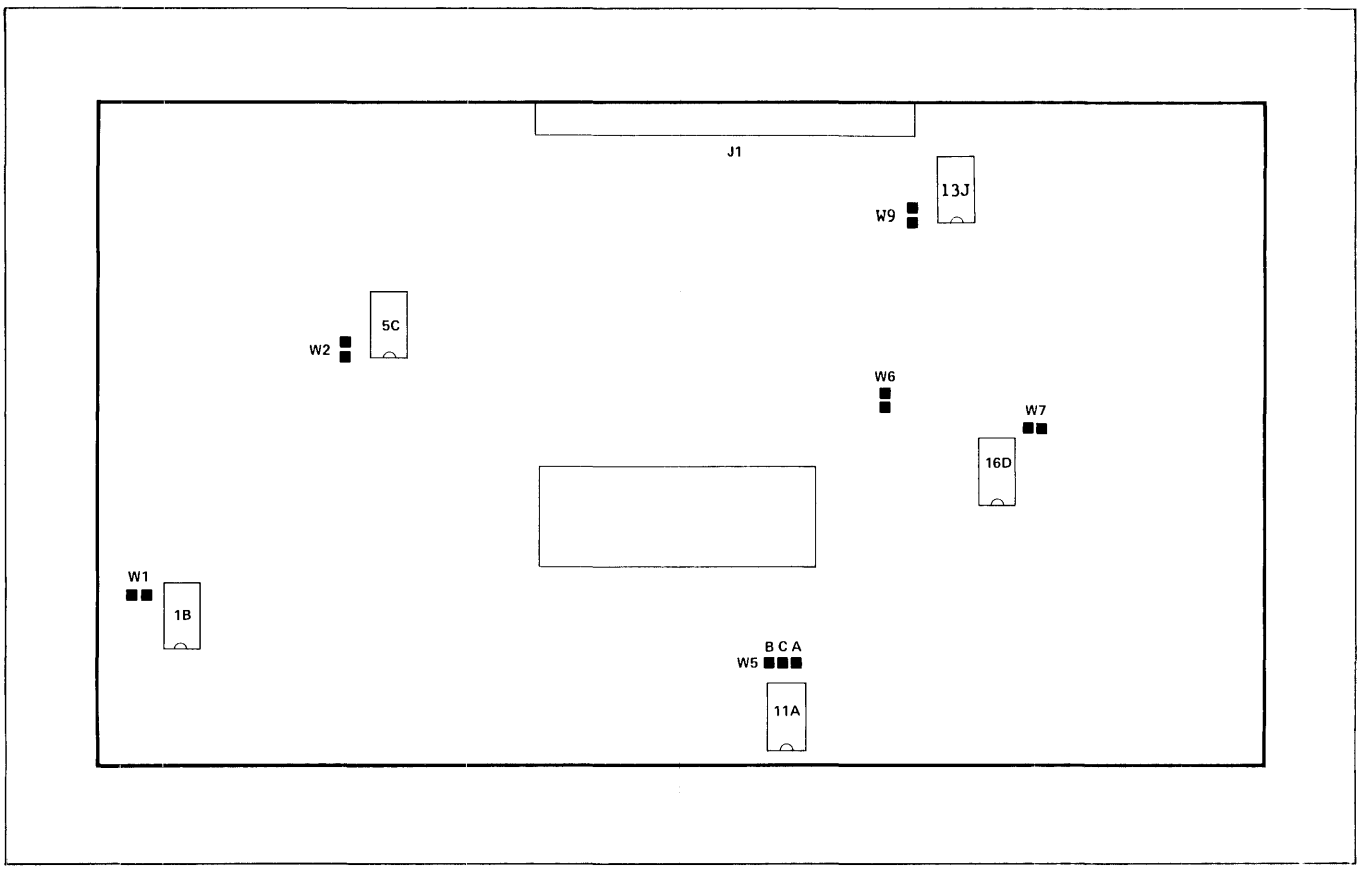


Figure 5-6. Jumper Locations for PCB Assembly 200213

2. "A" Cable Mating connector on Drive or Controller

Description	AMP Part Number
60 pin right angle header	3-86479-4
60 pin vertical header	3-87227-0

3. "B" Cable (Non Shielded)

Description	3M Part Number
Connector (26 pin)	3399-3000
Connector pull tab	3490-2
Flat cable (26 conductor) with ground plane and drain wire	3476-26

4. "B" Cable (Shielded)

Description	Berg P/N	Brand-Rex P/N
Connector (26 pin)	65043-024	
Contact, insert	75691-007	
Cable, shielded 20 pair		T-8277A

5.5.2 DC Power Connector. This connector is used to supply DC power to the drive. It is a 6-pin AMP MATE-N-LOK connector, and the recommended mating connector is an AMP 1-480270-0 socket with AMP 60619-1 pins.

Table 5-4. DC Power Connector

J3-PIN	VOLTAGE
1	Ground
2	+24 VDC
3	−5 VDC
4	−12 VDC
5	+5 VDC
6	Ground (+24V Return)

5.5.3 AC Power Connector. This connector is used to supply AC power to the disc drive when the PRIAM optional power supply is used. The mating connector is a Belden 5PH-386 or equivalent.

Table 5-5. AC Power Connector

PIN	VOLTAGE
L	100 to 240 VAC (HOT)
E	Frame Ground
N	100 to 240 VAC (COMMON)

5.5.4. Remote Panel Connector. The Remote Panel Connector is provided for monitoring drive functions via a front panel or test connector. This is defined in Table 5-6.

Table 5-6. Remote Panel Connector

PIN NO.	J8 3350-20 & 6650-20	J6 if 15450-20
Pin 1	−Write Protect	
Pin 2	−Fault Reset	
Pin 3	−Ready	
Pin 4	GROUND	
Pin 5	−On Cylinder	
Pin 6	−Drive Fault	
Pin 7	180 ohms to GND	
Pin 8	+5 VDC	

Table 5-7. Remote Write Protect Function
(Front Panel Switch Write Protects when closed)

3350-20 (200148)	Open Switch 10N-8 to enable Wr. Prot. Switch
15450-20 (200263)	Open Switch 2E-8 to enable Wr. Prot. Switch

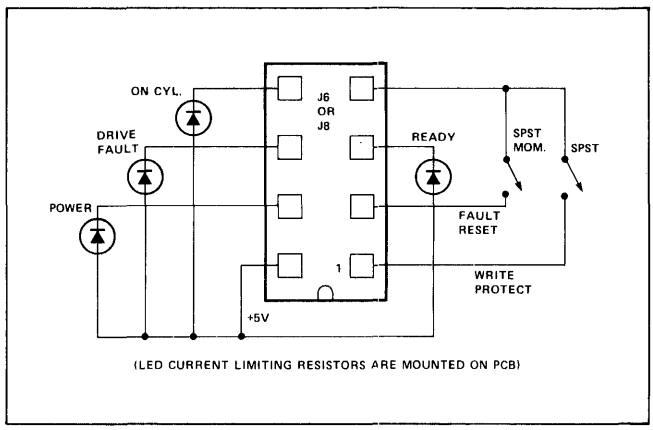


Figure 5-7. Typical Test Panel Schematic

5.5.5 Interface Cable Characteristics. The Interface Cable characteristics are as follows:

1. "A" Cable (Non Shielded)

   Type: 30 twisted pair, flat cable
   Twists per inch: 2
   Impedence: 100 ± 10 ohms
   Wire size: 28 AWG, 7 strands
   Propagation time: 1.6 to 1.8 ns/foot
   Maximum cable length: 100 feet cumulative
   Voltage rating: 300 volts rms

2. "A" Cable (Shielded)

   Type: twisted pair
   Twists per inch: 1.25
   Impedence: 95 ohms
   Wire size: 26 AWG, 7 strands
   Diameter over conductor: 0.039 nominal
   Diameter over insulator: 0.562 nominal
   Propagation time: 1.6 to 1.8 ns/ft
   Maximum cable length: 50 ft cumulative

3. "B" Cable (With Ground Plane)

   Type: 26 conductor, flat cable with ground plane and drain wire
   Impedence: 65 ohms (3M part number 3476-26)
   Wire size: 28 AWG, 7 strands
   Propagation time: 1.5 to 1.8 ns/foot
   Maximum cable length: 50 feet
   Voltage rating: 300 volts rms

4. "B" Cable
   Type: Twinax
   Impedence: 160 ± 16 ohms
   Wire size: 30 AWG, 7 strands
   Diameter over outer insulator: 0.620″ maximum
   Propagation velocity: 70% minimum
   Maximum cable length: 50 feet

5.6 Signal Functional Requirements. Table 5-8 defines the Tag Bus I/O Interface ("A" cable), Table 5-9 defines the Tag Bus Decode data, Table 5-10 defines the "B" cable interface.

Table 5-8. Tag Bus I/O Interface ("A" Cable)

Function	Connector Pins	
	Low	High
Unit Select Tag	43	44
Unit Select 2^0	45	46
Unit Select 2^1	47	48
Unit Select 2^2	51	52
Unit Select 2^3	53	54
Tag 1	1	2
Tag 2	3	4
Tag 3	5	6
Bit 0	7	8
Bit 1	9	10
Bit 2	11	12
Bit 3	13	14
Bit 4	15	16
Bit 5	17	18
Bit 6	19	20
Bit 7	21	22
Bit 8	23	24
Bit 9	25	26
Open Cable Detector	27	28
Index	35	36
Sector	49	50
Fault	29	30
Seek Error	31	32
On Cylinder	33	34
Unit Ready	37	38
Unused (always 0)	39	40
Write Protected	55	56
Power Sequence Pick		57
Power Sequence Hold		58
Unused	41	42
Spare (Optional Bus Bit 10)	59	60

60 position, 28 AWG, 30 twisted pair straight flat cables maximum length — 100 feet

Table 5-9. Tag Bus Decode ("A" Cable)

Bus	Tag 1 Cylinder Address	Tag 2 Head Select	Tag 3 Control Select
Bit 0	2^0	2^0	Write Gate
Bit 1	2^1	2^1	Read Gate
Bit 2	2^2	2^2	Unused
Bit 3	2^3	Unused	Unused
Bit 4	2^4	Unused	Fault Clear
Bit 5	2^5	Unused	Unused
Bit 6	2^6	Unused	RTZ
Bit 7	2^7	Unused	Unused
Bit 8	2^8	Unused	Unused
Bit 9	2^9	Unused	Unused
Bit 10 (optional)	2^{10}	Unused	Unused

Table 5-10. "B" Cable Interface.

Function	Connector Pins Low	High
Write Data	15	14
Ground		13
Write Clock	11	12
Ground		10
Servo Clock	3	2
Ground		1
Read Data	5	6
Ground		4
Read Clock	9	8
Ground		7
Seek End	19	20
Unit Selected	18	17
Ground		16
Index	23	22
Ground		21
Sector	25	26
Ground		24

26 connector flat cable
maximum length — 50 feet

5.6.1 Interface Signal Descriptions. This section gives functional descriptions for the signals on the "A" and "B" interface connectors. Details on how to transmit and receive these signals are given in Section 5.6.2.

Address and control information is transferred to the drive on a 10-bit bus, with three tag lines defining the type of information on the bus. Unit selection is provided by four binary coded lines gated into the drive by a Unit Select tag. Major status conditions of the selected drive, as well as index and sector marks, are returned to the controller on seven lines.

Data and clock signals between the drive and the controller require five lines. These lines are associated with a physical drive using a radial connection between the drive and the controller. Two additional lines in this cable supply an interrupt signal (Seek End) and an indication of selection (Unit Selected). See Tables 5-8 and 5-10 for the pin assignments of these lines on the two interface cables.

1. *Bus Bits 0 to 9* The 10 bus lines are used to transmit cylinder address, head address, or control functions from the controller to the drive. Bit 0 is the least significant bit and Bit 9 is the most significant bit (unless Bit 10 is used).

2. *Tag 1 (Cylinder Address)* When Tag 1 is active, the ten (or eleven) bus lines are used to carry the cylinder address to the drive. Since the drive is a direct addressing device, the controller need only place the new address on the lines and strob the lines with Tag 1 for seek initiation (see Figure 5-10). The drive must be On Cylinder before Tag 1 is sent. The bus lines should be stable throughout the tag time.

3. *Tag 2 (Head Select)* When Tag 2 is active, the bus bit lines are used to carry the head address information to the drive. The controller strobes the head addresses into the drive with Tag 2. In the 3350-20 and 6650-20, only bus bits 0 and 1 are used. In the 15450-20, only bus bits 0, 1 and 2 are used. All other bus bits are ignored.

4. *Tag 3 (Control Select)* Tag 3 acts as an enable, and must be true for the entire read or write operation.

   RTZ operation does not require Tag 3 to remain active. (See Figure 5-10).

   a. Bit 0 (Write Gate)
   Write Gate enables the write driver. See Figure 5-13 for typical Write Gate timing requirements.

   NOTE: The time for switching from Write Gate to Read Gate is 14 microseconds instead of the 10 microseconds required by the standard SMD specification.

   b. Bit 1 (Read Gate)
   Read Gate enables digital read data onto the Read Data lines. The leading edge of Read Gate triggers the read chain to synchronize on an all zeros pattern (see Figures 5-11, 5-12 and 5-13 for typical Read Gate timing).

   NOTE: The time for switching from Write Gate to Read Gate is 14 microseconds instead of the 10 microseconds required by the standard SMD specification.

   c. Bit 2 (Servo Offset Plus)

   In the 3350-20, 6650-20, and 15450-20, this signal causes no physical movement of the heads. It does cause On Cylinder and Seek End to go false for 450 microseconds, in order to meet the normal timing requirements of the SMD family of drives.

   d. Bit 3 (Servo Offset Minus)

   In the 3350-20, 6650-20 and 15450-20, this signal causes no physical movement of the

heads. It does cause On Cylinder and Seek End to go false for 450 microseconds, in order to meet the normal timing requirements of the SMD family of drives.

e. Bit 4 (Fault Clear)

A pulse of 250 nanoseconds minimum, sent to the drive on this line, clears Fault status. The Fault status may re-occur if the fault condition still exists.

f. Bit 5 (AM Enable)

Not supported by this interface. No response will occur when this operation is attempted.

g. Bit 6 (RTZ)

A pulse, 250 nanoseconds minimum, 10 milliseconds maximum, sent to the drive on this line, moves the head carriage to cylinder zero, sets the head address to head zero, and clears Seek Error.

This operation takes significantly longer than a normal seek to cylinder zero. It should be used for re-calibration only and not for normal seek operations.

h. Bit 7 (Data Strobe Early)

Not supported by this interface. No response will occur when this operation is attempted.

i. Bit 8 (Data Strobe Late)

Not supported by this interface. No response will occur when this operation is attempted.

j. Bit 9 (Release)

Not supported by this interface. No response will occur when this operation is attempted.

5. Unit Select Tag

Unit Select Tag is used to select the drive defined by the Unit Select 1, 2, 4, and 8 lines. The drive is selected at the leading edge of Unit Select Tag, and responds within 200 nanoseconds with Unit Selected. The drive address on the Unit Select lines must be stable 200 nanoseconds before the leading edge of Unit Select Tag.

In the 3350-20, 6650-20, and 15450-20, the Unit Select lines must remain stable until 200 nanoseconds after the leading edge of Unit Select Tag. In all drives, the Unit Select Tag must remain stable throughout the time the drive is selected. For detailed timing information, see Figure 5-15.

6. Unit Select 1, 2, 4, and 8

These four lines are binary coded to select one of 16 logical drive addresses. The address placed on the Unit Select lines is compared by each drive against the logical address determined by the settings of the drive address switches on the main PCB. When the Unit Select Tag occurs the drive which matches becomes the one selected. Care must be taken to assure that each physical drive is assigned a different logical address.

Four dip switches are used for assigning the drive a logical address (see Section 5.3.).

7. Individual Lines

a. Sector

The sector mark is derived from Index and the servo track data, using a byte counter. Timing integrity is maintained throughout seek operations (see Figure 5-14). The number of sectors per revolution and/or the number of bytes per sector, is switch selectable. In the 3350-20, 6650-20, and 15450-20, the sector switches are located on the main PCB (see Section 5.3).

The microprocessor sets sector size during initialization. If the switch settings are changed while the drive is powered up, power must be removed from the drive and then restored to cause the newly selected sector size to be established at the drive.

b. Fault

When the Fault line is true, a fault condition exists at the drive. The drive can detect the following types of faults:

1. Write Fault (Write Gate with Write Protect)
2. Write Off Cylinder (Write Gate without On Cylinder)
3. Multiple Heads Selected
4. No transitions during write (MFM format)
5. Write Gate without write current at the head
6. Write current at the head without Write Gate
7. Write during a Servo Offset operation
8. Write Gate and Read Gate occurring simultaneously
9. Read Off Cylinder (Read Gate without On Cylinder)
10. Unable to Restore (RTZ) drive

A fault condition immediately inhibits writing. The Fault line may be reset by Fault Clear, or by Restore (RTZ).

c. Seek Error

When the Seek Error line is true, a seek error has occurred. The Seek Error line may be reset by RTZ. Seek Error indicates that the drive was unable to complete a seek operation. When this condition is detected, the drive automatically returns to cylinder zero.

NOTE: For 3350s, seek addresses greater than 560 (230 Hex), and for 6650 and 15450 Seek addresses of greater than 1120 (460 Hex), will cause Seek Error to go true within 450 microseconds, instead of the 100 nanoseconds required by the standard SMD specification.

d. On Cylinder

On Cylinder indicates that the servo has positioned the heads over the desired data tracks. On Cylinder is reset by a seek operation or a Restore operation.

e. Index

The Index signal occurs once per revolution. Its leading edge is considered the leading edge of Sector Zero. Index is typically a two-byte wide pulse (see Figure 5-14). Timing integrity is maintained throughout seek operations.

f. Unit Ready

Unit Ready indicates that the drive is up to speed, the heads are positioned over the recording surface, and no fault condition exists.

g. Open Cable Detector

The open cable detect circuit disables the interface whenever the "A" Cable is disconnected.

h. Address Mark Found

Address Mark Found is not supported by this interface. This line is always false.

i. Unit Selected

When the four Unit Select lines compare with the setting of the drive address switches on the main PCB and the Unit Select Tag is active, the Unit Select line on the "B" Cable goes true (see Figure 5-15). If, on a daisy-chained system, multiple Unit Selected responses are received by the controller, it may indicate that duplicate switch settings have been used.

j. Write Protected

Setting the Write Protect switch on the drive's main PCB inhibits all write operations, and causes the Write Protected line to be true. Attempting to write to a protected drive will cause the Fault line to go true.

k. Seek End

Seek End is the OR combination of On Cylinder or Seek Error. It indicates that a seek operation has terminated (see Figure 5-10 for timing details).

l. Power Sequencing

Power Sequencing is not supported by this interface. Power Sequence Pick and Power Sequence Hold are interconnected to represent a Sequenced Up drive at all times.

With the 3350-20, 6650-20, and 15450-20 drives, both Power Sequence Pick and Power Sequence Hold must be held at ground potential to enable drive operation. If either line is open, or at +1.4 volts or greater, the drive will sequence down (move the heads to the landing zone and stop the spindle motor) and remain sequenced down until both lines are again at ground potential. When this occurs, the drive will sequence up, and, when the motor is at speed, become Ready.

m. Busy

The Busy indication is not supported by this interface.

8. Data and Clock Lines (see Figure 5-16)

a. Write Data

Write Data carries NRZ data to be recorded on the disc.

b. Servo Clock

The Servo Clock is a phased-locked clock generated from the servo track data. It is used to serialize write data. Servo Clock is available at all times (not gated by Unit Select) while the drive is Ready.

c. Read Data

The Read Data line transmits the recovered data in NRZ form.

d. Read Clock

The Read Clock signal defines the beginning of the data cell. Read Clock is an internally derived clock signal that is synchronous

with the recovered data, as shown in Figure 5-15. Read Clock is in phase with Read Data within 10 microseconds after the leading edge of Read Gate.

e. Write Clock

The Write Clock signal from the controller to the drive must by synchronized with the NRZ write data, as shown in Figure 5-16. The Write Clock is derived from the Read/Reference Clock transmitted by the drive during a write operation. Write Clock need not be transmitted continuously, but must be transmitted at least 250 nanoseconds prior to Write Gate.

5.6.2 Interface DC Characteristics. This section, through tables and figures, sets forth the details that need to be observed, in order to properly transmit and receive the interface signals listed in Tables 5-8 and 5-10 and described in Section 5.6.1.

All input and output signals are differential, using SMD standard transmitters and receivers to provide a terminated, balanced transmission system.

The "A" Cable is a twisted pair flat cable. The "B" cable is a flat ribbon cable with ground plane and drain wire. Twisted pair or ground plane shielding, or both, are used to minimize crosstalk and to reduce inductive coupling.

1. Terminated and Balanced Transmission System

Transmitters and receivers of the SMD standard types 75110A and 75108 or equivalent are used to provide a terminated and balanced transmission system, as shown in Figure 5-7.

2. Line Transmitter Characteristics

The SMD standard line transmitters (Figure 5-8) are compatible with the line receivers described below.

a. Output Signal Levels

Data Signals: See Figure 5-7.
Control Signals: See Figure 5-8.

b. Output Line Polarity

Control Signals: On the "A" Cable, the transmitters are connected to the I/O line so that the output, labeled Z (Figure 5-8) is connected to

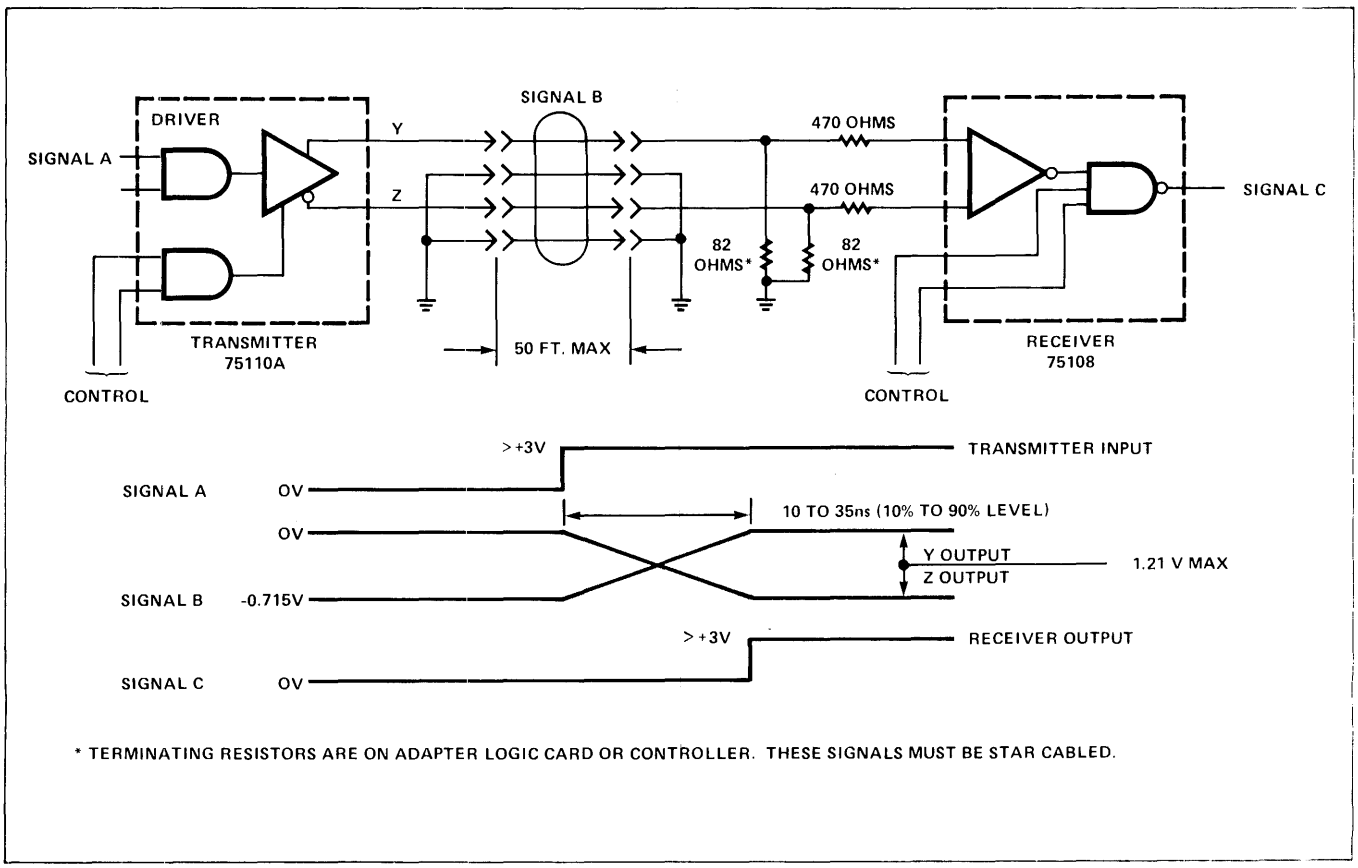


Figure 5-8. Typical Read/Write Data and Clock Transmitter and Receiver

the odd numbered pin of the cable connector. This output in turn connects to the receiver pin labeled B (Figure 5-9) except for the Unit Selected line, which is connected in the opposite manner.

When transmitter and receiver are connected in this manner, a logical 1 into the transmitter produces a logical 1 out of the receiver, except for the Unit Selected line, where a logical 1 into the transmitter produces a logical 0 out of the receiver.

3. Input Amplifier (Receiver) Characteristics

The drive's input amplifier (Figure 5-9) is SMD-standard compatible with the line transmitter described above.

a. Receiver Propagation Delay

The receiver propagation delay is typically 17 nanoseconds, both for a logical 0-to-1 transition and for a logical 1-to-0 transition.

b. Receiver Input Polarity

Control Signals: The input, labeled B (Figure 5-9) on the receiver is connected to the odd numbered pin cable connector, and thus connects to the transmitter pin labeled Z (Figure 5-8).

Data Signals: See Figure 5-7.

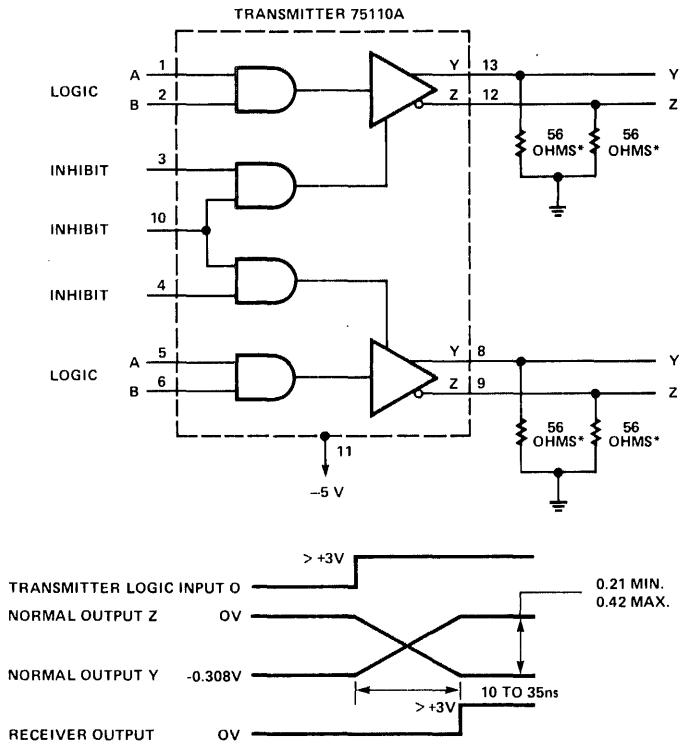


Figure 5-9. Control Line Transmitter

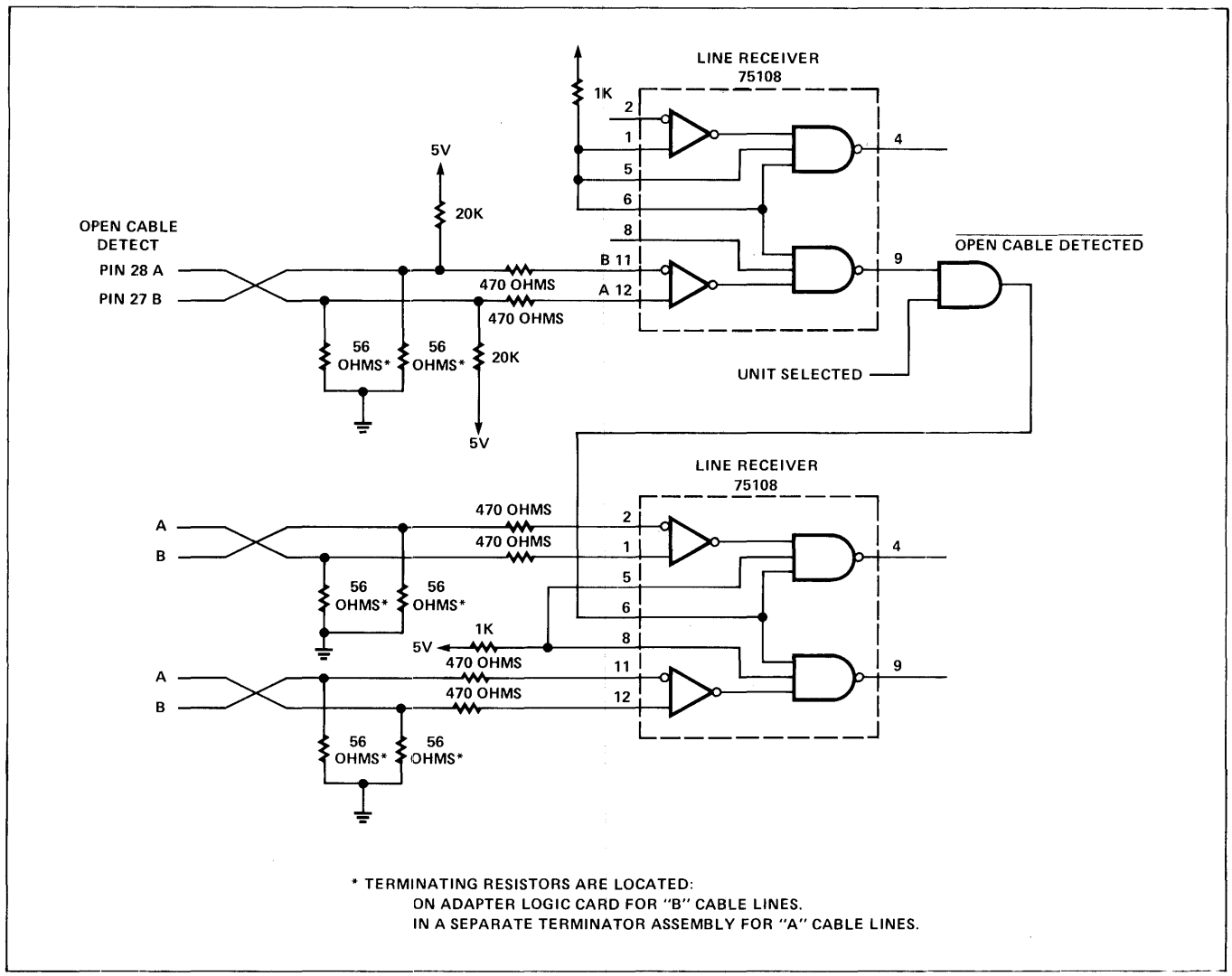
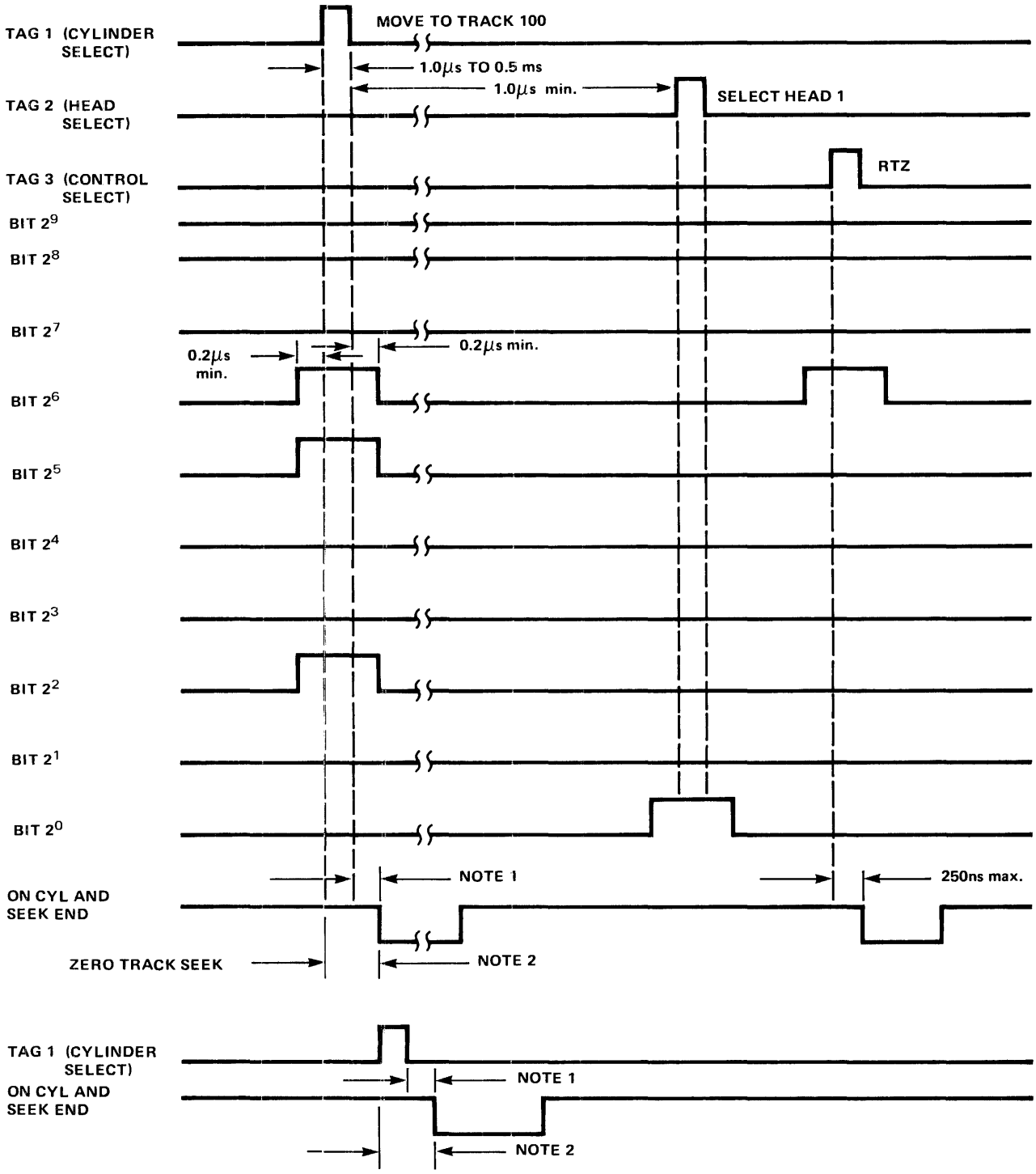


Figure 5-10. Control Line Receiver

5.6.3 Interface Timing. This section discusses the timing requirements for the various operations performed on the controller interface.

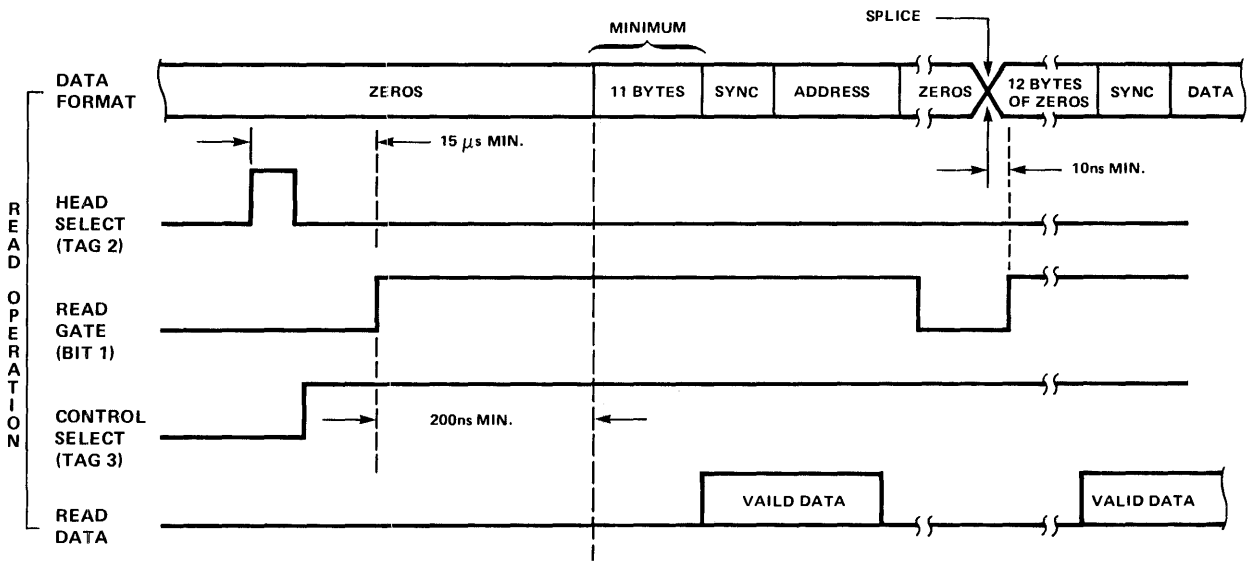


NOTE 1: 120 ns MAXIMUM FOR 3350 SMD, 6650 SMD, AND 15450 SMD (14" DRIVES WITH IMBEDDED SMD INTERFACE). SEE NOTE 2 FOR ALL OTHER DRIVES.

NOTE 2: 450 ns FROM LEADING EDGE OF TAG 1 FOR ALL DRIVES USING SMD ADAPTER.

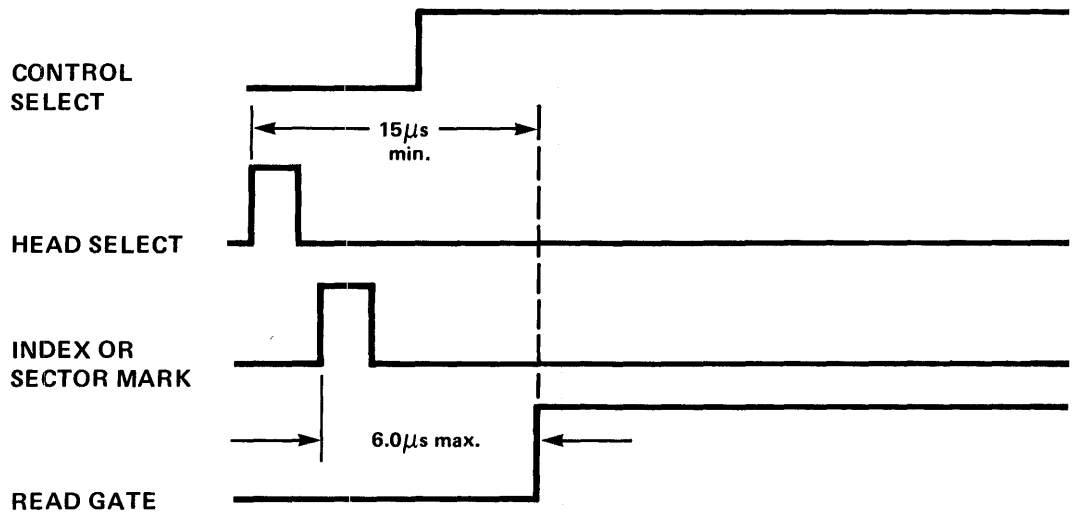
ON CYLINDER AND SEEK END SIGNALS ARE IDENTICAL UNLESS A SEEK ERROR OCCURS. SEEK ERROR INITIATES A CONSTANT SEEK END UNTIL RTZ CLEARS THE ERROR.

Figure 5-11. Tag and Bus Timing



READ GATE MUST BE DROPPED PRIOR TO THE WRITE SPLICE. IT MUST BE RAISED AT LEAST ONE BIT AFTER THE WRITE SPLICE, AND WITH AT LEAST 10 BYTES OF ZEROS REMAINING IN THE SYNC FIELD. A 12-BYTE EXAMPLE CONSISTS OF ONE BYTE FOR WRITE SPLICE AND 11 BYTES FOR VFO SYNC.

Figure 5-12. Typical Read Timing



IF A READ OPERATION IS TO BE PERFORMED AFTER INDEX OR SECTOR MARK, READ GATE MUST NOT OCCUR LATER THAN 6.0 MICROSECONDS AFTER THE LEADING EDGE OF INDEX OR SECTOR MARK.

Figure 5-13. Typical Read Control Timing

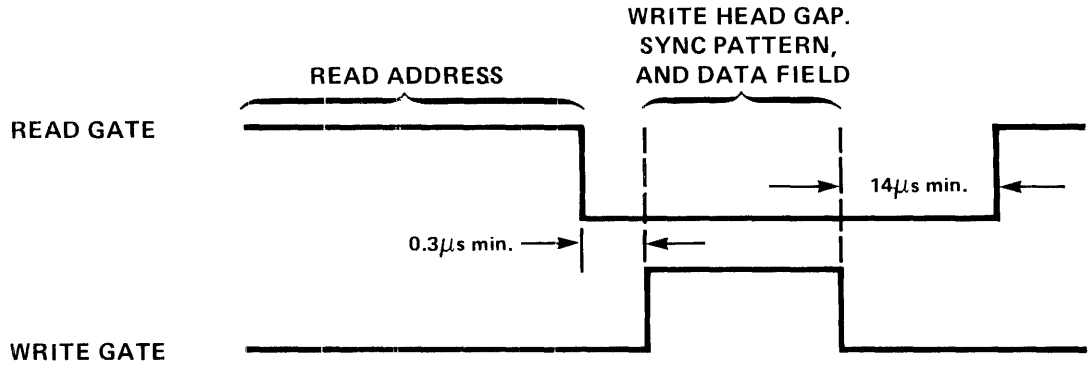
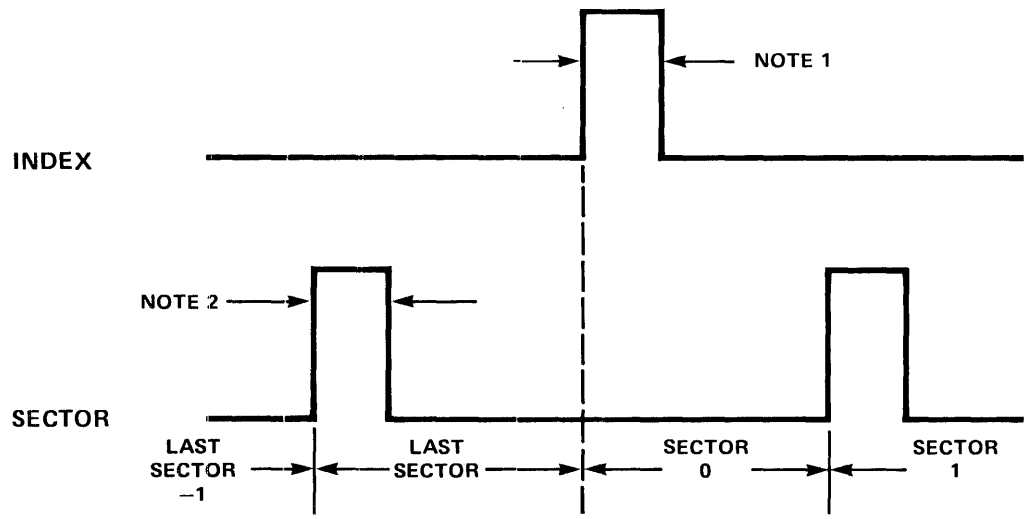


Figure 5-14. Typical Write Control Timing



NOTE 1: 1.24 ± 0.03 MICROSECONDS FOR 3450 AND 7050 USING SMD ADAPTER

NOTE 2: 1.24 ± 0.03 MICROSECONDS FOR 3450 AND 7050 USING SMD ADAPTER

Figure 5-15. Index and Sector Mark Timing

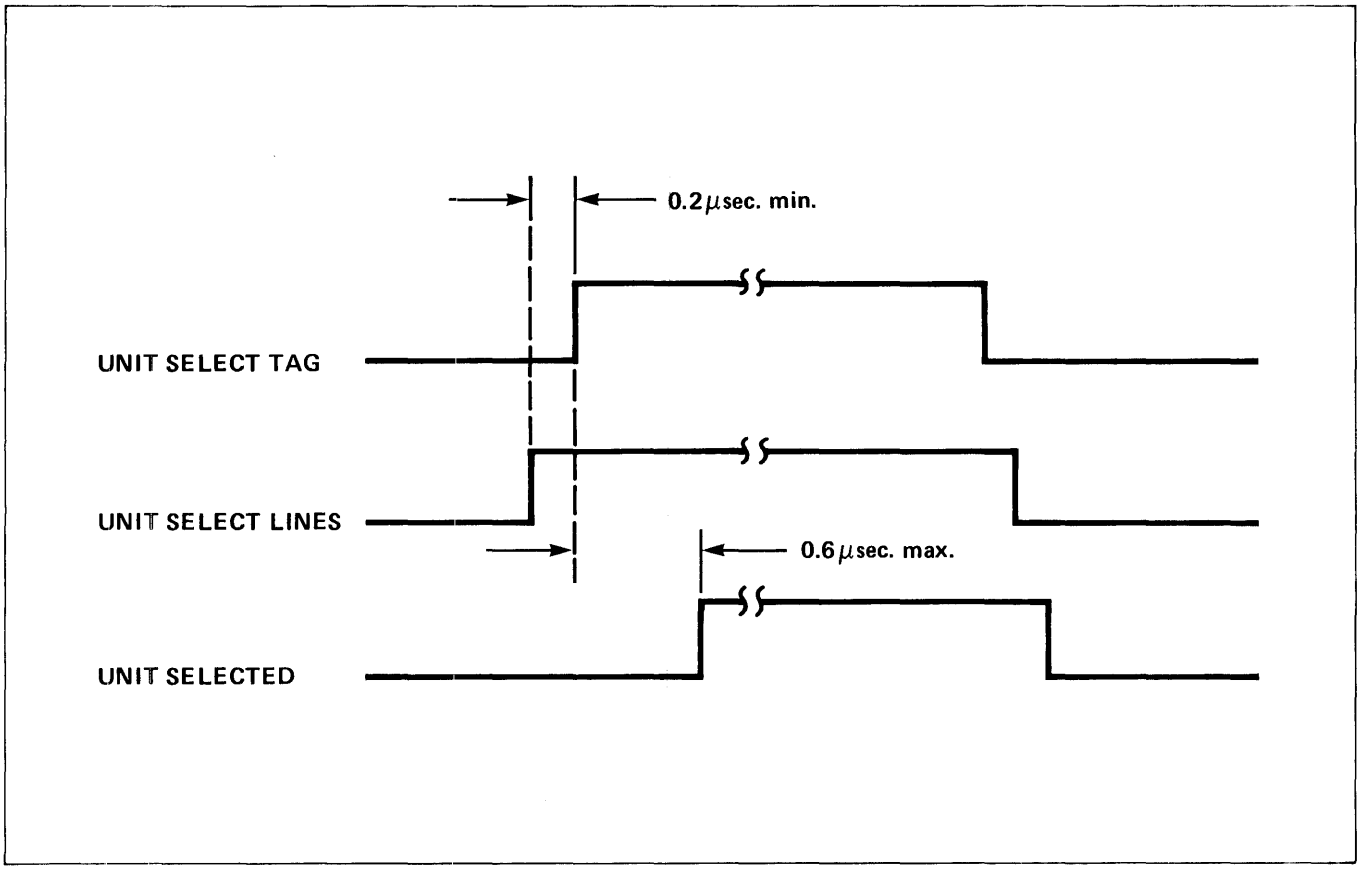


Figure 5-16. Drive Select Timing

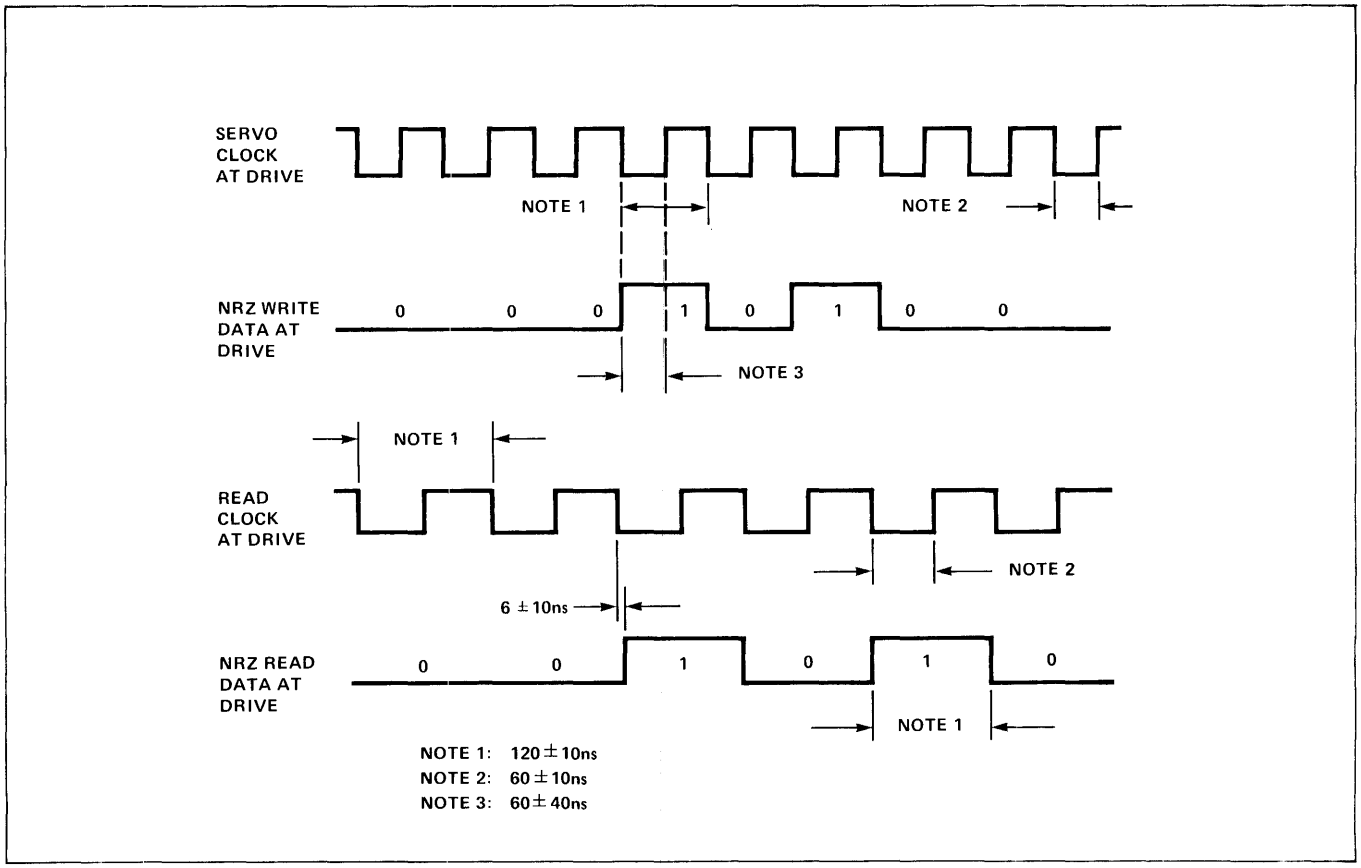


Figure 5-17. NRZ Data and Read Clock Timing

5.7 Track Format Considerations. Some hardware constraints must be observed when designing a track format. The following sections discuss these design characteristics and other important related details to be considered in the design of the track format.

5.7.1. Write/Read Timing Constraints

1. Read Initialization Time

   Between the de-selection of one head and the selection of another head, there is a 5-microsecond delay within the drive, due to circuit characteristics. The time from the initiation of a head change until data can be read using the selected head is 25 microseconds maximum (5 microseconds for head selection, 10 microseconds for read amplifier stabilization, and 10 microseconds for VFO synchronization).

2. Write-to-Read Recovery Time

   Assuming head selection is stabalized, the time lapse before Read Gate can be enabled after switching Write Gate off is 10 microseconds minimum.

3. Read-to-Write Recovery Time

   Assuming head selection is stabilized, the time before Write Gate can be enabled after switching Read Gate off is 1.0 microsecond minimum.

4. Beginning-of-Record Tolerance

   This tolerance (a gap of 9 bytes) allows for write splice and write-to-read recovery time for multi-sector operations (see Figure 5-17).

5. Read VFO Synchronization

   Nine microseconds are needed for the variable frequency oscillator to synchronize. Zeros should be written during this time.

6. Sync Pattern

   The sync pattern, indicating the beginning of the address or data area, consists of 1 byte.

7. Write Driver Turn On

   The write driver turn on time is about 960 nanoseconds (one byte time). This time must be accounted for, in order to know where the write splice areas are located.

5.7.2 Control Timing Constraints

1. Read Data Field

   Read Gate is the control line associated with a read operation.

   The leading edge of Read Gate allows the VFO to synchronize on an all-zeros pattern. Read Gate also enables the output of the data separator onto the I/O lines. There may be invalid data transitions on these lines during the synchronization period. Read Gate must be dropped and raised again after going through a write splice area. Read Gate may be enabled 60 ± 4 clock periods after the leading edge of Index or Sector.

   The sync pattern search may begin 72 servo clock periods (9 byte times) after the leading edge of Read Gate.

   Head switching and read amplifier stabilization requirements (Figure 5-17) determine the latest time at which a head can be selected, in order to read the next successive sector, using the format shown in Figure 5-17.

   Read Data and Read Clock may not have valid data until 9 microseconds after the leading edge of Read Gate, due to the VFO synchronizing time.

   There should be no write splice area while Read Gate is raised.

2. Write Data Field

   Write Gate is the control line associated with a write operation.

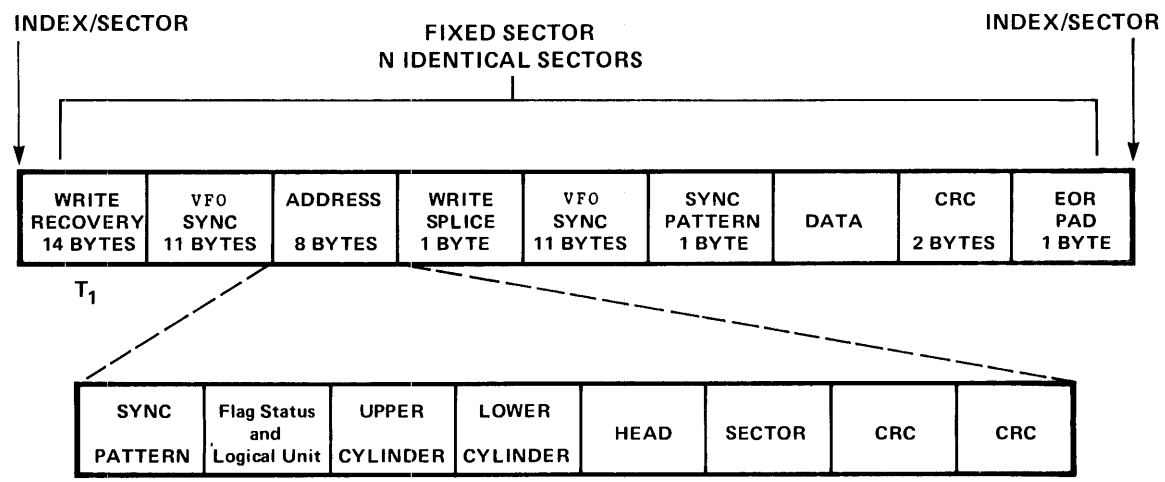
   The sector address must always be read and verified, prior to writing the data field, except while formatting.

   Writing the data field must always be preceded by writing the VFO sync field and sync pattern.

   The controller must provide an internal delay of at least two bit times (approximately 240 nanoseconds) between the trailing edge of Read Gate and the leading edge of Write Gate. This delay allows for signal propagation tolerances and prevents overlap of Read Gate and Write Gate in the drive.

Writing the data field must always be followed by writing the data checkword and at least an eight-bit gap of zeros at the end of the checkword.

During formatting, Write Gate is raised upon detecting index or sector. During a record update, Write Gate is raised within two byte times after the last bit of the address.



T_1 = TIME BETWEEN LEADING EDGE OF INDEX/SECTOR AND READ GATE. A SPLICE POINT MAY EXIST WITHIN THIS AREA.

EXAMPLE: WHAT IS THE DATA FIELD LENGTH USING 66 SECTORS?

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK}}{\text{NUMBER OF SECTORS/TRACK}} - \text{(SYNC FIELDS, TOLERANCE, GAPS AND ADDRESSES)}$$

$$= \frac{20{,}160^*}{66} - 49 = 256 \text{ BYTES/SECTOR}$$

$$\%\ \text{EFFICIENCY} = \frac{256 \times 66}{20{,}160} \times 100 = 83.8\%$$

* 20,160 BYTES/TRACK ASSUMED.

NOTE: WRITE RECOVERY IS 14 BYTES INSTEAD OF 16 BYTES, AND EOR PAD IS 1 BYTE INSTEAD OF 8 BYTES, AS RECOMMENDED BY THE STANDARD SMD SPECIFICATION.

Figure 5-18. Recommended Sector Format

5.7.3 Suggested Data Format. All PRIAM Disc Drives are programmable hard sectored drives. Index and sector marks are derived from the servo sync generated from the servo head. The number of sectors per track is programmed by the user by setting the appropriate sector DIP switches located on the drives' Main PCB. Once these switches are set and the drive is formatted, the sector count is fixed. If the sector count is changed in the sector switches, then the drive has to be reformatted.

Provision must be made in the system software to perform a write format operation over the entire disc (see Figure 5-17). To insure reliable recording and retrieval of data on PRIAM drives, the following formatting procedure is recommended:

1. Select desired drive, cylinder, head and sector.

2. The controller must provide a 5 microsecond minimum delay after selecting a head before the leading edge of a sector pulse is detected.

3. Search for leading edge of desired sector.

4. Detect leading edge of the desired sector and raise Write Gate.

5. Write all zeros for write recovery and VFO sync field (24 bytes minimum).

6. Write a sync pattern, the address, and the address checkword.

7. Write all zeros for write splice gap and VFO sync field (12 bytes minimum).

8. Write a sync pattern, the data field, the two-byte data field checkword, and the five-byte field of zeros (see Figure 5-17). The data field should preferably be a worst case pattern.

9. The end tolerance gap specified by the standard SMD specification is not required by this drive. However, if it is used, it is recommended that zeros be written to the next sector pulse.

10. If the next sector of the same track is to be formatted, and the head is not deselected, Write Gate should be left on in this case. All zeros should be written until the leading edge of the next address field.

5.8. System Grounding. PRIAM recommends an AC grounding scheme as shown in Figure 5-18.

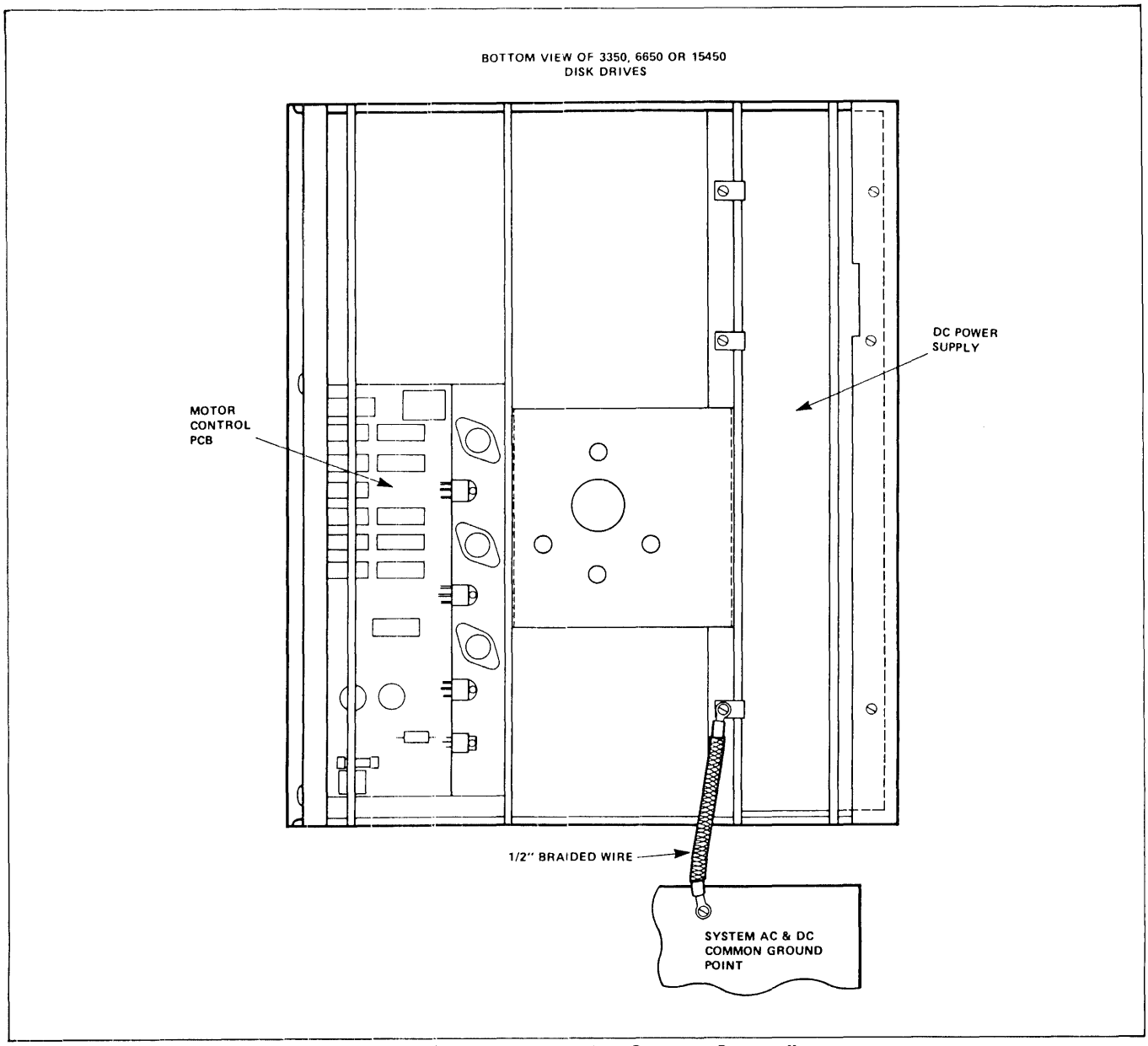


Figure 5-19. Recommended System Grounding

APPENDIX A
Return of PRIAM Drives for Servicing

IF YOU PURCHASED THIS PRODUCT DIRECTLY FROM PRIAM

To obtain repair service, whether the unit is under warranty* or not, contact PRIAM Field Service, San Jose. You will need to provide the product type/model, serial number, a purchase order number and a brief description of the reason for return. We will provide a Return Authorization number to be prominently displayed on a shipping container in which the product(s) are being returned, and a quote of estimated charge, if any. The product should be packaged in its original shipping case or other adequate packaging to prevent in-transit damage (see Section 3.4). Such damage is not covered by PRIAM. Ship ONLY the drive. Remove all non-PRIAM accessories (e.g., slides, cabinets, cables).

*To determine warranty coverages please refer to the warranty information included with your purchase agreement.

IF YOU OBTAINED THIS PRODUCT FROM A SOURCE OTHER THAN PRIAM

Please contact the firm that provided you with this product concerning servicing. PRIAM does not offer repair service, whether in warranty or out, to anyone other than the original PRIAM customer. All PRIAM warranties are non-transferable.

APPENDIX B
Environmental Specifications for Drives Packed in PRIAM Shipping Container

Ambient Temperature	-40° to 60°C (-40° to 140°F)
Relative Humidity	5% to 95% without condensation.
Altitude	From 1000 feet below sea level to 40,000 feet above sea level.
Shock	Will meet Interstate Commerce Commission drop test requirements, Federal Test Method Standard 101B, Methods B and D, Level A.

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