DISKOS 3350

DISC DRIVE PRODUCT SPECIFICATION

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DISKOS 3350 PRODUCT
SPECIFICATION

INDEX

FIGURES

I. INTRODUCTION

A. Purpose

This specification describes the performance and the physical and electrical characteristics of the PRIAM DISKOS 3350 disc drive. It provides the necessary information to connect a DISKOS 3350 to a disc drive controller through a microprocessor type of interface.

B. General Description

The DISKOS 3350 uses advanced Winchester and microprocessor technologies to provide users with a low-cost disc drive having high capacity, fast access, and long-term reliability. A linear motor voice coil positioner with track following servo enables the DISKOS 3350 to position Winchester type heads quickly and precisely. These low-force heads assure high data reliability. An advanced Winchester-technology disc is driven by a brushless DC motor; the head positioner coil and carriage, heads, and disc are enclosed in a sealed, contamination-resistant chamber to assure high reliability.

Two heads are used with each disc surface, and a full head area on the disc is dedicated to servo information for track following, seeking, and write timing. Thus, the complete 3350 Winchester disc drive technology recently introduced in large and expensive disc systems is applied to a low cost drive designed for small system use.

A microprocessor provides interface flexibility and monitors drive operation. For example, it controls the power up and down sequencing and a self-test program checks drive performance during each power up sequence. Any malfunction detected by these tests will prevent drive start-up, reducing the chance of loss of data or damage to the drive.

C. Features

1. 33 megabytes of mass storage at low cost for small system usage.

2. Advanced Winchester technology discs and heads provide efficient and cost-effective data density.

3. Linear motor voice coil positioner offers:

   a. Fast access to data.

   b. Mechanical simplicity and precise positioning.

   c. Potential for expanded capacity with same basic device.

   d. High reliability head carriage with compensation for long-term wear.

4. Track following head positioning servo assures:

   a. High data reliability through exact locating of heads on data tracks.

   b. Accurate tracking regardless of thermal effects on drive.

   c. Short start up time of 30 seconds nominal.

5. Brushless DC spindle drive motor improves reliability by:

   a. Accelerating and braking the disc quickly, extending disc and head life and improving data reliability.

   b. Elimination of the belts, pulleys, switches, starting capacitors, and mechanical brakes normally associated with AC motors in Winchester disc drives.

   c. Elimination of brushes so that brush wear and noise problems do not occur.

6. On-track skip defect lengthens product life and improves data reliability.

7. Reserved area on disc surface for head landing and takeoff protects data integrity.

8. Ultra-short length of 20 inches facilitates use with advanced, smaller systems.

9. Light weight--only 33 pounds--reduces cost of installation.

10. Flexible, microprocessor-based interface:

    a. Eliminates handshake protocols, freeing valuable processor time.

    b. Supports daisy-chained drives and overlapping seeks.

    c. Simplifies controller design and allows up to a 25-foot controller cable without the need for additional line drivers and receivers.

11. Microprocessor-controlled self-test protects data and the drive and aids troubleshooting.

12. Proprietary closed air system with positive pressure and continuous refiltration of air assures long term data reliability by preventing entry of contaminants into head/disc chamber.

13. DC operation permits flexibility of prime power source and ease of battery backup.

14. Skip defect data is stored within the drive, eliminating the need for defect record keeping and manual insertion of data during system integration.

15. Open, welded-rod frame enhances free circulation of cooling air within the system cabinet.

16. VFO/data separator provided.

17. Selectable sector size: 16 to 4096 bytes, including gaps and headers.

18. Optional integrated power supply fits within small DISKOS 3350 package size.

II. PRODUCT DESCRIPTION

A. Operational Specifications

Operational specifications of the DISKOS 3350 disc drive are shown in Table 1 below.

TABLE 1. DISKOS 3350 OPERATIONAL SPECIFICATIONS

Capacity (unformatted)	33.9 Mbytes
Bytes per track	20,160
Bytes per cylinder	60,480
Number of cylinders	561
Single Track Positioning Time	8 ms
Average Track Positioning Time	45 ms
Maximum Track Positioning Time	85 ms
Average Rotational Latency Time	9.7 ms
Recording Density	6,430 BPI
Track Density	480 TPI
Data Transfer Rate	1.04 Mbytes/sec
Recording Code	MFM
Interface Code	NRZ
Start Time	30 sec
Stop Time	30 sec

B. Physical Characteristics

The physical characteristics of the DISKOS 3350 disc drive are shown in Table 2 below.

TABLE 2. DISKOS 3350 PHYSICAL CHARACTERISTICS

CHARACTERISTIC	BASIC DRIVE	RACK MOUNTED OPTION
Height (inches)	6.8	6.8
Width (inches)	16.6	17.6
Depth (inches)	20.0	20.0
Weight (pounds)		
With power supply	50	56
Without power supply	33	39

Mounting attitudes of the drive are as follows:

1. Horizontal: Spindle motor down.

2. Vertical: On either edge; positioner motion horizontal.

The physical and mounting dimensions for the drive are shown in Figure 1.

C. Controls

1. PANELS

The DISKOS 3350 drive is normally supplied without a front panel. There are no front panel controls or indicators.

There is no rear panel. All connections are made directly to the printed circuit board via ribbon cable type connectors.

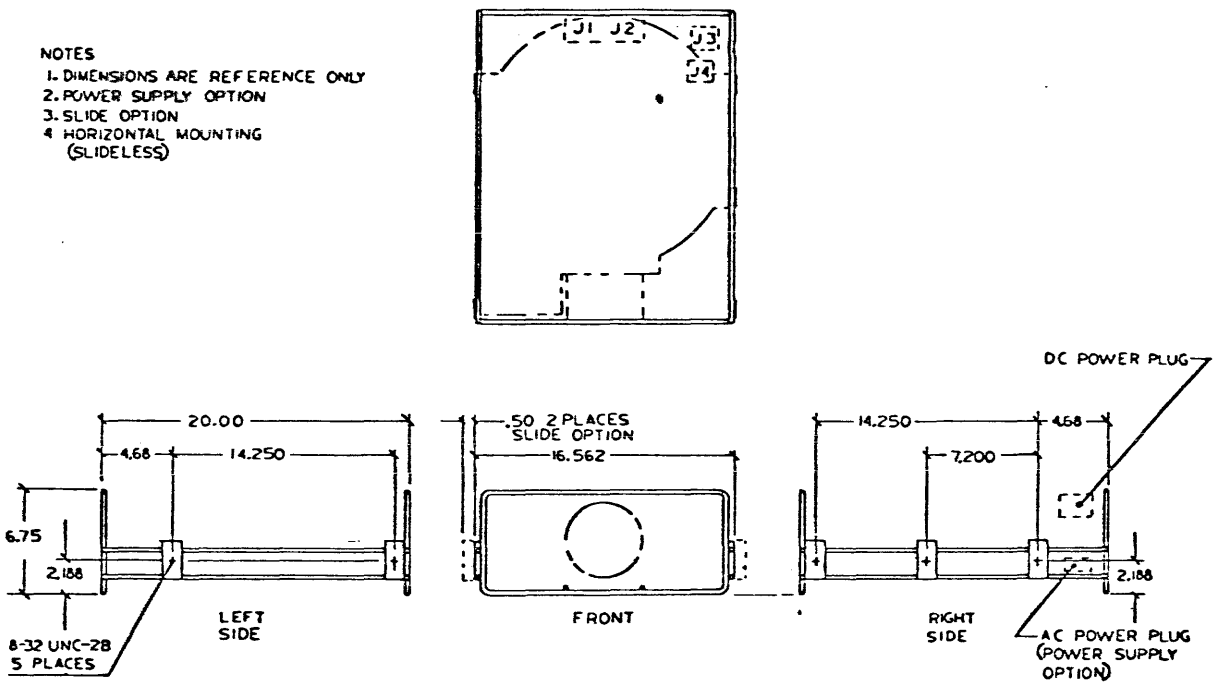


Figure 1. DISKOS 3350 DISC DRIVE

2. INTERNAL CONTROLS

Mini-dip type switches are provided to select drive address, sector length, and write protect functions, as shown below.

TABLE 3. DISKOS 3350 INTERNAL CONTROLS

Switch 16R-1	Select Drive Address 1
Switch 16R-2	Select Drive Address 2
Switch 16R-3	Select Drive Address 3
Switch 16R-4	Select Drive Address 4
Switch 16R-5	Skip Defect Write Enable
Switch 16R-6	Write Clock Phase Select
Switch 16R-7	Write Clock Transmit Enable
Switch 16R-8	Write Protect - Head 2
Switch 23N-8	Sector Length - bit 16
Switch 23N-7	Sector Length - bit 32
Switch 23N-6	Sector Length - bit 64
Switch 23N-5	Sector Length - bit 128
Switch 23N-4	Sector Length - bit 256
Switch 23N-3	Sector Length - bit 512
Switch 23N-2	Sector Length - bit 1024
Switch 23N-1	Sector Length - bit 2048

D. Environmental Characteristics

1. TEMPERATURE

a. Equipment Operational: 10° C to 40° C (57° F to 104° F).

b. Equipment Non-operational: -40° C to 60° C (-40° F to 140° F).

c. 150 feet per minute air velocity must be maintained over base casting.

2. HUMIDITY

a. Equipment Operational: 10% to 80% relative humidity, with a wet bulb temperature limit of 26° C (78° F) without condensation.

b. Equipment Non-operational: 10% to 80% without condensation.

3. ALTITUDE

a. Equipment Operational: From 1000 feet below sea level to 7000 feet above sea level.

b. Equipment Non-operational: From 1000 feet below sea level to 40,000 feet above sea level.

E. Reliability

1. MTBF

The DISKOS 3350 has an expected Mean Time Between Failures (MTBF) of 8000 power-on hours.

2. MTTR

The DISKOS 3350 is designed so that the Mean time to Repair (MTTR) is less than 1/2 hour.

3. PREVENTIVE MAINTENANCE

No preventive maintenance is required.

F. Power Requirements

1. DC POWER REQUIREMENTS

When the DISKOS 3350 is provided without the power supply and with the standard microprocessor interface, the following power is required from the system:

+24 VDC, ± 5%, 7A maximum;	7A Typical @ startup, 5.5A typical after startup during seek operation & 4A typical after startup but not seeking.
+ 5 VDC, ± 5%, 4A maximum;	1.5A Typical
- 5 VDC, ± 5%, 2A maximum;	1A Typical
-12 VDC, ± 5%, 0.7A maximum;	0.5A Typical.

2. AC POWER REQUIREMENTS

When the DISKOS 3350 is provided with its own power supply, the following power is required:

Power: 425 watts;

Voltage: 100 VAC ± 10%, 50-60 HZ;
120 VAC ± 10%, 50-60 HZ;
220 VAC ± 10%, 50-60 HZ;
240 VAC ± 10%, 50-60 HZ.

III. DATA INTEGRITY

A. Seek Errors

Seek errors result when the head does not reach the correct track, which can be verified by reading the ID field. Whenever such an error occurs, the drive's track counter must be reset to zero by issuing a RESTORE command to the drive, which will move the head back to cylinder zero. Then a new SEEK command may be issued.

Seek incomplete occurs when the track following servo is unable to lock onto a track within 3.1 milisec. The drive will automatically restore the heads to cylinder zero and give SEEK FAULT status. Then a new SEEK command may be issued.

The seek error rate is less than one error in 10^6 SEEK executions.

B. Recoverable Errors

Recoverable read errors result from transient conditions and are usually corrected by simply re-reading. Errors are normally detected by using cyclic redundancy checking (CRC), performed in the disc drive controller. Each field is normally terminated with two CRC bytes.

The recoverable read error rate is less than one error in 10^{10} bits.

C. Non-Recoverable Errors

A non-recoverable error is one which persists after 10 attempts to read the record. This error may be a write error, in which case rewriting the record clears the error. Or, the error may be a disc defect, in which case the error may persist even though the record is rewritten.

The non-recoverable error rate is less than one error in 10^{13} bits. Errors that are detected and mapped (either by alternate track or skip defect methods) during initialization are not included in determining this error rate.

D. Defects

A maximum of 40 defects per drive are allowed, with no more than three on any one unflagged data track. Each defect is 2 or less bytes long.

A maximum of 15 tracks may be flagged with each flagged track counting as one defect occurrance. Tracks are flagged when the number of defects per track exceeds 3, or when any single defect is longer than 2 bytes.

E. Defect Information

Recorded on each track between index and the first sector pulse is a short data record which contains defect information relating to that track. This record contains the location of the byte containing the first bit in error (in bytes from index, $\pm$ 1 byte). Each location is contained in a two byte binary address. There are three location addresses and a flag byte in the record. All zeroes indicates that there are no defects in the track. See Fig. 17 for the defect record format.

This information is accessed by initiating a read, coincident with the front edge of the index pulse, *and* reading until the leading edge of the sector pulse. See paragraph V.B.2 for the skip defect record definition.

IV. INTERFACE

A. General

PRIAM offers a basic 8-bit bidirectional bus control interface designed to be readily connected to popular 8-bit and 16-bit microprocessors. Across this interface all spindle motor and head positioning controls are passed.

Read and Write Data is passed via synchronous serial-bit NRZ signal lines. The interface provides INDEX, SECTOR MARK, READ/REFERENCE CLOCK, and WRITE CLOCK signals.

Up to four drives may be daisy chained along a single 50 conductor flat ribbon cable. Power is provided via a separate connector.

Each of these interface areas is discussed in the balance of this section in terms of:

1. Address and Command Control;

2. Serial Data Transfer;

3. Physical Interface.

B. Address and Command Control

All cylinder addresses, status information and commands are transferred over a three-state bidirectional DBUS 0 through 7 lines. These eight lines present an open circuit (tri-state) to the controller's bus until activated by DRIVE SELECT. An active DRIVE SELECT combined with RD (Read) sets the DBUS into the transmit mode while DRIVE SELECT combined with an active WR (Write) sets the DBUS into the receive mode. The information to control the DISKOS 3350 resides in six accessible 8-bit registers. These are:

1. Control Command Register which receives and stores commands from the controller;

2. Target Address Register - Upper Byte which receives the two most significant bits of the desired cylinder address;

3. Target Address Register - Lower Byte which receives the eight least significant bits of the desired cylinder address;

4. Status Register which contains pertinent information about present operation;

5. Current Address Register - Upper Byte which contains the two most significant bits of the current cylinder address;

6. Current Address Register - Lower Byte which contains the eight least significant bits of the current cylinder address.

Accessing of the registers is accomplished by a combination of active levels on DRIVE SELECT, RD, or WR, and register address lines A1 and A0, as shown in Table 4. The Command and Target Address Registers can only receive information and the Status and Current Address Registers can only transmit information.

TABLE 4. REGISTER SELECTION

A1	A0	WR	RD	Selected Register
0	0	0	1	Status Register
0	0	1	0	Command Register
0	1	0	1	Current Address-Upper Byte
0	1	1	0	Target Address-Upper Byte
1	0	0	1	Current Address-Lower Byte
1	0	1	0	Target Address-Lower Byte

Five Control Commands are used. All are single byte commands and are listed in Table 5.

TABLE 5. COMMAND SUMMARY

	BITS							
COMMAND	7	6	5	4	3	2	1	0
SEQUENCE UP	0	0	0	0	0	0	0	1
SEQUENCE DOWN	0	0	0	0	0	0	1	0
RESTORE	0	0	0	0	0	0	1	1
SEEK	0	0	0	0	0	1	0	0
FAULT RESET	0	0	0	0	0	1	0	1

1. SEQUENCE UP

The SEQUENCE UP Command causes the disc drive spindle motor to power up. The rotational speed of the disc is monitored, and when the drive is up to speed, the heads are positioned to cylinder zero. CYLINDER ZERO, SEEK COMPLETE and READY status is set at the successful completion of this command.

2. SEQUENCE DOWN

The SEQUENCE DOWN command causes the heads to be positioned to the landing zone and the spindle motor is braked to a stop. WRITE PROTECT status will be set at the completion of this command.

3. RESTORE

The RESTORE command causes the drive carriage to be repositioned to cylinder zero. The drive RESTORES automatically on SEQUENCE UP, or when a SEEK FAULT is detected, or when an "off track" condition is detected while in the track following (READY) mode.

4. SEEK

The SEEK command uses the contents of the Target Address Registers (both Upper and Lower) for desired cylinder address information. Upon receipt of this command, the drive will go NOT READY and will move the carriage to the desired cylinder. When this is complete, the drive will again become READY and SEEK COMPLETE status will be posted.

5. FAULT RESET

The FAULT RESET command clears both fault condition flip-flops (SEEK FAULT and DRIVE FAULT).

The following table is a definition of the various bits in the Current Address Register and Target Address Register.

TABLE 6. ADDRESS REGISTER BIT DEFINITION

	7	6	5	4	3	2	1	0
Current Address Reg. Upper Byte	0	0	0	0	0	0	C_9	C_8
Current Address Reg. Lower Byte	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
Target Address Reg. Upper Byte	0	0	0	0	0	0	C_9	C_8
Target Address Reg. Lower Byte	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

where . . .

	C_9	C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
Cylinder 000	0	0	0	0	0	0	0	0	0	0
Cylinder 001	0	0	0	0	0	0	0	0	0	1
:										
:										
:										
:										
Cylinder 554	1	0	0	0	1	0	1	0	1	0
Cylinder 555	1	0	0	0	1	0	1	0	1	1

The following is a definition of the various bits of the Status Register.

TABLE 7. STATUS REGISTER BIT DEFINITION

Bit	Name	Description
0	Ready	The drive is up to speed, servo system is locked onto a servo track, and the unit is in a state to read, write, or seek.
1	Seek Complete	This bit is set when seek operation is completed.
2	Seek Fault	A fault was detected during a seek operation.
3	Cylinder Zero	Access arm is set to Cylinder 0.
4	Busy	Drive is in process of executing a command.
5	Drive Fault	A fault was detected during a write operation or a drive unsafe condition was detected.
6	Write Protect	The head selected is write protected. Write protection is set by switches in the drive or when the drive is not sequenced up.
7	Command Reject	Control or Register Load command received while drive is not ready, or improper command received.

The timing and electrical details are described in the Physical Interface part of this section.

C. Serial Data Transfer

Several individual signal lines provide timing and status information to facilitate the serial data transfer between the drive and controller. These signals are:

1. INDEX

A 6.8-microsecond pulse that occurs whenever the servo track index mark is encountered to indicate the beginning of a track. The timing is discussed in the Physical Interface section.

2. READY

This signal indicates that the selected drive is ready to read, write, or seek. When this line is false, WRITE, READ and SEEK commands should not be initiated by the controller. However, READY will go false whenever a SEEK command is initiated.

READY will be true when the drive is at speed, the track-following servo is locked onto a servo track and no fault condition exists.

3. SECTOR MARK

SECTOR MARK is a 960 nanosecond pulse that occurs at the beginning of each sector. The sector size is selectable by setting mini-dip type switches on the drive. Eight mini-dip switches are provided to select sector length. Each switch is assigned a binary bit position between 16 and 2048, thus, the sector size (time between sector pulses) may be set to any integral multiple of 16 up to 4096 bytes. See Table 8 for switch assignment.

TABLE 8. SECTOR LENGTH SWITCH

Switch	Sector Length Bit
23N-8	bit 16
23N-7	bit 32
23N-6	bit 64
23N-5	bit 128
23N-4	bit 256
23N-3	bit 512
23N-2	bit 1024
23N-1	bit 2048

For example, if the desired format is the 256-byte, soft sector with minimum gap sizes described in Section V, Suggested Data Format, the total length, in bytes, between sector marks would be:

Gap 1	23 bytes
ID Field	9 bytes
Gap 2	11 bytes
Data Field	261 bytes
Total:	304 bytes.

To establish this format, the following switches would be set on:

Switch 23N-4 - Sector Length bit 256
Switch 23N-7 - Sector Length bit 32
Switch 23N-8 - Sector Length bit 16.

For more detailed information on sector formats, see Section V, Suggested Data Formats.

4. HEAD SELECT 1, HEAD SELECT 2

These logic level signals are used to select the appropriate head. These signals are low active and gated by DRIVE SELECT.

TABLE 9. HEAD SELECTION

Head Select 1	Head Select 2	Selected Head
HIGH	HIGH	HEAD ZERO
LOW	HIGH	HEAD ONE
HIGH	LOW	HEAD TWO
LOW	LOW	HEAD ZERO

Head zero is selected by the unused combination so that there will always be a head connected to the read circuitry.

5. WRITE GATE

WRITE GATE enables data to be written on the disc when in the active state. READY must be valid before signaling WRITE GATE. An attempt to write between INDEX and the first SECTOR MARK will result in a DRIVE FAULT because the prerecorded skip defect information is write protected. DRIVE FAULT will be set if any of the following error conditions occur during writing.

TABLE 10. DRIVE FAULT CONDITIONS

1 - WRITE GATE without write current at the head
2 - Write current at the head without WRITE GATE
3 - WRITE GATE without READY
4 - More than one head selected
5 - No transitions during write
6 - WRITE GATE with WRITE PROTECT
7 - Spindle Speed Error
8 - RESET while drive Sequenced Up
9 - Off-Track condition when track following (READY)
10 - Failure to Restore
11 - Software Error (Watch-dog timer time out).

Normally, for full sector write using the hard sector format, WRITE GATE is activated at the leading edge of SECTOR MARK and terminated with the last byte of the postamble or the leading edge of the next SECTOR MARK or INDEX.

6. WRITE CLOCK

Provides clocking and synchronization for WRITE DATA. Preferably WRITE CLOCK is generated by the controller by echoing the REFERENCE CLOCK signal back to the drive through a similar delay path. Thus, it is at the same frequency and with a phase delay similiar to WRITE DATA. However, a switch is provided so that WRITE CLOCK may originate at the DRIVE and be transmitted to the controller. A second switch is provided to select the phasing of WRITE CLOCK that is to be transmitted. The timing of these signals is shown in the Physical Interface section.

7. WRITE DATA

Provides the data to be stored on the track. The required format is NRZ (non-return to zero). READ/REFERENCE CLOCK (received from the drive) is used by the controller to clock WRITE DATA on the positive edge. READ/REFERENCE CLOCK is retransmitted back to the drive as WRITE CLOCK. The negative edge of WRITE CLOCK is used to strobe WRITE DATA into the drive's encoder circuitry. Detailed timing diagrams are shown in the Physical Interface section.

8. READ GATE

This signal must be enabled in a gap area (all 0's recorded) and at least 9 microseconds before the sync byte. READ GATE enables the VFO clock to synchronize with the information from the read head. Raising READ GATE during a data record may cause the VFO to spuriously lock in incorrect phase relationship for correct decoding of recorded information.

Six microseconds after the leading edge of READ GATE the READ CLOCK is selected for the READ/REFERENCE CLOCK signals.

9. READ/REFERENCE CLOCK

Provides clocking and synchronization for reading and writing data. When READ GATE is not active this signal is the REFERENCE CLOCK which is derived from the servo track information.

Six microseconds after the leading edge of READ GATE, READ/REFERENCE CLOCK is switched to the VFO clock which is phase locked to READ DATA. A change in the READ/REFERENCE CLOCK phase will occur when it is switched between the servo and VFO clocks.

10. READ DATA

Data from the drive is in serial bits NRZ (non-return to zero) form and is synchronized with READ/REFERENCE CLOCK after a six microsecond delay from the leading edge of READ GATE. READ DATA may not be valid for the first 9 microseconds after READ GATE is enabled.

D. Physical Interface

All drive signal connections are made via a single 50-pin ribbon cable connector. A second 50-pin connector is available for daisy chaining to another drive or for a terminator for the last drive in the string. Terminator P/N is 200028. Up to four drives may be daisy chained.

A separate connector for DC power is provided. However, if the optional power supply is installed, then its output is connected to this DC power connector and AC power must be supplied to the optional power supply.

1. J1 AND J2 CONNECTORS

J1 and J2 are 50-pin ribbon cable connectors. The pins are numbered 1 through 40. A recommended mating connector is Spectra-Strip 802-050-004 or Scotchflex 3425-0000.

J1 and J2 Connector

Pin	Signal
1	Ground
2	+ DBUS 0
3	+ DBUS 1
4	+ DBUS 2
5	+ DBUS 3
6	+ DBUS 4
7	+ DBUS 5
8	+ DBUS 6
9	+ DBUS 7
10	Ground
11	- READ GATE
12	Ground
13	- RESET
14	Ground
15	- WRITE GATE
16	Ground
17	- RD
18	- WR
19	+ AD 1
20	+ AD 0
21	Ground
22	- DRIVE SELECT 1
23	- DRIVE SELECT 2
24	- DRIVE SELECT 3
25	- DRIVE SELECT 4
26	Ground
27	Ground
28	+ 5 VOLTS DC (TERMINATOR POWER)
29	(RESERVED)
30	- HEAD SELECT 2
31	- HEAD SELECT 1
32	Ground
33	- INDEX
34	Ground
35	- READY
36	Ground
37	- SECTOR MARK
38	Ground
39	+ WRITE DATA
40	- WRITE DATA
41	Ground
42	+ WRITE CLOCK
43	- WRITE CLOCK
44	Ground
45	+ READ/REFERENCE CLOCK
46	- READ/REFERENCE CLOCK
47	Ground
48	+ READ DATA
49	- READ DATA
50	Ground

2. J3 CONNECTOR

This connector is used to supply DC power to the drive when the optional power supply is not used. J3 is a 6-pin AMP MATE-N-LOK Connector, and the recommended mating connector is an AMP 1-480270-0 socket using AMP 60619-1 pins.

J3 CONNECTOR

PIN	VOLTAGE
1	GND
2	-5 VDC
3	+5 VDC
4	GND
5	-12 VDC
6	+24 VDC

3. J4 CONNECTOR

This connector is used to supply AC power to the drive when the optional power supply is used. J4 is a 3-pin connector. The mating connector is Belden 5PH-386 or equivalent.

J4 CONNECTOR

PIN	VOLTAGE
L	AC INPUT (HOT)
E	FRAME GROUND
N	AC RETURN (COMMON)

4. INTERFACE SIGNALS

Following is an electrical description of each interface signal.

a. +DBUS 0-7

A high active 8-bit wide bus used to transfer commands and status between drive and controller. These lines connect directly to an 8304B (or 8286) bus transceiver as shown in Figure 2.

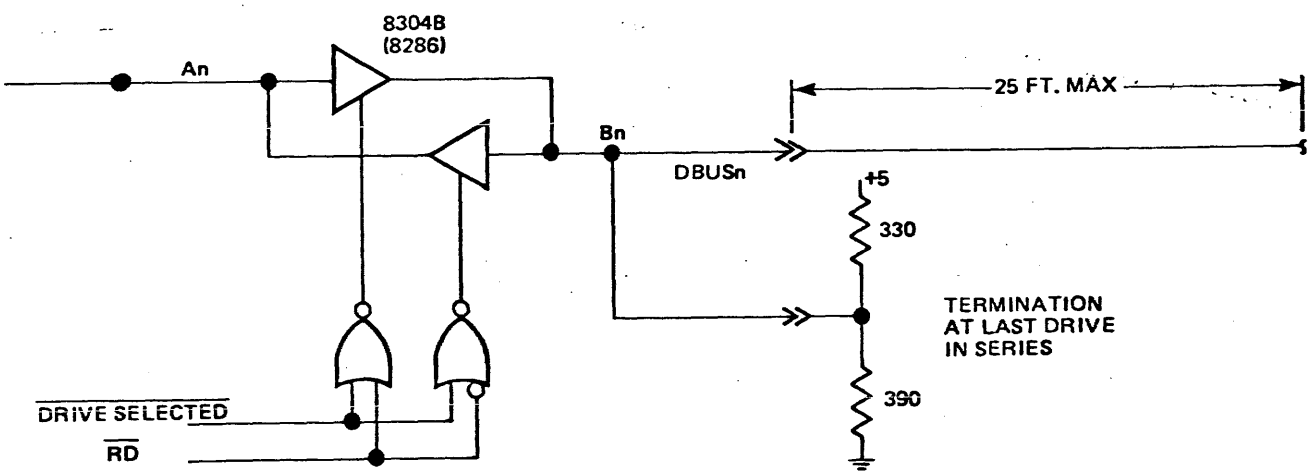


Figure 2. DBUS Transceiver

TABLE 11. DBUS DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{OL}	Output Low Level		0.5	V	I_{OL} = 32 MA
V_{OH}	Output High Level	2.4		V	I_{OH} = -5 MA
I_{OFF}	Output Off Current		-0.2	mA	V_{OFF} = 0.45 V
			+0.2	mA	V_{OFF} = 5.25 V
V_{IL}	Input Low Level		0.9	V	
V_{IH}	Input High Level	2.0		V	

If long cables are used, these lines should be terminated at each end.

b. + AD0-1

A high active 2-bit wide address bus, whose function is to select one of three registers in which data is stored or from which it is read. These lines connect directly to a 74LS244 Schmitt-Triggered Receiver enabled by DRIVE SELECTED as shown in Figure 3.

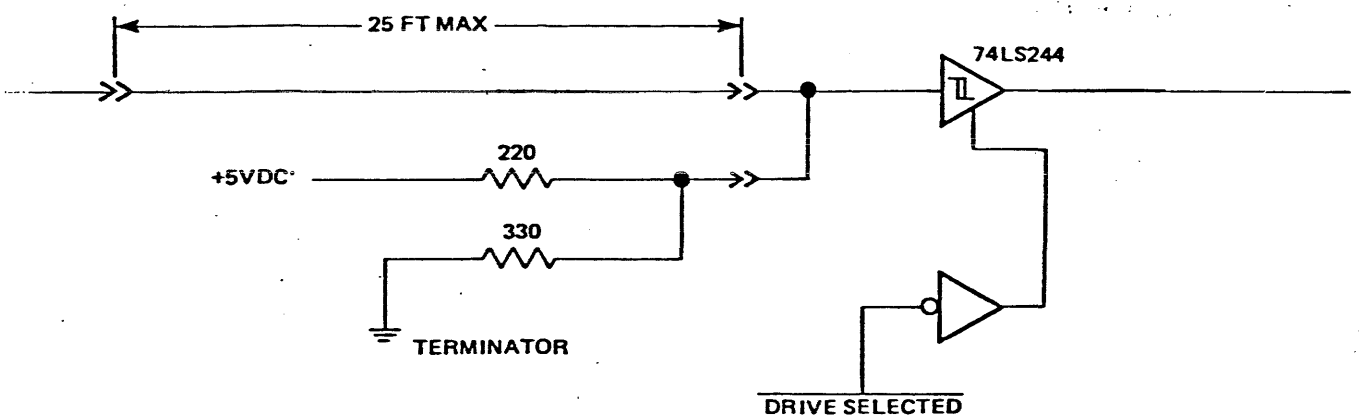


Figure 3. Single Line Receiver Gated By Drive Select

TABLE 12. SINGLE LINE RECEIVER GATED BY DRIVE SELECT
DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Input High Level	2		V	
V_{IL}	Input Low Level		0.8	V	
I_{IH}	High Level Input Current		0.02	mA	V_I = 2.7V
I_{IL}	Low Level Input Current		-0.2	mA	V_I = 0.4V

If long cables are used, these lines should be terminated at the drive end with PRIAM terminator P/N 200028.

c. - RD

This low active signal is used to gate the contents of the selected register (decode of AD1,AD0) onto the DBUS. This line is connected to a 74LS244 as shown in Figure 3. Also, the DC characteristics are listed in Table 12.

Long cables should be terminated at the drive end. PRIAM provides an optional terminator (Figure 5).

d. - WR

This low active signal is used to gate the contents of the DBUS into the selected register. This line is connected to a 74LS244 as shown in Figure 3 and its DC characteristics are listed in Table 12.

Long cables should be terminated at the drive end. PRIAM provides an optional terminator (Figure 3).

e. - RESET

This low active signal resets the drive logic. If the drive is Sequenced Down when RESET occurs it will remain sequenced down. If the drive is Sequenced Up, it will remain up and the carriage will RESTORE to Cylinder Zero. This line is connected to a 74LS244 as shown in Figure 3 and its DC characteristics are listed in Table 12.

Long cables should be terminated at the drive (Figure 3).

f. - DRIVE SELECT 1-4

These low active signals enable drive response. No reading, writing, register selection, or command response will occur unless the drive is selected. These single-ended receiver lines are shown in Figure 4. Long cables should be terminated (Figure 4).

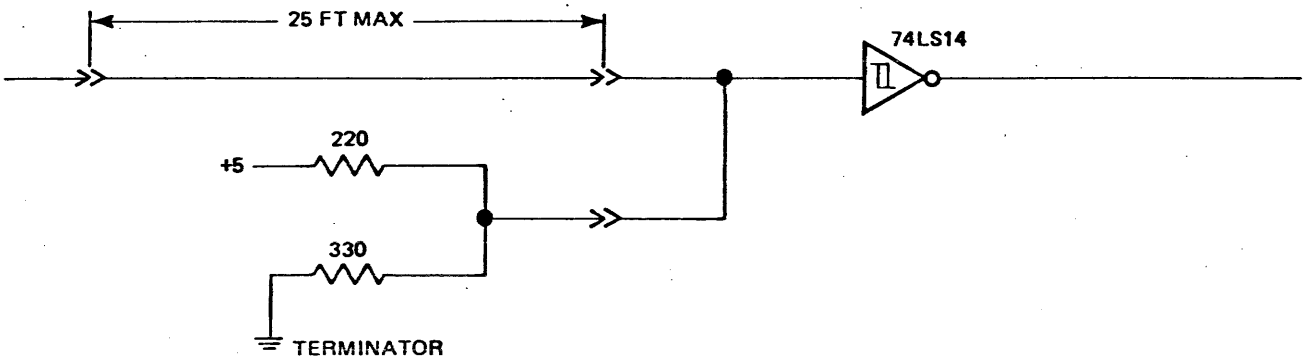


Figure 4. Single End Line Receiver

TABLE 13. SINGLE LINE RECEIVER DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{T+}	Positive-going threshold	1.4	1.9	V	
V_{T-}	Negative-going threshold	0.5	1	V	
I_{IH}	High level input current		.020	mA	V_I = 2.7V
I_{IL}	Low level input current		-0.400	mA	V_I = 0.4V

Long cable connections should be terminated.

g. -HEAD SELECT 1-2

These low active signals are used to select the desired head for reading or writing. The head selection decoding is shown in Table 9. These lines are connected to a 74LS244 as shown in Figure 3 and its DC characteristics are listed in Table 12.

Long cable connections should be terminated (Figure 3).

h. -READY

This low active signal from the drive indicates that it is up to speed and ready to read, write or seek. It is driven by a 75462 open collector driver as shown in Figure 5.

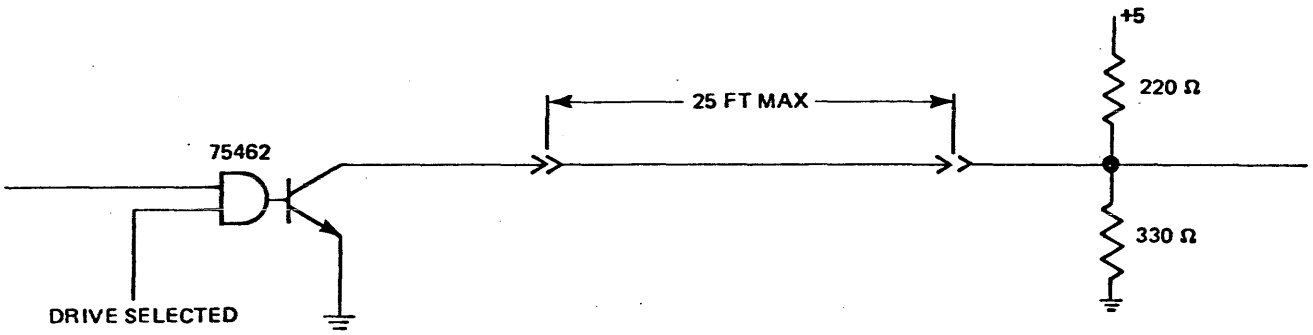


Figure 5. Single Line Driver

TABLE 14. SINGLE LINE DRIVER DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
I_{OH}	High level output current		0.10	mA	
I_{OL}	Low level output current	300		mA	
V_{OL}	Low level output voltage		0.8	V	I_{OL} = 300mA

This line must be terminated at the controller.

i. -INDEX

This low active signal indicates the beginning of a track. The INDEX pulse is 6.8 microseconds wide. It is driven by a 75462 open collector driver as shown in Figure 5 and has the DC characteristics listed in Table 14. This line must be terminated at the controller.

j. -SECTOR MARK

This low active signal indicates the beginning of a sector. The SECTOR MARK pulse is 960 nanoseconds wide. It is driven by a 75462 open collector driver as shown in Figure 5 and has the DC characteristics listed in Table 14. This line must be terminated at the controller.

k. -WRITE GATE

This low active signal enables the writing of data by the selected head. This signal is received by a 74LS244 as shown in Figure 3 and its DC characteristics are listed in Table 12. Long cable connections should be terminated at the drive (Figure 3).

l. -READ GATE

This low active signal initiates synchronization of the drives phase lock loop for data separation. READ GATE must be enabled during a gap. This signal is received by a 74LS244 as shown in Figure 3 and its DC characteristics are listed in Table 12. Long cable connections should be terminated at the drive (Figure 3).

m. +, - WRITE DATA

WRITE DATA is an NRZ serial data signal synchronous with WRITE CLOCK. It is received by a RS422 type differential line receiver section as shown in Figure 6.

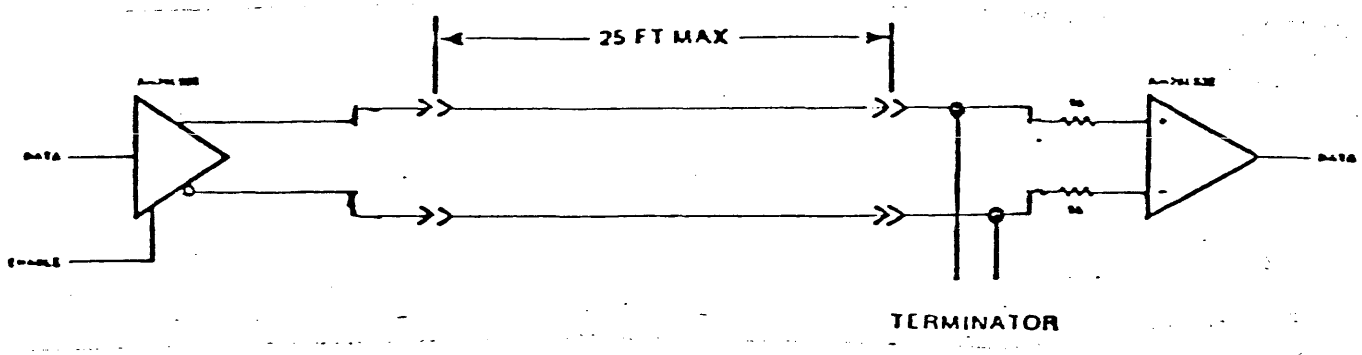


Figure 6. Differential Line Drivers & Receivers

The DC characteristics are listed in Table 15. The last drive in a string should be terminated with PRIAM terminator P/N 200028.

TABLE 15. DIFFERENTIAL LINE RECEIVER DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{TH}	Differential input high-threshold		0.2	V	
V_{ICR}	Common-mode input range	+15 to -15		V	
$I_{I(REC)}$	Receiver input current		2.3	mA	

n. +, - WRITE CLOCK

This signal is switch selectable and may be either a square wave signal from the controller which is phase locked to the WRITE DATA. Or, if the switch is set in the other position, WRITE CLOCK is a square wave signal from the drive to the controller to provide clocking and synchronization for WRITE DATA. The controller should be designed so that WRITE DATA is stable at the drives connector during the positive transition of WRITE CLOCK. If long cables are used, cable delays must be considered.

The timing for these signals is shown in Figure 11. It must be stable from 120 nanoseconds before WRITE GATE and remain stable during WRITE GATE. The nominal period of WRITE CLOCK is 120 nanoseconds. It is received by a RS422 type differential line receiver as shown in Table 15 and Figure 6. These lines should be terminated.

TABLE 16. DIFFERENTIAL LINE DRIVER DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{OH}	High level output voltage	2.5		V	I_{OH} = -20mA
V_{OL}	Low level output voltage		0.32	V	I_{OL} = 20mA
I_{OZ}	Off-state (non-selected) output current		±0.02	mA	
I_{OH}	High-level output current		-20	mA	
I_{OL}	Low-level output current		20	mA	
I_{OS}	Short circuit output current	-30	-150	mA	

o. +, - READ/REFERENCE CLOCK

This square wave signal provides clocking and synchronization for reading and writing data. It is derived from either the servo clock or the VFO synchronized to the READ DATA signal. The nominal period is 120 nanoseconds. It is driven by a RS442 type differential line driver as shown in Figure 6 and its DC characteristics are listed in Table 16.

p. +, - READ DATA

This serial NRZ signal is used to transmit data from the drive to the controller. This output is valid 9 micro- seconds after READ GATE is enabled. It is driven by a RS422 type differential line driver as shown in Figure 6 and its DC characteristics are listed in Table 16.

In the following section, timing requirements are discussed. Register load timing is shown in Figure 7 and the AC characteristics are listed in Table 17.

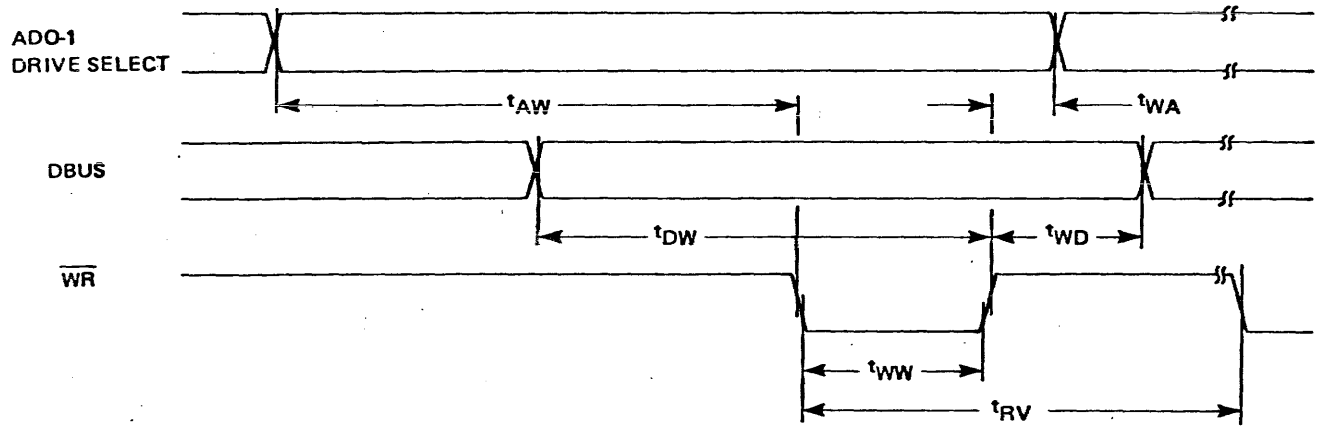


Figure 7. Register Load Timing

TABLE 17. REGISTER LOAD AC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{AW}	Address stable before WR	60		ns
t_{WA}	Address hold time for WR	30		ns
t_{WW}	WR pulse width	100		ns
t_{DW}	Data set up time for WR	60		ns
t_{WD}	Data hold time for WR	30		ns
t_{RV}	Recovery time between WR	200		ns

Register read timing is shown in Figure 8 and the AC characteristics are listed in Table 18.

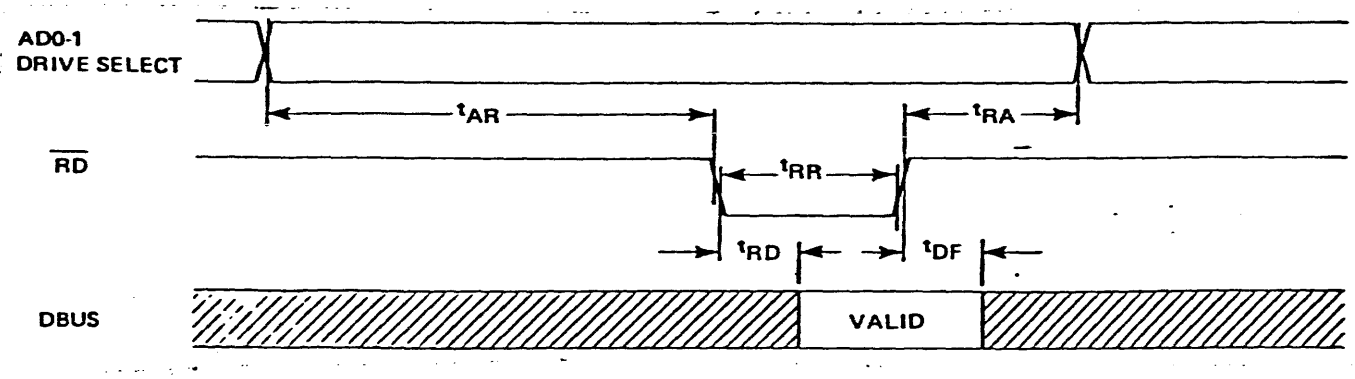


Figure 8. Register Read Timing

TABLE 18. REGISTER READ AC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{AR}	Address stable before RD	60		ns
t_{RA}	Address hold time for RD	30		ns
t_{RR}	RD pulse width	100		ns
t_{RD}	Data delay from RD		60	ns
t_{RD}	RD to data floating	10	40	ns

Reset timing is shown in Figure 9 and the AC characteristics are listed in Table 19.

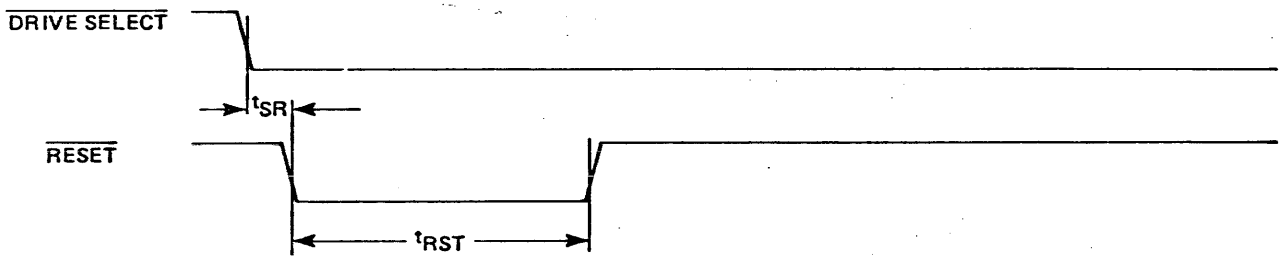


Figure 9. Reset Pulse Width Timing

TABLE 19. RESET AC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{RST}	Reset pulse width	100		ns
t_{RST}	DRIVE SELECT TO RESET	0		ns

INDEX and SECTOR MARK timing are shown in Figure 10 and their AC characteristics are listed in Table 20.

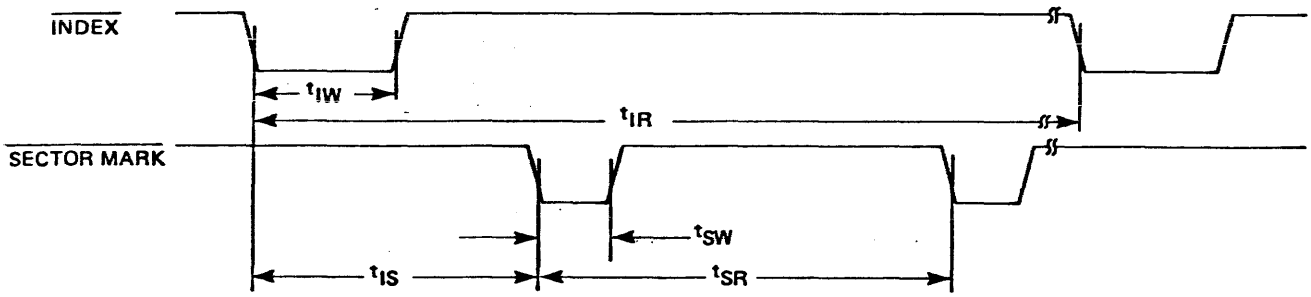


Figure 10. INDEX and SECTOR MARK Timing

TABLE 20. INDEX AND SECTOR MARK AC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{IW}	INDEX pulse width	1.73	1.92	2.11	us
t_{IR}	INDEX period	17.4	19.35	21.3	ms
t_{SW}	SECTOR MARK pulse width	816	960	1100	ns
t_{IS}	INDEX to first SECTOR MARK	26.1	30.7	35.3	us
t_{SR}*	Sector width (depends on selected size)				
	for 304 bytes (256 data)	263	292	321	us
	for 1072 bytes (1024 data)	926	1029	1132	us

* t_{SR} = (Sector size (in bytes) X 960 ns) $\pm$ 10%

WRITE DATA and WRITE CLOCK timing relationship is shown in Figure 11 and their AC characteristics are listed in Table 21.

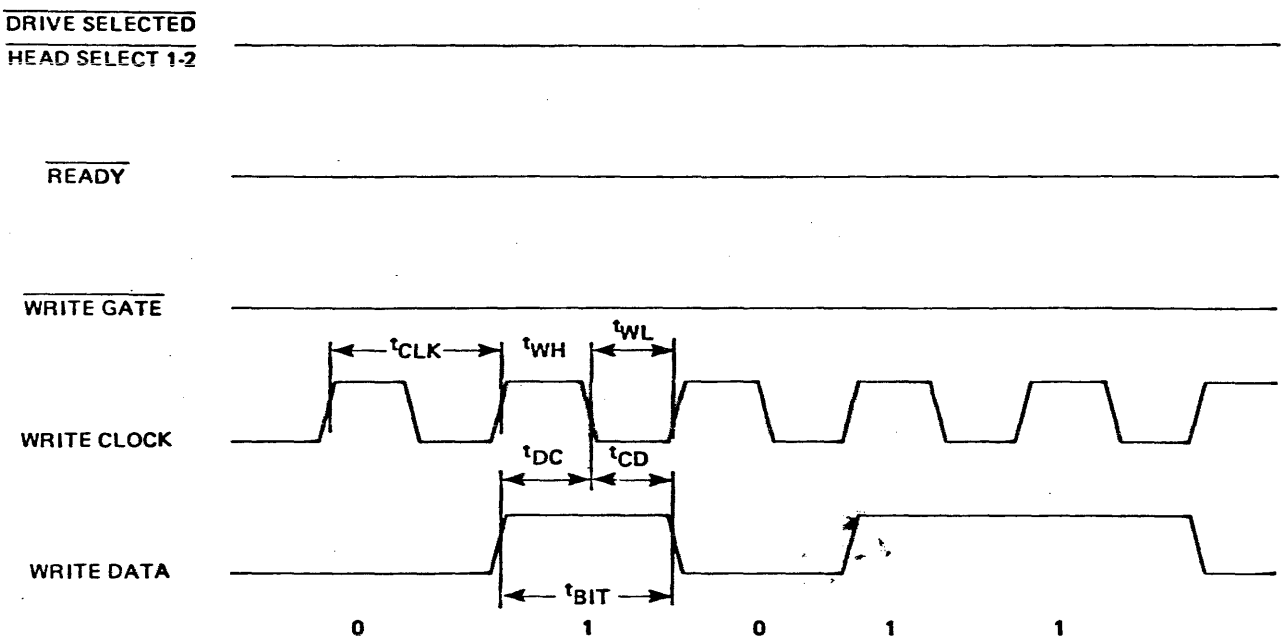


Figure 11. WRITE DATA and WRITE CLOCK Timing

TABLE 21. WRITE DATA AND WRITE CLOCK AC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{CLK}	WRITE CLOCK period	102	120	138	ns
t_{WH}	WRITE CLOCK high pulse width	51	60	69	ns
t_{WL}	WRITE CLOCK low pulse width	51	60	69	ns
t_{BIT}	WRITE DATA bit period	102	120	138	ns
t_{DC}	WRITE DATA setup time	20	60		ns
t_{CD}	WRITE DATA hold time	20	60		ns

READ DATA and READ CLOCK timing relationship is shown in Figure 12 and their AC characteristics are listed in Table 22.

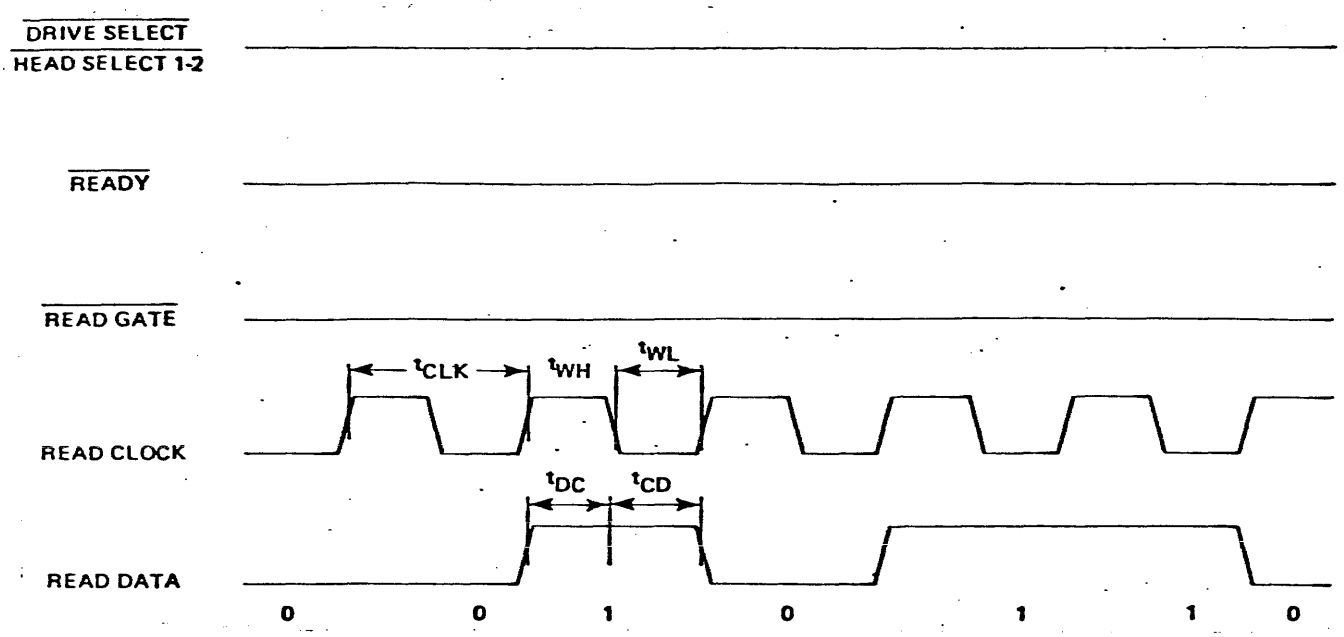


Figure 12. READ DATA and READ CLOCK Timing

TABLE 22. READ DATA AND READ CLOCK AC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{CLK}	READ CLOCK period	102	120	138	ns
t_{WH}	READ CLOCK high pulse width	51	60	69	ns
t_{WL}	READ CLOCK low pulse width	51	60	69	ns
t_{BIT}	READ DATA bit period	102	120	138	ns
t_{DC}	READ DATA setup time	40	60		ns
t_{CD}	READ DATA hold time	40	60		ns

Figure 13 shows timing requirements for writing full sectors (ID and data fields) and also for writing sector data fields only.

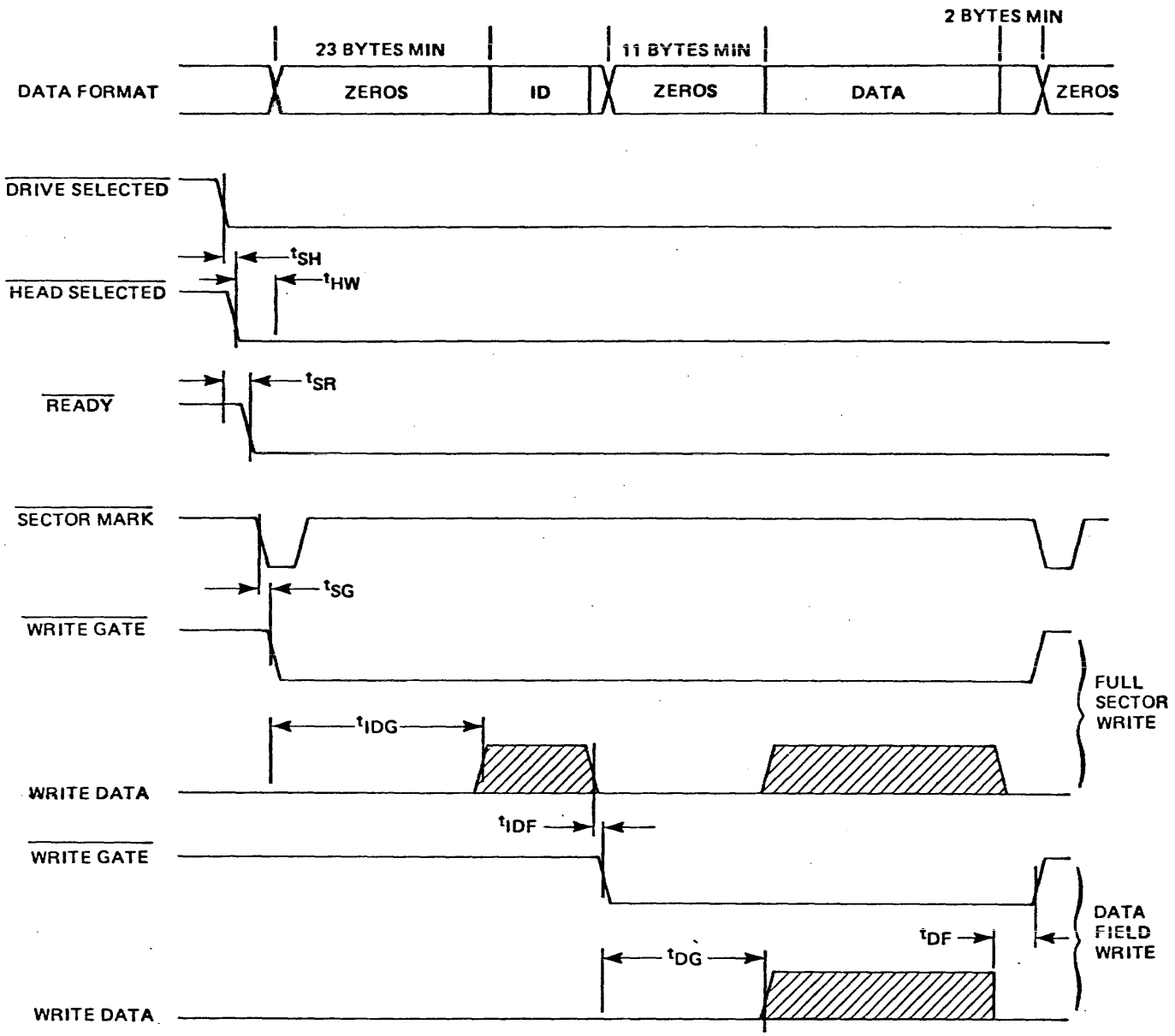


Figure 13. Record Writing Timing

TABLE 23. RECORD WRITING CONTROL AC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{SH}	DRIVE SELECTED to HEAD SELECTED	20			us
t_{SR}	DRIVE SELECTED to READY	100			ns
t_{SG}	SECTOR MARK TO WRITE GATE	-1	0	1	us
t_{IDG}	ID gap timing (23 bytes min)	18.8	22.1		us
t_{IDF}	ID fill (2 Byte min)	1.63	1.92		us
t_{DG}	Data gap (no Write to read transitions (11 byte min)	8.98	10.56		us
t_{DF}	Data fill (2 Byte min)	1.63	1.92		us
t_{HW}	Head Select to WRITE GATE	100			ns

Figure 14 shows timing requirements for reading ID and data fields and for reading data fields only.

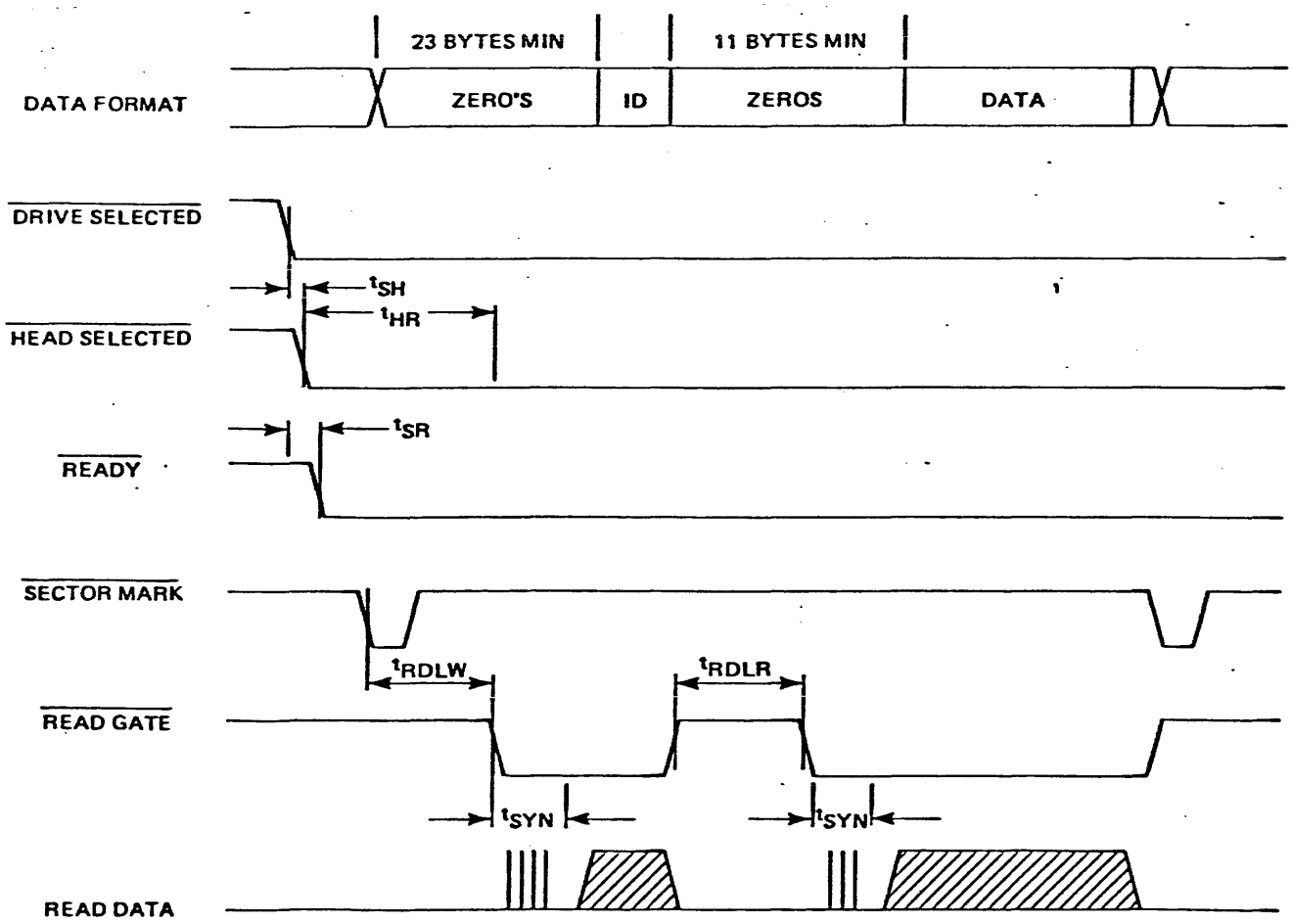


Figure 14. Record Reading Timing

TABLE 24. RECORD READING CONTROL AC CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{SH}	DRIVE SELECTED to HEAD SELECTED	20		us
t_{SR}	DRIVE SELECTED to READY	100		ns
t_{RDLW}	READ GATE DELAY for gaps allowing WRITE to READ transitions	13		us
t_{RDLR}	READ GATE DELAY for gaps limited to READ to READ or READ to WRITE transitions	1.9		us
t_{SYN}	READ PLO SYNCHRONIZATION (Data not valid for this period)		9	us
t_{HR}	HEAD SELECT to READ GATE	25		us

The combined operations are shown in Figure 15.

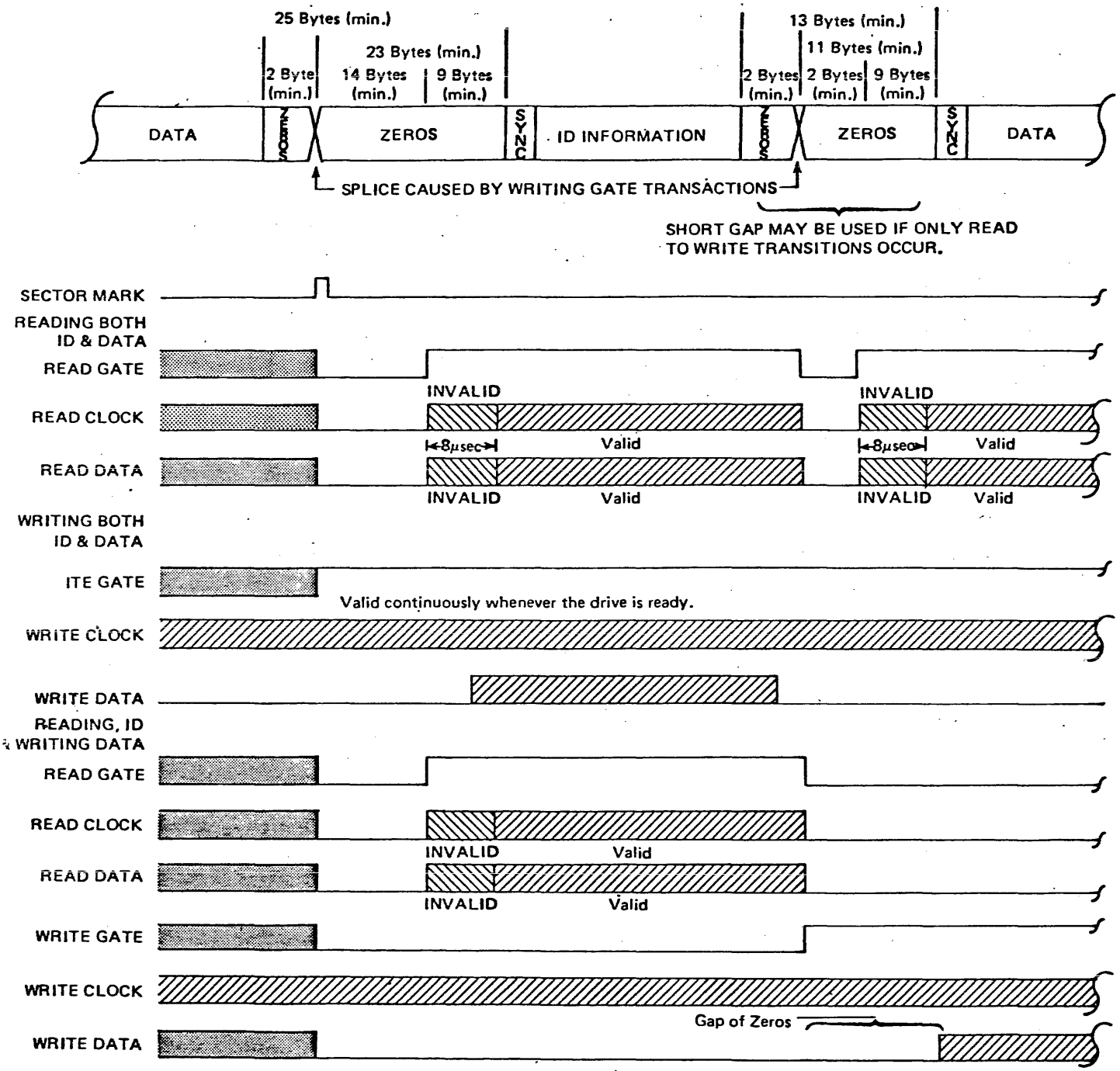


Figure 15. READ & WRITE Transitions During Gaps

V. SUGGESTED DATA FORMATS

A. Format Definitions

Two formats are suggested, one similar to the soft sectored format used on flexible discs, the other similar to the flexible disc hard sectored format.

1. Soft Sector Format

This format has the sector ID field and the data field separated by a gap. This allows reading of the ID field to verify position, and subsequently switching to write mode during the gap and writing a new data field.

2. Hard Sector Format

In this format the ID may be omitted or imbedded in the data field. If it is imbedded, it must be rewritten each time the data field is rewritten.

These two suggested formatting approaches are described in detail in the balance of this section.

B. Soft Sector Format

The soft sector format is shown in Figure 16 and is described below.

Each track starts with an INDEX pulse, which corresponds to a certain area of the servo track. Also, the servo track provides rotational position information for the generation of SECTOR MARK pulses. A sector pulse precedes each record and successive records are separated by gaps within which the sector pulses occur.

1. PRE-RECORD GAP (GAP 1)

The Pre-Record Gap, or Gap 1, appears at the beginning of every record. It consists of 23 bytes of zeros. The length of Gap 1 never varies. The first Gap 1, after INDEX, is followed by the Skip Defect Record. All other Gap 1's, after SECTOR MARKS, are followed by ID records.

2. SKIP DEFECT RECORD

The Skip Defect Record consists of 11 bytes: a Data Sync using the hexadecimal pattern FB, the physical address of the first defect using two bytes, the physical address of the second defect using two bytes, the physical address of the third defect using two bytes, a check sum across the previous six bytes using two bytes, and fill characters of zeros using two bytes. The checksum is the complement of the sixteen bit sum of the three defect addresses.

3. ID FIELD

This Identification Field uses nine bytes: an ID sync of one byte, the head address and high order cylinder address of one byte, the low order cylinder address of one byte, the sector number of one byte, a sector length and flag bytes, two CRC (cyclic redundancy check) bytes, and two bytes of zeros for filling. The cylinder and head address, along with the sector number, verify that the drive has addressed the correct track and sector.

4. ID GAP (GAP 2)

The ID Gap, or Gap 2, separates each successive Identification Field from its Data Field. It contains 11 bytes of zeros.

5. DATA FIELD

Following Gap 2, the Data Field may consist of any number of bytes but lengths of 133, 261, 517, or 1029 bytes are common for 128, 256, 512 or 1024 data lengths. The first byte is a data sync, while the last four bytes consist of two bytes of CRC and two bytes of zeros for filling.

6. PRE-INDEX GAP (GAP 3)

The Pre-Index Gap, or Gap 3, is used only once on a track. It appears at the end of the last data field and persists until INDEX. This gap contains zeros.

Table 25 lists a few of the various available soft sector track formats.

TABLE 25. SOFT SECTOR FORMAT INFORMATION

Data Field Length (bytes)	Sector Length	Sectors Per Track	Gap 1 (bytes)	Gap 2 (bytes)	Gap 3 (bytes)	Data Per Track (bytes)	Data Capacity (bytes)	Percent Utilization (bytes)
128	176	114	23	11	60	14,592	24,558,336	72.4%
256	304	66	23	11	60	16,896	28,435,968	83.8%
512	560	35	23	11	524	17,920	30,159,360	88.8%
1024	1072	18	23	11	828	18,432	31,021,056	91.4%

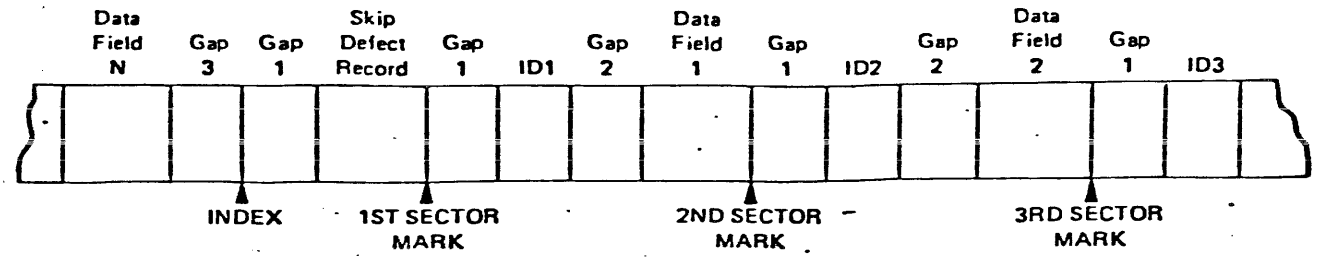


Figure 16. Soft Sector Format

Index: Derived from servo track

Gap 1:	Zeros	23 Bytes
Skip Defect Record:	Data sync "FB" HEX	1 Byte
	1st defect address	2 Bytes
	2nd defect address	2 Bytes
	3rd defect address	2 Bytes
	Check sum	2 Bytes
	Fill characters - zeros	2 Bytes
Sector Mark:	Derived from INDEX and servo clock	
Gap 1:	Zeros	23 Bytes
ID Field:	ID sync	1 Byte
	Head and high order cylinder address	1 Byte
	Low order cylinder address	1 Byte
	Sector address	1 Byte
	Sector length & flag	1 Byte
	CRC	2 Bytes
	Fill characters - zeros	2 Bytes
Gap 2:	Zeros	11 Bytes
Data Field	Data sync	1 Byte
	Data	n Bytes
	CRC	2 Bytes
	Fill characters - zeros	2 Bytes
Gap 3:	Zeros	Size depends on data field size

C. Hard Sector Format

The hard sector format is shown in Figure 17 and is described below.

Each track starts with an INDEX pulse, which corresponds to a certain area of the servo track. Also, the servo provides rotational position information for the generation of SECTOR MARK pulses. A sector pulse precedes each record and successive records are separated by gaps within which sector pulses occur.

1. PRE-DEFECT RECORD GAP (GAP 1)

The Pre-Defect Record Gap, or Gap 1, appears at the beginning of the skip defect record. It consists of 23 bytes containing zeros. The length of Gap 1 never varies. Gap 1 occurs after INDEX and is followed by the Skip Defect Record.

2. SKIP DEFECT RECORD

The Skip Defect Record consists of 11 bytes: a Data Sync using the hexadecimal pattern FB, the physical address of the first defect using two bytes, the physical address of the second defect using two bytes, the physical address of the third defect using two bytes, a check sum across the previous six bytes using two bytes, and fill characters of zeros using two bytes.

3. PRE-DATA RECORD GAP (GAP A)

The Pre-Data Record Gap, or Gap A, appears at the beginning of every data record. It consist of 27 bytes of zeros. The minimum size is 23 bytes but a sector must be an integral multiple of 16 bytes. Thus, 27 bytes is appropriate for the selected data record overhead.

4. DATA FIELD

Following Gap A is the Data Field, which may consist of any number of bytes but lengths of 133, 261, 517, or 1029 bytes are common for 128, 256, 512 or 1024 data lengths. The first byte is a data sync, while the last four bytes consist of two bytes of CRC and two bytes of zeros for filling.

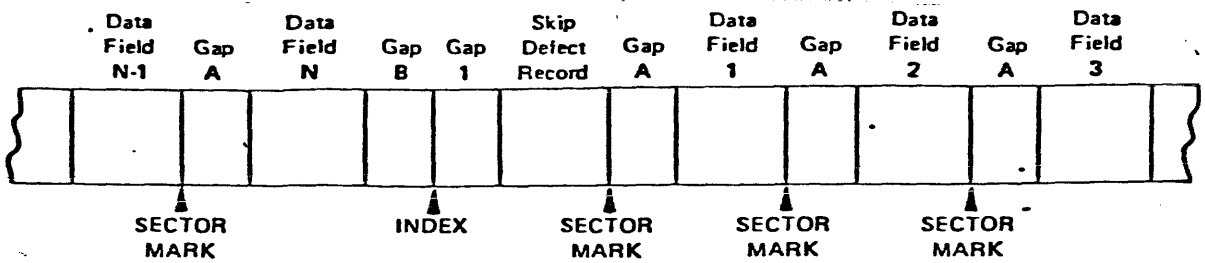
5. PRE-INDEX GAP (GAP B)

The Pre-Index Gap, or Gap B, is used only once on a track. It appears at the end of the last data field and persists until INDEX. This gap consists of zeros.

Table 26 lists a few of the various available hard sector track formats.

TABLE 26. HARD SECTOR FORMAT INFORMATION

Data Field Length (bytes)	Sector Length	Sectors Per Track	Gap A	Gap B	Data Per Track (bytes)	Data Capacity (bytes)	Percent Utilization
128	160	125	27	124	16,000	26,928,000	79.4%
256	288	69	27	252	17,664	29,728,512	87.6%
512	544	36	27	540	18,432	30,021,056	91.4%
1024	1056	19	27	60	19,456	32,744,448	96.5%



Index:	Derived from Servo Track	
Gap 1:	Zeros	23 bytes
Skip Defect Record:	Date Sync, "FB" HEX	1 byte
	1st defect address	2 bytes
	2nd defect address	2 bytes
	3rd defect address	2 bytes
	Check sum	2 bytes
	Fill characters - zeros	2 bytes
Sector Mark:	Derived from INDEX and servo clock	
Gap A:	Zeros	27 bytes
Data Field:	Data Sync	1 byte
	Data	n bytes
	CRC	2 bytes
	Fill characters - zeros	2 bytes
Gap B:	Zeros	Size depends on data field size

Figure 17. Hard Sector Format

05/13/80
1748A

ERRATA SHEET

DISKOS 3350
Disc Drive Product Specification

dated May 15, 1980

Page 7, Table 3.

Switch 16R-6; is: Write Clock Phase Select
Should be: Write Protect Head 0

Switch 16R-7:
is: Write Clock Transmit Enable
Should be: Write Protect Head 1

Add as note to Table 3.

Switch 16R-1 through 16R-4 enables Drive address when in the "ON" position.

Switch 16R-5 enables writing in the Skip Defect Record when in the "OFF" position.

Switch 16R-6 through 16R-8 enables Write Protect for the selected head when in the "OFF" position.

Switch 23N 1 through 8 enables designated sector length when in the "ON" position.

TO: D. Reiser DATE: July 10, 1980

FROM: A. Ebright

SUBJECT: SMART Interface First Release

The first release of the SMART Interface Code (~~1/2~~ 8/21) does not contain the following features:

~~1. HIR is not implemented.~~
2. Defect Mapping is not implemented.
3. The Verify Command is not implemented.
4. There are no micro-diagnostics.

Table I describes the sector format currently implemented.

Logical Size	Physical Size	Sector/Track	Switch Setting
128	192	104	5,6
256	320	~~63~~ 62	4,6
512	576	34	3,6
1024	1088	18	2,6

TABLE I. Sector Format Summary