PRO-LOG
CORPORATION

STD 7000

7601
Input/Output Port Card
USER'S MANUAL

7601 TTL OUTPUT PORT CARD USER'S MANUAL

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7000 STD BUS

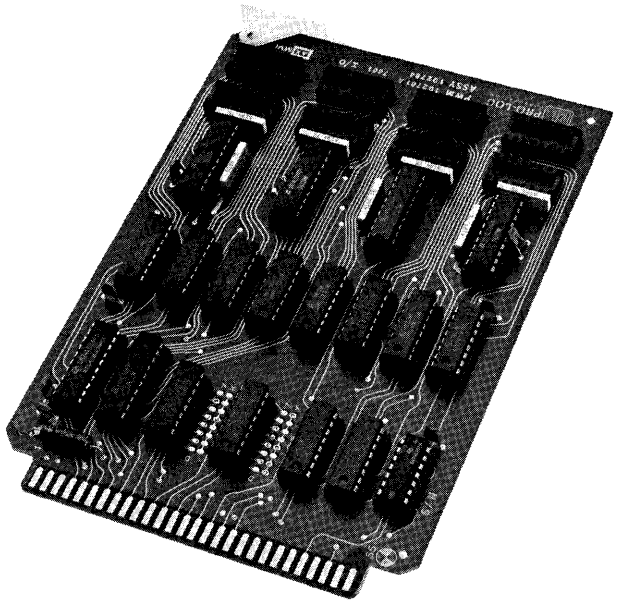
7601 INPUT/OUTPUT PORT CARD

TTL INPUT/OUTPUT PORT CARD

This card provides four 8-bit gated input ports (32 input lines) and four 8-bit latched output port (32 output lines).

Input port lines and output port lines are accessed at 16-pin DIP sockets on the card. I/O lines are TTL compatible with an input rating of 4 low-power Schottky TTL loads and an output drive rating of 20 low-power Schottky TTL loads (5 TTL loads). A reset line is available.

The 7601 decodes eight address lines with provision for expansion and memory mapping. An on-card jumper system allows users to establish the four consecutive I/O port pair addresses occupied by the 7601.



FEATURES

- **User selected port address (256 port field)**
- **Input rating: 4 LSTTL loads**
- **Output rating: 20 LSTTL loads (5 TTL loads)**
- **Provision for expansion and memory mapping**
- **Input buffers have 200 MV of hysteresis for additional noise margin**
- **Input lines include 4.7K pullup resistors**
- **All IC's socketed**
- **Single +5V operation**

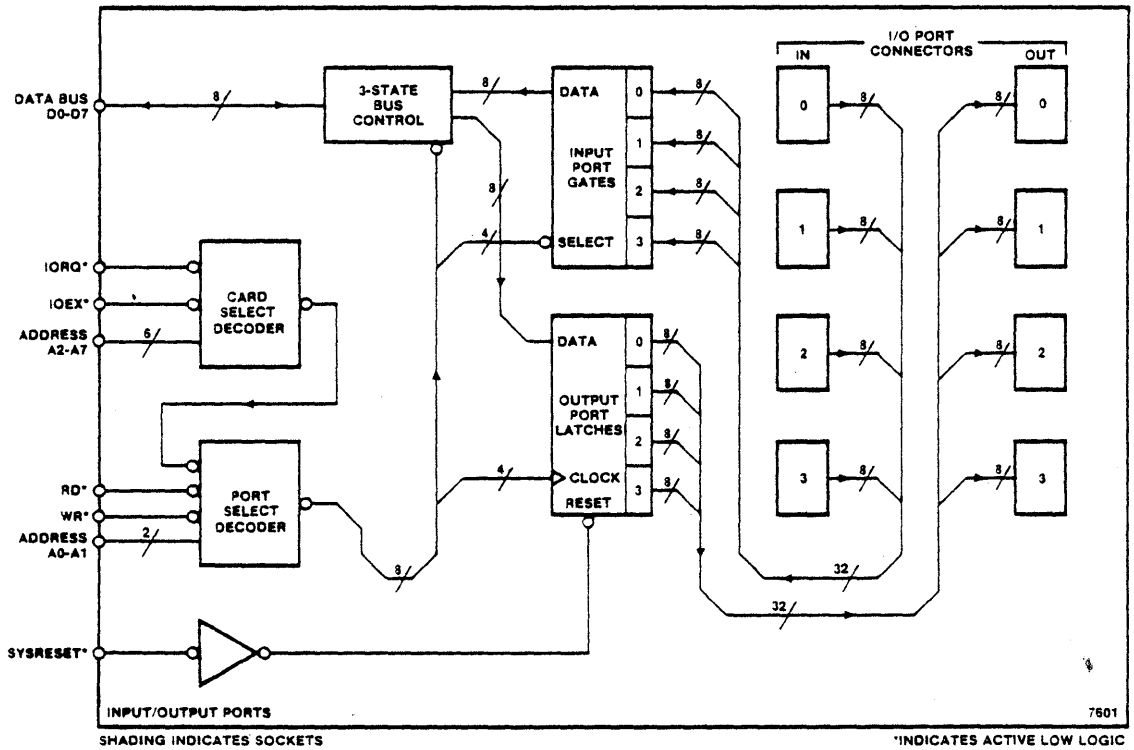


FIGURE 1

2. FUNCTIONAL DESCRIPTION

The 7601 provides 32 TTL output lines and 32 TTL input lines. All signal lines are alternated with ground lines. These signal lines can be up to 10 feet (3.05m) long with proper electrical considerations. All port lines are addressable in eight bit bytes.

OUTPUT

When writing to an eight bit output port the data bus data is latched in the output port. The output data will remain latched in that state until it is written to with new data or the SYSRESET* signal clears the port.

RESET

The SYSRESET* line clears all four output ports to zero simultaneously. The input ports are unaffected. On system power-up the SYSRESET* signal clears the output ports.

INPUT

When reading from an eight bit input port, the state of the input lines at the time of the read is transferred to the data bus.

GENERAL PURPOSE INTERFACE

The 7601 is useful as a general purpose TTL interface card. If flat cable or twisted pair discrete wire cable assemblies are used, the ground-signal-ground of the I/O connectors minimizes crosstalk between inter-system signal lines in electrically noisy environments.

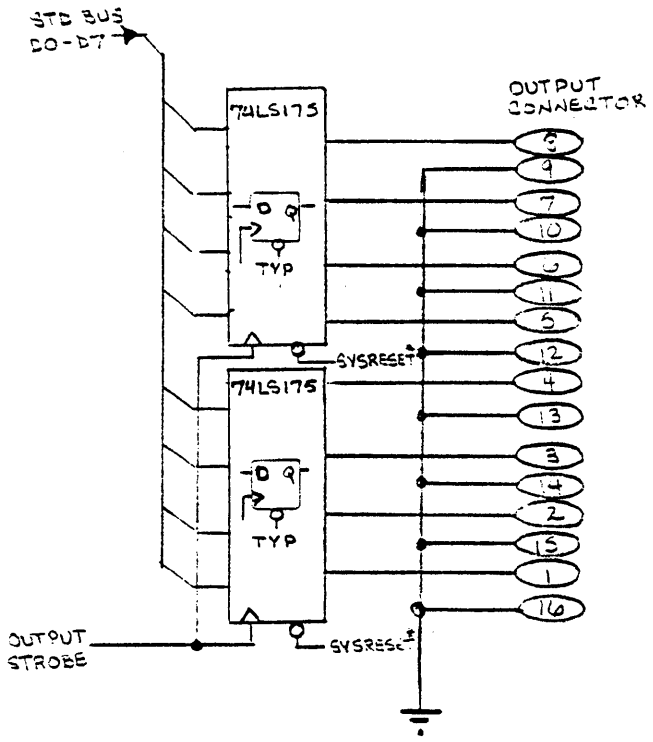


FIGURE 2A - TYPICAL OUTPUT PORT CIRCUIT

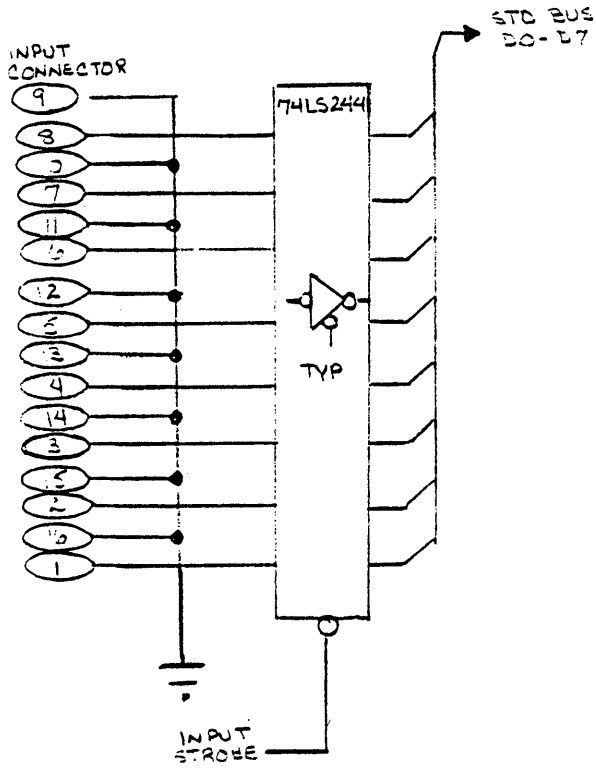


FIGURE 2B - TYPICAL INPUT PORT CIRCUIT

3. CARD ADDRESS MAPPING

The 7601 card is selected by a decoded combination of address lines A2 through A7. The user chooses the card address combination by connecting one jumper wire each from SX and SY to pad matrices adjacent to U3 and U4. (See Assembly Diagram)

The 7601 is mapped at Port 00 to 03 hexadecimal. To map the 7601 anywhere in the hexadecimal address range of 00-FF change the decoder outputs connected to SX and SY.

PORT ADDRESSES

Address lines A0 and A1 select one of four sequential port addresses. One input port and one output port reside at each address. The RD* and WR* control inputs differentiate between input gating or output latch functions.

4. ADDRESS DECODER OPERATION

Refer to the schematic, Document #102783

The 7601 uses two cascaded 74LS42 decoders (U3, U4) to decode address lines A2-A7. These decoders are enabled only when IORQ* and IOEXP* are active. Address lines A0, A1 and the WR* signal are used to gate the select strobes (which control the output ports) from U6. Address lines A0, A1 and the RD* signal are used to gate the select strobes (which control the input ports) from U5.

CHANGING THE 7601 PORT ADDRESS

Refer to the assembly diagram, Document #102784

Locate decoders U3 and U4 (74LS42) adjacent to the STD BUS edge connector. Each decoder device has a dual gow of pads which form decoder output select matrices. Make one (and only one) connection to each of the matrices adjacent to U3 and U4.

The decoder jumper pads numbered as shown in the card address selection figure are adjacent to the decoder chips on the 7601. Also shown are the jumpers (at X0 and Y0) which produce hexadecimal port addresses 00, 01, 02, and 03, the selections made when the card is shipped.

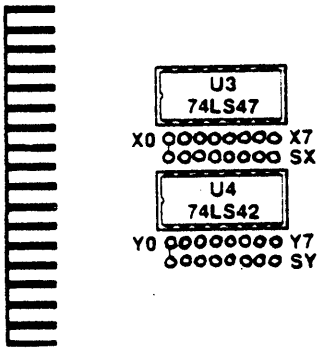


FIGURE 3 - CARD ADDRESS SELECTION

The I/O address mapping and jumper selection table for four addresses per card shows where to place jumper straps to obtain any four sequential port addresses in the hexadecimal range 00-FF. Using the lower of the 2-digit hexadecimal addresses desired, find the most significant hexadecimal address digit along the vertical axis, and the least significant hex digit on the horizontal axis. For example, port addresses 50, 51, 52 and 53 are obtained by connecting jumpers at X2 and Y4.

The only restriction that applies in address selection for the 7601 is that the lower of the four port addresses (00 as shipped) must occur only at every fourth possible address; for example, the sequence 01, 02, 03 and 04 is not allowed by the decoder.

The pad matrices adjacent to U3 and U4 are on 0.10 inch (0.25cm) centers. The jumper wires may be conveniently replaced by wirewrap post if frequent address selection changes are anticipated.

MOST SIGNIFICANT HEX ADDRESS	LEAST SIGNIFICANT HEX ADDRESS																JUMPER SELECTION X & Y
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	X0 Y0				X0 Y1				X0 Y2				X0 Y3				X AND Y
1	X0 Y4				X0 Y5				X0 Y6				X0 Y7				
2	X1 Y0				X1 Y1				X1 Y2				X1 Y3				
3	X1 Y4				X1 Y5				X1 Y6				X1 Y7				
4	X2 Y0				X2 Y1				X2 Y2				X2 Y3				
5	X2 Y4				X2 Y5				X2 Y6				X2 Y7				
6	X3 Y0				X3 Y1				X3 Y2				X3 Y3				
7	X3 Y4				X3 Y5				X3 Y6				X3 Y7				
8	X4 Y0				X4 Y1				X4 Y2				X4 Y3				
9	X4 Y4				X4 Y5				X4 Y6				X4 Y7				
A	X5 Y0				X5 Y1				X5 Y2				X5 Y3				
B	X5 Y4				X5 Y5				X5 Y6				X5 Y7				
C	X6 Y0				X6 Y1				X6 Y2				X6 Y3				
D	X6 Y4				X6 Y5				X6 Y6				X6 Y7				
E	X7 Y0				X7 Y1				X7 Y2				X7 Y3				
F	X7 Y4				X7 Y5				X7 Y6				X7 Y7				

FIGURE 4 - I/O Address Mapping And Jumper Selection Table For 4 Addresses Per Card

5. 7601 CARD ENVIRONMENTAL SPECIFICATIONS

RECOMMENDED OPERATING LIMITS				ABSOLUTE NON-OPERATING LIMITS		
PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
Free Air Temperature	0	25	55	-40	75	°C
Humidity ①	5		95	0	95	%RH

① Non-condensing

6. ELECTRICAL SPECIFICATIONS

7601 GENERAL PURPOSE TTL I/O CARD ELECTRICAL TEST SPECIFICATION

MNEM.	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NON-OPERATING LIMITS		
		MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
Vcc	Supply voltage	4.75	5.00	5.25	0.0	7.00	Volt
T_A	Free air temp.	0	25	55	-40	75	C

USER WORST CASE ELECTRICAL CHARACTERISTICS OVER RECOMMENDED TEST LIMITS

FOR AN INPUT PORT

MNEM	PARAMETER	MIN	TYP	MAX	UNIT
V_{IH}	High Level Input Voltage	2.0			volt
V_{IL}	Low Level Input Voltage			0.7	volt
	Hysteresis $(V_{T+} - V_{T-})$	0.2	0.4		volt
for input current each port line represents 4 LSTTL loads*					

FOR AN OUTPUT PORT

MNEM	PARAMETER	MIN	TYP	MAX	UNIT
V_{OH}	High Level Output Voltage (2)	2.7	3.5		volt
V_{OL}	Low level Output Voltage (1)		3.5	0.5	volt
Each output can drive 20 LSTTL loads*					

STD BUS ELECTRICAL CHARACTERISTICS OVER RECOMMENDED TEST LIMITS

MNEM	PARAMETER	MIN	TYP	MAX	UNIT
I_{CC}	Supply Current		300	475	mA
	STD BUS Input Load	See Figure 6			
	STD BUS Output Drive	See Figure 6			

(1) V_{CC} = 4.5V I_{OL} = 8mA

(2) V_{CC} = 4.5V I_{OH} = 400µA

* 1 LSTTL load = 0.4mA

7. MECHANICAL

- Meets all STD BUS general mechanical specifications
- May require one additional card slot width (0.5 inch) for ribbon cable access to port sockets.
- Connectors use low profile 16-pin DIP plugs with heavy duty pins. T and B Ansley catalog No. 609-M165H or equivalent

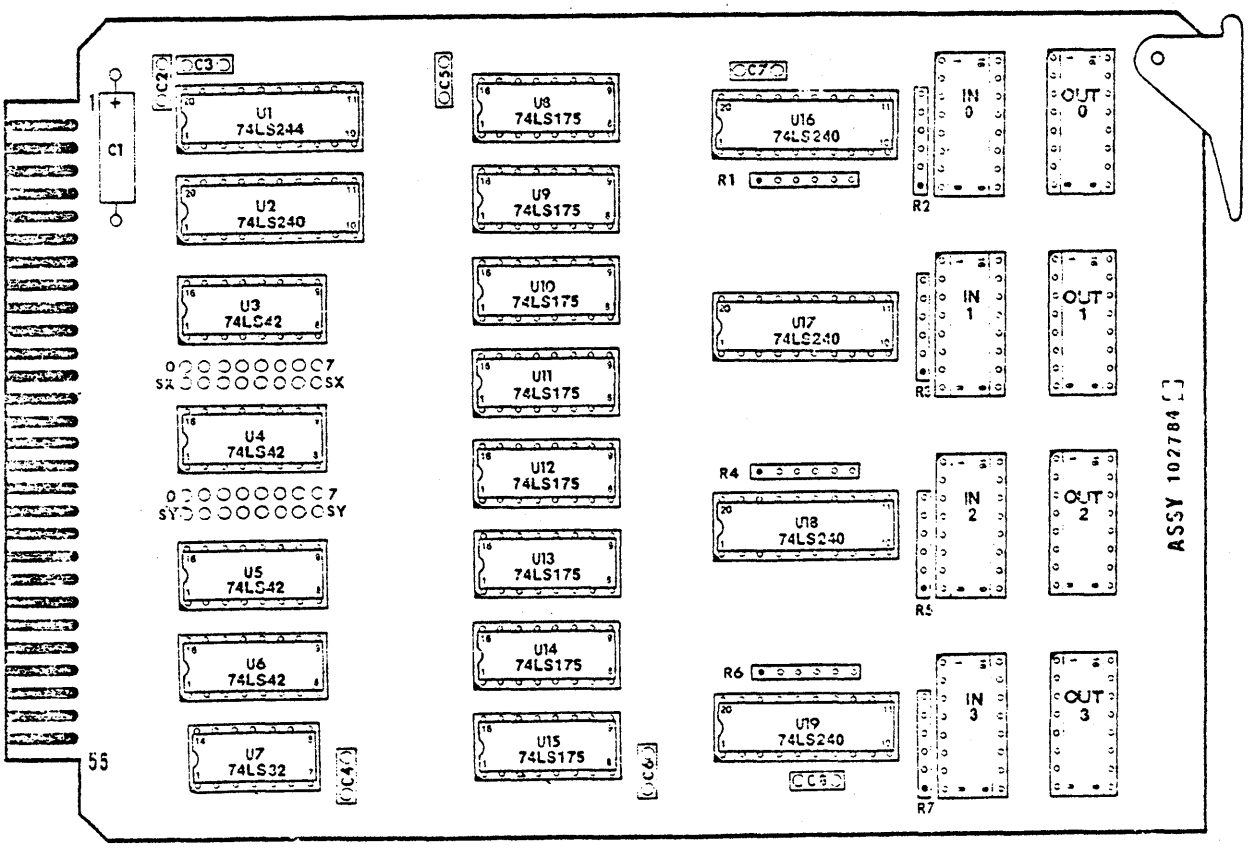


FIGURE 5 - 7601 ASSEMBLY

STD/7601 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE) INPUT (LOADING)**	MNEMONIC		PIN NUMBER	OUTPUT (DRIVE) INPUT (LOADING) **	MNEMONIC	
-5 VOLTS	VCC		2	1		VCC	-5 VOLTS
GROUND	GND		4	3		GND	GROUND
-5V			6	5			-5V
D7	1		8	7		1	D3
D6	1		10	9		1	D2
D5	1		12	11		1	D1
D4	1		14	13		1	D0
A15			16	15		1	A7
A14			18	17		1	A6
A13			20	19		1	A5
A12			22	21		1	A4
A11			24	23		1	A3
A10			26	25		1	A2
A9			28	27		2	A1
A8			30	29		2	A0
RD*	1		32	31		1	WR*
MEMRQ*			34	33		1	IORQ*
MEMEX*			36	35		1	IOEXP*
MCSYNC*			38	37			REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*			44	43			INTAK*
NMIRQ*			46	45			WAITRQ*
PBRESET*			48	47	1		SYSRESET*
CNTRL*			50	49			CLOCK*
PC1	IN		52	51	OUT		PC0
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX -V

*Designates Active Low Level Logic

** Designates LSTTL Loads

FIGURE 6 - **Edge Connector Pin List**

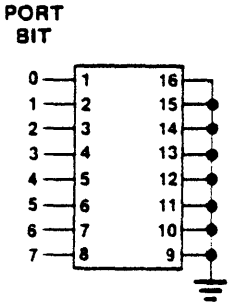


FIGURE 7 - **Input or Output Port Socket**

8. 7601 OPERATING SUBROUTINE MODULES

This section provides flow diagrams and subroutines to operate your 7601 card. These may be used intact, or used as models to construct subroutines for a specific application.

The subroutines are written in 8080-family assembly code and will execute on 8080. 8085, and Z80 processors. The memory addresses selected are compatible with Pro-Log's 7801 (8085A) and 7803 (Z80) processor cards. The 7601 port addresses used are the address jumper selections made when the 7601 is shipped.

To use these subroutines in systems other than those described above, the memory and/or I/O port addresses may require change for compatibility.

The flow diagrams presented can be easily translated into the assembly code used by any microprocessor since they show the steps required to achieve 7601 operation without reference to a particular microprocessor.

The (Check Bits) subroutine will compare the present input port status with the port status from the last time that the port was read.

To use the routine the HL pointer must point to a place in memory where port status is stored. Also the port must be read into the Accumulator before calling the routine.

Upon return from the routine the location that the HL pointer was previously set will contain new port status. Plus the next four locations will contain change status.

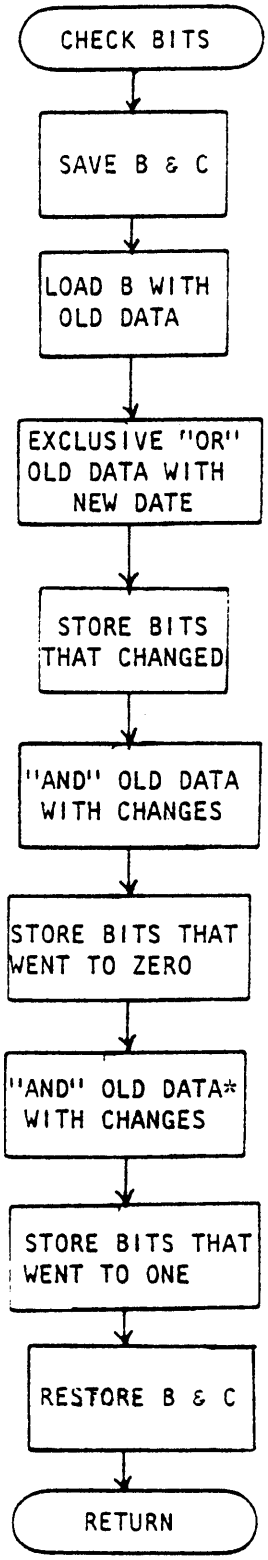
Uses Registers A, H and L

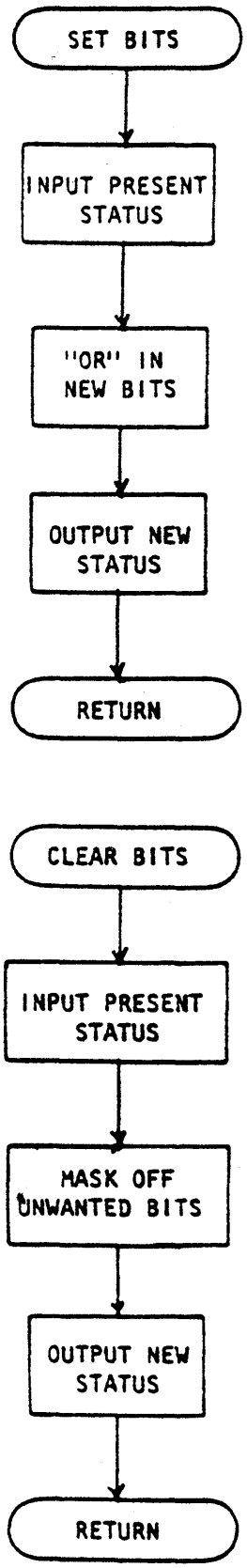
M	XX New Data	← Location HL was set to
M + 1	XX Old Data	
M + 2	XX Changes	
M + 3	XX Bits to Zero	
M + 4	XX Bits to One	

Memory after Return

The (Set Bit) routine can set a bit or bits on an output port. To use the routine, load the accumulator with the bits that should be changed and set the HL pointer to a place in memory where the port status is stored.

The (Clear Bit) routine can clear a bit or bits on an output port. To use the routine, load the accumulator with the bits that should be changed and set the HL pointer to a place in memory where the port status is stored.


CHECK BITS
SAVE B & C
LOAD B WITH OLD DATA
EXCLUSIVE "OR" OLD DATA WITH NEW DATE
STORE BITS THAT CHANGED
"AND" OLD DATA WITH CHANGES
STORE BITS THAT WENT TO ZERO
"AND" OLD DATA* WITH CHANGES
STORE BITS THAT WENT TO ONE
RESTORE B & C
RETURN


SET BITS
INPUT PRESENT STATUS
"OR" IN NEW BITS
OUTPUT NEW STATUS
RETURN
CLEAR BITS
INPUT PRESENT STATUS
MASK OFF UNWANTED BITS
OUTPUT NEW STATUS
RETURN

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PROGRAM ASSEMBLY FORM

TITLE 7601 DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
	0			LDPI	HL	← Set Pointer
	1			—	XX	
	2			—	XX	
	3			IPA		← Input New Data
	4			—	XX	
	5	C5	(Check Bits)	PSP	BC	← Save Contence of Regs B and C
	6	46		LDB	M(HL)	← Put OLD Data in B
	7	77		STAN	(HL)	← Store New Data
	8	23		ICP	(HL)	← Store OLD Data in Next Location
	9	70		STBN	(HL)	
	A	AB		XRA	B	← OLD ⊕ NEW = CHANGES
	B	23		ICP	HL	← Store CHANGES in Next Location
	C	77		STAN	(HL)	
	D	4F		LDC	A	← Put Changes in C
	E	78		LDA	B	← Put OLD DATA IN A
	F	A1		ANA	C	← OLD • CHANGES = Bits to Zero
	0	23		ICP	HL	← Store Bits to Zero in Next Location
	1	77		STAN	(HL)	
	2	78		LDA	B	← Compliment OLD DATA
	3	2F		CMA		
	4	A1		ANA	C	← $\overline{OLD}$ • CHANGES = Bits to ONE
	5	23		ICP	HL	← Store Bits to ONE in Next Location
	6	77		STAN	(HL)	
	7	C1		PLP	BC	← Restore Contence of Reg B and C
	8	C9		RTS	UN	← Return from Subroutine
	9					USES REGS A and Bits in HL
	A					
	B					
	C					
	D					
	E					
	F					

```
00001111  OLD
⊕ 01011010  NEW
  01010101  CHANGES
```

```
00001111  OLD
• 01011010  CHANGES
  00001010  Bits to Zero
```

```
11110000  OLD
• 01011010  CHANGES
  01010000  Bits to ONE
```

RAM MEMORY AFTER Return (uses 5 locations)	XX NEW DATA	M
	XX OLD DATA	M+1
	XX CHANGES	M+2
	XX Bits to Zero	M+3
	XX Bits to ONE	M+4

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PRO-LOG CORPORATION

PROGRAM ASSEMBLY FORM

TITLE 7601 DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
	0			LDAI		← LOAD A WITH BIT(S) TO BE SET
	1			-	XX	
	2			LDPI	HL	← SET MEMORY POINTER
	3			-	XX	
	4			-	XX	
	5	47	(SET BITS)	LDB	A	← SAVE BITS IN B
	6	7E		LDA	M(HL)	← GET PRESENT PORT STATUS
	7	B0		ORA	B	← OR IN NEW BITS
	8	77		STAN	(HL)	← STORE NEW PORT STATUS
	9	D3		OPA		← SEND NEW DATA TO PORT
	A	XX		-	XX	
	B	C9		RTS		
	C					
	D					
	E					
	F					
	0			LDAI		← LOAD A WITH BIT(S) TO BE CLEARED
	1			-	XX	
	2			LDPI		← SET MEMORY POINTER
	3			-	XX	
	4			-	XX	
	5	2F	(CLEAR BITS)	CMA		← COMPLEMENT BITS AND PUT IN B
	6	47		LDB	A	
	7	7E		LDA	M(HL)	← GET PRESENT PORT STATUS
	8	A0		ANA	B	← MASK OF BITS
	9	77		STAN	(HL)	← STORE NEW PORT STATUS
	A	D3		OPA		← SEND NEW DATA TO PORT
	B	XX		-	XX	
	C	C9		RTS		
	D					
	E					
	F					

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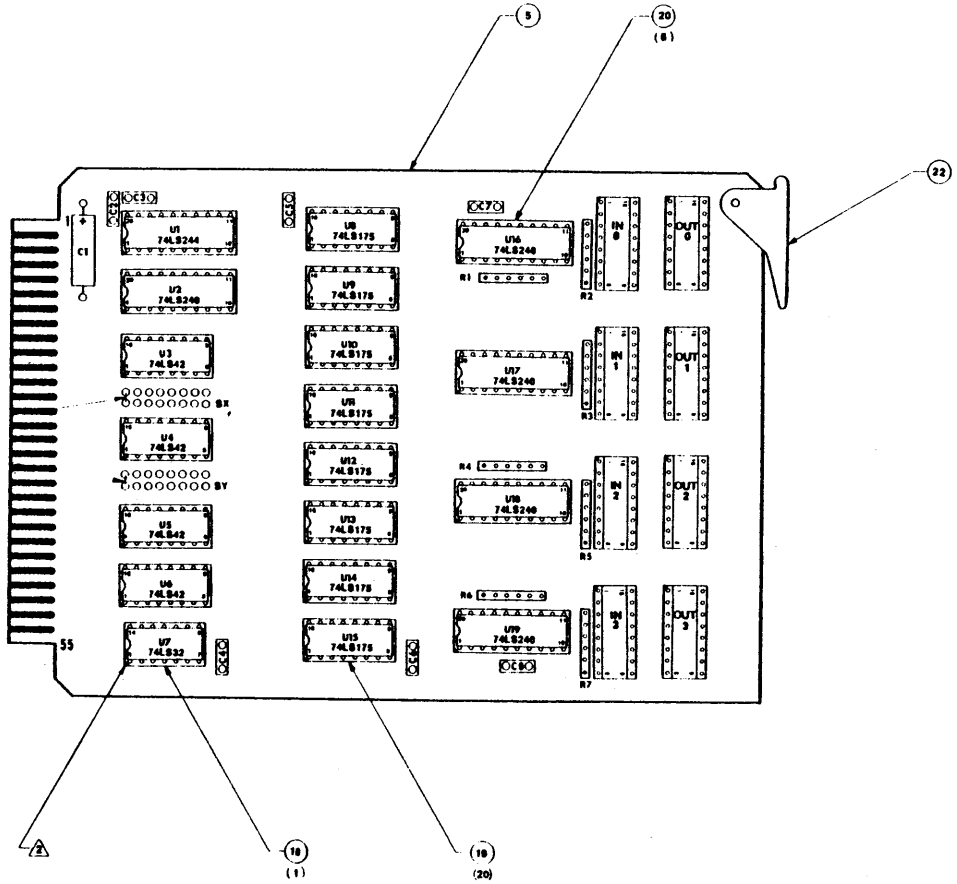
REVISIONS				
ZONE/DIV REV	DOC REV	DESCRIPTION	DATE	APPR
	A	[illegible]	[illegible]	[illegible]



△ MATED TO SOCKET
△2 INDICATES PIN NO 1 OF SOCKETS (TYP).
1. FOR ASSY PROCEDURES SEE AS1004.
NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC NO.102783
PARTS LIST NO.102785

REFERENCE ONLY

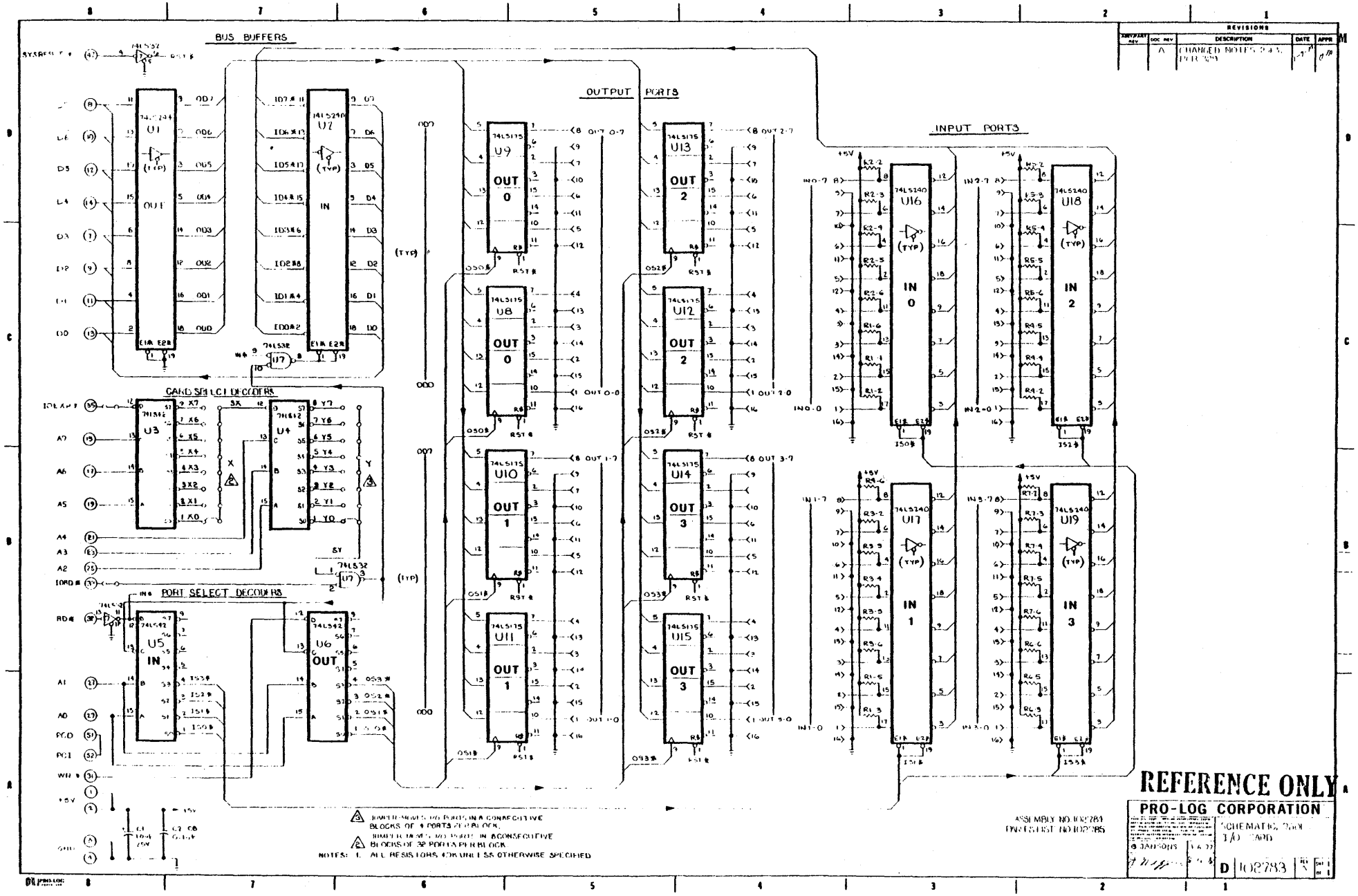
ITEM	DESCRIPTION	REF DESIGNATION
10	47K NETWORK	R1 - R7
9		
8	0.1 uF 50V	C2 - C8
7	1.0 uF 25V	C1

PRO-LOG CORPORATION

ASSEMBLY, 7400 I/O CARD

C. A. CLARK 6/12/78

D 102784


BUS BUFFERS
OUTPUT PORTS
INPUT PORTS
CARD SELECT DECODERS
PORT SELECT DECODERS
REVISIONS
DESCRIPTION
DATE
APPR
CHANGED NOTES 2 & 5.
PRO-LOG CORPORATION
SCHEMATIC, 2001
I/O CARD
D
102783
REFERENCE ONLY
ASSEMBLY NO. 102781
PWB ARTWORK NO. 102785
NOTES: 1. ALL RESISTORS 470Ω UNLESS OTHERWISE SPECIFIED

USER'S MANUAL

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