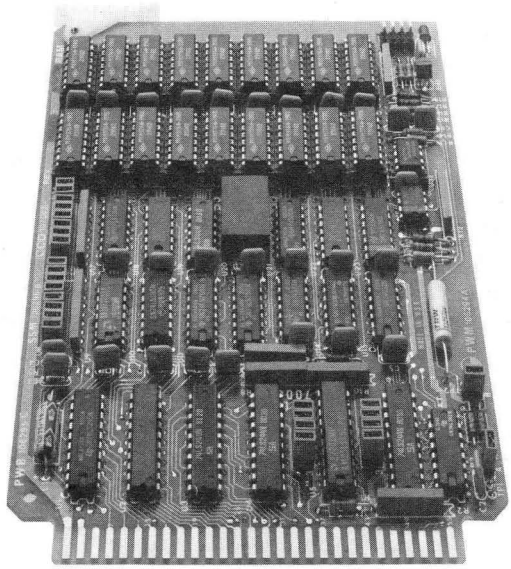
DATA SHEET

STD BUS 128K BYTE DYNAMIC RAM CARD 7707

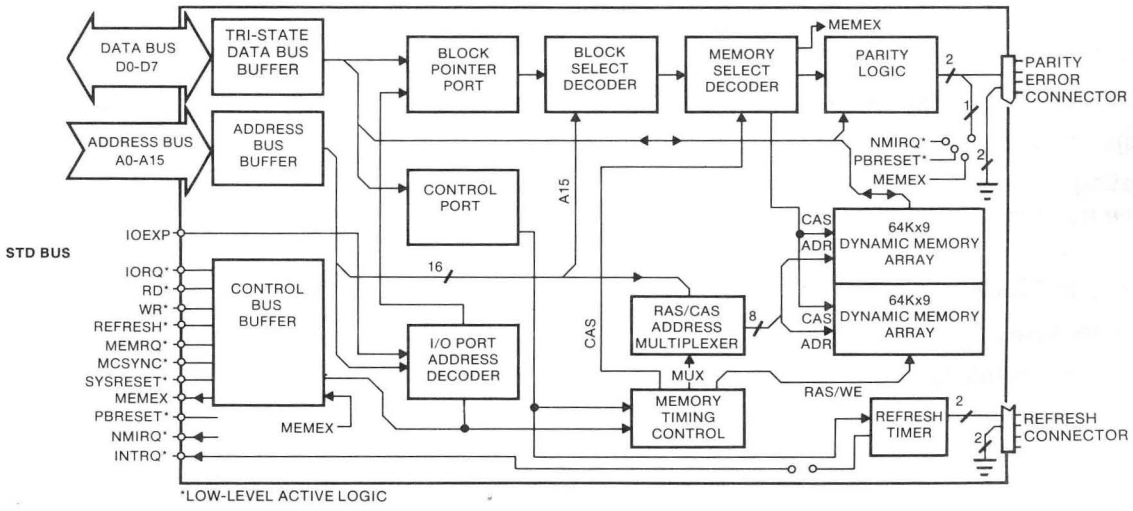
The 7707 is a dynamic RAM card providing the latest in high-density semiconductor memory for the STD BUS. It greatly reduces the number of cards needed to implement large memory schemes, thereby reducing cost. The 7707 also improves the efficiency of disk-based systems and features error detection. The memory management logic of the 7707 provides for the efficient use of 8-bit microprocessor memory while maintaining compatability with the 16-bit 8088.

The 7707 is suitable for a number of memory management techniques; for example, the allocation of banks of memory to individual time-sharing operators or the interleaved running of unrelated programs. The 7707 is designed with sockets for dynamic RAM chips and is available in two options; a full 128K byte card and a depopulated 64K byte version. The 7707 is compatible with Z80A, 8085A, 6809, 8088 and others.



FEATURES

- Fully STD BUS buffered
- Compatible with 8085A (at 6.25 MHz), Z80A (at 4 MHz), 6809 (at 1 MHz), 8088 (at 5 MHz) and others
- 128K byte capacity (64K byte option)
- Software controlled memory banking in 32K byte blocks
- Refresh via offboard DMA, software, or Z80A REFRESH* signal
- Onboard 555 timer provides refresh timing
- Single +5V operation
- Error detection provided by parity bit on each byte
- Uses industry standard 64K bit dynamic RAM
- Control of MEMEX signal by onboard port
- Allows expansion to 384K bytes with 8-bit processors
- Allows expansion to 896K bytes with the 8088
- Two-year warranty



FUNCTIONAL CAPABILITY

The 7707 comprises seven functional elements: bus buffers; memory support, management, and access logic; dynamic memory array; refresh timer; and parity logic.

STD BUS data, address and control lines used with the dynamic memory card are buffered through the bus buffers. The memory support logic provides for control of the MEMEX and Refresh signal lines during dynamic memory operation. The memory array is banked into four 32K-byte blocks and decodes a 20-bit address, allowing direct addressing of up to 896K bytes. An onboard I/O port controls the four most significant address bits when operating with an 8-bit microprocessor. When operated with the 16-bit 8088 microprocessor, the 7707 demultiplexes the four most significant address bits from the data bus. The memory access logic controls this as well as the signal timing required by dynamic memory devices.

Memory parity checking is implemented by the ninth bit which is stored at each data location, and automatically checks for errors during read operations. If a parity error is detected, the card can interrupt, reset, or return to a control program. Dynamic RAM chips are refreshed automatically through the Refresh signal from a Z80, software instruction, or external DMA. Additionally, if multiple 7707 cards in the system have the same I/O address, all the cards are refreshed simultaneously.

ELECTRICAL SPECIFICATIONS

- VCC = 5V ± 0.25V
- ICC = TYP MAX

	TYP	MAX
64K	540 to 1100 mA (standby) 810 to 1500 mA (operating) 730 to 1380 mA (refresh)	
128K	570 to 1150 mA (standby) 1110 to 1550 mA (operating) 950 to 1700 mA (refresh)	

ENVIRONMENTAL SPECIFICATIONS

- Free-air operating temperature: 0° to +55°C
- Storage temperature: -40° to +75°C
- Operating humidity: 5% to 95% noncondensing relative humidity

ORDERING INFORMATION

7707-64: 64K bytes dynamic RAM

7707-128: 128K bytes dynamic RAM

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER		MNEMONIC
PE*		8	2	1		GROUND
PEINT*		40	4	3		GROUND
TCLR*	2		6	5		GROUND
TIC*		40	8	7		GROUND

*Low-level active logic

Connector J1 Parity Error/Refresh

PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC	PIN NUMBER	OUTPUT (LSTTL DRIVE)	INPUT (LSTTL LOADS)	MNEMONIC
+5V	IN		2	1		IN	+5V
GROUND	IN		4	3		IN	GROUND
-5V			6	5			-5V
D7	1	55	8	7	55	1	D3
D6	1	55	10	9	55	1	D2
D5	1	55	12	11	55	1	D1
D4	1	55	14	13	55	1	D0
A15	1		16	15		1	A7
A14	1		18	17		1	A6
A13	1		20	19		1	A5
A12	1		22	21		1	A4
A11	1		24	23		1	A3
A10	1		26	25		1	A2
A9	1		28	27		1	A1
A8	1		30	29		1	A0
RD*	10		32	31		10	WR*
MEMRQ*	10		34	33		10	IORQ*
MEMEX		55	36	35		1	IOEXP
MCSYNC*	10		38	37		15	REFRESH*
STATUS 0*			40	39			STATUS 1*
BUSRQ*			42	41			BUSAK*
INTRQ*		40	44	43			INTAK*
NMIRQ*		40	46	45			WAITRQ*
PBRESET*		40	48	47		10	SYSRESET*
CNTRL*			50	49			CLOCK*
PCI	IN		52	51	OUT		PCO
AUX GND			54	53			AUX GND
AUX -V			56	55			AUX +V

*Low-level active logic

STD Edge Connector

MECHANICAL SPECIFICATIONS

Meets all STD Series 7000 mechanical specifications.

USER'S MANUAL

Request Pro-Log document #109895.