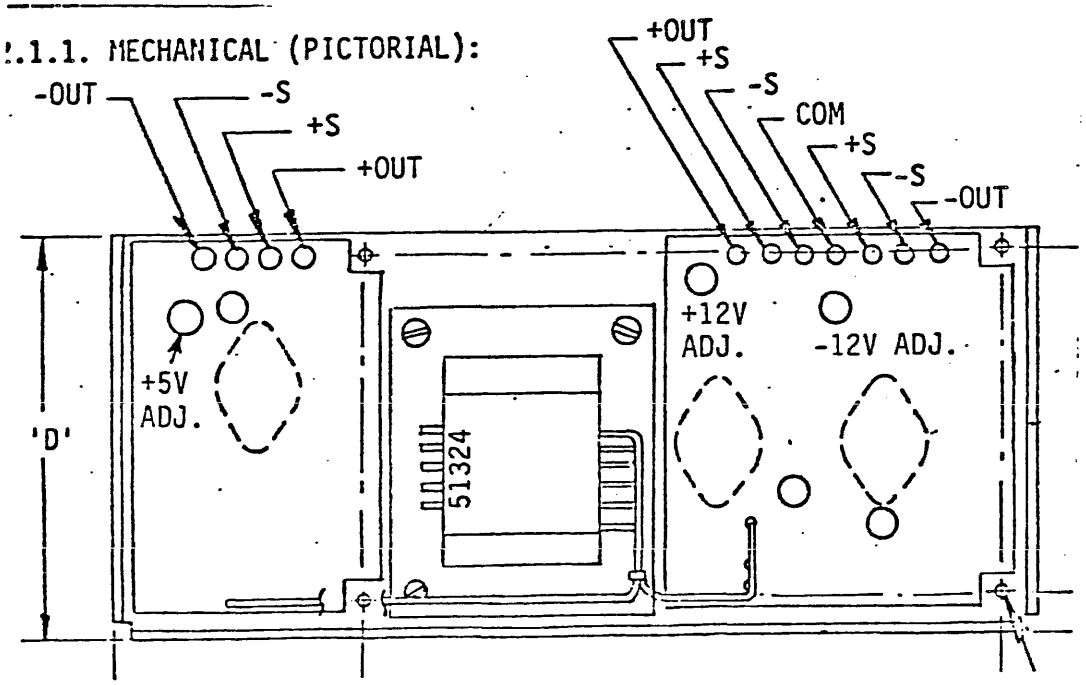
Fuses

never happen

F1	Battery back-up
F2	Tape drive & +5 @ 75 amp
F3	Disc drive & +5 +/- 12
F4	Fans

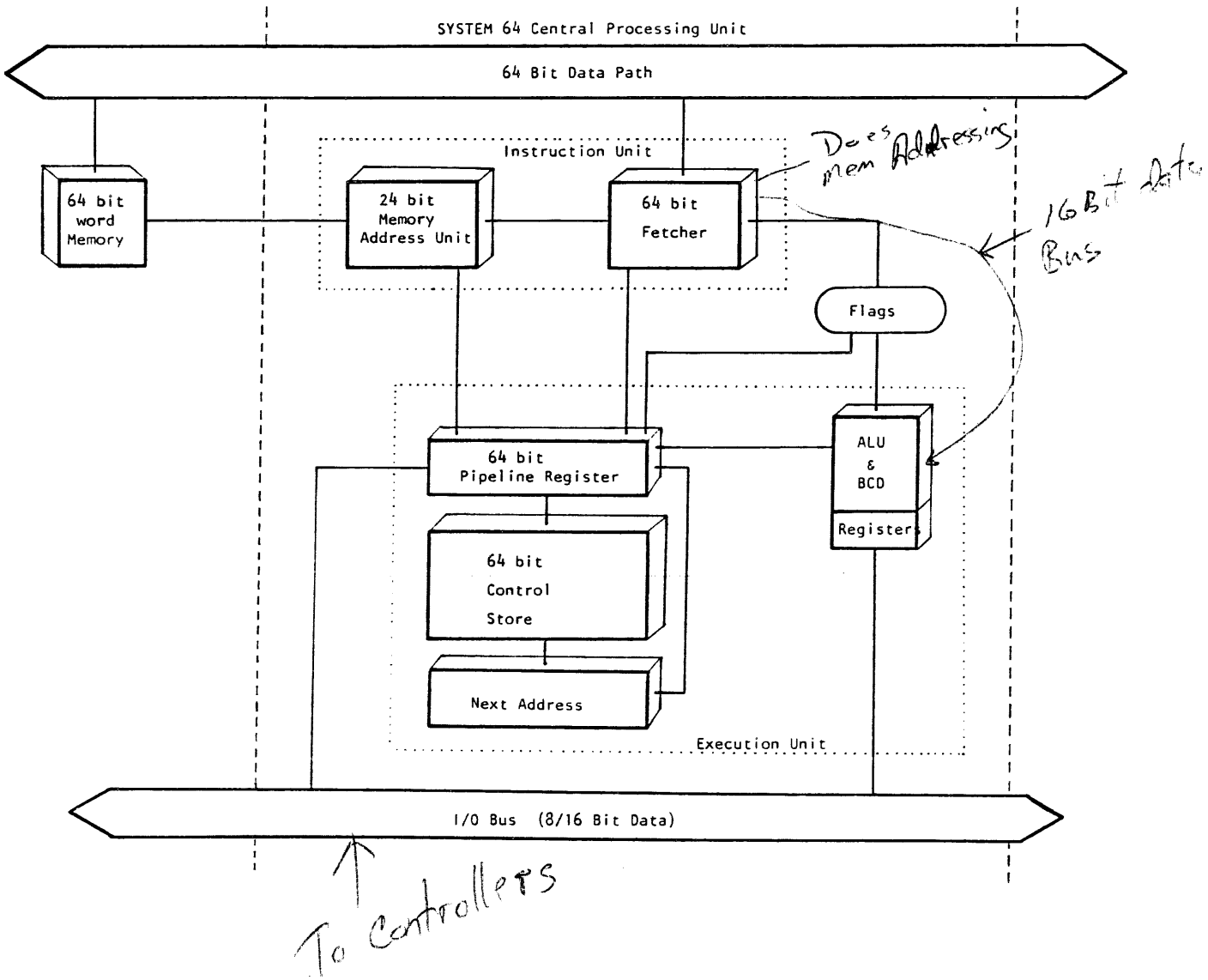
Backplane Connector

1.	+OUT	+12	8.		
2.	-S/COMS		9.	Common	Gnd
3.	-S	(-12)	10.	+OUT	+5
4.	+S	(+5)	11.	-OUT	-5
5.	-S	(-5)	12.	-OUT	-12
6.			13.	+S	(+12)
7.			14.	+S	(+12)

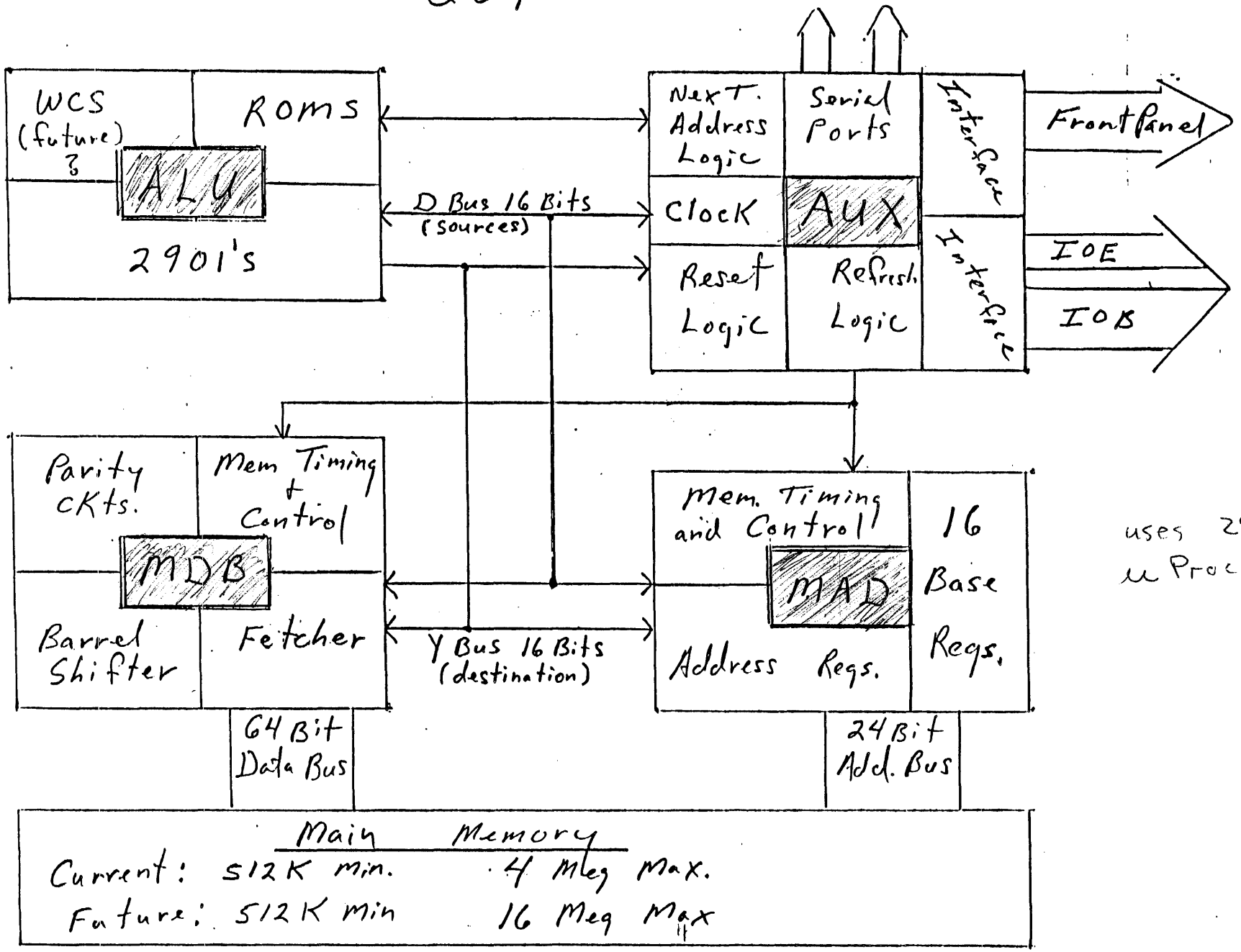


CPU Components

The following diagram represents the relationship between the components of the central processing unit:



QC4



uses 2901 μProc

2

200/300 LIMITATIONS

A. 8 BIT WIDE 1 MICROSECOND MEMORY.

B. INSTRUCTIONS MUST BE CONSTRUCTED.

C. SERIAL PROCESSING AT MICRO LEVEL.
   I.E. - SINGLE MEMORY ADDRESS REGISTER.

D. 8 BIT I/O INTERFACE.

E. SINGLE INSTRUCTION SET.

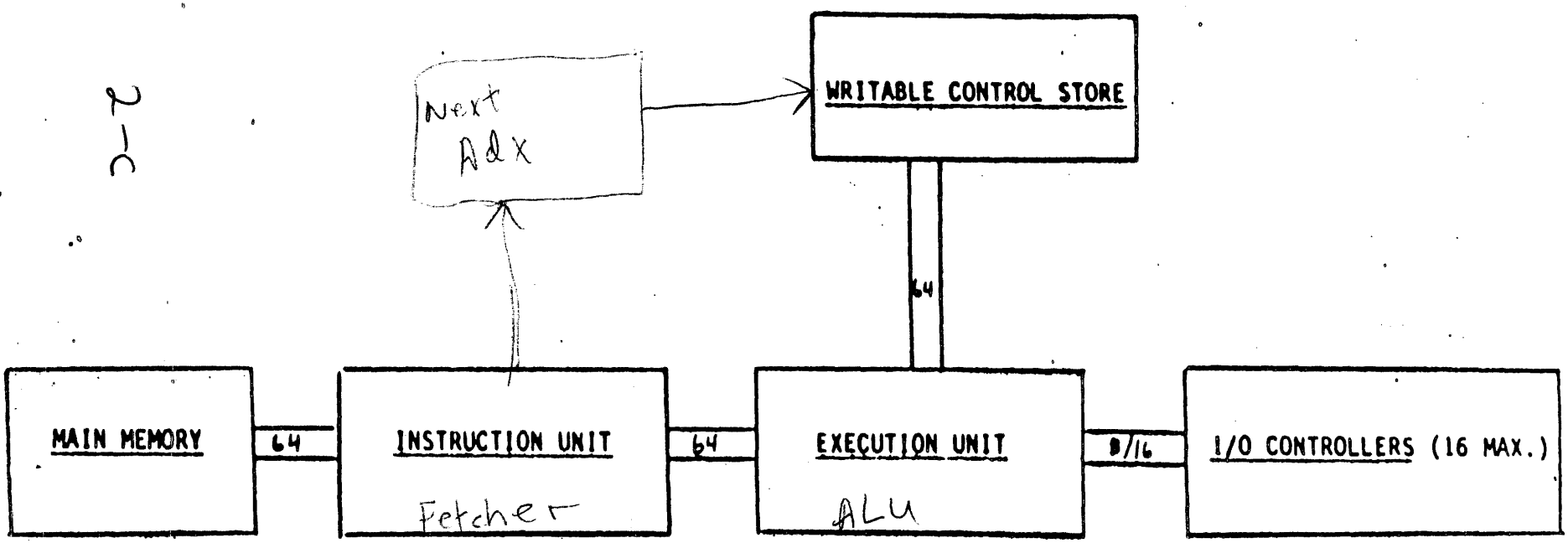
System 64

SYSTEM ~~100~~ ANSWERS

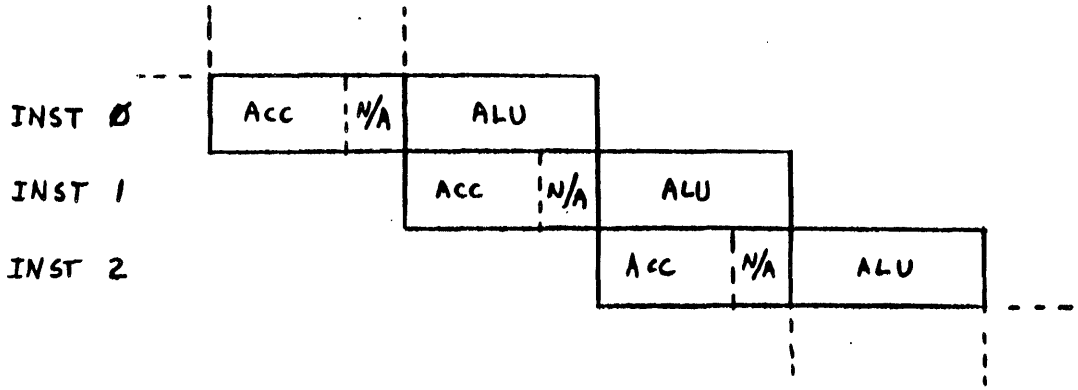
A. 64 BIT WIDE, 0.4 MICROSECOND MEMORY.
B. PARALLEL PROCESSING AT MICRO LEVEL.
   1. MULTIPLE ADDRESS REGISTERS.
   2. AUTOMATIC FETCH AND DECODE.
C. 8/16 BIT EXPANDED I/O INTERFACE.
D. SOFT INSTRUCTION SET.

2-B

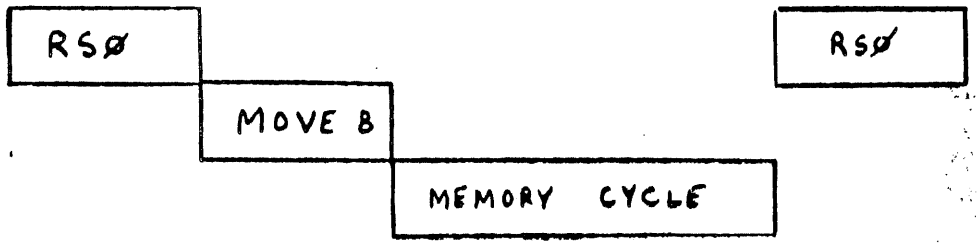
SYSTEM 400 OVERVIEW



REVIEW - BREAKWATER μP TIMING

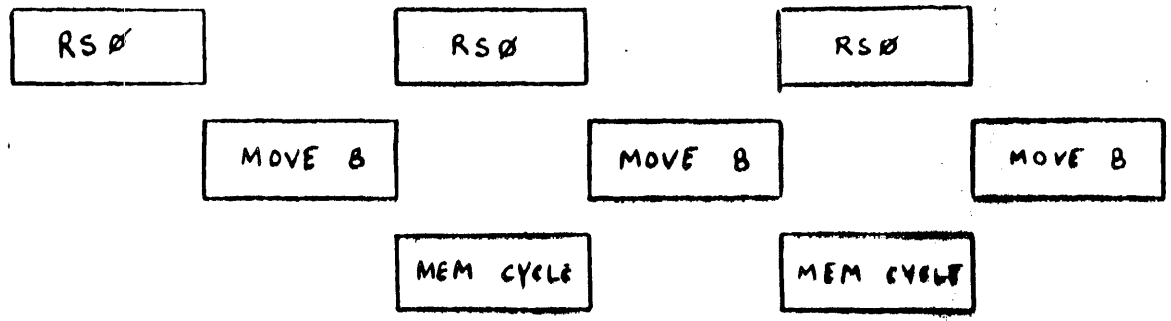


Q29 IOU DATA MOVEMENT



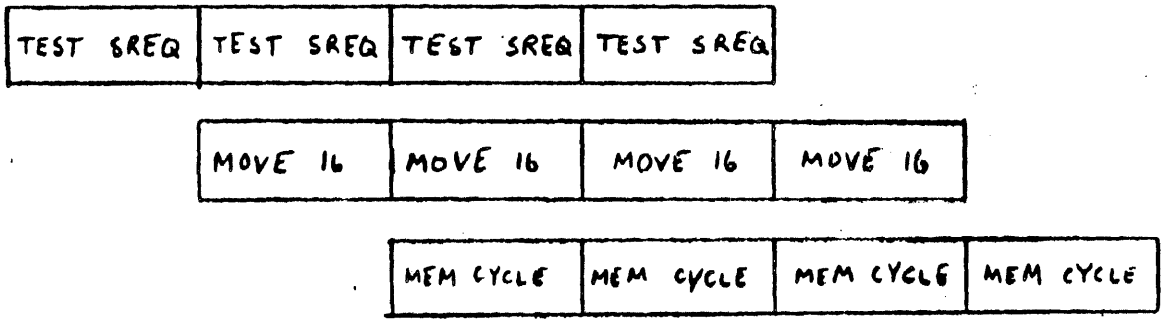
DATA RATE = 450 K. BYTE / SEC.

IOU DATA MOVEMENT ON 400



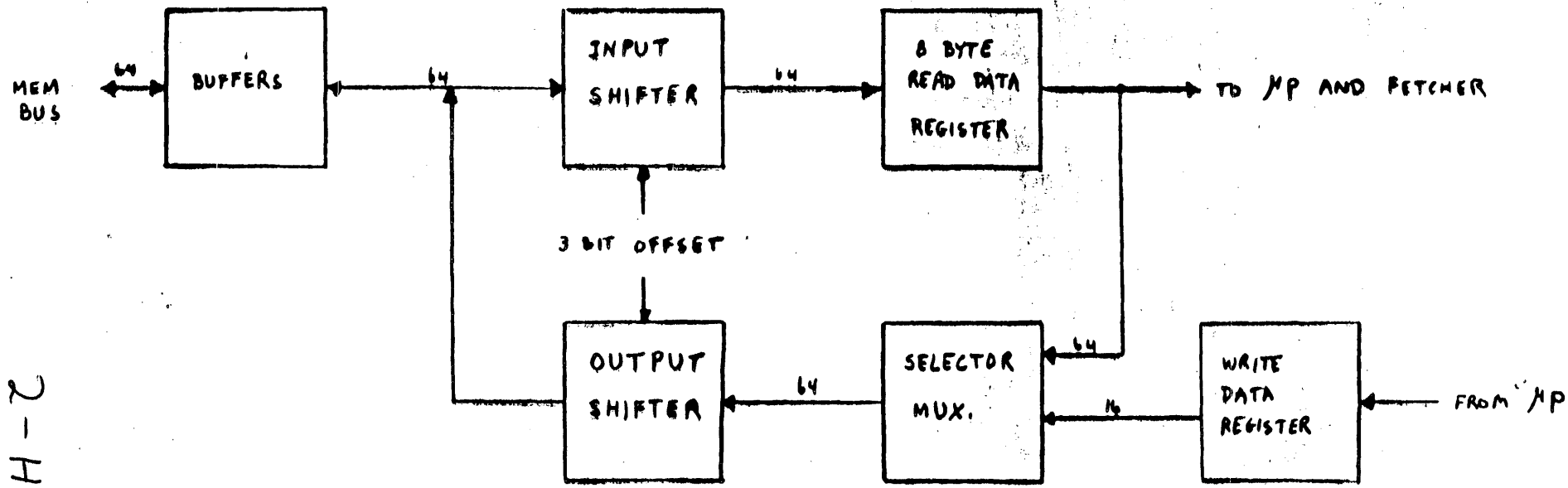
MAX. DATA RATE = 1.25 M. BYTE/ SEC.

PROPOSED EXPANSION DATA MOVEMENT

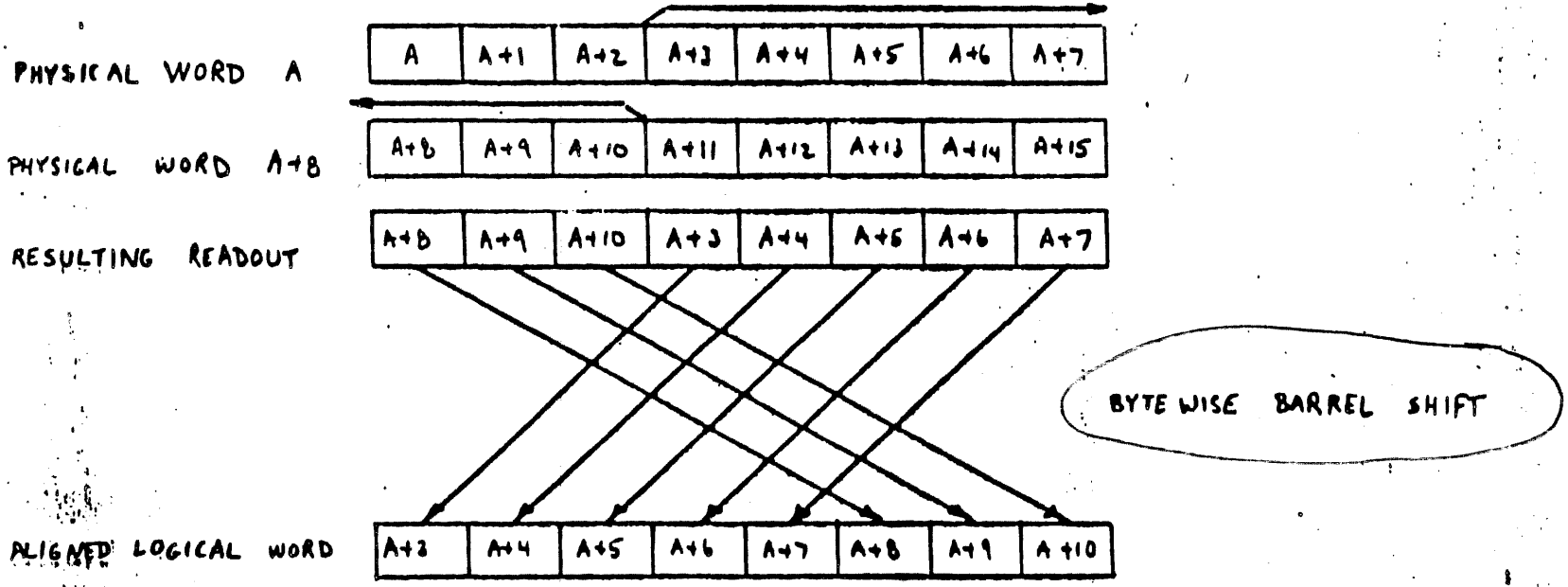


MAX. DATA RATE = 5 M. BYTE / SEC.

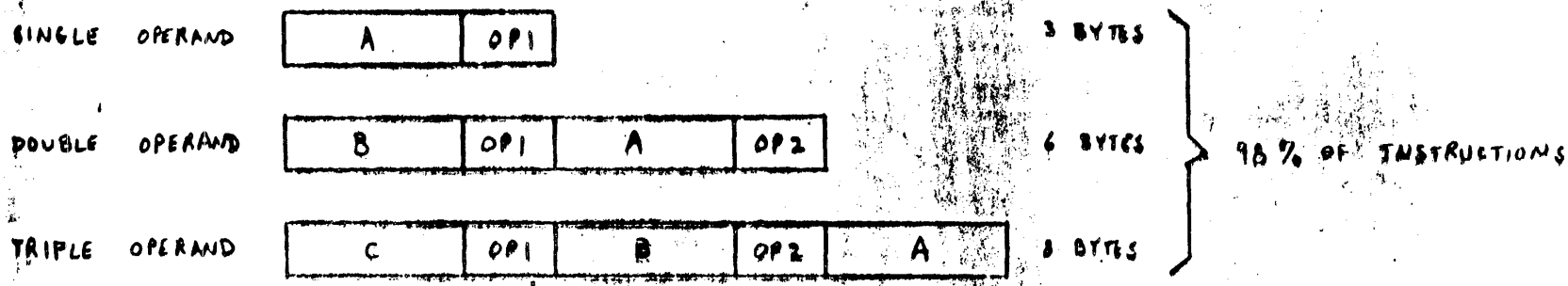
OVERALL DATA PATH



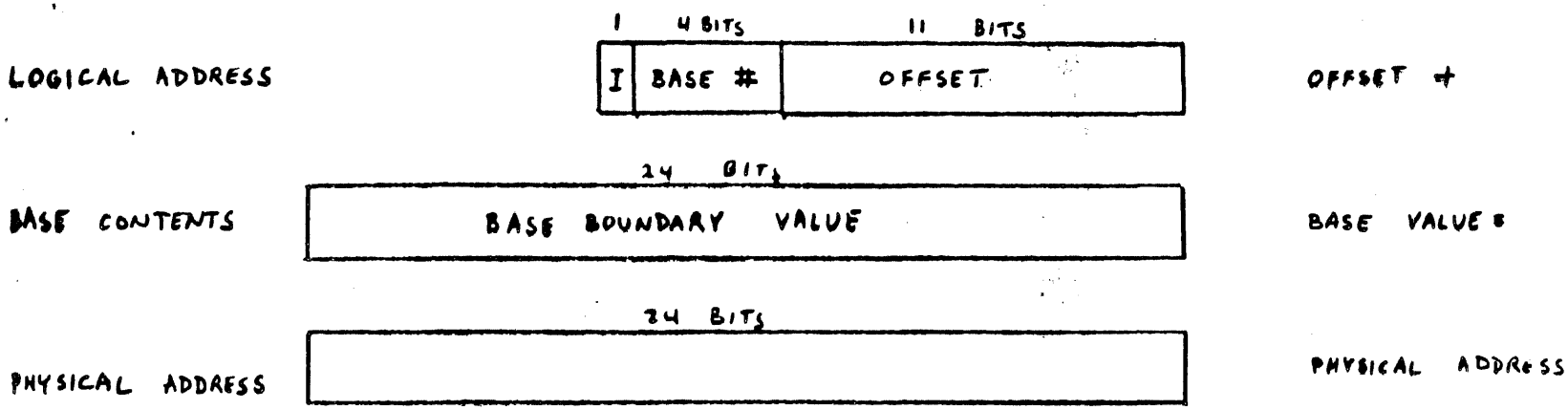
LOGICAL MEMORY WORD



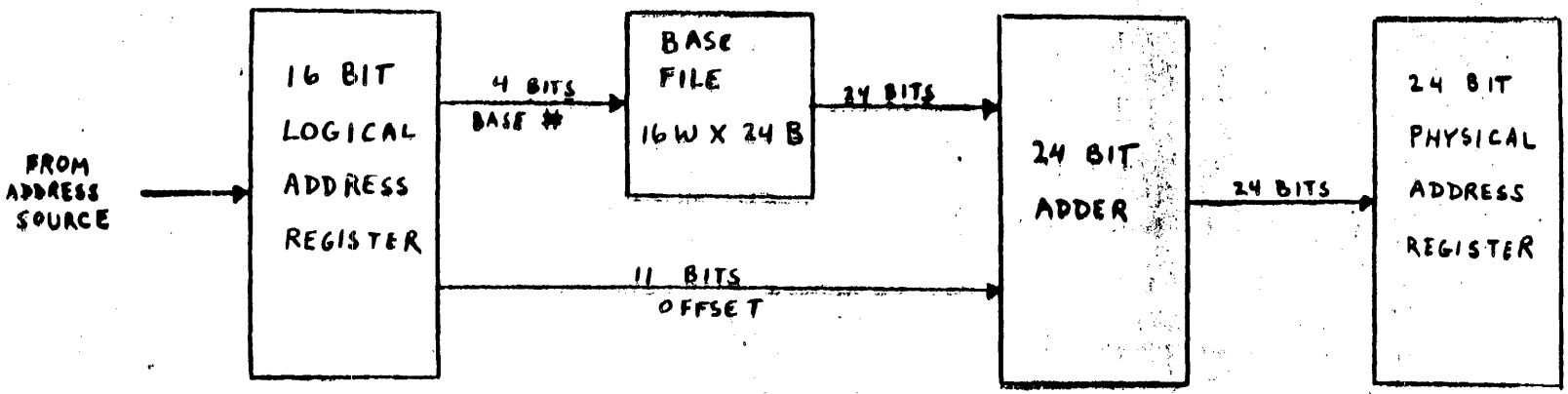
"REAL" INSTRUCTION FORMATS



QANTEL LOGICAL ADDRESSING



AUTOMATIC ADDRESS CONVERSION



LOGICAL WORD ADDRESSING