

Fuses

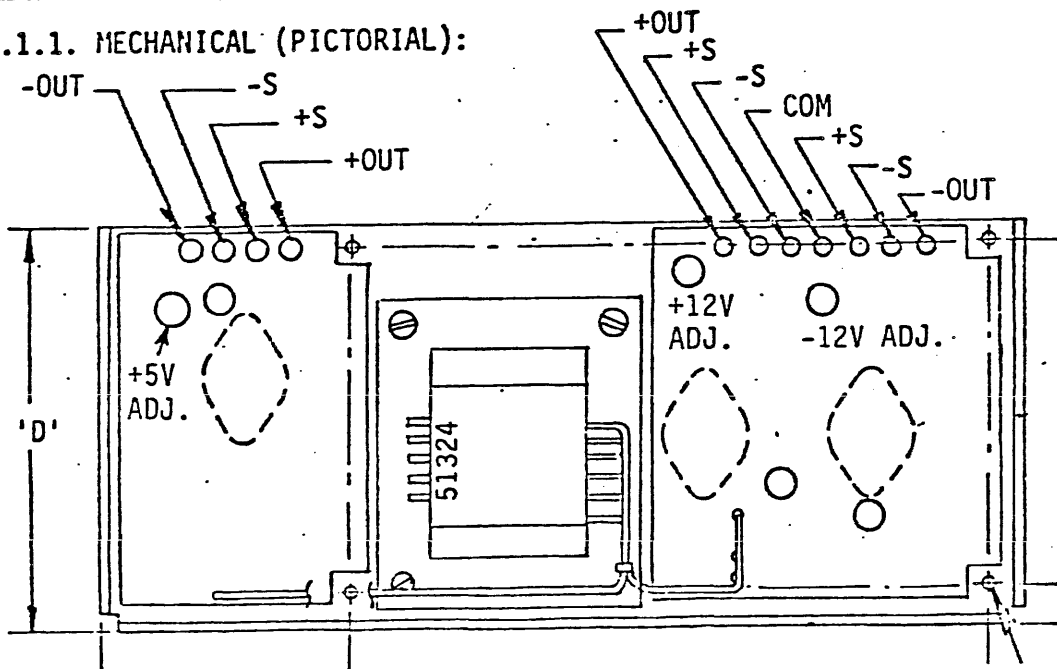
- F1 Battery back-up
- F2 Tape drive & +5 @ 75 amp
- F3 Disc drive & +5 +/- 12
- F4 Fans

*never happen*

Backplane Connector

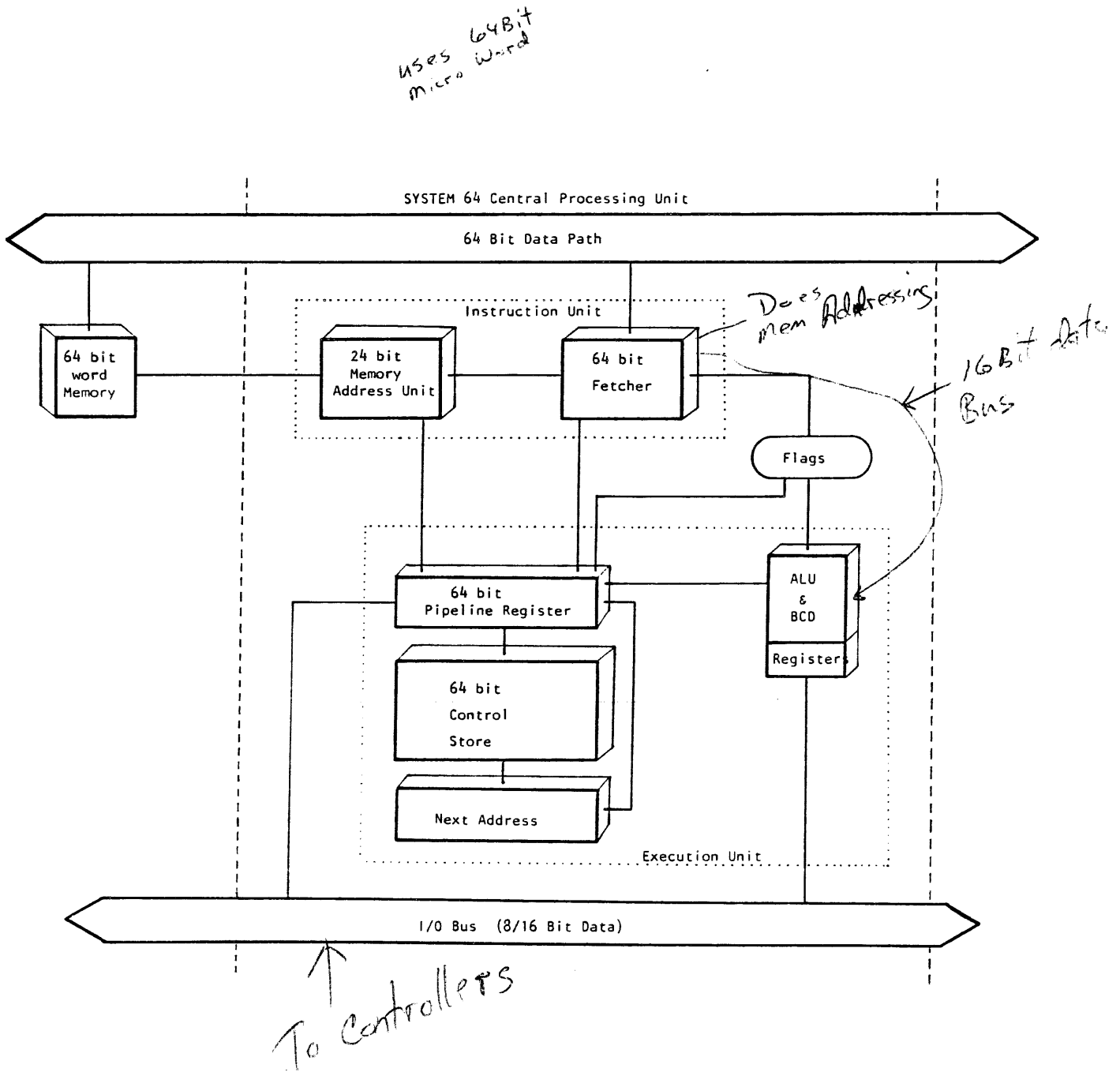
1.	+OUT	+12	8.		
2.	-S/COMS		9.	Common	Gnd
3.	-S	(-12)	10.	+OUT	+5
4.	+S	(+5)	11.	-OUT	-5
5.	-S	(-5)	12.	-OUT	-12
6.			13.	+S	(+12)
7.			14.	+S	(+12)

1.1.1. MECHANICAL (PICTORIAL):

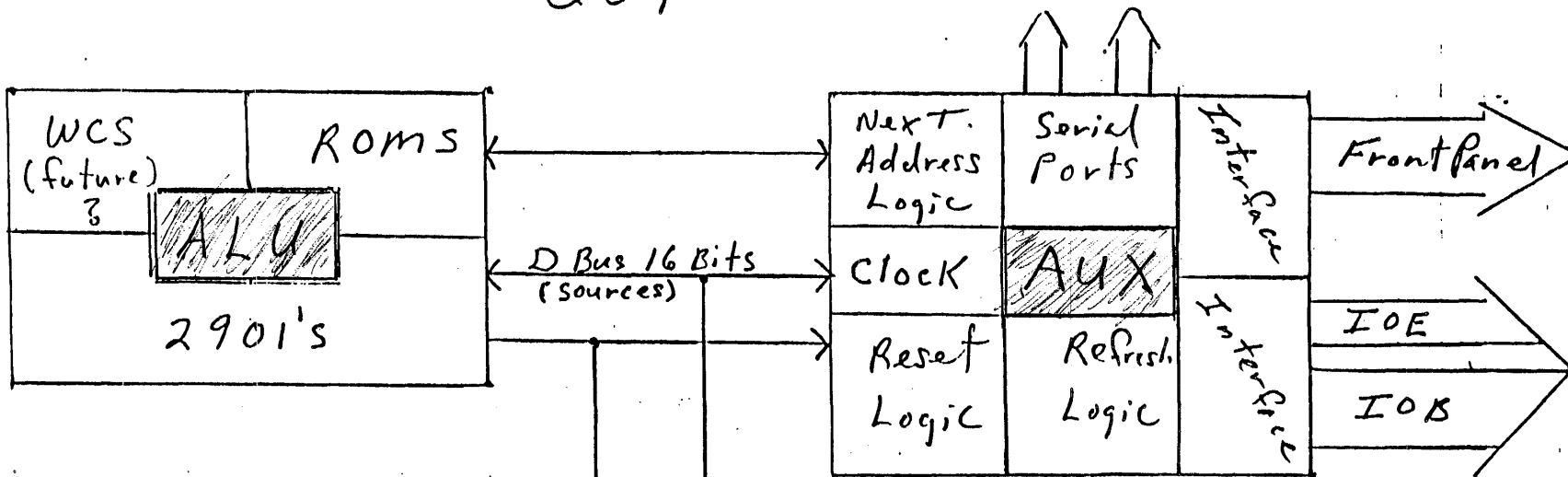


### CPU Components

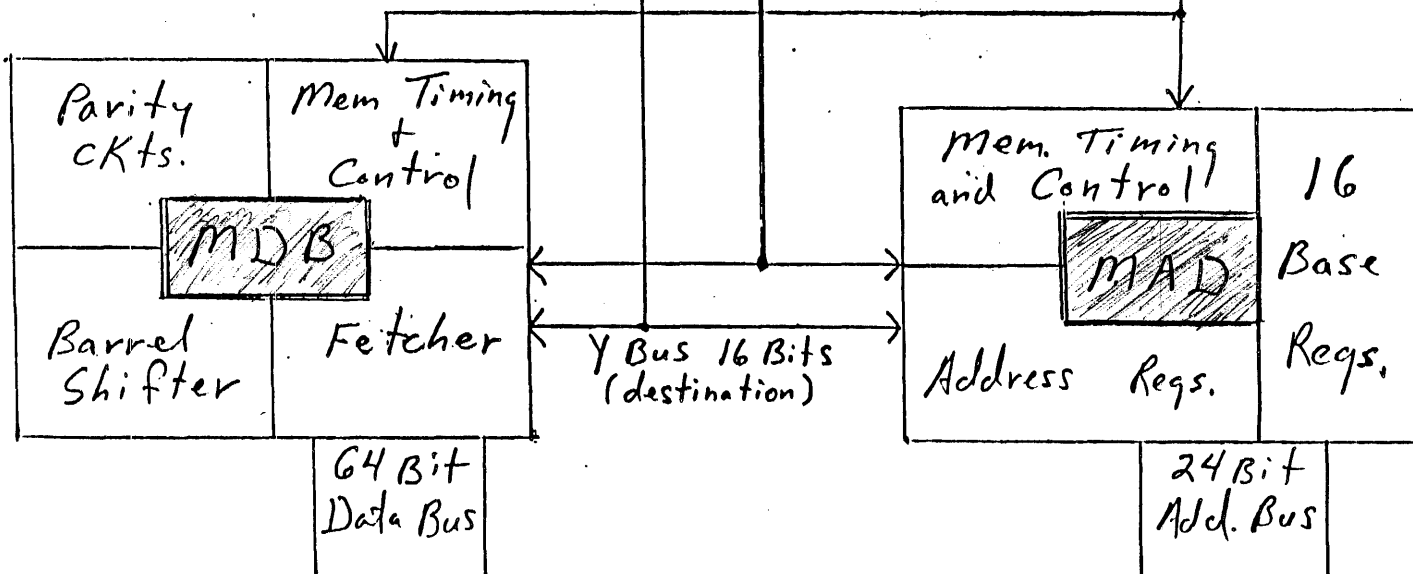
The following diagram represents the relationship between the components of the central processing unit:



Q64



2



uses 2901  
u Proc

	Main Memory	Memory
Current:	512K min.	4 Meg Max.
Future:	512K min	16 Meg Max

### 200/300 LIMITATIONS

- A. 8 BIT WIDE 1 MICROSECOND MEMORY.
- B. INSTRUCTIONS MUST BE CONSTRUCTED.
- C. SERIAL PROCESSING AT MICRO LEVEL.  
I.E. - SINGLE MEMORY ADDRESS REGISTER.
- D. 8 BIT I/O INTERFACE.
- E. SINGLE INSTRUCTION SET.

2-A

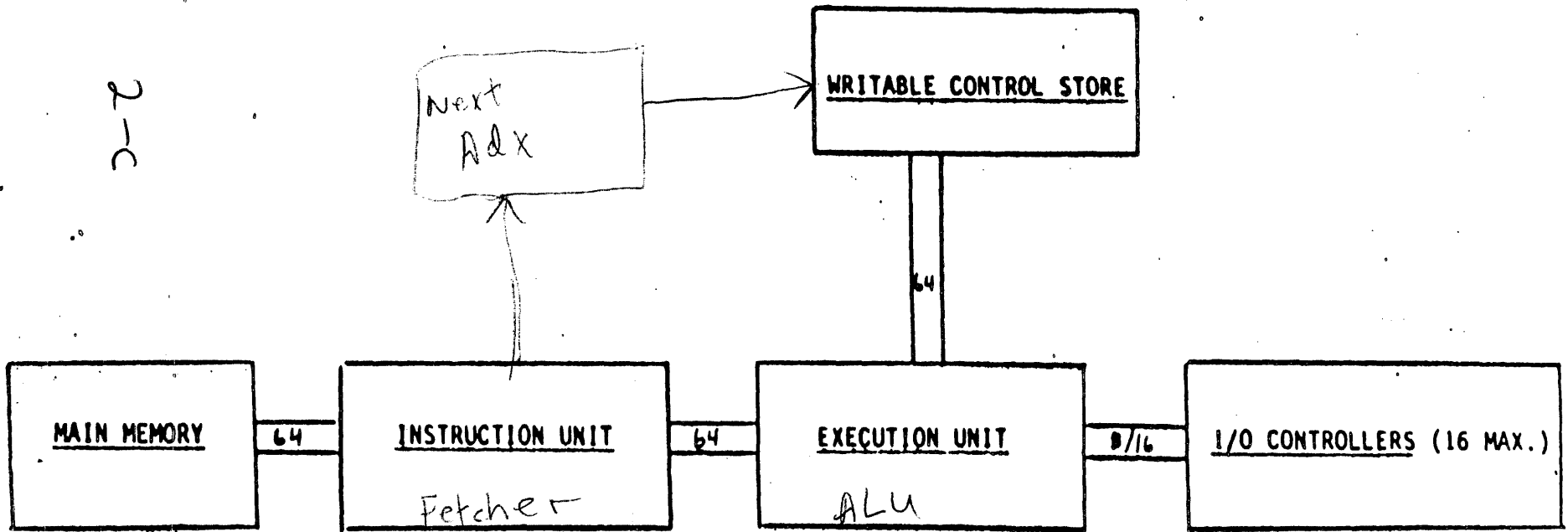
System 64

SYSTEM ~~400~~ ANSWERS

- A. 64 BIT WIDE, 0.4 MICROSECOND MEMORY.
- B. PARALLEL PROCESSING AT MICRO LEVEL.
  - 1. MULTIPLE ADDRESS REGISTERS.
  - 2. AUTOMATIC FETCH AND DECODE.
- C. 8/16 BIT ~~EXPANDED~~ I/O INTERFACE.
- D. SOFT INSTRUCTION SET.

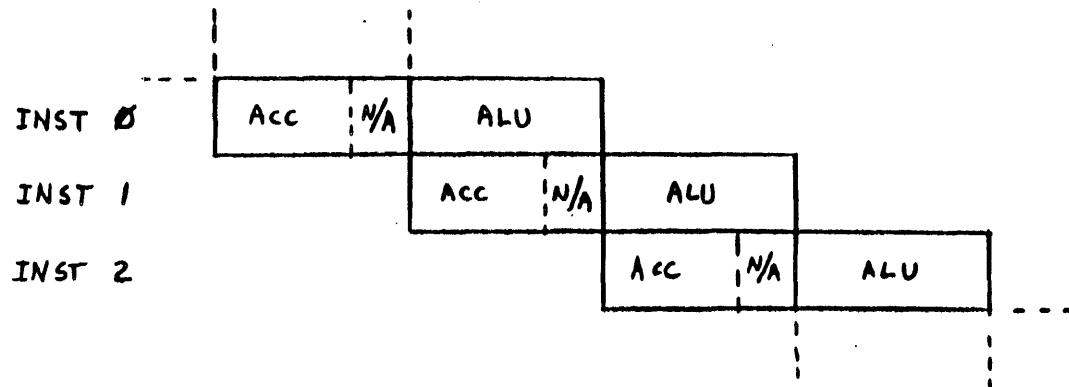
2-B

# SYSTEM 400 OVERVIEW

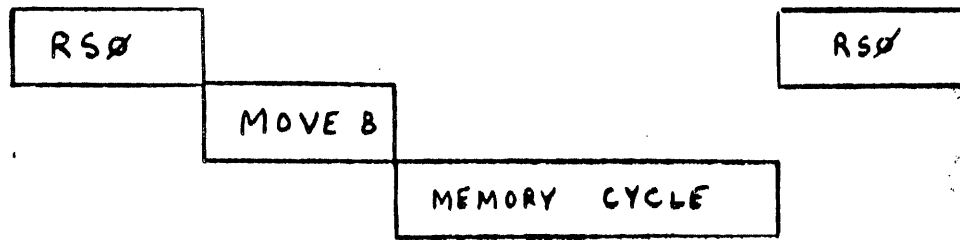


# REVIEW - BREAKWATER MP TIMING

2-D



# Q29 IOU DATA MOVEMENT

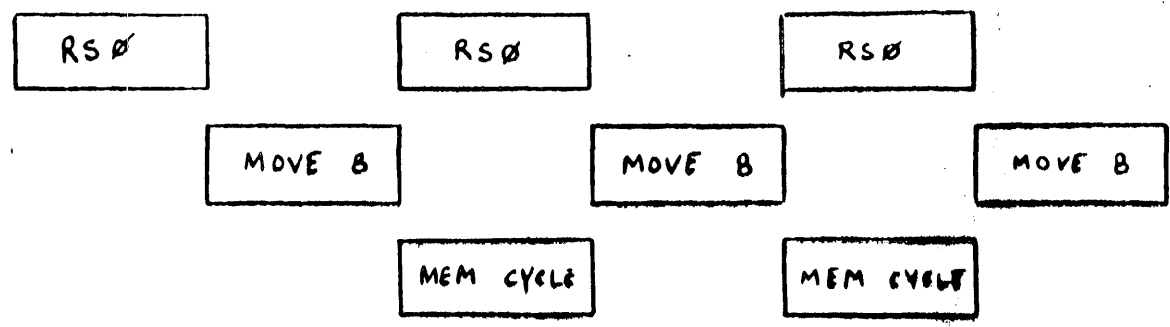


DATA RATE = 450 K. BYTE / SEC.

2-E



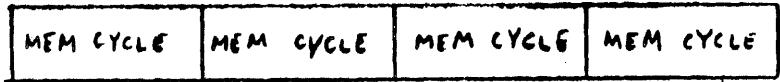
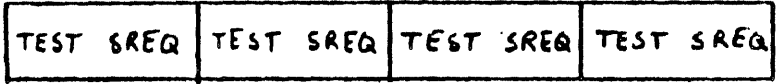
# IOU DATA MOVEMENT ON 400



MAX. DATA RATE = 1.25 M. BYTE / SEC.

2-F

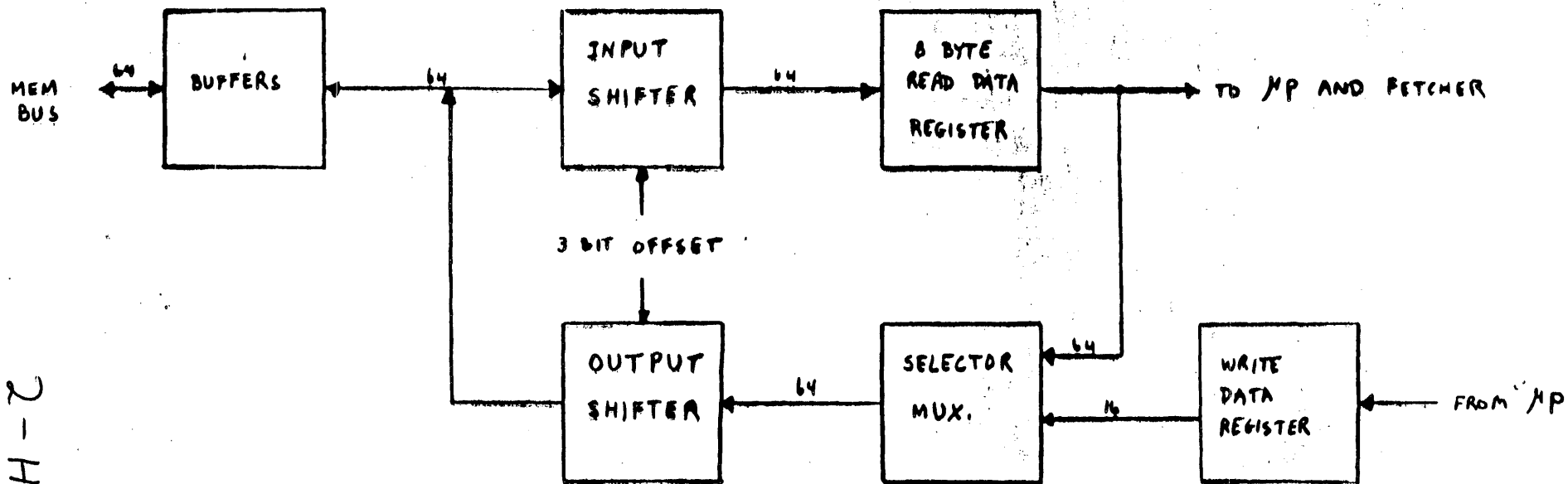
# PROPOSED EXPANSION DATA MOVEMENT



2-6

MAX. DATA RATE = 5 M. BYTE / SEC.

# OVERALL DATA PATH



H-2

# LOGICAL MEMORY WORD

PHYSICAL WORD A



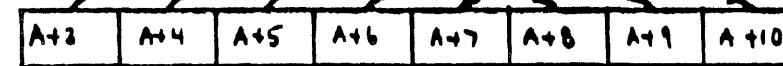
PHYSICAL WORD A+8



RESULTING READOUT



ALIGNED LOGICAL WORD



BYTEWISE BARREL SHIFT

3

# "REAL" INSTRUCTION FORMATS

SINGLE OPERAND



3 BYTES

DOUBLE OPERAND



6 BYTES

TRIPLE OPERAND

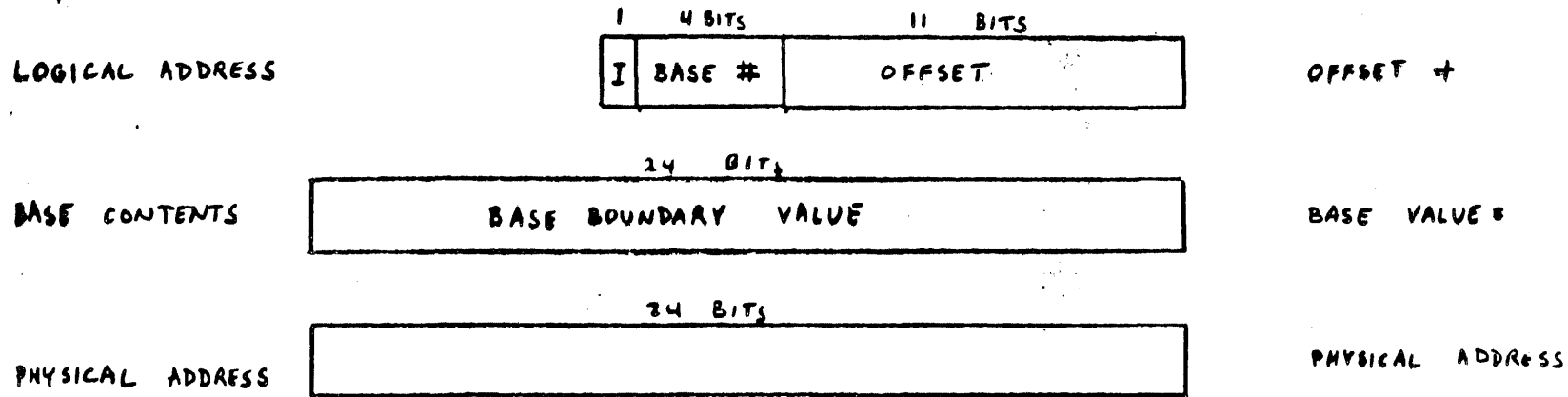


8 BYTES

98% OF INSTRUCTIONS

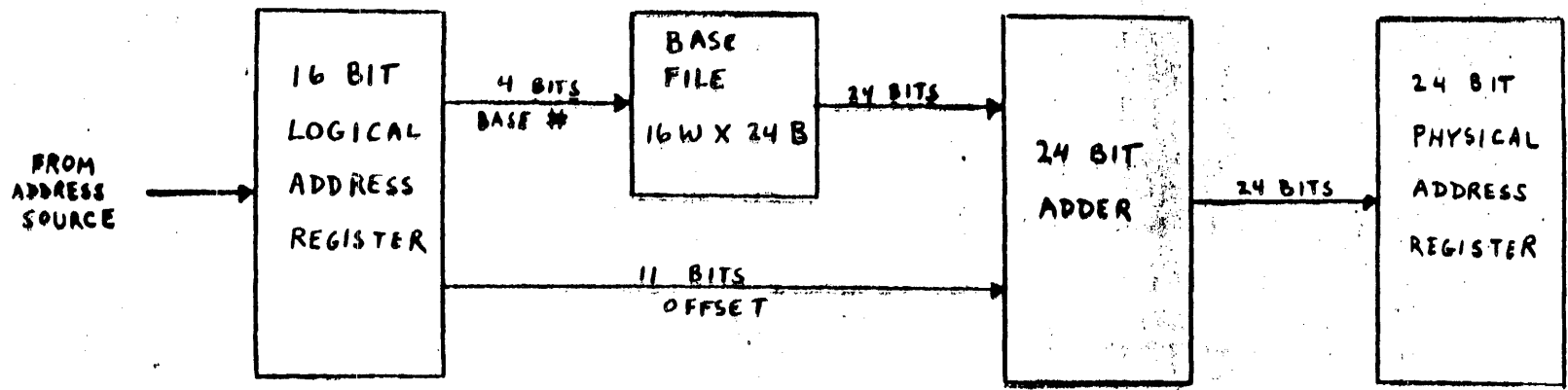
2-I

# QANTEL LOGICAL ADDRESSING



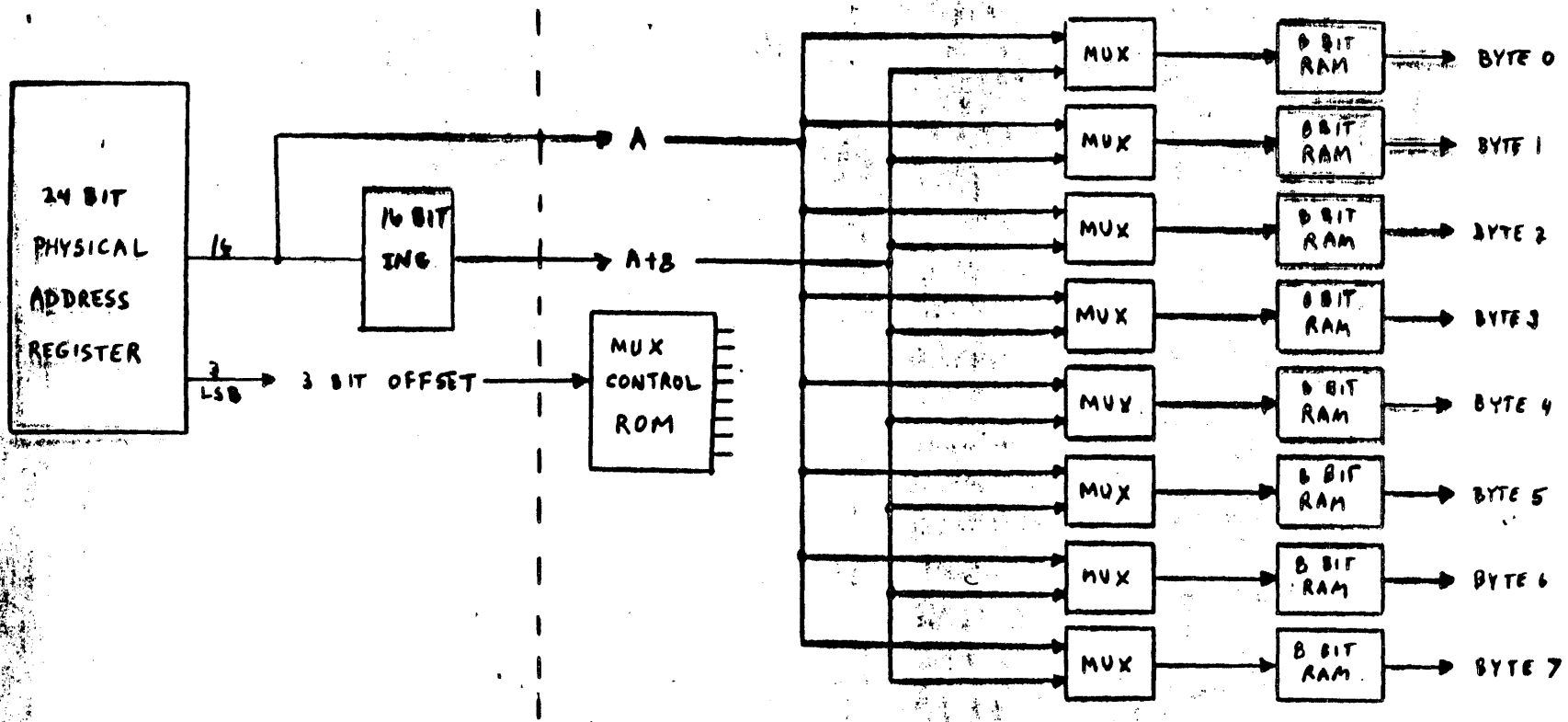
2-K

# AUTOMATIC ADDRESS CONVERSION



2-1

# LOGICAL WORD ADDRESSING



2-5