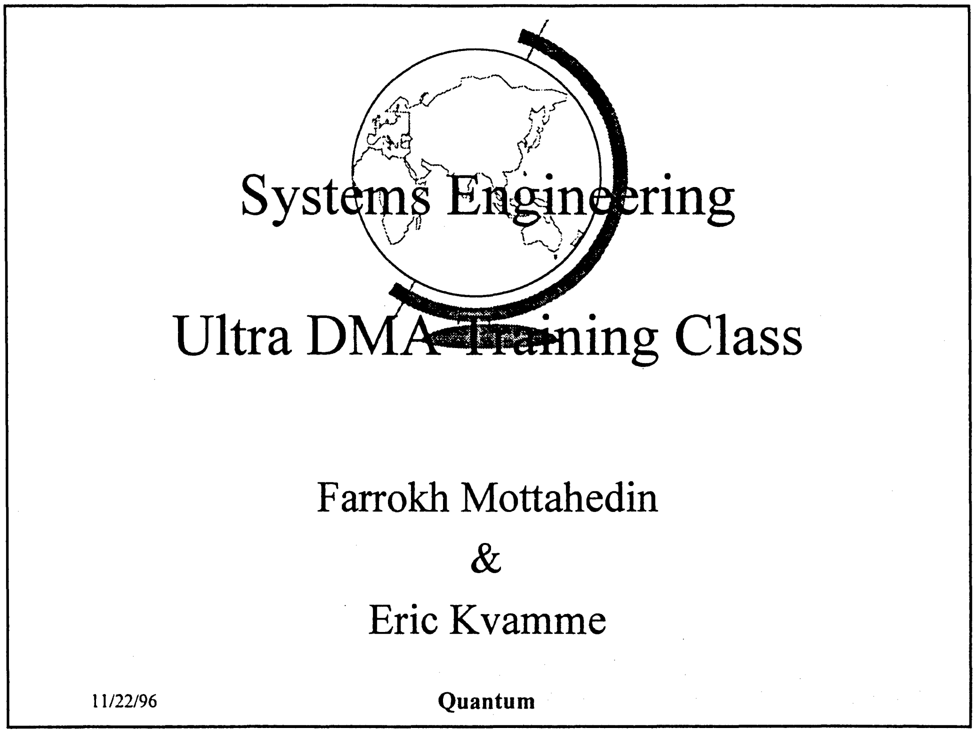
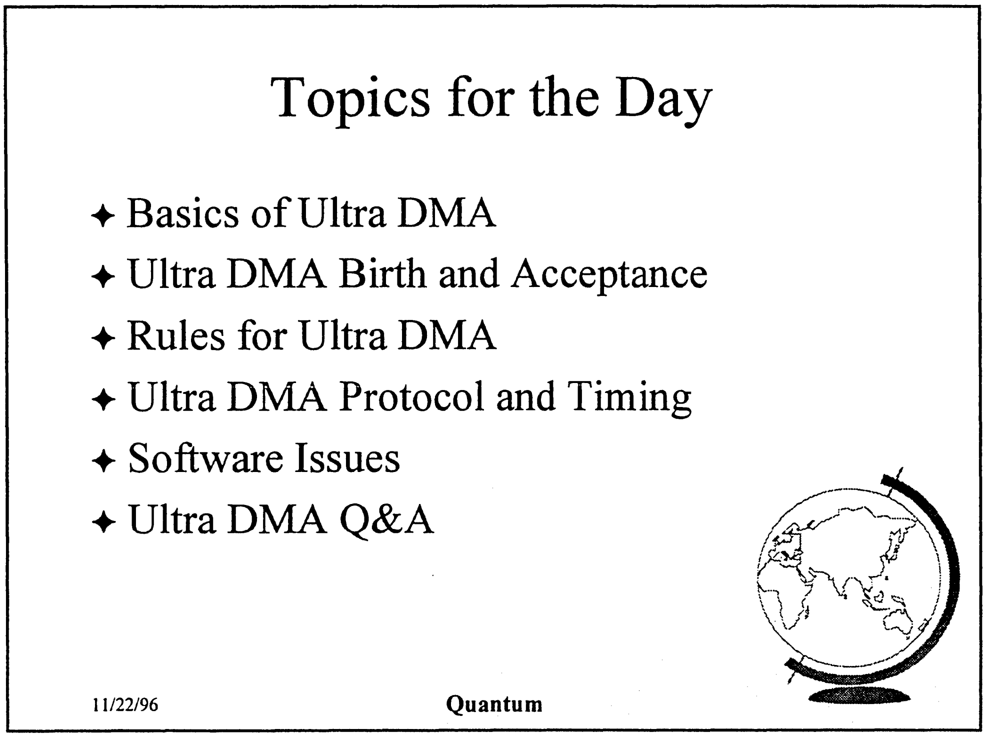


Systems Engineering

Ultra DMA Training Class

Farrokh Mottahedin
&
Eric Kvamme

11/22/96 **Quantum**



Topics for the Day

- ✦ Basics of Ultra DMA
- ✦ Ultra DMA Birth and Acceptance
- ✦ Rules for Ultra DMA
- ✦ Ultra DMA Protocol and Timing
- ✦ Software Issues
- ✦ Ultra DMA Q&A

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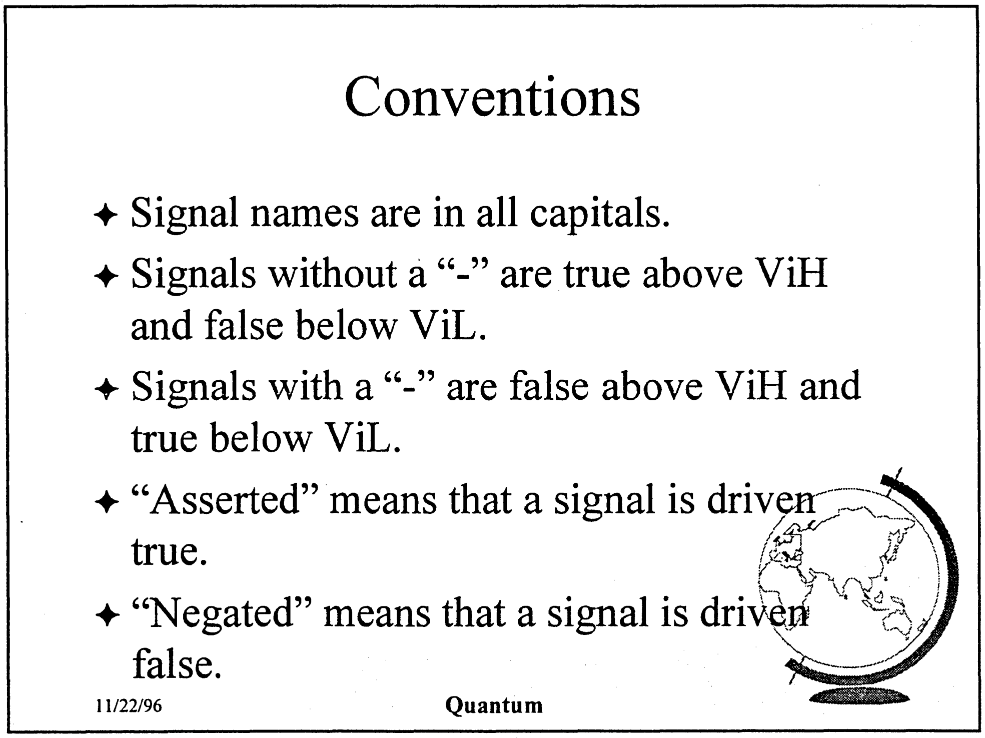

Conventions

- Signal names are in all capitals.
- Signals without a "-" are true above ViH and false below ViL.
- Signals with a "-" are false above ViH and true below ViL.
- "Asserted" means that a signal is driven true.
- "Negated" means that a signal is driven false.

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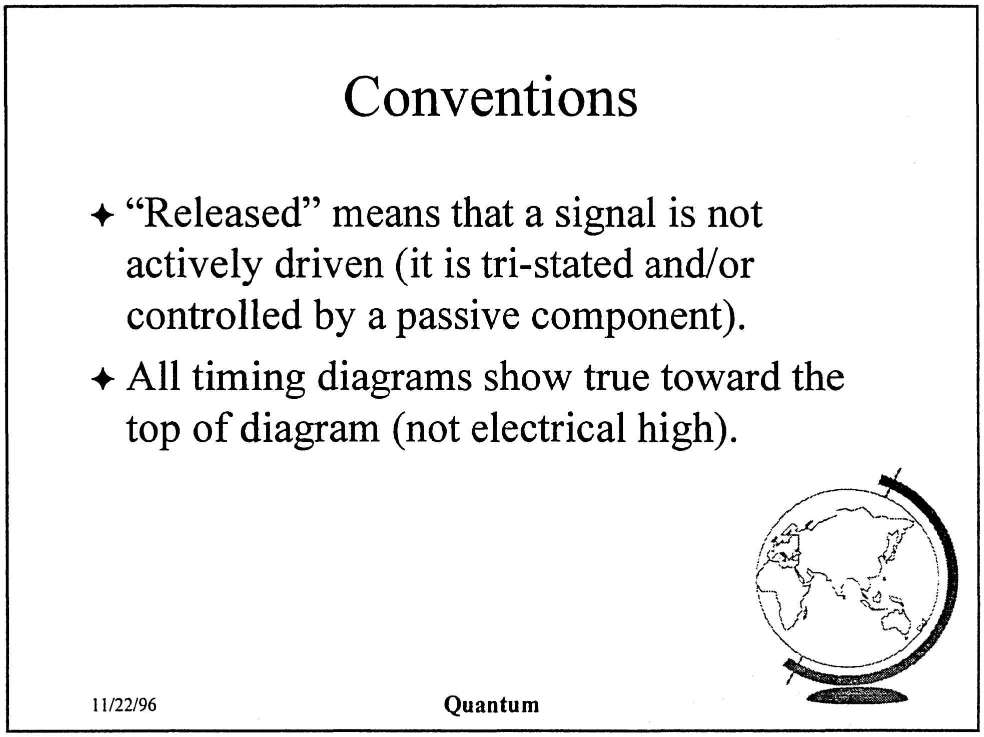

Conventions

- “Released” means that a signal is not actively driven (it is tri-stated and/or controlled by a passive component).
- All timing diagrams show true toward the top of diagram (not electrical high).

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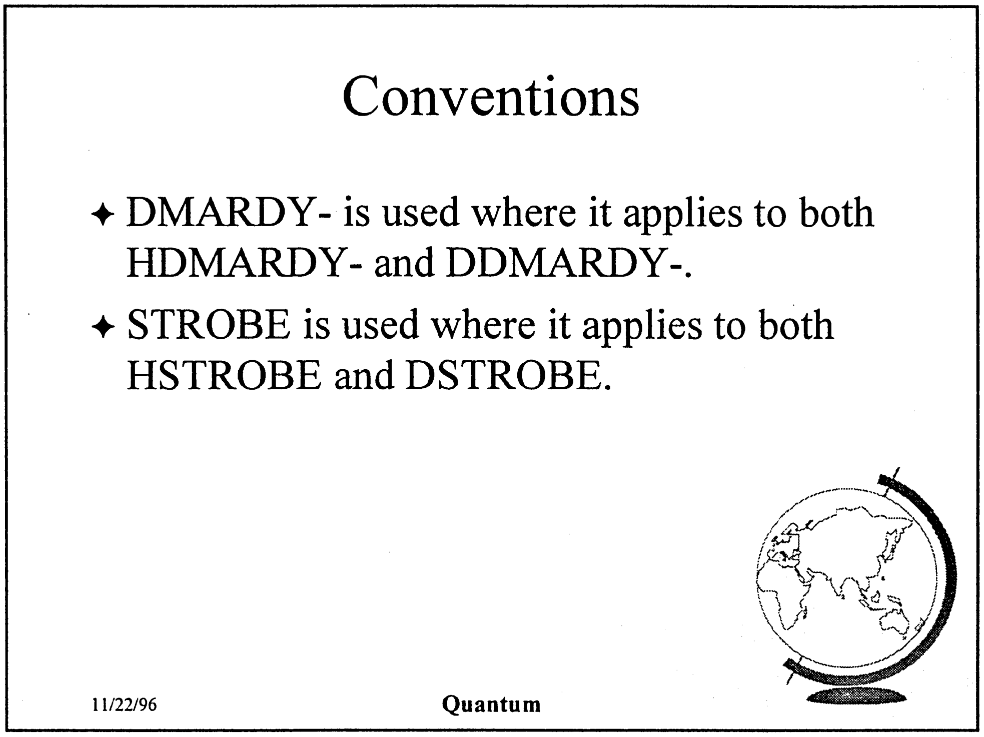

Conventions

- ✦ DMARDY- is used where it applies to both HDMARDY- and DDMARDY-.
- ✦ STROBE is used where it applies to both HSTROBE and DSTROBE.

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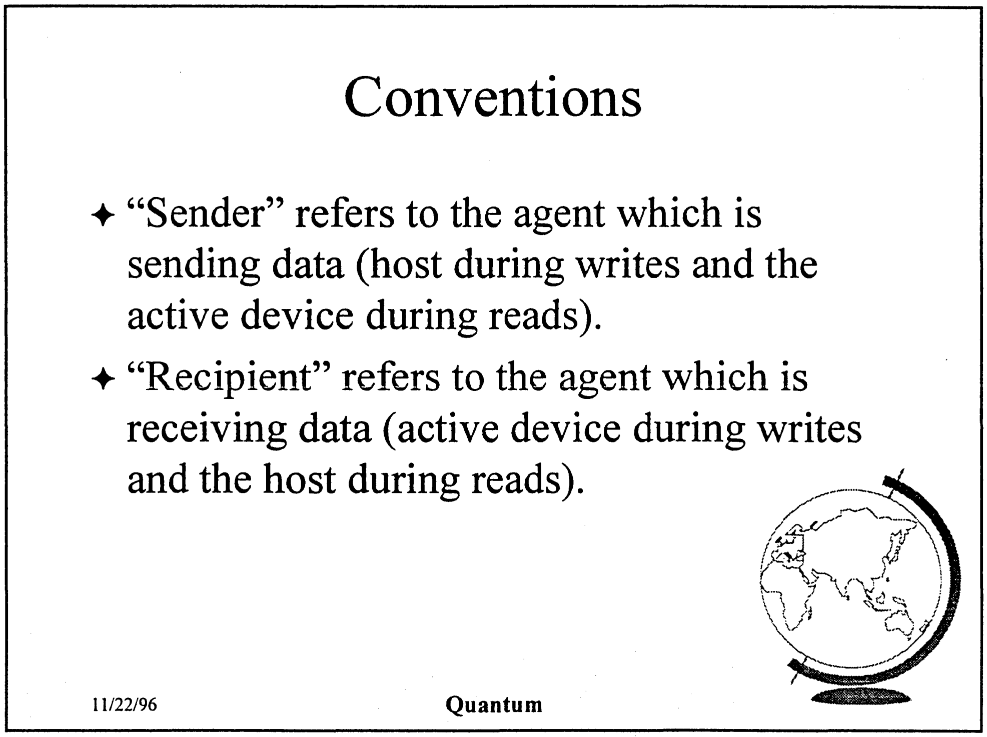

Conventions

- ✦ “Sender” refers to the agent which is sending data (host during writes and the active device during reads).
- ✦ “Recipient” refers to the agent which is receiving data (active device during writes and the host during reads).

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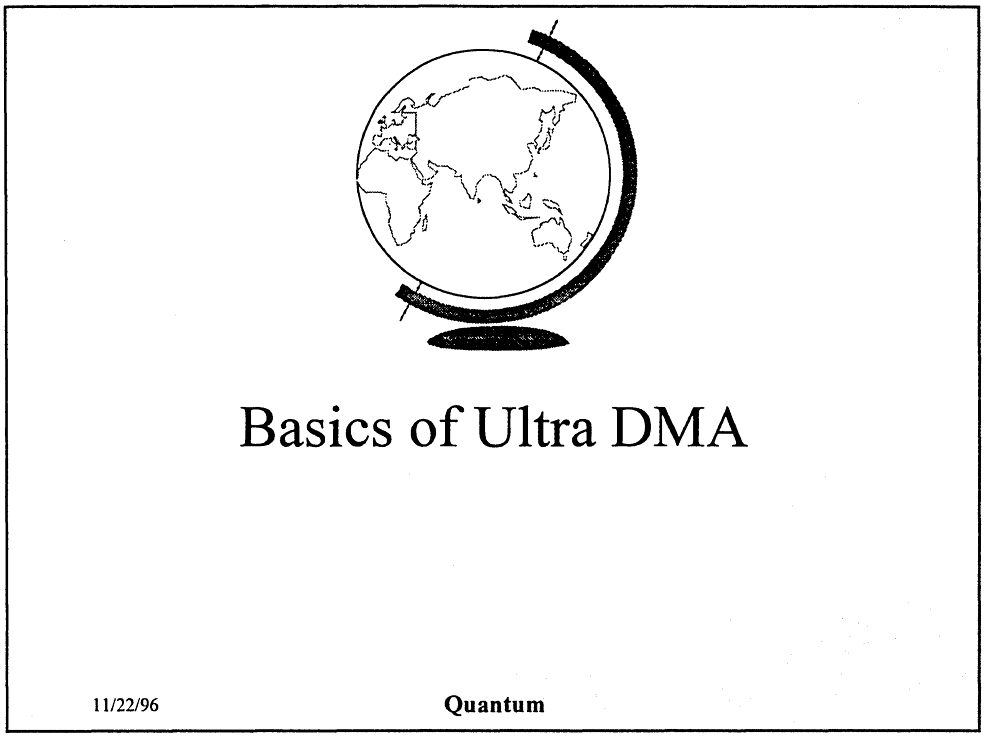

Basics of Ultra DMA

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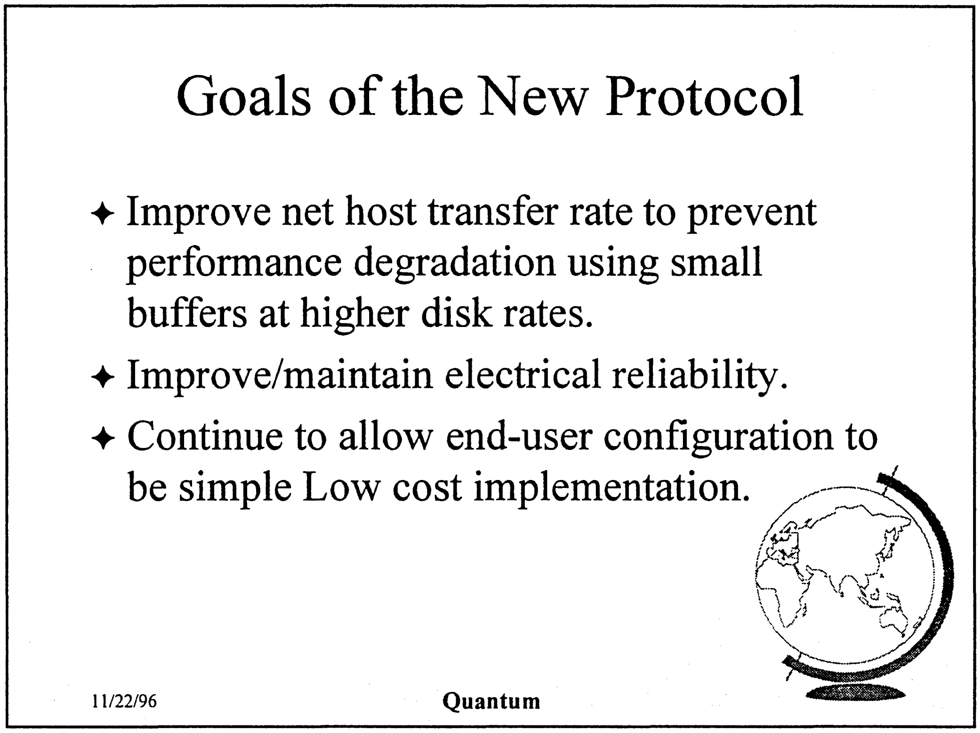

Goals of the New Protocol

- ✦ Improve net host transfer rate to prevent performance degradation using small buffers at higher disk rates.
- ✦ Improve/maintain electrical reliability.
- ✦ Continue to allow end-user configuration to be simple Low cost implementation.

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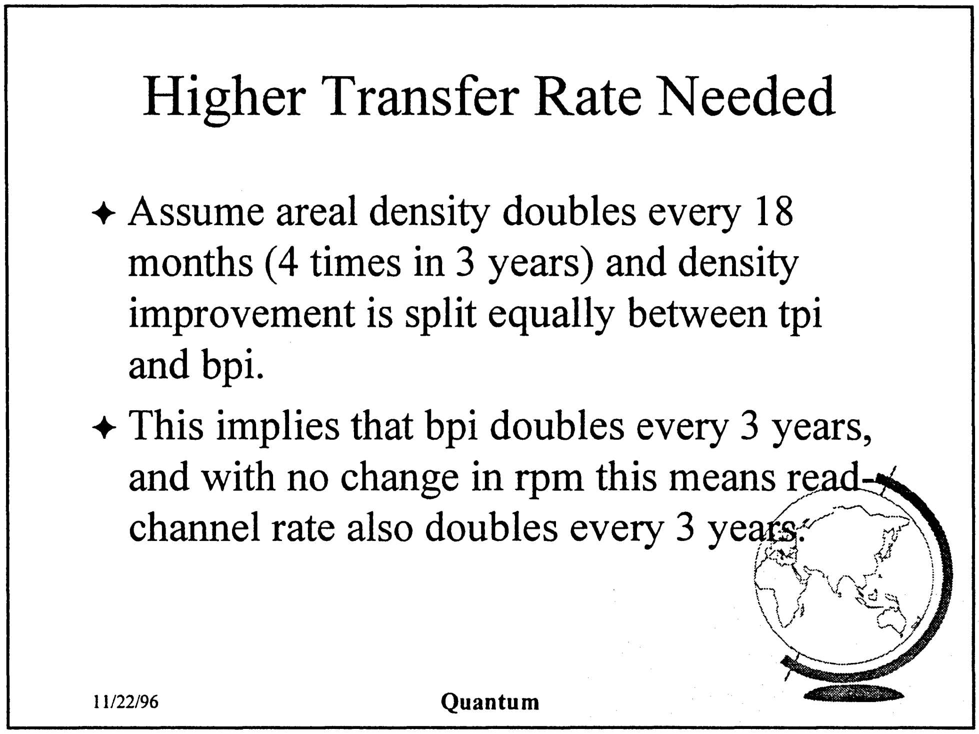

Higher Transfer Rate Needed

- ✦ Assume areal density doubles every 18 months (4 times in 3 years) and density improvement is split equally between tpi and bpi.
- ✦ This implies that bpi doubles every 3 years, and with no change in rpm this means read-channel rate also doubles every 3 years.

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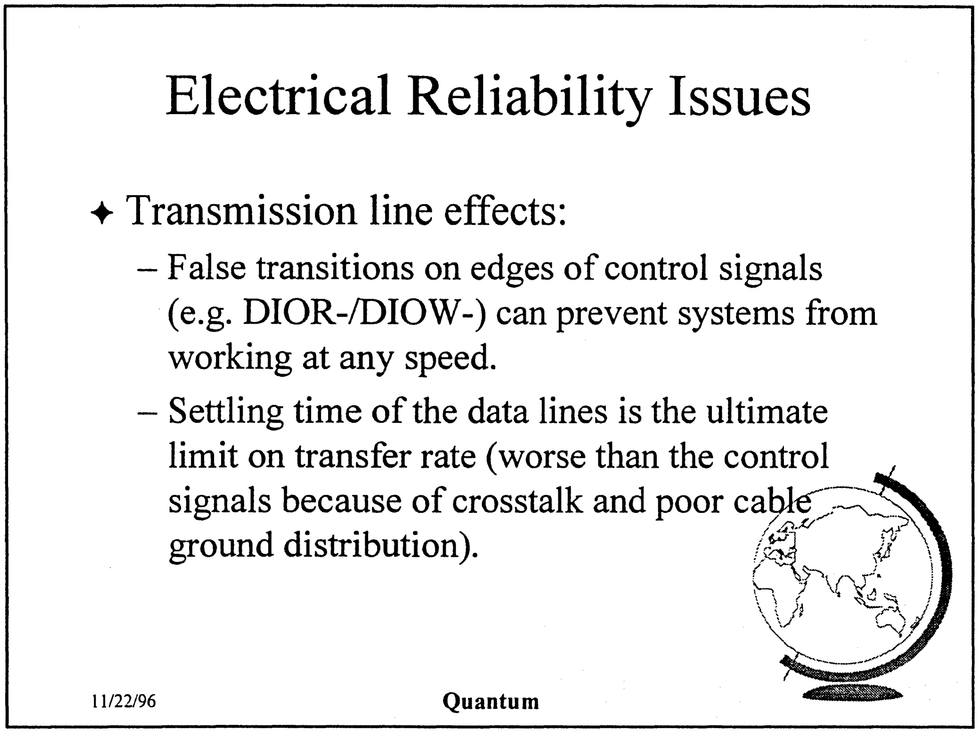
If 3.5" performance products move up from 5400 rpm to 7200 rpm in 1998, Fireball-class products will have a read channel rate of 85 x 2 x 1.33 = 227Mb/s (or 28MB/s).

Net host transfer rate must be greater than the average on-track data transfer rate (which is about 80 % of the read channel speed), so in this example we need a net host transfer rate of about 23MB/s.

Peak host transfer rate must be considerably higher to accommodate the protocol and interrupt overhead.



Electrical Reliability Issues

- ✦ Transmission line effects:
  - – False transitions on edges of control signals (e.g. DIOR-/DIOW-) can prevent systems from working at any speed.
  - – Settling time of the data lines is the ultimate limit on transfer rate (worse than the control signals because of crosstalk and poor cable ground distribution).

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Worst-case settling times are in the range of 25 to 35 ns, depending on the configuration.

Solutions today:

I/O drivers that limit slew rate (no less than 5ns),

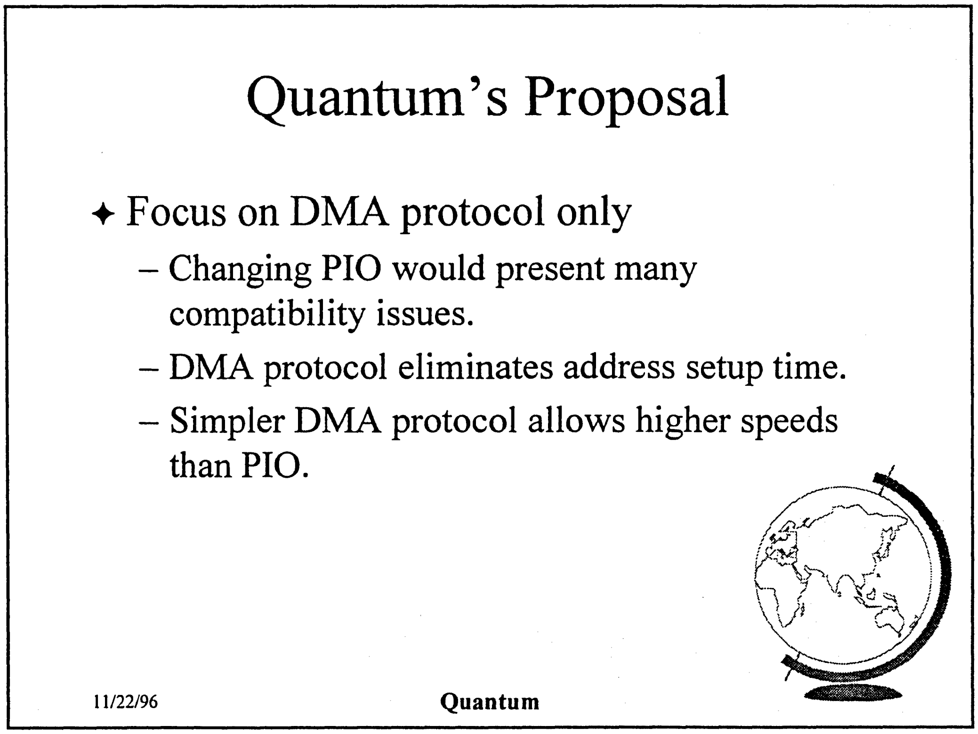
Host and device series resistor termination.

Possible solutions for supporting faster transfer rate:

Improve "analog plant" (drivers, receivers, cable and connectors)

New protocol to make better use of time available

Add CRC check as protection against poor implementations



Quantum's Proposal

- ✦ Focus on DMA protocol only
  - – Changing PIO would present many compatibility issues.
  - – DMA protocol eliminates address setup time.
  - – Simpler DMA protocol allows higher speeds than PIO.

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Introduce a new DMA protocol for speeds up to 33 MB/s

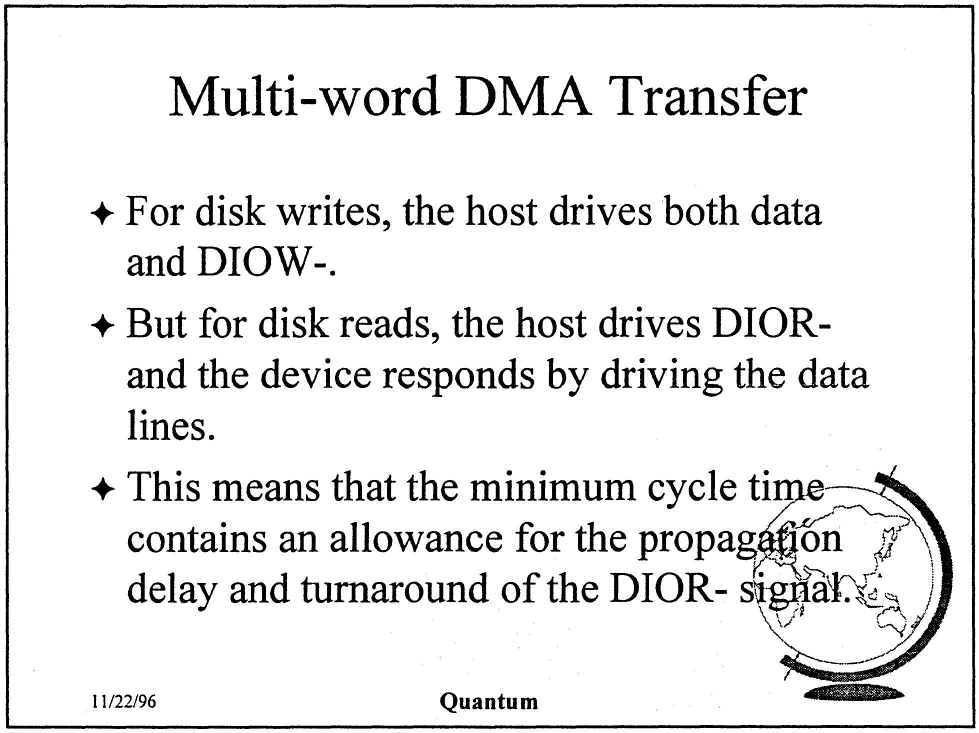
New protocol allows more efficient use of the bus than today's DMA

Higher data transfer rates can be obtained with the same analog plant in use today.

Minimizing analog changes increases speed of industry adoption (analog changes frequently take a long time for the industry to reliably implement).

Reliability enhanced by adding CRC checking.

The new protocol can also be used at 16MB/s to take advantage of its improved reliability compared with today's Mode 2 DMA



Multi-word DMA Transfer

- For disk writes, the host drives both data and DIOW-.
- But for disk reads, the host drives DIOR- and the device responds by driving the data lines.
- This means that the minimum cycle time contains an allowance for the propagation delay and turnaround of the DIOR- signal.

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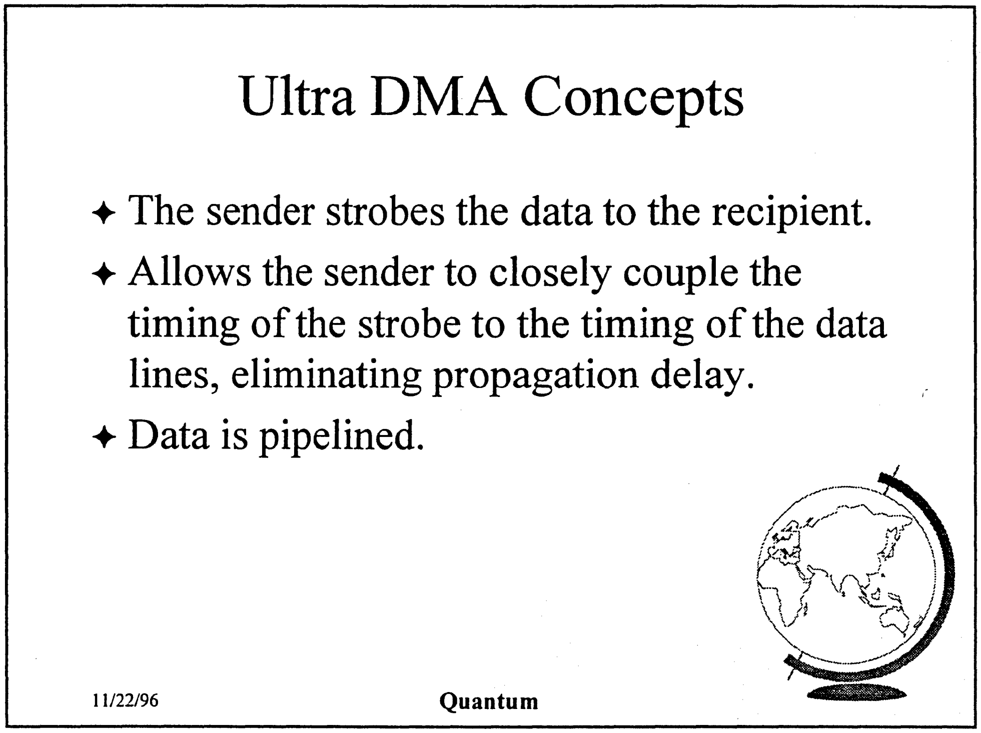
This limits the maximum transfer rate achievable with today's "analog plant."



Ultra DMA Concepts

- ✦ The sender strobes the data to the recipient.
- ✦ Allows the sender to closely couple the timing of the strobe to the timing of the data lines, eliminating propagation delay.
- ✦ Data is pipelined.

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A key difference between Ultra DMA transfers and the existing Multi-Word DMA is that the control signal which latches data into the receiving agent is generated by the same agent which drives the data bus. Ownership of the data bus and this strobe signal are given either to the device or the Host based on the command being a Read or a Write.

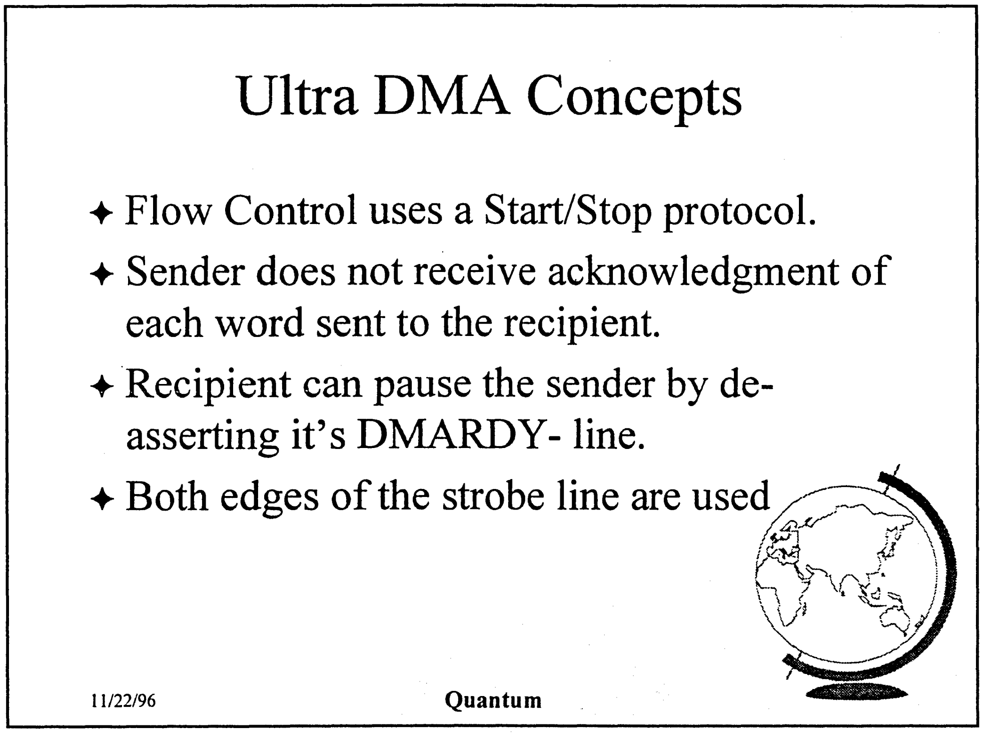
The sender sends the next word without receiving positive acknowledgment of receipt of the previous word from the recipient.

This eliminates propagation delay from the critical timings.

Fully backward compatible

PIO operations are unaffected.

New DMA must be activated by system with SET FEATURES.



Ultra DMA Concepts

- ✦ Flow Control uses a Start/Stop protocol.
- ✦ Sender does not receive acknowledgment of each word sent to the recipient.
- ✦ Recipient can pause the sender by de-asserting it's DMARDY- line.
- ✦ Both edges of the strobe line are used

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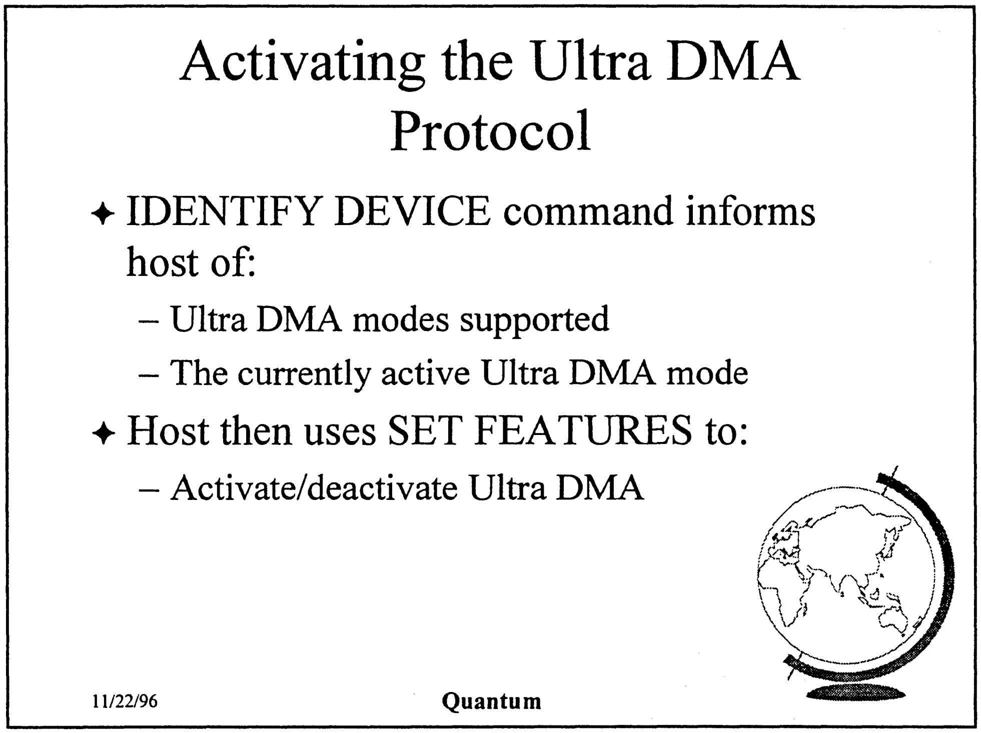
With CMOS drivers, both asserted and negated edges can have clean transitions.

This allows a doubling of transfer rate while maintaining the same transition frequency on DIOR- that the old protocol uses at 16 MB/s.



Activating the Ultra DMA Protocol

- ✦ IDENTIFY DEVICE command informs host of:
  - – Ultra DMA modes supported
  - – The currently active Ultra DMA mode
- ✦ Host then uses SET FEATURES to:
  - – Activate/deactivate Ultra DMA

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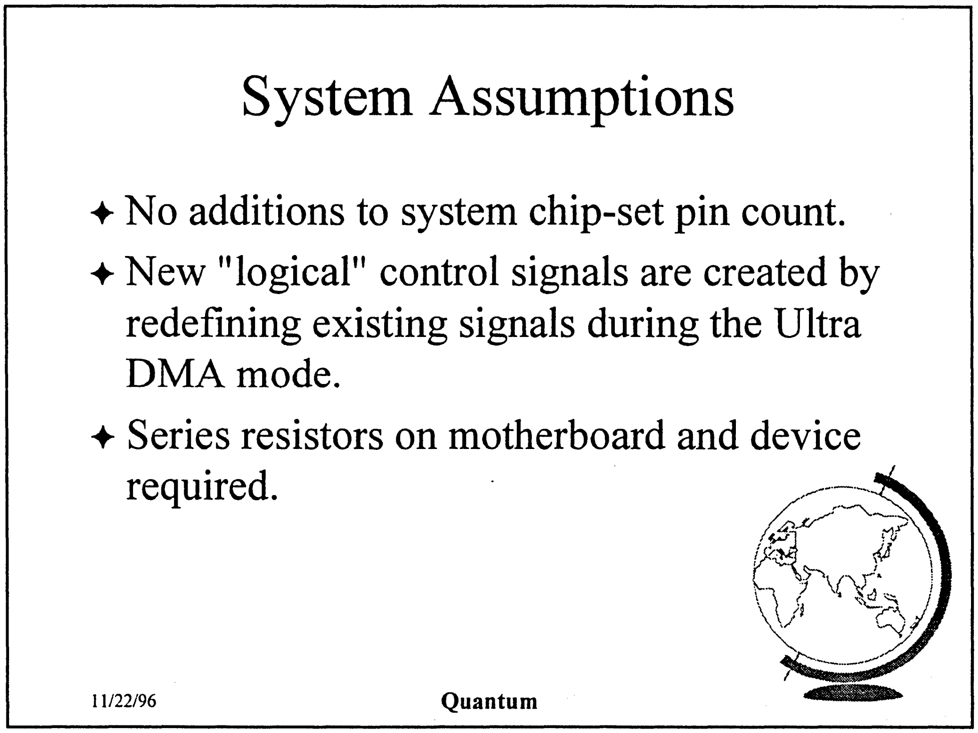
During system initialization, the host will query the device with the IDENTIFY DEVICE command, to determine if it has Ultra DMA capability. The device will also report all the modes it can support.

The host would then decide which mode it wants to operate in, and notify the device with a SET FEATURES command, as well as program the ATA bridge chip.

This process is repeated every power up/hard reset.



System Assumptions

- No additions to system chip-set pin count.
- New "logical" control signals are created by redefining existing signals during the Ultra DMA mode.
- Series resistors on motherboard and device required.

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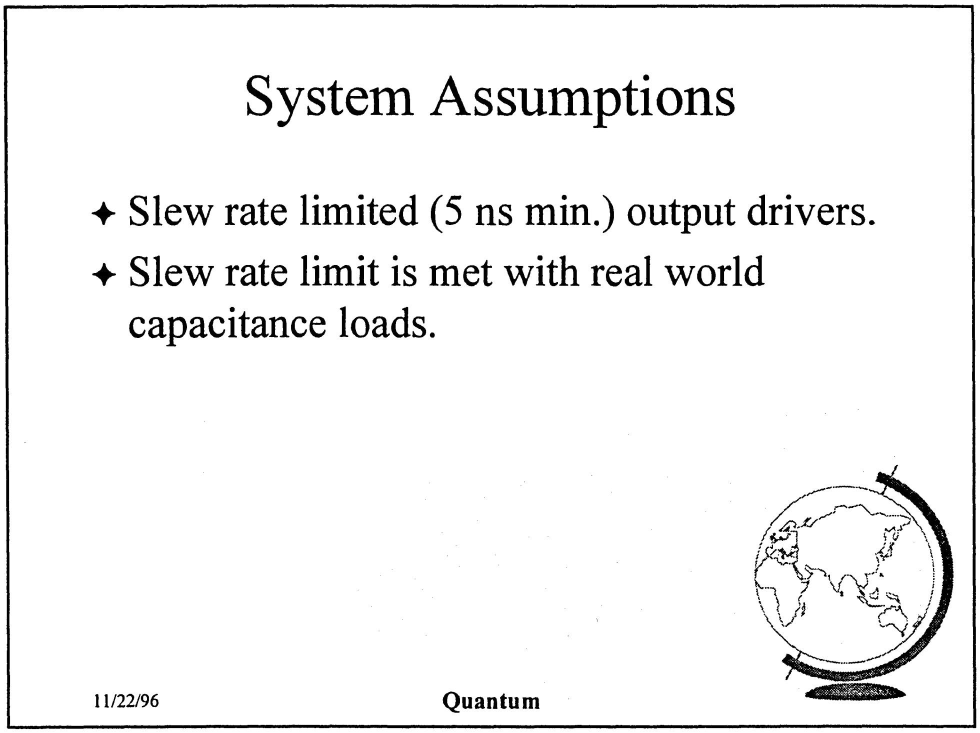


System Assumptions

- ✦ Slew rate limited (5 ns min.) output drivers.
- ✦ Slew rate limit is met with real world capacitance loads.

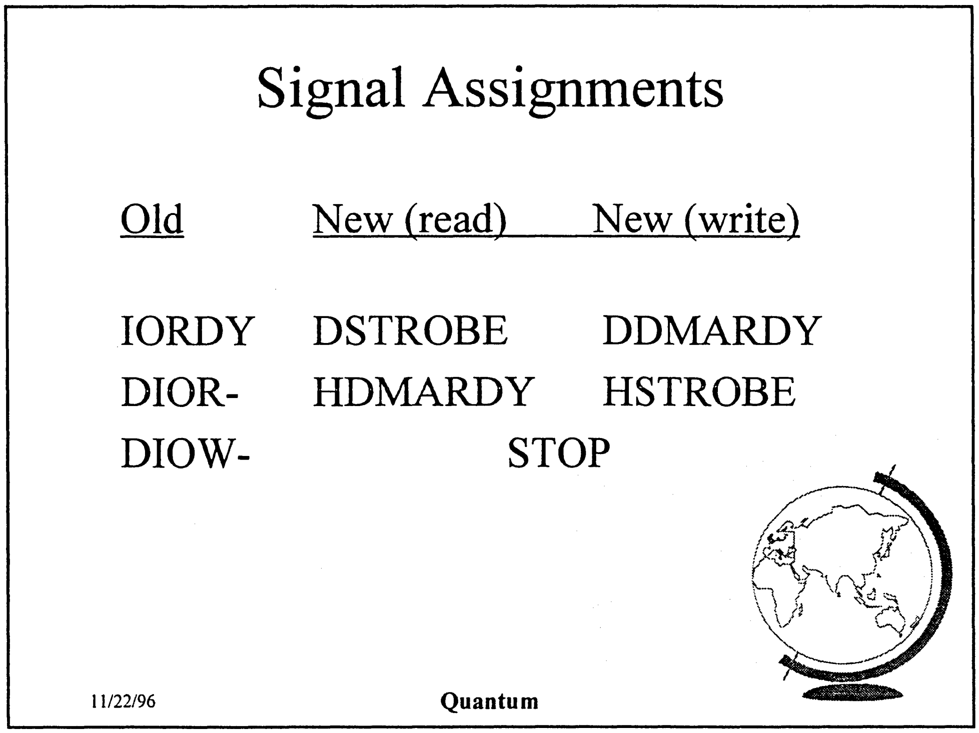
11/22/96 **Quantum**

Today's clock lines (DIOW- and DIOR-) work OK at 16MB/s

Negated edge of DIOR-/IORDY provides a clean signal

Data lines are shared between two ports

Data lines can settle within 33ns of driving



Signal Assignments

Old	New (read)	New (write)
IORDY	DSTROBE	DDMARDY
DIOR-	HDMARDY	HSTROBE
DIOW-	STOP	

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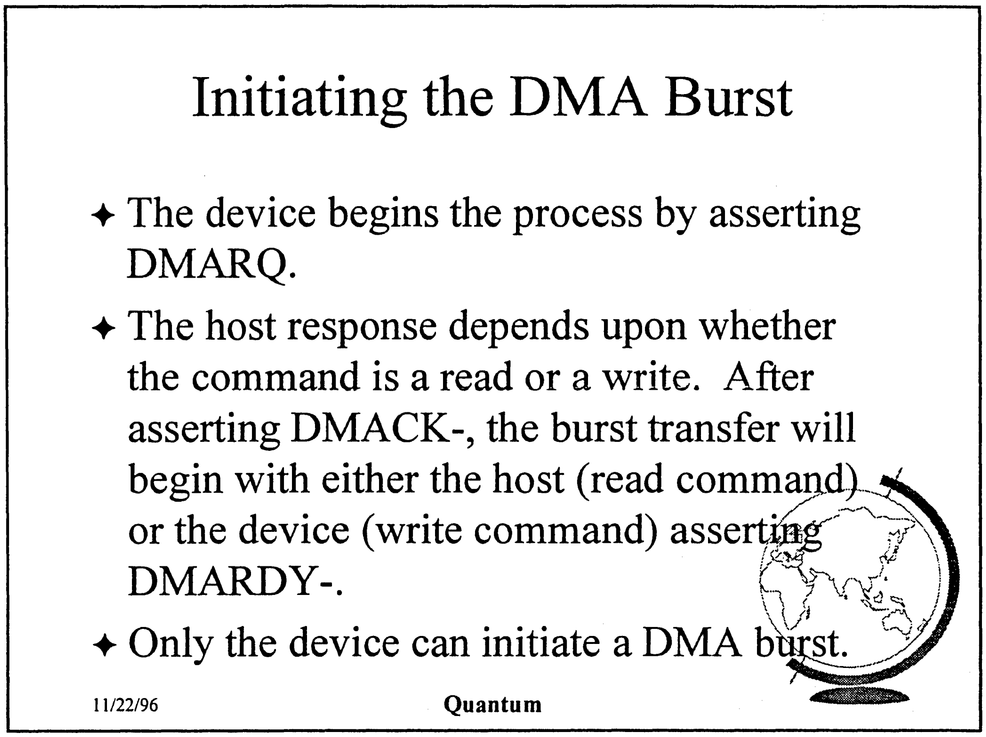
All of the control signals have been chosen such that they are uni-directional . This allows for a minimum of changes from the currently recommended series termination scheme on the ATA cable. DMARQ and DMACK- retain their current ATA definitions, while the remainder of the control signals use lines which already have another purpose, but are re-defined during a Ultra DMA Burst.

Note that DMARQ and DMACK- signals remain unchanged.



Initiating the DMA Burst

- ✦ The device begins the process by asserting DMARQ.
- ✦ The host response depends upon whether the command is a read or a write. After asserting DMACK-, the burst transfer will begin with either the host (read command) or the device (write command) asserting DMARDY-.
- ✦ Only the device can initiate a DMA burst.

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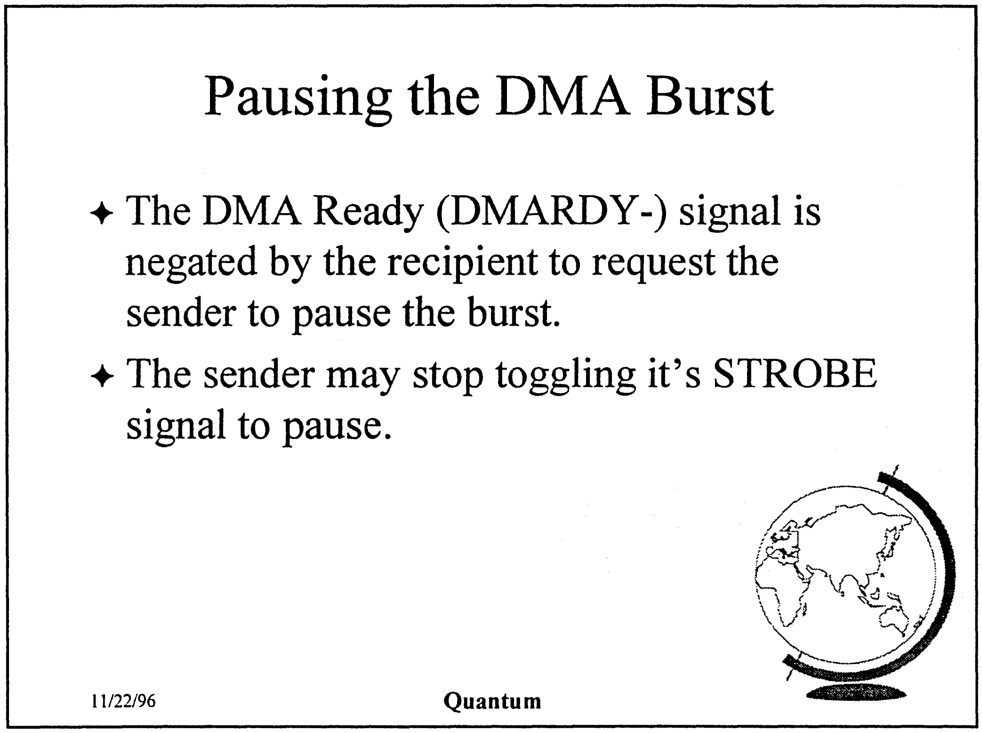
An ATA DMA command (DMA Read or DMA Write) would be accomplished through a series of Ultra DMA bursts. **Each Ultra DMA burst has 3 distinct phases of operation:**

1. **Start-up phase**
2. **Data transfer phase**
3. **Burst Termination**

The drive begins the burst by asserting DMARQ. The host responds by asserting DMACK-. For writes, the host deasserts STOP, drives the first data word and sends the first STROBE when the drive asserts DMARDY-. For reads, the host tri-states the data bus, and then deasserts STOP and asserts DMARDY- The drive then sends the first data word.

After the start-up phase, the owner of the strobe (host for DMA Writes, drive for DMA reads) sends data to the recipient by toggling the strobe (at the minimum period for the programmed mode), Tdvs ns after sending valid data. Note that both edges of STROBE are used to transfer data. The sender can pause the burst by not toggling the strobe (leaving it high or low.) The recipient pauses the burst by negating DMARDY-. The sender resumes a burst by sending strobes and the receiver resumes a burst by re-asserting -DMARDY.



Pausing the DMA Burst

- The DMA Ready (DMARDY-) signal is negated by the recipient to request the sender to pause the burst.
- The sender may stop toggling it's STROBE signal to pause.

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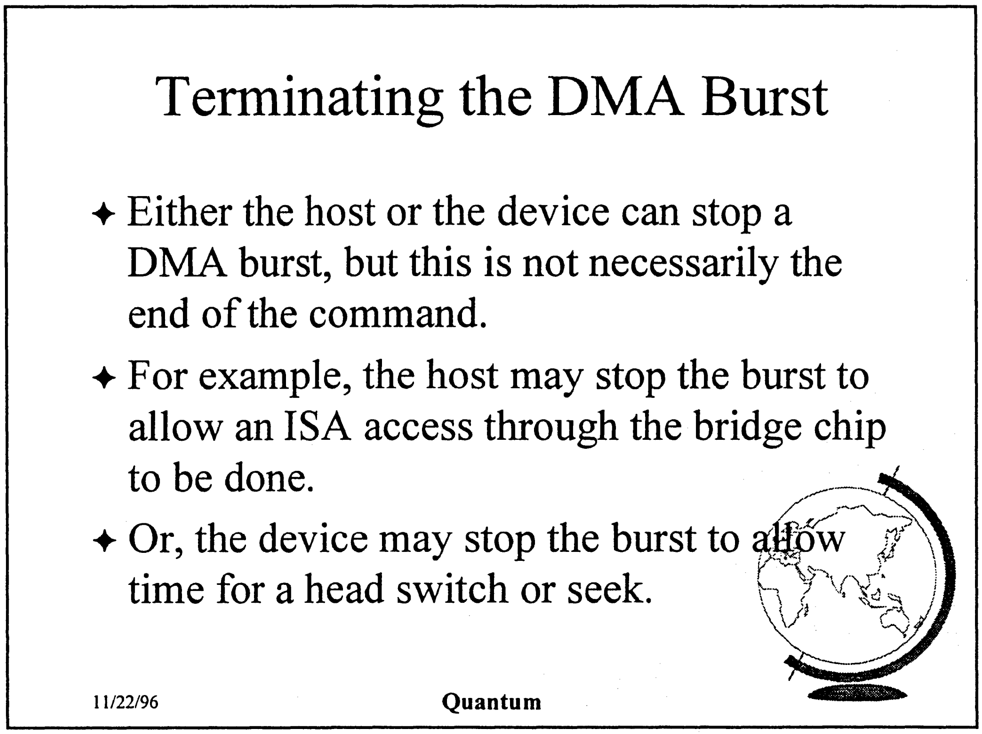
If the recipient negates DMARDY- following a transition on STROBE, then the burst will be paused with no more than 2 additional data transfers. (This type of pause is typical of a temporary "FIFO full" situation at the recipient.)

Note that the sender may pause the burst merely by stopping the transitions on the STROBE signal.

A pause may be followed by a burst termination. An example might be an ISA access through the bridge chip-requiring the burst to be first paused and then stopped.

The sender resumes a burst it has paused by transitioning STROBE again, and the recipient resumes a burst it has paused by re-asserting DMARDY-.



Terminating the DMA Burst

- ✦ Either the host or the device can stop a DMA burst, but this is not necessarily the end of the command.
- ✦ For example, the host may stop the burst to allow an ISA access through the bridge chip to be done.
- ✦ Or, the device may stop the burst to allow time for a head switch or seek.

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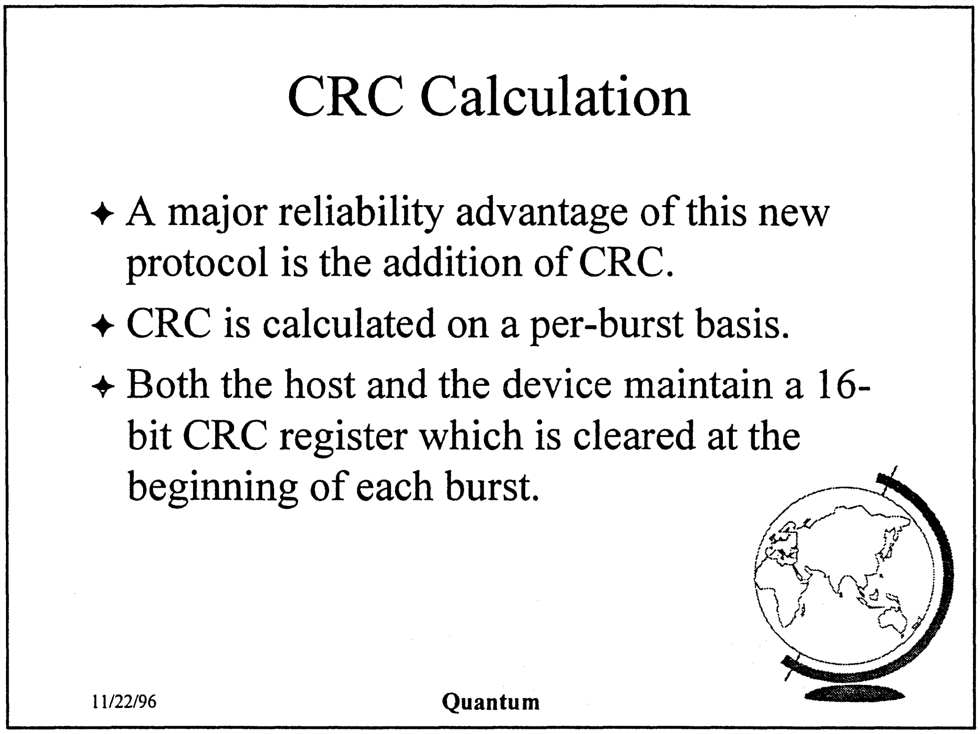
Either agent can stop a burst. Note this is not the same as ATA command termination; it is simply a termination of the current burst. The command will be resumed at some later time.

The host signals stop request by asserting STOP and the device signals stop request by negating DMARQ. The host acknowledges stop request by asserting STOP and the device acknowledges by negating DMARQ. The sender then returns the STROBE high if necessary. The host then sends the CRC data (for Reads **and** Writes) on the negation of DMACK-. At this point the device is free to request a new burst.



CRC Calculation

- A major reliability advantage of this new protocol is the addition of CRC.
- CRC is calculated on a per-burst basis.
- Both the host and the device maintain a 16-bit CRC register which is cleared at the beginning of each burst.

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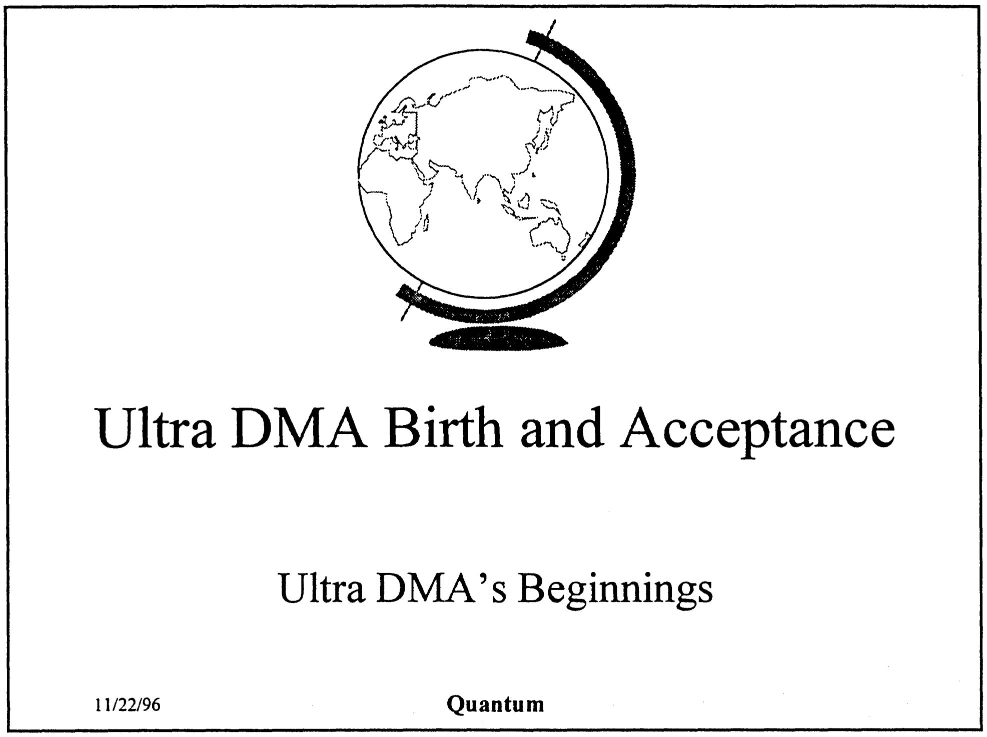
At the termination of each burst, the host sends the contents of its CRC register to the device with the negation of -DMACK.

The device must check the CRC data from the host with the CRC data it has calculated on the burst. These values must match.

If the two CRC values do not match, it is reported as a CRC error at the end of the command.



Ultra DMA Birth and Acceptance

Ultra DMA's Beginnings

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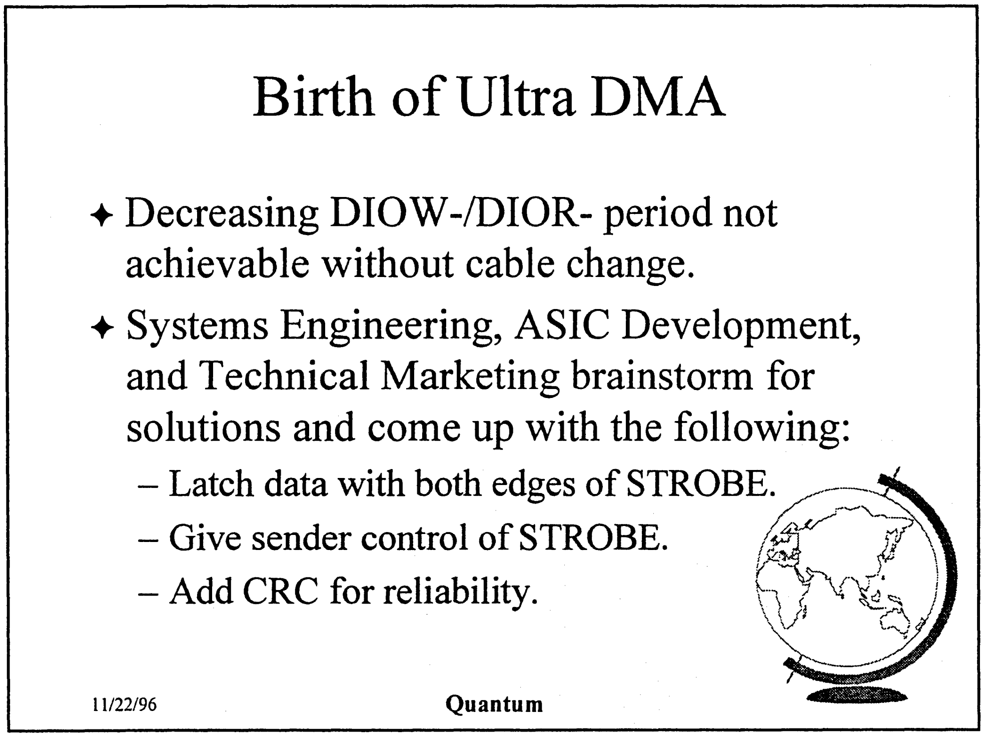

Birth of Ultra DMA

- ✦ Decreasing DIOW-/DIOR- period not achievable without cable change.
- ✦ Systems Engineering, ASIC Development, and Technical Marketing brainstorm for solutions and come up with the following:
  - – Latch data with both edges of STROBE.
  - – Give sender control of STROBE.
  - – Add CRC for reliability.

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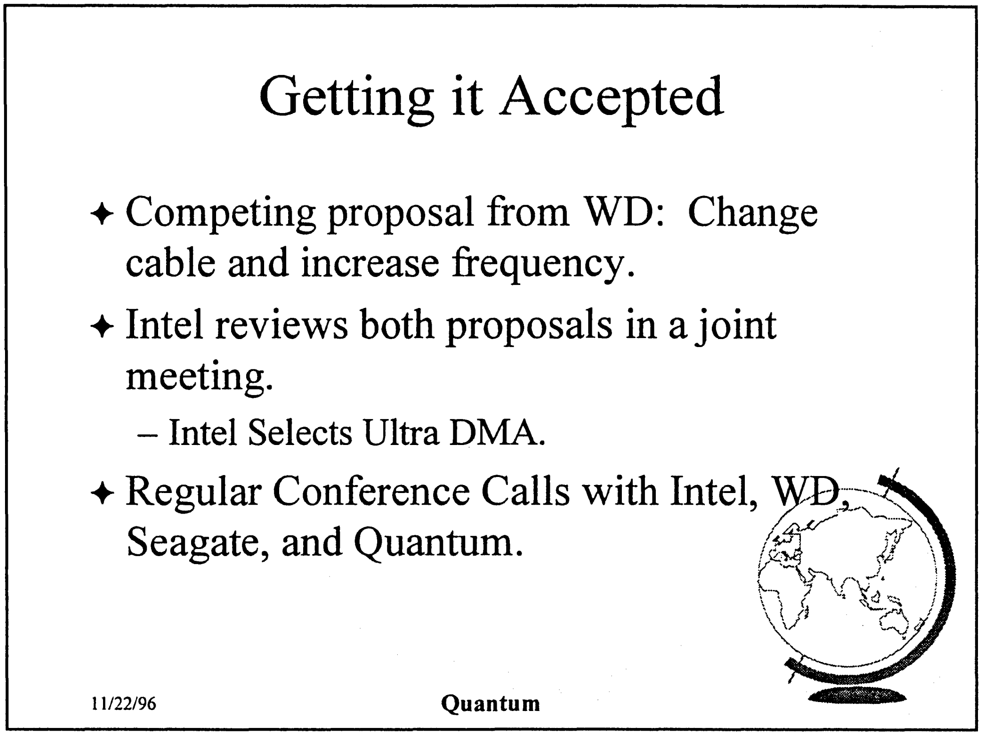

Getting it Accepted

- Competing proposal from WD: Change cable and increase frequency.
- Intel reviews both proposals in a joint meeting.
  - Intel Selects Ultra DMA.
- Regular Conference Calls with Intel, WD, Seagate, and Quantum.

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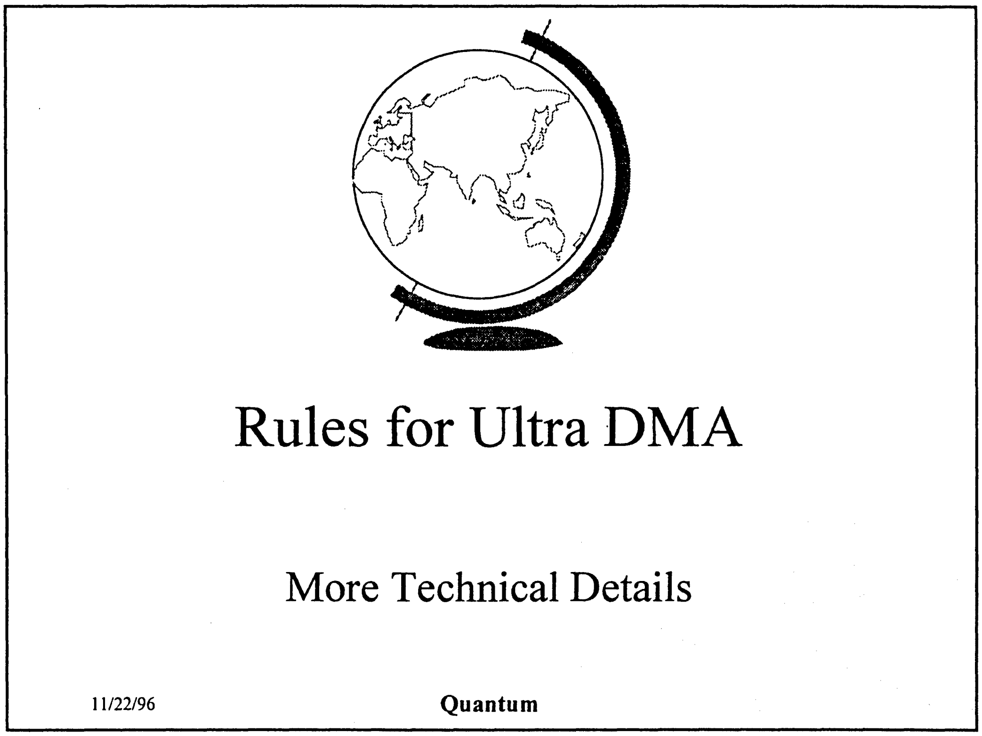

Rules for Ultra DMA

More Technical Details

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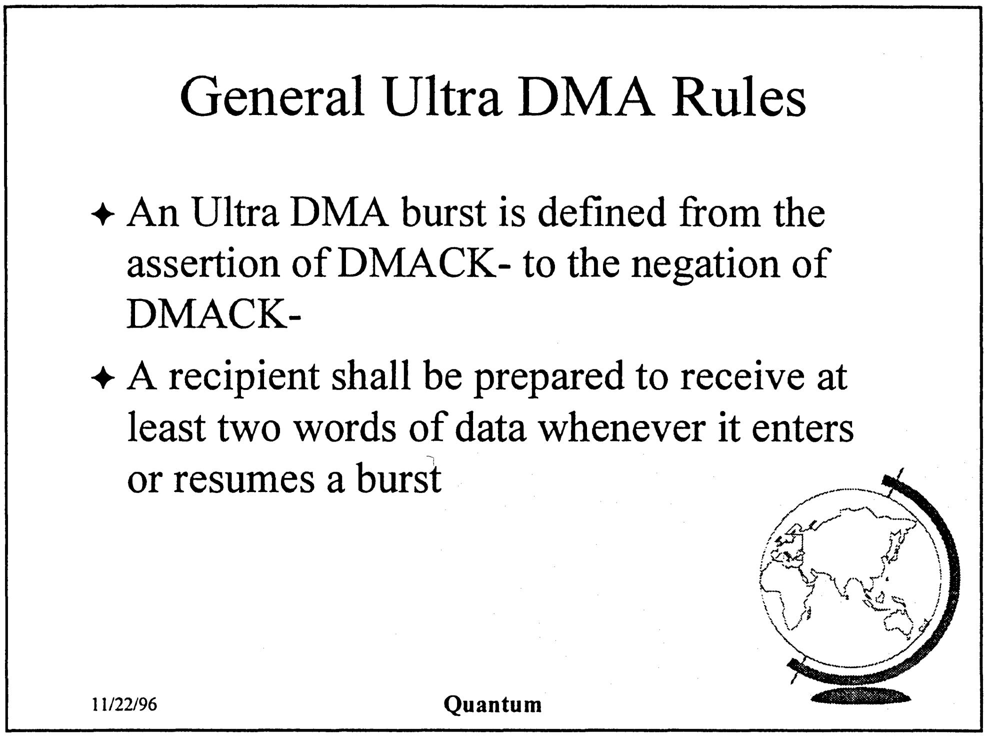

General Ultra DMA Rules

- An Ultra DMA burst is defined from the assertion of DMACK- to the negation of DMACK-
- A recipient shall be prepared to receive at least two words of data whenever it enters or resumes a burst

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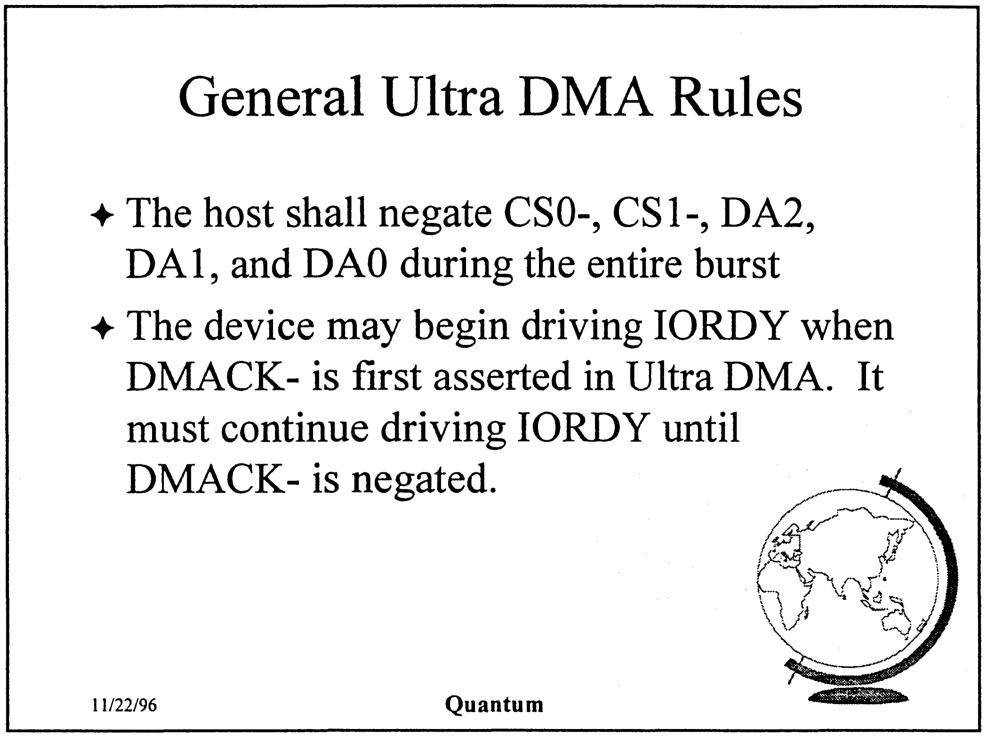
While it would always be a violation for the sender to generate two more strobes once DMARDY- is negated on it's side of the cable, it is still possible for the recipient that is attempting to pause the burst to see two more strobes after it negates DMARDY- without any violation of the protocol. This is because the sender may have already sent a STROBE transition that has not yet reached the recipient before the recipient negates DMARDY-.



General Ultra DMA Rules

- ✦ The host shall negate CS0-, CS1-, DA2, DA1, and DA0 during the entire burst
- ✦ The device may begin driving IORDY when DMACK- is first asserted in Ultra DMA. It must continue driving IORDY until DMACK- is negated.

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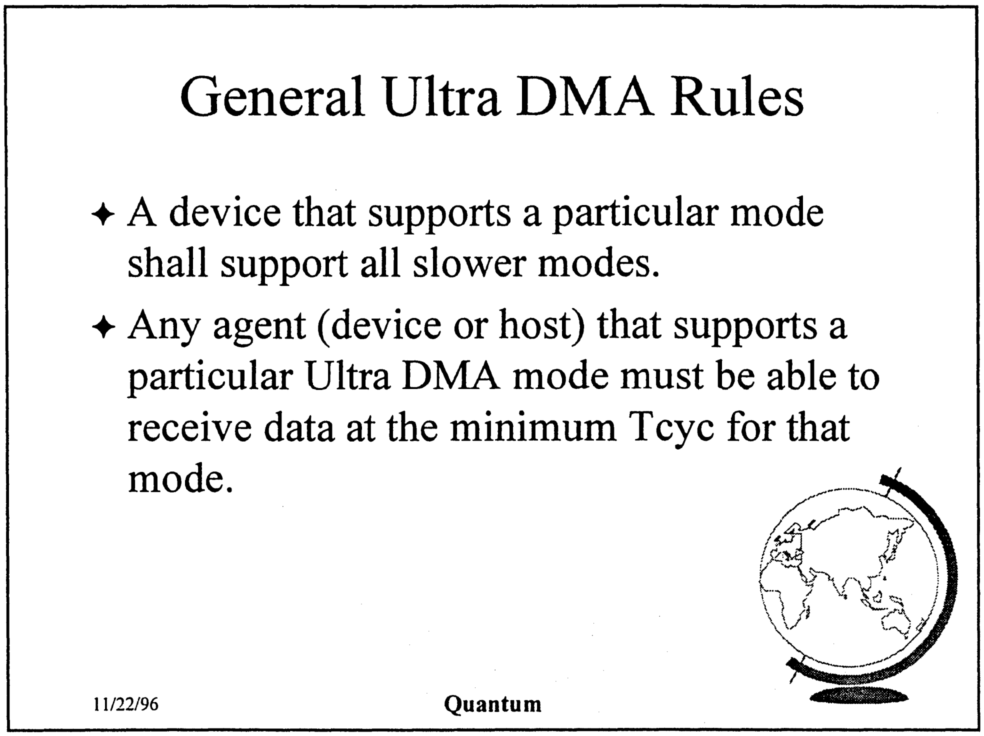

General Ultra DMA Rules

- A device that supports a particular mode shall support all slower modes.
- Any agent (device or host) that supports a particular Ultra DMA mode must be able to receive data at the minimum Tcyc for that mode.

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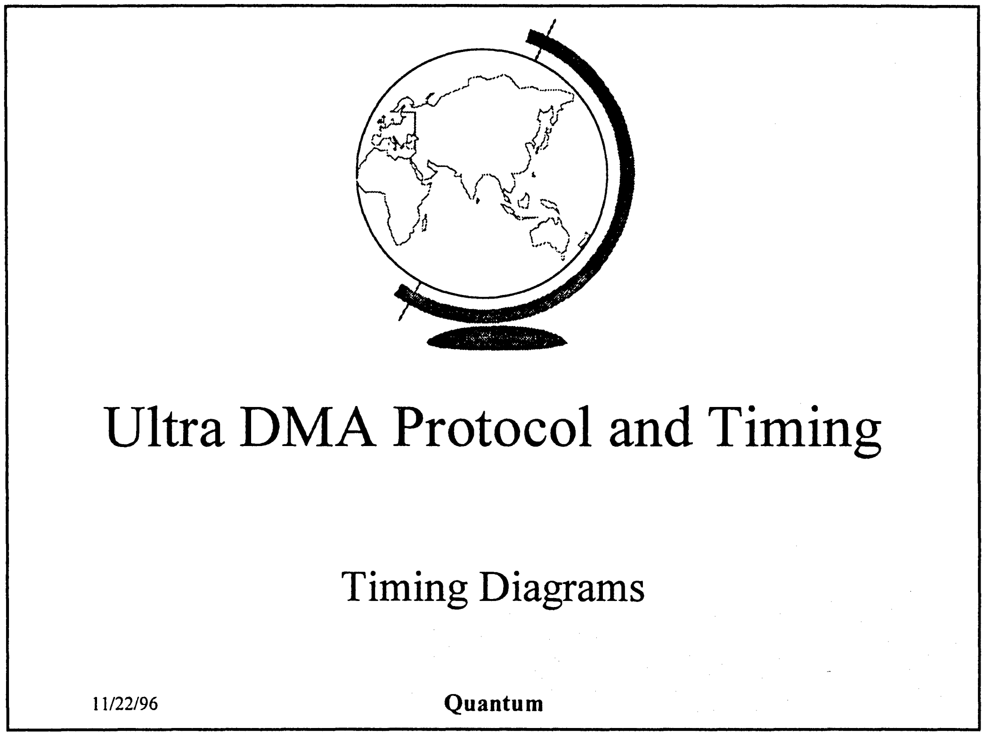

Ultra DMA Protocol and Timing

Timing Diagrams

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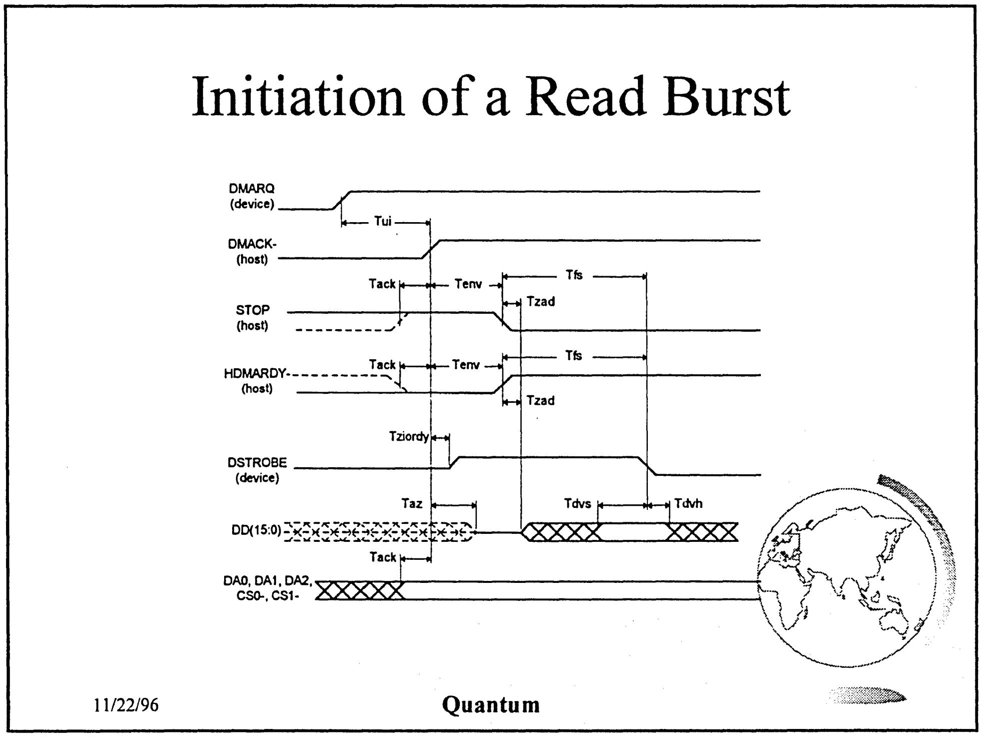

Initiation of a Read Burst

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Quantum

1)The host shall keep DMACK- in the negated state before the burst is initiated.

2)The device shall assert DMARQ to initiate a burst. After this assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE by the device.

3)The host shall assert STOP.

4)The host shall negate HDMARDY-.

5)The host shall negate CS0-, CS1-, DA2, DA1, and DA0.

6)Steps (3), (4) and (5) may occur in any order or at the same time and all shall occur at least Tack ns before continuing. When the host is ready to begin the requested burst, it shall assert DMACK-. The host shall keep DMACK- asserted until the end of the burst.

7)The host shall release DD(15:0) within Taz ns after asserting DMACK-.

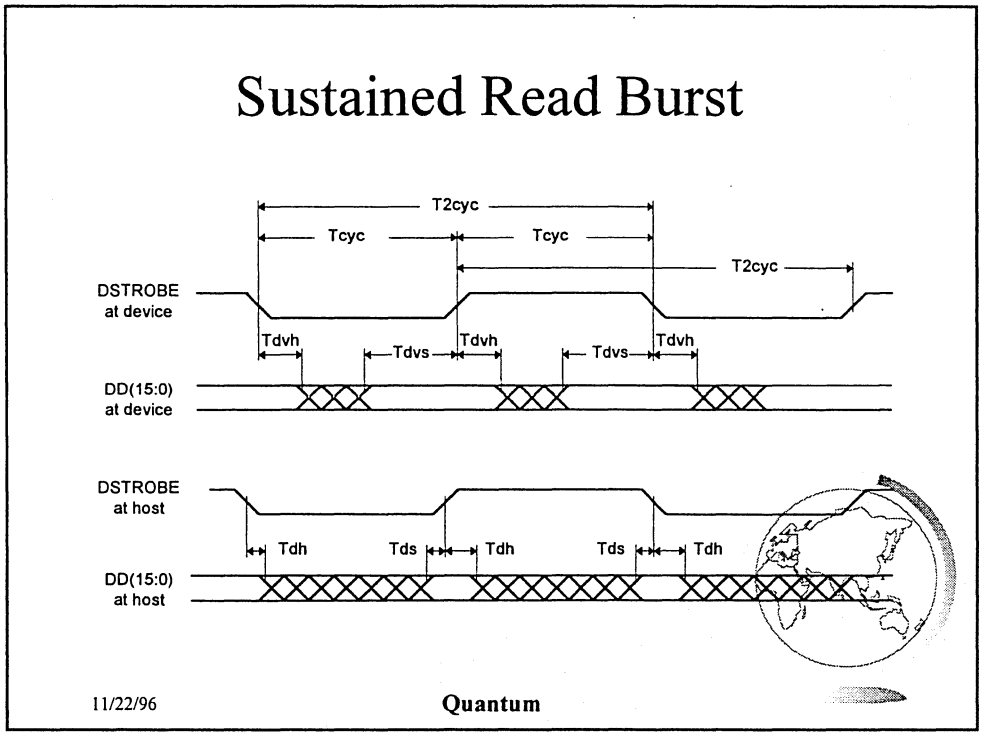
8)The device may assert DSTROBE Tziordy ns after the host has asserted DMACK-. Once the device has driven DSTROBE the device shall not release DSTROBE until the end of the burst.

9)The host shall negate STOP and assert HDMARDY- within Tenv ns after asserting DMACK-. After negating STOP and asserting HDMARDY-, the host shall not change the state of either signal until after receiving the first transition of DSTROBE from the device (i.e., after the first data word has been received).

10)The device shall drive DD(15:0) no sooner than Tzad ns after the host has asserted DMACK-, negated STOP, and asserted HDMARDY-.

11)The device shall drive the first word of the data transfer onto DD(15:0). This step may occur when the device first drives DD(15:0) in step (10).

12)To transfer the first word of data the device shall negate DSTROBE within Tfs ns after the host has negated STOP and asserted HDMARDY-. The device shall negate DSTROBE no sooner than Tdvs ns after driving the first word of data onto DD(15:0).



Sustained Read Burst

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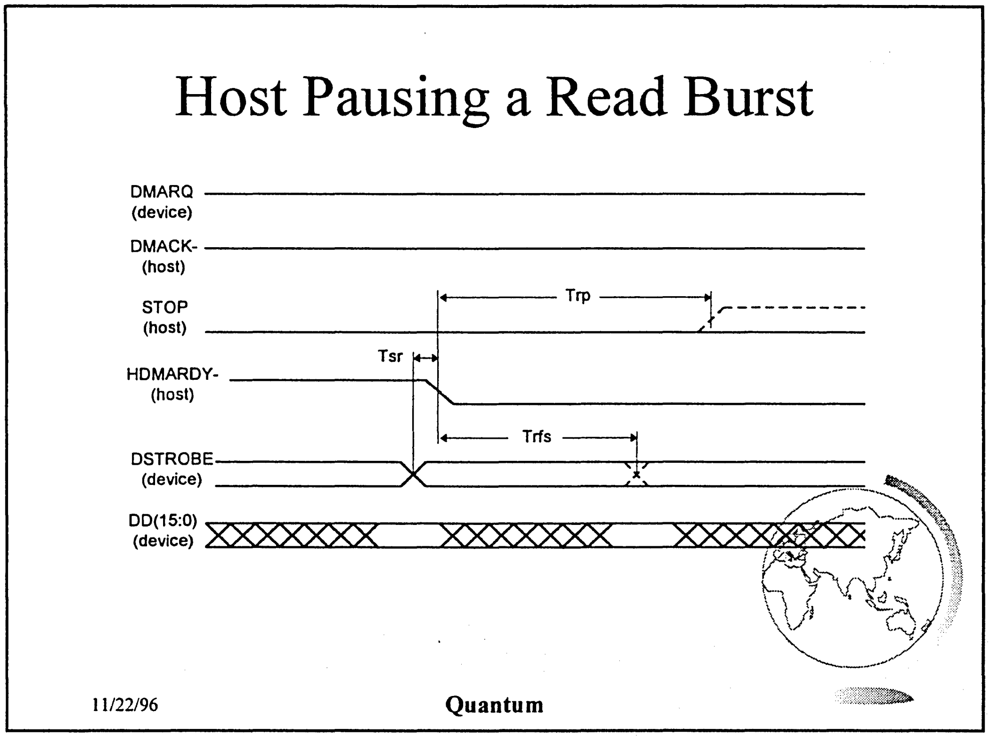
1)The device shall drive a data word onto DD(15:0).

2)The device shall toggle DSTROBE to latch the new word no sooner than Tdvs ns after changing the state of DD(15:0). The device shall toggle DSTROBE no more frequently than Tcyc ns for the currently active Ultra DMA mode.

3)The device shall not change the state of DD(15:0) until at least Tdvh ns after toggling DSTROBE to latch the data.

4)The device shall repeat steps (1), (2) and (3) until the data transfer is complete or the burst is paused, whichever occurs first.



Host Pausing a Read Burst

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Device pausing a read burst

1)The device shall not pause the burst until at least one data word of the burst has been transferred.

2)The device shall pause the burst by stopping its toggling of DSTROBE. The host shall never infer that a burst is paused because the device has stopped toggling DSTROBE.

3)The device shall resume the burst by toggling DSTROBE.

Host pausing a read burst

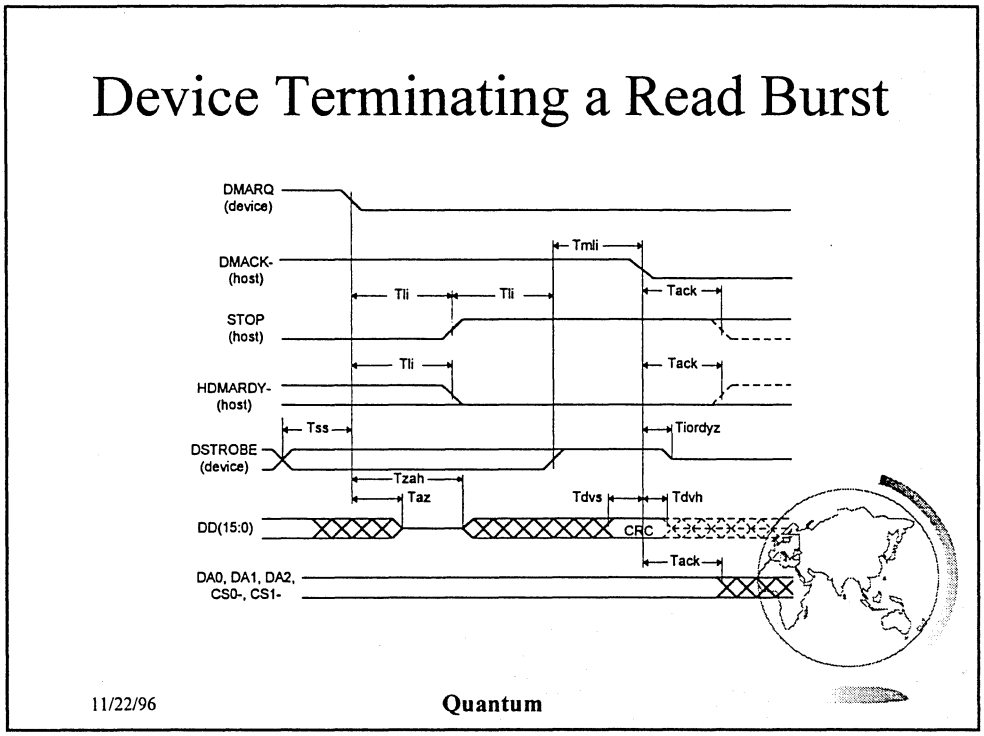
1)The host shall not pause the burst until at least one data word of the burst has been transferred.

2)The host shall pause the burst by negating HDMARDY-.

3)The device shall stop its toggling of DSTROBE within Trfs ns of the host negating HDMARDY-.

4)If the host negates HDMARDY- within Tsr ns after the device has toggled DSTROBE, then host shall be prepared to receive zero or one additional data words. If the host negates HDMARDY- greater than Tsr ns after the device has toggled DSTROBE, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and Trfs timing for the device. The host shall not assume the burst is paused until Trp after negating HDMARDY-.

5)The host shall resume the burst by asserting HDMARDY-.



Device Terminating a Read Burst

11/22/96 Quantum

1)The device shall initiate termination of the burst by stopping its toggling of DSTROBE.

2)The device shall negate DMARQ no sooner than Tss ns after the last toggle of DSTROBE. The device shall not assert DMARQ again until after the current burst is terminated.

3)The device shall release DD(15:0) no later than Taz ns after negating DMARQ.

4)The host shall assert STOP within Tli ns after the device has negated DMARQ. The host shall not negate STOP again until after the current burst is terminated.

5)The host shall negate HDMARDY- within Tli ns after the device has negated DMARQ. The host shall continue to negate HDMARDY- until the current burst is terminated. Steps (4) and (5) may occur at the same time.

6)The host shall drive DD(15:0) no sooner than Tzah ns after the device has negated DMARQ

7)If DSTROBE is negated, the device shall assert DSTROBE within Tli ns after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE.

8)The host shall place the result of its CRC calculation on DD(15:0). See section 9.w.5 for calculation of CRC. Step (8) may occur as soon as step (6).

9)The host shall negate DMACK- no sooner than Tmli ns after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated HDMARDY-, and no sooner than Tdvs ns after the host places the result of its CRC calculation on DD(15:0).

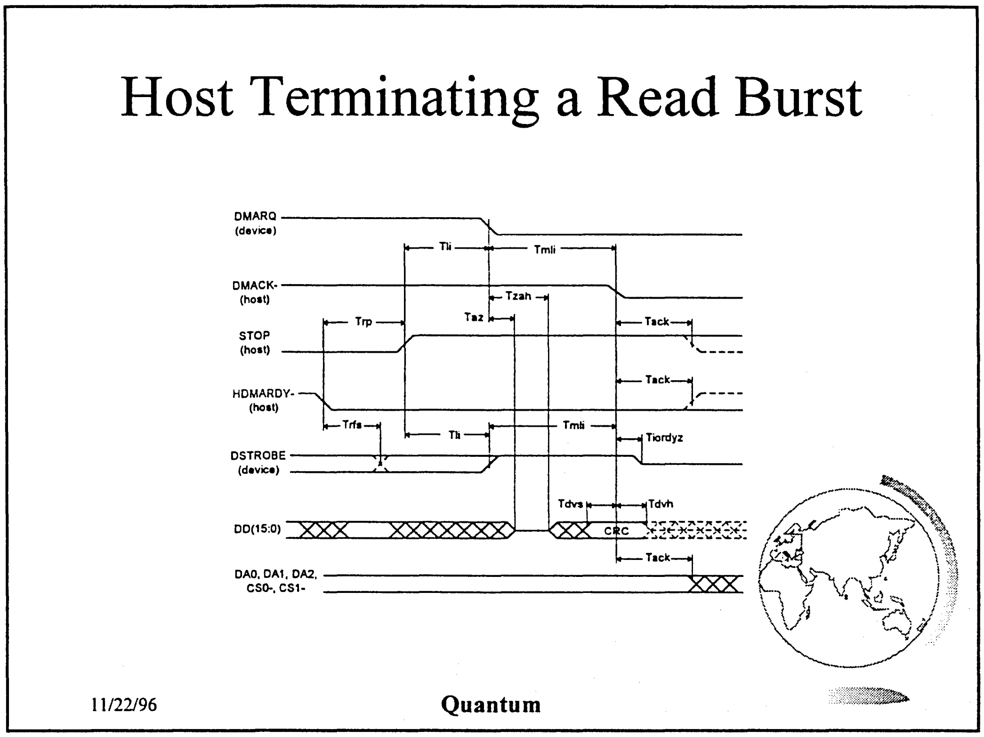
10)The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.

11)The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs, the device shall retain the fact that a miscompare error has occurred for reporting at the end of the command. See section 9.w.5 for calculation of CRC.

12)The device shall release DSTROBE within Tiordyz ns after the host negates DMACK-.

13)The host shall not negate STOP nor assert HDMARDY- until at least Tack ns after negating DMACK-.

14)The host shall not assert CS0-, CS1-, DA2, DA1, or DA0 until at least Tack ns after negating DMACK-.



Host Terminating a Read Burst

11/22/96

Quantum

1)The host shall not initiate burst termination until at least one data word of the burst has been transferred.

2)The host shall initiate burst termination by negating HDMARDY-.

3)The device shall stop its toggling of DSTROBE within Trfs ns of the host negating HDMARDY-.

4)If the host negates HDMARDY- within Tsr ns after the device has toggled DSTROBE, then the host shall be prepared to receive zero or one additional data words. If the host negates HDMARDY- greater than Tsr ns after the device has toggled DSTROBE, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and Trfs timing for the device. The host shall not assume the burst is paused until Trp ns after negating HDMARDY-.

5)The host shall assert STOP no sooner than Trp ns after negating HDMARDY-. The host shall not negate STOP again until after the current burst is terminated.

6)The device shall negate DMARQ within Tli ns after the host has asserted STOP. The device shall not assert DMARQ again until after the current burst is terminated.

7)If DSTROBE is negated, the device shall assert DSTROBE within Tli ns after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE.

8)The device shall release DD(15:0) no later than Taz ns after negating DMARQ.

9)The host shall drive DD(15:0) no sooner than Tzah ns after the device has negated DMARQ.

10)The host shall place the result of its CRC calculation on DD(15:0). See section 9.w.5 for calculation of CRC.

11)The host shall negate DMACK- no sooner than Tmli ns after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated HDMARDY-, and no sooner than Tdvs ns after the host places the result of its CRC calculation on DD(15:0).

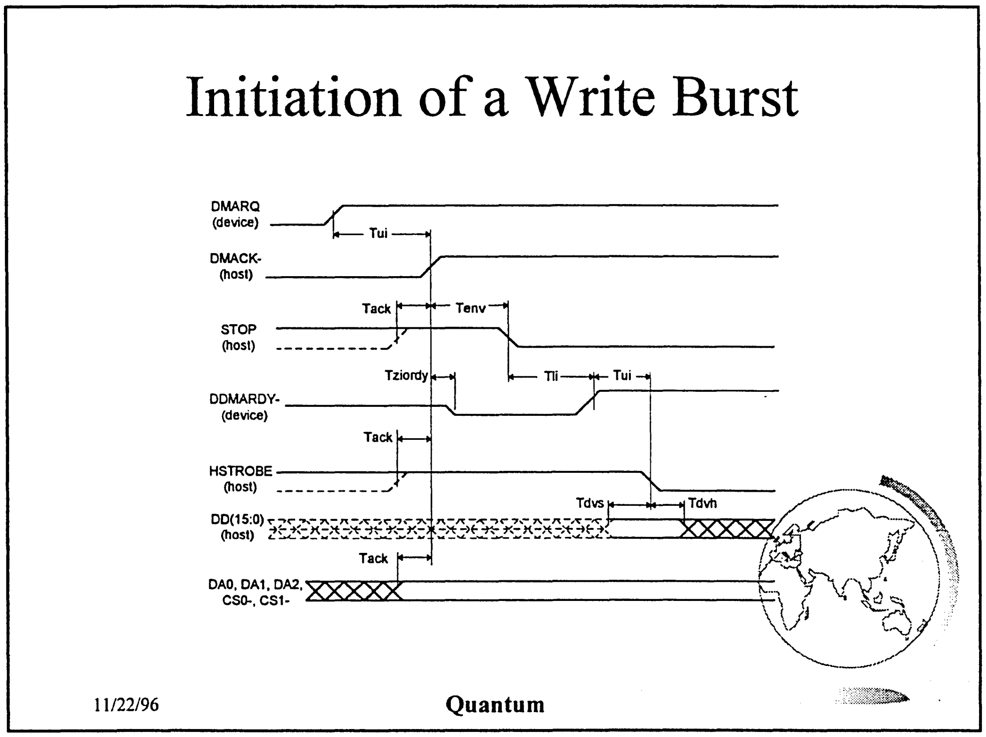
12)The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.

13)The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs, the device shall retain the fact that a miscompare error has occurred for reporting at the end of the command. See section 9.w.5 for calculation of CRC.

14)The device shall release DSTROBE within Tiordyz ns after the host negates DMACK-.

15)The host shall neither negate STOP nor assert HDMARDY- until at least Tack ns after the host has negated DMACK-.

16)The host shall not assert CS0-, CS1-, DA2, DA1, or DA0 until at least Tack ns after the host has negated DMACK-.



Initiation of a Write Burst

11/22/96 **Quantum**

1)The host shall keep DMACK- in the negated state before the burst is initiated.

2)The device shall assert DMARQ to initiate a burst.

3)The host shall assert STOP.

4)The host shall assert HSTROBE.

5)The host shall negate CS0-, CS1-, DA2, DA1, and DA0.

6)Steps (3), (4), and (5) may occur in any order or at the same time and all shall occur at least Tack ns before continuing. When the host is ready to begin the requested burst, it shall assert DMACK-. The host shall keep DMACK- asserted until the end of the burst.

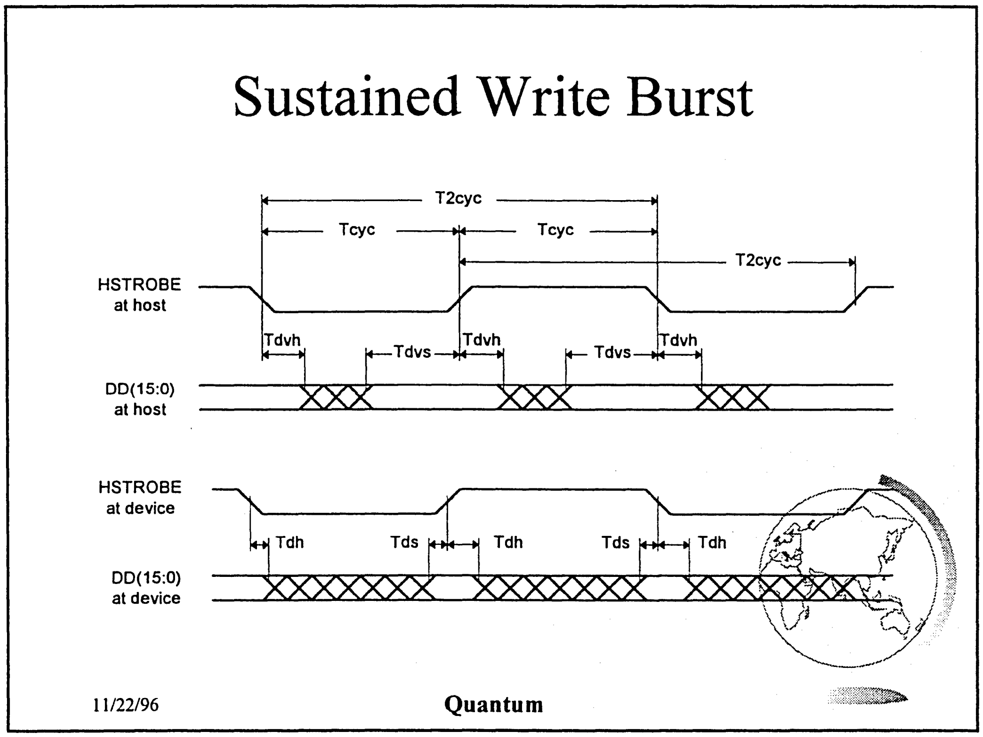
7)The device may negate DDMARDY- Tziordy ns after the host has asserted DMACK-. Once the device has negated DDMARDY-, the device shall not release DDMARDY- until the end of the burst.

8)The host shall negate STOP within Tenv ns after asserting DMACK-. The host shall not assert STOP until after the first negation of HSTROBE.

9)The device shall assert DDMARDY- within Tli ns after the host has negated STOP. After asserting DMARQ and DDMARDY- the device shall not negate either signal until after the first negation of HSTROBE by the host.

10)The host shall drive the first word of the data transfer onto DD(15:0). This step may occur any time during burst initiation.

11)To transfer the first word of data: the host shall negate HSTROBE no sooner than Tui ns after the device has asserted DDMARDY-. The host shall negate HSTROBE no sooner than Tdvs ns after the driving the first word of data onto DD(15:0).



Sustained Write Burst

11/22/96

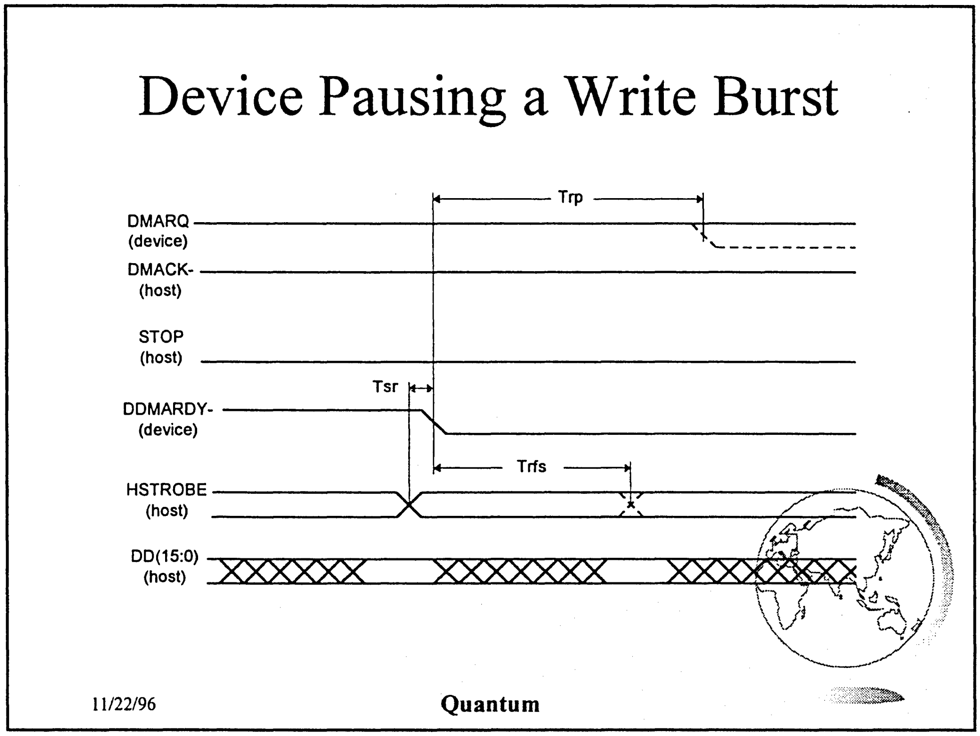
Quantum

1)The host shall drive a data word onto DD(15:0).

2)The host shall toggle HSTROBE to latch the new word no sooner than Tdvs ns after changing the state of DD(15:0). The host shall toggle HSTROBE no more frequently than Tcyc ns for the currently active Ultra DMA mode.

3)The host shall not change the state of DD(15:0) until at least Tdvh ns after toggling HSTROBE to latch the data.

4)The host shall repeat steps (1), (2) and (3) until the data transfer is complete or the burst is paused, whichever occurs first.



Device Pausing a Write Burst

11/22/96 Quantum

9.y.3.1 Host pausing a data out burst

1)The host shall not pause the burst until at least one data word of the burst has been transferred.

2)The host shall pause the burst by stopping its toggling of HSTROBE. The device shall never infer that a burst is paused because the host has stopped toggling HSTROBE.

3)The host shall resume the burst by toggling HSTROBE.

9.y.3.2 Device pausing a data out burst

1)The device shall not pause the burst until at least one data word of the burst has been transferred.

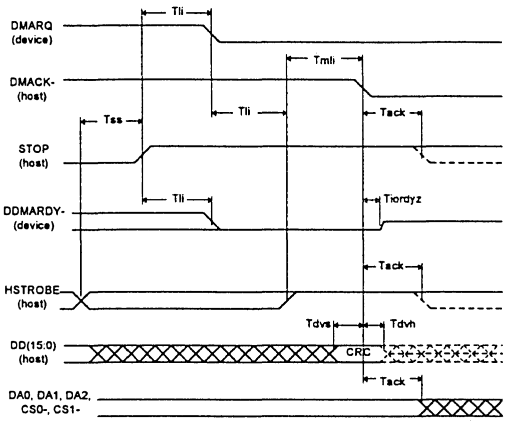
2)The device shall pause the burst by negating DDMARDY-.

3)The host shall stop its toggling of HSTROBE within Trfs ns of the device negating DDMARDY-.

4)If the device negates DDMARDY- within Tsr ns after the host has toggled HSTROBE, then the device shall be prepared to receive zero or one additional data words. If the device negates DDMARDY- greater than Tsr ns after the host has toggled HSTROBE, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and Trfs timing for the host. The device shall not assume the burst is paused until Trp ns after negating DDMARDY-.

5)The device shall resume the burst by asserting DDMARDY-.

Host Terminating a Write Burst



11/22/96

Quantum

1)The host shall initiate termination of the burst by stopping its toggling of HSTROBE.

2)The host shall assert STOP no sooner than Tss ns after it last toggled HSTROBE. The host shall not negate STOP again until after the current burst is terminated.

3)The device shall negate DMARQ within Tli ns after the host asserts STOP. The device shall not assert DMARQ again until after the current burst is terminated.

4)The device shall negate DDMARDY- within Tli ns after the host has negated STOP. The device shall not assert DDMARDY- again until after the current burst termination is complete.

5)If HSTROBE is negated, the host shall assert HSTROBE within Tli ns after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE.

6)The host shall place the result of its CRC calculation on DD(15:0). See section 9.w.5 for calculation of CRC.

7)The host shall negate DMACK- no sooner than Tmli ns after the host has asserted HSTROBE and STOP and the device has negated DMARQ and DDMARDY-, and no sooner than Tdvs ns after placing the result of its CRC calculation on DD(15:0).

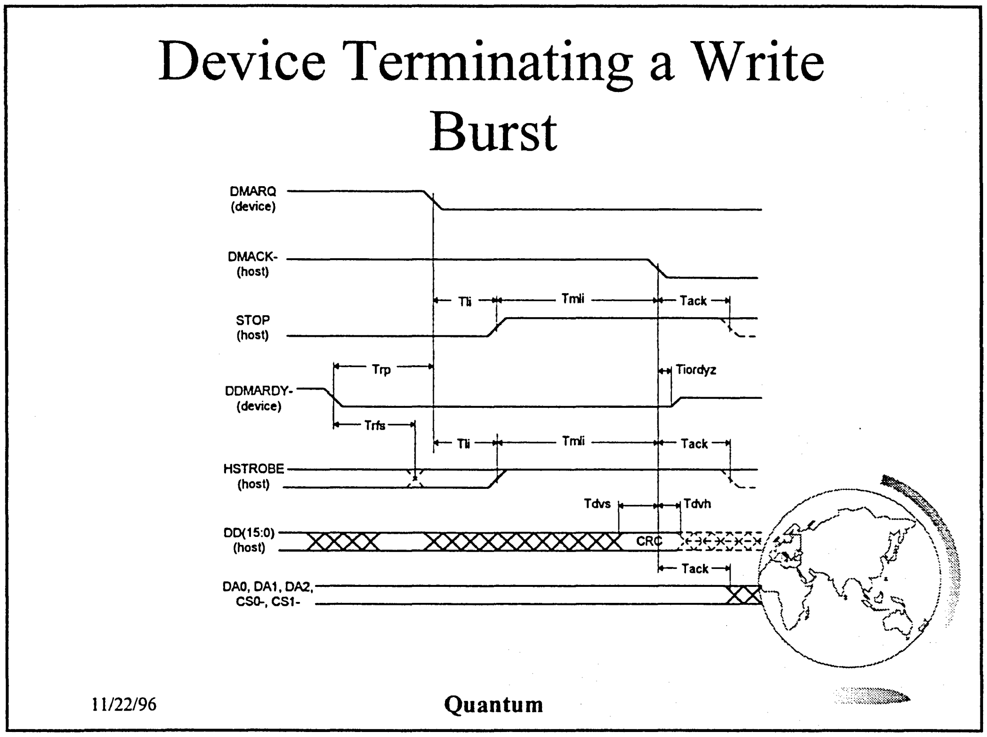
8)The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.

9)The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs the device shall retain the fact that a miscompare error has occurred for reporting at the end of the command. See section 9.w.5 for calculation of CRC.

10)The device shall release DDMARDY- within Tiordyz ns after the host has negated DMACK-.

11)The host shall neither negate STOP nor negate HSTROBE until at least Tack ns after negating DMACK-.

12)The host shall not assert CS0-, CS1-, DA2, DA1, or DA0 until at least Tack ns after negating DMACK-.



Device Terminating a Write Burst

11/22/96 **Quantum**

1)The device shall not initiate burst termination until at least one data word of the burst has been transferred.

2)The device shall initiate burst termination by negating DDMARDY-.

3)The host shall stop its toggling of HSTROBE within Trfs ns of the device negating DDMARDY-.

4)If the device negates DDMARDY- within Tsr ns after the host has toggled HSTROBE, then the device shall be prepared to receive zero or one additional data words. If the device negates DDMARDY- greater than Tsr ns after the host has toggled HSTROBE, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and Trfs timing for the host.

5)The device shall negate DMARQ no sooner than Trp ns after negating DDMARDY-. The device shall not assert DMARQ again until after the current burst is terminated.

6)The host shall assert STOP within Tli ns after the device has negated DMARQ. The host shall not negate STOP again until after the current burst is terminated.

7)If HSTROBE is negated, the host shall assert HSTROBE within Tli ns after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE.

8)The host shall place the result of its CRC calculation on DD(15:0). See section 9.w.5 for calculation of CRC.

9)The host shall negate DMACK- no sooner than Tmli ns after the host has asserted HSTROBE and STOP and the device has negated DMARQ and DDMARDY-, and no sooner than Tdvs ns after placing the result of its CRC calculation on DD(15:0).

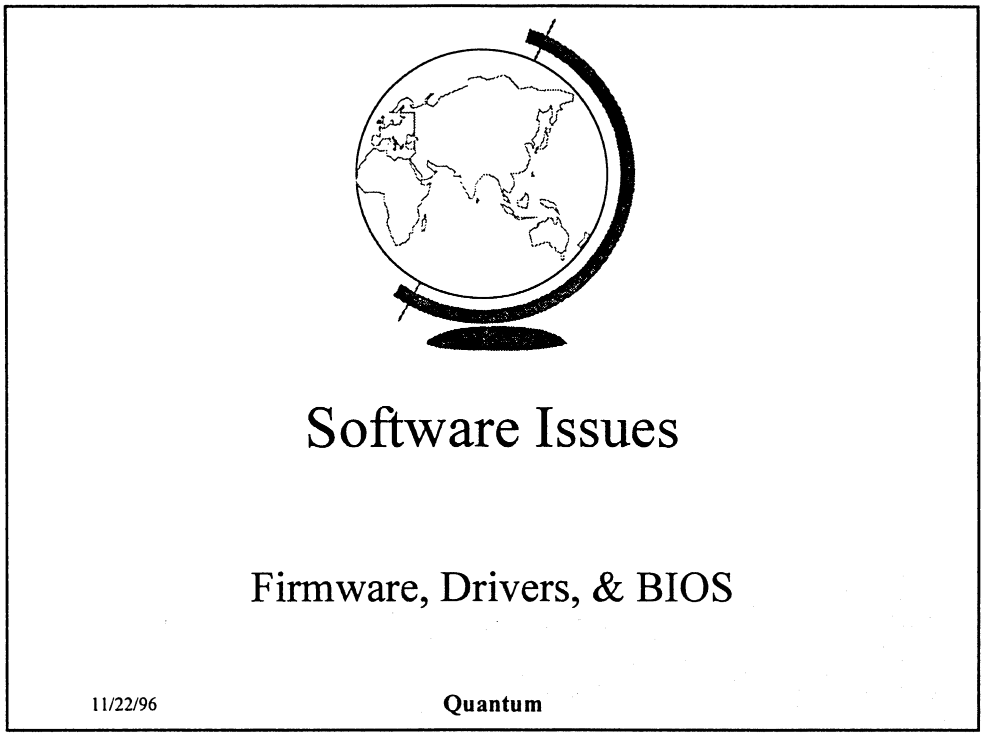
10)The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.

11)The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs the device shall retain the fact that a miscompare error has occurred for reporting at the end of the command. See section 9.w.5 for calculation of CRC.

12)The device shall release DDMARDY- within Tiordyz ns after the host has negated DMACK-.

13)The host shall neither negate STOP nor HSTROBE until at least Tack ns after negating DMACK-.

14)The host shall not assert CS0-, CS1-, DA2, DA1, or DA0 until at least Tack ns after the host has negated DMACK-.



Software Issues

Firmware, Drivers, & BIOS

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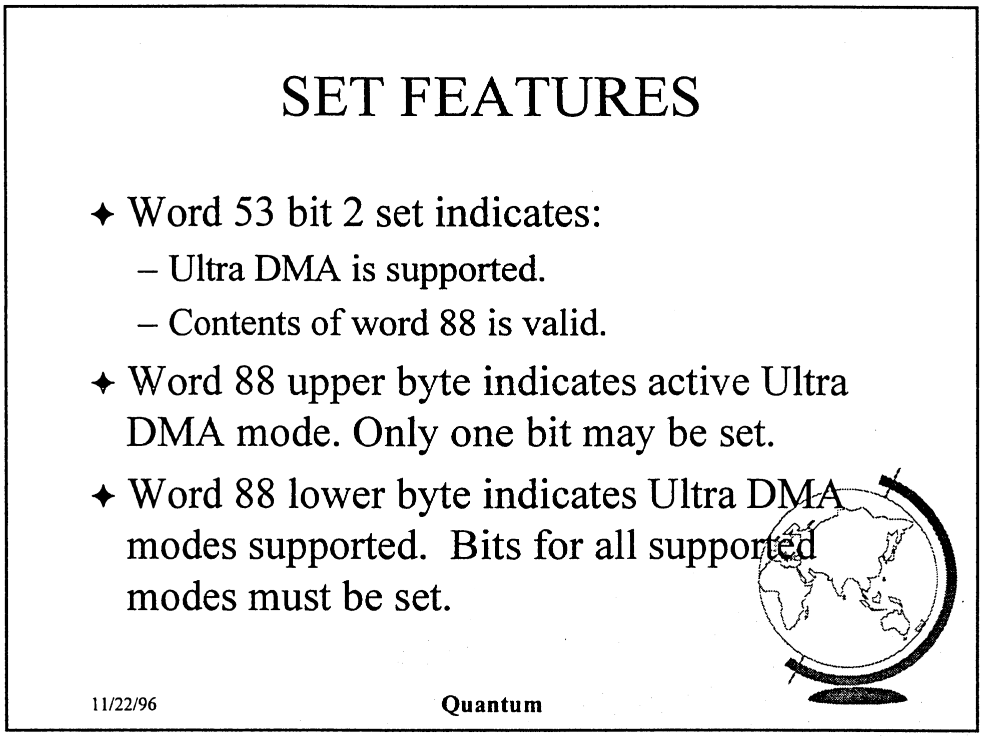

SET FEATURES

- Word 53 bit 2 set indicates:
  - Ultra DMA is supported.
  - Contents of word 88 is valid.
- Word 88 upper byte indicates active Ultra DMA mode. Only one bit may be set.
- Word 88 lower byte indicates Ultra DMA modes supported. Bits for all supported modes must be set.

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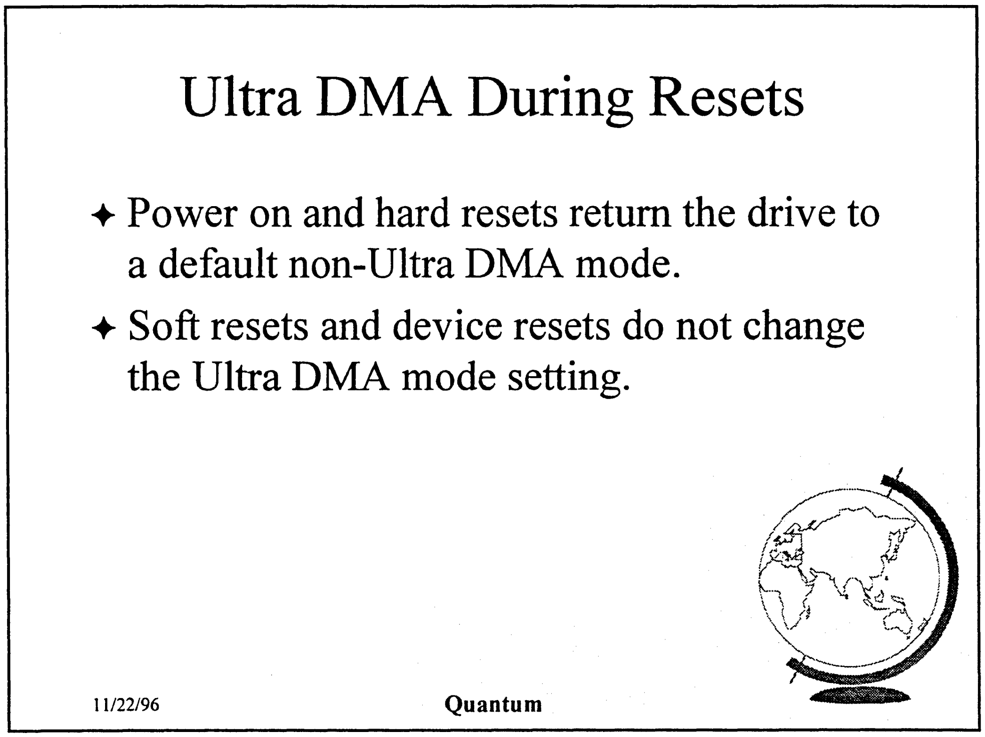

Ultra DMA During Resets

- ✦ Power on and hard resets return the drive to a default non-Ultra DMA mode.
- ✦ Soft resets and device resets do not change the Ultra DMA mode setting.

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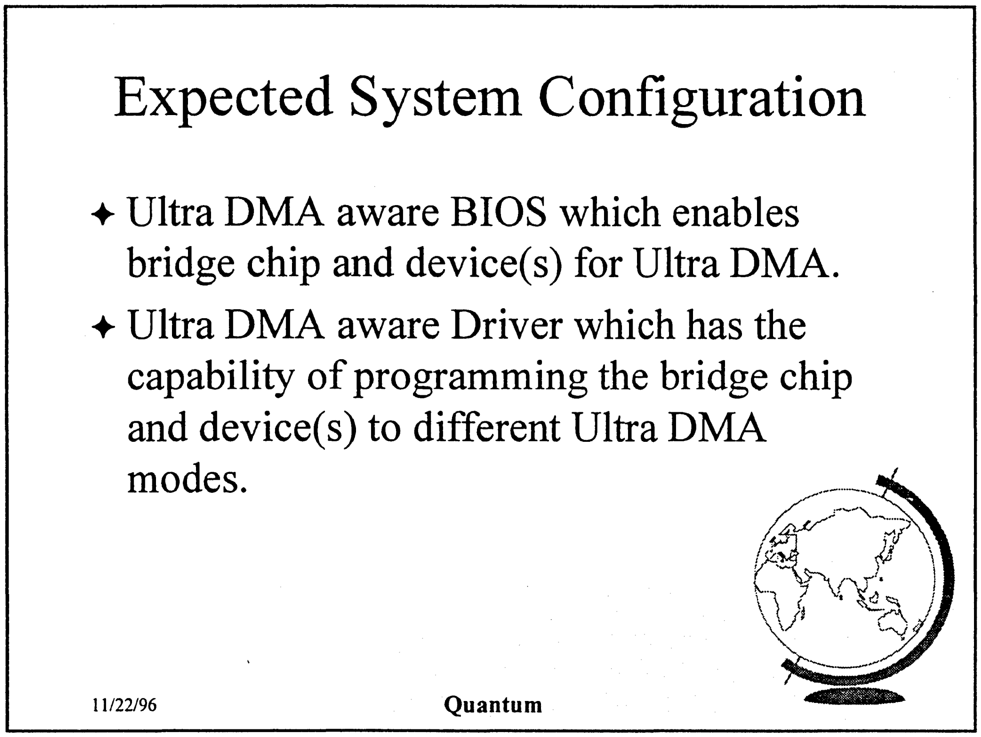

Expected System Configuration

- ✦ Ultra DMA aware BIOS which enables bridge chip and device(s) for Ultra DMA.
- ✦ Ultra DMA aware Driver which has the capability of programming the bridge chip and device(s) to different Ultra DMA modes.

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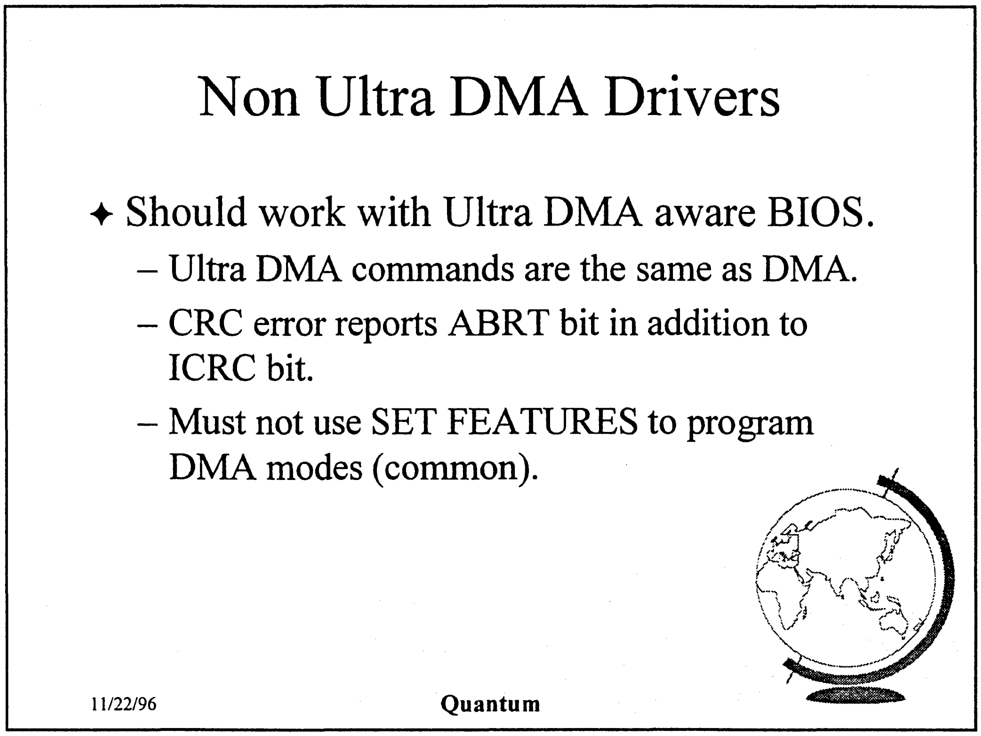

Non Ultra DMA Drivers

- ✦ Should work with Ultra DMA aware BIOS.
  - – Ultra DMA commands are the same as DMA.
  - – CRC error reports ABRT bit in addition to ICRC bit.
  - – Must not use SET FEATURES to program DMA modes (common).

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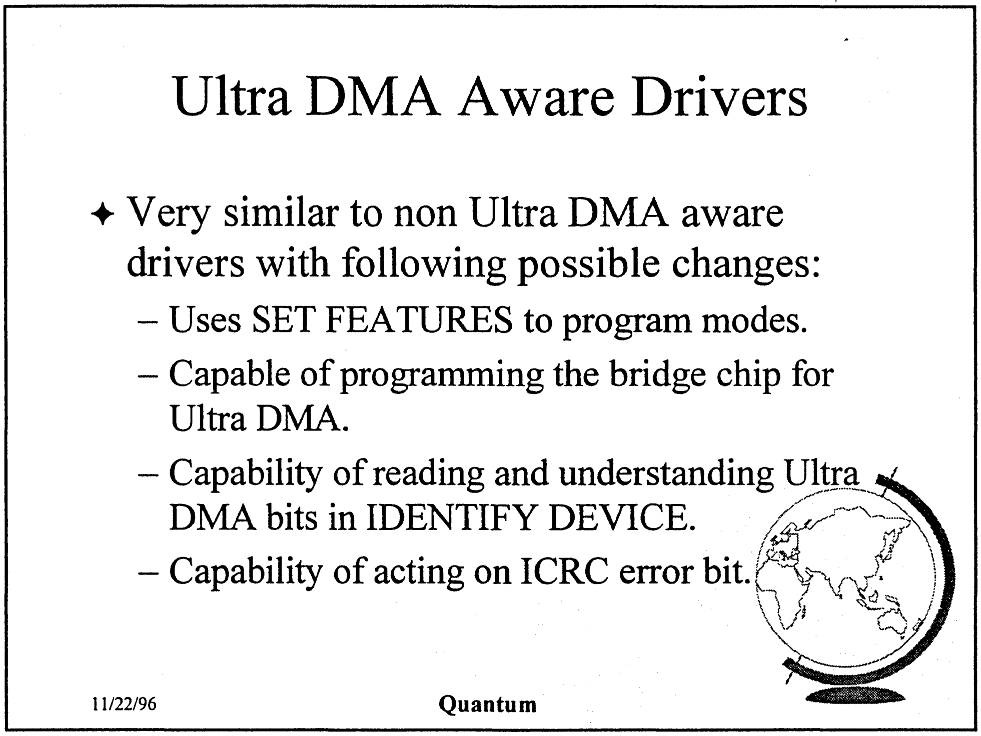

Ultra DMA Aware Drivers

✦ Very similar to non Ultra DMA aware drivers with following possible changes:

- Uses SET FEATURES to program modes.
- Capable of programming the bridge chip for Ultra DMA.
- Capability of reading and understanding Ultra DMA bits in IDENTIFY DEVICE.
- Capability of acting on ICRC error bit.

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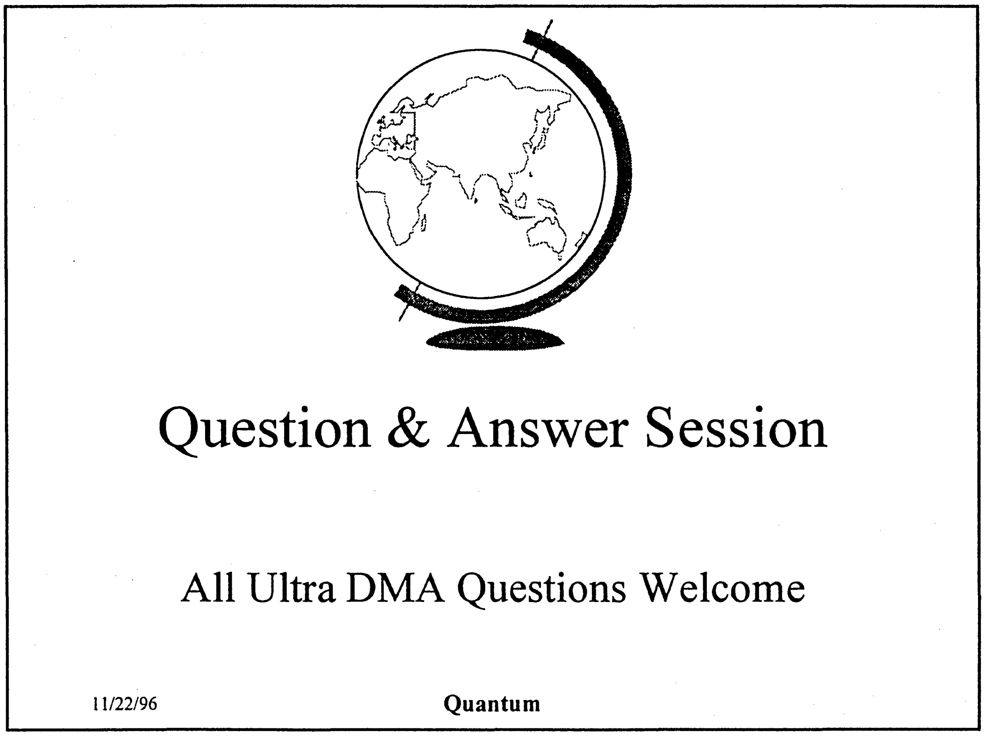

Question & Answer Session

All Ultra DMA Questions Welcome

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