The Stride 600/MSBC Series Supermicro
(A Technical Overview)

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ML0052A

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THE STRIDE 600/MSBC SERIES SUPERMICROCOMPUTER

(A TECHNICAL OVERVIEW)

The objective of the Stride 68020 R&D team was to design a computer based on a 68020 CPU which would be low-cost, fast, highly configurable, and able to operate asynchronously with multiple CPUs on a single VMEbus.

It was a further requirement that the design scheme not violate any VMEbus specification or UNIX standard.

The acronym "MSBC" or "Multi-function Single Board Computer" was chosen as the name for Stride's new product line because it best described the unique functionality of the product. Never before has a SBC been designed to be so fast and configurable. Since every MSBC is a complete computer in every respect, any given MSBC can be programmed as a system or as a controller. Therefore, a system can be logically configured in one of three ways:

1) *As a conventional single CPU system.* Since all disk, memory and serial I/O support is provided "on-board", no additional boards are required. This "uni-processor" architecture is common to the industry and typically found on systems offered by NCR, Altos, Sun, DEC and Convergent Technologies just to name a few.

2) *As a multi-processing system* with up to 14 single-board computers operating on a single VMEbus, each with its own disk, memory and serial I/O. Inter-system communications are supported using the industry standard TCP/IP which has been implemented over the VMEbus, affording speeds 400 percent greater than Ethernet.

3) *As a functionally distributed system* where, in addition to the main CPU, additional MSBC modules can be logically and physically dedicated to a specific task such as a disk or serial I/O controller, relieving the main CPU overhead. Accordingly, a typical system would use a MSBC as a CPU/system controller, a second MSBC as a serial I/O controller and a third MSBC as a disk I/O controller.

From a marketing viewpoint, the MSBC Series has been positioned as a 3rd generation 68020 which is highly programmable, configurable, and expandable to fit the needs of a wide variety of technical markets and programming environments.

Summary of Specifications

CPU:

A 16 MHz design using 100ns RAM is accessed in only 4 states.

MMU:

The Motorola 68851 PMMU supports all memory management and address translation functions for applications which require an MMU. No additional wait states are added for MMU operations.

RAM:

The Stride 600/MSBC main board contains 2MB or 4MB of parity RAM using 256K chips or optionally, 8MB or 16MB using 1MB RAM chips. A high-speed "local" bus interface and the use of a "sky" board will allow for further expansions up to 128MB RAM (using 4MB chips) on a system with a single sky expansion board. Since all RAM timing and control logic is "on-board" there is no need to access or load the VMEbus with memory I/O which would otherwise load the bus and add additional wait states.

STATIC RAM

128K bytes of 3-state static RAM has been provided for speed-critical functions. Certain operating system routines reside in this static RAM to further increase system performance.

SCSI interface:

The Stride 600/MSBC utilizes a SCSI interface to provide access to a maximum of 7 devices including floppy and hard disk drives, tape drives, and optical disk devices. This popular interface is very fast, allowing a continuous transfer from a 15MBit/sec and consuming a maximum of 35% of the available processor time.

The MicroSage-designed SCSI bus controller will drive SCSI peripherals at their maximum design capability while minimizing system loading. In addition to the availability of a wide variety of unusually large, and extremely fast disk and tape systems, an exclusive asynchronous mode provides a unique *reconnect* and *disconnect* feature which permits the operation of multiple drives in *parallel* on the SCSI bus. This parallel operation of the SCSI bus improves disk throughput and enhances file server performance.

ROM/CMOS RAM:

Support for 1 ROM and 1 CMOS RAM socket plus 4 more sockets which can be configured either as ROM or static RAM. This flexibility will allow configurations with up to 160K of CMOS RAM, or up to 320K of ROM. Power fail detection and battery back-up support is provided for all CMOS RAM.

Serial Ports:

Eight serial ports are included as standard. Each port can be configured at speeds of 50 - 38400 baud, and each port supports RTS, CTS, and CD. To protect the system from

accidental damage, each port is protected against spikes or surges through the use of clamping diodes and limiting resistors.

On-board decoding and interrupt control supports expansion for up to 40 serial ports through the use of inexpensive "sky" port boards. Each "sky" port board has 16 serial ports.

RTC:

The real-time clock is a battery backed-up CMOS clock which retains the system time even during power off or board shipment.

Network:

The local area network employed has been designed to be hardware compatible with the "MAP" network. It has been implemented using a Motorola token bus controller and the Motorola carrier band modem. The MAP network is expected to be very popular in the factory automation market. It offers a high data transfer rate (10MB/sec), and low installation cost and uses simple 75 ohm coax cabling.

There are no other known single board computers, 68020 or otherwise, which contain an onboard "MAP" type network with a high-speed DMA interface.

Monitoring:

Built-in diagnostics monitor +5v, +12v, -12v, battery back-up voltage, the optional standby battery voltage, the temperature, and air flow over the board. These outputs can be monitored under program control or remotely using a modem.

Parallel Processing:

The MSBC will operate in either bus master or bus slave modes of operation. When the MSBC is not specifically requesting the VME bus, it will leave it free for others to use. The basic scheme will allow up to 14 MSBC/CPU boards to be utilized on the same bus at once. The large on-board ROM space will allow a second board in a system to be used as a powerful I/O processor.

Reliability:

The 600 Series has been designed from the ground up to be extremely reliable. The serial lines are protected from normal static discharges; even plugging a serial cable into the 220v mains will only blow the protection fuses for that port - the rest of the system will be not be affected. CMOS logic will be used throughout most of the system providing high noise margins and low power dissipation. Where appropriate, signal lines will be of controlled impedance and terminated to further reduce system noise. The air flow and temperature monitoring will help insure that the system is operating within its design parameters.

Upgrade Path:

The MSBC has been designed using the same form-factor as the Stride 400 Series. Specifically, this will permit the company to offer UNIX 68020 upgrades to over 4000 installed

systems.

VMEbus Architecture: A full VMEbus with all 7 levels of interrupt has been
                                    implemented. A maximum configuration holds up to 14
                                    logically isolated CPU boards mounted on a single VMEbus,
                                    with each operating autonomously *either* as bus master or as
                                    bus slave. A message passing communication protocol is
                                    used between computer boards over the VMEbus for speed.
                                    The VMEbus supports a raw data rate of 80MB/sec with
                                    expected actual throughput calculated at 10MB/sec, which
                                    offers significant performance advantages over other com-
                                    munications schemes such as Ethernet.

400 Series 68020

The Stride 600/MSBC follows the introduction of the Stride 400/68020 Series which was
specifically designed and targeted at the p-System, PDOS and Pick markets. The timed
introduction of the 600/MSBC UNIX-based product line has given the company an oppor-
tunity to design and introduce a more advanced 3rd generation 68020 system which incor-
porates design schemes and related technologies which are more technically advanced than
conventional 68020 offerings.