PDP-5/SDS-930 COMMUNICATIONS LINK

R-16

PMIJ

PROGRAMMER'S GUIDE

Gary D. Hornbuckle

University of California, Berkeley

Document No. 20.50.20 Issued May 5, 1965 Revised July 11, 1966 Contract SD-185 Office of Secretary of Defense Advanced Research Projects Agency Washington 25, D. C.

# TABLE OF CONTENTS

1.0	Introduction	1							
2.0	Initiation of a Transmission Cycle								
3.0	Transmit/Receive Cycle (T/R Cycle)	3							
4.0	Leaving Transmit Mode	4							
	4.1 Panic Conditions	4.							
5.0	Link Instructions	5							
	5.1 SDS End	5							
	5.1.1 Interrupt Locations	5							
	5.1.2 Interrupt Control	6							
	5.1.3 Link Select (Transmit Request, End Transmission, Etc	7							
	5.1.4 DMC Programming	8							
	5.1.5 Skip Instructions 1	1							
	5.2 PDP-5 End	1							
	5.2.1 Interrupt Locations 1	1							
	5.2.2 Interrupt Control	2							
	5.2.3 Link Select (Transmit Request, End Transmission)	.3							
	5.2.4 Read In/Out, Skip 1	.4							
6.0	IOT Command Combinations	5							
7.0	TSS Provisions for Link	.8							
	7.1 Output (930 to PDP-5)	.8							
	7.1.1 General	8							
	7.1.2 Character Output	.8							
	7.1.3 Block Output	.8							

	7.1.4	Output Abnormal Conditions	20
7.2	Input	•••••••	21
	7.2.1	General	21
	7.2.2	Input Abnormal Conditions	22

ŝ

 $\bigcirc$ 

 $\bigcirc$ 

Ċ

1

#### 1.0 Introduction

The PDP-5/SDS-930 Communications Link (herein referred to as the Link) provides a means for either computer to transmit data to the receiving computer at a rate of approximately 60,000 bits/second. From the programmer's point of view, the transmission is 12-bit parallel (called a word) at a frequency of one word every 200 usec. At the programmer's option, receiving and/or transmitting in either computer can be under interrupt or skip control.

Transmission is in one direction only in a given cycle; that is, the receiving computer must wait until the transmitting computer is finished before it can initiate a cycle of its own.

The SDS terminal is connected to the 930 Data Multiplex channel and EOM selector. The PDP-5 terminal connects to the Input Mixer (i.e., Accumulator) and is controlled by IOT instructions. Although this document is intended primarily for system programmers, section 7 is devoted to TSS provisions for programming the Link. Also, the PDP-5 interrupt Monitor INT\* should be referred to for normal user Link programming in the PDP-5.

\* Document No. 30.30.20

2.

#### 2.0 Initiation of a Transmission Cycle

Each end of the Link can initiate only a transmission cycle (consisting of from one to any number of words transmitted); the receiving computer can ignore transmission requests simply by not executing the proper receive instructions. However, the Link hardware will remember one level of transmission requests if the Link is not in the Inactive Mode; i.e., the Link is in the Transmit or Receive Mode.

Once a transmit request has been made, the request is remembered until the Link next reaches its inactive state, at which time the Transmit Mode is entered, the request is turned off, and the requesting computer notified, at which time it can immediately transmit two words. These two words are not necessarily recieved, however, since each end of the Link has a 12-bit buffer for parallel read in/out.

### 3.0. Transmit/Receive Cycle (T/R Cycle)

When either computer requests a transmission cycle, it is notified that the Link hardware has entered the requested transmit mode by receiving an interrupt, provided interrupts have not been disarmed or disabled. The receiving computer is not notified of an ensuing T/R cycle until the first word is waiting in its buffer to be read in.

That is, in all cases, once the hardware enters a mode, each computer is notified of its Link buffer condition by either interrupts, or skip instructions if interrupts are disarmed or disabled. The Link interrupt requests become false when the buffer is emptied (the word read in) or filled (a word read out to the buffer) depending on the mode. These interrupt request lines are the same ones sensed by skip instructions, but are gated by enable flip-flops before reaching the interrupt logic. In the 930, the standard AIR (arm interrupts) and EIR (enable interrupts) instructions apply; the Receive and Transmit Interrupts can be armed individually in both machines.\*

From the above discussion is is seen that it is generally necessary for both computers to have interrupt control enabled and armed while in the Inactive Mode in order to know when to enter the Receive Mode or when the first word can be transmitted. There is no other signal to the receiving computer that its buffer is full and no other signal to the transmitting computer that its request to initiate

See Document No. 20.50.20 for description of PDP-5 interrupt logic.

transmission has been granted than the interrupt request lines (which can be sensed with skip instructions).

4.0. Leaving Transmit Mode

Instructions are provided for both machines to turn off or end transmission. The instructions can be executed at any time following read out to the Link buffer of the last word to **be** sent. However, the Link hardware does not enter the Inactive Mode until the last word has been sent and read in by the receiving computer.

If the turn-off instructions are executed by either computer when it is not transmitting, the turn-off request is ignored.

The turn-off logic will not affect any transmit request made previous to the turn-off request.

# 4.1. Panic Conditions

Provisions are provided in both machines for recovering from software blow-up, i.e., for returning the link to Idle Mode and clearing all stacked Enter and End Transmit Mode requests. This is not so simple since either end cannot distinguish End Transmission from Clear or Reset requests from the other machine, and under normal circumstances, End Transmission requests do not destroy stacked Transmission requests.

The simplest method to insure that the Link is clear is to (a) push the Master Clear button\* once or the START button twice

\* Located on the back side of card P23 in the EOM selector rack.

on the SDS end, or switch POWER-ON on the PDP-5. Since this method is not practical in a Time-Sharing system, special clear instructions are provided for both machines.

The following clearing procedure may be done in either order, but both are necessary to insure the Idle mode with no stacked transmit requests:

- (a) Execute clear instruction in PDP-5\* and do not issue Transmit request. This will clear current state and PDP-5 Transmit request.
- (b) Enter 930 program which executes a clear and no Transmit requests. This clears current state and 930 Transmit request.

An alternative procedure is to execute two clear instructions in either machine (spaced at least 10 usec apart), assuming the other is not issuing repeated transmit requests.

- 5.0. Link Instructions
  - 5.1. SDS End
    - 5.1.1. Interrupt Locations

2048 .... Link Receive Interrupt 2058 .... Link Transmit Interrupt 2028 .... DSCII Word-count = 0 2038 .... DSCII End-of-Record

\*See Section 5.2.5.

5.1.2. Interrupt Control

AIR ARM INTERRUPTS 0 02 20020 2 13 8 9 AIR must be followed by the PARALLEL ØUTPUT (PØT) instruction. The word the PØT instruction addresses is: WC E R 00 C R т  $\overline{0}$ 6 91011 12 13 14 012 C arm all interrupts with 1 in Bits 8-23. 102 disarm all interrupts with O in Bits 8-23 112 same as Ol, and 10, R Link Receive Interrupt T Link Transmit Interrupt WC Word count ER End of Record EIR ENABLE INTERRUPTS . 0 02 20002 2  $\overline{0}$ 3 8 9 EIR enables the SDS-930 interrupt system. DISABLE INTERRUPTS DIR 0 02 20004

DIR disables the SDS-930 interrupt system. See also the SDS Manual concerning non-interruptible and privileged instructions.

8

9

the has the states

2

3

# 20.50.20 July 11, 1966

5.1.3.	Link Select (Tra	unsmit Request, E	nd Transmission, Etc.)		
>	еøм зохоз <sub>8</sub>	SELECT LINK	(EØM Type 3)		
	<b>.</b>				
	0 02	3 0	x 03		
	0 2 3 8	9 10 11 12 14 1	5 17 18 23		
	This EØM Type 3 must be executed				
	(see below) in order to select the Link as the $I/O$				
	device (Bits 20-	-23 select the Li	nk.). X is decoded		
	in the Link hard	lware to perform	the following func-		

X	•	Function
1 <sub>8</sub>	• • • • • •	Transmit Request
28	• • • • • •	Force Link to Idle Mode
3 <sub>8</sub>	••••	End Transmission
48		Start Transmission
5 <sub>8</sub>	•••••	Start Rec
(any F)	* * * * * *	Select Link

tions:

NOTE: EØM is privileged in that no interrupt can occur

between any type EØM and the instruction following it.

### 5.1.4 DMC Programming

Either computer may initiate a request to transmit data by executing certain instructions. Then, upon receiving notice from the LINK through interrupts that the LINK is prepared to enter a specific mode, the 930 program must first set up the appropriate (2-word) interlace words in memory, execute a sequence of  $E\phi M/P\phi T$  commands to select the appropriate DSC II subchannel termination conditions, and then inform the LINK to start operation.

### Transmit Request

The 930 requests to transmit by executing:

EØM 30103g

When the LINK next enters the Idle mode, a LINK transmit interrupt occurs.

Interlace Word

word	count	address
0	8	9 23

The interlace words for subchannel 244 are in memory cells 244 (even word) and 245 (odd word). The DMC cycle for all subchannels is:

- 1) Read odd or even interlace word
- 2) Increment address, decrement word count
- 3) Test word count = 0
- 4) Restore interlace word
- 5) Data Input or Output

6) Stop or Continue

- a) If word count  $\neq 0$ , continue
- b) If even word and word count = 0, switch to odd word
- c) If odd word and word count = 0 and cycle bit set, switch to even word
- d) Otherwise disconnect and cause word count interrupt.

In particular, for 2 words transmitted, starting at location  $500_8$  the interlace word would initially be  $0020477_8$ . Word count = 0 implies 512 word buffer. The initial address is the buffer starting address -1.

#### Select EØM

To set up the DSC II terminate conditions one first executes an EØM class 7:

	0	ЕØМ	7	8	DSC II	Number
. '	0 2	3 8	9 11	12 14	15	23

(in particular; EØM 72244 for subchannel 240). This is followed by a PØT instruction, the contents of whose effective address contains

	1	0	0	0		eør	ZCT	С	E/Ø	
0	11	12			19	20	51	22	23	Ĩ.

where (a)  $E \emptyset R = 1$  arms end-of-record interrupt

(b) ZCT = 1 arms count=0 interrupt

(c) C = 1 allows automatic switching from odd to even interlace word when count = 0

(d)  $E/\phi = 1$  selects odd interlace word for starting

In particular, if the potted word contains a 5, cycling begins with the odd word, and terminates and causes an interrupt when the odd word count = 0. With a potted word of 7, the same is true except that termination (disconnect) does not occur at odd word count = 0, but instead switches to the even word.

#### Start DSC EØM

The DSC is actually selected (started) by

	0	ЕОМ	7		D	DSC	II Number	
1	0 2	3 8	9	11	12 <b>14</b>	15		3

(in particular; EOM 71244 for subchannel 244). This is followed by a PØT instruction the contents of whose effective address contains anything except bits 13 through 23=0. This special case will cause the DSC II to terminate when the word count

9.

next = 0 regardless of any previsouly established terminate conditions.

### Start LINK EOM

The Link is started into Transmit or Receive mode by

EOM 30X03 where X = 4 - Start Transmit

## 5 - Start Receive

These commands may be executed any time the LINK is in the Idle mode (as sensed by an SKS 30703); i.e., the initial request interrupts need not occur.

### LINK End Transmission

To end transmission, an EOM  $30303_8$  is executed anytime following the last word sent assuming a word-count = 0 and automatic disconnect has occurred. If otherwise, the Idle mode will be entered when the current word being sent has been received by the PDP-5.

5.1.5. Skip Instructions

SKS

**30**x038

----

SKIP IF LINK STATE TRUE

40 0 X 03 3 0 19 10 11 12 14 15 17 18 + 13 +8 1 2 The SKS Type 3 (System Test Mode) is used to test for different states of the Link depending upon X. If the state is not true, the next instruction is executed; otherwise, the next instruction is skipped. Bits 20-23 select the Link. The states or signals tested are as follows:

<u>x</u>	n e . g . n	Skip if State True
18	• • • • • • •	Receive Interrupt Request (Link Buffer Full, Receive Mode)
38		Transmit Interrupt Request (Link Buffer Empty, Transmit Mode)
7 <sub>8</sub>	• • • • • •	Inactive Mode
(Others	)	Unused

NOTE: It is not necessary that SKS be preceded by a Link Select EØM.

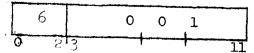
5.2. PDP-5 End

## 5.2.1. Interrupt Locations

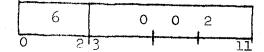
75<sub>8</sub> .... Link Transmit Interrupt 76<sub>8</sub> .... Link Receive Interrupt Locations 75 and 76 will normally contain 12-bit addresses which represent the effective address transferred to upon receiving an interrupt. 5.2.2. Interrupt Control

IØN

ENABLE INTERRUPTS



IØN enables all PDP-5 interrupts. An IØN must be executed following each interrupt two instructions before the next instruction that may be interrupted; i.e., the instruction immediately following the IØN will be executed before the next interrupt can occur. IØF DISABLE INTERRUPTS



IØF disables all PDP-5 interrupts. An IØF automatically occurs following each interrupt.

ARM

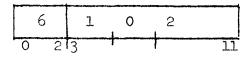
ARM INTERRUPTS

6 1 0 1 213 11

Execution of ARM with AC bit ll true, arms the link transmit flag, bit 10, the link receive flag. If a bit is false, the arm/disarm state of that flag is unaffected.

DARM

DISARM INTERRUPTS



Disarm is the same as ARM except that the interrupt if Disarmed if it's associated AC bit is true. 12.

6 1 0 4 IØT 104<sub>8</sub> ñ 213

A PDP-5 interrupt causes an effective JMS\* 18. Starting at Location 2 will normally be a program which executes an IRC which OR's the contents of the Accumulator with the Interrupt Counter Word which has the following format:

JMP\* 608+C INTERRUPT CØUNTER WØRD

10 3 C

where C represents the device causing the interrupt; in this case:

C

LTR

6

158 .... Link Transmit Interrupt

 $16_8$  .... Link Receive Interrupt Normally, this Interrupt Counter Word is executed following each interrupt where  $60_8 - 77_8$  are locations of 16 distinct interrupt routines.

LINK TRANSMIT REQUEST

4

5.2.3. Link Select (Transmit Request, End Transmission)

2

1

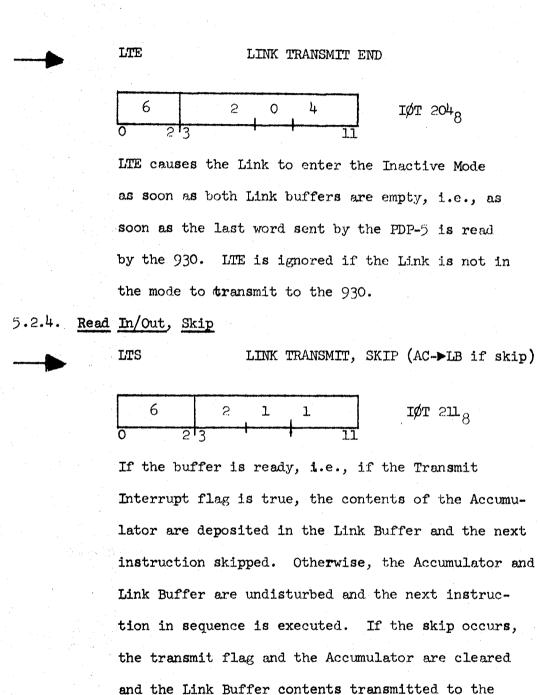
IØT 2148

LTR is executed once for each block of words transmitted. If the Link is busy, the request is remembered until the next Inactive Mode is reached by the Link hardware; i.e., the request is turned off only when the Link enters the (PDP-5) Transmit

Mode.

LINK RECEIVE, SKIP (LB-AC if skip)

IØT 2012



0

2

1

SDS-930.

6

213

LRS

If the Buffer is ready, i.e., if the Receive Interrupt Request flag is true, the contents of the Accumulator are OR'd with the contents of the Link Buffer and the next instruction skipped. Otherwise, the Accumulator and Link Buffer are undisturbed and the next instruction in sequence is executed. As each word is read by the PDP-5, another word is requested from the SDS-930 (by the Link hardware).

DGØ

CLEAR AND RESET

2 1 5 IØT 2128 6 23

This general clear instruction starts display, resets GO, Pen-down, Pen-up, and Link flags, and forces the Link to the Idle mode. However, the 930-Transmit request toggle is not cleared so the 930-Transmit mode may immediately follow.

6.0 IOT Command Combinations

IØT		Function	
6201*	• • •	Link Receive, Skip.	
6204	• • •	End Transmission.	
620 <b>5</b>	• • •	Link Receive, End Transmission, Ski	.p

\* IØT 202 is associated with the RAND Tablet and is normally not useful with LINK IØT's.

16.

62 <b>12</b>	• • • • • • • •	Reset Link to IDLE Mode.
6211	• • • • • • • • •	Link Transmit, Skip, Clear AC.
6213	• • • • • • • • •	Not Useful.
6214	• • • • • • • •	Link Transmit Request.
6216	• • • • • • • • •	Reset Link, Enter Transmit Request.
6215	•••••	Request Transmit Mode, Transmit, Skip. (If the Skip Occurs, a Transmit Request Is Necessarily Posted.)
6217		Not Useful.

EXAMPLE: The following three instructions will transmit one word, in Accumulator, to the SDS-930 return Link to Inactive Mode, and Leave AC Cleared.

IØT	212	Force Link to Idle Mode.
IØT	2 <b>15</b>	Transmit Skip, Request Transmit Mode.
JMP	•-1	
IØT	204	End Transmission

The following program will send a Zero to the 930, regardless of the state of the link hardware (Provided 930 is listening), and then receive a block of words (first 2 words received are in parenthesis).

(Load Address Switch Clears AC)

IØT	215	Program Will Repeatedly Request.
JMP	•-1	Transmit Mode Until Granted By
IØT	2 <b>05</b>	End Transmission, Receive, Skip.
JMP	•-1	
DCA	•+3	

IØT	201	Receive, Skip
JMP	•-1	
(DCA	·+1)	First Word Received
(JMP	•-6)	Second Word Received

7.0 TSS Provisions for Link

As of system 1.83, the PDP-5/930 Link input and output will operate as follows:

7.1 Output (930 to PDP-5)

7.1.1 General

One must first open the file with BRS 1 for device number 7.

LDX =7 BRS 1

The return will skip with the file number in A when the file has been successfully opened. If the file is already open or there is not room for another file in the system, no skip will occur.

The same file is closed by

LDA =file number BRS 2

This BRS never skips.

Once the file is open, one can transmit single characters with CIO, or a block with BIO.

# 7.1.2 Character Output

CIO is operated as follows:

LDA =code CIO =file number

where code is an arbitrary 8-bit character (normally a 7-bit internal ASCII character). CIO never skips.

In this case the PDP-5 will receive "code+ $4000_8$ ". The  $4000_8$  is how the PDP-5 can tell character from block mode.

7.1.3 Block Output

A block is transmitted by

LDA	=word count
LDX	=starting address
BIO	=file number

After all words have been sent, the return skips. No skip occurs upon abnormal or error conditions, to be discussed later.

The data sent is the word count (N) which must be  $0 < N \leq 2047$ and does <u>not</u> include itself. Next, the low order 12-bits of each data word between the starting address, SA, and SA+N-1 is sent. As an example, the following could be received by the PDP-5 with the call:

TAD	=file	number		4	
JMS* SA	BIO		PDP-5	program	
EA					

where, upon return

SA/	4041	character A
	4042	character B
	4043	character C
	0003	block word count
	0041	
	0042	3 word block
	4043	
	4137	character rubout
	0001	block word count
EA/	5640	l word block

Note that the PDP-5 must keep in sync -- a character is looked for only after the end of a block (or after a character).

For the example above, the 930 program would have had to use four CIO's and two BIO's as follows:

•		
•	•	
LDA	=41	
CIO		number
LDA	=42	
CIO		number
LDA	=43	
CIO	=file	number
LDA	=3	
LDX	SA.	
BIO	=file	number
BRU	error	
LDA	=137	
CIO	=file	number
LDA	=1	
LDX	=5640	
BIO	=file	number
BRU	error	

where SA/ DATA 41,42,4043

## 7.1.4 Output Abnormal Conditions

- (1) File not open
  - (a) CIO illegal instruction
  - (b) BIO illegal instruction
- (2) Word count too large (word count = 0 is a no op)
  - (a) CIO can't occur (no word count involved)
  - (b) BIO illegal instruction
- (3) PDP-5 not responding.

An abnormal termination occurs if the data is not sent within 500 milliseconds if swapping is occurring. 500ms is entirely sufficient for a 2048 word block, and termination occurs only if the PDP-5 is improperly programmed.

- (a) CIO I/O condition termination -- sets flag bit 5 and causes interrupt 4 if armed.
- (b) BIO I/O condition termination -- sets flag bit 5. If interrupt 4 is armed, it occurs; otherwise the BIO returns without skipping.
- (4) End of Record interrupt received.

This occurs if the PDP-5 executes a CLEAR LINK instruction when the link is not in IDLE mode. (IDLE =  $\overrightarrow{\text{RECEIVE}}$  OR  $\overrightarrow{\text{TRANSMIT}}$ ). Same as 2.4 (3) above, except that flag bit 6 is set.

## 7.2 Input

## 7.2.1 General

Input is similar except the device number is 6 for opening the files. Both input and output files may be open simultaneously. For BIO, at most WC words (WC  $\leq 2047$ ) may be received. If N<WC, where N is the word count transmitted by the PDP-5, the BIO will not skip on return; the A register will contain SA+N, where SA is the initial core address of the block; bit 8 will be set in the file number; and interrupt 4 will occur, if armed. If N>WC, the BIO will skip, and further calls on BIO are necessary to read the remaining words; the count N-WC is placed in the A register.

Note that for output, above, the PDP-5 Monitor INT makes no distinction between block and character mode, and the user program must make the distinction. In the Input case, however, the 930 monitor makes a distinction -- characters received are stored in an internal teletype buffer and handled like teletype input while blocks are written directly into the user's program as requested through BIO.

As characters are received, they are buffered internally in the monitor -- rubout is treated exactly as a teletype rubout, but only a word count is buffered for block input. When the character buffer is full, or a block word count is received, the PDP-5 Link is temporarily suspended with no information lost, until the user program receives the data. Hence the following abnormalities exist:

(a) Block word count received - CIO input requested.

(b) Character received - BIO input requested.

In order to simplify the 930 monitor, these abnormalities will be treated with a special termination condition -- unlike the usual file I/O where the block/character conversion is handled automatically.

#### 7.2.2 Input Abnormal Conditions

- (1) File not open (see 2.4 (1) above)
- (2) BIO request word count too large (see 2.4 (2) above)
- (3) End of record or Word Count = O received. Treated exactly the same as End-of-Record interrupt condition, 2.4 (4) above. This is necessary since the End-of-Record is caused only if the Link is not IDLE.
- (4) RUBOUT character received. Treated same as teletype rubout (Interrupt 1 or fork termination).
- (5) Wrong Mode
  - (a) Block word-count received, CIO input requested. Sets
    flag bit 7. Interrupt 4 occurs if armed, otherwise CIO
    returns. The block may be received with BIO.
  - (b) Character received, BIO input requested. Sets flag bit 7. Interrupt 4 occurs if armed, otherwise BIO returns without skipping. All characters received are buffered internally and must be read with CIO.