ST4038
PRODUCT MANUAL

Seagate

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INTRODUCTION

The ST4038 provides OEMs and system integrators with the high capacity and performance required for applications such as file servers, multi-tasking/multi-user small business systems, or systems with enhanced graphics.

Operating systems needing frequent and rapid data access will benefit from the 40 millisecond average access time. Designed for high volume production and performance, the ST4038 employs a dedicated-surface closed-loop servo system with a linear voice-coil actuator. This combination provides fast access to the desired track and continuous position feedback for unequaled recording performance. The prerecorded servo pattern insures precise head positioning and data integrity when exposed to thermal gradients such as system warm-up. The Read/Write heads automatically position and lock in the shipping zone when powered down.

High reliability in high volume requires special attention. Both reliability and availability are assured by using industry-proven mini-monolithic data heads and oxide media at conservative recording densities. Our innovative slider/flexure head assemblies permit greater stability and margins than with traditional Winchester recording heads.

Seagate manufactures, tests and ships disc drives with consistent high quality. Our manufacturing facilities have been designed and located exclusively for high volume production and testing of disc drives. Seagate's ongoing commitment to vertical integration assures availability of the latest technology at the same consistent quality and lowest possible cost.

Seagate's inspection techniques and process methods are qualified and controlled at every stage of assembly. Final assembly is conducted within a carefully controlled and constantly monitored Class 100 or better clean-room environment.

Every printed circuit board and finished disc drive is subjected to separate burn-in tests under stressed conditions. All functional parameters on every drive are verified with extensive marginalized testing. Each recording surface is inspected and all media defects are identified and mapped. The printed final test results are shipped with each drive. Our customer acceptance levels are among the highest in the industry.

1.0 SPECIFICATION SUMMARY

DRIVE CAPACITY 1.1

UNFORMATTED CAPACITY 1.1.1

Per Drive:	38.17 Megabytes
Per Cylinder:	52,080 Bytes
Per Track:	10,416 Bytes

FORMATTED CAPACITY 1.1.2

Per Drive:	31.90 Megabytes
Per Cylinder:	43,520 Bytes
Per Track:	8,704 Bytes
Per Sector:	512 Bytes
Sectors per Track:	17

PHYSICAL ORGANIZATION 1.1.3

Tracks:	3,665
Cylinders:	733
Read/Write Heads:	5
Servo Heads	1
Discs:	3

ACCESS TIME DEFINITION AND TIMING 1.2

Access time is defined as the time from the leading edge of the first Step pulse received to SEEK COMPLETE (including carriage settling). The period between Step pulses must be between 10 μsec. to 70 μsec.

Average access time is measured over a 243-track seek (one-third stroke).[1] The calculation assumes the following:

1. Step pulses are issued at a 35 μsec. rate
2. Nominal temperature and power
3. The average is taken from an inward one-third stroke, plus an outward one-third stroke.

Track-to-Track:	11.0 msec. max.
Average:	40.0 msec. max.[1]
Maximum Seek:	85.0 msec. max.[1]
Average Latency:	8.33 msec.

FUNCTIONAL SPECIFICATIONS 1.3

Rotational Speed:	3,600 RPM ± 0.5%
Recording Density:	9,617 BPI/FCI
Track Density:	750 TPI
Recording Method:	MFM
Data Transfer Rate:	5.0 Megabits/second

PHYSICAL SPECIFICATIONS 1.4

Height:	3.25 ± .01 inches (82.55 ± 0.25 mm)
Width:	5.75 $^{+.00}_{-.02}$ inches (146.05 $^{+.00}_{-.51}$ mm)
Depth:	8.00 inches max. (203.2 mm)
Weight:	6.0 lbs (2.7 Kg)

1. Buffered-Seek

1.5 RELIABILITY SPECIFICATIONS

MTBF:	12,000 Power-on Hours[2]
PM:	Not Required
MTTR:	30 Minutes
Service Life:	5 Years

1.5.1 READ ERROR RATES

Recoverable Read Errors:	1 per 10^{10} bits read [3]
Nonrecoverable Read Errors:	1 per 10^{12} bits read [4]
Seek Errors:	1 per 10^6 seeks

1.5.1.1 BIT JITTER

Bit jitter reduction determines the relationship between the leading edge of READ DATA and the center of the data window.

The specified Read error rates are based on the following bit jitter specification: The data separator must provide at least -40 dB of bit jitter reduction at 2F with an offset error of less than 1.5 nsec. shift from the center of the data window.

1.5.2 MEDIA DEFECTS

A media defect is a Read error when data, which has been correctly written, cannot be recovered within 16 retries.

A printout will be provided with each drive shipped listing the location of any defect by head, cylinder, sector and byte[5]. It will also specify the number of bytes from Index.

There will be no more than nine (9) defects per Read/Write surface for a maximum total of thirty-six (36) per drive. Cylinder Zero will be free of defects.

1.6 ENVIRONMENTAL SPECIFICATIONS

1.6.1 AMBIENT TEMPERATURE

Operating:	10 °C to 45 °C (50 °F to 113 °F)
Nonoperating:	-40 °C to 60 °C (-40 °F to 140 °F)

1.6.2 TEMPERATURE GRADIENT

Operating:	10 °C/hr (18 °F/hr) max.
Nonoperating:	Below condensation

1.6.3 RELATIVE HUMIDITY

Operating:	8 to 80% noncondensing
Maximum Wet Bulb:	26 °C (78.8 °F)
Nonoperating:	5 to 95% noncondensing

2. Typical usage:
   a. 25 °C ambient temperature
   b. Sea level
   c. Calculated per *Mil. Spec. 217.*
3. Recoverable within 16 retries
4. Not recoverable within 16 retries
5. Based on a 32-sector, 256 byte/sector format

ALTITUDE LIMITS 1.6.4

Operating:	-1,000 ft to 10,000 ft
Nonoperating:	-1,000 ft to 30,000 ft

OPERATING SHOCK 1.6.5

Maximum permitted shock without incurring nonrecoverable errors: 10 G's. [6,7]

OPERATING VIBRATION 1.6.6

Maximum permitted vibration, at the following frequencies, without incurring nonrecoverable errors:[7]

Frequency	Vibration
5 — 17 Hz Displacement (double amplitude)	0.036″
17 — 150 Hz Acceleration (peak-to-peak)	0.55 G
200 — 500 Hz Acceleration (peak to peak)	0.25 G
500 — 200 Hz Acceleration (peak-to-peak)	0.25 G
150 — 17 Hz Acceleration (peak-to-peak)	0.55 G
17 — 5 Hz Displacement (double amplitude)	0.036″

NONOPERATING SHOCK 1.6.7

Maximum shock without incurring physical damage or degradation in performance: 35 G's. [7,8,9]

NONOPERATING VIBRATION 1.6.8

Maximum vibration, at the following frequencies, without incurring physical damage or degradation in performance:[7,8]

Frequency	Vibration
2—200 Hz	1.0 G (peak to peak)
200—2 Hz	1.0 G (peak to peak)

DC POWER REQUIREMENTS 1.7

The ST4038 is listed in accordance with UL 478 and CSA C22.2 (0-M1982), and meets all applicable sections of IEC 380 and VDE 0806/08.81, as tested by *TUV-Rheinland, North America.*

Power may be applied or removed in any sequence without loss of data or damage to the drive.

+12 VDC:

Voltage Tolerance (inc. ripple):	± 5% Both seek and nonseek conditions
Maximum Current at Power-on:	4.0 Amp
Seeking:	2.5 Amp typical [10]
	4.0 Amp (pulse) [10]
Nonseeking:	1.5 Amp typical [11]

6. 11 msec. half-sine wave shock pulse.
7. Input levels at the drive mounting screws, drive mounted in an approved orientation.
8. Heads positioned in the shipping zone
9. 12.3 msec. square-wave shock pulse (ΔV=166.6 inch/sec.)
10. Measured under the following standard operating conditions:
    a. 25 °C ambient temperature
    b. Sea level
    c. Nominal voltages applied
    d. Spindle rotating, drive seeking with buffered one-third stroke followed by two revolutions of non-seek time.
11. Measured under the following standard operating conditions:
    a. 25 °C ambient temperature
    b. Sea level
    c. Nominal voltages applied
    d. Spindle rotating and drive not seeking

+5 VDC:

Voltage Tolerance (inc. ripple):	± 5% Both seek and nonseek conditions
Maximum Current at Power-on:	1.5 Amp
Seeking:	1.5 Amp typical [10]
Nonseeking:	1.5 Amp typical [11]

Power:

Seeking:	37.5 Watts typical[10]
Nonseeking	25.5 Watts typical[11]

1.7.1 INPUT NOISE RIPPLE

The maximum permitted ripple is 100 mV (peak-to-peak) on either +12 VDC or +5 VDC measured on the host system power supply across the following equivalent resistive loads:

+ 12 Volts: 8 Ω
+ 5 Volts: 3 Ω

1.7.2 INPUT NOISE FREQUENCY

20 MHz max. on both the +12 VDC and +5 VDC lines

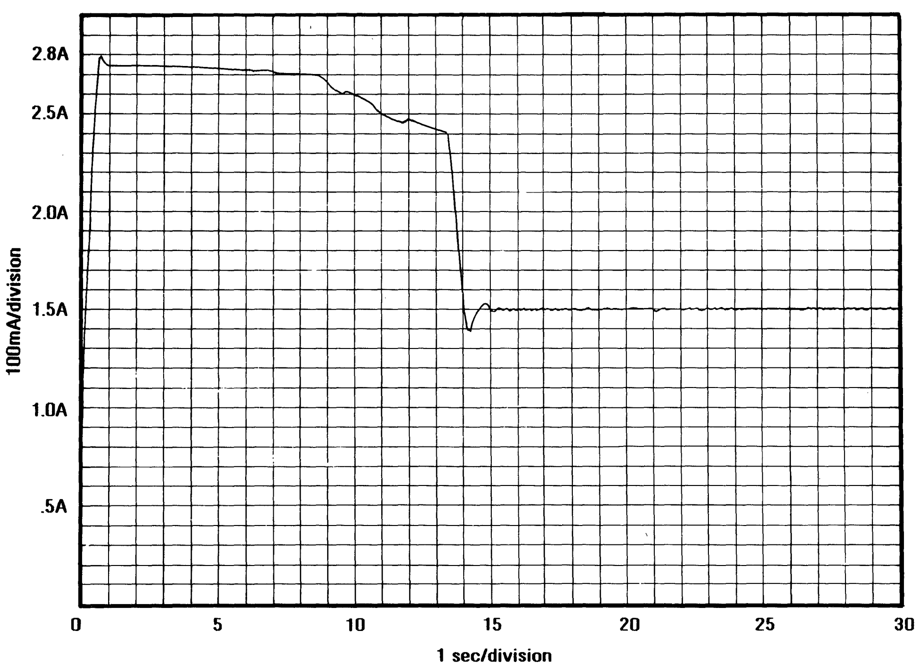
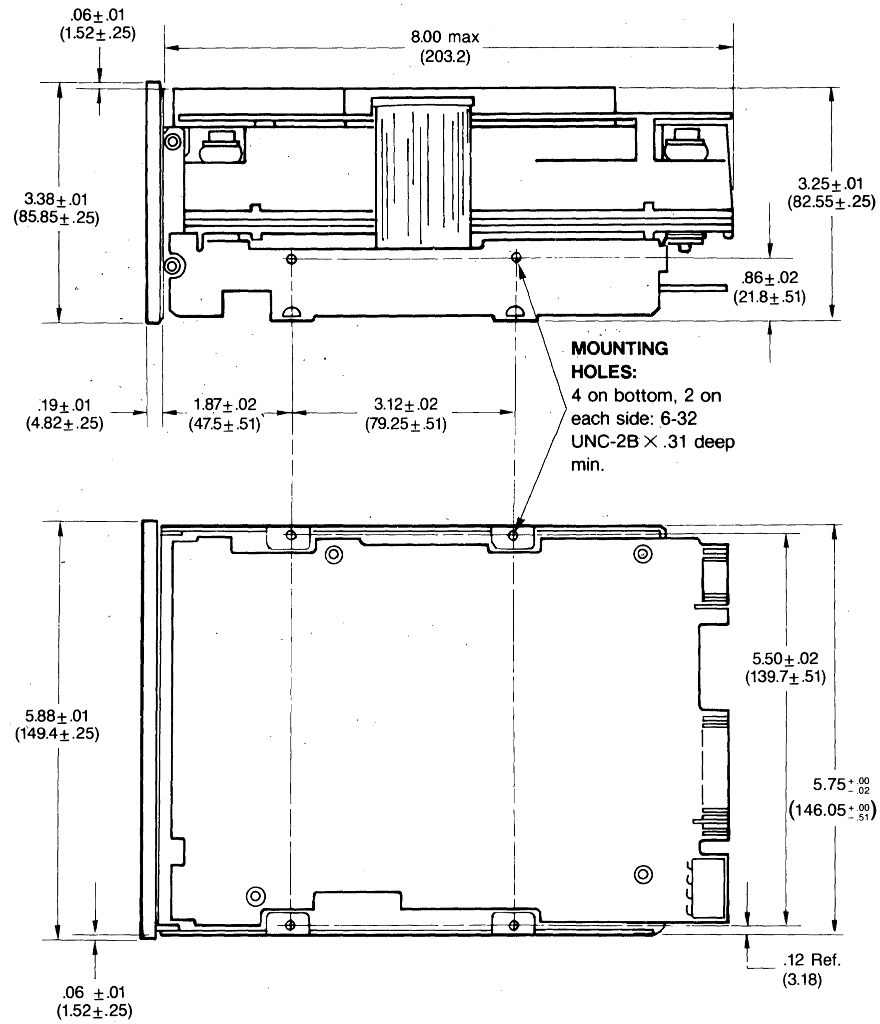


FIGURE 1: Typical +12 Volt DC Start-Up Current Profile

FIGURE 2:
Mounting Dimensions



MOUNTING REQUIREMENTS 1.8

The ST4038 may be mounted in the following orientations:

Horizontal:	Spindle motor down
Sides:	Left or right

Refer to *Figure 2* for mounting dimensions.

The drive should not be tilted front to back, in any position, by more than ± 5°. For optimum performance the drive should be formatted in the same orientation as it will be mounted in the host system.

SHOCK MOUNTING RECOMMENDATION 1.8.1

It is recommended that any external shock mounts between the drive and the host frame be designed so that the composite system has a vertical resonant frequency of 25 Hz or lower.

A minimum clearance of 0.050 inch should be allowed around the entire perimeter of the drive to allow for cooling airflow and motion during mechanical shock or vibration.

1.8.2 HANDLING AND STATIC-DISCHARGE PRECAUTIONS

After unpacking, and prior to system integration, the drive is exposed to potential handling and ESD hazard.

Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

It is strongly recommended that the drive always rest on a padded surface until the drive is mounted in the host system.

1.8.3 SHIPPING ZONE

Upon power-down, the carriage will automatically move to the shipping zone and the carriage lock will engage. All portions of the head/slider assembly will park inboard of the maximum data cylinder, 732.

The heads may also be parked by issuing a seek command to cylinder 733. When power is applied, the lock will automatically disengage and the heads will recalibrate to Track Ø.

If the heads are parked while the power is still applied, and Step pulses are then issued, the lock will disengage and the drive will recalibrate to Track Ø.

2.0 ST4038 HOST/DRIVE INTERFACE

This section details the physical specifications of the host/drive interface connectors. Connector dimensions and pin assignments follow under each subsection. Refer to *Figure 7* for an overall view of the drive interface connectors.

CONTROL/STATUS SIGNALS: PCB EDGE-CONNECTOR J1 2.1

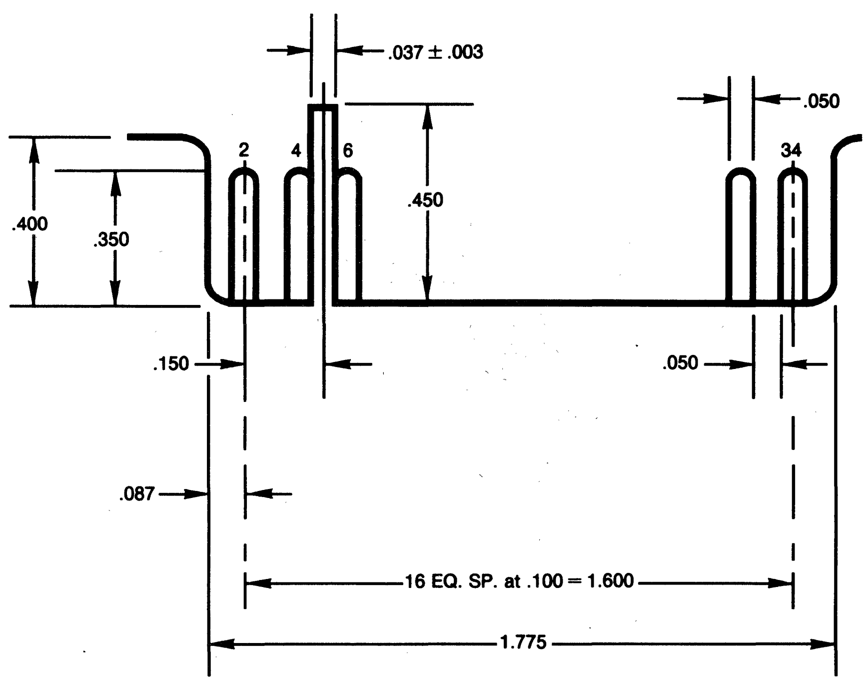
Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

Control and status signals between the host and the drive are transmitted through a 34-pin PCB edge-connector, J1. *Figure 3* below indicates connector dimensions and *Table 1* lists the pin assignments. A host/drive interconnection is illustrated in *Figure 4.*

With the drive resting on a padded surface, oriented with the Main Control PCB up and the edge-connectors toward you, J1 is to your left and J2 is on the right. Refer to *Figure 7* for position.

J1 pins are numbered 1 through 34 with the even pins located on the component side of the PCB. All odd pins are ground. A key slot is provided between pins 4 and 6. Pin 2 is labeled. The recommended mating connector for J1 is AMP ribbon connector part number 88373-3.

FIGURE 3: J1 Connector Dimensions



BOARD THICKNESS: 0.062 ± 0.007
TOLERANCE: 0.XXX ± 0.005
(unless otherwise noted)

GROUND RTN PIN	SIGNAL PIN	SIGNAL NAME
1	2	-HEAD SELECT 2^3
3	4	-HEAD SELECT2^2
5	6	-WRITE GATE
7	8†	-SEEK COMPLETE
9	10	-TRACK ∅
11	12†	-WRITE FAULT
13	14	-HEAD SELECT 2^0
15	16	RESERVED
17	18	-HEAD SELECT 2^1
19	20†	-INDEX
21	22†	-READY
23	24	-STEP
25	26	-DRIVE SELECT 1
27	28	-DRIVE SELECT 2
29	30	-DRIVE SELECT 3
31	32	-DRIVE SELECT 4
33	34	-DIRECTION IN
†STATUS ENABLED WITH DRIVE SELECT		

TABLE 1: J1 Host/Drive Pin Assignments

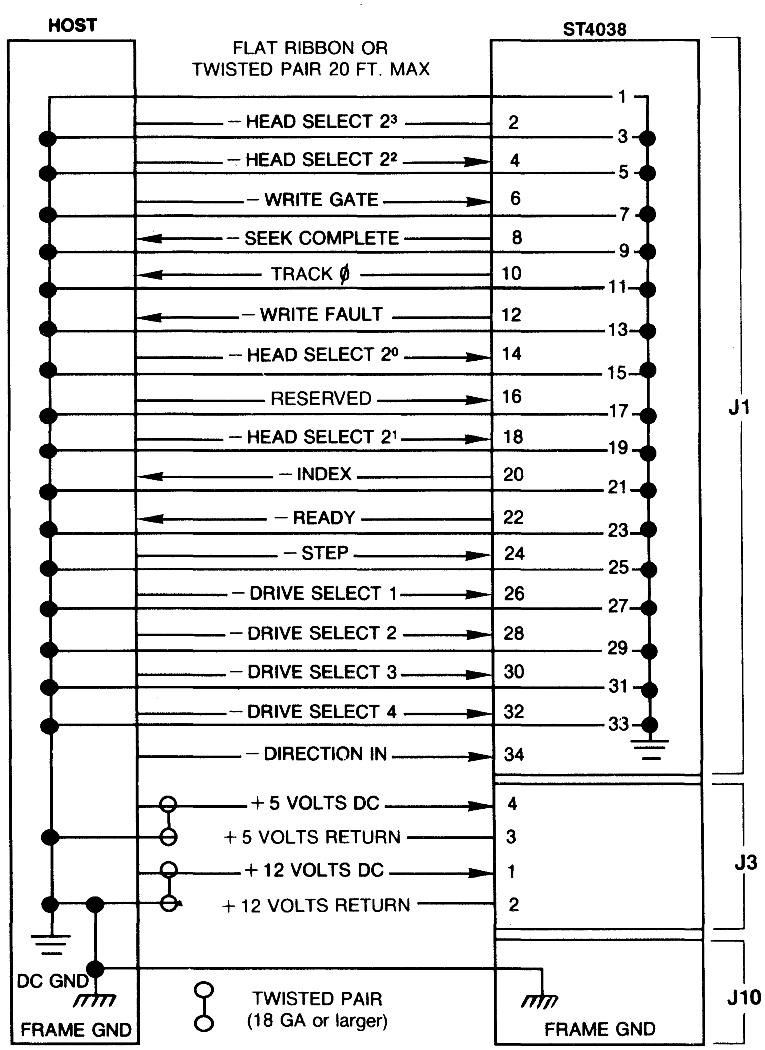


FIGURE 4: Control/Status Signals

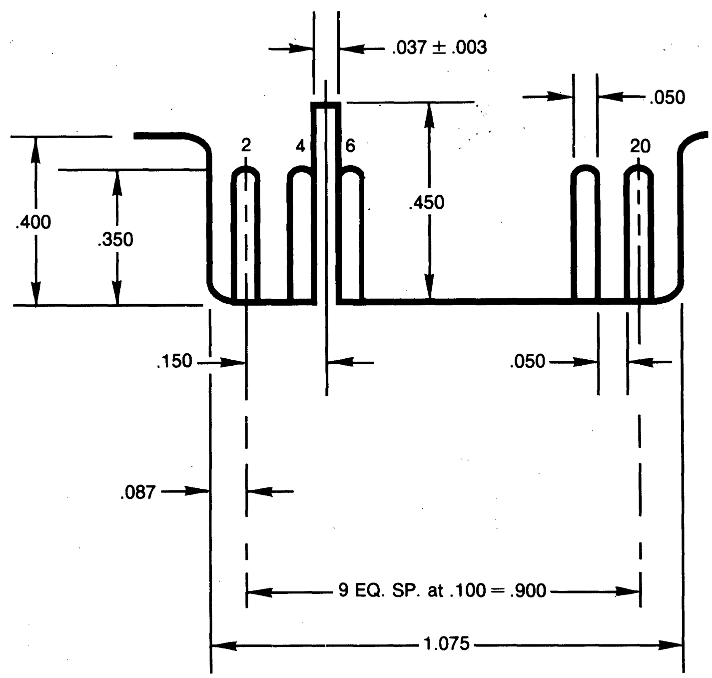
Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

Read/Write data signals are received and transmitted over a 20-pin PCB edge-connector, J2. *Figure 5* indicates connector dimensions and *Table 2* lists the pin assignments. A host/drive interconnection is illustrated in *Figure 6.*

With the drive resting on a padded surface, oriented with the Main Control PCB up and the edge-connectors toward you, J2 is to your right and J1 is on the left. Refer to *Figure 7.*

J2 pins are numbered 1 through 20 with the even pins located on the component side of the PCB. A key slot is provided between Pins 4 and 6. Pin 2 is labeled. The recommended mating connector for J2 is AMP ribbon connector, part number 88373-6.

FIGURE 5: J2 Connector Dimensions

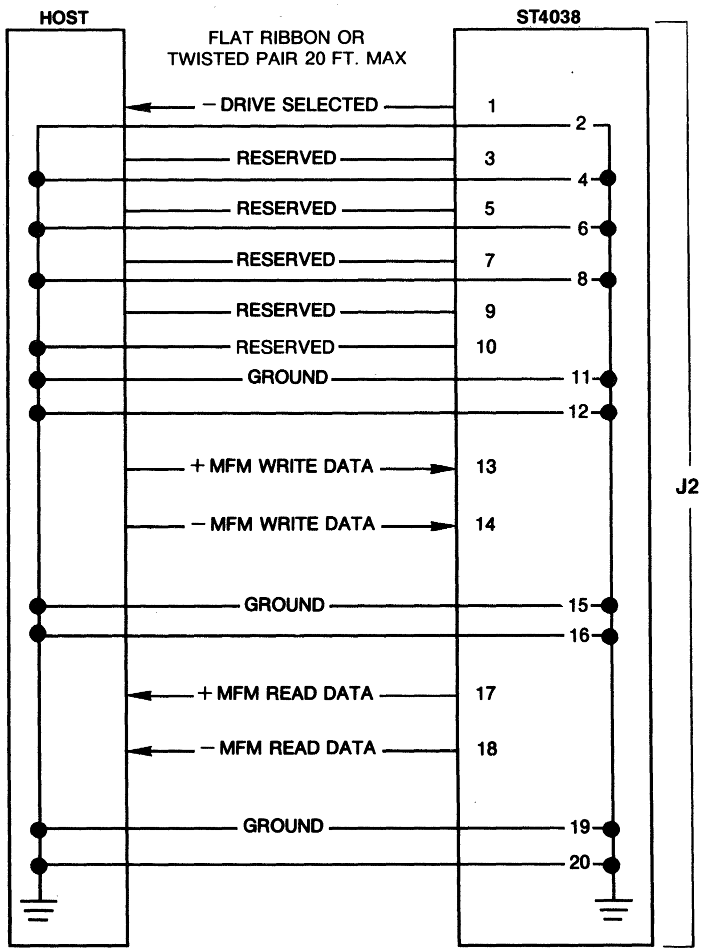


BOARD THICKNESS: 0.062 ± 0.007
TOLERANCE: 0.XXX ± 0.005
(unless otherwise noted)

TABLE 2: J2 Host/Drive Pin Assignments

GROUND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	-DRIVE SELECTED
4	3	RESERVED
6	5	RESERVED
8	7	RESERVED
10	9	RESERVED
12	11	GROUND
	13	+ MFM WRITE DATA
	14	− MFM WRITE DATA
16	15	GROUND
	17	+ MFM READ DATA
	18	− MFM READ DATA
20	19	GROUND

FIGURE 6: Data Signals



DC POWER: CONNECTOR J3 2.3

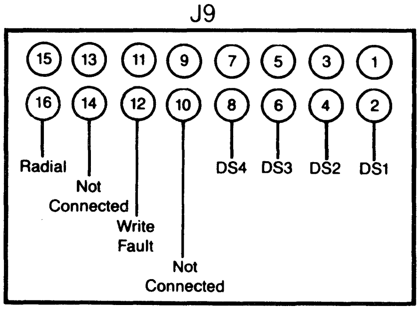
Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

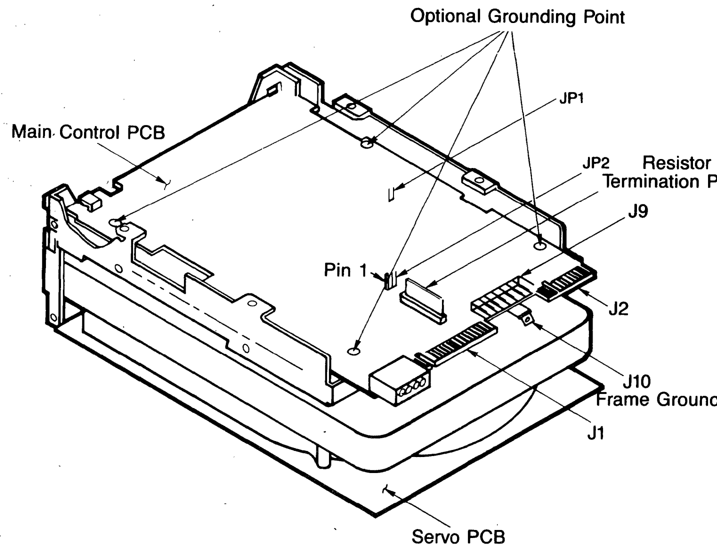
DC power is transmitted from the host to the drive via the power connector J3. J3 is a 4-pin AMP "Mate-N-Lock" connector, AMP part number 350211-1, mounted on the component side of the PCB. The recommended mating connector is AMP part number 1-480424-0.

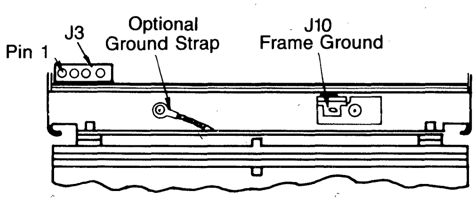
Applications using cable lengths less than five feet, may use #18AWG wire and AMP 61314-4 strip pins.

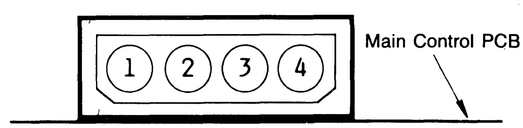
For applications requiring cable lengths greater than five feet, #14AWG wire is recommended using AMP 61117-4 strip pins.

FIGURE 7: Host/Drive Interface and Drive Configuration









PIN	POWER
1	+ 12 VOLTS
2	+ 12 VOLTS RETURN
3	+ 5 VOLTS RETURN
4	+ 5 VOLTS

DC Power Connector and Pin Assignments

FRAME GROUNDING: LUG J10 2.4

J10 is an AMP "Faston," part number 61761-2. It is located on the frame between and below the host/drive interface connectors. The recommended mating connector is AMP part number 62187-2. Refer to *Figure 7.*

3.0 DRIVE CONFIGURATION

The ST4038 may be configured for specific system requirements. These options are detailed in *Sections 3.1* though *3.4*.

3.1 DRIVE CONFIGURATION: SHUNT J9

J9 is a 16-pin right-angle shunt located midway between J1 and J2. Use the provided shorting blocks to enable the DRIVE SELECT lines and any required option. *Figure 7* illustrates J9 and indicates pin 1.

Note that pins 9-10 and 13-14 are not connected.

3.2 DRIVE SELECT

The DRIVE SELECT line enables the controller to select and address the drive. Control cable interface options use either a Daisy-Chain or Radial configuration.

Pins 1-2 shorted enable DRIVE SELECT 1
Pins 3-4 shorted enable DRIVE SELECT 2
Pins 5-6 shorted enable DRIVE SELECT 3
Pins 7-8 shorted enable DRIVE SELECT 4

3.2.1 DAISY-CHAIN

Each drive in the chain must be configured as either DRIVE SELECT 1, 2, 3 or 4, so that only one DRIVE SELECT line activates a device. The *last* drive in the chain must have a 220/330 Ω resistor termination pack installed. Refer to *Figure 7* for the resistor termination pack location.

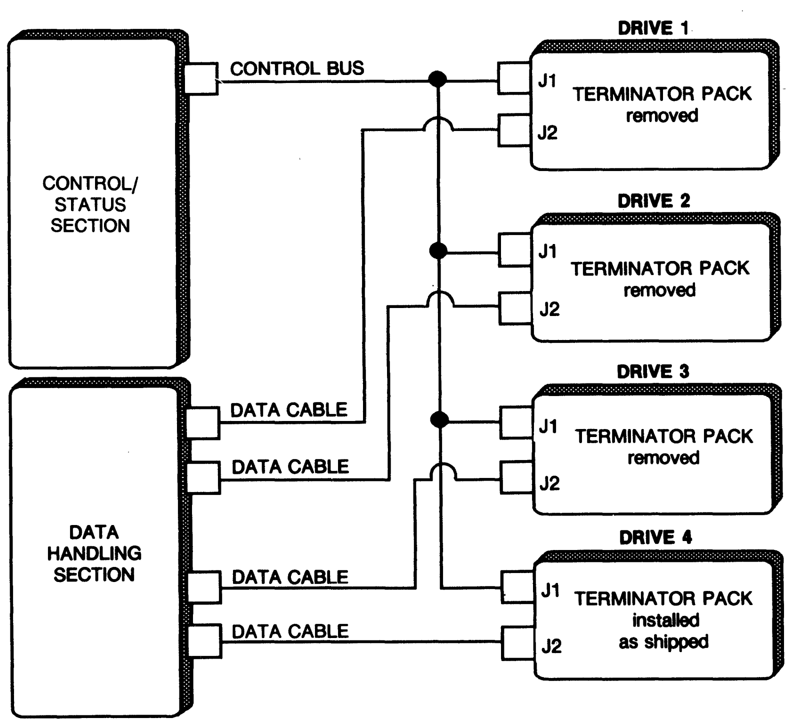


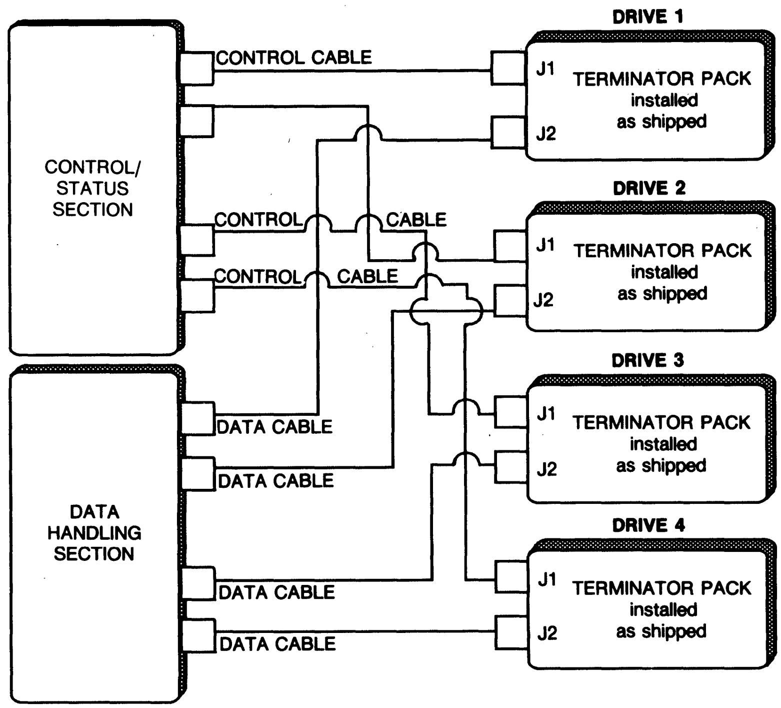
FIGURE 8: Daisy-Chain Configuration

RADIAL 3.2.2

The Radial option is enabled by shorting pins 15 and 16 at J9. Drives configured to this option are always selected and respond to all control signals issued on the attached control cable. The resistor termination pack must remain installed on *each* radially-connected drive. *Figure 9* illustrates a host/drive Radial configuration.

The LED activity light, if installed, will not light with the Radial option.

FIGURE 9: Radial Configuration



WRITE FAULT LATCH OPTIONS: CONNECTORS JP2 AND J9 3.3

These options allow the user to configure the WRITE FAULT reset to specific system requirements.

JP2 has three jumper pins, and is located adjacent to the 34-pin J1 connector. *Figure 7* illustrates JP2 and indicates pin 1. J9 is located midway between the PCB edge-connectors (see *Section 3.1*).

Note: As shipped, there may be a trace between pins 2 and 3 on JP2. This trace must be cut to allow use of the option requiring pins 1 and 2.

STANDARD: pins 1 and 2 shorted at JP2

WRITE FAULT will be cleared when Write Gate is false. A WRITE FAULT will only occur when Write Gate is True.

LATCHED: pins 2 and 3 shorted at JP2

This option will maintain WRITE FAULT True after Write Gate goes False and is recommended for controllers that do not edge-detect WRITE FAULT.

The latched operation has two configurations which are provided at the J9 shunt, pins 11 and 12.

1. **No jumper at J9:** The WRITE FAULT signal can only be cleared by a power-off/on cycle. Use of this option in conjunction with the DC-Unsafe option, (*Section 3.4*), is not recommended.
2. **Pins 11-12 shorted at J9:** The WRITE FAULT signal can be cleared by de-selecting the drive. When the drive is de-selected, and the fault condition is corrected, the WRITE FAULT signal will be false.

3.4 DC-UNSAFE OPTION: CONNECTOR JP1

When the two jumpers at JP1 are shorted, a DC-unsafe condition will cause a WRITE FAULT signal to be sent to the interface. Use *Figure 7* to locate JP1. Refer to *Section 5.6* for a more detailed discussion of WRITE FAULT.

4.0 CONTROL INPUT SIGNALS

The control signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing.

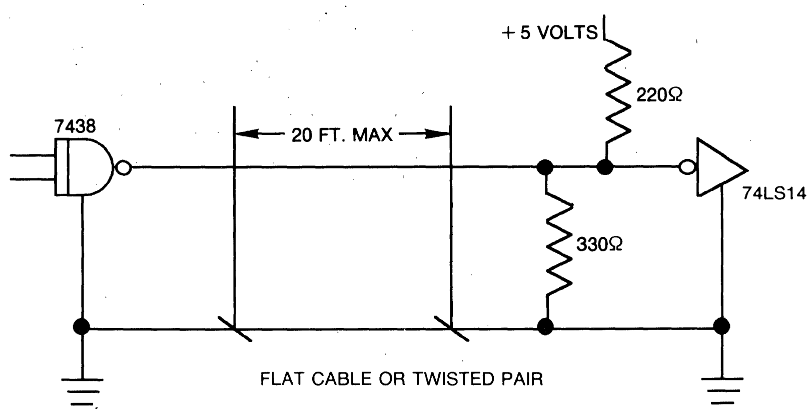
The signals to be multiplexed are WRITE GATE, HEAD SELECT 2^0, HEAD SELECT 2^1, HEAD SELECT 2^2, HEAD SELECT 2^3, DIRECTION IN, and STEP. These lines are terminated with a removable 220/330 Ω resistor pack.

The multiplexing signals are DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3, and DRIVE SELECT 4. These lines are terminated in a single fixed 220/330 Ω resistor pack.

Control signals are transmitted across the driver/receiver combination illustrated in *Figure 10.* Control input signals are activated in accordance with the following specifications:

True: 0.0 Volts DC to 0.4 Volts DC at I = -48 mA max.
False: 2.5 Volts DC to 5.25 Volts DC at I = +250 μA (open collector)
Termination: 220/330 Ω resistor pack

FIGURE 10: Control Signals Driver/Receiver Combination



HEAD SELECT 2^0, 2^1, 2^2, 2^3 — 4.1

These signals allow the selection of each Read/Write head in a binary code sequence. The lines are numbered 0 through 3. HEAD SELECT line 2^0 is the least significant line. When all HEAD SELECT lines are high on the interface, Head 0 is selected. Refer to *Figure 11* for HEAD SELECT timing.

Note that HEAD SELECT 2^3 is an invalid signal for the ST4038. The line is present on the interface, but is terminated. The drive will not respond to this input signal.

WRITE GATE — 4.2

The active state of this signal, or low level, enables data to be written to the disc and inhibits carriage motion if WRITE FAULT is active on the receipt of the first Step pulse. When inactive, or high, this signal enables data to be transferred from the drive and enables Step pulses to move the heads. Heads may not be switched while WRITE GATE is active.

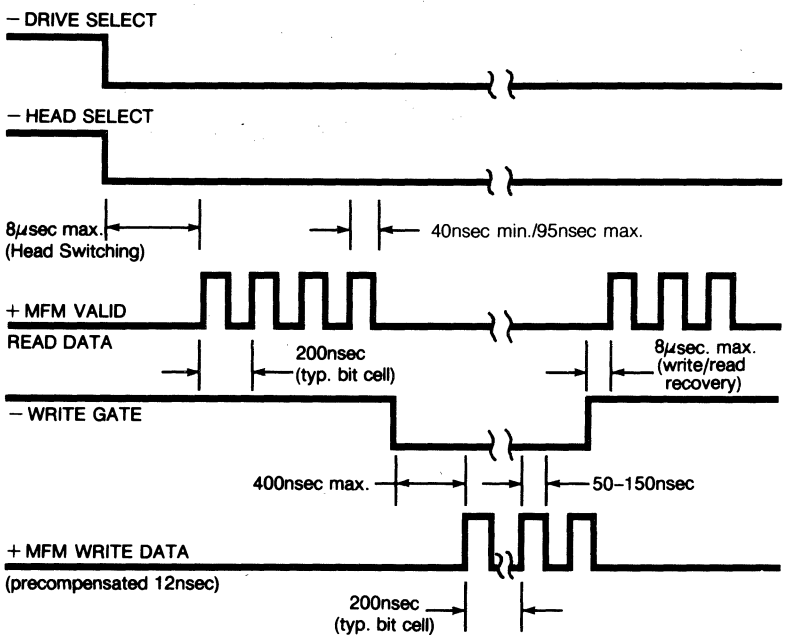


FIGURE 11:
Read/Write Timing

4.3 STEP

The STEP signal is a 2 μsec. to 10 μsec. pulse that initiates Read/Write head motion. The number of pulses issued determines distance traveled. The rate of Step pulses determines the access method.

If the period between pulses is from 10 μsec. to 70 μsec., the access method will be Buffered-Seek. Slow-Step is employed if the period between pulses is greater than or equal to 3 msec.

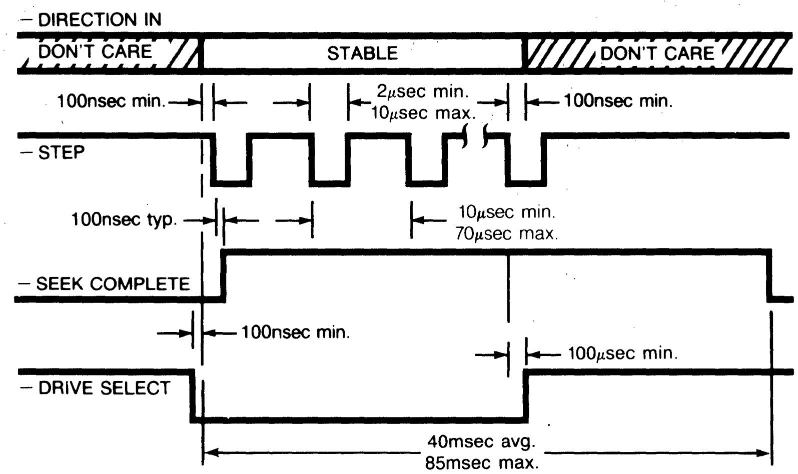
DIRECTION IN must be stable 100 nsec. before the leading edge of the first step pulse and remain stable for 100 nsec. after the last pulse in a string of Step pulses. Step pulses issued between 70 μsec. and 3 msec. may be lost.

If excessive Step pulses are issued which would cause a seek inward beyond Cylinder 733 or outward beyond Cylinder Zero, the drive will enter the Auto-Truncation mode. Refer to *Section 4.3.4.*

4.3.1 BUFFERED SEEK

To minimize access time, pulses may be issued at an accelerated rate and buffered in a counter. Initiation of the seek starts immediately after the first pulse is received and continues during pulse accumulation. The seek is completed following receipt of all pulses.

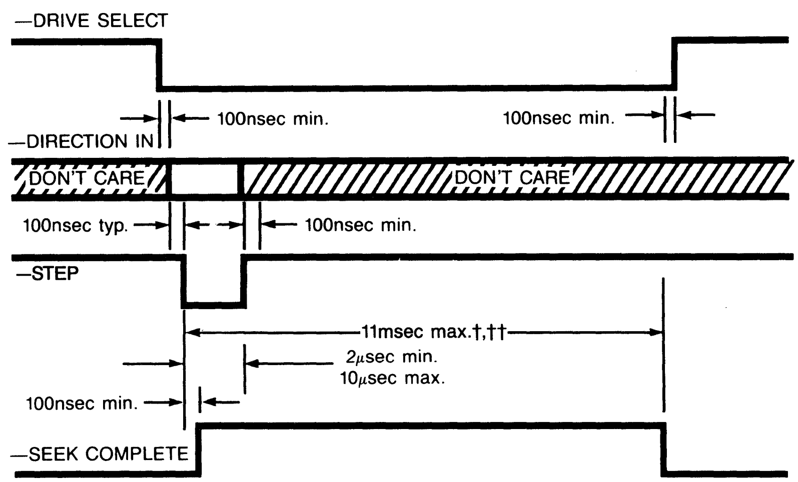
FIGURE 12:
Buffered-Seek Timing



SLOW-STEP (Track-To-Track) 4.3.2

In Slow-Step, the servo motor is settled and SEEK COMPLETE is issued 11 msec. max. after the leading edge of the Step pulse.

FIGURE 13:
Slow-Step Timing



† Assumes drive maintains velocity at incoming pulse rate.
†† For multiple-track, time depends on length of seek.

4.3.3 SEEK-RETRY

Seek-Retry is an internally generated command and is implemented by the drive to enhance seek performance.

If the drive detects an off-track condition, or the seek cannot be completed, the drive will recalibrate the heads to Track Ø and retry the seek. All writing is inhibited during retry.

If the target track is still not achieved, or the seek was not completed, the drive will set WRITE FAULT true, and READY and SEEK COMPLETE false. WRITE FAULT will remain active until the condition which caused the fault is corrected and the reset is completed.

4.3.4 AUTO-TRUNCATION

The drive will enter the Auto-Truncation mode if the controller issues an excessive number of Step pulses, which would place the Read/Write heads outward beyond Track Ø or inward beyond cylinder 733.

With Auto-Truncation active, the drive disallows additional pulses, takes control of the servo motor and recalibrates the heads to Track Ø.

CAUTION: If the controller is still issuing Slow-Step pulses after the ST4038 issues SEEK COMPLETE from Auto-Truncation mode, the drive will either reenter Auto-Truncation mode with DIRECTION IN false, or step the remaining cylinders with DIRECTION IN true.

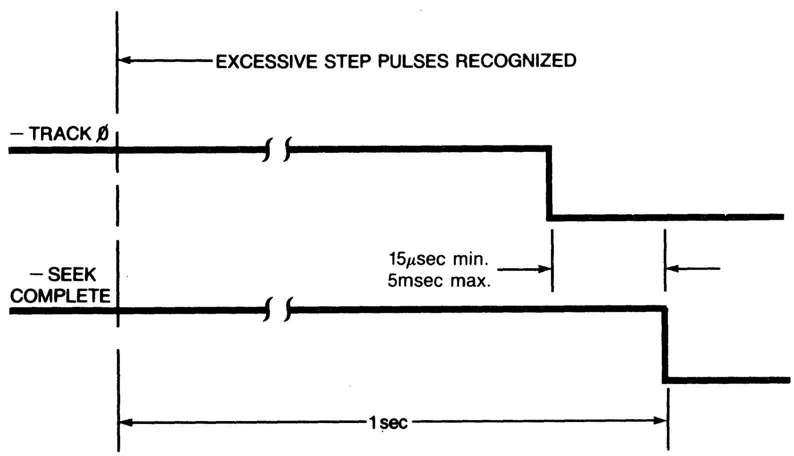


FIGURE 14: Auto-Truncation Timing

4.4 DIRECTION IN

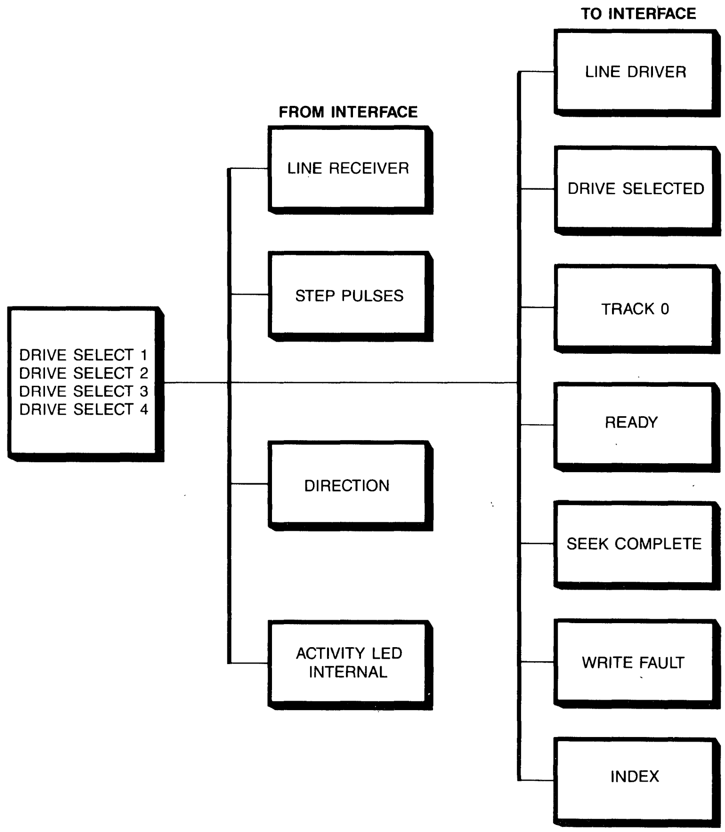
DIRECTION IN defines the direction the Read/Write heads will move when the STEP line is pulsed. With DIRECTION IN true, each pulse causes the heads to move one cylinder inward toward the spindle.

When DIRECTION IN is false, each pulse causes the heads to move one cylinder outward toward Track Ø.

DRIVE SELECT 4.5

The DRIVE SELECT line is activated by the host/controller to select and address the drive. Refer to *Section 3.0.*

FIGURE 15: Drive Select



5.0 CONTROL OUTPUT SIGNALS

The control output signals are gated to the interface when selected. The control output signals are DRIVE SELECTED, INDEX, TRACK Ø, READY, SEEK COMPLETE and WRITE FAULT.

5.1 DRIVE SELECTED

DRIVE SELECTED is a status signal transmitted over J2, which informs the host system of the selection status of the drive. The signal is driven by a TTL open collector, as illustrated in *Figure 10.* The signal goes low (true) on the interface only when the device is correctly configured (see *Sections 3.1-3.2*) and the DRIVE SELECT line is activated by the host system.

5.2 INDEX

This signal is provided by the drive once each revolution (16.67 msec. nominal) to indicate the beginning of a track. Normally this signal is at a high level and makes the transition to low to indicate INDEX. Only the transition from high to low, or the leading edge, is valid.

During power-on, INDEX is not available until the Read/Write heads have moved out of the shipping zone.

5.3 TRACK Ø

This signal is low (true) only when the Read/Write heads are positioned at Cylinder Zero.

Track Ø is the only cylinder that provides interface recognition. The drive is designed to recalibrate to Track Ø during power-on and Auto-Truncation operations.

Track Ø may also be accessed via conventional Buffered-Seek and Slow-Step modes. After Track Ø is true, no actions may be taken by the controller until SEEK COMPLETE is also true.

5.4 READY

This signal, when true together with SEEK COMPLETE, indicates that the drive is ready to Read, Write or Step and that all control input signals are valid. When this line is high, all reading, writing and stepping are inhibited. The maximum time after power-on for READY to be true is 20 seconds.[12]

READY remains false during the power-up sequence until:

1. The recalibration to Track Ø is complete
2. Spindle speed is stable within ± 0.5% of nominal
3. Drive initialization routines are complete
4. DC voltages are within tolerance

12. The specified 20 seconds max. time interval is calculated from the point that the power supply voltages are within the ±5% voltage tolerance.

SEEK COMPLETE 5.5

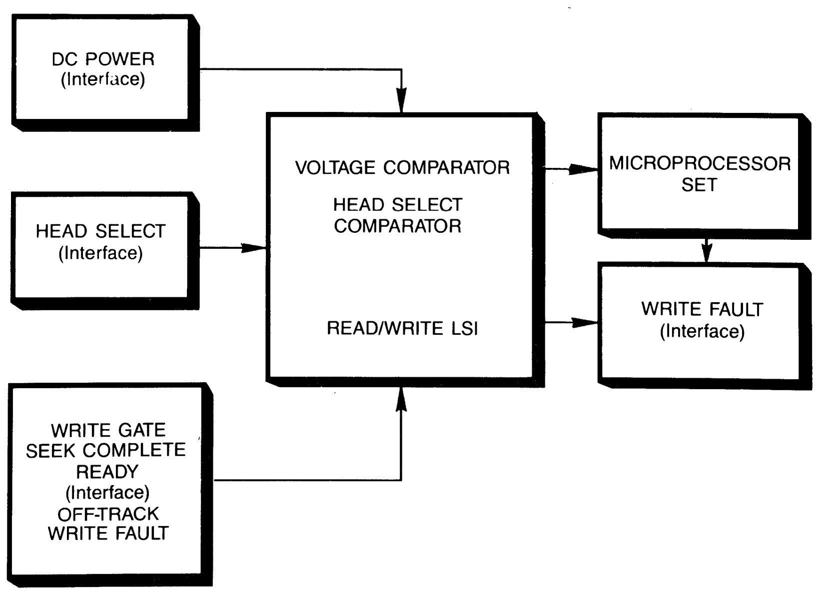
This signal goes to a low level on the interface when the Read/Write heads have settled on the target track upon completion of a seek. Seeking, reading or writing should not be attempted when SEEK COMPLETE is false. SEEK COMPLETE goes false in the following four cases:

1. When a recalibration sequence is initiated (by drive logic) at power-on
2. 100 nsec. max. after the leading edge of a Step pulse
3. If either +5 Volts or +12 Volts are detected as unsafe
4. If the drive attempts a Seek-Retry after settling on a track

WRITE FAULT 5.6

This signal notifies the host system that a condition exists at the drive which, if not corrected, would cause improper writing on the disc. WRITE FAULT will remain true until the condition causing the fault is corrected and a power-off/on reset is completed.

FIGURE 16: Fault Detection Flow



WRITE FAULT SIGNAL GENERATION 5.6.1

With DRIVE SELECT active, and one of the following conditions true, the WRITE FAULT signal will be issued to the interface and Write Current will be inhibited.

1. Write Gate true with no Write Current flowing to the head
2. Write Current to the heads with no Write Gate
3. The drive attempts more than one Seek-Retry

5.6.1.1 WRITE CURRENT INTERRUPTION

Any of the following conditions will cause Write Current to be inhibited when Write Gate is true:

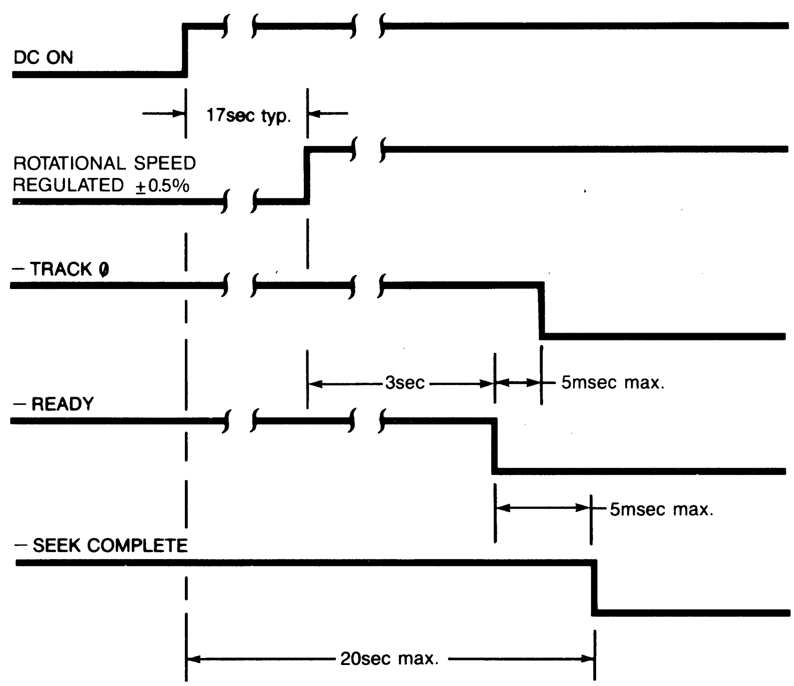
1. Multiple heads selected
2. No head selected
3. SEEK COMPLETE false
4. READY false
5. DC-Unsafe true (see *Section 3.4*)
6. A Step pulse is received
7. The Read/Write heads are significantly off-track

6.0 POWER-ON SEQUENCE

The application of DC power initiates a sequence which starts and regulates the spindle motor, recalibrates the Read/Write heads to Track Ø and issues READY and SEEK COMPLETE sequentially to terminate the sequence.

READY and SEEK COMPLETE are issued to the interface when the drive is available to accept commands. Upon power-up, the drive is available to accept commands 20 seconds max. after the power supply voltages maintain the specified tolerance.

FIGURE 17: Typical Power-On Sequence



7.0 DATA TRANSFER LINES

Two pairs of balanced signals are used for the transfer of data: MFM WRITE DATA and MFM READ DATA. All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed.

These lines are provided at the J2 connector. Refer to *Figure 18* for the data signal driver/receiver combination.

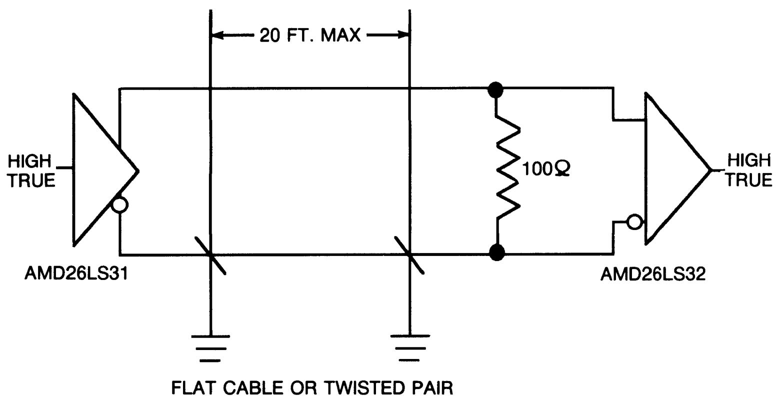


FIGURE 18: Data Signal Driver/Receiver Combination

8.0 READ/WRITE OPERATIONS

WRITE OPERATION 8.1

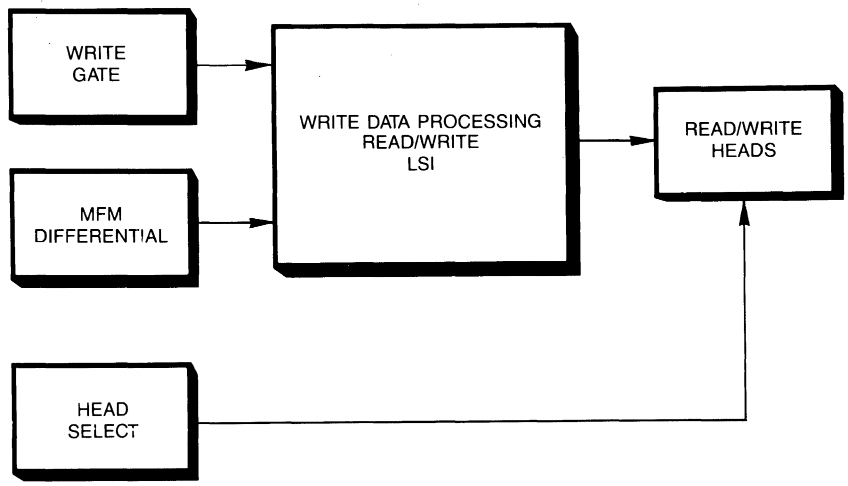


FIGURE 19: Write Operation Flow

In order to Write, the following conditions must be satisfied:

WRITE FAULT inactive
SEEK COMPLETE active
READY active
DRIVE SELECT active
Write Gate active

MFM WRITE DATA 8.1.1

WRITE DATA is transmitted by a differential pair which defines the transitions to be written on the disc. The +MFM WRITE DATA line going more positive than the -MFM WRITE DATA line is the active transition. This signal must be driven to an inactive state when in READ mode.

WRITE GATE 8.1.2

A Write sequence is initiated when Write Gate is activated which causes the Read/Write LSI to apply +12 Volts to the selected head's center tap. Data is then sent to the Read/Write LSI.

WRITE DATA PROCESSING 8.1.3

The Read/Write LSI receives Differential MFM Write data and transforms it to single line pulse data. Depending whether plus or minus data is to be written, the Read/Write LSI activates the preamp LSI.

As the Read/Write heads travel inward, the circumference of the tracks, of course, decreases and the bits are necessarily written closer together. The Write Current is therefore reduced at specific cylinders to reduce pulse crowding. The reduction is linear and occurs at cylinders 183, 266 and 549. The amount of current to be written is established by the Reduced Write Current circuit.

The ST4038 does not require the host system to specify the Reduced Write Current Cylinders. This function is managed internally by the MPU.

8.1.4 PRECOMPENSATION

Precompensation is recommended on cylinders 300 through 732 in order to achieve optimum performance. The optimum amount of precompensation is 12 nsec. for both early and late bits. *Table 3* indicates the bit patterns and the direction to be compensated. An **X** denotes a "don't care" state.

TABLE 3: Precompensation Pattern

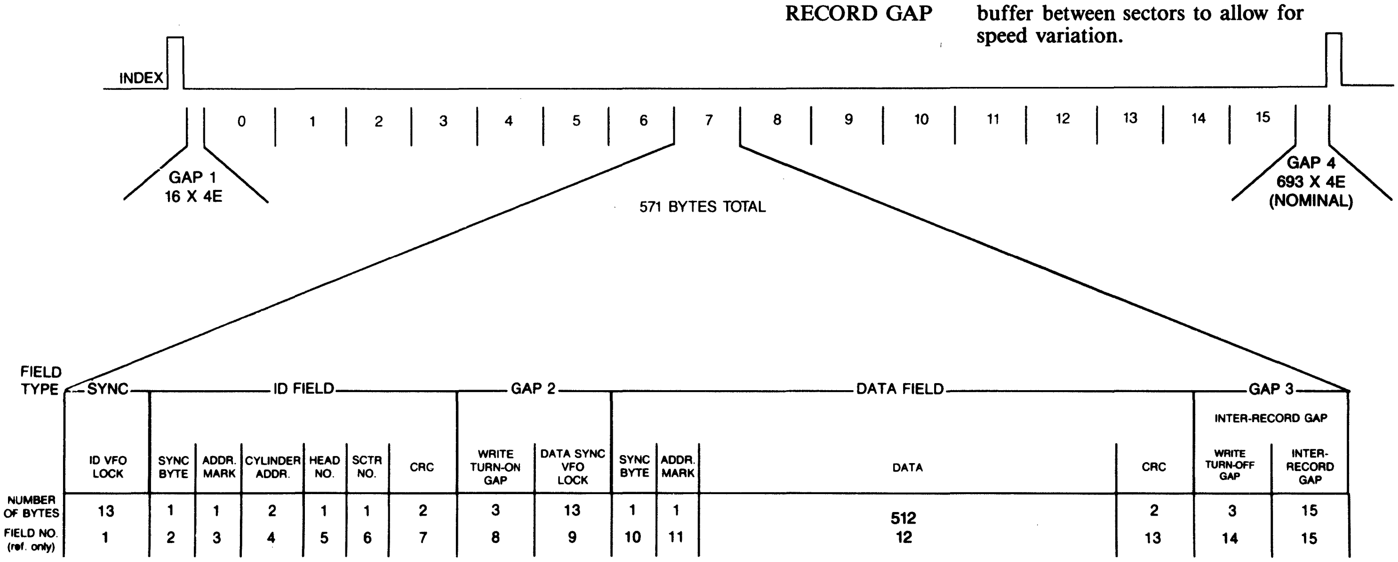
PREVIOUS		SENDING	NEXT	TIMING
X	0	1	1	WRITE DATA LATE
X	1	1	0	WRITE DATA EARLY
1	0	0	0	WRITE CLOCK LATE
0	0	0	1	WRITE CLOCK EARLY

ALL OTHER PATTERNS NOMINAL

Figure 20 illustrates a suggested format example.

FIGURE 20: 17 Sector, 512-Byte/Sector Format Example

REFERENCE NUMBER	NUMBER OF BYTES	FIELD NAME	FIELD DESCRIPTION
1	13	ID VFO LOCK	A field of all zeros to sync the VFO for the ID
2	1	SYNC BYTE	"A1" Hex with a dropped clock to notify the controller that data follows.
3	1	ADDRESS MARK	"FE" Hex defining that ID field data follows.
4	2	CYLINDER NUMBER	A numerical value in Hex defining the detent position of the actuator.
5	1	HEAD NUMBER	A numerical value in Hex defining the head selected.
6	1	SECTOR NUMBER	A numerical value in Hex defining the sector for this section of the rotation.
7	2	CRC	Cyclic Redundancy Check information used to verify the validity of the ID field information just read.
8	3	WRITE TURN-ON GAP	Zeros written during format to isolate the write splice created. This field assures valid reading of field number 7 and allows the 13 bytes required for Data VFO lock.
9	13	DATA SYNC VFO LOCK	A field of all zeros to sync the VFO for the data field.
10	1	SYNC BYTE	"A1" Hex with a dropped clock to notify the controller that data follows.
11	1	ADDRESS MARK	"F8" Hex defining that user data follows.
12	512	DATA	This area available for user data.
13	2	CRC	Cyclic Redundancy Check information used to verify the validity of the user data field information just read.
14	3	WRITE TURN-OFF GAP	Zeros written during update to isolate the write splice created. This field assures valid reading of field number 13 and allows the 13 bytes required for VFO lock for the ID field of the next sector.
15	15	INTER RECORD GAP	A field of all zeros which acts as a buffer between sectors to allow for speed variation.



8.2 READ OPERATION

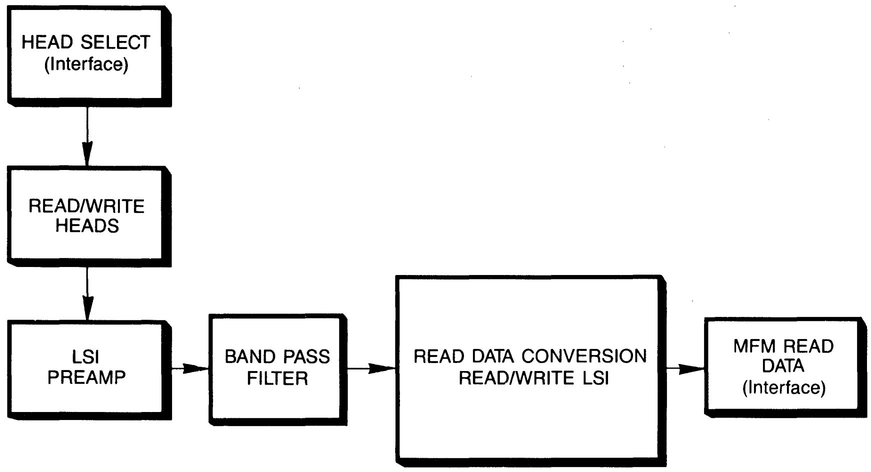


FIGURE 21:
Read Operation Flow

8.2.1 MFM READ DATA

The data recovered by reading a prerecorded track is transmitted to the host system by a differential pair of MFM READ DATA lines. The transition of the +MFM READ DATA line going more positive than the -MFM READ DATA line represents a flux reversal on the track of the selected head.

8.2.2 HEAD SELECT

The Binary Decoder selects the Read/Write head based on the status of the Head Select lines, 2^0, 2^1 and 2^2.

Head Select 2^3 is an invalid signal for the ST4038. This line is present on the interface, but is terminated. The drive will not respond to this input signal.

During Read operations the Read/Write head center tap (HCT) is set at approximately +5 Volts by the Read/Write LSI.

8.2.3 LSI PREAMP

With the HCT active, data from the selected head will flow into the preamp which amplifies the signal and also acts as a high-pass filter.

8.2.4 BAND PASS FILTER

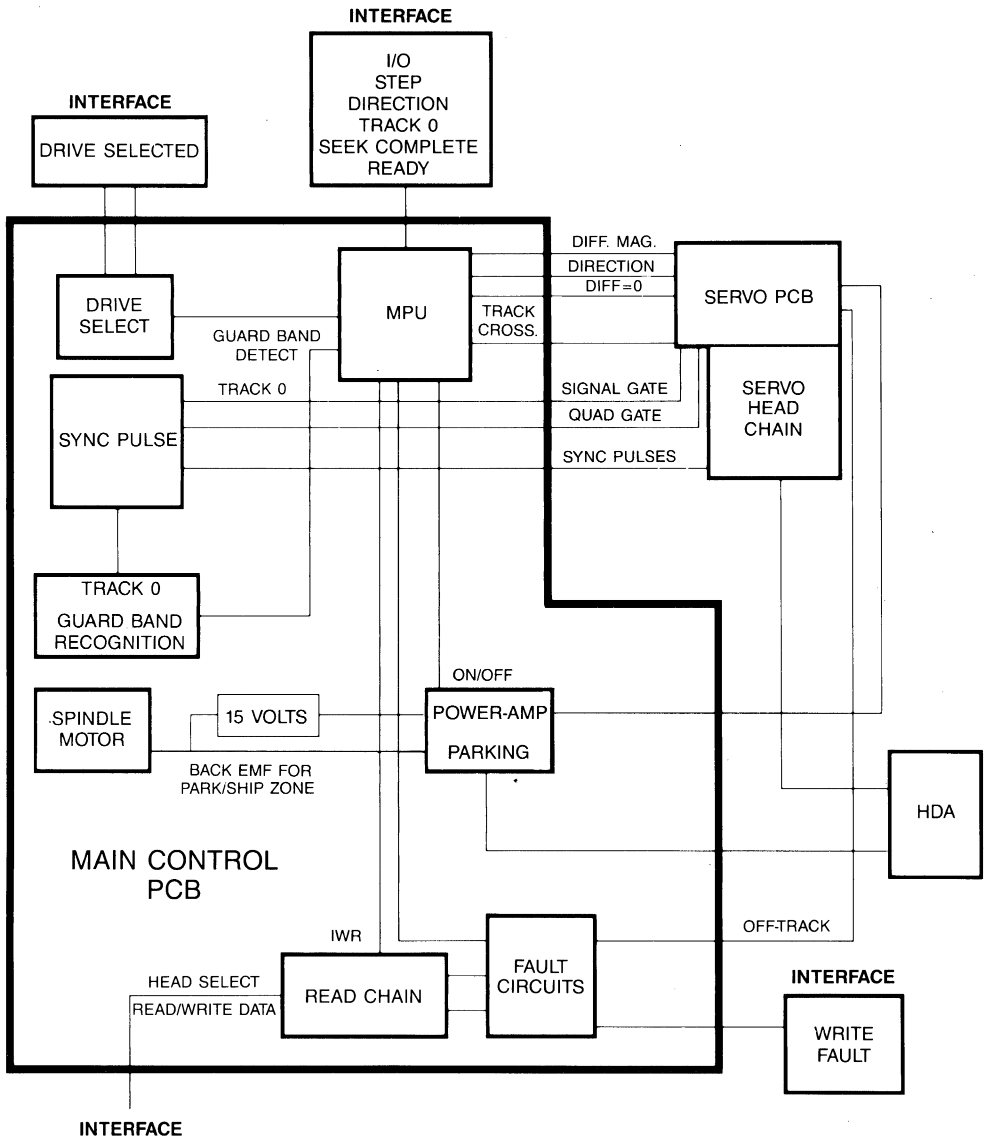
This filter network attenuates high frequency noise, which is outside the normal data signal range.

8.2.5 READ DATA CONVERSON

Amplified Read data enters the Read/Write LSI and exits as high speed MFM (differential) Read data. The Read/Write LSI functions are:

- Differentiate Read data and shift 90°
- Analog to digital conversion via a zero-cross detector
- Remove erroneous data bits
- Convert digital data to differential MFM data, thereby providing immunity to common mode noise during transmission

FIGURE 22:
ST4038 Control
and Servo PC Boards



9.0 GENERAL THEORY OF OPERATION

9.1 MICROPROCESSOR

The ST4038 employs a microprocessor to monitor and control internal drive functions and host interface lines. The MPU has three active modes: Initializing, Seeking and Waiting.

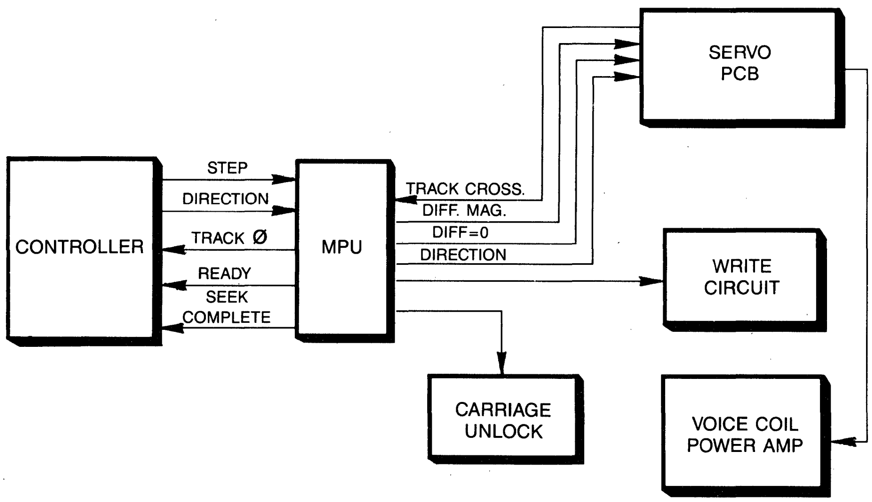


FIGURE 23: MPU

9.1.1 INITIALIZING

At Power-on:

- The MPU initializes the interface
- Checks the WRITE FAULT circuit
- Monitors the spindle motor speed during spin-up via the Hall sensor in the motor hub and, when up-to-speed, via Index pulses written on the servo surface.

Once the drive is at speed, the MPU will power-up the servo motor (linear voice-coil actuator), disengage the carriage lock and recalibrate the Read/Write heads to Track Ø.

The drive will then check the WRITE FAULT circuit, monitor Index, update the Interface and send READY and SEEK COMPLETE. The drive is then available to accept commands from the host.

9.1.2 SEEKING

During the seek mode the MPU will:

- Count the incoming Step pulses
- Check the host DIRECTION line and set the servo DIRECTION line
- Monitor track crossing pulses
- Monitor the guard-band detection circuit

EXECUTING A SEEK 9.1.2.1

The MPU loads the destination track number into the track-counting circuit. There is now a difference between the current position and the target track.

If, for example, the Read/Write heads were at track 200 and a seek was required to track 350, this would be a difference of 150. This difference magnitude causes the servo circuit to input a seek velocity proportional to this difference. A large difference magnitude would translate into a longer seek and a higher actuator velocity would be required.

As tracks are crossed, the MPU monitors and counts the track crossing pulses, which the servo circuit generates from the servo surface. The difference counter is updated and decremented by the MPU. As the destination track approaches, the difference approaches zero. When the digital to analog convertor (DAC) reads zero, the servo circuit assumes "on target track" and initiates a track following routine (i.e., difference=0).

The information written to the servo surface is for position feedback only and does not supply a specific "address" toward which the Read/Write heads are seeking.

The seeking speed of the servo motor does not decrease directly proportional to the decrease in the difference magnitude; on a long seek it is necessary for the actuator to accelerate quickly, maintain optimum speed and decelerate only as the target track approaches.

Optimum acceleration/deceleration trajectories are calculated in the square root generator. During a typical one-third stroke the acceleration pattern will be approximately triangular.

WAITING MODE 9.1.3

During this mode, the drive will monitor INDEX via the servo surface, monitor for track-crossing pulses and sample the guard-band detect circuit. If track-crossing pulses are received, indicating that the Read/Write heads have drifted off-center from the target track, SEEK COMPLETE is dropped and the drive initiates action to return to the target track. The interface is then updated.

The ST4038 employs a quadrature signal servo system. The servo information is written on a single dedicated surface. When in the track-following mode, the drive is monitoring the servo surface for a nulling signal indicating that the Read/Write heads are on the target track. A variation in signal amplitude will indicate an off-track condition and the servo circuit will initiate action to return to the target track. When seeking, the servo head monitors the track-crossing pulses, which provide continuous position feedback.

10.0 SERVO THEORY OF OPERATION

10.1 TRACK Ø and GUARD-BANDS

Track Ø information is monitored via the servo surface and processed on the Main Control PCB. Outboard of Track Ø and inboard of the shipping zone are guard-bands to alert the MPU that the Read/Write heads are traveling beyond the area of normal operation. If the heads enter the guard-bands, power to the servo motor is interrupted and a recalibration to Track Ø is initiated.

10.2 TRACK FOLLOWING

When in the track-following mode, the servo-feedback loop is monitoring for a known null condition, or least variation in signal amplitude. Cells, which contain North-South or South-North transitions, are written to the servo surface. These transitions are monitored and commutated into a predictable pattern. The servo circuit interprets this signal for position feed-back. A variation indicates an off-track condition. When the servo head is positioned as illustrated in *Figure 24,* a null condition exists.

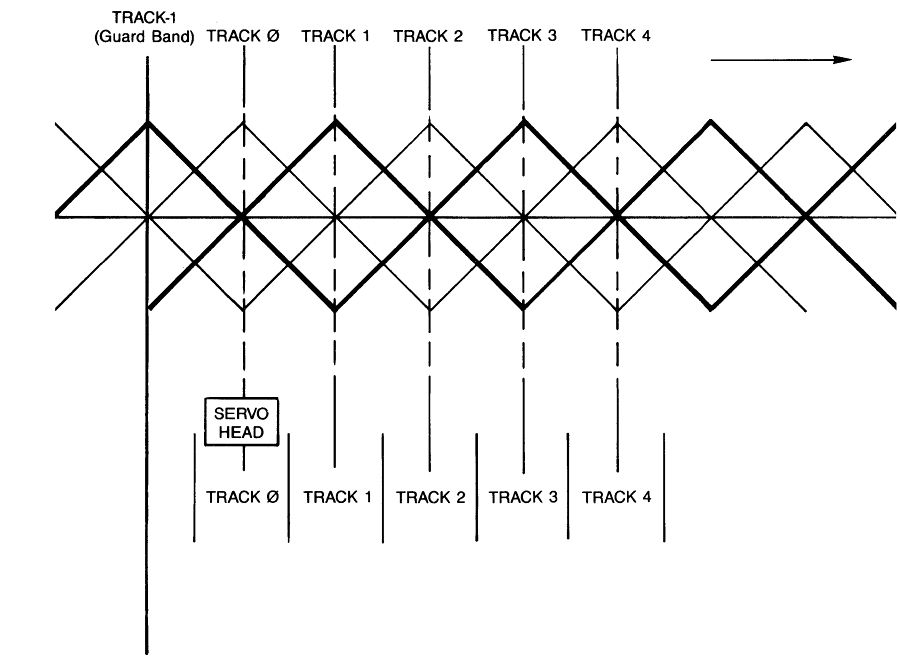
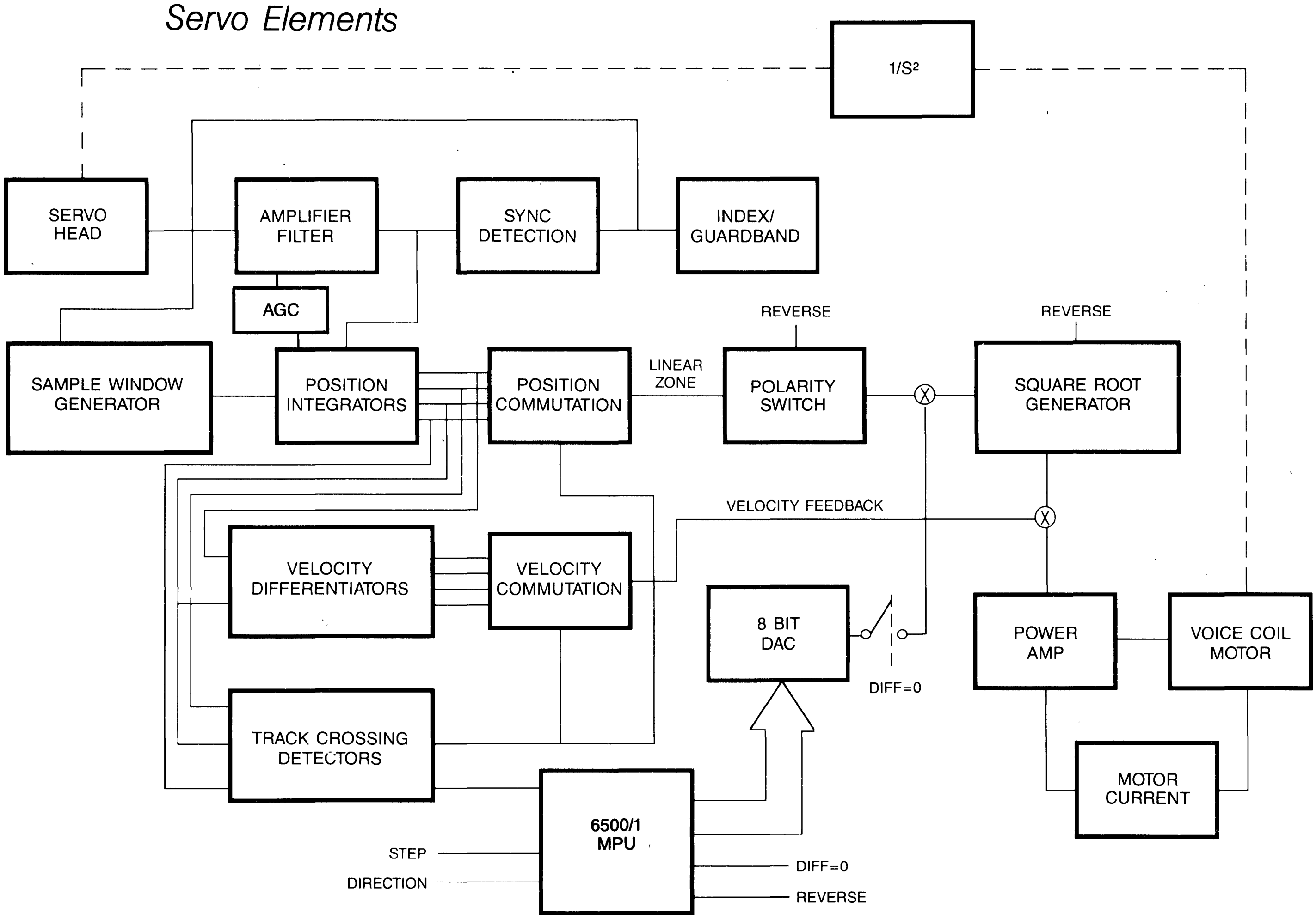


FIGURE 24: Position and Quad Error Signals

FIGURE 25: Servo Elements



11.0 MECHANICAL

11.1 LINEAR VOICE-COIL ACTUATOR

A voice-coil actuator is essentially a copper wound coil which surrounds a magnetic pole assembly. Simply stated, it is a moving coil within a magnetic field. The operation is similar to an audio speaker voice-coil. As current is fed into the coil, the carriage moves according to the right-hand rule, and the greater the current—the higher the velocity.

The actuator is a low-mass integrated coil/carriage assembly incorporating six bearings. The four lower bearings ride on a fixed cylindrical way and the upper two ride on a preloaded cylindrical way. Because the frame must provide a return path for the magnetic flux, it is relatively massive compared to the rest of the assembly.

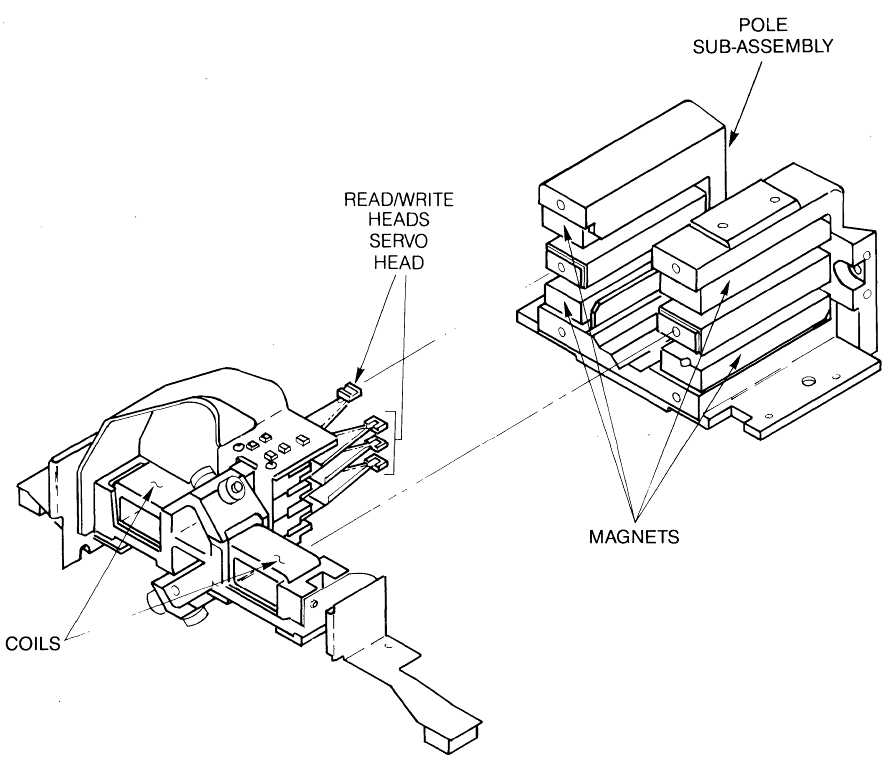


FIGURE 26: ST4038 Linear Actuator

11.2 AIR FILTRATION SYSTEM

The ST4038 employs a captured-air-space recirculation system. The 0.3 micron filter maintains Class 100 standards within the sealed head/disc assembly (HDA) and requires no maintenance during the life of the drive. A filtered port permits ambient pressure equalization. During normal operations there is no measurable flow of air between the HDA and the outside environment.

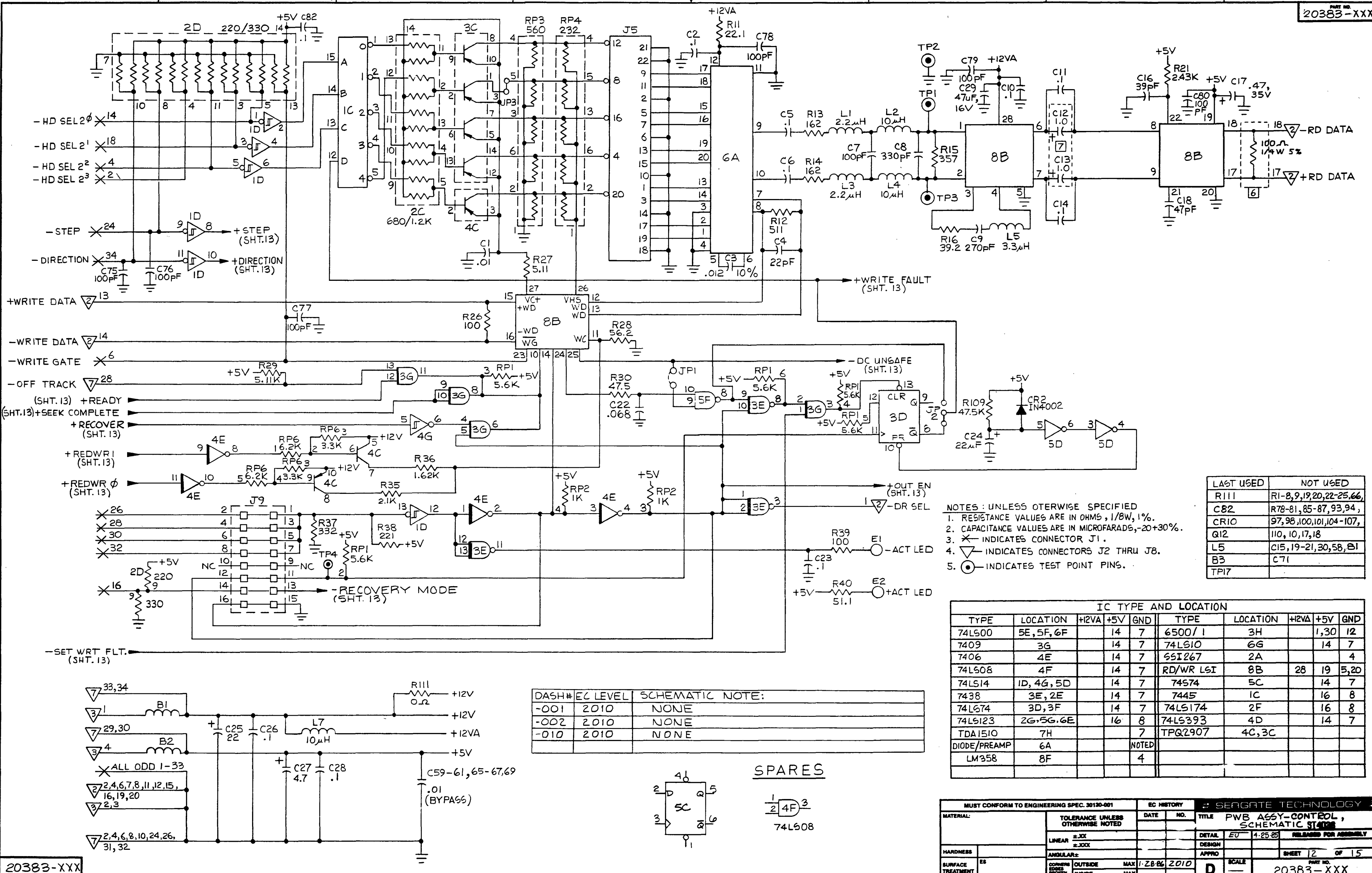
READ/WRITE HEADS AND SERVO HEAD 11.3

The Read/Write heads and servo head fly on an air bearing created by the rotating disc. The heads are loaded toward the disc surface so that stability is maintained in all approved mounting orientations. Flying height measured at the inner radius is typically 15 microinches and 25 microinches at the outer radius.

The ST4038 does not require any preventative maintenance. The HDA is sealed and Seagate will consider a unit to be out of warranty if the seal has been broken. Should a drive require service, consult your distributor or your regional field sales office.

Rough handling accounts for more Winchester drive damage than all other factors combined. Your ST4038 is designed for consistent and reliable service across a wide range of environmental factors. It is, however, a precision instrument and when transporting or shipping a unit please ensure that the drive is correctly packed in the original Seagate (or approved substitute) container.

12.0 SCHEMATICS, COMPONENT LOCATIONS



NOTES : UNLESS OTERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS , 1/8W, 1%.
2. CAPACITANCE VALUES ARE IN MICROFARADS,-20+30%.
3. ✕— INDICATES CONNECTOR J1 .
4. ▽— INDICATES CONNECTORS J2 THRU J8.
5. ⊙— INDICATES TEST POINT PINS.

LAST USED	NOT USED
R111	R1-8,9,19,20,22-25,66,
C82	R78-81,85-87,93,94,
CR10	97,98,100,101,104-107,
Q12	110, 10,17,18
L5	C15,19-21,30,58,81
B3	C71
TP17	

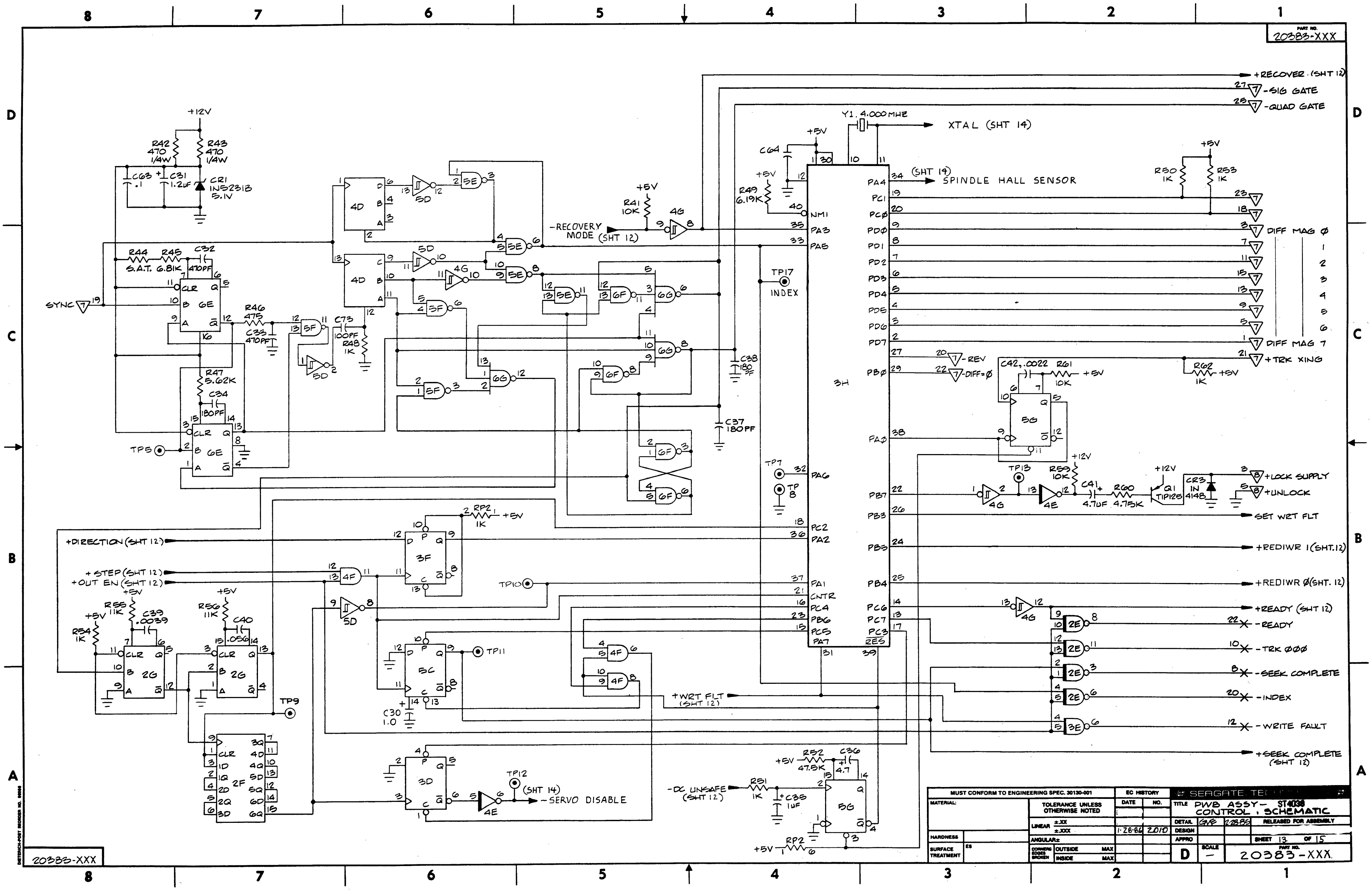
DASH#	EC LEVEL	SCHEMATIC NOTE:
-001	2010	NONE
-002	2010	NONE
-010	2010	NONE

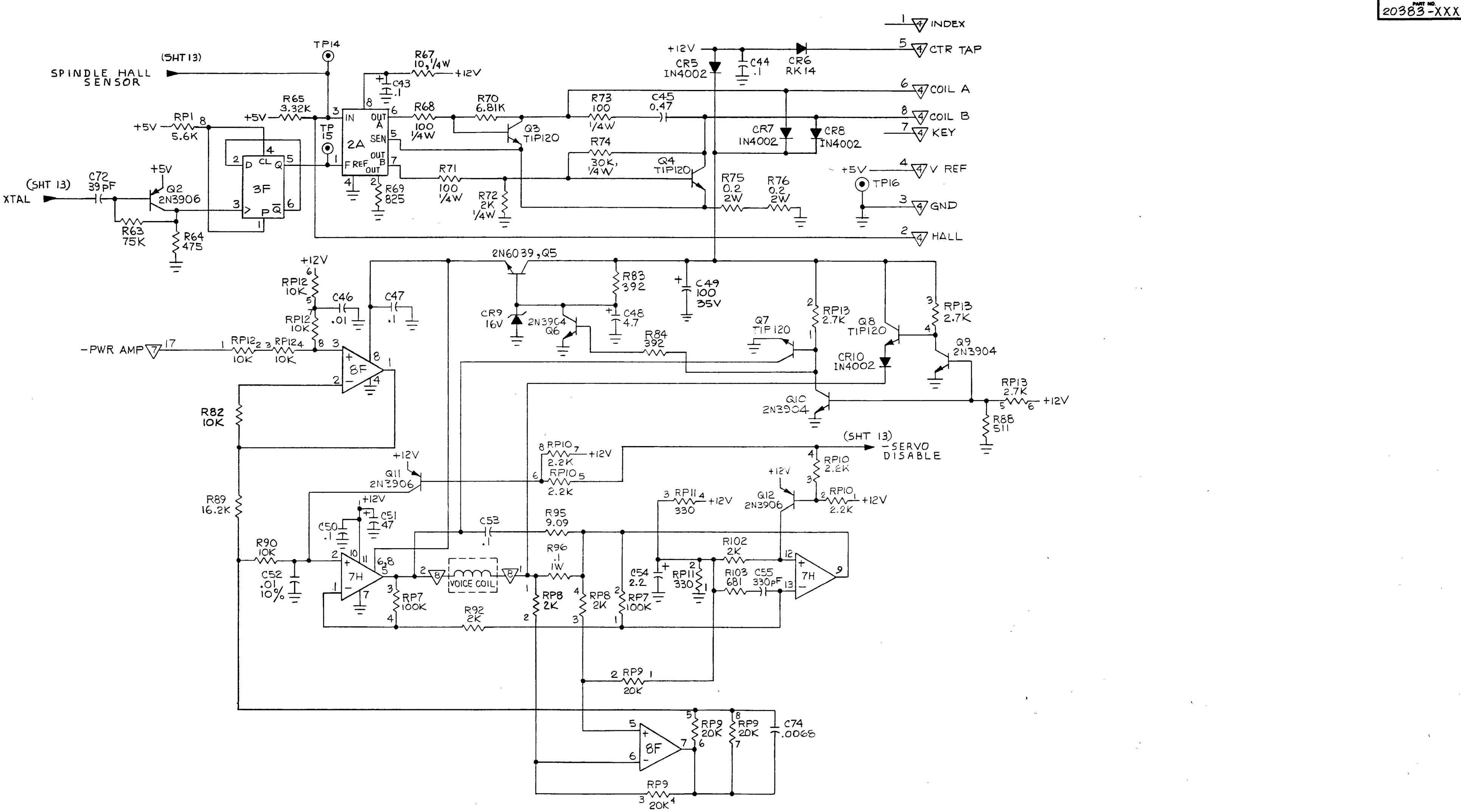
IC TYPE AND LOCATION

TYPE	LOCATION	+12VA	+5V	GND	TYPE	LOCATION	+12VA	+5V	GND
74LS00	5E, 5F, 6F		14	7	6500/1	3H		1,30	12
7409	3G		14	7	74LS10	6G		14	7
7406	4E		14	7	SSI267	2A			4
74LS08	4F		14	7	RD/WR LSI	8B	28	19	5,20
74LS14	1D, 4G, 5D		14	7	74S74	5C		14	7
7438	3E, 2E		14	7	7445	1C		16	8
74LS74	3D, 3F		14	7	74LS174	2F		16	8
74LS123	2G,5G,6E		16	8	74LS393	4D		14	7
TDA1510	7H			7	TPQ2907	4C, 3C			
DIODE/PREAMP	6A			NOTED					
LM358	8F			4					

MUST CONFORM TO ENGINEERING SPEC. 30120-001		EC HISTORY		SEAGATE TECHNOLOGY	
MATERIAL:	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE PWB ASSY-CONTROL, SCHEMATIC ST[redacted]	
	LINEAR ±.XX ±.XXX			DETAIL EU 4-25-85	RELEASED FOR ASSEMBLY
				DESIGN	
HARDNESS	ANGULAR±			APPRO	SHEET 12 OF 15
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX / INSIDE MAX	1-28-86	2010	D SCALE —	PART NO. 20383-XXX

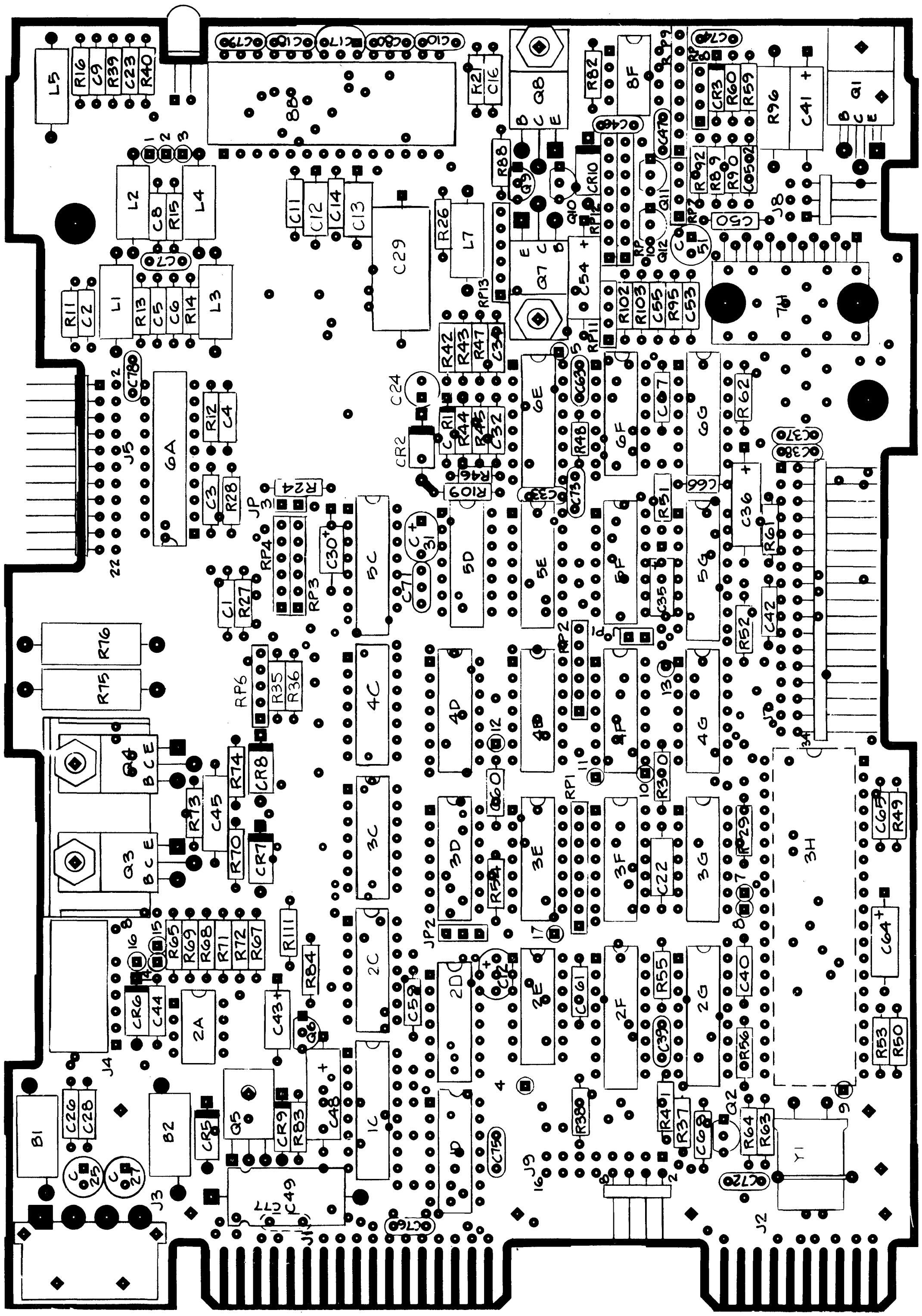
20383-XXX


20383-XXX
+RECOVER (SHT 12)
-SIG GATE
-QUAD GATE
Y1 4.000 MHZ
XTAL (SHT 14)
(SHT 14) SPINDLE HALL SENSOR
-RECOVERY MODE (SHT 12)
TP17 INDEX
DIFF MAG Ø
DIFF MAG 7
+TRK XING
-REV
-DIFF=Ø
SYNC
+LOCK SUPPLY
+UNLOCK
SET WRT FLT
+REDIWR 1 (SHT. 12)
+REDIWR Ø (SHT. 12)
+READY (SHT 12)
-READY
-TRK ØØØ
-SEEK COMPLETE
-INDEX
-WRITE FAULT
+SEEK COMPLETE (SHT 12)
+DIRECTION (SHT 12)
+STEP (SHT 12)
+OUT EN (SHT 12)
+WRT FLT (SHT 12)
-DC UNSAFE (SHT 12)
(SHT 14) -SERVO DISABLE
MUST CONFORM TO ENGINEERING SPEC. 30130-001
TOLERANCE UNLESS OTHERWISE NOTED
SEAGATE TECHNOLOGY
TITLE PWB ASSY- ST4038 CONTROL, SCHEMATIC
RELEASED FOR ASSEMBLY
1-26-86 2010
SHEET 13 OF 15
D
20383-XXX

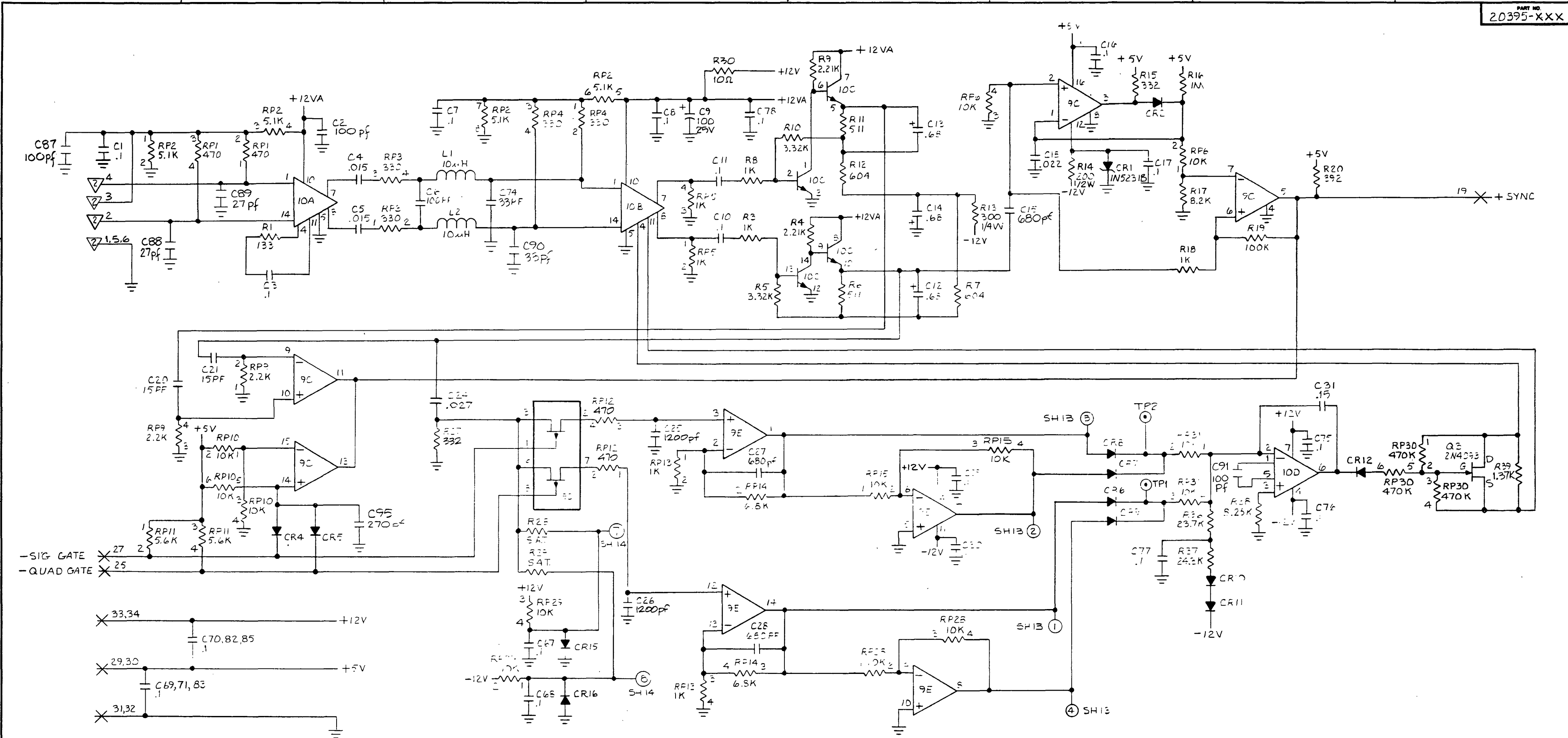


MUST CONFORM TO ENGINEERING SPEC. 30130-001		EC HISTORY		SEAGATE TECHNOLOGY
MATERIAL:	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.	TITLE PWB ASSY-CONTROL, SCHEMATIC ST4038
	LINEAR ±.XX ±.XXX			DETAIL EU 4-25-85 RELEASED FOR ASSEMBLY
HARDNESS	ANGULAR±	1-28-86	2010	APPRO SHEET 14 OF 15
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX			D SCALE PART NO. 20383-XXX

20383-XXX



20395-XXX



NOTES - UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS, 1/4W, 1%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. INDICATES CONNECTOR J1.
4. INDICATES CONNECTOR J2.
5. ALL DIODES ARE 1N4148.
6. COMPONENT NOT INSTALLED
7. VALUES OF R22 & R84 ARE: 14.3K FOR -001 VERSION, 20K FOR -010 VERSION
8. VALUE OF R73 ARE: 237K FOR -001 VERSION, 162K FOR -010 VERSION

REF DES	
LAST USED	NOT USED
CR17	
L4	
Q3	
R81	R2,55,80
RP31	
RT1	
C94	

I C CHART

TYPE	LOCATION	+12V	-12V	+5V	GND	TYPE	LOCATION	+12V	-12V	+5V	GND
74LS75	8F			5	12	HI-201HS-5	9D	13	4		5
						µA78S40	1E				3,10,11
74LS4[illegible]	[illegible]			16	8	T[illegible]3904	[illegible]				
74LS13[illegible]	5F			14	7	TPQ3[illegible]	[illegible]				
LM741E	1D,10D,2F,10F	7	4			AH5010	3F 10E				3,5,10,12
LF13333	1F	12	5		2,9,10						
LF347E	1E,2E,9E	4	11								
MC3452P	9C			16	4,8						
NE592	1CA,10E	10+12VA			5						
LM311	4E,7E	8	4		1						
DAC0808	2C		3	13	2						
LM339	9F	3	12								

DASH #	E.C. LEVEL	SCHEMATIC NOTE
010	1932	7
001	1932	7

MUST CONFORM TO ENGINEERING SPEC. 30130-001

EC HISTORY	
DATE	NO.
11-21-85	1932

MATERIAL:

TOLERANCE UNLESS OTHERWISE NOTED

LINEAR ±.XX ±.XXX

ANGULAR ±

HARDNESS

SURFACE TREATMENT ES

CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX

SEAGATE TECHNOLOGY

TITLE PWB ASSY - SERVO SCHEMATIC ST4038

DETAIL JRS 1-10-85

DESIGN

APPRO

RELEASED FOR ASSEMBLY

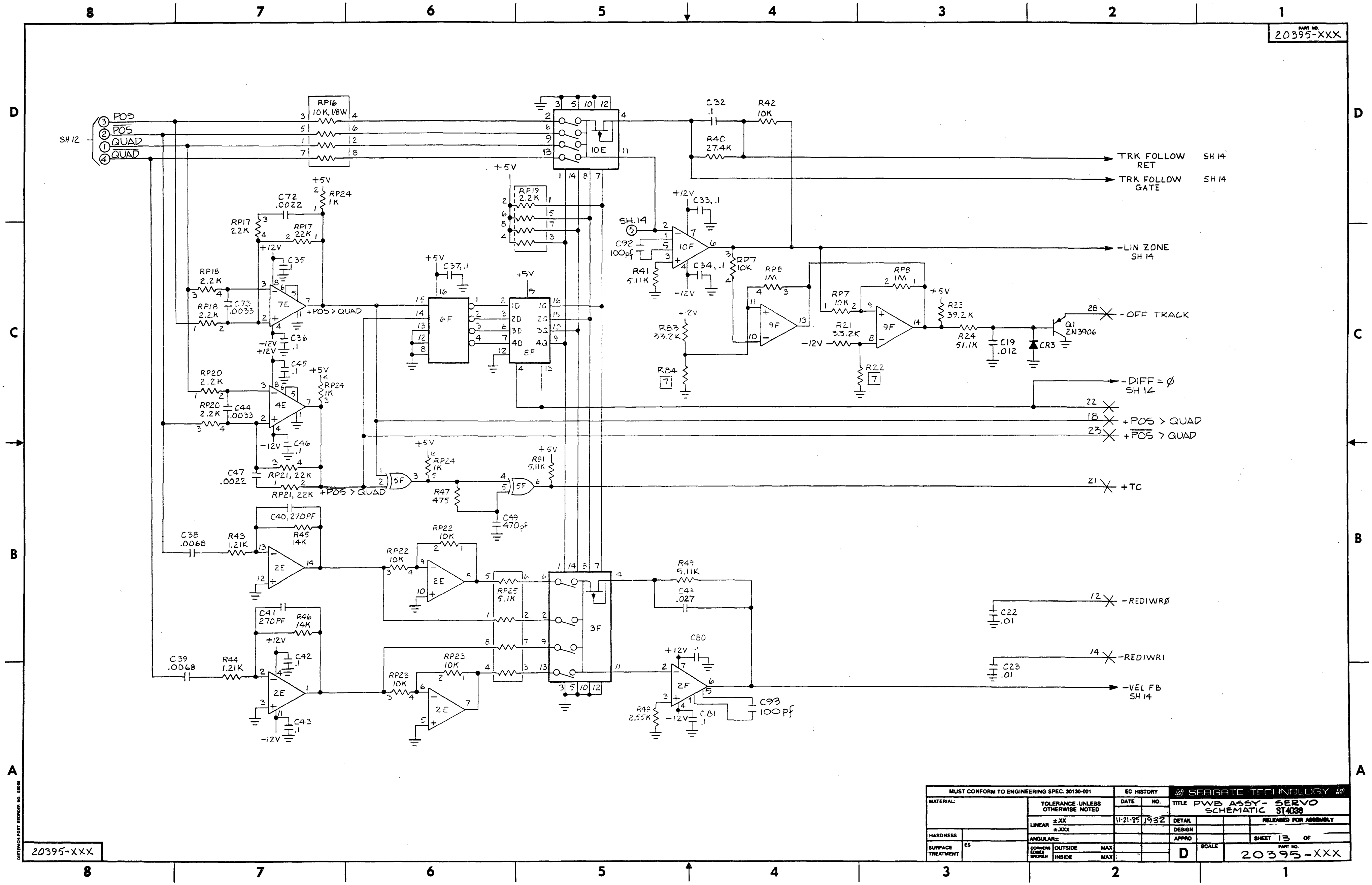
SHEET 12 OF

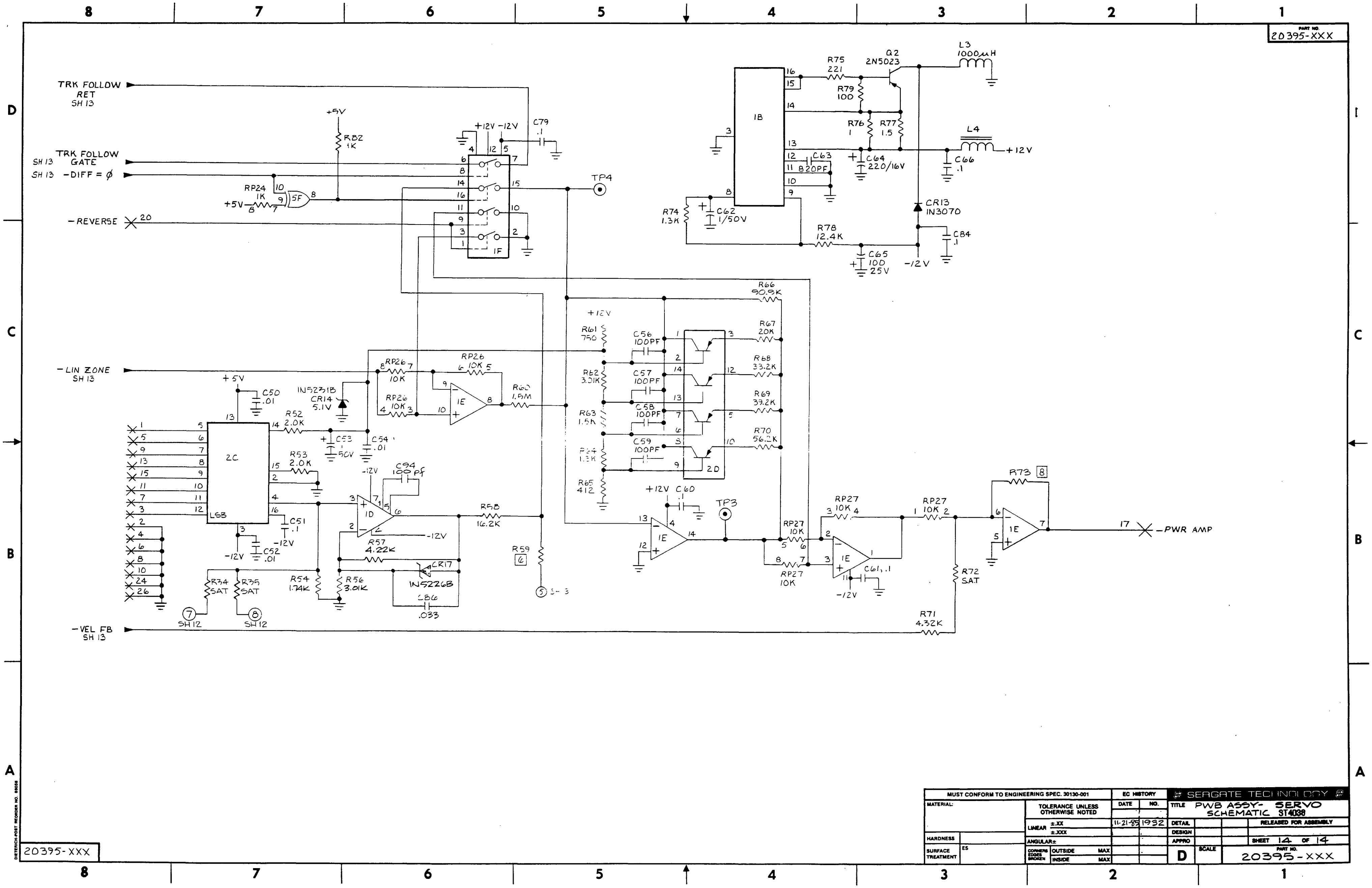
D

SCALE

PART NO. 20395-XXX

20395-XXX


20395-XXX
SH 12
POS
POS
QUAD
QUAD
RP16 10K, 1/8W
10E
C32 .1
R42 10K
R40 27.4K
TRK FOLLOW RET SH 14
TRK FOLLOW GATE SH 14
+5V
RP19 2.2K
RP24 1K
C72 .0022
RP17 2.2K
RP17 22K
+12V
C35 .1
RP18 2.2K
C73 .0033
RP18 2.2K
7E
+POS > QUAD
-12V
C36 .1
C37, .1
6F
8F
SH.14
C33, .1
C92 100pf
10F
R41 5.11K
C34, .1
R207 10K
-LIN ZONE SH 14
RP8 1M
RP7 10K
RP8 1M
9F
R21 33.2K
R23 39.2K
R24 51.1K
C19 .012
CR3
Q1 2N3906
-OFF TRACK
R83 33.2K
R84
R22
C45 .1
RP20 2.2K
4E
RP20 2.2K
C44 .0033
C46 .1
-DIFF = Ø SH 14
+POS > QUAD
+POS > QUAD
C47 .0022
RP21, 22K
RP21, 22K
+POS > QUAD
5F
R47 475
R51 5.11K
C49 470pf
+TC
C40, 270PF
R45 14K
C38 .0068
R43 1.21K
2E
RP22 10K
RP22 10K
RP25 5.1K
3F
R49 5.11K
C48 .027
-REDIWRØ
C22 .01
C41 270PF
R46 14K
C42 .1
C39 .0068
R44 1.21K
RP23 10K
RP23 10K
C80
2F
C93 100pf
R48 2.55K
C81 .1
C43 .1
-REDIWR1
C23 .01
-VEL FB SH 14
MUST CONFORM TO ENGINEERING SPEC. 30130-001
MATERIAL:
TOLERANCE UNLESS OTHERWISE NOTED
LINEAR ±.XX ±.XXX
ANGULAR ±
HARDNESS
SURFACE TREATMENT
EC HISTORY
DATE NO.
11-21-85 1932
SEAGATE TECHNOLOGY
TITLE PWB ASSY- SERVO SCHEMATIC ST4038
DETAIL
DESIGN
APPRO
RELEASED FOR ASSEMBLY
SHEET 13 OF
D
SCALE
PART NO. 20395-XXX
20395-XXX



20395-XXX
TRK FOLLOW RET SH 13
SH 13 TRK FOLLOW GATE
SH 13 -DIFF = Ø
-REVERSE
+5V
R82 1K
RP24 1K
5F
+12V -12V
C79 .1
1F
TP4
1B
R75 221
Q2 2N5023
L3 1000µH
R79 100
R76 1
R77 1.5
L4
+12V
C63 820PF
C64 220/16V
C66 .1
R74 1.3K
C62 1/50V
R78 12.4K
C65 100 25V
CR13 IN3070
C84 .1
-12V
R66 90.9K
R61 750
C56 100PF
R67 20K
R62 3.01K
C57 100PF
R68 33.2K
R63 1.5K
C58 100PF
R69 33.2K
R64 1.3K
C59 100PF
R70 56.2K
R65 412
2D
-LIN ZONE SH 13
+5V
C50 .01
RP26 10K
IN5231B CR14 5.1V
1E
R60 1.5M
2C
LS8
R52 2.0K
C53 50V
C54 .01
R53 2.0K
C94 100 pf
1D
R58 16.2K
R57 4.22K
CR17 IN5226B
C86 .033
R59 6
SH 3
C51 .1
C52 .01
R34 SAT
R35 SAT
R54 1.74K
R56 3.01K
SH12
+12V C60 .1
TP3
RP27 10K
C61 .1
R73 8
R72 SAT
R71 4.32K
-PWR AMP
-VEL FB SH 13
MUST CONFORM TO ENGINEERING SPEC. 30130-001
EC HISTORY
SEAGATE TECHNOLOGY
MATERIAL:
TOLERANCE UNLESS OTHERWISE NOTED
DATE NO.
11-21-85 1932
TITLE PWB ASSY- SERVO SCHEMATIC ST4038
RELEASED FOR ASSEMBLY
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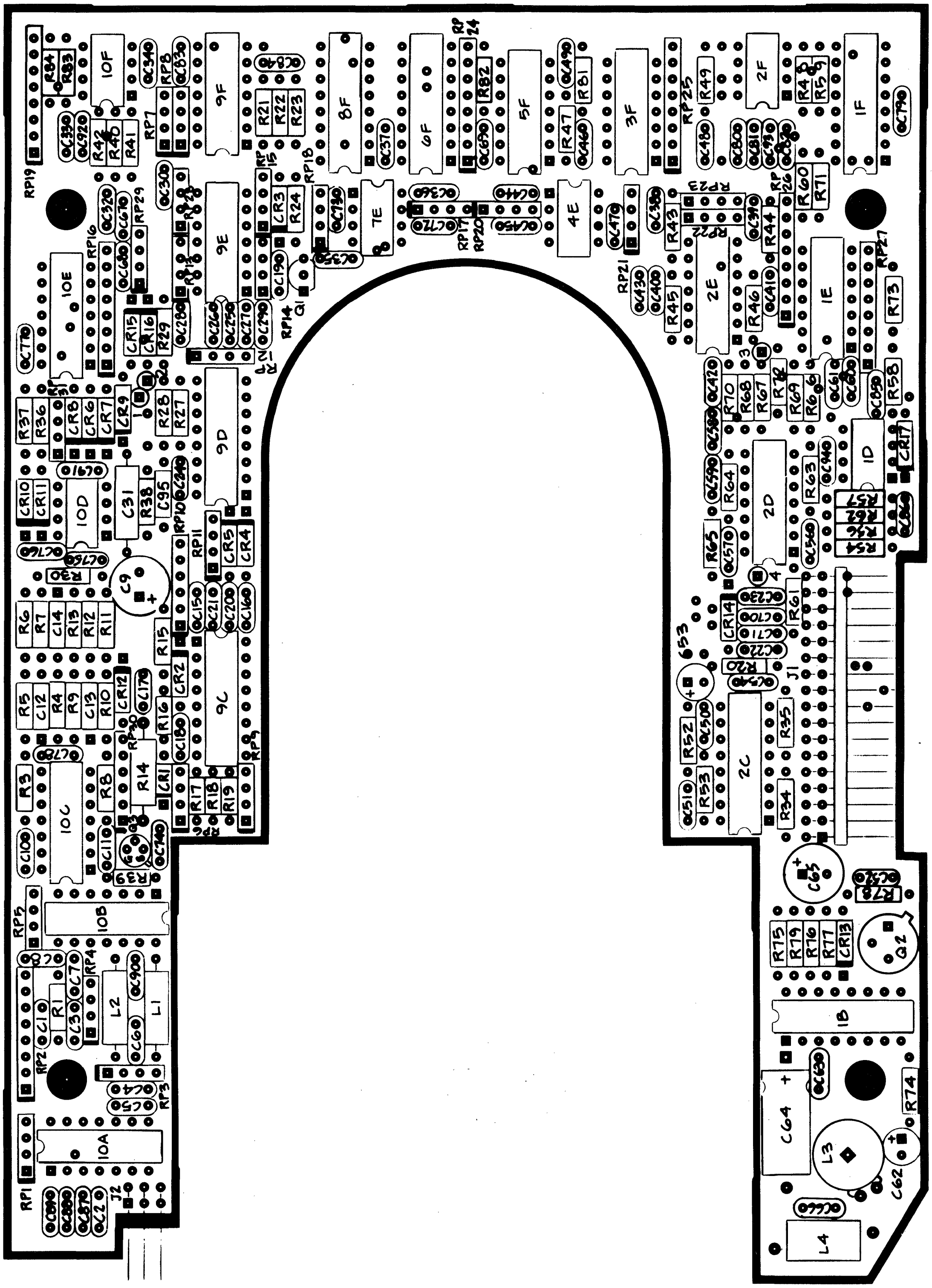
LINEAR ±.XX ±.XXX
ANGULAR±
HARDNESS
SURFACE TREATMENT
CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX
SHEET 14 OF 14
D
SCALE
PART NO. 20395-XXX



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