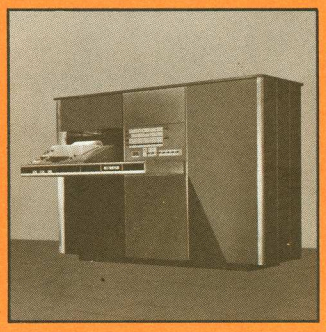
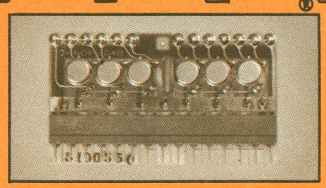
systems engineering laboratories, incorporated

BULLETIN 9056

# SEL 840
# GENERAL PURPOSE DIGITAL COMPUTER



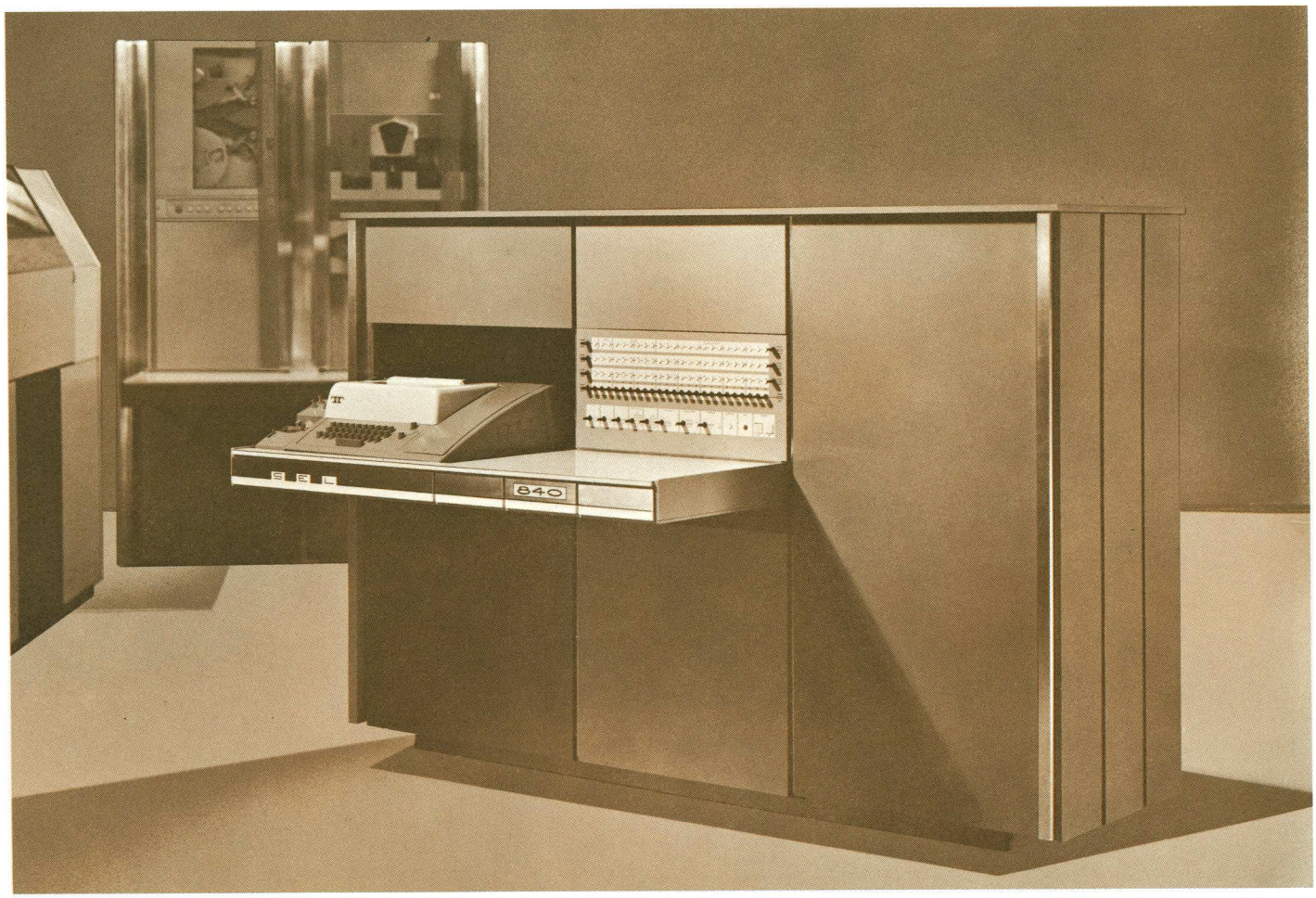
SEL®



## FEATURES

- **ALL SILICON MONOLITHIC INTEGRATED CIRCUITS**
- ONE PASS ASA FORTRAN IV INCLUDING RECURSIVE SUBROUTINE CAPABILITY
- OPTIONAL EXTENDED ARITHMETIC UNIT PROVIDES CONCURRENT FLOATING POINT ARITHMETIC
- 1.75-MICROSECONDS FULL CYCLE - FULL PARALLEL OPERATION
- UP TO 32,768 WORDS OF MEMORY DIRECTLY ADDRESSABLE

- 24-BIT BINARY WORD
- UP TO THREE HARDWARE INDEX REGISTERS
- MULTI-LEVEL INDIRECT ADDRESSING
- UP TO 60 TRUE LEVELS OF PRIORITY INTERRUPT
- UP TO EIGHT BUFFERED I/O CHANNELS WITH BLOCK TRANSFER LOGIC
- UP TO SIX DIRECT MEMORY ACCESS CHANNELS
- EXTENSIVE AND VERSATILE INSTRUCTION LIST



THE SEL 840 GENERAL PURPOSE 24-BIT PARALLEL COMPUTER HAS THE HIGHEST THROUGHPUT RATE OF ANY MACHINE IN ITS SIZE AND PRICE CLASS. IN ADDITION TO FULFILLING REQUIREMENTS FOR VERSATILE HIGH SPEED COMPUTATION, THE SEL 840 PROVIDES SYSTEM CAPABILITIES DEVELOPED THROUGH EXTENSIVE SEL EXPERIENCE IN THE DATA ACQUISITION AND CONTROL FIELDS. A COMPREHENSIVE INPUT/OUTPUT CONFIGURATION PRODUCES THE FLEXIBILITY NECESSARY FOR SEL 840 USE IN THESE APPLICATIONS:

- GENERAL PURPOSE SCIENTIFIC COMPUTATION
- HIGH SPEED DATA PROCESSING
- ON-LINE, REAL TIME DATA READOUT IN ENGINEERING UNITS
- ON-LINE DATA COMPRESSION, CORRECTION AND RECORDING
- REAL TIME CLOSED LOOP DIRECT DIGITAL CONTROL
- HIGH SPEED AUTOMATIC CHECKOUT
- DIRECT DIGITAL CONTROL FOR INDUSTRIAL PROCESSES

## SEL 840 BASIC SPECIFICATIONS

WORD SIZE

24 Bits

INTERNAL OPERATION

Fully Parallel

INTERNAL MEMORY FULL CYCLE TIME

1.75 Microseconds

CORE STORAGE

4096 Words

I/O UNIT

ASR-33 Typewriter with Tape Reader and Punch (10 Characters/Second)

TEMPERATURE ENVIRONMENT

10°C to 45°C (50°F to 113°F)

SIZE

72" Wide x 48" High x 20" Deep
(37" Deep Including Desk Top)

COMPUTATION TIMES INCLUDING ACCESS AND INDEXING:

ADD .....3.5 Microseconds
SUBTRACT .....3.5 Microseconds
MULTIPLY .....24.5 Microseconds
DIVIDE .....26.25 Microseconds

THE FOLLOWING HARDWARE AND FEATURES ARE ALSO INCLUDED WITH MAIN FRAME:

Hardware Program Counter
Double Length Accumulator
Multi-Level Indirect Addressing
Complete Software Package
Manual Program Stop and Sense Switches
Hardware Index Register
Two Independent I/O Channels
8-Bit Character Assembly Buffered I/O Channel
24-Bit Word I/O Channel
Four Independent Levels of True Priority Interrupt

## SEL 840 STANDARD OPTIONS

ADDITIONAL CORE STORAGE IN MAIN FRAME

Up to 32,768 words in modules of 4096 words each

ADDITIONAL PRIORITY INTERRUPTS

Up to 60, each individually armable

ADDITIONAL I/O CHANNELS

Up to six, each character or word buffered independent channels

EXTENDED ARITHMETIC UNIT (EAU)

An optional arithmetic and control unit that performs hardware single and double precision and floating point arithmetic independent of the main arithmetic unit, but sharing the memory.

DIRECT MEMORY CHANNELS

Up to six, each containing block transfer hardware. Maximum word rates of 570 KC. Direct memory channels may operate in same memory module as program on a cycle stealing basis or in separate modules simultaneously without program interruption.

REAL TIME CLOCK

Resolution 1 Millisecond

INTERMEDIATE SPEED MULTIPLY

Execution Time .....12.25 $\mu$ sec

INTERMEDIATE SPEED DIVIDE

Execution Time .....14.00 $\mu$ sec

## SEL 840 COMPUTER ORGANIZATION

MEMORY

Up to eight 4096-address magnetic core modules provide a maximum of 32,768 24-bit storage locations. All 32,768 locations are directly addressable.

"A" ACCUMULATOR (A)

Main Arithmetic Register

"B" ACCUMULATOR (B)

A 24-bit extension of the "A" Accumulator

TRANSFER REGISTER (T)

The register into which all words from memory are stored pending operation.

INDEX REGISTER (I)

Up to three addressable 15-bit hardware index registers.

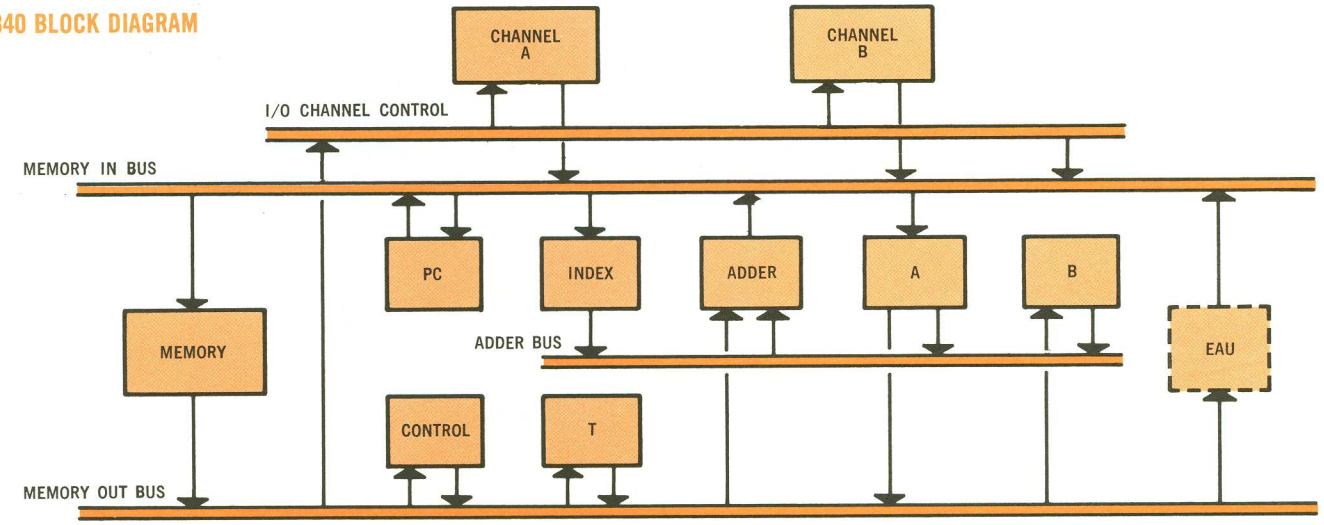
ADDER

Full 24-bit parallel adder used in all arithmetic and logical operations.

PROGRAM COUNTER (PC)

A 15-bit incremental counter that provides the current instruction address.

## SEL 840 BLOCK DIAGRAM

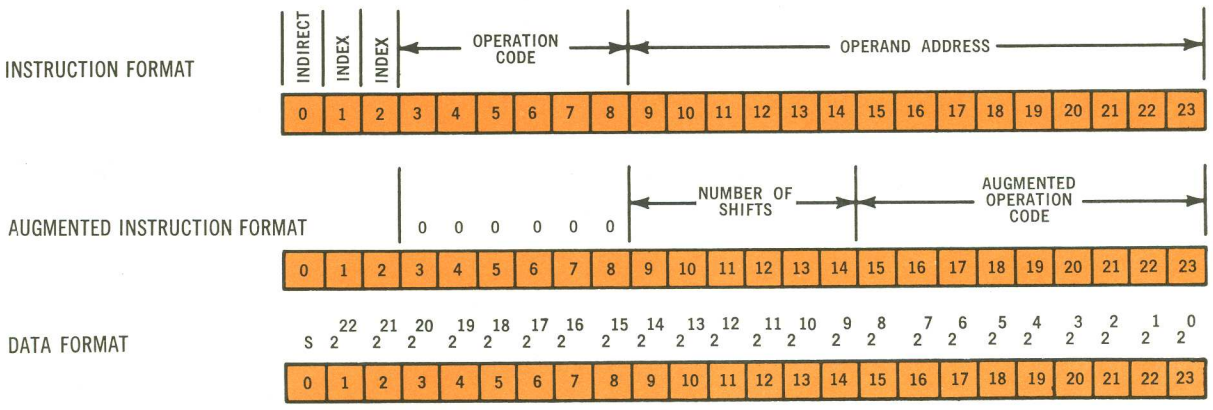



## INPUT/OUTPUT CONFIGURATION

The basic SEL 840 is equipped with two addressable I/O channels, each of which can connect 16 I/O units to the processor. For maximum versatility, one channel is used for parallel transfers of 24-bit data words and the second is used for transfer of 6 or 8 bit characters. The character format and transfer rates are controlled by the program, and the data is moved though the bus structure to memory or to the A accumulator.

Up to six additional buffered channels with or without block transfer control can be connected to the system bus structure, or up to six direct memory channels (DMC) can be added as options to allow direct communication between I/O devices and the system memory modules. A wide variety of hardware options is available with DMC units which include character formatting and block transfer logic. The I/O instruction words are constructed to facilitate the incorporation of the DMC units in the system with no alteration in the word structures. Augmented external ACT instructions allow control of 32K separate functions or controls.

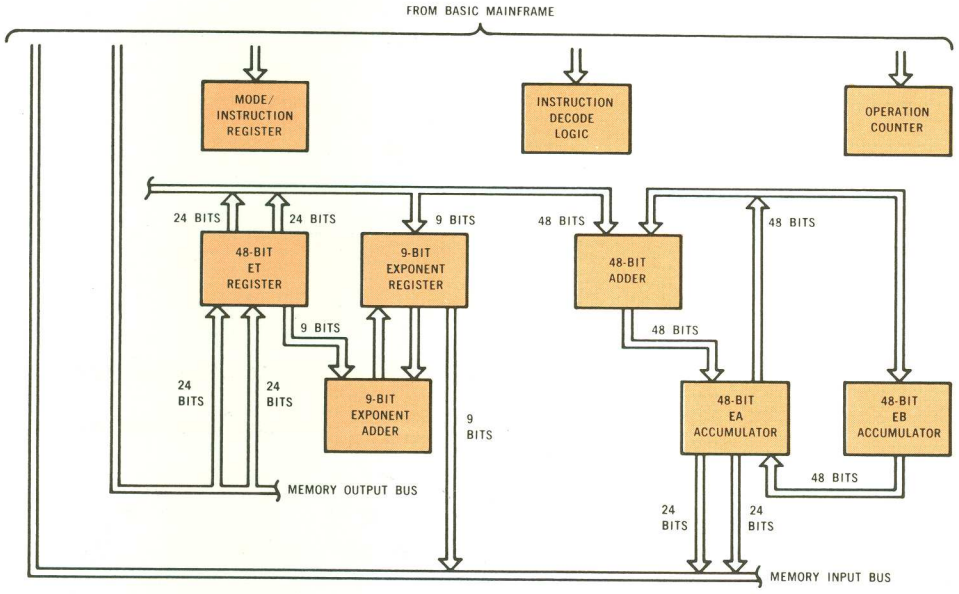
## SEL 840 WORD FORMAT



## EAU

The SEL 840 is the only computer in its size class that offers an independent, concurrent, second arithmetic unit. This optional extended arithmetic unit (EAU) is supplied with a complete set of twenty-two additional hardware commands. As an example of the concurrency available, the main frame is released to the next program instruction after the first 5.25 microseconds of the EAU double precision multiply command. The remainder of the 52.5 microsecond multiply time is performed concurrently with the main frame. The EAU can operate in single precision or double precision fixed point and in normalized or unnormalized floating point modes. The second word of double precision operands is fetched from (or stored in) core automatically.

## EAU BLOCK DIAGRAM




## EAU INSTRUCTION LIST

The following instructions are added to the basic SEL 840 repertoire when the EAU option is exercized.

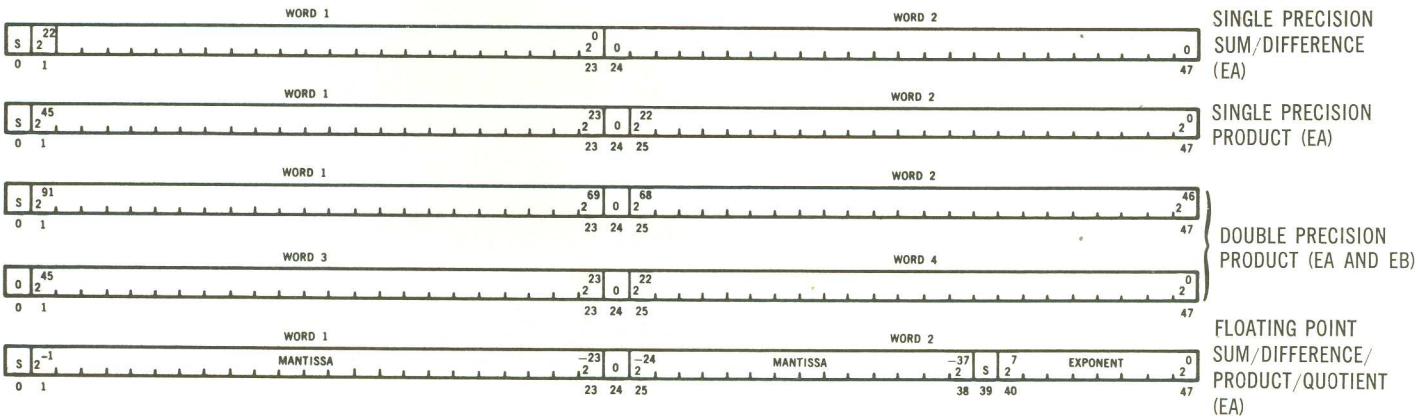
| CLASS | CODE Mnemonic | TIME (Microseconds) FP | SP | DP | FUNCTION |
|---|---|---|---|---|---|
| EXTENDED ARITHMETIC UNIT (EAU) | ESP′ | | 1.75 | | Set single precision. (SP) |
| | EDP′ | | 1.75 | | Set double precision. (DP) |
| | EFP′ | | 1.75 | | Set floating point. (FP) |
| | EFU′ | | 1.75 | | Set floating point unnormalized. |
| | EAD | $5.25+\frac{n}{2}+\frac{p}{2}$ | 3.5 | 5.25 | Add |
| | ESU | $5.25+\frac{n}{4}+\frac{p}{2}$ | 3.5 | 5.25 | Subtract |
| | EMU | $40.25+\frac{n}{2}$ | 26.25 | 52.5 | Multiply |
| | EDV | $49+\frac{n}{2}$ | 29.75 | 57 | Divide |
| | ELN | 5.25 | 3.5 | 5.25 | Load negative in A accumulator* |
| | ELO | 5.25 | 3.5 | 5.25 | Load A accumulator* |
| | EST | 5.25 | 3.5 | 5.25 | Store A accumulator* |

| CLASS | CODE Mnemonic | TIME (Microseconds) | FUNCTION |
|---|---|---|---|
| EXTENDED ARITHMETIC UNIT (EAU) | EPS′ | 1.75 | Skip A accumulator* positive. |
| | ESN′ | 1.75 | Skip A accumulator* negative. |
| | ESZ′ | 1.75 | Skip A accumulator* zero. |
| | EAR′ | 1.75 | Skip EAU ready. |
| | ENO′ | $1.75+\frac{n}{2}$ | Normalize A accumulator.* |
| | EAB′ | 1.75 | Transfer A accumulator* to B accumulator.* |
| | EBA′ | 1.75 | Transfer B accumulator′ to A accumulator.* |
| | EIA′ | 1.75 | Interchange A and B accumulators.* |
| | ELL | 3.5 | Load least significant half of A accumulator.* |
| | ESL | 3.5 | Store least significant half of A accumulator′.* |

′Augmented Instructions
*A and B accumulator in EAU are not the same as those in main frame and are both 48 bit registers.

n=No. of shifts to renormalize
p=No. of shifts to align exponents

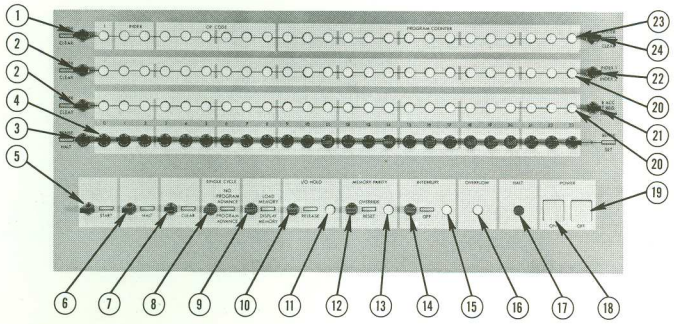
## TYPICAL EAU DATA FORMATS



## OPERATOR'S CONSOLE

The operator's console is unusually complete with immediate selectable display of any register. Provision to enter manual data into any register or core location is standard. The SEL 840 is the only machine in its size or price class with a hardware program stop available at the console. The entire console is designed for maximum operator/machine communication.

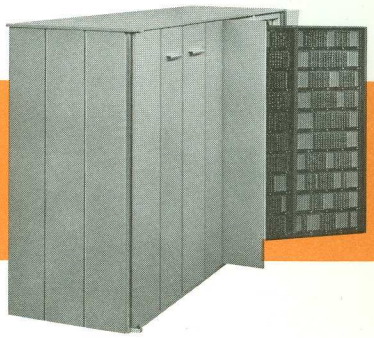
## SEL 840 CONTROL PANEL

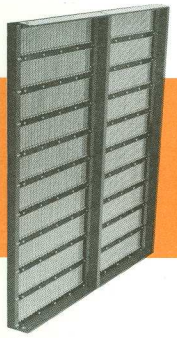


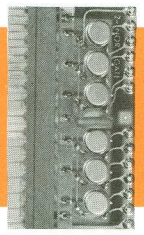

1. Raised to transfer bits 0 - 8 of the T register to the instruction register containing the operation code and address modifiers.
   Depressed to clear the instruction register.
2. Raised to transfer the contents of the T register to the selected register.
   Upper switch is depressed to clear the selected register.
   Lower switch depressed to clear T register.
3. Raised to connect switches 0 - 23 as console SENSE switches.
   Depressed to connect switches 9 - 23 as program HALT switches. (Computer halts when the program count equals selected value.)
4. Switches 0 - 23 are raised (lock) to function as SENSE or HALT switches and depressed to enter ONE bits into the T register.
5. Depressed to start computer operation.
6. Depressed to halt computer operation.
7. Depressed to clear all major registers and control latches.
8. Raised to repeat current instruction. Does not advance program counter.
   Depressed to execute single instruction in normal sequence and advances program counter.
9. Raised to enable SINGLE CYCLE switch to load contents of T register into memory.
   Depressed to enable SINGLE CYCLE switch to transfer contents of memory address to T register.
10. Depressed to release I/O wait and allow computer to resume.
11. Lights to indicate a wait for I/O function.
12. Raised to allow computer operation in the event of a memory parity error (lock).
    Centered to halt computer operation when memory parity error is detected.
    Depressed to reset the parity error latch.
13. Lights to indicate the detection of a memory parity error.
14. Depressed to inhibit operation of priority interrupts (lock).
15. Lights to indicate a priority interrupt.
16. Lights to indicate an arithmetic overflow condition.
17. Lights to indicate a program halt.
18. Pressed to apply power to computer.
    Lights when DC power is applied to computer.
19. Pressed to remove power from computer.
    Lights when AC power is connected to computer.
20. Indicators display the contents of the selected register.
21. Raised to gate the contents of the T register to the B accumulator and to display the contents of B accumulator register.
    Centered to display the contents of the T register.
    Depressed to gate the contents of the T register to Index Register 3 and to display the contents of index 3 register.
22. Raised to gate the contents of the T register and clear inputs to Index Register 1 and to display the contents of index 1 register.
    Centered to gate the contents of the T Register and clear inputs to the A accumulator and to display the contents of A accumulator register.
    Depressed to gate the contents of the T register and clear inputs to Index Register 2 and to display the contents of index 2 register.
23. Display the contents of the program counter.
24. Raised to enter bits 9 - 23 of the T register into the program counter.
    Depressed to clear the program counter.

Notes: 1. Only the SENSE, HALT and display selection switches are active while the computer is operating.
2. Switches 3 , 9 , 21 and 22 lock in all positions.

## MAINTENANCE EFFICIENCY UNSURPASSED







### SEL 840 MAIN FRAME

Sel 840 Main Frame opens in rear, and "pages" containing micrologic modules swing out exposing all computer circuitry for maintenance

### PAGE

Pages contain circuit modules. Each module has test points for troubleshooting ease. Connectors are Elco Varicon. Wire Wrap used exclusively for highest reliability and easiest field service.

### SEL MICROLOGIC MODULE

Silicon monolithic integrated digital circuits exclusively. TO-5 cans allow same serviceability as discrete component circuits, but give latest state of the art speed and reliability. Components mounted on one side only.

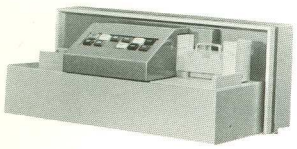
## SEL SERVICES FOR 840 USERS

- Two Week Programming and 4 Week Maintenance Courses Beginning Once Each Quarter at Fort Lauderdale.
- On Call Service Contracts.
- Field Resident Service/Operation contracts.
- Programming Services.

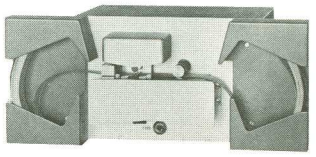
## SEL 800 SERIES PERIPHERAL EQUIPMENT

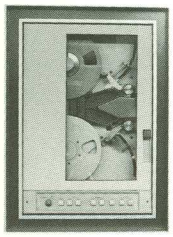
The SEL 840 computer has a wide range of available input/output equipment. Each peripheral device has its own control unit which is compatible with each computer in the SEL 800 series. The peripheral equipment utilizes the buffering capability of the computer to provide the time interface between the slower peripheral units and the computer's processor.

### SEL 840 PERIPHERAL EQUIPMENT

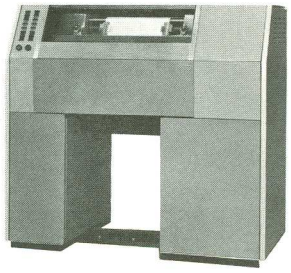


| Catalog No. | Description | |
|---|---|---|
| **80-400** | **— CARD READERS AND PUNCHES** | |
| 80-410 | — Medium Speed Reader | 100 Cards/Minute |
| 80-420 | — High Speed Reader | 200 Cards/Minute |
| 80-430 | — Medium Speed Punch | 10 Cards/Minute |
| 80-440 | — High Speed Punch | 100 Cards/Minute |
| **80-500** | **— PAPER TAPE READERS AND PUNCHES** | |
| 80-710 | — ASR-33 Reader/Punch (Supplied with Main Frame) | 10 Characters/Second |
| 80-510 | — High Speed Photoelectric Reader | 300 Characters/Second |
| 80-520 | — High Speed Punch | 110 Characters/Second |

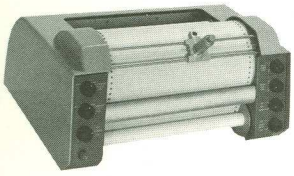




| | | |
|---|---|---|
| **80-600** | **— MAGNETIC TAPE, DRUM AND DISC SYSTEMS** | |
| 80-610-2 | — Tape Control Unit—Controls 2 ea. 80-615 units | |
| 4 | — Tape Control Unit—Controls 4 ea. 80-615 units | |
| 8 | — Tape Control Unit—Controls 8 ea. 80-615 units | |
| 80-615 | — Magnetic Tape Unit, 200, 556 and 800 bits at up to 150 ips. | |
| 80-63X | — Drum Storage | Various Access Times and Capacities |
| 80-65X | — Disc Storage | Various Access Times and Capacities |



| | | |
|---|---|---|
| **80-700** | **— TYPEWRITERS AND LINE PRINTERS** | |
| 80-710 | — ASR-33 (Supplied with Main Frame) | 10 Characters/Second |
| 80-720 | — Selectric | 15 Characters/Second |
| 80-730 | — Low Speed | 300 Lines/Minute — 120 Columns |
| 80-732 | — High Speed | 1000 Lines/Minute — 120 Columns |
| 80-734 | — High Speed | 1200 lines/min. — 20 Columns |
| 80-736 | — High Speed | 2400 lines/min. — 20 Columns |



| | | |
|---|---|---|
| **80-800** | **— PLOTTERS AND DISPLAYS** | |
| 80-810 | — Incremental Plotter | 12 in. chart width — 300 Steps/Sec. |
| 80-812 | — Incremental Plotter | 31 in. chart width — 300 Steps/Sec. |
| 80-821 | — 21" CRT Display | 2048 Characters |
| 80-806 | — 6" CRT. Display | 512 Characters |
| 80-805 | — High Resolution 5" CRT Display | 4096 Characters |
| 80-820 | — Vector Generator | Used with 80-821 or 80-806 or 80-805 |
| 80-822 | — Character Generator | Used with 80-821 or 80-806 or 80-805 |
| 80-824 | — Refresh Memory | Used with 80-821 or 80-806 or 80-805 |
| 80-830 | — Light Pen for CRT Displays | |
| **80-900** | **— SPECIAL INTERFACES** | |
| 80-910 | — SEL 600 Data Acquisition Systems | |
| 80-920 | — Direct Digital Control Outputs | |
| 80-930 | — Custom Interfaces | |

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