Gould Buffered Tape Processor

Model 8051

Technical Manual

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CHAPTER 1

GENERAL DESCRIPTION

1.1 Introduction

This manual contains reference information concerning the installation, operation, and maintenance of the Buffered Tape Processor (BTP) Model 8051. The BTP is manufactured by Gould Inc., Computer Systems Division, Fort Lauderdale, Florida.

The information in this manual is presented in the following order:

Chapter 1	General Description
Chapter 2	Operation
Chapter 3	Programming
Chapter 4	Theory of Operation

The assemblies, circuit cards, logic drawings, and schematics are contained in the Buffered Tape Processor Drawings Manual (304-003170).

Note

The acronym BTP, as used throughout this manual, is synonymous with the Buffered Tape Processor, Model 8051, unless otherwise noted.

1.2 Physical Description

The buffered tape processor system consists of the following components: a BTP and a formatted magnetic tape transport.

1.2.1 Buffered Tape Processor

The buffered tape processor (BTP) is contained on a single 15 inch wide by 18 inch deep plug in circuit board (see Figure 1-1). A row of connector pins, which runs the full width of the board, provides the electrical interface to the SelBUS and to the tape formatter. These pins are segmented into three groups: 184 pins, in the middle, for the SelBUS and two groups of 50 pins, on each side, for the external device connections. Three smaller sets of connector pins, on the opposite end of the board, are provided for test purposes.

A toggle switch on the BTP, which is accessible to operations and maintenance personnel, provides a means for logically disconnecting the BTP from the SelBUS without removing the board from the chassis. An LED is located next to the toggle switch to indicate microdiagnostic status. Three sets of jumpers set the BTP SelBUS priority and address.

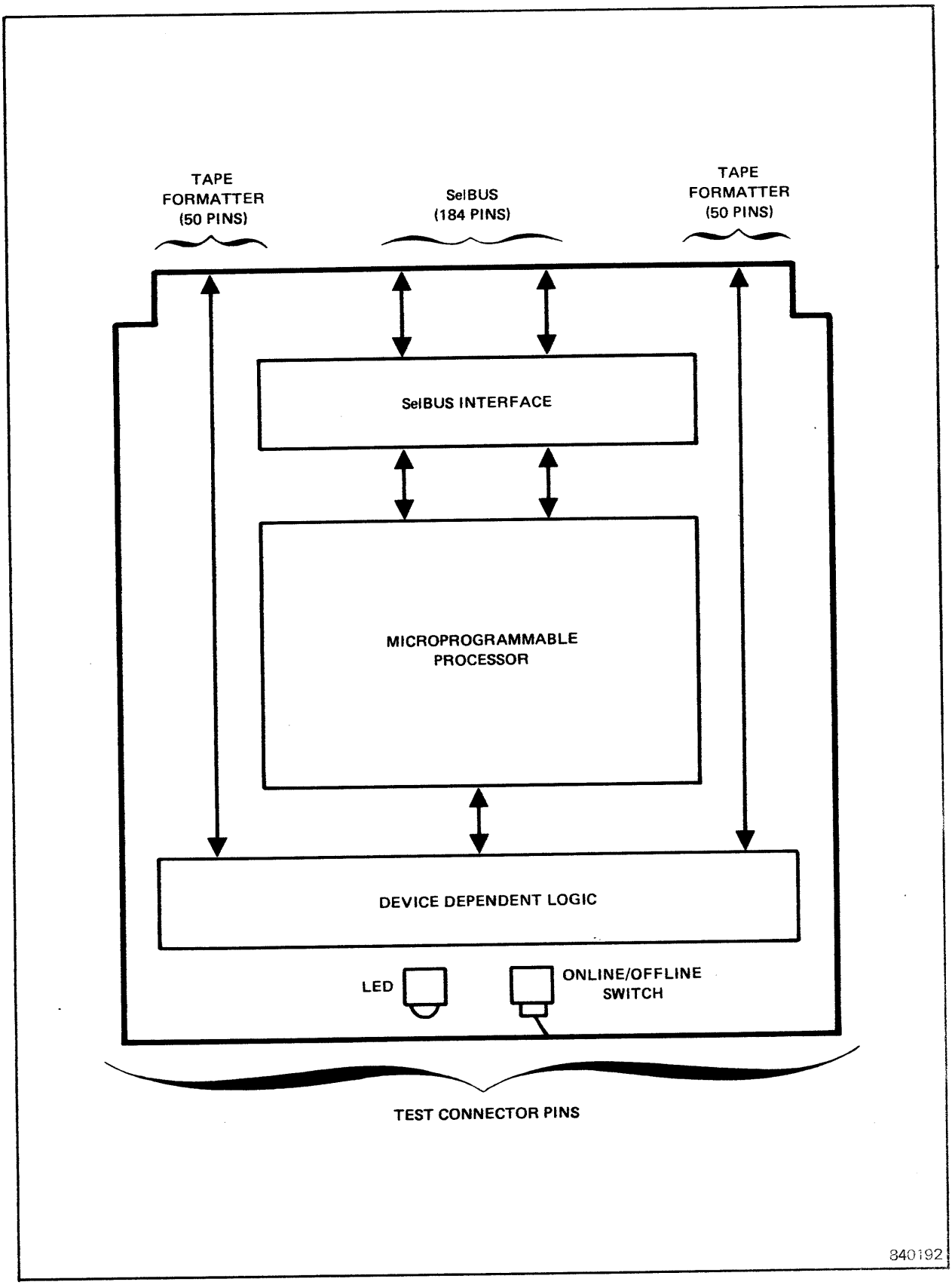


Figure 1-1. Buffered Tape Processor Card Layout

1.2.2 Formatted Tape Transport

The BTP supports the standard Pertec imbedded formatter interface used by most tape drive manufacturers. However, this does not imply that all tape units implementing this interface will operate correctly with the BTP. Currently, only those tape units specified by Gould CSD are supported.

1.2.3 Interconnection

The BTP connects to the formatted tape unit through two 50 pin flat ribbon cables. At the external device the cables are terminated using 50 pin slotted edge connectors. At the BTP the cables are connected to a universal IOX card which primarily provides support to the cables and eliminates possible backplane damage caused by direct cable connection to pin side of the SelBUS. The maximum allowable distance between the BTP and the formatted tape unit is thirty feet.

1.3 Functional Description

The BTP is a programmed I/O channel controller. It requires a minimum of one formatted tape transport. However, it can support a maximum of eight drives.

The buffered tape system functions as a single programmed channel capable of controlling one tape drive at any given time. Parallel operations are restricted to parallel tape rewind operations. Functionally, the formatter combination is considered to be an integrated channel controller that operates with selector channel characteristics. The magnetic tape units are called devices. The BTP formatter combination is called the buffered tape processor system.

The buffered tape processor system is designed to accommodate tape transports that operate at speeds of up to 125 inches per second, with a recording density of 1600 bits per inch (BPI) at data rates of up to 200,000 characters per second.

The channel-drive combination is fully compatible with IBM nine-track tapes. The nine-track compatibility includes both NRZI and PE recording modes at 800 and 1600 BPI, respectively.

The command set is sufficiently rich to permit the full utilization of the programmed I/O concept. When tapes contain both file and record labels, it is possible to initiate lengthy tape searches with a single-start I/O instruction. These searches are subsequently conducted without CPU support or intervention. When the search is complete the required data transfer is executed, the I/O program is terminated, and only then is the CPU interrupted. The termination of data flow causes the BTP to generate an interrupt, which the CPU recognizes. The CPU then initiates a query to the BTP, resulting in a status transfer to the CPU, which indicates either a successful data transfer or any errors that were encountered.

The BTP is the basic hardware structure for the BTP system and consists of four functional parts (refer to Figure 1-2):

1. A SelBUS interface, which provides the communications path between the BTP and the CPU or the BTP and memory.

2. A microprocessor, which has a control memory that contains the microprogram (firmware) for controlling the SelBUS interface, microprocessor, cache control, and interface logic. Together, the SelBUS interface and the microprocessor comprise the IOM (input/output BTP microprogrammable processor).

3. The cache control logic which consists of 64K byte of dynamic RAM and its timing circuits, read/write address circuits, parity check/generate on the RAM paths, and multiplexed data paths to the microprocessor.

4. Device interface logic which contains the drivers and receivers to communicate to the formatter in the tape transport, status registers and strobe synchronization logic, and parity check/generate logic on the tape data paths.

Although the microprogram for the BTP installs in the control memory of the microprocessor, it is considered part of the device-dependent interface since it provides the control for the device.

The SelBUS interface provides logic circuits, staging registers, and drivers to allow the microprogrammable processor (MP) to communicate with the CPU and memory over the SelBUS. Jumpers, which may be altered to establish individual system requirements, determine the SelBUS priority level and the IOM address.

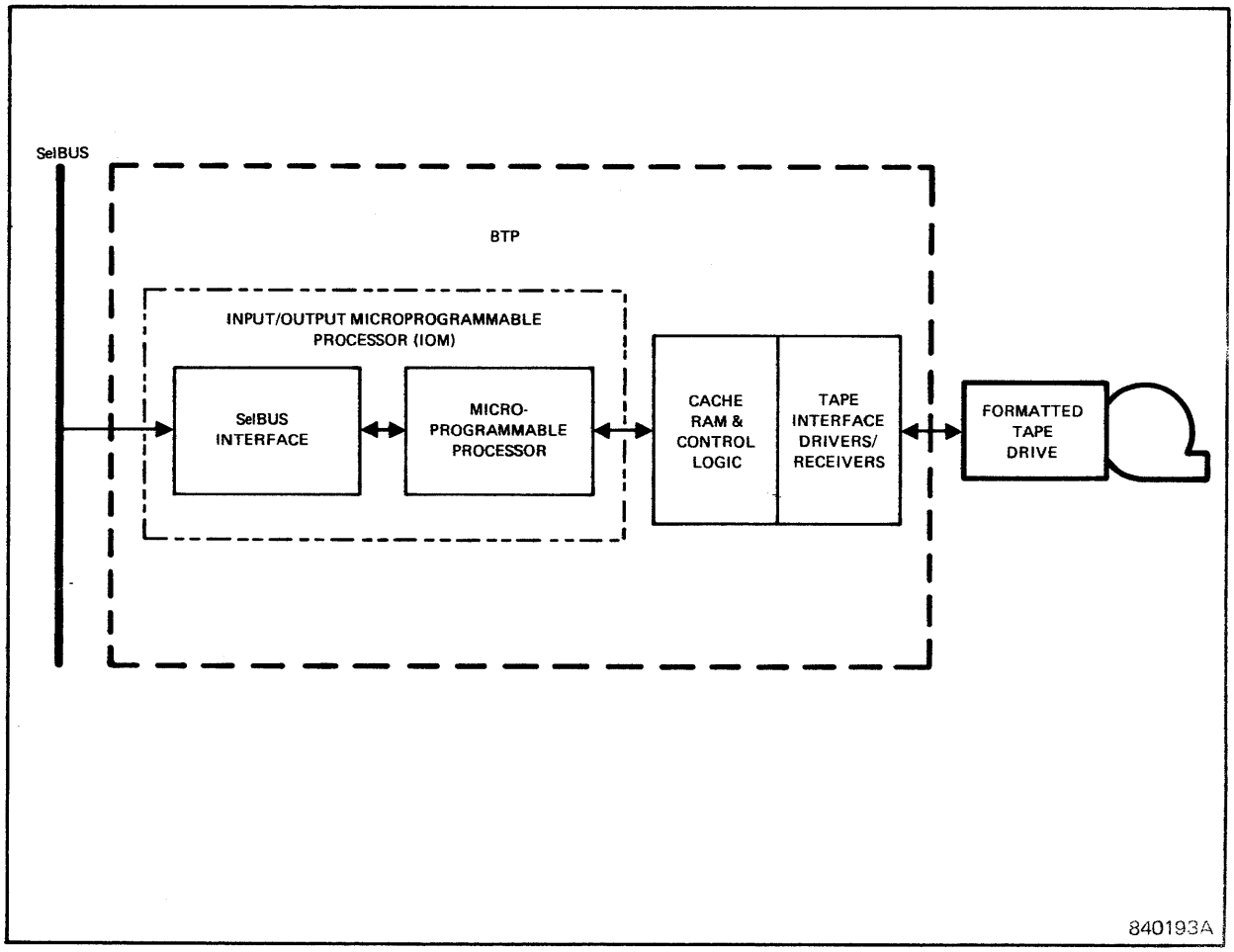


Figure 1-2. Functional Block Diagram - Buffered Tape Processor System

The MP in the BTP is a CPU and performs logical, control, and arithmetic functions. The MP contains a read-only memory (ROM) control unit, an arithmetic logic unit (ALU), two 16-bit by 16-word register files, and order structure logic used in the generation of external control signals.

The device-dependent logic consists of registers, latches, buffers, drivers, and receivers that interconnect the BTP to the formatted tape drive. The device-dependent logic performs the following functions:

1. Transmits and receives an eight-bit data byte to or from the active tape drive via the formatter. The data byte is the information read from the tape or to be written onto the tape.

2. Accepts and stores device status signals indicating the status of the active tape drive unit.

3. Sends pulse and level order commands via the formatter to cause the tape drive to perform the desired operation.

4. Controls data transfers between the tape interface and the cache memory.

1.4 System Configurations

Figure 1-3 is a block diagram that illustrates the BTP system organization. The formatter provides for the attachment of from one to four tape transports. The buffered tape processor system specifications are provided in Table 1-1.

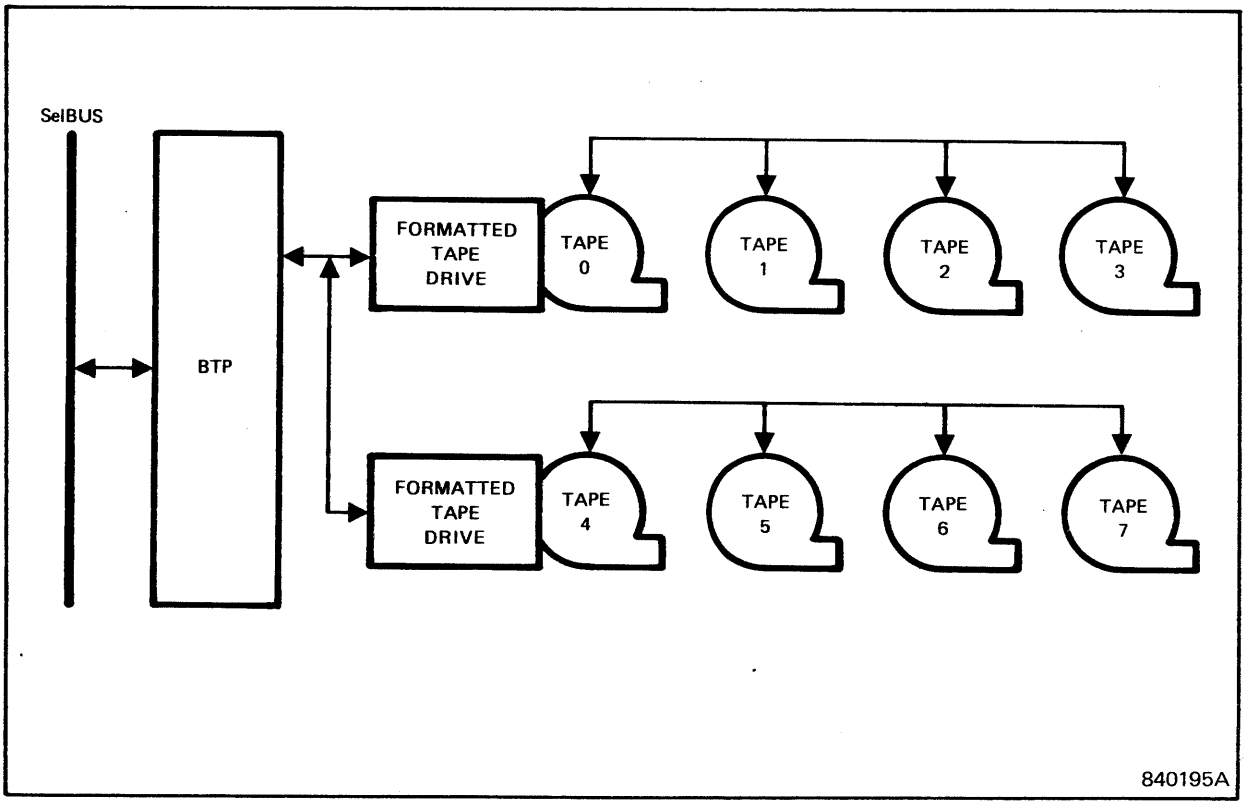


Figure 1-3. Buffered Tape Processor System Configuration

Table 1-1
Buffered Tape Processor System Specifications

Characteristics	Specifications
Buffered Tape Processor	
Device Transfer rate	36K bytes to 200K bytes/sec
Processor Transfer rate	up to 2M bytes/sec
Recording densities	800 or 1600 bpi
Dimensions	15 in. x 18 in.
Weight	3 lb
SelBUS slot requirements	1 slot
SelBUS electrical load	1 board
Power	Provided by CPU
Temperature/humidity	Same as CPU
Max cable length to formatted unit	30 ft
Formatted Tape Unit	
Data format	NRZI or PE
Number of tracks	9
Recording densities	800/1600 bpi
Gap size	0.6 in.
Parity generation	Controller implemented
Tape speeds	up to 125 ips

CHAPTER 2

OPERATION

2.1 Introduction

This section of the manual contains the operating and programming instructions for the buffered tape processor (BTP).

2.2 Controls and Indicators

Refer to Figure 2-1 for graphic representation of controls and indicators on the BTP.

2.2.1 Controls

2.2.1.1 Offline Switch

The BTP circuit card is provided with an offline switch located on the front edge of the circuit card. This switch must be placed in the online position for the BTP to communicate with the SelBUS and CPU. The online position is the right-hand position of the switch when the circuit card is installed correctly in the logic chassis.

2.2.1.2 Physical Address Selection

The IOM portion of the BTP circuit card has a set of jumpers that selects the physical address (SelBUS address) of the IOM. The address selected by these jumpers must correspond to the IOM physical address associated with the IOM I/O instruction address during the CPU initial program load of the initial configuration list. The physical address jumpers are shown on Logic Drawing 130-103640 (Sheet 8), in the drawings manual. The physical address jumpers are referenced by a logic call out of E12-1 and 16 through E12-7 and 10. Jumpers must be installed to reflect the low true physical address of the IOM. Jumper E12-1 and 16 selects the most significant address bit, and jumper E12-7 and 10 selects the least significant address bit. Jumper E12-8 and 9 is not used.

2.2.1.3 SelBUS Priority Recognition Selection

The IOM portion of the BTP circuit card has a set of 21 priority recognition jumpers. These jumpers are used to assign priorities to all system modules that have a SelBUS transfer priority higher than this BTP.

The priority recognition jumpers are shown on Logic Drawing 130-103640 (Sheet 18) and are referenced by call outs D22, D23, and D24. To assign higher priority transfer devices, the jumper corresponding to the specific higher priority levels must be placed in the closed (on) position, and the jumpers corresponding to the priority level assigned to this magnetic tape controller IOM and all lower priority levels must be placed in the open (off) position.

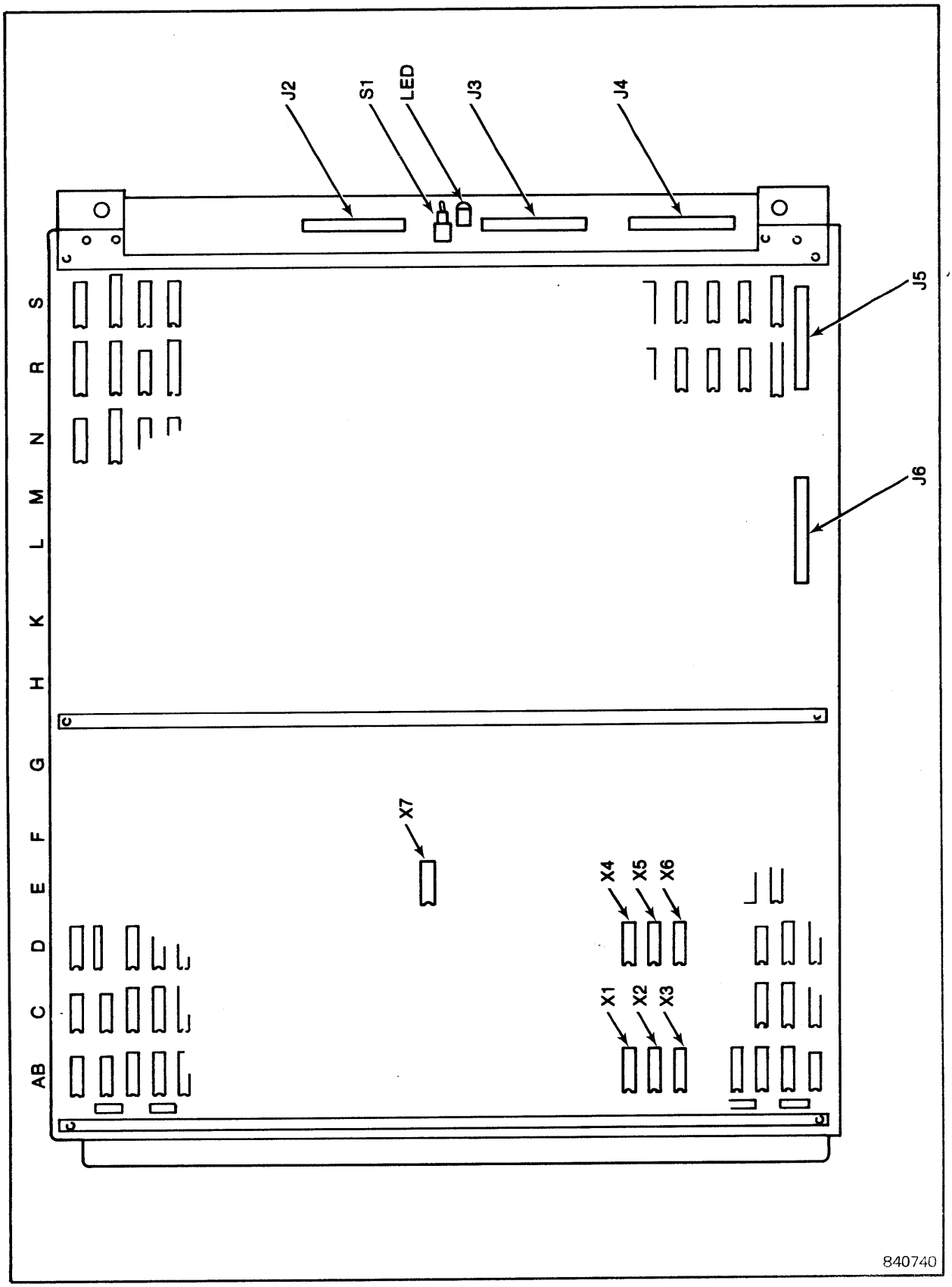


Figure 2-1. Buffered Tape Processor Controls and Indicators

2.2.1.4 SelBUS Priority Generation Selection

The IOM portion of the BTP circuit card has 22 priority generation jumper connections used to assign the bus transfer priority level to the BTP. The priority generation jumpers are shown on Logic Drawing 130-103640 (Sheet 18) and are referenced by call outs A22, A23, and A24. To assign a SelBUS priority level to the BTP, the jumpers controlling the priority level must be placed in the closed (on) positon and all remaining jumpers must be placed in the open (off) position. The priority level chosen by this procedure must correspond to the priority level used for this IOM in the priority recognition jumpers.

2.2.1.5 SelBUS Priority Enable Selection

The CPU logic chassis backplane has a SelBUS terminator circuit card that contains a set of 22 priority enable jumpers. These jumpers must be set so that jumpers connected to priority levels assigned to modules on the SelBUS are placed in the open (off) position, and jumpers connected to unassigned priorities are in the closed (on) position.

2.2.1.6 Tape Transport Address Selection

The subaddress sent to the BTP channel, during CPU transactions, is used to select one of the attached tape transports. The tape address is selectable by setting either jumper or switches located on the imbedded formatter. The attached transports usually have a rotary switch accessible at the transport operator panel. Refer to the tape transport technical manual for specific details.

2.2.2 Indicators

The BTP is provided with a red LED to indicate the general state of the channel. Three states are defined as follows:

1. Idle State - the LED flashes at half second intervals indicating successful and continuing execution of the internal microdiagnostics.

2. Error State - the LED remains on during microdiagnostic failures. It may also remain on if the system clocks have failed or the system reset failed.

3. Active State - the LED remains off when the BTP is currently communicating with the CPU or the tape interface.

The LED is mounted at a right angle to the circuit card and faces the open end of the logic chassis. It is located next to, but not controlled by the offline switch.

2.3 Power On/Off Procedures

DC power is supplied to the BTP circuit card by the logic chassis in which the BTP circuit card is installed. The power on/off procedures for the logic chassis are normally covered by the CPU power on/off procedures, which are described in the appropriate CPU technical manual.

2.4 Operating Procedures

There are no special operating procedures for the BTP; however, the technical manuals for the devices attached to the BTP should be consulted before the BTP is operated.

CHAPTER 3

PROGRAMMING

3.1 Introduction

This section contains macroprogramming instructions for the buffered tape processor (BTP). It also provides a brief description of the software instructions used to control and obtain status from the BTP. A more complete description of software I/O instructions is provided in the CPU reference manual.

Input/output operations are initiated and controlled by information with two types of formats: instructions and commands. Instructions are decoded by the CPU and are part of the CPU program. Commands are decoded and executed by the channel and the device.

Both instructions and commands are created by the software programmer, assembled, and loaded into memory. During execution, CPU firmware translates the macroinstructions and commands written by the programmer into a series of SelBUS transfers between the CPU, memory, and the channel. An example of a typical sequence for a start I/O instruction is shown in Figure 3-1.

3.2 I/O Instructions and Commands

3.2.1 Extended I/O Instructions

The BTP is controlled by the extended I/O set of software instructions. Figure 3-2 provides the basic format for these instructions and lists the suboperation codes of the instruction. The 9 codes shown (SIO, TIO, DCI, RSCHNL, HIO, STPIO, ECI, ACI, and DACI) are the only codes supported by the BTP firmware. Any other codes will generate an error response from the BTP.

For all extended I/O instructions, the constant in bits 16 through 31 of the instruction plus the contents of the general register indicated by bits 6 through 8 of the instruction (if bits 6 through 8 are nonzero) specify the logical channel and subaddress. The channel will ignore the subaddress for operations that pertain only to the channel. The extended I/O instructions can be executed only when the CPU is in privileged mode and is operating with a mode setting of program status doubleword (PSD).

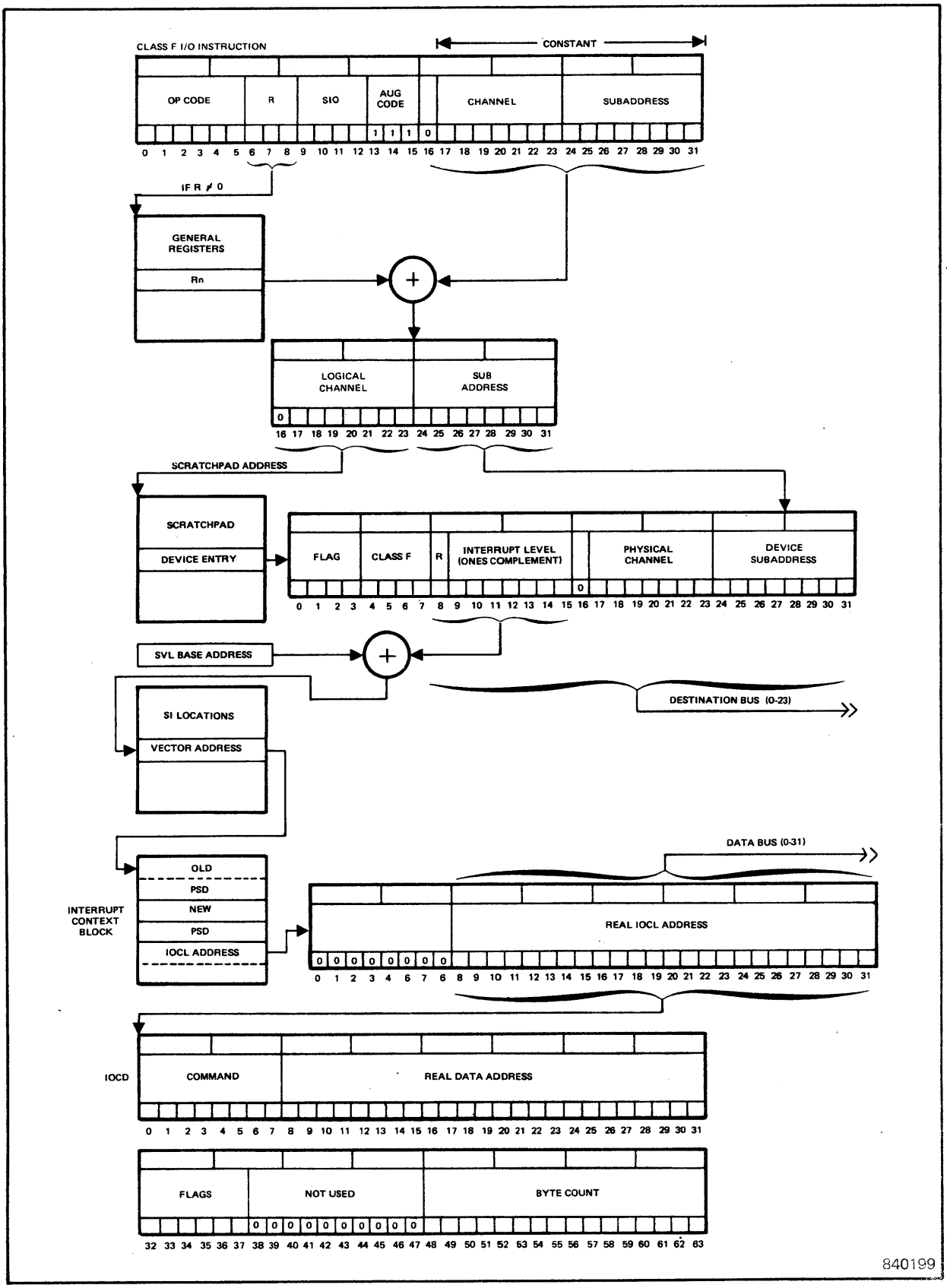
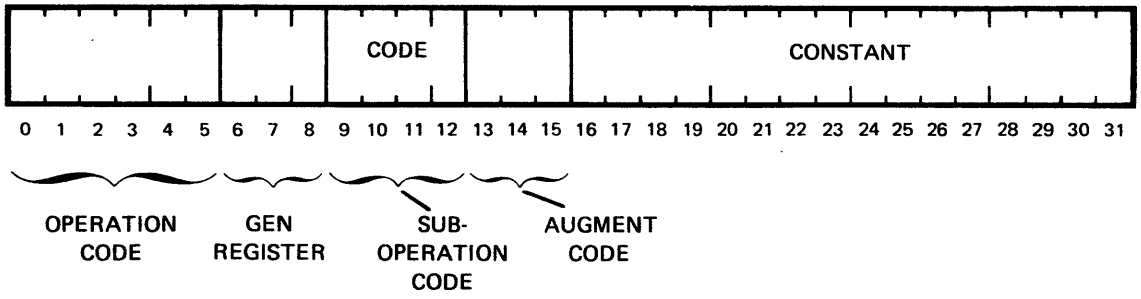


Figure 3-1. Instruction Execution Sequence, Start I/O



BITS	DEFINITION
0-5	SPECIFIES THE OPERATIONS CODE (111111)
6-8	WHEN NONZERO, THIS FIELD SPECIFIES THE GENERAL REGISTER WHOSE CONTENTS WILL BE ADDED TO THE CONSTANT FIELD (BITS 16-31) TO FORM THE LOGICAL CHANNEL AND SUBADDRESS.
9-12	SPECIFIES THE SUBOPERATION CODE:

0010	X'2'	START I/O	(SIO)
0011	X'3'	TEST I/O	(TIO)
0100	X'4'	STOP I/O	(STPIO)
0101	X'5'	STOP I/O	(RSCHNL)
0110	X'6'	HALT I/O	(HIO)
0111	X'7'	GRAB CONTROLLER	(GRIO)*
1000	X'8'	RESET CONTROLLER	(RSCTL)*
1001	X'9'	ENABLE WRITE CHANNEL WCS	(ECWCS)*
1011	X'B'	WRITE CHANNEL WCS	(WCWCS)*
1100	X'C'	ENABLE CHANNEL INTERRUPT	(ECI)
1101	X'D'	DISABLE CHANNEL INTERRUPT	(DCI)
1110	X'E'	ACTIVATE CHANNEL INTERRUPT	(ACI)
1111	X'F'	DEACTIVATE CHANNEL INTERRUPT	(DACI)

13-15	AUGMENT CODE (111)
16-31	CONSTANT FIELD RELATED TO ADDRESS

*NOT SUPPORTED BY THE BTP.

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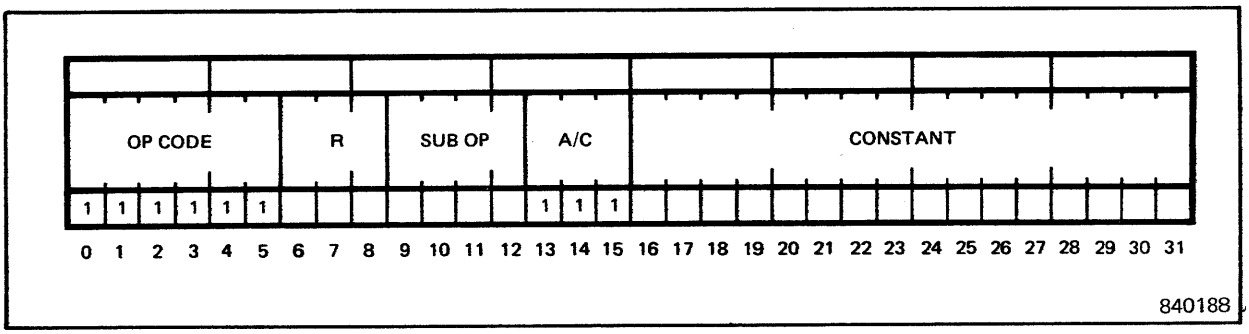
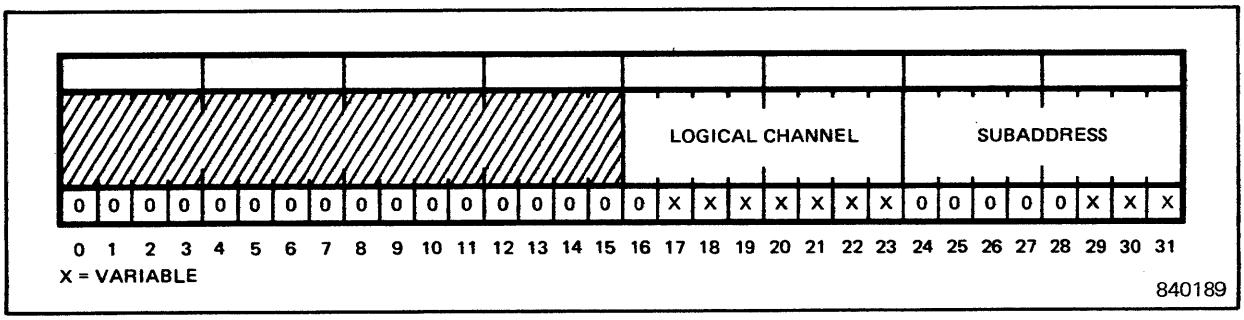
Figure 3-2. Extended I/O Instruction Format

All BTP instructions are in the following format:



The operation code (bits 0 through 5) and the augment code (A/C) (bits 13 through 15) must contain ones. The R field (6 through 8), if nonzero, specifies the general register whose contents are added to the constant field (bits 16 through 31) to form the logical channel and subaddress. If R is specified as zero, only the constant field is used. The format of the constant field is shown below:



The sub op field (bits 9 through 12) specifies the type of operation that is to be performed.

The BTP instructions must be executed by the CPU, operating in the privileged PSD mode. This operating condition is obtainable by executing a mode set instruction.

Bits 9 through 12	Sub Op
0 0 0 0 - X'0'	Unassigned
0 0 0 1 - X'1'	Unassigned
0 0 1 0 - X'2'	Start I/O (SIO)
0 0 1 1 - X'3'	Test I/O (TIO)
0 1 0 0 - X'4'	Stop I/O (STPIO)
0 1 0 1 - X'5'	Reset channel (RSCHNL)
0 1 1 0 - X'6'	Halt I/O (HIO)
0 1 1 1 - X'7'	Not supported
1 0 0 0 - X'8'	Not supported
1 0 0 1 - X'9'	Not supported
1 0 1 0 - X'A'	Unassigned
1 0 1 1 - X'B'	Not supported
1 1 0 0 - X'C'	Enable channel interrupt (ECI)
1 1 0 1 - X'D'	Disable channel interrupt (DCI)
1 1 1 0 - X'E'	Activate channel interrupt (ACI)
1 1 1 1 - X'F'	Deactivate channel interrupt (DACI)

If execution is requested in any mode other than the ones previously mentioned, the following actions will occur:

1. If the nonprivileged mode was chosen, a privileged violation trap occurs.
2. If the program status word (PSW) mode was chosen, an undefined instruction trap occurs.

The condition codes (CC) are set for the execution of all BTP instructions. The codes indicate the successful or unsuccessful initiation of an I/O instruction. The condition codes can be set by the CPU, for channel busy and inoperable or undefined channel, or by the information passed directly from the channel. The assignments for the condition codes are as follows:

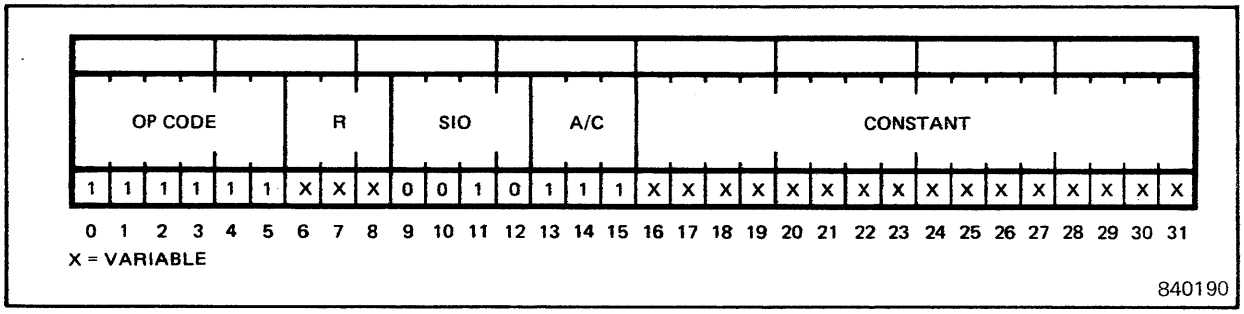
CC1	CC2	CC3	CC4	
0	0	0	0	Request not activated (echo status), unused
0	0	0	1	Channel busy
0	0	1	0	Channel inoperable or undefined
0	0	1	1	Subchannel busy
0	1	0	0	Status stored
0	1	0	1	Unsupported transaction
0	1	1	0	Unassigned
0	1	1	1	Unassigned
1	0	0	0	Request accepted and queued, no echo status
1	0	0	1	Unassigned
1	0	1	0	Unassigned
1	0	1	1	Unassigned
1	1	0	0	Unassigned
1	1	0	1	Unassigned
1	1	1	0	Unassigned
1	1	1	1	Unassigned

Although 16 encoded conditions are possible, only the assigned patterns occur.

3.2.1.1 Start I/O (SIO)

The SIO instruction starts the execution of an IOCL. When issued to the BTP, it will return one of the following four condition codes:

Condition Code	Function
1	The channel busy condition code is returned if another SIO is still in execution.
4	The status stored condition code indicates status has been stored (status pending), but no acknowledgement has been received. The memory address where the status has been stored is also returned. This condition code clears the status pending condition.
5	The unsupported transaction condition code is returned if the SIO is issued to an invalid subaddress. Note: 0 through 3 are the only valid subaddresses.
8	The request accepted and queued, no echo status condition code is sent when all preliminary checks indicate the operation will be performed satisfactorily. Having sent this condition code, software can always expect at least one interrupt and the accompanying termination status, which will indicate the success or failure of the SIO execution. Note that if an SIO is issued to a channel that has not been INCHed, the SIO will not be executed, an interrupt will not be generated, and status will not be posted, even though a condition code of eight has been sent.



Bits 0 through 5 (FC hexadecimal) specify the operation.

Bits 6 through 8, when nonzero, specify the general register. The register contents are added to the constant to form the logical channel and subaddress.

Bits 9 through 12 (2 hexadecimal) specify an SIO operation.

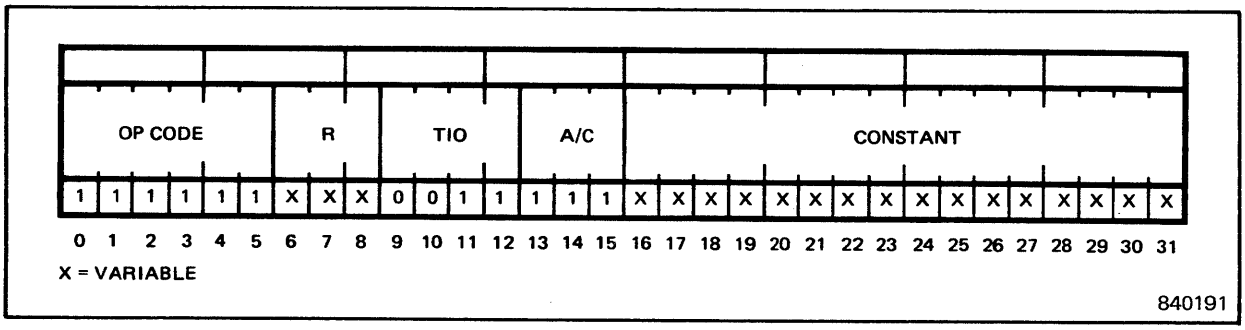
Bits 13 through 15 (7 hexadecimal) specify the augment code.

Bits 16 through 31 specify a constant that is added to the contents of R to form the logical channel and subaddress. If R is zero, only the constant is used to specify the logical channel and subaddress.

3.2.1.2 Test I/O (TIO)

The TIO instruction probes the channel/controller and returns one of the following five condition codes:

Condition Code	Function
1	The channel busy condition code indicates that the channel is busy executing an SIO.
3	The subchannel busy condition code indicates that the subchannel is rewinding.
4	The status stored condition code indicates status has been stored (status pending), but has not yet been acknowledged by software. The memory address where the status has been stored is also returned. This condition code clears the status pending condition.
5	The unsupported transaction condition code indicates an invalid subaddress.
8	The request accepted and queued, no echo status condition code indicates that the BTP can accept an SIO.



Bits 0 through 5 (FC hexadecimal), when zero, specify the general register. The register contents are added to the constant to form the logical channel and subaddress.

Bits 6 through 8, when nonzero, specify the general register. The register contents are added to the constant to form the logical channel and subaddress.

Bits 9 through 12 (3 hexadecimal) specify a TIO operation.

Bits 13 through 15 (7 hexadecimal) specify the augment code.

Bits 16 through 31 specify the constant that is added to the contents of R to form the logical channel and subaddress. If R is zero, only the constant is used to specify the logical channel and subaddress.

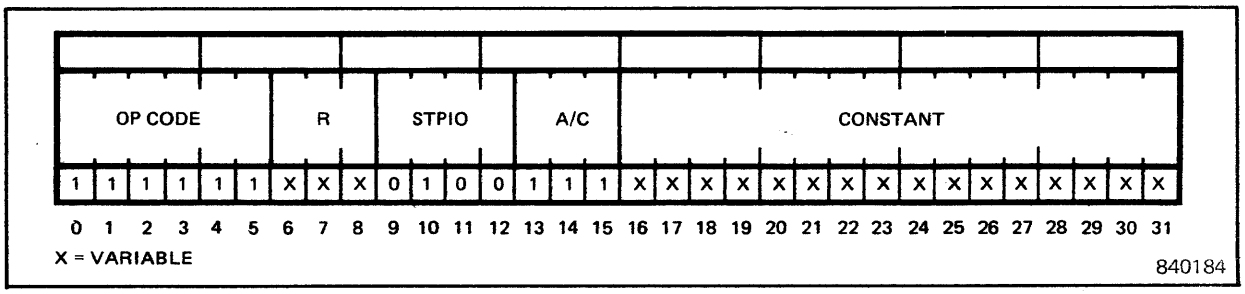
3.2.1.3 Stop I/O (STPIO)

The STPIO instruction terminates the current I/O operation after the completion of the current IOCD. The STPIO instruction applies only to the addressed subchannel. Its only function is to suppress command and data chain flags in the current IOCD.

If a stop I/O is issued to an active channel but the active subchannel and the stop I/O subchannel do not match, a channel busy condition code is returned and the original command is completed. If the channel is not active, the stop I/O and halt I/O look identical; that is, if the subchannel is not rewinding, an accepted condition code is returned, a status of channel end/device end (CE/DE) is stored, and an interrupt is requested. If the subchannel is rewinding, CE is stored and DE is sent out when the rewind is complete.

The stop I/O will return one of the following four condition codes:

Condition Code	Function
1	The channel busy condition code indicates that the channel is busy and that the active subchannel and the subchannel to which the STPIO was issued do not match. After the condition code is issued, the firmware returns to complete the task that caused the channel to be active.
4	The status stored condition code indicates status has been stored (status pending) but has not yet been acknowledged by software. The memory address where the status has been stored is also returned. This condition code clears the status pending condition.
5	The unsupported transaction condition code indicates an invalid subaddress.
8	The request accepted and queued condition code indicates that a stop I/O was accepted.



Bits 0 through 5 (FC hexadecimal) specify the operation code.

Bits 6 through 8, when nonzero, specify the general register. The register contents are added to the constant to form the logical channel and subaddress.

Bits 9 through 12 (4 hexadecimal) specify an STPIO operation.

Bits 13 through 15 (7 hexadecimal) specify the augment code.

Bits 16 through 31 specify a constant that is added to the contents of R to form the logical channel and subaddress. If R is zero, only the constant is used to specify the logical channel and subaddress.

3.2.1.4 Halt I/O (HIO)

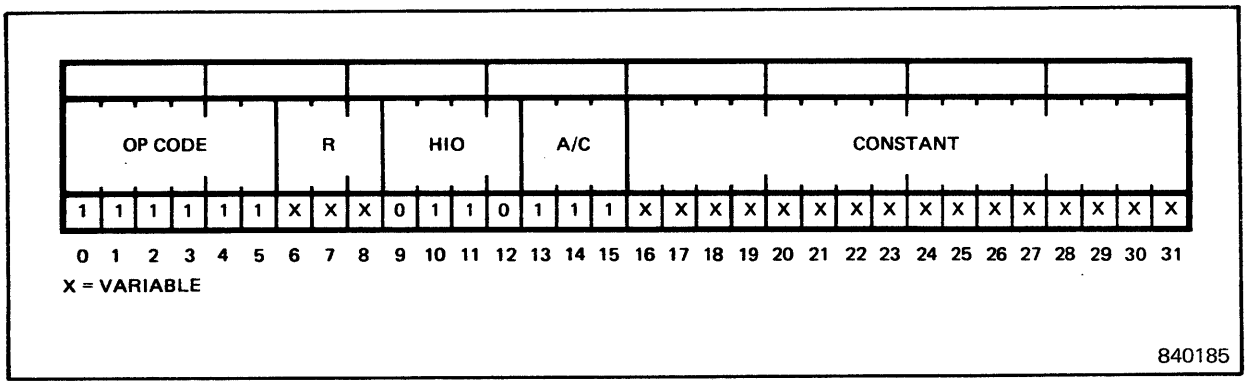
The halt I/O instruction performs an immediate but orderly halt if the subchannel to which the halt I/O is issued is active. However, if the channel is active and the active subchannel and the halt I/O addressed subchannel do not match, a channel busy condition code is returned. If the channel is not active, then the instruction is accepted and a channel end/device end (CE/DE) status is posted. If the subchannel is rewinding, a channel end is issued, followed by a device end when the rewind is complete.

The halt I/O will return one of the following three condition codes:

Condition Code	Function
1	The channel busy condition code indicates that the channel is busy and that the active subchannel and the subchannel to which the HIO was issued do not match. After the condition code is issued, the firmware returns to complete the task that caused the channel to be active.
5	The unsupported transaction condition code indicates an invalid subaddress.
8	The request accepted and queued condition code indicates that a halt I/O was accepted.

Note

Condition code 4 (status stored) will not be returned.



Bits 0 through 5 (FC hexadecimal) specify the operation code.

Bits 6 through 8, when nonzero, specify the general register. The register contents are added to the constant to form the logical channel and subaddress.

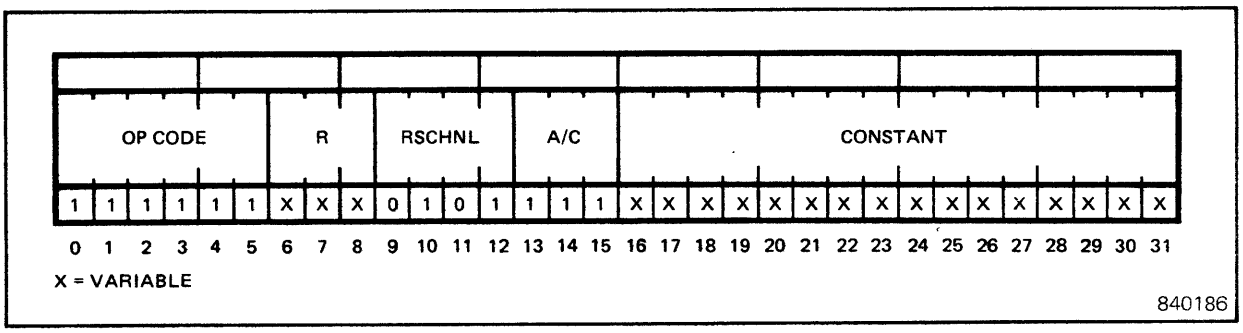
Bits 9 through 12 (6 hexadecimal) specify an HIO operation.

Bits 13 through 15 (7 hexadecimal) specify the augment code.

Bits 16 through 31 specify a constant that is added to the contents of R to form the logical channel and subaddress. If R is zero, only the constant is used to specify the logical channel and subaddress.

3.2.1.5 Reset Channel (RSCHNL)

The RSCHNL instruction ceases and resets all activity on the addressed channel and returns the channel to the idle state. RSCHNL also resets all subchannels and the devices connected to them. Any requesting or active interrupt level is reset. No condition codes are returned.



Bits 0 through 5 (FC hexadecimal) specify the operation code.

Bits 6 through 8, when nonzero, specify the general register. The register contents are added to the constant to form the logical channel and subaddress.

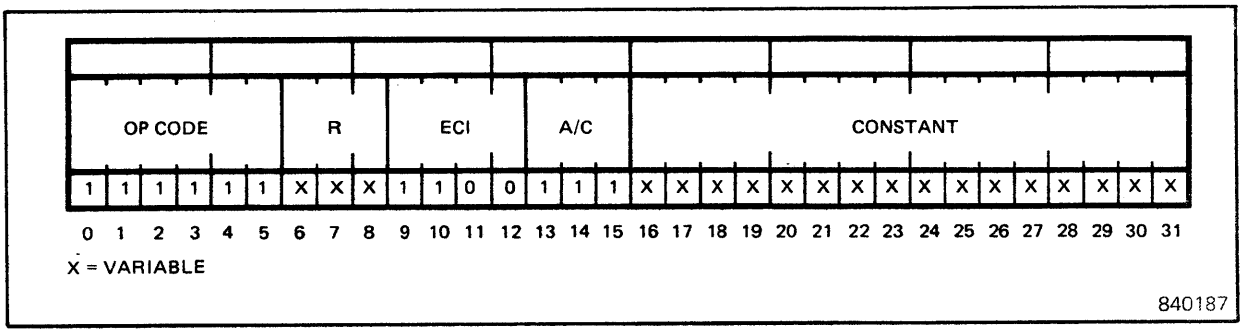
Bits 9 through 12 (5 hexadecimal) specify an RSCHNL operation.

Bits 13 through 15 (7 hexadecimal) specify the augment code.

Bits 16 through 31 specify a constant that is added to the contents of R to form the logical channel and subaddress. If R is zero, only the constant is used to specify the logical channel and subaddress.

3.2.1.6 Enable Channel Interrupt (ECI)

The ECI instruction enables the addressed channel to request interrupts from the CPU.



Bits 0 through 5 (FC hexadecimal) specify the operation code.

Bits 6 through 8, when nonzero, specify the general register. The register contents are added to the constant to form the logical channel and subaddress.

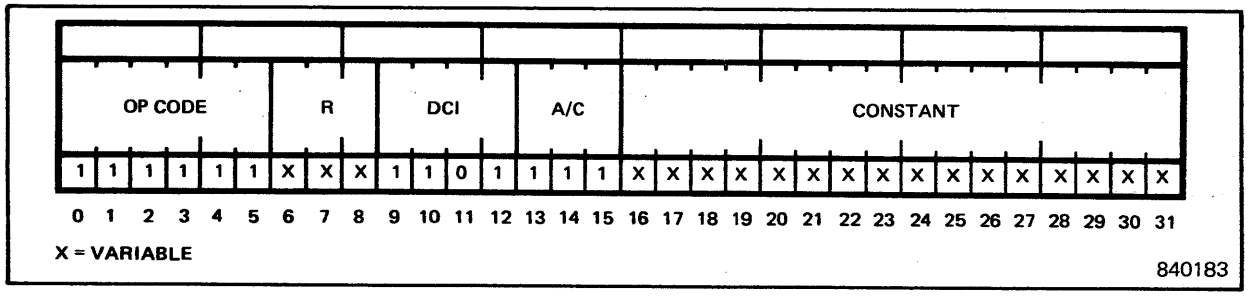
Bits 9 through 12 (C hexadecimal) specify an ECI operation.

Bits 13 through 15 (7 hexadecimal) specify the augment code.

Bits 16 through 31 specify a constant that is added to the contents of R to form the logical channel and subaddress. If R is zero, only the constant is used to specify the logical channel and subaddress.

3.2.1.7 Disable Channel Interrupt (DCI)

The DCI instruction disables the addressed channel from requesting interrupts from the CPU.



Bits 0 through 5 (FC hexadecimal) specify the operation code.

Bits 6 through 8, when nonzero, specify the general register. The register contents are added to the constant to form the logical channel and subaddress.

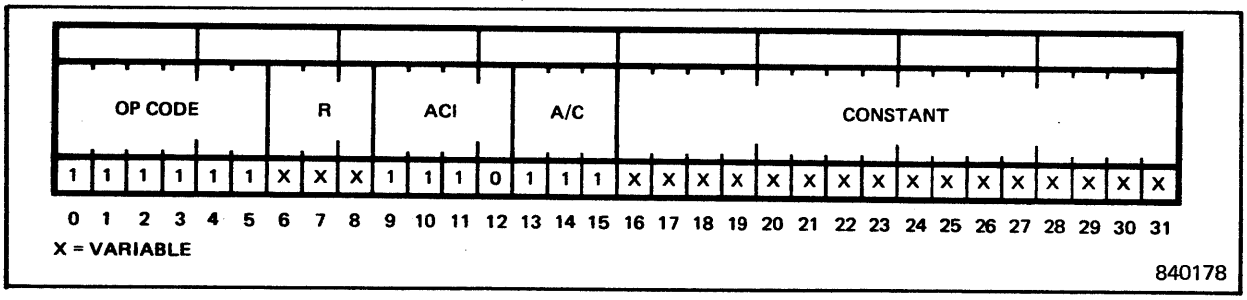
Bits 9 through 12 (D hexadecimal) specify a DCI operation.

Bits 13 through 15 (7 hexadecimal) specify the augment code.

Bits 16 through 31 specify a constant that is added to the contents of R to form the logical channel and subaddress. If R is zero, only the constant is used to specify the logical channel and subaddress.

3.2.1.8 Activate Channel Interrupt (ACI)

The ACI instruction causes the addressed channel to begin actively contending with other interrupt levels. This action prevents its level and all lower priority levels from requesting an interrupt. If a request for interrupt is currently pending in the channel, the requested interrupt is removed; however, the interrupt level remains in contention.



Bits 0 through 5 (FC hexadecimal) specify the operation code.

Bits 6 through 8, when nonzero, specify the general register. The register contents are added to the constant to form the logical channel and subaddress.

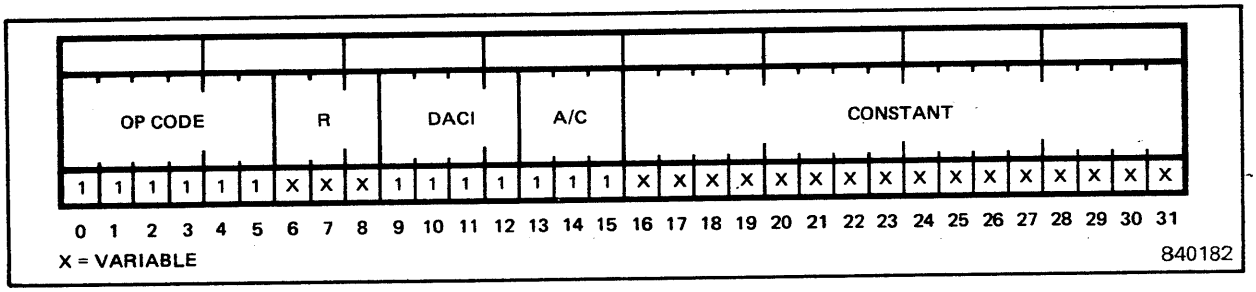
Bits 9 through 12 (E hexadecimal) specify an ACI operation.

Bits 13 through 15 (7 hexadecimal) specify the augment code.

Bits 16 through 31 specify a constant that is added to the contents of R to form the logical channel and subaddress. If R is zero, only the constant is used to specify the logical channel and subaddress.

3.2.1.9 Deactivate Channel Interrupt (DACI)

The DACI instruction removes the addressed channel's interrupt level from contention. If a request for an interrupt instruction is currently queued, the DACI instruction causes the queued request to actively request an enabled channel.



Bits 0 through 5 (FC hexadecimal) specify the operation code.

Bits 5 through 8, when nonzero, specify the general register. The register contents are added to the constant to form the logical channel and subaddress.

Bits 9 through 12 (F hexadecimal) specify a DACI operation.

Bits 13 through 15 (7 hexadecimal) specify the augment code.

Bits 16 through 31 specify a constant that is added to the contents of R to form the logical channel and subaddress. If R is zero, only the constant is used to specify the logical channel and subaddress.

The deactivated capability is also provided by the branch and reset interrupt (BRI) instruction. Note: This capability is provided only in the Gould 32/70 SERIES Computers.

The execution of the DACI and BRI instructions implies that the channel is currently active.

3.2.2 Input/Output Initiation

An I/O operation is initiated by a start I/O instruction. If the specified channel/subchannel is present and not busy, the SIO is accepted and the CPU continues to the next sequential instruction. The channel/controller asynchronously processes the I/O request specified by the instruction.

3.2.2.1 Input/Output Command List Address (IOCLA)

The input/output command list address (IOCLA) specifies the real address of the first IOCD associated with a start I/O. The information is transferred to the channel, and the contents are not affected by an I/O operation.

Upon execution of the I/O instruction, the software is free to modify the IOCLA. A start I/O is the only instruction that can cause the IOCLA to be transferred to the channel.

Successful execution of the SIO causes the CPU to transmit the IOCLA to the channel. The IOCLA is located in the main memory at locations specified by the service interrupt

vector plus 16. Each of the 16 channels has a corresponding service interrupt vector. The format for the IOCLA, indicated by the contents of the service interrupt vector plus 16, is shown in Figure 3-3. The real IOCLA is passed to the channel on the data bus.

3.2.2.2 Input/Output Command Doubleword (IOCD)

The IOCLA specifies the address of the input/output command list (IOCL) to be executed by the channel. An IOCL consists of one or more input/output command doublewords (IOCD). Each IOCD must be aligned on a fullword boundary and have the format shown in Figure 3-4.

The real data address specifies the starting address of the data area. The data address will be a byte address and the channel will internally align the information transferred to or from main memory. While any starting address is allowable, more efficient system operation will result if the software programmer aligns the data area to start at a fullword boundary (bits 30 and 31 of address being zero).

The byte count specifies the number of bytes that are to be transferred to or from main memory. Although the channel may transfer data to/from memory one, two or four bytes at a time, it will accommodate byte counts that are not multiples of its natural transfer width.

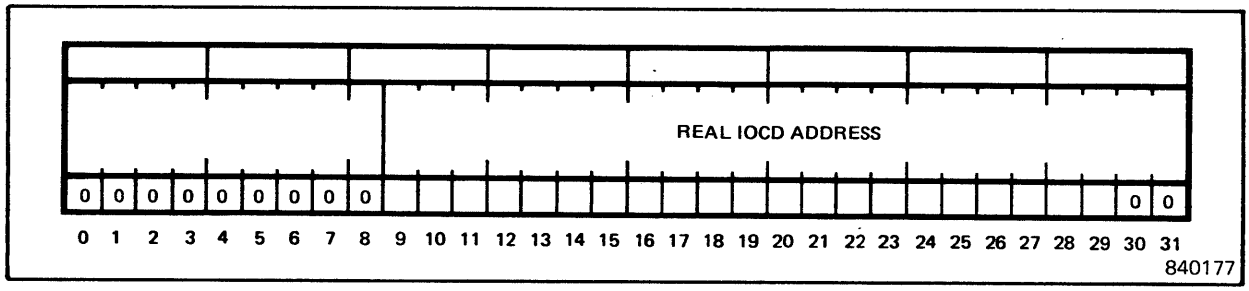


Figure 3-3. Input/Output Command List Address (IOCLA)

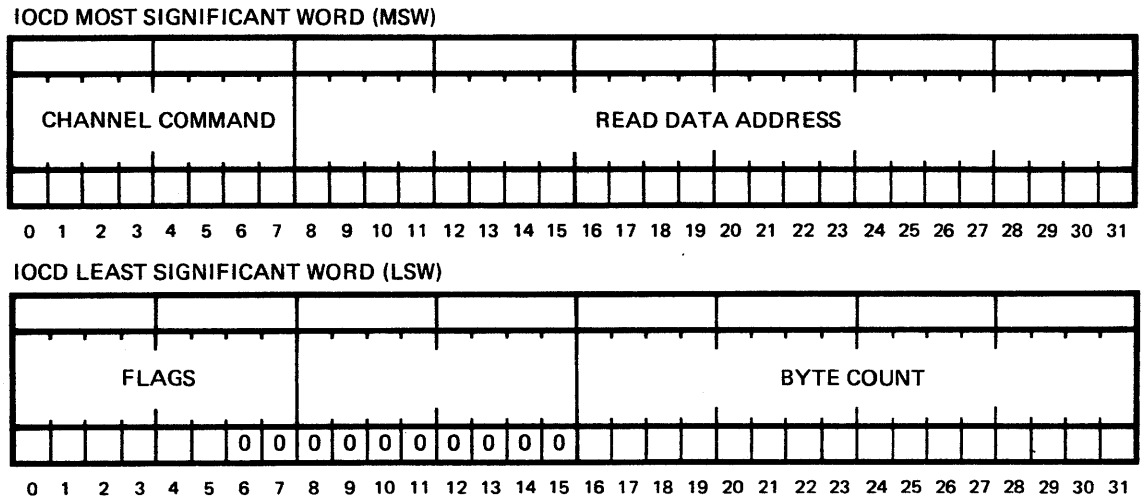
3.2.2.3 Channel Commands (Op-codes)

The BTP supports 16 commands that are passed to it via the opcode field of the I/O command doubleword. These consist of channel control, device control, and data commands. Table 3-1 lists these commands, provides the hexadecimal value for each opcode, and a brief description.

3.2.2.4 Channel Flags

The IOCD format provides a field of eight bits which make up the flag byte. The flag byte provides the programmer with the capability to perform functions that exceed the typical tape controllers. These flags are described as follows:

Mnemonic	Bit	Description
DC	0	Data chain - this allows a single tape record to be broken into discontiguous segments for a read, and allows discontiguous memory segments to be combined into a single record.



WORD	BITS	DEFINITION
MSW	0-7	COMMAND CODE. SPECIFIES CHANNEL COMMAND TO BE EXECUTED BY THE BTP.
MSW	8-31	REAL DATA ADDRESS. THE ADDRESS OF THE LOCATION IN MAIN MEMORY WHERE DATA IS LOCATED OR TO WHICH DATA WILL BE TRANSFERRED.
LSW	0-7	FLAG BYTE. THE FOLLOWING FLAGS MODIFY COMMAND EXECUTION: 0 DATA CHAIN (HOLDS OF TERMINATION WHEN XFER COUNT = 0) 1 COMMAND CHAIN 2 SUPPRESS INCORRECT LENGTH 3 SKIP 4 PROGRAM CONTROLLED INTERRUPT 5 N/A 6 ZERO 7 ZERO
LSW	8-15	NOT USED. ALWAYS ZERO
LSW	16-31	BYTE COUNT. DESIGNATES THE NUMBER OF BYTES TO BE TRANSFERRED.

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Figure 3-4. Input/Output Command Doubleword (IOCD)

Table 3-1
Channel Commands

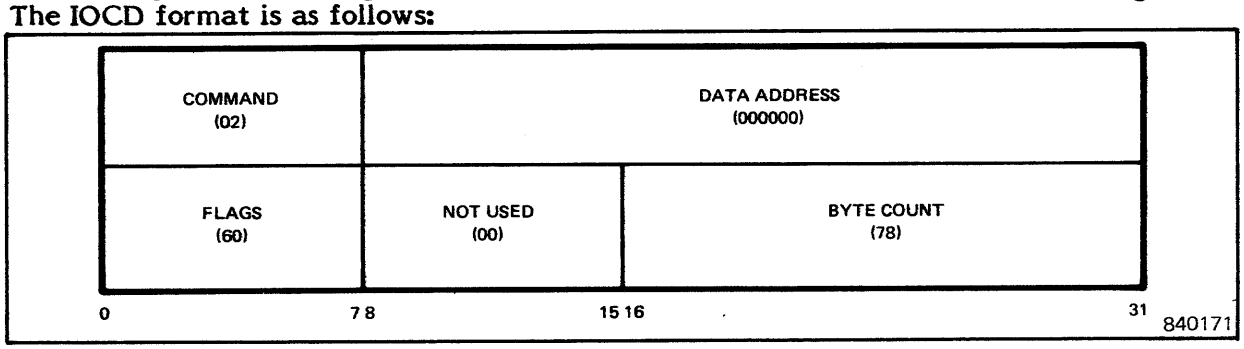
Mnemonic	Hex Code	Description	Type
INCH	00	Initialize channel	Channel control
NOP	03	No operation	Channel control
SNS	04	Sense/resync buffer	Channel control
SETM	83	Set mode register	Channel control
WRT	01	Write data to tape	Data command
RDF	02	Read data forward	Data command
RDB	0C	Read data backward	Data command
RDC	13	Read and compare	Device control
AR	43	Advance record	Device control
BR	53	Backspace record	Device control
AFM	63	Advance to filemark	Device control
BFM	73	Backspace to filemark	Device control
WFM	93	Write filemark	Device control
ERA	A3	Erase fixed length	Device control
REW	23	Rewind to load point	Device control
RWU	33	Rewind and unload	Device control

Mnemonic	Bit	Description
CC	1	Command chain - this connects contiguous IOCDs together to allow the channel to execute each in succession without the software initiating each operation.
SKIP	2	Skip data transmission - when used with data chaining, allows segments of a record to be skipped, preventing data transmission to SelBUS memory. Valid for read operations only.
SLI	3	Suppress length indicator - this is used on records read from tape that are not equal to the byte count as specified in the IOCD (error status is generated). The use of this flag prevents the posting of the status and if the error is due to a short record, chaining will still be allowed.
PPCI	4	Post programmed controlled interrupt - when this is set and used during chained IOCDs, an interrupt is requested for servicing when the IOCD associated with the flag has been completed. This is a useful flag for tracking multiple buffers. Note: This bit is referred to as the PPCI bit and the interrupt which is generated as a result of this bit being set is the program controlled interrupt (PCI).
N/U	5-7	Not used.

3.3 CPU Initial Program Load (IPL)

The initial program load (IPL) instruction causes the BTP to load main memory with a user program located on the tape media. The IPL instruction depends upon operator stimulus at the operator console to select the BTP and device address to be loaded. The CPU must be halted before the operator can initiate the IPL.

The CPU generates a single IOCD located in main memory locations zero through four. The IOCD format is as follows:



The hexadecimal values are: 02000000
60000078

where:	command	02	= read opcode
	data address	00	= starting buffer address
	flags	60	= command chain and suppress
	byte count	78	= 120 (decimal) bytes to be transferred to memory

The format of the tape record loaded into memory is as follows:

Bytes	Contents	Memory Address
00-03	New PSD, word 1	00000000
04-07	word 2	00000004
08-11	New IOCD, word 1	00000008
12-15	word 2	0000000C
16-77	User loader program	00000010

After the IPL protocol is issued to the BTP and it starts the process, the CPU monitors memory location 00000004 looking for the contents to change from 60000078. This tells the CPU a new PSD has been placed in memory. The CPU cannot load the new PSD until it receives an interrupt from the BTP. The BTP generates the interrupt only when it completes the IOCD list. Note that the overlay is chained into and causes the BTP to execute the new IOCD which is placed in memory from the record it initially read. The user loader program may specify as many records as necessary to be loaded in memory to satisfy programming requirements.

3.3.1 Condition Codes

Status returned from the channel is understood to be a subchannel status, associated with a specific subchannel. Subchannel status is routinely presented to the CPU. Status responses take two forms: a condition code setting and a status doubleword.

A condition code is always generated in response to a CPU instruction. The condition code may or may not be accompanied by a status doubleword. The channel response and condition codes are shown in Figure 3-5.

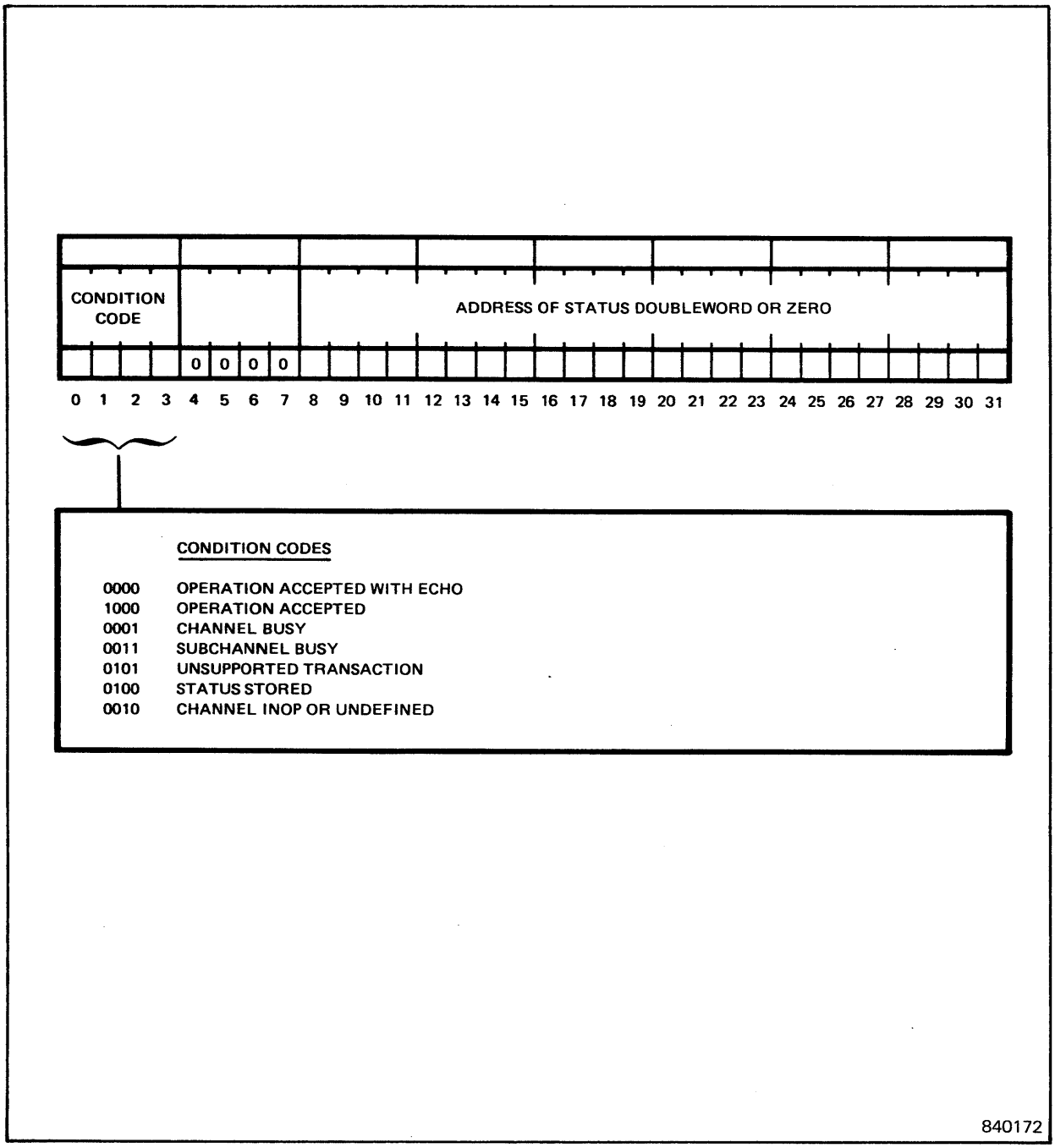
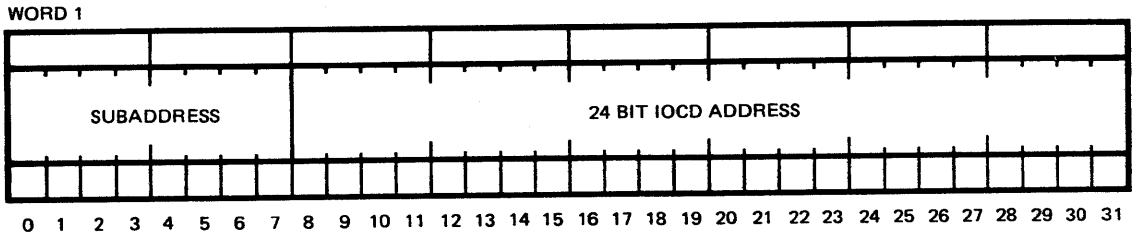


Figure 3-5. Channel Condition Code Response

3.3.2 Status Doublewords

The BTP channel maintains a four word status queue in the BTP's allocated main memory buffer. The two status doublewords are used alternately by the BTP. After the status is stored in one of the status entries, the BTP sends the address to the CPU during a DRT. When the BTP has additional status to be posted, it uses the other location and notifies the CPU that new status is available. When the CPU acknowledges the request, the new status address is again sent to the CPU via a DRT. The status queue contains two status doublewords which are formatted as follows:

Status Doubleword



STATUS BITS

BIT	MNEMONIC	FUNCTION
0	ECHO	HALT I/O AND STOP I/O FUNCTION
1	PCI	PROGRAM CONTROLLED INTERRUPT
2	IL	INCORRECT LENGTH
3	CPC	CHANNEL PROGRAM CHECK
4	CDC	CHANNEL DATA CHECK
5	CCC	CHANNEL CONTROL CHECK
6	IC	INTERFACE CHECK
7	CHC	CHAINING CHECK
8	DB	DEVICE BUSY
9	SM	STATUS MODIFIER
10	CNTE	CONTROLLER END
11	ATTN	ATTENTION
12	CE	CHANNEL END
13	DE	DEVICE END
14	UC	UNIT CHECK
15	UE	UNIT EXCEPTION

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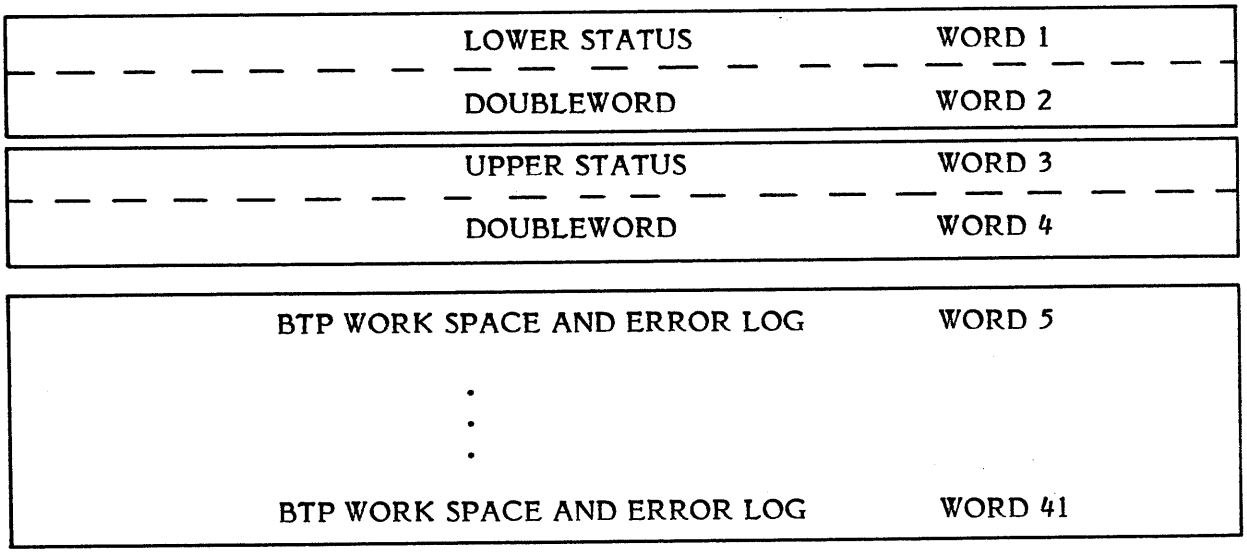
Main memory status allocation



3.3.2.1 Final Status Presentation

All I/O programs terminate with final status presentation; program execution is not complete until this status is presented. The normal means for accomplishing this status presentation is via an I/O interrupt. When the interrupt is acknowledged, two words of status are presented and program execution is complete.

The status doubleword format is shown in Figure 3-6. Word one contains the subaddress of the interrupting device and the absolute IOCD address of the final IOCD, plus eight. Word two contains the channel status as it existed at program termination and the residual byte count.

Should the attempt to interrupt the CPU and present final status coincide with an SIO or test input/output (TIO) instruction, the final status is presented, the instruction is ignored, and the interrupt is withdrawn.

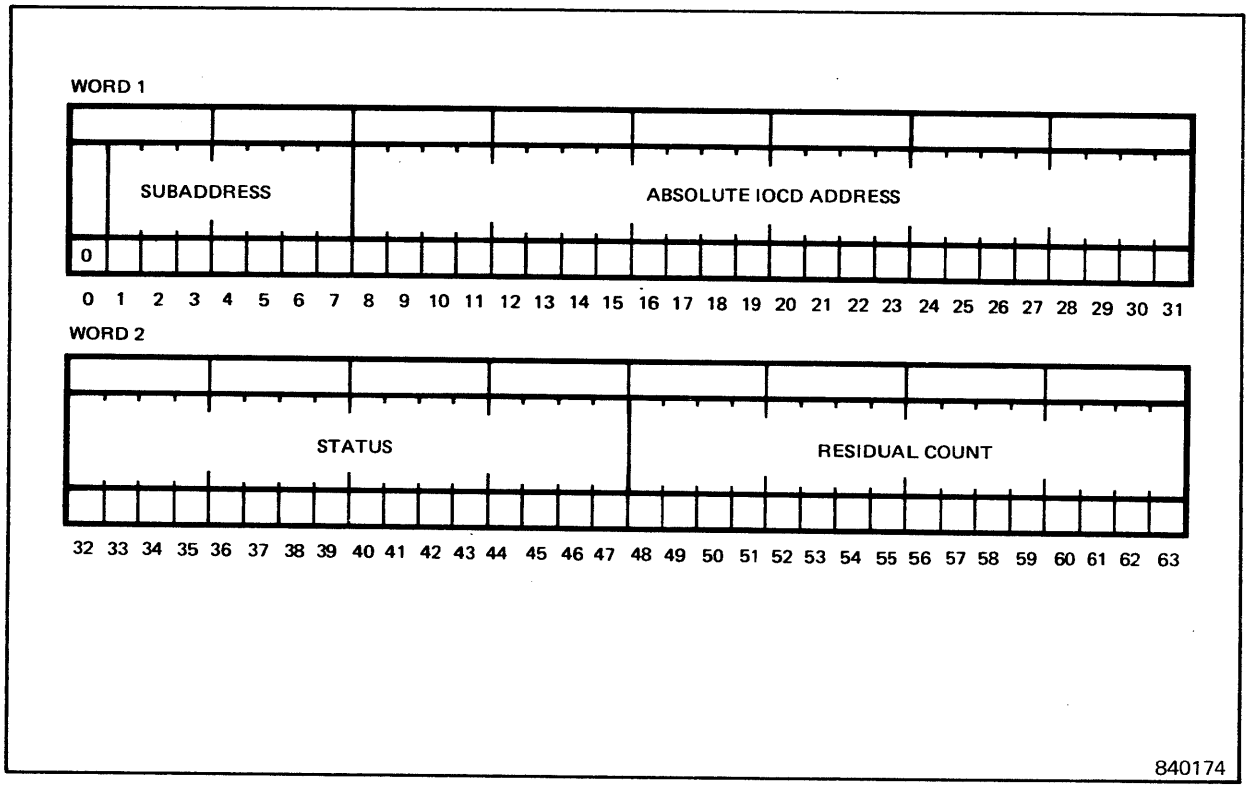


Figure 3-6. Final Status Doubleword Format

3.3.2.2 Program Controlled Interrupts

A program controlled interrupt (PCI) may be specified in any IOCD, including the first IOCD of an I/O program. When a PCI is called for, a PCI flag bit is set by the BTP. This section schedules the issue of a PCI when IOCD execution is complete. The effort to issue the PCI is delayed until all data operations associated with the IOCD execution are complete. The PCI polling is then initiated, and the channel continues with I/O program execution. When the CPU acknowledges the interrupt, PCI status is transmitted to the CPU. PCI status has the same format as final status. However, the PCI bit will be on alone, and the byte count field may or may not be significant.

3.3.2.3 Device End and Unsolicited Interrupts

When a tape rewind is initiated and command chaining is not specified, a channel end interrupt is presented when the rewind has been successfully initiated. Later, when the rewind completes, a second device end interrupt occurs, signaling that the transport has rewound and returned to the ready state. Device end (DE) interrupts are not issued while an I/O program is in execution. Instead, they are issued one at a time after any I/O program in execution is complete.

The need to issue a device end (DE) interrupt is noted in the BTP by setting a rewind flag for the associated drive. When the drive returns are ready, the flag is reset and the interrupt is issued. It is possible that more than one drive will complete and interrupt during a time when the channel is busy. In this event, interrupts are issued sequentially in a fixed drive priority order.

In addition to the rewind DE interrupts, a DE interrupt is issued whenever a drive changes its state of readiness. This capability operates as follows. When the channel is activated by INCH command execution operation, each drive is polled for its state of readiness. The state of the READY signal is recorded. Subsequently, the channel polls the drives and compares them to the previously set READY flags to detect any change in a drive's READY signal. This polling occurs at a low rate (500 millisecond intervals) and takes place only when the channel is not busy executing an I/O program.

This unsolicited interrupt makes it possible for the system to be made aware of changes in drive availability without polling from the CPU. It automatically notifies the CPU when a system operator has loaded a tape or when a tape malfunction, such as the loss of vacuum in tape columns, causes a drive to lose its ready state. Again, this monitoring function is fully effective only when it is supported by the use of the offline or rewind and unload BTP commands.

3.4 Initialization

3.4.1 Main Memory Buffer Allocation

The BTP requires a 41 word allocation in main memory to be used for status storage, cache queue work space, error retry counter, and error log tables. The layout and format is shown in Figure 3-7. A complete description of the BTP usage of the cache queue work space is in Chapter 4 Section 4.3.3.2 of this manual.

3.4.2 Channel Initialization

Prior to any I/O request other than the IPL sequence, the BTP requires the allocation of main memory to allow normal operation of the channel. The responsibility of initializing the main memory allocation buffer is placed upon the software.

The BTP requires the following entries in the allocation area established at the time the INCH command is issued to the BTP. Refer to Figure 3-7.

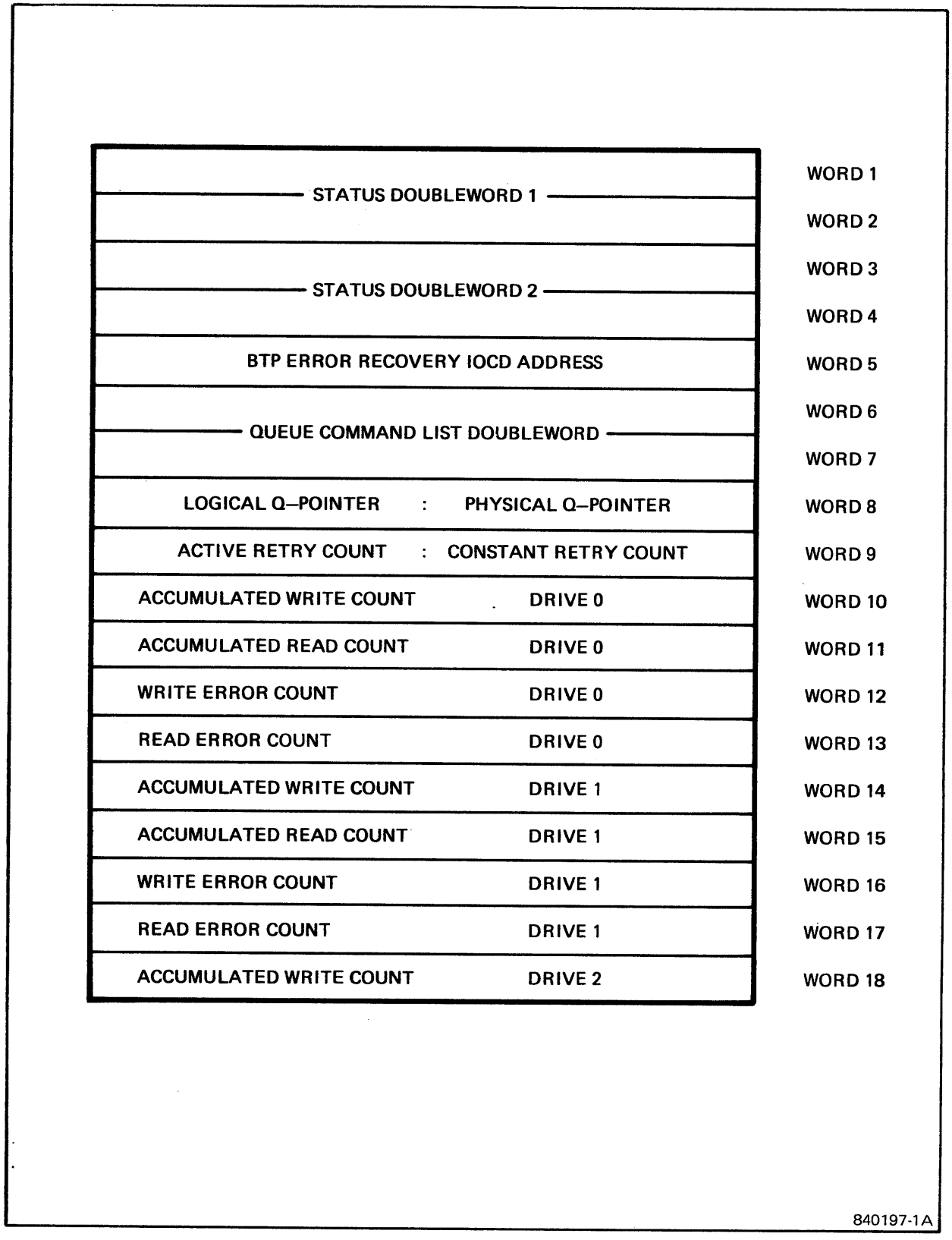


Figure 3-7. Main Memory Buffer Layout

ACCUMULATED READ COUNT	DRIVE 2	WORD 19
WRITE ERROR COUNT	DRIVE 2	WORD 20
READ ERROR COUNT	DRIVE 2	WORD 21
ACCUMULATED WRITE COUNT	DRIVE 3	WORD 22
ACCUMULATED READ COUNT	DRIVE 3	WORD 23
WRITE ERROR COUNT	DRIVE 3	WORD 24
READ ERROR COUNT	DRIVE 3	WORD 25
ACCUMULATED WRITE COUNT	DRIVE 4	WORD 26
ACCUMULATED READ COUNT	DRIVE 4	WORD 27
WRITE ERROR COUNT	DRIVE 4	WORD 28
READ ERROR COUNT	DRIVE 4	WORD 29
ACCUMULATED WRITE COUNT	DRIVE 5	WORD 30
ACCUMULATED READ COUNT	DRIVE 5	WORD 31
WRITE ERROR COUNT	DRIVE 5	WORD 32
READ ERROR COUNT	DRIVE 5	WORD 33
ACCUMULATED WRITE COUNT	DRIVE 6	WORD 34
ACCUMULATED READ COUNT	DRIVE 6	WORD 35
WRITE ERROR COUNT	DRIVE 6	WORD 36
READ ERROR COUNT	DRIVE 6	WORD 37
ACCUMULATED WRITE COUNT	DRIVE 7	WORD 38
ACCUMULATED READ COUNT	DRIVE 7	WORD 39
WRITE ERROR COUNT	DRIVE 7	WORD 40
READ ERROR COUNT	DRIVE 7	WORD 41

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Figure 3-7. Main Memory Buffer Layout (Continued)

Word 9 error retry count

The retry count is initialized with the number of retries the user wishes the BTP to perform to recover from errors. The right-half word is copied by the BTP to the left-half word. The left-half word is the active retry count, whereas the right-half word is the constant supplied by the software.

If the software loads zeros in the right-half word, the BTP uses a default value of 0005 for the retry count. The BTP then places the value 0005 in the right and left-half and words.

Since the BTP queues write requests from software into its cache RAM, the software cannot perform write error recovery. If the BTP cannot recover from the error, neither can the software, therefore it is recommended that the retry word be initialized to 0000 allowing the default value to preside.

The error recovery algorithm is described in Chapter 4 Section 4.3.8 of this manual.

Words 10 through 41 Error Log

The error log should be initialized the first time the BTP is brought from an un-initialized state, or if it has been re-initialized to relocate the main memory buffer.

The BTP updates each entry in the error log to indicate data errors relative to the amount of data transferred.

The BTP increments the accumulated write count with the byte count specified by the IOCD in execution. The same applies to the accumulated read count.

The BTP increments the write error count by one for a detected write error. It does not add the retries required to successfully write the data. The same applies to the read error count.

CHAPTER 4

THEORY OF OPERATION

4.1 Introduction

The buffered tape processor (BTP) is shown in the overall block diagram Figure 4-1. This figure depicts the BTP in its maximum configuration capability. The BTP system consists of a single logic card, two cables, and an IOX card.

4.2 General Theory

4.2.1 Purpose

The purpose of the BTP is to provide a high performance buffered interface between the CPU and the magnetic tape drive. The BTP performs tape error recovery between the buffer and the tape drive while simultaneously performing data transfer operations to or from the CPU. The BTP performs complex tasks that do not require CPU/software intervention until the task is complete, eliminating the typical overhead and resources associated with tape operations. The BTP increases overall system efficiency by utilizing the command chain, data chain, transfer-in-channel (TIC), programmed controlled interrupts, skip, and the read and compare capabilities.

4.2.2 Basic Organization

4.2.2.1 System Components

The BTP sub-system consists of three components: the BTP circuit card, the IOX connector card, and a formatted tape drive.

The BTP is based on a 32-bit microprogrammable I/O processor. It contains the channel, buffer, and device logic all on one circuit card. Installed in the SelBUS, the BTP provides data transfer rates of up to two megabytes per second in or out of the cache buffer.

The IOX card provides support for the cables and eliminates possible backplane damage caused by direct cable connection to the pin side of the SelBUS. The IOX card is totally passive, there is no logic or signal transposing performed. The IOX connects to the P1A and P1C connectors on the SelBUS adjacent to the BTP slot. Two 50 pin flat ribbon cables are connected from the IOX to the formatted tape drive.

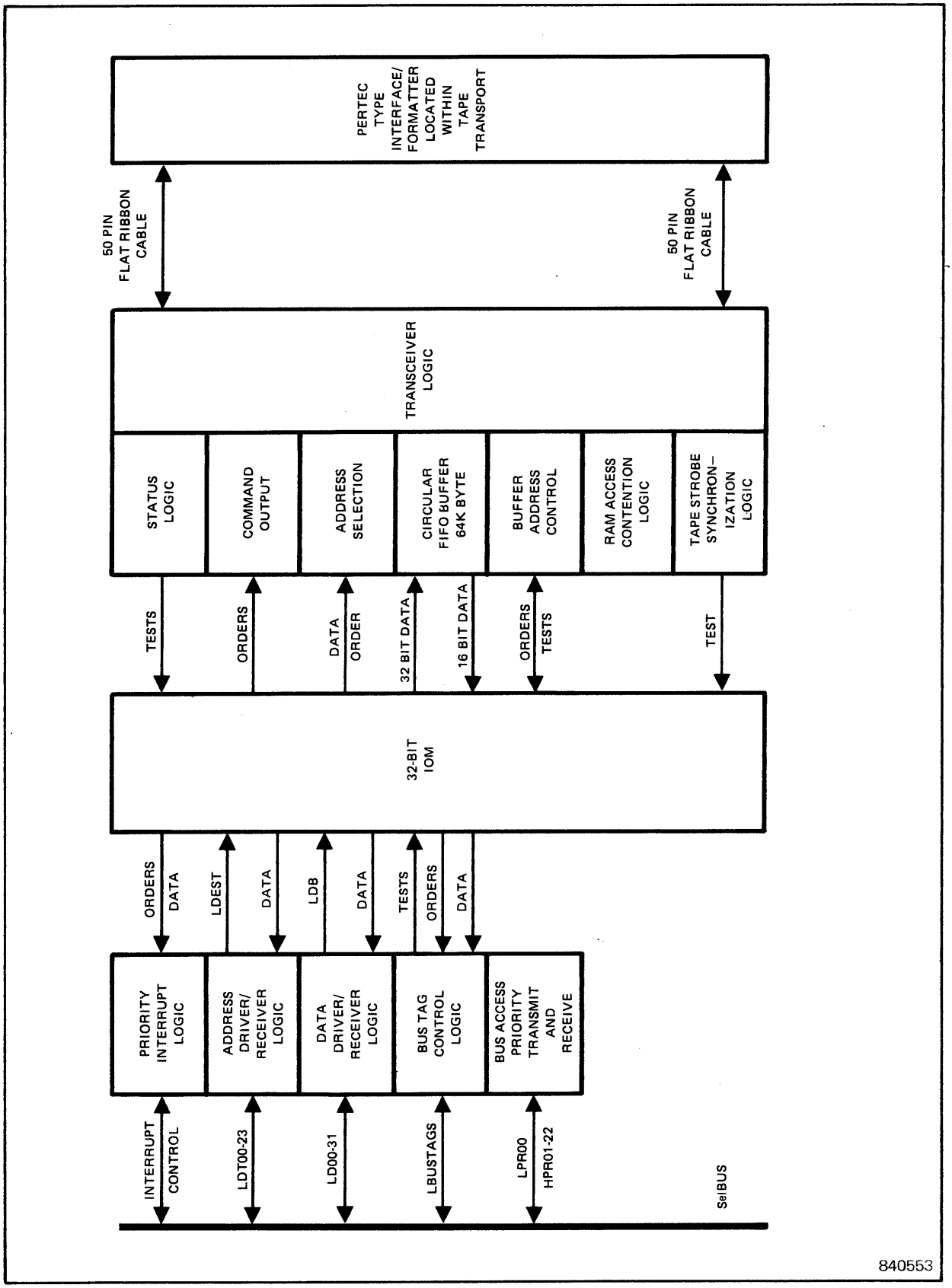

Figure 4-1. BTP Block Diagram

The BTP supports the Pertec type imbedded formatter interface. This industry standard interface is available from many tape drive manufacturers, however, only those specified by Gould CSD should be used. Other tape drives may not perform as expected on the BTP, resulting in improper operation.

4.2.2.2 System Firmware

The BTP firmware, resident to the BTP, controls the overall operation of the BTP. It is the channel's responsibility to support CPU and memory communications. The controllers responsibilities include buffer management and control functions for up to eight tape drives. There are onboard firmware diagnostics executing tests whenever the BTP is idle, thus allowing fault isolation to the board level.

4.2.2.3 Overall Operation

The BTP is considered an integrated channel controller since the controller logic and firmware is part of the channel logic a d firmware. T e BTP operate as a selector channel with the formatted tape drive. This means that once an operation is initiated, to a selected tape drive, the BTP cannot service another drive until the operation is complete. This is due to the Pertec type interface.

The BTP attempts to increase system efficiency by reducing the amount of system resources that are typically used to support tape operation. The buffer allows the connected tape drive to take on the appearance of a 1200 inch per second tape drive recording 1600 characters per inch.

The BTP's reduced requirement of the system resources means that other devices in the system, particularly the disc, can receive a greater portion of the resources. For example, a 75 inch per second (ips) tape drive writing at 1600 characters per inch (cpi) requires 17 milliseconds to write 2048 bytes, plus 5 milliseconds to start the tape in motion. The BTP's buffer requires 1.02 milliseconds for the entire operation. Therefore, the system has (22 minus 1.02 =) 20.98 milliseconds of additional time, that was previously dead time wasted, waiting for the tape operation to complete.

Once an operation is completed at the buffer level, the BTP generates an interrupt request indicating the completion. At this point the BTP is able to accept another command from software even though the physical operation at the tape drive level may not be finished.

The delayed write approach through the buffer places the burden of error recovery upon the BTP. Once the BTP begins buffered write operations the standard software error recovery techniques cannot be used. The BTP performs a backspace record-erase followed with a re-write of the record. The retry count defaults to five, however, the user can establish a maximum retry at the initialization of the BTP if so desired.

Since the BTP performs delayed writes to the tape drive, the physical tape events such as end-of-tape and unrecoverable write errors are not synchronized to the system. In order to insure data integrity the software must re-synchronize the BTP to the system at the end of a job via the SENSE command. The BTP delays responding to the SENSE command until the buffer is empty, or if it has an unrecoverable error condition to report. This requirement is only necessary for write operations, read operations are always in synch to the system.

When using the BTP to restore data from the tape, the BTP encounters the initial 5 millisecond access delay, however, the buffer continues to access more records from tape without any software initiation. This is record prefetching, and it reads ahead until the queue is full. This technique provides optimum access to the tape since most tape operations are sequential.

4.3 Detailed Theory

4.3.1 BTP Processor

4.3.1.1 SelBUS Interface

The SelBUS is a high performance synchronous time division multiplexed bus that functions at a continuous rate of 26.67 million bytes per second. It provides a direct high speed path between the CPU, the memory, and the IOMs.

The SelBUS interface, contained on the IOM, provides drivers and receivers for data and control lines on the SelBUS, a toggle switch for electrically disconnecting the BTP from the SelBUS, control logic, clock and reset logic, priority interrupt polling logic, SelBUS priority logic, 24-bit destination bus (address) register, and a 32-bit SelBUS data register.

4.3.1.2 Microprogrammable Processor

The basic microprocessor used for the BTP is the I/O microprocessor (IOM). The IOM microinstructions are 32-bits wide. There are two 16-bit groups of 16 registers that are available as working read/write memory (RA and RB register groups). The output from each register pair is the input to the 16-bit wide arithmetic logic unit (ALU), the SelBUS interface, and the IOM port of the cache RAM. Data is input to the register pairs through two four-to-one multiplexers controlled by a microcommand. Conditional branches are performed by testing one of the 64 available signal lines, some of which are dedicated to the IOM, with the remainder within the buffer control logic and the tape formatter interface. There are 40 ORDERS, 24 of which create a 75 nanosecond pulse, and the remaining 16 are latched such that they can be set or reset by the microinstruction. There is a micro level interrupt that is activated by a non-present memory condition, an error transfer on the SelBUS, a reset channel command, or by the CPU accessing the SelBUS interface. The microinterrupt, if enabled, causes the microprogram counter to be reset to zero where the interrupt processing routine is located. Also, during the microinterrupt phase, the hardware automatically stores the current value of the micro PC into the RA register group address zero. The control read-only memory (CROM) for the BTP IOM is 4096 words by 32-bits wide. The control firmware resides in the CROM and controls the IOM, which in turn controls the SelBUS interface, the cache control logic and the formatter interface.

4.3.1.3 Tape Interface Logic

The tape formatter interface logic consists of drivers, receivers, and registers that provide communications between the microprocessor/buffer and the tape formatter. Table 4-1 lists the P1A and P1C connections, Table 4-2 lists the signals transmitted to the tape formatter, and Table 4-3 lists the signals received from the tape formatter.

Table 4-1
P1A and P1C Connectors (Sheet 1 of 2)

CONNECTOR	SIGNAL PIN	GROUND PIN	SIGNAL
P1A	2	1	FBY
	4	3	LWD
	6	5	WD4
	8	7	GO
	10	9	WD0
	12	11	WD1
	14	13	SGL
	16	15	LOL
	18	17	REV
	20	19	REW
	22	21	WDP
	24	23	WD7
	26	25	WD3
	28	27	WD6
	30	29	WD2
	32	31	WD5
	34	33	WRT
	36	35	THR2
	38	37	EDIT
	40	39	ERASE
	42	41	WFM
	44	43	THR1
	46	45	TAD0
	48	47	RD2
	50	49	RD3

Table 4-1
P1A and P1C Connectors (Sheet 2 of 2)

CONNECTOR	SIGNAL PIN	GROUND PIN	SIGNAL
P1C	1	5	RDP
	2	5	RD0
	3	5	RD1
	4	5	LDP
	6	5	RD4
	8	7	RD7
	10	9	RD6
	12	11	HER
	14	13	FMK
	16	15	ID/CCG
	18	17	FEN
	20	19	RD5
	22	21	EOT
	24	23	OFL
	26	25	NRZI
	28	27	RDY
	30	29	RWD
	32	31	FPT
	34	33	RSTR
	36	35	WSTR
	38	37	DBY
	40	39	SPEED
	42	41	CER
	44	43	ONL
	46	45	TAD1
	48	47	FAD
	50	49	DEN

Table 4-2
Signals to the Tape Formatter

SIGNAL PIN	GROUND PIN	SIGNAL	DESCRIPTION
P1C-48	-47	FAD	Formatter address
P1A-46	-45	TAD0	Transport address 0
P1C-46	-45	TAD1	Transport address 1
P1A-8	-7	GO	Command strobe
P1A-18	-17	REV	Reverse/forward command bit
P1A-34	-33	WRT	Write/read command bit
P1A-42	-41	WFM	Write filemark command bit
P1A-38	-37	EDIT	Edit modifier
P1A-40	-39	ERASE	Erase command bit
P1A-44	-33	THR1	Read threshold 1
P1A-36	-35	THR2	Read threshold 2
P1C-50	-49	DEN	Density select
P1A-20	-19	REW	Rewind control signal
P1C-24	-23	OFL	Off-line control signal
P1A-4	-3	LWD	Last word control signal
P1C-18	-17	FEN	Formatter enable
P1A-22	-21	WP	Write parity bit
P1A-10	-9	W0	Write data bit 0
P1A-12	-11	W1	Write data bit 1
P1A-30	-29	W2	Write data bit 2
P1A-26	-25	W3	Write data bit 3
P1A-6	-5	W4	Write data bit 4
P1A-32	-31	W5	Write data bit 5
P1A-28	-27	W6	Write data bit 6
P1A-24	-23	W7	Write data bit 7
P1A-16	-15	LOL	Load on line control signal

Table 4-3
Signals from the Tape Formatter

SIGNAL PIN	GROUND PIN	SIGNAL	DESCRIPTION
P1A-2	-1	FBY	Formatter busy
P1C-38	-37	DBY	Data busy
P1C-16	-15	ID/CCG	Ident burst/check character gate
P1C-12	-11	HER	Hard error
P1C-14	-13	FMK	Filemark
P1C-28	-27	RDY	Ready
P1C-44	-43	ONL	Online
P1C-30	-29	RWD	Rewinding
P1C-32	-31	FPT	File protect
P1C-4	-5	LDP	Load point
P1C-22	-21	EOT	End of tape
P1C-26	-25	NRZI	NRZI/PE mode
P1A-14	-13	SGL	Single (N.U.)
P1C-40	-39	SPEED	Transport speed indicator
P1C-36	-35	WSTR	Write strobe
P1C-34	-33	RSTR	Read strobe
P1C-1	-5	RP	Read parity bit
P1C-2	-5	R0	Read data bit 0
P1C-3	-5	R1	Read data bit 1
P1A-48	-47	R2	Read data bit 2
P1A-50	-49	R3	Read data bit 3
P1C-6	-5	R4	Read data bit 4
P1C-20	-19	R5	Read data bit 5
P1C-10	-9	R6	Read data bit 6
P1C-8	-7	R7	Read data bit 7
P1C-42	-41	CER	Corrected error

The Pertec type interface is considered to operate as a selector interface. There is no capability to allow simultaneous data transmission. Once a transport is selected and commanded, the channel must be dedicated to that particular device. The only exception is during a rewind operation. Once the drive is directed to perform a rewind, the channel is free to communicate with another tape unit. The BTP can transfer data to another unit, or it can issue another rewind. If the channel selects another rewind, it is free again to transfer data or rewind.

The Pertec type interface consists of unidirectional read and write data paths. Each path contains eight data bits and one parity bit for odd parity. The data is strobed with an associated read strobe or write strobe which is then monitored by the IOM test matrix. When reading data from tape the read strobe (RSTR) clocks the incoming data and parity into a holding register resulting in an automatic request to put the data and parity in RAM. When the tape is commanded to write data it generates a write strobe to the BTP interface requesting data from the buffer. The data must be, and is, ready for the write strobe (WSTR). There is no interlocked handshaking of data. Therefore, the BTP is responsible for initiating the operation and servicing the end of the operation. The BTP firmware does not become involved with data transfers at the actual interface level, instead, it handles data at its ports to the RAM.

The Pertec type interface provides the BTP with device status signals that are tested prior to and after a command is issued to the tape unit. The interface signal NRZI is used to identify the density which is currently selected at the tape unit. When the unit is operating in the PE mode (1600 bpi) it automatically generates an identification burst during a write operation, when positioned at load point. The BTP expects the ID BURST and verifies its occurrence. During a read operation in PE mode, where the tape is initially positioned at load point, the absence of the ID BURST indicates that the tape mounted is not recorded, or is not recorded in PE. The BTP prevents the tape unit from allowing tape run-away, and generates error status. When the tape unit is selected in NRZI mode (800 bpi) it does not use the ID BURST for density verification. However, it does generate the ID BURST, but it is used to signal the end of the data portion of a tape record and the beginning of check character transmission during read operations to the receiving logic in the BTP. The BTP does not use the check characters, it simple gates out the read strobe when ID-CCG-TST is asserted.

To initiate tape operations, the BTP firmware tests for the basic state of the tape unit such as rewind, online, file protected, and ready. In addition to the elementary signals, the BTP must also be aware of data busy (DBY) and formatter busy (FBY). Commands are not issued during the active state of data busy. Data busy indicates that data is or about to be transferred. The formatter busy signal is monitored whenever the BTP requires a change in the direction of the tape. This signal implies that the tape is still in motion. In order to obtain a streaming effect in the tape unit the BTP issues another command to the tape during this time provided the cache is capable of handling the operation. In streaming tape transports this period of time is referred to as the re-instruct window. Its duration is typically thirty percent of the total interrecord gap timing.

The actual commands are formed by the microcode as literal values eventually loaded into the RA register via an RB to RA pass. The register outputs are connected to open collector drivers to the formatter interface. The order structure has a level order assigned to the GO signal at the interface. The firmware sets the order and holds the register for approximately 10 clocks. The order is reset three clocks before the register is dropped because the formatter accepts the command on the trailing edge of the GO signal. Holding the register beyond the resetting of GO insures that the command code is stable.

The Pertec type interface currently allows up to eight tape units to be addressable by one interface. However, the maximum formatted start/stop tape units allowed is only two. This is due to the tape addressing convention implemented in the tape units. Therefore, the first formatted tape unit supports up to three additional non-formatted slave tape units, and the second formatted tape unit supports an additional three slaves. Refer to section 2.2.1.6 for tape transport address selection.

4.3.1.4 Buffer Control Logic

The buffer control logic is comprised of random access memory (RAM) and its supporting logic. For the purposes of this description the BTP cache RAM will be referred to as RAM.

RAM Access Contention

The access to the RAM must be controlled and prioritized to insure the prevention of read/write overruns and refresh delays. The peripheral writing or reading the RAM has the highest priority due to a non-interlocked data transfer scheme. The five modes to request access to RAM are as follows:

Tape write to RAM - priority 1

Tape read from RAM - priority 1

Refresh request - priority 2

IOM write to RAM - priority 3

IOM read from RAM - priority 3

When a request is received by RAM it transmits an acknowledge to the address counter and comparator, read/write save address register, memory timing, and the requesting port.

RAM Timing

The proper timing requirements for the RAM are provided by the memory timing generator. The clock signal (H2CLK) stages the control signals from the RAM access contention logic. LMEMCYCLE generates row address select (RAS) and column address select (CAS) to RAM. RAS occurs during any type of memory access. CAS occurs during any normal read or write access and is prevented by LREFENA during a refresh cycle. LWRTENA generates write enable (WE) during any input to the RAM.

RAM "Save Address Register" Timing

Space in the RAM is allocated dynamically allowing high utilization of the RAM to form a data buffer.

The BTP is capable of recovering from tape read and tape write errors that occur in the peripheral. To recover from a tape read error, the BTP re-loads the start address of the tape record in RAM and starts the read operation over again. To recover from a tape write error, the BTP goes back to the beginning of the tape block in RAM to fetch the data.

Write RAM Address Counter

The write RAM address counter provides sequential access to the RAM during a write operation. The counter is incremented upon the receipt of a write acknowledge from the RAM. The counter is cleared during a system reset or microprogram control (pulse order LFLUSH).

The counter may also be loaded with a 16-bit address from an input register. This register contains the start address of a tape record that is read into RAM. This is the write save address register. The register allows reloading of the write counter in the event of a RAM write error occuring from a tape read error.

There is no way to verify the data written by the IOM to RAM. The parity is generated at the time the data is written and cannot be checked until it is read later.

Read RAM Address Counter

The read RAM address counter provides sequential access to the RAM during a read operation. The counter is incremented upon the receipt of a read acknowledge from the RAM. The counter is cleared during a system reset or microprogram control (pulse order LFLUSH).

The counter may also be loaded with a 16-bit address from an input register. This register contains the start address of a tape record currently being read out of RAM. This is the read save address register. It is required to allow reloading of the first address of the record currently being read out of RAM to recover from tape write errors and RAM read errors.

RAM Write/Read Address Comparator

Comparing write/read address for error is accomplished by the comparator logic. The source of the write address bits presented to the comparator is directly from the output of the write counter. The source of the read address bits presented to the comparator is from the output of the read save address register. The comparator compares the present read address to the write address to prevent writing over a record currently being read out of RAM.

Comparator Control Logic

The comparator control logic examines the HFULL/E signal during a write or read access to RAM. If address equality occurred during a read then the RAM is considered empty, if it occured during a write then the RAM is considered full.

During a full condition HOLD WRITE-FF is set to prevent any further write requests to RAM. A read will cause an address inequality condition and reset HOLD WRITE-FF.

During an empty condition HOLD READ-FF is set to prevent any further read requests to RAM. A write will cause an address inequality condition and reset HOLD READ-FF.

RAM Refresh Timing, Address, and Polling Logic

The dynamic RAM must be refreshed within four milliseconds, the ROW addresses are comprised of eight bits and there are 256 ROWs to be addressed. Therefore, the access rate per ROW is 15.625 microseconds.

The circuit polls the access logic to perform a refresh cycle every 14.7 microseconds to allow for the loss of poll during a tape access.

RAM Address Multiplexer

There are two levels of multiplexing; the first level is a 3 to 1 mux which selects the write, read, or refresh address counters, and the second level is a 2 to 1 mux which multiplexes the 16-bit output of the first level. This results in an 8-bit address path.

IOM to RAM 4:1 Data Mux and Control Logic

This logic provides the IOM with a data path into the RAM. The data path is a 4 to 1 multiplexer used to reduce firmware overhead when writing into RAM. RAM is loaded from the IOM A and B registers with 1 to 4 bytes, the selection of which byte is first is accomplished with two level orders.

When the IOM writes 4 bytes into RAM it must select the "byte 0" as its starting position, check the IOMINREQ signal to verify the RAM input multiplexer is empty and then issue the pulse order LOUTPUT while holding the A and B registers for that instruction.

When the IOM is writing the last byte of data it must select the "byte 3" starting position, and align the B register to output to that field. Before the LOUTPUT is issued, the LAST BYTE-FF must be set. When the data is written to RAM, the end-of-record flag is set with the last byte of data.

Tape to RAM - Data and Control Logic

This logic accepts a byte of data from the tape interface during a tape read operation, holds it in the tape input register, and polls to write it in RAM. To indicate the last data received from tape, the logic uses the DBY-TE pulse to set the RAM end-of-record flip-flop (LWEOR) causing the data to be written into two successive locations of RAM. However, when the IOM reads the data and detects the flag, it realizes the end-of-record and drops the duplicate data.

During a tape read ahead operation, where the IOM commands reading more tape than requested by software, it is posible for the buffer to become full. If this occurs, the comparator logic prevents an overwrite of the RAM by the tape, but it cannot stop the tape from sending data and data strobes. If more than one strobe is received before the prior one is serviced an input overrun will be set. When the overrun is detected by the IOM it will disqualify the partial record read, adjust the record queue, and reposition the tape.

Tape Read/RAM Write Parity Check and Generate

To maintain data integrity, a parity check and generate circuit has been provided at the input to the RAM.

When the IOM is writing data to RAM the logic generates a parity bit on the eight data bits and the end-of-record flag bit. When the tape writes data to RAM two events occur: First, the data read from the tape has parity associated with it and is checked against the data. Second, based on the end-of-record flag bit, a new parity bit is generated and sent to RAM. If the data read has a parity error it will be detected by the IOM, and the record will be disqualified.

RAM Array

The RAM array is comprised of ten 64k bit 120 nanosecond dynamic MOS RAMs. The 10 bits are arranged as: eight data bits, one parity bit, and one flag bit.

RAM to IOM Demultiplexer

This circuit routes eight bits of data onto a 16-bit data path to the IOM from the RAM, under complete control of the IOM. The data, accessed one byte at a time, is demultiplexed and routed to the IOM regardless of whether the data was placed in RAM during a read forward or read backward from tape. The request to access data from RAM is performed by two pulse orders (L1BREQ and L2BREQ). L1BREQ and L2BREQ requests one and two bytes of data respectively.

If the logic detects a RAM parity error during the read, it will reset the requesting logic and generate LPERR. This will cause a microinterrupt and the firmware will attempt to recover the data from RAM, or backup the tape and attempt to read the data into RAM again.

If the logic detects the end-of-record flag, it resets the requesting logic and notifies the firmware that there is no more data for this record. The data associated with the flag is invalid and considered overhead.

Tape Write/RAM Read Parity Generate and Check

This logic checks the parity of the RAM data, if the parity is wrong, during a tape read or write, an interrupt will be generated. The logic also regenerates the correct parity to tape after exclusive ORing the parity bit with the end-of-record flag bit.

RAM to Tape - Data and Control Logic

During a write to tape from RAM the tape drive sends the IOM a strobe (WSTR). WSTR is synchronized with the system clock to generate a signal to send one byte of information to tape.

However, the first byte is not read from RAM via WSTR, it is read using the data busy (LDBY) signal. The LDBY signal indicates that the tape is in motion and up to speed. In PE mode the tape sends the WSTR to the IOM approximately 41 byte periods after DB occurs because the preamble is 41 bytes in length. When the end-of-record flag from RAM is detected, it causes a control bit to be sent to the tape interface with the data to notify the drive to stop writing data.

End of Tape Latching Logic

The end-of-tape latch maintains the end-of-tape status once the drive positions the tape beyond the EOT marker. The EOT latch is reset when the tape is positioned before the EOT marker. This latch is required because some tape drive units only transmit EOT at the time it occurs.

4.3.1.5 SelBUS Signals

The SelBUS is a bidirectional, synchronous-time-division, multiplexed bus. The completely passive SelBUS is part of the chassis backplane, it allows the transmission of commands from the CPU to the BTP, and data between main memory and the BTP.

The SelBUS consists of 184 parallel lines: 32 data, 24 address, 23 SelBUS priority, 39 control and tag lines. Other lines on the SelBUS include power, ground and spares for possible future expansion. Refer to the CPU technical manual for a detailed description of these lines and Appendix A at the rear of this manual for the pin assignment of each signal.

4.3.1.6 Tape Input/Output Signals

Input/output (I/O) signals to and from the formatted tape drive travel through connectors J1 and J2 of the IOX circuit card which is connected to P1A and P1C of the SelBUS, respectively.

INPUTS TO THE BTP

DATA STROBES

The formatted tape drive generates a write strobe (WSTR) to the BTP after a write command is issued to the tape drive. The leading edge of WSTR notifies the BTP that data is about to be transferred. Data is actually accepted by the formatter on the trailing edge of WSTR. During a read operation when the formatter is sending data to the BTP, the formatter generates a read strobe (RSTR). The leading edge of RSTR notifies the BTP that data is on the read data bus and the BTP accepts the data on the trailing edge of RSTR.

READ DATA

Eight read data signals (R0 through R7) and one read parity signal (RP) are sent to the BTP during read operations. The data is accepted on the trailing edge of RSTR as mentioned under data strobes.

TRANSPORT STATUS

There are six signals that indicate the status of the selected tape drive and are defined as follows:

1. Ready (RDY) is true when the tape drive is ready to accept a command, for example, when a rewind command has completed, or no subsequent rewind command is in progress and the tape drive is online.

2. Online (ONL) is true when the online switch of the tape drive is set to the active position.

3. Rewind (RWD) is true when the transport is currently rewinding.

4. File protected (FPT) is true when the write enable ring is absent from the mounted supply tape reel. No write operations are permitted.

5. Load point (LDP) is true when the reflective BOT marker on the tape media is positioned under the BOT sensor.

6. End-of-tape (EOT) is true when reflective EOT marker on the tape media is positioned under the EOT sensor. Data may exist up to ten feet beyond the EOT marker.

CONFIGURATION SIGNALS

These signals indicate the configuration of the selected transport as follows:

1. NRZI is true when the tape drive is selected to operate in the NRZI mode of recording. The 800 bits per inch (bpi) density is supported by the tape unit when in NRZI. When false, this signal implies phase-encoded (PE) recording mode which records data at 1600 bpi.

2. Single (SGL) refers to the type of head used, for example, single or dual stack. The tape drives supported by the BTP do not use this signal.

3. Speed indicates the higher speed capability is enabled in a dual speed tape drive.

FORMATTER BUSY

Formatter busy (FBY) goes active when a command is issued to the formatter and remains active until tape motion stops after completion of the command.

DATA BUSY

Data busy (DBY) becomes true when the tape drive has achieved proper speed and passed the inter record gap. It remains true untill the end of the record is reached. A subsequent command of the same mode and direction may be issued after the trailing edge of DBY in order to maintain streaming.

CHECK CHARACTER GATE/IDENTIFICATION BURST (CCG-ID)

In NRZI recording mode this signal is used to indicate that CRCC or LRCC, at the end of a record, is being sent to the BTP. The BTP internally gates out read strobes with CCG-ID to avoid placing the CRCC or LRCC into the cache. In PE recording mode, CCG-ID indicates that an identification burst has been read from or written to tape. The ID BURST is located at the beginning of-tape (BOT) position.

HARD ERROR

Hard error (HER) is true when the formatted tape drive detects an error condition that it cannot correct. It is tested by the BTP at the end of the DBY signal.

CORRECTED ERROR

Corrected error (CER) is valid in the PE mode, and is used to indicate that a single track dropout occured. The BTP re-writes the record if detected during a write operation. No action is taken if the error is detected during a read operation.

FILE MARK

File mark (FMK) indicates that the formatted tape drive has detected a file mark on tape. This occurs for read operations and write filemark operations.

OUTPUTS FROM THE BTP

ADDRESS SELECTION

Three signals are used to select formatted tape drives and slave units. This allows a maximum of eight tape drives, two masters and six slaves. The selection of one of two formatted master drives is accomplished with formatter address (FAD). The selection of the tape drive is accomplished with transport address zero (TAD0) and transport address one (TAD1).

COMMAND SIGNALS

The formatter commands implemented by the BTP are sent to the formatter via a command strobe (GO). This strobe is one microsecond wide, and the command is latched in the formatter on the trailing edge of go. The signals used to encode the formatter commands are as follows:

1. Reverse/forward (REV) specifies forward or reverse tape motion.

2. Write/read (WRT) selects the mode of operation.

3. Write file mark (WFM) when used with WRT writes a file mark. When WRT is false it specifies a file mark search.

4. Edit is used to modify the read reverse stop delay to allow better head positioning when editing tapes. When writing, the write current is gradually turned off to prevent disturbing the adjacent record. This mode is not supported by the BTP.

5. Erase is used with WRT and WFM to generate a fixed length gap of approximately four inches. When used during searches it inhibits the formatted tape drive from transmitting read strobes.

6. Read threshold level one (THR1) is not used by the tape drives that use dual stack heads.

7. Read threshold level two (THR2) is used to lower the threshold in the read circuits to recover low amplitude data. This signal is used during read error recovery sequences performed by the BTP.

8. Density select (DEN) is implemented in dual format formatted tape drives to select NRZI or PE mode. When true the NRZI mode is selected. Streaming tape drives use this to select the streaming mode.

MISCELLANEOUS CONTROL SIGNALS

The following signals are issued to the formatted tape drive as a pulse with a duration of one microsecond. These types of commands do not cause the formatter to become busy, rather, these are routed to the selected transport.

1. Rewind (REW) causes the selected tape drive to rewind to load point.

2. Off-line (OFL) causes the selected tape drive to be placed in the off-line mode. When used with the REW signal, the tape drive will unload when the load point is reached. Not all tape drives support this feature.

3. Formatter enable (FEN) when false causes the formatted tape drive to reset. This signal is not gated via any address signals, therefore when issued, all formatted tape drives will reset.

4. Load-online (LOL) causes tape to be tensioned once power is applied to the drive. A second pulse, delayed at least one microsecond, causes the selected drive into the online mode. This signal is not supported by the BTP.

WRITE DATA SIGNALS

There are eight write signals (W0 through W7) and one write parity signal (WP) that are sent to the tape drive during write operations. The data is accepted on the trailing edge of WSTR the same way as inputs to the BTP.

The BTP notifies the formatted tape drive to stop writing data via the last word (LWD) signal. This signal is sent to the drive with the last byte of data transmitted causing the formatter to stop the write operation.

4.3.2 Firmware Description

4.3.2.1 Microinstruction Definitions

The 32-bit microword used by the BTP is divided into a variety of fields for different purposes. These fields are decoded by hardware in the BTP and executed using the test and order structures, the 16-bit arithmetic logic unit, and the A and B register groups. The BTP microword is patterned after the basic IOM with a few differences. Primarily, the order structure contains a fifth order group which operates exclusive of the other four. Some changes in the test and order signal assignments to the SelBUS and B register have occured. As a result of these changes a new microdefinition file has been created. It is used to allow interpretation of the source file when assembled. Refer to the IOM technical manual for a complete description of the microword format.

4.3.2.2 Test and Order Structures

The order structure is comprised of five groups of 3:8 demultiplexers. Of these, two contain latched outputs (level orders), and the remaining three are non-latched (pulse orders) and are active for only one instruction cycle. The primary function of the order structure is to allow the microprogram internal and external hardware control. Pulse orders are typically used to clock latches and registers, where a level order is typically used to steer multiplexers, or generate external control signals greater than one clock cycle. This structure is arranged to allow simultaneous control of two pulse order groups and two level order groups. One pulse order group operates exclusive of the others, and therefore has had low usage functions assigned to it. Refer to Table 4-4 for order groups and order assignments.

The test structure or matrix is comprised of eight 8:1 multiplexers. This matrix allows the microprogram to respond to the various internal hardware status signals that are connected to the RAM cache logic, ALU status register, B register group bits 00 through 15, SelBUS interface flip-flops, and tape status receivers. This matrix can test any two signals within the same 32-bit field for the same logic polarity if necessary. All external test signals are first synchronized with the system clock before being presented to the test matrix. Refer to Table 4-5 for the test group and their assignments.

Table 4-4
Pulse and Level Orders

Pulse Orders	Group	Mnemonic	Description
0	0	-	Spare
1	0	-	Spare
2	0	-	Spare
3	0	-	Spare
4	0	LCLR-STAT	Clear tape status latches
5	0	LLDADDR	Load tape address register
6	0	LCLR-RD	Clear RAM read logic
7	0	LCLR-TER	Clear Tape read & parity error logic
0	4	LMICROACK	Clear SelBUS interface
1	4	LMICROTRANS	Grab SelBUS interface logic
2	4	LCLR-HIO	Clear halt I/O flip-flop
3	4	LMICRODATALD	Strobe SelBUS data register
4	4	LMICRODESTLD	Strobe SelBUS address register
5	4	LMICROREADY	Ready response to CPU
6	4	LLSTBYT	Last byte to write RAM
7	4	LBRANCH-SEL	Indirect branch control
0	8	LCLRINT	Clear SelBUS serial interrupt request
1	8	LREQINT	Request SelBUS serial interrupt
2	8	L2BREQ	Two byte read request from RAM
3	8	L1BREQ	One byte read request from RAM
4	8	LRESTOREWRT	Restore RAM write address
5	8	LRESTORERD	Restore RAM read address
6	8	LOUTPUT	Load RAM input multiplexer
7	8	LFLUSH	Clear RAM address counters

Level Orders	Group	Mnemonic	Description
0	1	LENDBY	Enable data busy edge strobes
1	1	-	Spare
2	1	LACTIVE	SelBUS serial interrupt request gate
3	1	LMICRORETRY	SelBUS retry response
4	1	LMICROBUSY	SelBUS busy response
5	1	HREW	Rewind control signal
6	1	LB2-3	RAM input mux select bytes two or three
7	1	HLOL	Tape load-on-line control signal
0	2	HOFL	Tape offline control signal
1	2	HFEN	Tape formatter enable
2	2	HGO	Tape command out strobe
3	2	HFIFO	RAM FAM FIFO mode control
4	2	LDIAG	Diagnostic LED control signal
5	2	LFWD	RAM read direction forward/reverse
6	2	LB0-1	RAM input mux select bytes zero or one
7	2	LWRTTAP	RAM write tape control signal

Table 4-5 (Sheet 1 of 2)
Test Group A and B

Test Group A Address	Mnemonic	Description
20	LBIN08	B register output bit 08
21	LBIN09	B register output bit 09
22	LBIN10	B register output bit 10
23	LBIN11	B register output bit 11
24	LBIN12	B register output bit 12
25	LBIN13	B register output bit 13
26	LBIN14	B register output bit 14
27	LBIN15	B register output bit 15
28	LAMSB-FF	ALU most significant bit flip-flop
29	LMEMDATAHERE	Memory data here flip-flop
2A	LRDIN	LRD input from Sel BUS
2B	LCNT0IN	Control 0 input from SelBUS
2C	LCNT1IN	Control 1 input from SelBUS
2D	HCPUREQST	CPU requesting decoded flip-flop
2E	HDATAINT	Micro level interrupt control
2F	LERRORIN	Error input from SelBUS
30	LEND	End-of-record flag from RAM
31	HEMPTY	RAM is empty
32	HIOMOUTREQ	IOM read RAM port is polling to RAM
33	LOUTUNDERRUN	Output to tape, data lost
34	HLSB	LSB register contains data
35	HMSB	MSB register contains data
36	LPERR	RAM output data contains parity error
37	LWSTR-TST	Tape write strobe test
38	HFMK-TST	Tape filemark detected test
39	LFPT-TST	Tape file-protected test
3A	HHER-TST	Tape hard error test
3B	LONL-TST	Tape on-line test
3C	LSGL-TST	Single gap (not used on most drives)
3D	LSPEED-TST	Tape drive speed indicator
3E	LWEOR	Write end-of-record flip-flop
3F	HWRTINT	Write mode interrupt

Table 4-5 (Sheet 2 of 2)
Test Group A and B

Test Group B Address	Mnemonic	Description
40	LBIN00	B register output bit 00
41	LBIN01	B register output bit 01
42	LBIN02	B register output bit 02
43	LBIN03	B register output bit 03
44	LBIN04	B register output bit 04
45	LBIN05	B register output bit 05
46	LBIN06	B register output bit 06
47	LBIN07	B register output bit 07
48	LAEQB-FF	ALU zero status flip-flop
49	LNONPRESMEM	Non present memory for SelBUS memory
4A	LHALTIO	SelBUS halt I/O flip-flop (reset channel)
4B	LMICROINPUT	SelBUS multiplexer select flip-flop
4C	HRFA07	Refresh address 07 (MSB)
4D	LSYNC	SelBUS end of interrupt poll synched
4E	+V(7)	Unconditional branch test
4F	LCPUDATAHERE	CPU grabbed SelBUS interface flip-flop
50	HCARRY-FF	ALU carry status flip-flop
51	HFULL	RAM is full status
52	HIOMINREQ	IOM write RAM port is polling to RAM
53	HINOVRRUN	Input from tape, data lost
54	LTAPERR	Parity on tape read data bus to IOM
55	LDBY-TST	Tape data busy test
56	HCCG-ID-TST	Tape CCG or ID burst test
57	LRSTR-TST	Tape read strobe test
58	LEOT-TST	Tape end-of-tape latch test
59	LRWD-TST	Tape rewinding test
5A	HCER-TST	Tape corrected error test
5B	LRDY-TST	Tape ready test
5C	LNRZI-TST	Tape NRZI or PE test
5D	LLDP-TST	Tape load point test
5E	LFBY-TST	Tape formatter busy test
5	HRDINT	Read mode interrupt

4.3.2.3 Register Definitions

The firmware defines 32 separate addressable registers in the A and B registers. Symbolic definition of the registers is done to aid in the programming of the microcode. Refer to Figure 4-2 for a symbolic representation of the registers and their bit assignments, and Table 4-6 for register definitions. A brief description of each register is as follows:

IRTN — Interrupt return register. This register can be soft-loaded by the firmware to allow controlled return from servicing a micro-interrupt condition, or it will be loaded with the current micro-PC via the hardware interrupt logic when the micro-level interrupts are enabled.

RTN1 — Level 1 linking register. Linking to subroutines which contain device controlled delays require this register. CPU intervention is allowed while I/O is in process but limited to first level linking.

RTN2 — Level 2 linking register. This is used to call subroutines which do not contain any device controlled delays. It is also used by the firmware during CPU proccessing as a first level linking register.

ALLOC — Memory allocation register pair. As specified by F-class I/O, the channel is allowed space in main memory for status posting and auxiliary storage. The address of this is passed during the INCH command and loaded into the ALLOC register pair. The INCH is the only way to load the register.

ID — Identification register. During the load RAM protocol with the CPU, the channel receives its physical address and loads it into this register. This data is then used during memory read transfers.

ILVL — Interrupt level. During the load RAM protocol a seven bit inverted serial SelBUS interrupt level is received and loaded into this register. This level is used by hardware to generate a serial poll on the SelBUS.

CTRL — Control register. This register contains tape interface level command codes, current addressed tape unit, and error recovery flags.

BUS — SelBUS data holding register pair. During CPU communication at the RSTX/ICT level, function codes and parameters are loaded into this register pair for testing.

WK3 — Working register pair 3. This is used as a working register during CPU processing. It is also used as a SelBUS address holding register to temporarily contain the interrupt level and subaddress sent by the CPU.

OP — IOCD or opcode-flag register. OP contains the opcode and flags from the current IOCD in progress.

SBCH — Subchannel address register. This is loaded with the desired subchannel address as specified by the RSTX processing.

MAR — Memory address register pair. This contains the address from the IOCD in progress. When data is transfered to or from main memory this register pair is maintained by the appropriate transfer routines.

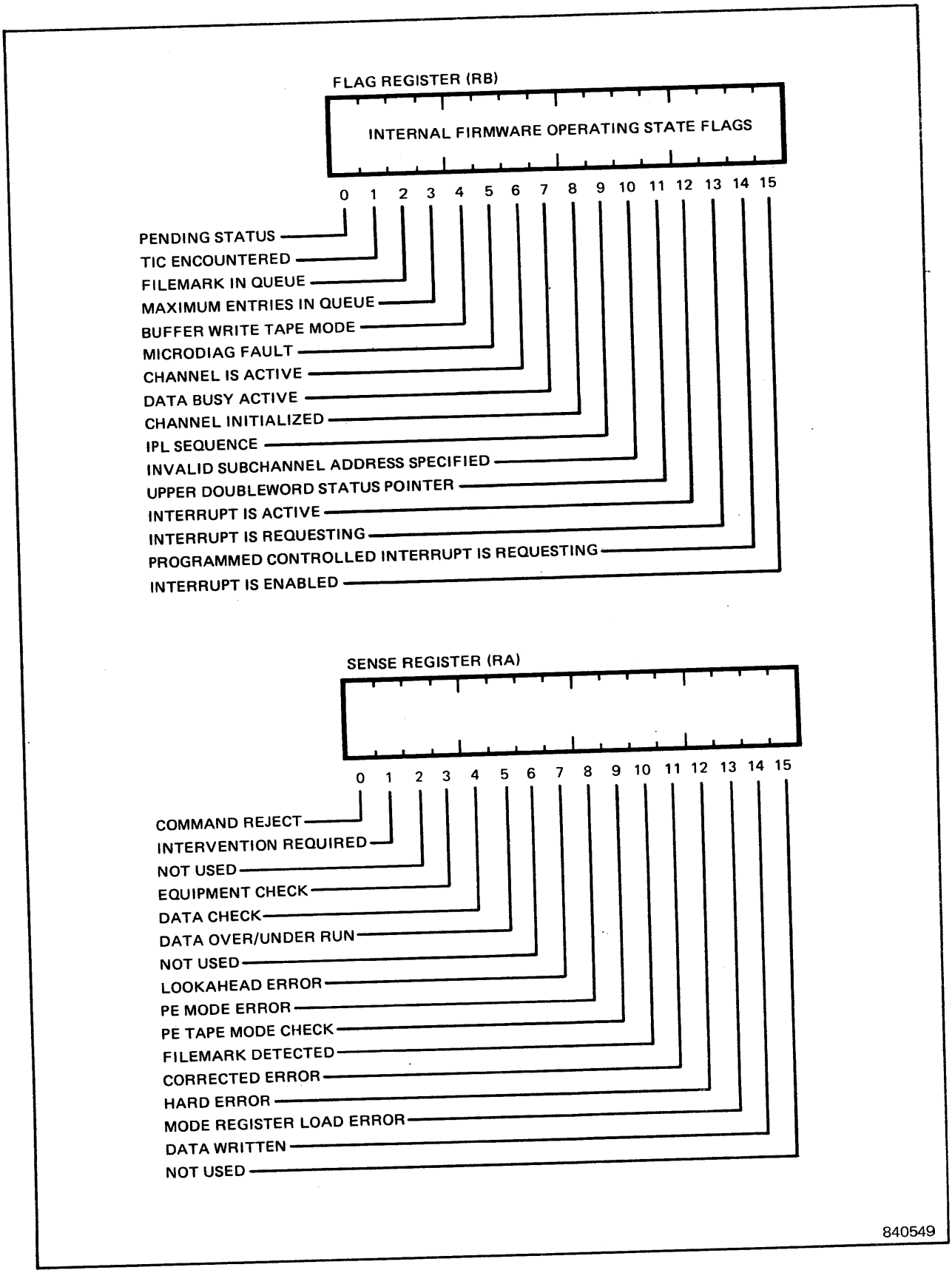

Figure 4-2. Register Bit Assignments (Sheet 1 of 4)

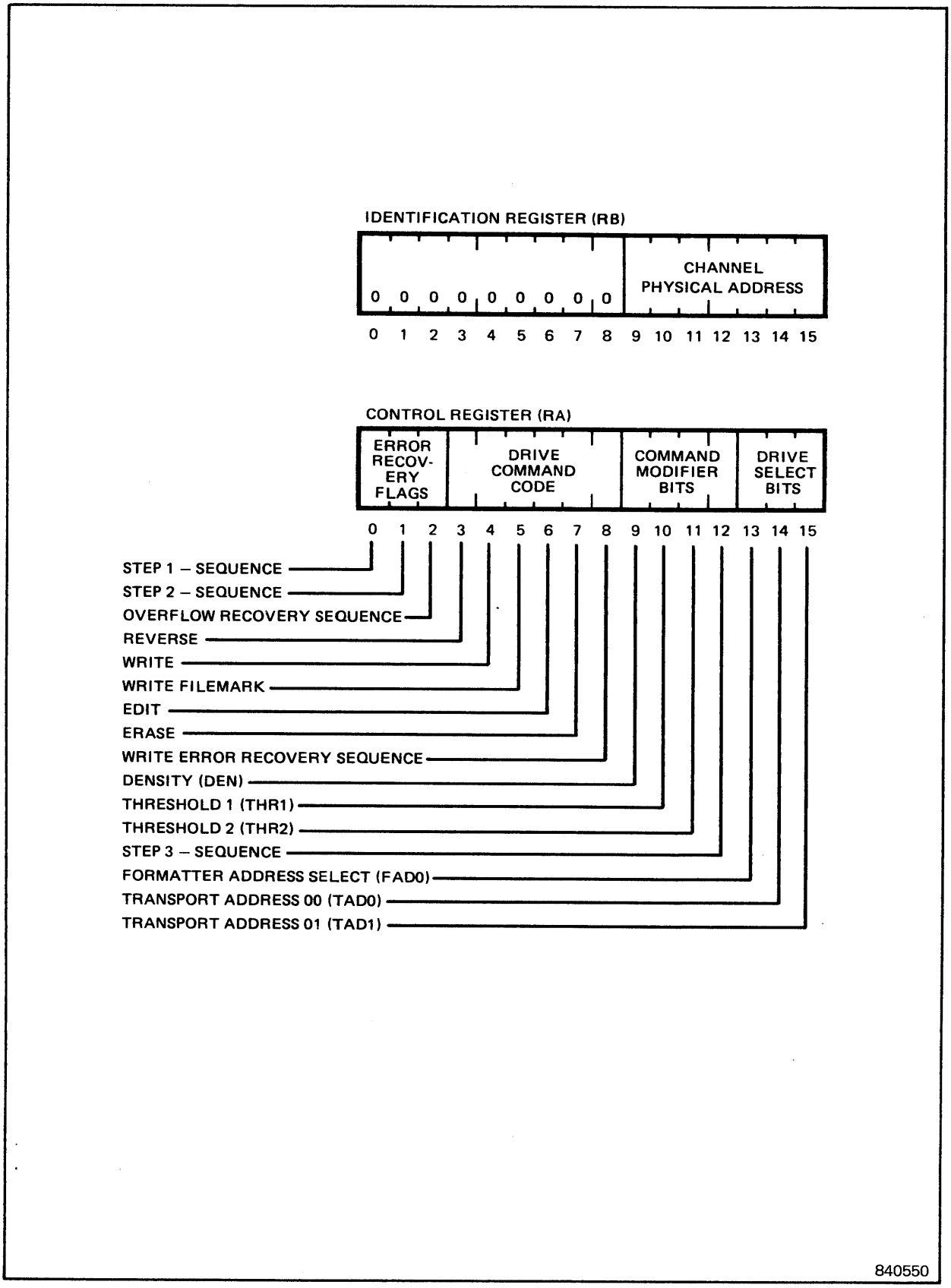

Figure 4-2. Register Bit Assignments (Sheet 2 of 4)

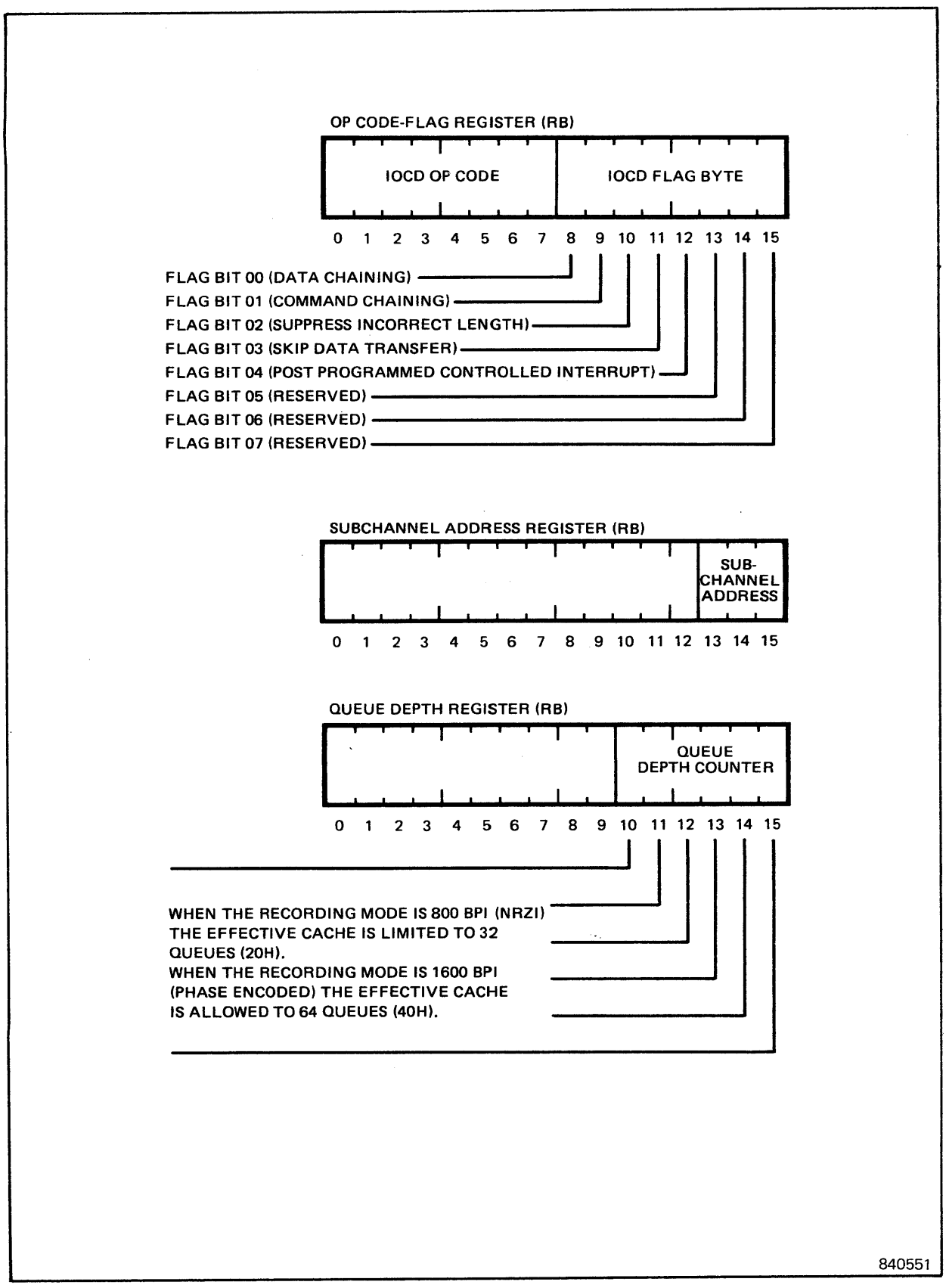

Figure 4-2. Register Bit Assignments (Sheet 3 of 4)

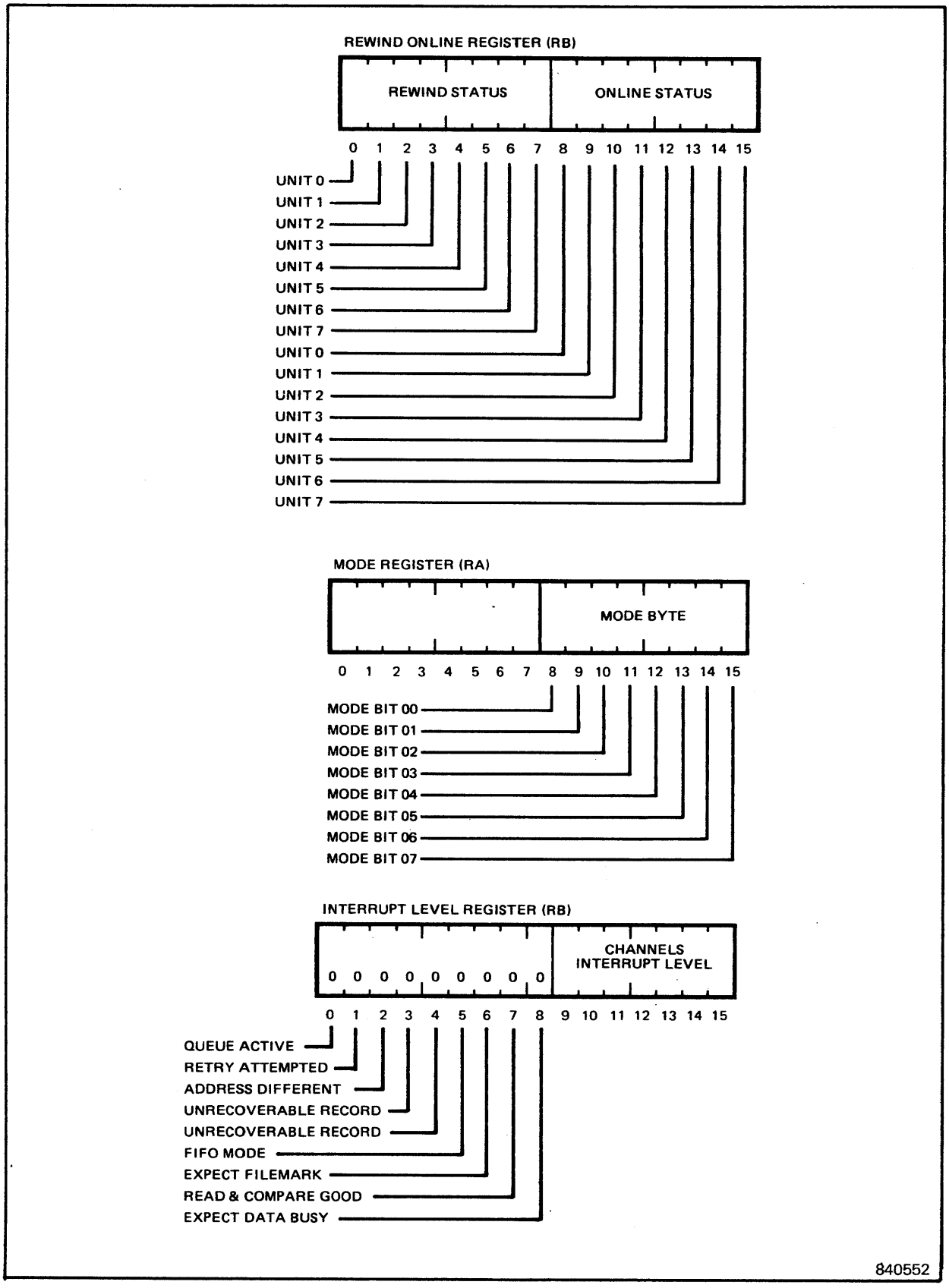

Figure 4-2. Register Bit Assignments (Sheet 4 of 4)

Table 4-6
Register Definitions

Mnemonic	Register Group/Address		Processing Type
IRTN	RA	0	I/O - CPU
FLG	RB	0	I/O - CPU
SNS	RA	1	I/O -
ID	RB	1	I/O - CPU
CTRL	RA	2	I/O -
OP	RB	2	I/O -
RTN1	RA	3	I/O - CPU
SBCH	RB	3	- CPU
RTN2	RA	4	I/O - CPU
Q	RB	4	I/O -
ALLOC	RA	5	I/O - CPU
ALLOC	RB	5	I/O - CPU
MAR	RA	6	I/O -
MAR	RB	6	I/O -
IOCD	RA	7	I/O -
IOCD	RB	7	I/O -
BCT	RA	8	I/O -
RW.ON	RB	8	I/O - CPU
SHFT	RA	9	I/O - CPU
LIT	RB	9	I/O - CPU
MODE	RA	A	I/O -
ILVL	RB	A	I/O - CPU
BUS	RA	B	- CPU
BUS	RB	B	- CPU
DATA	RA	C	I/O -
DATA	RB	C	I/O -
WK1	RA	D	I/O -
WK1	RB	D	I/O -
WK2	RA	E	- CPU
WK2	RB	E	I/O -
WK3	RA	F	- CPU
WK3	RB	F	- CPU

BCT — Byte count register. This is loaded with the byte count specified in the current IOCD. This register is decremented during transfer routines to reflect the amount of data transferred.

IOCD — I/O command doubleword address register. This register contains the address of the current IOCD in process. During chaining the address is increased by eight to allow fetching the next IOCD contents.

DATA — Data register pair. This is used by I/O routines as a temporary holding register between the cache RAM and the SelBUS staging register.

MODE — Mode register. This is loaded via the SETMODE command from an IOCD. One byte of operating mode bits can be sent to the channel to modify its operating characteristics.

Q — Queue depth register. This is maintained by the I/O routines and the cache control routines. It is used to indicate the number of records and filemarks queued for write operations or prefetched during read ahead operations.

SNS — Sense register. Specific drive status and operating results are accumulated into this register. The contents of which are read via an IOCD level SENSE command.

SHFT — Shift holding register. This is used by shift subroutines to shift data.

LIT — Literal holding register. This is used throughout firmware as a destination for a microinstruction load literal operation (similar to a load immediate).

WK1 — Working register pair 1. This working register is used only by I/O main processing routines. CPU processing has restricted access.

WK2 — Working register pair 2. The A register is used only by the CPU main processing routines. The B register is used only by I/O main processing routines.

RW.ON — Rewind online register. The most significant byte contains unitary indication of each possible drives rewinding state. The least significant byte contains the corresponding online states.

FLG — Flag register. Internal firmware operating status flags are required to note the many concurrent operations.

4.3.3 BTP Functional Organization

4.3.3.1 Functional Description

The BTP is a programmed I/O channel controller. It requires a minimum of one formatted tape transport. However, it can support a maximum of eight drives.

The system functions as a single programmed channel capable of controlling one tape drive at any given time. Parallel operations are restricted to parallel tape rewind operations. Functionally, the formatter combination is considered to be an integrated channel controller that operates with selector channel characteristics. The magnetic tape units are considered devices. The BTP formatter combination is called the system.

The system is designed to accommodate tape transports that operate at speeds of up to 125 inches per second, with a recording density of 1600 characters per inch at data rates of up to 200,000 characters per second.

The channel-drive combination is fully compatible with IBM nine-track tapes. The nine-track compatibility includes both NRZI and PE recording modes at 800 and 1600 characters per inch, respectively.

The command set is sufficiently rich to permit the full utilization of the programmed I/O concept. When tapes contain both file and record labels, it is possible to initiate lengthy tape searches with a single-start I/O instruction. These searches are subsequently conducted without CPU support or intervention. When the search is complete the required data transfer is executed, the I/O program is terminated, and only then is the CPU interrupted. The termination of data flow causes the BTP to generate an interrupt, which the CPU recognizes. The CPU then initiates a query to the BTP, resulting in a status transfer to the CPU, which indicates either a successful data transfer or any errors that were encountered.

The BTP is the basic hardware structure for the BTP system and consists of four functional parts:

1. A SelBUS interface, which provides the communications path between the BTP and the CPU or the BTP and main memory.

2. A microprocessor, which has a control memory that contains the microprogram (firmware) for controlling the SelBUS interface, microprocessor, cache control, and interface logic. Together, the SelBUS interface and the microprocessor comprise the IOM (input/output BTP microprogrammable processor).

3. The buffer control logic which consists of 64K bytes of dynamic RAM and its timing circuits, parity check/generate on the RAM paths, and multipexed data paths to the micro-processor.

4. Device interface logic which contains the drivers and receivers to communicate to the formatter in the tape transport, status registers and strobe synchronization logic, and parity check/generate logic on the tape data paths.

Although the microprogram for the BTP installs in the control memory of the microprocessor, it is considered part of the device-dependent interface since it provides the control for the device.

The SelBUS interface provides logic circuits, staging registers, and drivers to allow the microprogrammable processor (MP) to communicate with the CPU and memory over the SelBUS. Jumpers, which may be altered to establish individual systems requirements, determine the SelBUS priority level and the IOM address.

The MP in the BTP is a CPU and performs logical, control, and arithmetic functions. The MP contains a read-only memory (ROM) control unit, an arithmetic logic unit (ALU), two 16-bit by 16-word register files, and order structure logic used in the generation of external control signals.

The device-dependent logic consists of registers, latches, buffers, drivers, and receivers that interconnect the BTP to the formatted tape drive. The device-dependent logic performs the following functions:

1. Transmits and receives an eight-bit data byte to or from the active tape drive via the formatter. The data byte is the information read from the tape or to be written onto the tape.

2. Accepts and stores device status signals indicating the status of the active tape drive unit.

3. Sends pulse and level order commands via the formatter to cause the tape drive to perform the desired operation.

4. Controls data transfers between the tape interface and the cache memory.

4.3.3.2 Main Memory Buffer

As per the F Class I/O requirements for status posting, space in main memory is allocated for two status doublewords. The BTP main memory buffer allows additional storage without adding hardware. The storage is required for these main functions: queue work space, error retry counter, and device error log table. The queue work space contains four words, a command type list of 64-bits occupies two words, a set of physical and logical pointers occupies one word. One word is used to contain the last non data chained IOCD. This word allows the BTP the ability to reprocess the IOCD list for certain types of error recovery. The error retry counter occupies one word. The left half-word is the working value and the right half-word is the constant. If the constant field is loaded with zero, during the INCH the microprogram defaults to five and loads both half-words. Any number other than zero is copied to the left half-word. The error log contains 4 words per device. These words represent accumulated write errors, accumulated read errors, a running total of the data written to tape and a running total of data read from tape. The accumulated write error entry is incremented upon detection of a write error. If a retry operation results in yet another error, it causes the increment to occur. The accumulated read error entry is incremented upon the detection of a read error. However, any errors occuring while the BTP is performing retries will not cause the increment to occur. This error log was established to provide a method of tracking errors that were corrected by the BTP and therefore never reported during the queueing operations. The BTP does not initialize the error log, rather it relies upon software initialization. Typically the log entries are initialized to zero when the system is booted or whenever software should examine the log.

4.3.4 Channel Mode and the Mode Register

Through the use of the IOCD command SETMODE the programmer is capable of modifing the operating mode of the BTP subsystem. The mode register is eight bits wide, but only three of these bits have significance. The other five are currently not used. The assigned bits (zero, one, and six) are described below.

Bit 0 is used to allow a read regardless mode when the BTP can't recover from an error automatically. It can be used in certain applications where program continuation may be more important than an unrecoverable record.

Bit 1 is used to allow the programmable selection of the tape unit density to either NRZI or PE when the drive supports controller selection.

Bit 6 is used to select GCR density on tape drives that support GCR capability.

	NRZI	PE	GCR
Bit one	0	1	X
Bit six	0	0	1

where as X = don't care (variable).

The remaining bits (2, 3, 4, 5, and 7) are not used and have no significance to the BTP.

4.3.5 I/O Program Execution

4.3.5.1 Starting I/O Program

The CPU start I/O (SIO) instruction is used to start all I/O programs. These are the three parts of the procedure:

1. Acceptance/rejection
2. IOCLA processing
3. IOCD processing and execution

4.3.5.2 Address (IOCLA) Acceptance

During the CPU-channel protocol of the SIO, the BTP channel determines whether or not it can accept the SIO and the IOCD list address. The factors are as follows:

1. Is the channel currently processing another SIO?
2. Does the channel have pending status to present?
3. Is the subaddress outside the allowable address range?

If any of the above conditions are true, the channel will reject the SIO. If condition one occurs, the channel sends a channel busy, response to the CPU, and then continues the execution of the current SIO. If condition two occurs, the channel posts status and notifies the CPU that the status has been stored. If condition three occurs, the channel sends an error response to the CPU.

Once the channel has determined that it can process the SIO, it places the IOCD list address in an internal register. The BTP then responds to the CPU with an accepted response which completes the CPU to BTP protocol for the SIO. The validity of the address is not checked untill the BTP begins to process it.

4.3.5.3 IOCLA Processing

The BTP uses the address passed to it during the SIO protocol to indicate the beginning of an I/O command list. The list may contain as few as one command doubleword, or as many as necessary to perform the desired operation.

4.3.5.4 IOCD Processing and Execution

IOCD processing occurs after the IOCLA has been processed. A delay may occur within the IOCD processing as a result of the SIO specifying a subchannel other than the previous subchannel. The changing of the selected drive will be delayed until the logical and physical pointers for the queue are equal. This means that queued write operations are completed before continuing, records that are prefetched during read operations are emptied from the queue, and the tape is repositioned to its logical position. Once these criteria have been met, the IOCD processing continues as follows:

1. The IOCD address is verified for word boundries.

2. The IOCD is fetched in two successive memory read operations. It is then passed to, and stored in various registers to support the fields of the IOCD.

3. The command field is tested for a TIC, if it is found, the I/O program is immediately terminated with channel program check (CPC) status being posted. The first IOCD cannot contain a TIC. Also, this is true if a TIC points to an IOCLA with a TIC as its first command.

4. The rewind state of the selected drive is tested, if it is found to be in the rewind state, the I/O program is terminated with device busy (DB) status.

5. The command is tested in a command decode routine which dispatches further processing to the specified command processor.

The IOCD flag bits 05, 06, and 07 must be set to zero. The other flag bits 00 through 04 are significant and are described below.

Bit	Description
00	Data chain (DC)
01	Command chain (CC)
02	Suppress incorrect length (SIL) indicator
03	Skip (SKIP) read data
04	Post program controlled interrupt (PPCI)

The requirements for IOCD validity apply to all IOCDs regardless of the command specified. The requirements are as follows:

1. IOCD word two, bits 05 through 15 must be zero.

2. The byte count must be non-zero.

3. TIC branch addresses must be a 24-bit address that addresses word boundries.

4.3.5.5 Command Execution

The contents of the IOCD command field is presented to an opcode decode routine where it is dispatched to the appropriate opcode processor. If the opcode cannot be decoded, a SIO will terminate with channel program check status and the sense register will be loaded with the command reject sense bit 0. When the selected command completes the operation it will exit to one of the following final processing areas:

REQ.DONE - BR, BF, ERASE, RDB.
CHK.CMD.CHAIN.2 - REW, REWU, INCH, SETM, SENSE, NOP
CHK.CMD.CHAIN. - WFM, WRT, RDC, RD, AR, AF

These areas gather the final status, divide it into logical or physical status and checks it for the type of command performed. The final processing determines the type of status to be generated, however, if command chaining is specified, command chaining will occur.

4.3.5.6 Data Chaining

The data chaining (DC) operation allows the programmer to write a record to tape from non-contiguous memory locations or read a record from tape into non-contiguous memory. This satisfies the requirements of mapped memory operating system environments. At the end of a data type command, the data chaining flag is tested, if set, the firmware will fetch the next sequential IOCD from memory. The command is ignored from the new IOCD, and the old command is retained.

Prior to processing the new IOCD, the PPCI flag in the old IOCD is tested, if set, the channel will request an interrupt indicating the completion of the last IOCD. In either case the control is passed back to the original command routine where the processing will continue to transfer the amount of data specified by the new buffer address and byte count.

During data chaining IOCDs may be linked sequentially, or linked via the transfer-in-channel (TIC) IOCD command allowing non-contiguous IOCD lists to be logically connected. Note that a TIC command may not link to another TIC command, otherwise the SIO will terminate with Channel Program Check status posted.

Data chaining will terminate when the data chaining flag is reset in the last IOCD. The final processing will then occur as it would for the non-data chained mode.

4.3.5.7 Command Chaining

The command chaining (CC) flag allows multiple IOCD executions with a single SIO instruction. When the chain is completed, the final processing will occur, posting status and attempting to request an interrupt to indicate completion of the SIO.

The use of command chaining with the TIC command allows the IOCD list to be non-contiguous, where the completion of one command list with a TIC command starts the channel processing of a new list. Command chaining is supported by all IOCD commands.

If an error occurs during command chaining that cannot be recovered by the channel, the chain is broken. When the status is posted, the next IOCD to be fetched will have its address stored in the status double word along with the error status, residual byte count, and the subchannel in error.

4.3.5.8 Tape Write Operation

The tape can be written with data which is separated by interrecord gaps created by the tape formatter, or with a filemark which is used to separate blocks of data. The actual filemark pattern on tape is created by the formatter with no data transfers occurring between the BTP and the formatter. The write record and write filemark commands are buffered and processed independently of the transport at speeds equal to memory rates when allowed. The only time the transport delays the high speed processing is when either the buffer is full or it has been previously operated in a read mode.

We will examine the situation where the tape is positioned at load point and there is no pending activity in the buffer. The software issues a SIO to write a record of data that is 8192 bytes in length. The channel passes firmware control to the write command processor, where initial drive and buffer tests are performed. Before the data is transferred from the system memory to the channel, the write processor links to the logical write check routine. Here the number of current entries is checked against the maximum allowed for that density (32 NRZI/64PE). If room is available, the logical queue pointer is fetched. This pointer is used to ensure that the operation flag in the command list indicates a data operation is queued. After the logical pointer is incremented, control is passed back to the write processor. Then the buffer address in the IOCD is validated. Next the transfer count is added to the error log to indicate the attempt to transfer data. Any necessary byte alignment is performed to allow full word transfer to occur between the channel and the system memory. At this time the high speed date transfer loop is entered. System environment permiting, transfer rates will reach 2.2 megabytes per second into the BTP RAM buffer. (An 8192 byte block will require about 4 milliseconds compared to 73 milliseconds on a 75 ips tape drive @ 1600 bpi.) When the transfer loop decrements the byte count to zero, control exits to the final processing code where an interrupt request is attempted and status is stored to indicate the successful completion of the operation.

Control is now passed to the idle routine where a simple algorithm determines when to initiate the physical operations queued to the tape unit. The algorithm employs a threshold of ten entries in the queue with hysteresis. Hysteresis is used to keep the RAM emptied if the tape is currently in motion when the queue level drops below 10 entries. If the software response is significantly slow and neither of the previous conditions exist, a 500 ms timer will be activated before the queue is emptied to tape. If any data/device commands other than a write or write filemark are received while there are still write entries in the buffer, then that command processor will link to an empty queue routine before processing the requested command.

4.3.5.9 Tape Read Operation

This section describes the techniques that employ the read-ahead buffer scheme (advance record, advance filemark, read, and read & compare). The other type of read operations read backward, backspace record, backspace filemark, do not use the read-ahead scheme and occur as synchronous operations. If the record did not exist in RAM, only the time of accessing the record from tape and the transfer rate of the tape transport would be added to the total completion time. The software issues a SIO to read the record of data

from the BTP system. Control is passed to the read processor where the firmware links to the read-ahead check routine if the buffer status checks indicate the buffer is currently in the read mode. The read-ahead check routine links to read the queue pointer and the queue list. This is done to check the prefetched command type that is next in the queue for filemark or data indication.

Control is then passed immediately back to the main read processor where the buffer address is validated and the initial byte alignment is checked. Bytes of data are transmitted to the system until the buffer address is word aligned. Transfers will then occur at 1.66 mb/second until the byte count is decremented to zero. At this point the logical pointer is incremented, and the queue depth register is decremented. At this time control passes to final processing where an interrupt request is attempted and the status is stored, indicating the successful completion of the operation.

Control is then passed to the idle routine where tests are made to determine if the queue is logically full. During the idle mode, if the queue has not been filled, the firmware waits for any physical tape operation to be completed, and to perform error checking on that operation. If all conditions appear normal, the idle routine will link to the read-ahead and write end of the record routine which will initiate another read operation to the tape transport. If the queue was determined to have the maximum number of entries, control would be passed to the scan units routine. Here, once formatter busy (FBY) is un-asserted, the tape transports would be polled at an interval of 500 ms to determine if any had changed their rewind/online states from those states previously recorded. If the last active drive had gone into a rewinding or offline state, the routine would clear the buffer hardware and flags. Otherwise, if any drive changes states, device and status will be posted for that drive and an interrupt request would be attempted to indicate the change of state.

4.3.5.10 Tape Search Operations

Tape search operations can be accomplished through the use of the read and compare command, along with the command chaining flag and the TIC command. Data chaining may also be used to compare specific fields within a record. The following information describes a simple record search routine that compares the full contents of a record (where all records are equal in length) to a buffer in the system memory. (Specific field search operations can be performed by expanding the initial read and compare IOCD into a data chained list with the skip and data chain flags set.) The completion of the RDC IOCD by the channel causes the channel to fetch the next sequential IOCD if the compare was unsuccessful, or to skip the next IOCD and fetch the following IOCD if the compare was successful. This technique of skipping an IOCD allows conditional IOCD execution based upon the results of the compare operation. A simple search routine can be constructed using three IOCDs in one list. This list would appear as follows:

IOCD1	RDC command CC flag	System buffer address Record byte count
IOCD2	TIC command No flags	IOCD1 address Byte count = 1
IOCD3	NOP command No flags	N.A. Byte count = 1

An SIO is issued for this list to the BTP. The BTP will then process the first IOCD. If the compare operation between the system memory and tape record were unsuccessful, the next IOCD (IOCD2) would be fetched. This would cause the BTP channel to fetch the first IOCD (IOCD1). The BTP would perform another read and compare with the next tape record. If the compare is successful, the channel would skip IOCD2 and fetch IOCD3. In this example IOCD3 (NOP command) would cause an interrupt request attempt thereby indicating the compare operation was completed. However, the interrupt alone does not indicate the successful compare. The status posted will contain a status modifier bit to indicate that the RDC operation was successful. Any other status besides status modifier, channel end and device end would indicate the failure of the compare operation.

4.3.5.11 Status Presentation and I/O Command List

Status is posted by the BTP channel whenever an I/O command list is completed. The location of where the status doubleword is stored is sent to the CPU as a DRT transfer. This DRT is sent to the CPU as a response when the interrupt request for the previously completed SIO is acknowledged by the CPU, or when a SIO, TIO, STPIO or ECI is sent to the channel. When the CPU receives the DRT from the channel, it places the contents into the sixth word of the interrupt context block. The software can then examine this word and use it to address the status doubleword. At that time, the software can determine the results of the operation and act accordingly. As part of the status doublword, the last IOCD executed will have its address incremented by eight (two memory words) and stored in the first word along with the subaddress of the device that is posting status. The software can determine from this information the last executed IOCD within a list of more than one IOCD. Contained in the second word of the status doubleword is device and channel status within the left halfword. The residual byte count of the last IOCD executed will be placed within the right halfword.

4.3.6 Interrupt Operation

The BTP's ability to request an interrupt to the CPU is controlled by four software instructions: ENABLE, DISABLE, ACTIVATE, and DEACTIVATE CHANNEL INTERRUPT. A brief description of these instructions is contained in the programming section of this manual (Chapter 3). The contention for controlling multiple interrupt requests is performed by each channel in the system that is doing the requesting. The hardware recognizes if a higher level interrupt is requesting, and it automatically repolls until its level is serviced. The BTP's firmware is unaware of the loss of the poll. The only effect is the latency of the software caused by having to service higher priority interrupts before servicing the BTP's interrupt request. Typically, when the software is capable of servicing the BTP's interrupt, it will issue an activate channel interrupt to the BTP. This causes its level and all lower priority interrupt levels to be blocked while the BTP's interrupt is serviced. When the software completes servicing the interrupt, it will issue a deactivate channel interrupt to the BTP, thereby allowing the BTP and any lower level interrupts to contend for service.

4.3.7 Error Recovery Algorithm

4.3.7.1 Write Error Recovery

The BTP will attempt to recover any write errors occurring at the tape transport by performing a backspace record command to the tape transport, positioning it at the beginning of the failed record. The BTP will then issue a fixed length erase command to the tape unit, which will erase 3.5 inches of tape. Once this is completed, the record in RAM is re-fetched and rewritten to the tape unit. Using the default retry count will result in 5 attempts to properly write the data. If the retry count is exhausted, the BTP will set the unit check status and the intervention required sense information. The potential for the error on tape to occur when the software is finished, exists, and when the software closes the device it must issue a sense to re-sync the BTP subsystem. At that time the BTP uses the sense as a vehicle to report the fatal error during a write.

4.3.7.2 Read Error Recovery

When the BTP detects a read error during pre-fetch read operations, internal flags are set, indicating an error has occurred. No attempt is made to recover the record in error until it is requested by the software. When software requests the record, the BTP will issue a backspace record command to the tape transport, positioning it at the beginning of the record that failed. The BTP will then issue a read forward with low read threshold 2 (THR2) to the transport, to recover low amplitude data from the tape unit. The sequence is repeated until the operation is completed successfully or the retry count is exhausted. Note that for each attempt the data is re-transmitted to the system memory. If the PPCI flag is used to track IOCD execution, it is suggested that the error retry count be initialized to '0001 hex and the mode register set with the read-regardless mode bit. This is recommended because the BTP maintains the IOCD list address for error recovery purposes and will re-issue the PPCI request when recovering read data errors. When the BTP is performing read ahead operations, it may cause the tape transport to encounter a partial record, which is not necessarily in the same density. It may also cause the tape transport to access tape that has not been written upon, and allow the tape to run away. These potential situtations restrict the BTP from performing error recovery on pre-fetched records. When a runaway condition occurs during pre-fetching, the BTP starts timing the runaway, and after approximately 2 feet of tape travel it resets the tape unit. It then sets internal flags to prevent any further pre-fetching. If the software requests to read that region of tape, the BTP will then allow approximately 25 feet of travel before it resets the drive.

4.3.8 Channel Commands

4.3.8.1 Initialize Channel

The initialize channel (INCH) command is required to initialize the channel from a reset state. The channel is prohibited from executing any I/O until it has been initialized. The exception to this rule is when the IPL process has been invoked. During the INCH operation, the channel performs many internal tasks. The primary function of the INCH is to provide the channel with a memory allocation address. This address is passed to the channel as part of the IOCD buffer address field and is loaded into an internal channel register. The address must be word bounded and located within existing memory. If not the channel rejects all further requests until it is reset by a system reset, or a reset channel instruction. The memory allocation address points to the first word of a four

word status queue which contains two status doublewords. The channel stores the status in either status doubleword to indicate the completion of an operation. In addition to four word status queue, the channel requires five words that are used for auxillary storage to maintain the logical and physical position of the tape relative to the BTP RAM buffer.

Once the channel has been initialized it should not be reinitialized unless a reset channel instruction is issued or a system reset is performed. If the channel receives an INCH command once it has been initialized, it will copy the auxillary storage into the new allocation in order to maintain the RAM buffer's logical and physical position. Also, whenever an INCH command is issued, the BTP must wait for any drive activity (other than rewind) to cease. (See Figure 3-7.)

The INCH command causes all drives that are attached to be addressed, in order to log their respective rewind and online status. During any period of inactivity in the BTP, the drives are scanned at a 500 millisecond interval. The current state of a drive is compared against its last logged state. If it has changed, an interrupt request is attempted. This function also allows the automatic posting of Device End status and an interrupt to be requested, indicating a rewind completion or a change in the online status of a drive.

An optional error log may be activated at this time by specifying the byte count of the INCH IOCD to contain a number greater than '0001 hex. This option will require four additional memory words for each drive attached. This additional allocation creates an error log entry based on the drive address and not on the number of drives attached. To allow the error log option, 32 consecutive words must be reserved for th BTP in addition to the original nine words mentioned previously. The error log entry for a particular drive contains counters which indicate the total number of bytes written to, the total number of bytes read from tape, the total number of write errors corrected (including multiple retry attempts upon the same record), and the total number of read errors corrected (multiple retrys upon the same record are not logged for read operations).

The ICOD fields are formatted as follows:

Command	'00 hex
Data address	Program dependent
Valid flag bits	CC and PPCI
Minimum byte count	'0001 hex
Maximum byte count	Ignored

4.3.8.2 No Operation

Command execution consists of the immediate initiation or command chaining I/O program termination, whichever is appropriate.

4.3.8.3 Sense

The sense (SNS) command causes the BTP to transmit one or four bytes of detailed drive status information, and when supported, extended sense information from the transport. The extended drive status is obtained by specifying a total byte count of 12 to retrieve 8 additional sense bytes. The extended sense is device dependent. The sense command also provides the ability to re-sync the buffer to the tape transport when the tape has been in the write mode. This forces the contents of the ram buffer to be written to the tape unit before the sense command is completed. The use of the sense command on

every I/O operation to the tape, will reduce the performance of the subsystem considerably. It is recommended that sense commands be issued only when an error status is detected or when the current task has been completed and the tape unit is closed.

During read operations the sense has no effect upon performance. However, extended sense data may not be transmitted when records have been pre-fetched. This restriction occurs at the physical drive, where the read operations are occurring asynchronous and thus the extended sense information is invalid.

SENSE BIT ASSIGNMENT

Bit	Description	Bit	Description
00	Command reject	16	Mode register bit 00
01	Intervention required	17	Mode register bit 01
02	(Spare)	18	Mode register bit 02
03	Equipment check	19	Mode register bit 03
04	Data check	20	Mode register bit 04
05	Data overrun	21	Mode register bit 05
06	(Spare)	22	Mode register bit 06
07	Lookahead error	23	Mode register bit 07
08	PE tape mode error	24	Drive ready
09	Tape PE mode check	25	Drive online
10	Filemark detected	26	Drive is file protected
11	Corrected error	27	Drive is NRZI
12	Hard error	28	(Spare)
13	Mode register load error	29	Drive is at load point
14	Data written	30	Drive is at end of tape
15	(Spare)	31	(Spare)

The IOCD fields are formatted as follows:

Command	'04 hex
Data address	Program dependent
Valid flag bits	CC, PPCI
Minimum byte count	'0001 hex
Maximum byte count	'000C hex

4.3.8.4 Set Mode

The set mode (SETM) command allows programmable modification to the operating characteristics of the BTP subsystem. This command allows one byte of mode data to be transferred from system memory to the BTP's internal mode register. The mode bit assignment allows for compatibility with current tape handlers. Although the density select bits are assigned, they are not implemented due to limitations within various manufacturers' tape transports. Mode bit zero allows a read to occur upon data regardless of whether it can be recovered by the BTP or not. This may be used when program continuation is more important than a bad record of data.

MODE BIT ASSIGNMENT

Bit		Description
00	0	Perform auto error recovery on read operation
	1	Read regardless if error recovery fails

The following assignments provide compatibility with previous handlers.

01	0	Select NRZI
	1	Select PE
02		(Spare)
03		(Spare)
04		(Spare)
05		(Spare)
06	0	Select density according to mode bit 01
	1	Select GCR
07		(HSTP scatter/gather mode)

The IOCD field are formatted as follows:

Command	'83 hex
Data address	Program dependent
Valid flag bits	CC, SIL, PPCI
Minimum byte count	'0001 hex
Maximum byte count	'0001 hex

4.3.8.5 Write

The write (WR) command causes the transfer of data from memory to tape. The data, as specified by the buffer address field of the IOCD, is transferred to the BTP buffer memory at a maximum rate of two megabytes per second. The BTP issues the write record command to the tape unit when its queue pointers indicate that the record is next in queue for transmission to tape. The write operation occurs asynchronously to the software issued command, the software depends on the BTP for write error recovery. To assure data integrity, it is recommended that the software resynchronize the BTP buffer by using a non-buffer command such as the SENSE command. This causes the BTP to finish unloading the buffer to tape and if any pending, unrecoverable, errors exist it can be reported at that time.

The IOCD fields are formatted as follows:

Command	'01 hex
Data address	Program dependent
Valid flag bits	CC, DC, and PPCI
Minimum byte count	'0001 hex
Maximum byte count	'FFFF hex

4.3.8.6 Read Forward

The read forward (RDF) command causes the transfer of data from the tape to memory. The data, as specified by the buffer address field of the IOCD, is transferred from the BTP buffer to the main memory of the CPU at a maximum rate of 1.66 megabytes per second. The BTP continues to read additional records until the buffer is full. Segments of a physical record may be skipped during transmission to main memory by the use of the SKIP and DC flags.

Tape read errors are corrected through error recovery schemes built into the BTP. The read threshold level is adjusted, and recovery is attempted five times using the default value. The error log can be monitored to identify tape units experiencing data errors.

The amount of data transmitted is specified by the byte count field of the IOCD. Should the end-of-record be detected before the byte count register is decremented to zero the incorrect length (IL) status bit is set preventing command chaining. Also, this can be avoided if the flag byte field of the IOCD has the suppress length indicator (SIL) bit set. Should the byte count be reduced to zero before the end-of-record is detected, the IL status bit is set and the remaining data beyond that point specified is thrown away.

If an end-of-file (EOF) mark is detected, data is not transferred. Unit exception (UE) and incorrect length (IL) status are generated, and the EOF bit is set in the sense register.

Should the end-of-tape (EOT) be encountered during a RDF command, the operation is allowed to continue normally until the end-of-record is detected. The end-of-tape condition sets the UE status bit, the sense EOT bit, and terminates the I/O program.

If the drive is selected for PE recording, the RDF command causes the BTP to check for the PE ID burst at the beginning-of-tape. If this burst is missing, the tape media was not recorded in PE and is not able to be read. The BTP generates a tape mode check (TMC) in the sense register and a unit check (UC) bit is set in the status register. This terminates the program.

The IOCD fields are formatted as follows:

Command	'02 hex
Data address	Program dependent
Valid flag bits	CC, DC, SKIP, SIL, and PPCI
Minimum byte count	'0001 hex
Maximum byte count	'FFFF hex

4.3.8.7 Read Backward

The read backward (RDB) command causes the transfer of data from tape to memory in descending order. The data, as specified by the buffer address field of the IOCD, is transferred from the BTP to the main memory of the CPU at the transport rate. Segments of a record may be skipped during transmission to main memory by the use of the SKIP and DC flags. The BTP does not attempt any error recover for this command. This command does not allow any record pre-fetching, as it operates synchronous to the computer. The amount of data transmitted is specified by the byte count field of the IOCD. Should the end-of-record be detected before the byte count register has been decremented to zero, the incorrect length (IL) status bit is set preventing command chaining. Also, this can be avoided if the flag byte field of the IOCD has the suppress

length indicator (SIL) bit set. Should the byte count be reduced to zero before the end-of-record is detected, the IL status bit is set and the remaining data beyond that point specified is thrown away. If the end-of-file (EOF) mark is detected, the data is transferred. At this time the Unit exception (UE), incorrect length (IL) status are generated, and the EOF bit is set in the sense register. Should the beginning of tape (BOT) be encountered during a RDB command, the operation is terminated immediately with unit exception status and sense BOT bit.

The IOCD fields are formatted as follows:

Command	'0C hex
Data Address	Program dependent
Valid Flag Bits	CC, DC, SKIP, SIL, PPCI
Minimum Byte Count	'0001 hex
Maximum Byte Count	'FFFF hex

4.3.8.8 Read and Compare

The read and compare (RDC) command causes the BTP to compare the data, as specified by the buffer address field of the IOCD, with data from the BTP internal buffer at a maximum rate of two megabytes per second. The BTP continues to read additional records until its buffer is full. Segments of a physical record may be skipped during comparison with main memory by the use of the SKIP and DC flags.

Indication of the success of the compare operation is presented via the status modifier (SM) bit. Also, if the compare is successful the following IOCD is skipped and the next successive IOCD is fetched by the BTP. Through the use of the transfer-in-channel (TIC) opcode, tape labels may be searched without software intervention.

Tape read errors are corrected through error recovery schemes built into the BTP. The read threshold level is adjusted, and recovery is attempted five times using the default value. The error log can be monitored to identify tape units experiencing data errors.

The amount of data compared is specified by the byte count field of the IOCD. Should the end-of-record be detected before the byte count register is reduced to zero the incorrect length (IL) status bit is set preventing command chaining. Also, this can be avoided if the flag byte field of the IOCD has the suppress incorrect length indicator (SIL) bit set. If the byte count is reduced to zero before the end-of-record is detected, the IL status bit is set and the remaining data beyond that point specified is thrown away.

If an end-of-file mark is detected, data can not be compared. Unit exception (UE) and incorrect length (IL) status are generated, and the EOF bit is set in the sense register.

Should the end-of-tape (EOT) be encountered during a RDC command, the operation is permitted to continue normally until the end-of-record is detected. The end-of-tape condition sets the UE status bit and the sense EOT bit, and terminates the I/O program.

If the drive is selected for PE recording, the RDC command causes the BTP to check for a PE ID burst at the beginning-of-tape. If the ID burst is missing, the tape media was not recorded in PE and is not able to be read. The BTP generates a tape mode check (TMC) in the sense register and a unit check (UC) bit is set in the status register. This terminates the program.

The IOCD fields are formatted as follows:

Command	'13 hex
Data address	Program dependent
Valid flag bits	CC, DC, SKIP, SIL, and PPCI
Minimum byte count	'0001 hex
Maximum byte count	'FFFF hex

4.3.8.9 Advance Record

The advance record (AR) command causes the BTP to position the tape past one record of data. No error checking or recovery will be performed for the record advanced. If the record existed in the BTP RAM, it will be accessed at the BTP's memory rates rather than the transport rate. If an end-of-file (EOF) mark is detected, the unit execution (UE) status is generated and the EOF bit is set in the sense register. Should the end-of-tape (EOT) be encountered during a AR command, the generation will be allowed to continue normally until the end-of-record has been detected. The end-of-tape condition sets the UE status bit, the sense EOT bit, and terminates the I/O program. If the drive is selected for PE recording, the AR command causes the BTP to check for the PE ID burst at the beginning-of-tape. If this burst is missing, the tape media has not been recorded in PE and is not able to read. The BTP generates a tape mode check (TMC) in the sense register and a unit check (UC) bit is set in the status register. This terminates the program.

The IOCD fields are formatted as follows:

Command	43
Data Address	N.A.
Valid Flag Bit	CC, PPCI
Minimum Byte Count	'0001 hex
Maximum Byte Count	Ignored

4.3.8.10 Backspace Record

The backsapce record (BR) command causes the BTP to position the tape past one record of data in reverse direction. No error checking will be performed for record backspace. The operation is not buffered in the BTP RAM and therefore occurs synchronously to the system. If an end-of-file (EOF) mark is detected, unit exception (UE) status is generated and the EOF bit is set in the sense register. Should the beginning of tape (BOT) be encountered during a RDB command, the operation is terminated immediately with unit exception status and the sense BOT bit.

The IOCD fields are formatted as follows:

Command	'53 hex
Data Address	N.A.
Valid Flag Bits	CC, PPCI
Minimum Byte Count	'0001 hex
Maximum Byte Count	Ignored

4.3.8.11 Advance Filemark

The advance filemark (AF) command will cause the BTP to position the tape to the next filemark on tape. No error checking or recovery will be performed upon any of the data prior to the filemark. If the filemark had been pre-fetched, and existed in the BTP RAM, it would be accessed at the BTP's memory rates. Should the end-of-tape be detected during an AF command, the operation is allowed to continue until the filemark is detected. Should the end-of-tape (EOT) be encounterd during a AR command, the operation is allowed to continue normally until the end-of-record is detected. The end-of-tape condition sets the UE status bit, the sense EOT bit, and terminates the I/O program. If the drive is selected for PE recording, the AR command causes the BTP to check for the PE ID burst at the beginning-of-tape. If this burst is missing, the tape media was not recorded in PE and is not able to be read. The BTP generates a tape mode check (TMC) in the sense register and a unit check (UC) bit is set in the status register. This terminates the program.

The IOCD fields are formatted as follows:

Command	'63 hex
Data Address	N.A.
Valid Flag Bits	CC, PPCI
Minimum Byte Count	'0001 hex
Maximum Byte Count	Ignored

4.3.8.12 Backspace Filemark

The backspace filemark (BFM) causes the BTP to position the tape in the reverse direction to the next filemark. No error checking will be performed upon any of the data prior to the filemark. The operation is not buffered in the BTP RAM and therefore occurs synchronously to the system. If an end-of-file (EOF) mark is detected, unit exception (UE) status is generated and the EOF bit is set in the sense register. Should the beginning of tape (BOT) be encountered during a RDB command, the operation is terminated immediately with unit exception status and the sense BOT bit.

The IOCD fields are formatted as follows:

Command	'73 hex
Data Address	N.A.
Valid Flag Bits	CC, PPCI
Minimum Byte Count	'0001 hex
Maximum Byte Count	Ignored

4.3.8.13 Write Filemark

The write filemark (WFM) command causes a filemark to be written on the tape. The actual filemark pattern and timing is controlled by the tape formatter. No data transfer occurs between the BTP and the tape unit to accomplish the operation. When an entry is available in the queue, the WFM request is queued and the response to software occurs immediately to indicate the completion of the WFM command. The BTP issues the WFM command to the tape unit when its queue pointers indicate that the filemark is next in queue for transmission to tape. The asynchronous operation occurs in the same manner as a write command (WR). It is again recommended that the software resynchronize the BTP buffer by using a non-buffered command such as the SENSE command. This causes

the BTP to finish unloading the buffer to tape and if any pending, unrecoverable errors exist, they can be reported at that time. Mode bits, as specified by the set mode command, alter the operating characteristics of the write command. These bits are defined in the set mode description.

The IOCD fields are formatted as follows:

Command	'93 hex
Data Address	N.A.
Valid Flag Bits	CC, PPCI
Minimum Byte Count	'0001 hex
Maximum Byte Count	Ignored

4.3.8.14 Erase Fixed

The erase fixed (ERA) command causes a 3.5 inch length of tape to be erased. The ERA command is not buffered and operates synchronously to the system. Any information contained in the buffer will be removed before the command is issued to the tape unit, thereby re-synchronizing the BTP to the computer. Should the end-of-tape (EOT) be detected during an ERA command, the operation continues until completed. The end-of-tape condition sets the UE status bit, the sense EOT bit, and terminates the I/O program.

The IOCD fields are formatted as follows:

Command	'A3 hex
Data Address	N.A.
Valid Flag Bits	CC, PPCI
Minimum Byte Count	'0001 hex
Maximum Byte Count	Ignored

4.3.8.15 Rewind

The rewind (REW) command causes the addressed tape unit to rewind the tape to its load point. Before the rewind is initiated, the buffer is tested for its operational state. If any write operations are pending in the buffer, they will be unloaded to the tape. If any read operations were pre-fetched, they will be thrown away. All buffer control flags will be reset and the hardware for the ram cleared when the rewind command is issued. When the REW command has caused the drive to start rewinding, the BTP generates channel end (CE) status and attempts to request an interrupt. At this time the BTP is capable of initiating an operation to a different tape unit. When the rewind operation is complete, the BTP will generate device-end (DE) status and attempt to request an interrupt.

The IOCD fields are formatted as follows:

Command	'23 hex
Data Address	N.A.
Valid Flag Bits	CC, PPCI
Minimum Byte Count	'0001 hex
Maximum Byte Count	Ignored

4.3.8.16 Rewind and Unload

The rewind and unloaded (RWU) command executes identically to the rewind except that when the drive reaches load point it will continue to rewind the tape until all of the tape is removed from the take-up reel. All the operational characteristics of the RW command apply to RWU, with this exception.

The IOCD fields are formated as follows:

Command	'33 hex
Data Address	N.A.
Valid Flag Bits	CC, PPCI
Minimum Byte Count	'0001 hex
Maximum Byte Count	Ignored

APPENDIX A

SelBUS PIN ASSIGNMENTS (Connector P1B)

Pin	Signal	Description
1	GND	Ground
2	GND	Ground
3	+5vA	Positive 5 volts dc from power supply
4	+5vA	Positive 5 volts dc from power supply
5	LD01	Data bit 01
6	LD00	Data bit 00
7	LD03	Data bit 03
8	LD02	Data bit 02
9	LD04	Data bit 04
10	GND	Ground
11	LD06	Data bit 06
12	LD05	Data bit 05
13	+5vB	Positive 5 volts dc from battery backup
14	LD07	Data bit 07
15	LD09	Data bit 09
16	LD08	Data bit 08
17	LD11	Data bit 11
18	LD10	Data bit 10
19	GND	Ground
20	LD12	Data bit 12
21	LD14	Data bit 14
22	LD13	Data bit 13
23	+5vB	Positive 5 volts dc from battery backup
24	LD15	Data bit 15
25	LD17	Data bit 17
26	LD16	Data bit 16
27	LD19	Data bit 19
28	LD18	Data bit 18
29	LD20	Data bit 20
30	GND	Ground
31	LD22	Data bit 22
32	LD21	Data bit 21
33	LCPUTRAP	CPU trap
34	LD23	Data bit 23
35	LD25	Data bit 25
36	LD24	Data bit 24
37	LD27	Data bit 27
38	LD26	Data bit 26
39	GND	Ground
40	LD28	Data bit 28
41	LD30	Data bit 30
42	LD29	Data bit 29
43	+5vB	Positive 5 volts dc from battery backup
44	LD31	Data bit 31

Pin	Signal	Description
45	GND	Ground
46	GND	Ground
47	+5vA	Positive 5 volts dc from power supply
48	+5vA	Positive 5 volts dc from power supply
49	LDT01	Destination bit 01
50	LDT00	Destination bit 00
51	LDT03	Destination bit 03
52	LDT02	Destination bit 02
53	LDT04	Destination bit 04
54	GND	Ground
55	LDT06	Destination bit 06
56	LDT05	Destination bit 05
57	LDT08	Destination bit 08
58	LDT07	Destination bit 07
59	LDT10	Destination bit 10
60	LDT09	Destination bit 09
61	LDT12	Destination bit 12
62	LDT11	Destination bit 11
63	GND	Ground
64	LDT13	Destination bit 13
65	LDT15	Destination bit 15
66	LDT14	Destination bit 14
67	LDT17	Destination bit 17
68	LDT16	Destination bit 16
69	LDT19	Destination bit 19
70	LDT18	Destination bit 18
71	LDT21	Destination bit 21
72	LDT20	Destination bit 20
73	LDT22	Destination bit 22
74	GND	Ground
75	LDTF	Byte transfer tap signal
76	LDT23	Destination bit 23
77	LREADY	Ready signal
78	GND	Ground
79	GND	Ground
80	LSYNC	Sync interrupt poll
81	LCKLE	System clock early
82	GND	Ground
83	GND	Ground
84	LCLK	System clock
85	LCLKL	System clock late
86	GND	Ground
87	GND	Ground
88	LSTSC	Stop system clock
89	+15v	Positive 15 volts dc
90	+15v	Positive 15 volts dc
91	GND	Ground
92	GND	Ground
93	GND	Ground
94	GND	Ground
95	-15v	Negative 15 volts dc
96	-15v	Negatvie 15 volts dc
97	LCPUSC	CPU stop clock

Pin	Signal	Description
98	GND	Ground
99	GND	Ground
100	LCLP	Clock problem
101	LINH00	Memory busy inhibit 00
102	GND	Ground
103	LINH01	Memory busy inhibit 01
104	LRESET	I/O reset
105	LINH02	Memory busy inhibit 02
106	LCLKOV	Clock override
107	LINH03	Memory busy inhibit 03
108	LRTC	Real time clock
109	+12v margin	Margin MOS memories (DSS test stand only)
110	-5v margin	Margin MOS memories (DSS test stand only)
111	GND	Ground
112	LPF	Power fail
113	LPFMEM	Power fail memory
114	Ext +5v	External positive 5 volt dc
115	LTRC	Transmitting C
116	LMUNLK	Unlock memory
117	LREFM	Refresh memory
118	LERROR	Memory error
119	LECK0	Echo bit 0
120	LRTRY	Retry
121	LECK1	Echo bit 1
122	GND	Ground
123	LD32/P0	Parity bit byte 0
124	LCHBSY	Channel busy
125	LD33/P1	Parity bit byte 1
126	LTX	Transfer tag bit
127	LD34/P2	Parity bit byte 2
128	LCPUSTART	CPU start
129	LDP0/P3	Parity bit byte 3
130	LTA	Transfer acknowledge
131	GND	Ground
132	LCNT0	Control 0 tag signal
133	LSCPATTN	System control panel attention
134	LCNT1	Control 1 tag signal
135	LPEF	Pre-refresh memory
136	LCPU	CPU bit line signal
137	+5vA	Positive 5 volts dc from power supply
138	+5vA	Positive 5 volts dc from power supply
139	GND	Ground
140	GND	Ground
141	LPR00	Poll priority bit 00
142	LRD	Read tag signal
143	HPR01	Poll priority bit 01
144	LMEM	Memory tag signal
145	HPR02	Poll priority bit 02
146	GND	Ground
147	HPR03	Poll priority bit 03
148	LUS	Memory unsuccessful tag bit
149	HPR04	Poll priority bit 04
150	+5vB	Positive 5 volts dc from battery backup

Pin	Signal	Description
151	HPR05	Poll priority bit 05
152	LMLK	Memory lock tag bit
153	HPR06	Poll priority bit 06
154	LIPOL	Interrupt poll
155	GND	Ground
156	LEOIP	End of interrupt poll
157	HPR07	Poll priority bit 07
158	LINTR	Interrupt request
159	HPR08	Poll priority bit 08
160	LIOIN	I/O interrupt inhibit
161	HPR09	Poll priority bit 09
162	LEXIN	External interrupt
163	HPR10	Poll priority bit 10
164	+5vB	Positive 5 volts dc from battery backup
165	HPR11	Poll priority bit 11
166	GND	Ground
167	HPR12	Poll priority bit 12
168	LERRED	Parity bit toggle signal
169	HPR13	Poll priority bit 13
170	LIORST	I/O reset
171	HPR15	Poll priority bit 15
172	HPR14	Poll priority bit 14
173	HPR17	Poll priority bit 17
174	HPR16	Poll priority bit 16
175	GND	Ground
176	HPR18	Poll priority bit 18
177	HPR20	Poll priority bit 20
178	HPR19	Poll priority bit 19
179	HPR22	Poll priority bit 22
180	HPR21	Poll priority bit 21
181	+5vA	Positive 5 volts dc from power supply
182	+5vA	Positive 5 volts dc from power supply
183	GND	Ground
184	GND	Ground

APPENDIX B

GLOSSARY OF LOGIC DRAWING TERMS

Mnemonic	Logic Drawing 130-103640 Sheet Number	Definition
H2CLK3	2	System clock buffered twice
H2CLK4	2	System clock buffered twice
H2CLK5	2	System clock buffered twice
H2CLKFREERUN	2	Free run clock buffered twice
H3ONSCLK1	10	30-nanosecond clock
H3ONSCLK2	10	30-nanosecond clock
H3ONSCLK3	10	30-nanosecond clock
H3CLK1	9	System clock buffered three times
H3CLK2	34	System clock buffered three times
HAEQB-TST	19	A equals B ALU status
HAIN00-15	11	A-file input bits 0 through 15
HALU-C	19	ALU carry
HALUS0	20	C-reg bit 27 and ALU function select 0 bit
HALUS0B	20	C-reg bit 27 and ALU function select 0 bit
HALUS1	20	C-reg bit 26 and ALU function select 1 bit
HALUS1B	20	C-reg bit 26 and ALU function select 1 bit
HALUS2	20	C-reg bit 25 and ALU function select 2 bit
HALUS2B	20	C-reg bit 25 and ALU function select 2 bit
HALUS3	20	C-reg bit 24 and ALU function select 3 bit
HALUS3B	20	C-reg bit 24 and ALU function select 3 bit
HBIN00-15	12	B-file input bits 0 through 15
HBRANCH	14	ROM output bit zero and branch microinstruction
HBUSDRT	4	SelBUS - data return transfer
HCARRY-FF	22	ALU carry status flip-flop
HCCG-ID-TST	22	Check character gate/identify burst test
HCER-TST	22	Corrected error test
HCLKECKX	21	Clock echo flip-flops
HCLKLVL2	10	Clock level 2
HCLKFULLFF	28	Clock full flip-flop
HCNT-PC	13	Enable program counter count mode
HCPUREQST	3	CPU request look-ahead
HCREG02	23	C-register bit 2
HCREG08-11	11	C-register bits 8 through 11
HCREG12-20	12	C-register bits 12 through 20
HCREG28-31	12	C-register bits 28 through 31
HCROM08-23	20	CROM output bits 8 throuh 23
HDATAINT	10	Microinterrupt from SelBUS interface
HDESTSTROBE	8	SelBUS destination staging reg strobe
HEMPTY	22	Cache RAM empty
HEN-INT	10	ROM output bit 3 and enable interrupts
HEN-ORDERS	23	Generate orders microinstruction
HFEN	17	Formatter enable tape interface (L-order)

Mnemonic	Logic Drawing 130-103640 Sheet Number	Definition
HFIFO	17	Select RAM to operate in FIFO mode - level order
HFMK-TST	22	File mark status from tape test
HFULL	22	Cache RAM full status
HFULL-E	28	Cache RAM full or empty
HGO	17	Strobe to tape interface (L-order)
HHER-TST	22	Hard error test
HHIO	4	WDOT halt I/O flip-flop
HINH	4	Memory busy inhibit
HINOVRRUN	22	Cache RAM input overrun
HINTRESET	2	Interrupt reset
HIOMINREQ	22	IOM input request
HIOMOUTREQ	22	IOM output request
HLOL	17	Load online to tape - level order
HLONGBR	20	ROM output bit 1 and branch microinstruction
HLOSTPOLLBUS	4	Lost SelBUS poll to higher device
HLOSTPRIOR	9	Lost interrupt priority
HLSB	22	Least significant byte RAM holding register loaded
HMA00-07	33	Cache RAM multiplexed address bits 0-7
HMDRTGATE	4	Memory DRT gate
HMEMDATAHERE	3	Memory data here
HMEMDRT	4	Memory data return transfer
HMEMOUT	4	Output transfer to memory
HMEMTRANS	4	Memory transfer
HMICRODRT	8	Microprocessor data return transfer
HMICROINPUT	7	Microprocessor input
HMSB	22	Most significant byte RAM holding register loaded
HMSDA	11	C-reg bit 21 and A/B reg input mux select
HMSDB	12	C-reg bit 21 and A/B reg input mux select
HMSDC	12	C-reg bit 21 and A/B reg input mux select
HMSDD	11	C-reg bit 21 and A/B reg input mux select
HNONPRSMEM	3	Nonpresent memory error
HOFFLINE	4	Offline flip-flop
HOFL	17	Offline level order to tape
HORDER-OUT	20	ROM output bit 2 & order microinstruction
HPC00-09	11	Program counter bits 0 through 9
HPCA	11	Program counter bit A MSB
HPCB	11	Program counter bit B
HPOLLBUS	4	Poll for SelBUS priority
HPOLLMEM	18	Poll bus for memory transfer
HPOLLPERMIT	9	Interrupt poll permit
HPR01-21	18	Poll priority bus bits 1 through 22
HRB0	12	C-reg bit 4 and bit-reg address bit 0
HRB0T	20	ROM output bit 4 and B-reg address bit 0
HRB1	12	C-reg bit 5 and B-reg address bit 1
HRB1T	20	ROM output bit 5 and B-reg address bit 1
HRB2	12	C-reg bit 6 and B-reg address bit 2
HRB2T	20	ROM output bit 6 and B-reg address bit 2

Mnemonic	Logic Drawing 130-103640 Sheet Number	Definition
HRB3	12	C-reg bit 7 and B-reg address bit 3
HRB3T	20	ROM output bit 7 and B-reg address bit 3
HRDA00-15	30	Cache RAM read address bits 0 through 15
HRDACK	24	Read acknowledge from cache contention logic
HRDC00-15	28	Cache RAM read address bits 0-15 to compare logic
HRDINT	22	Read transfer service test
HREQFIN	4	Requested finished
HREQFIND	4	Request finished delayed
HRESET	2	I/O reset
HREW	17	Rewind level order to tape
HRFA00-06	29	Refresh address bits 0 through 6
HRFA07	22	Refresh address bit 7 to test structure
HSETWEOR	24	Set write end-of-record flip-flop in RAM
HSHIFTEN	9	Shift enable
HSIO	4	Start I/O
HSKEW50	10	50 ns skew clock to contention logic
HSNAP00-23	19	Snapshot output bits 0 through 23
HSNAP26-29	19	Shapshot output bits 26 through 29
HSNAP32-63	19	Snapshot output bits 32 through 63
HSTART	4	OK to start
HSTARTPOLL	4	Start poll for SelBUS transfer
HSTROB-OPR	10	Strobe operation register C-reg
HSYNC	9	Sync interrupt poll
HTAOUT	21	Transfer acknowledge out control signal
HTAPINACK	24	Acknowledge to HTAPINREQ
HTAPINREQ	24	Request from tape to input data to RAM
HTAPOUTREQ	24	Request from tape to output data from RAM
HTEST-RT	22	Test result true
HTESTADR0	22	ROM output bit 24 and test address bit 0
HTESTADR1	22	ROM output bit 25 and test address bit 1
HTESTADR2	22	ROM output bit 26 and test address bit 2
HTESTADR3	22	ROM output bit 27 and test address bit 3
HTESTADR4	22	ROM output bit 28 and test address bit 4
HTESTADR5	22	ROM output bit 29 and test address bit 5
HTESTADR6	22	ROM output bit 30 and test address bit 6
HTESTADR7	22	ROM output bit 31 and test address bit 7
HTRANSIN	8	Transfer addressed to this IOM
HTRANSIN+1	4	Transfer input + 1 clock
HTRANSOUT	4	Transmit out to SelBUS
HWARAM	10	Write A-RAM strobe
HWBRAM	12	Write B-RAM strobe
HWONPOLL	4	Bus priority poll won
HWRA00-15	30	Cache RAM write address bits 0 through 15
HWRTACK	24	Any RAM write request acknowledged
HWRTINT	22	Write transfer service test
L1BREQ	17	One byte request to read RAM (pulse order)
L1CLKFREERUN	10	Free run clock buffered once
L2BREQ	17	Two byte request to read RAM (pulse order)
L2CLK1	10	System clock buffered twice

Mnemonic	Logic Drawing 130-103640 Sheet Number	Definition
L2CLK2	3	System clock buffered twice
L2CLK3	10	System clock buffered twice
L2CLK4	2	System clock buffered twice
L3CLK1	9	System clock buffered three times
L3CLK2	9	System clock buffered three times
L3CLK20	9	System clock
LACTIVE	4	Active - level order
LACTIVEINTR	9	Active interrupt order delayed
LAEQB-FF	22	ALU zero status flip-flop
LAIN00-15	11	A-file output bit bits 0 through 15
LALU00-15	12	ALU latch output bits 0 through 15
LALU00T-15T	16	ALU direct output bus bits 0T through 15T
LALUMSB	19	ALU output most significant bit
LAMSB-FF	22	Stored most significant bit of ALU output
LB0-1, LB2-3	17	Select 1 to 4 bytes to be written to RAM from 4 byte multiplexer
LBIN00-15	12	B-file output bus bits 0 through 15
LBLOCK	20	Block cycle wait microinstruction
LBLOCK+1	10	Block cycle plus one wait microinstruction
LBRANCH	20	Branch microinstruction
LBRANCH-SEL	17	Branch select - pulse order 18
LBRFF	20	C-reg bit 0 and branch microinstruction
LBUSYGATE	4	SelBUS interface busy
LBYTETX	8	Byte transfer
LCAS	33	RAM column address strobe
LCHBSY	4	Channel busy
LCLEAR-CREG	23	Clear C register
LCLEAR-PC	23	Clear program counter
LCLK	2	System clock from SelBUS
LCKR-HIO	4	Clear halt I/O order
LCLR-RD	17	Clear read
LCLR-STAT	17	Clear status latch from tape
LCLR-TER	17	Clear tape parity on LWEOR-FF
LCLRINT	9	Clear interrupt - pulse order
LCNT0	8	Control 0 tag signals from/to SelBUS
LCNT0IN	3	Control 0 tag signal
LCNT1	8	Control 1 tag signal
LCNT1IN	3	Control 1 tag signal
LCPUDATAHERE	3	Computer data is here
LD00-15	5	Data bits 0 through 15
LD02-1	5	Data bus bit 2
LD16-31	6	Data bits 16 through 31
LDATASTROBE	5	SelBUS data staging reg strobe
LDB00-15	11	Data bits 0 through 15
LDB16-31	12	Data bits 16 through 31
LDBY-LE	34	LDBY leading edge pulse 150 nanoseconds
LDBY-TE	24	LDBY trailing edge pulse 150 nanoseconds
LDBY-TST	22	LDBY test
LDEN	39	Density select to tape interface
LDEST00-15	11	Destination bits 0 through 15
LDESTSTROBE	7	SelBUS destination staging reg strobe

Mnemonic	Logic Drawing 130-103640 Sheet Number	Definition
LDIAG	17	Turn diag LED on/off - level order
LDT00-15	8	Destination bits 0 through 15
LDT16-23	7	Destination bits 16 through 23
LDTF	8	Byte transfer tag signal to SelBUS
LECK0	21	Echo zero
LECK1	21	Echo one
LEDIT	39	Edit command bit to tape
LENAREQ	35	Clears HLSB and HMSB flip-flop
LEND	22	End of logical record in cache RAM
LENDBY	17	Enable data busy LE and TE pulses
LEOIP	9	Enable interrupt poll from SelBUS
LEORIN	32	Input to cache RAM to indicate EOR
LEOT-TST	22	End-of-tape test bits
LERASE	39	Erase command bit to tape interface
LERROR	21	Error tape signal from SelBUS
LERRORIN	22	Error tape signal to test matrix
LEXT00-15	12	External input bits 0 through 15
LFAD	39	Formatter address select
LFBY-TST	22	Formatter busy test
LFEN	39	Formatter enable
LFLUSH	17	Reset cache RAM logic and counters - pulse order
LFPT-TST	22	File protect test
LFWD	17	Forward control signal to RAM read holding register
LGO	39	Formatter initiate command
LHALTIO	4	Halt I/O flip-flop
LHOLDRD	24	Hold any read request to RAM
LHOLDWRT	24	Hold any write request to RAM
LINH0-3	21	SelBUS inhibit bits 0 through 3
LINT-CYCL	10	Interrupt this cycle
LINT-CYCL+1	10	Interrupt this cycle plus one cycle
LINT-NXT-CYC	10	Interrupt on the next cycle
LINTADDR	9	Interrupt address level
LINTR	9	Interrupt request to SelBUS
LINTRESET	9	Interrupt reset
LINTRESET1	9	Interrupt reset
LIOIN	2	I/O interrupt inhibit from SelBUS
LIOINH	2	Interrupt inhibit
LIOMINACK	24	IOM input ackhowledge from RAM contention logic
LIOMOUTACK	24	IOM output acknowledge from RAM contention logic
LIORST	2	I/O reset from SelBUS
LIPOL	9	Interrupt poll
LLD-PCU	13	Load program counter upper bits
LLDADDR	17	Load tape address register - pulse order
LLDP-TST	22	Load point test
LLOL	39	Load on line control to tape
LLOSTPOLL	9	Lost SelBUS poll
LLSBSTB	35	Least significant byte strobe

Mnemonic	Logic Drawing 130-103640 Sheet Number	Definition
LLSTBYT	24	Last byte to RAM from IOM
LLWD	37	Last byte to tape
LMEM	8	Memory tag bit
LMEMCYCLE	24	Any cache RAM memory cycle
LMEMDATAHERE	3	Memory data is here
LMEMREAD	8	Memory read transfer
LMEMTX	8	Memory transfer
LMICROACK	4	Microprocessor acknowledge pulse order
LMICROBUSY	4	Microbusy order
LMICRODATALD	3	Microprocessor data load - pulse order
LMICRODESTLD	4	Microprocessor destination load
LMICORDRT	8	Microprocessor data return transfer
LMICRODRTFIN	4	Microprocessor data return transfer finished
LMICROINPUT	5	Microprocessor output transfer
LMICROMWTFIN	4	Microprocessor memory write transfer finished
LMICROREADY	4	Microprocessor ready
LMICRORETRY	4	Microretry order
LMICROTRANS	4	Microprocessor transmit
LMSBSTB	35	RAM output holding register MSB strobe
LMSC	12	Multiplexer select inverted CREG20
LMUXADDR	30	Multiplexer for dynamic RAM address
LNONPRSMEM	22	Nonpresent memory error
LNRZI-TST	22	NRZI/PE status test
LOFFLINE	2	Offline flip-flop
LONL-TST	22	Online test
LOUPUT	17	Load 32 bits into RAM - pulse order
LOUTUNDERRUN	22	RAM empty under run
LP-OFF	13	PROM off for test purposes
LPERR	22	RAM parity error
LPOLLBUS	18	SelBUS poll
LPR00	18	Poll priority bus bit 0
LPROM-EN0000	13	Enable ROM address 0 through 2047
LPROM-EN2048	13	Enable ROM address 2048 through 4096
LR00-07	32	Read tape data bits 0 through 7
LRAMD00-07	35	RAM data output bits 0 through 7
LRAMEOR	35	RAM output end-of-record flag bit
LRAMP	36	RAM output parity bit
LRAMP-X	36	RAM output parity bit exclusive ORed
LRAMPIN	32	Parity bit to RAM input
LRAS	33	RAM row address strobe
LRD	8	Read tag signal from/to SelBUS
LRDENA	24	Cache RAM read cycle enable
LRDIN	3	Read tag signals to text matrix
LRDX	3	Read tag signal from/to SelBUS
LRDY-TST	22	Ready status test from tape interface
LREAD	24	Cache RAM read cycle
LREADY	4	Read signal to SelBUS
LREFENA	24	Cache RAM allowed refresh cycle
LREFREQ	24	Refresh logic requesting
LREQINT	9	Request interrupt
LRESET	2	I/O reset

Mnemonic	Logic Drawing 130-103640 Sheet Number	Definition
LRESET1	4	I/O reset
LRESET2	4	I/O reset
LRESET3	4	I/O reset
LRESET4	2	I/O reset
LRESETA	2	I/O reset
LRESTORERD	17	Restore cache beginning of read address - pulse order
LRESTOREWRT	17	Restore cache beginning of write address - pulse order
LREV	39	Reverse command bit to tape
LREW	39	Rewind control to tape
LRP	32	Parity bit read from tape interface
LRP-S	32	Parity bit read from tape interface test
LRSTR-LE	34	Read strobe leading edge
LRSTR-TST	22	Read strobe test
LRTRY	4	Retry to SelBUS
LRWD-TST	22	Rewinding test
LSGL-TST	22	Single gap head test (NOT USED)
LSHIFTEN	9	Enable interrupt shift poll
LSKEW30	10	Clock delayed 30 nanoseconds
LSKEW45	10	System clock delayed 45 second
LSKEW50A	10	50 ns skewed clock to contention logic
LSKEW50B	10	50 ns skewed clock to contention logic
LSPEED-TST	22	Speed of tape status test
LSRA-CLK	25	Save read address clock for cache RAM
LSTOPCLK	2	Stop clock
LSTOPDATA+1	3	Stop data cock + 1 cycle
LSTOPDATACLK	3	Stop data clock
LSTOPDESTCLK	3	Stop destination clock
LSTSC	2	Stop clock from SelBUS
LSWA-CLK	25	Save write address clock for cache RAM
LSYNC	9	Sync interrupt poll
LTA	4	Transfer acknowledge
LTAD0	39	Tape transport address, bit 0
LTAD1	39	Tape transport address, bit 1
LTAOUT	4	Transfer acknowledge to SelBUS
LTAPERR	22	Parity error on tape data received
LTAPOUT	37	Tape write data register strobe
LTAPOUTACK	24	Tape output from RAM request acknowledged
LTEST-RT	22	Test results true
LTHR1	37	Threshold 1 to tape interface
LTHR2	37	Threshold 2 to tape interface
LTRANSOUT1	5	Transmit out to SelBUS
LTRANSOUT2	6	Transmit out to SelBUS
LTRANSOUT3	6	Transmit out to SelBUS
LTRANSOUT4	7	Transmit out to SelBUS
LTRANSOUT5	7	Transmit out to SelBUS
LTRANSOUT6	8	Transmit out to SelBUS
LTX	8	Transfer tag bit
LUS	21	Unsuccessful control from SelBUS
LUSXMENT	4	Unsuccessful memory transfer

Mnemonic	Logic Drawing 130-103640 Sheet Number	Definition
LW0-7	37	Write data bits 0 through 7 to tape
LWAITFORDRT	4	Wait for data return transfer
LWBUS00-07	31	Write data bus to cache RAM bits 0-7
LWD00-07	33	Write data inputs to cache RAM bits 0-7
LWE	33	RAM write enable control
LWEOR	22	Write end-of-record flip-flop test
LWFM	39	Write file mark
LWONPOLL	4	Won bus transfer priority poll
LWP	37	Write parity to tape
LWRA	10	CREG bit 22 and enable A-reg write
LWRB	10	C-reg bit 23 and enable B-reg write
LWRITE	24	Cache RAM write cycle
LWRT	39	Write command bit to tape
LWRTENA	24	Cache RAM write cycle enabled
LWRTTAPE	24	Select IOM to RAM to tape control path
LWSTR-TE	34	Write strobe trailing edge pulse
LWSTR-TST	22	Write strobe test

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