SA1404 Controller PROMS BS40, BS40*, or BS40+

Preliminary OEM Manual

Shugart

TABLE OF CONTENTS

1.0 Introduction

The SA1404 Controller is a sophisticated disk controller/formatter capable of handling a maximum of four SA4000 (SA4004, SA4008, SA4100) disk drives.

Commands are issued to the controller over a host adaptor in the host computer. The controller will detect data burst errors from the SA4000 (24 bits in length) and correct data burst errors (4 bits in length) before data is transferred to the computer.

2.0 SA1404 Controller

2.1 Features

2.1.1 The capabilities supplied as standard with the SA1404 are listed below:

OVERLAPPED SEEK	In multiple drive configurations, the host can issue seeks to different drives without waiting for the first drive to complete its seek.
AUTOMATIC SEEK AND VERIFY	A seek command is implied in every data transfer command (READ, WRITE, CHECK, etc.). If the heads are not positioned over the correct cylinder, a seek is initiated, and a cylinder verification is performed after the seek completes.
FAULT DETECTION	Two classes of faults are flagged to improve error handling: * Controller faults * Disk faults
AUTOMATIC HEAD SWITCHING	If during a multi-block data transfer the end of a track is reached, the controller automatically switches to the next track. If the end of a cylinder is reached, the controller issues a seek and resumes the transfer.

DATA ERROR DETECTION AND CORRECTION	If a data error is detected during a disk data transfer, the SA1404 will determine whether or not the error is correctable. If uncorrectable, the SA1404 will indicate this. If the error is correctable, either a pointer and mask can be requested by the host for applying the correction or the error can be automatically corrected by the SA1404.
LOGICAL TO PHYSICAL UNIT CORRELATION	Logical Unit Number (LUN's) are independent of physical port numbers. All accesses specify LUN's.
ON BOARD SECTOR BUFFER	A sector buffer is provided on the controller to eliminate the possibility of data overruns during a data transfer.
EFFICIENT HOST PROTOCOL	A bidirectional bus between the controller and host provides a simple yet efficient communication path. In addition, a high level command set permits effective command initiation.
SECTOR INTERLEAVING	Section interleaving is programmable with up to 32 ways.
ODD PARITY	The 8 data bits on the interface bus can have odd parity. Depending on user preference, parity can be disabled.
FIXED SECTOR SIZE	The sector size is fixed at 256 bytes of data.
NUMBER OF DRIVES	The controller will connect to a maximum of four (4) SA4000 drives.
BAD SECTOR WRITE PROTECT SECTOR	A sector can be flagged as bad sector or write-protected sector by the specified bits in ID field.
COPY COMMAND	Copies sectors from source drive to destination drive

2.1.2 Optional capabilities that can be provided

are as listed below:

MULTIPLE HOST	Up to 7 host computers may be connected to the controller.
MICRO DIAGNOSTICS	An on-board set of diagnostics is initiated by a set of switches on the controller. A complete set of drive diagnostics is also available
VARIABLE SECTOR SIZE	Sector sizes other than 256 bytes are available.

2.2 System Configuration

The controller and data separator comprise a single PCB. A maximum of four (4) 4000 series drives may be connected as shown in Fig. 2.1.

REV	SH	DWG. NO.

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	REV	DESCRIPTION	DATE	APPROVED

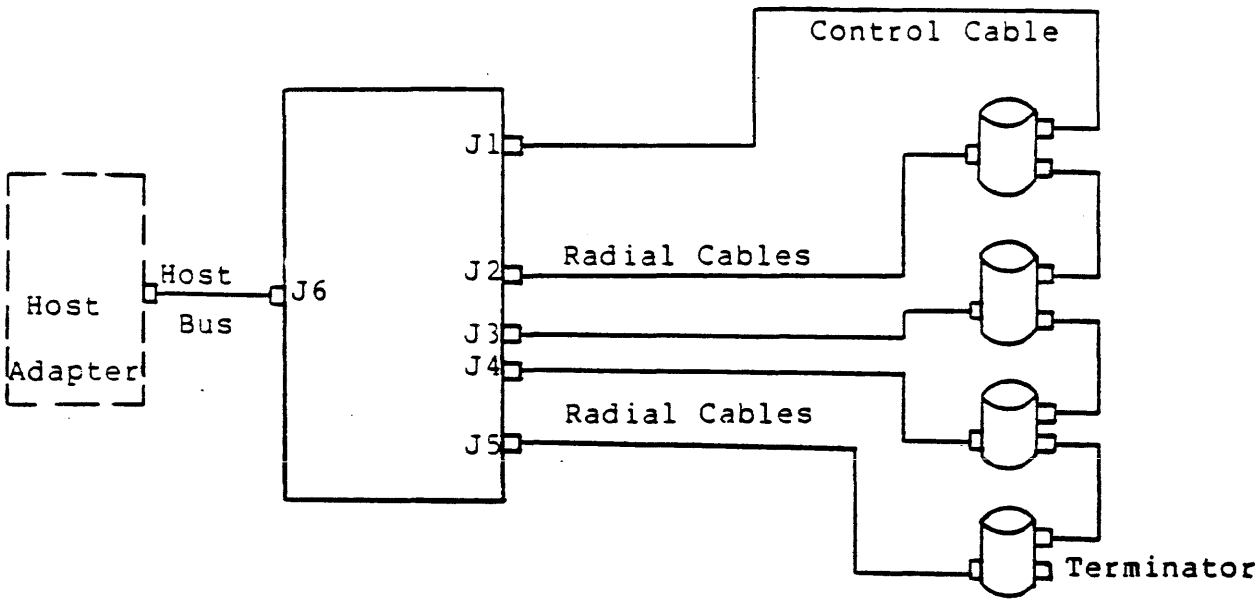


Figure 2.1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO. SA1404				
	APPROVALS	DATE			
MATERIAL	DRAWN V. TAO	4-28-80			
	CHECKED				
FINISH	ISSUED		SIZE A	FSCM NO.	DWG. NO. REV
DO NOT SCALE DRAWING			SCALE		SHEET

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	REV.	DESCRIPTION	DATE	APPROVED

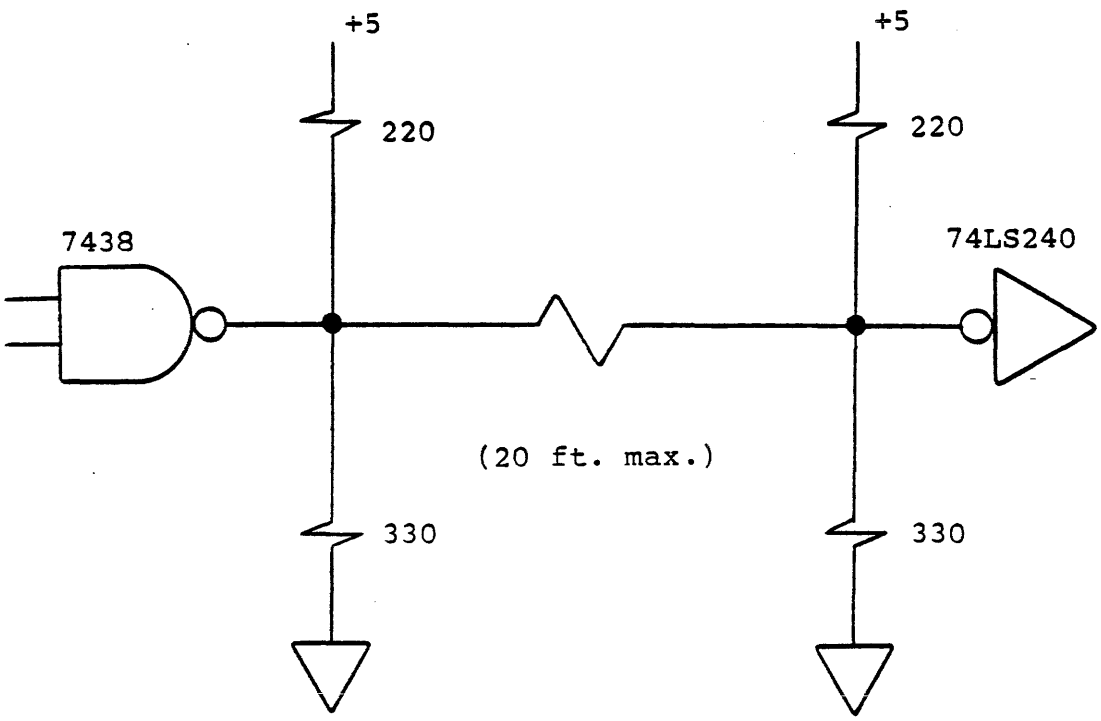


Figure 2.2

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.			
	APPROVALS	DATE	ELECTRICAL INTERFACE	
MATERIAL	DRAWN			
	CHECKED		SIZE A	FSCM NO. / DWG. NO. / REV.
FINISH	ISSUED			
DO NOT SCALE DRAWING			SCALE	SHEET

2.3 Theory of Operation

Disk commands are issued to the SA1404 via the host bus following a defined protocol. The host initiates a command sequence by selecting the controller on the bus. If the controller is not busy, it requests command bytes from the host for task execution.(Command structure is described in 4.0). Depending on the type of command, the controller will request up to 10 bytes. Upon reception of the last command byte, the controller begins execution of the command.

For the data transfer commands, a check is performed on the disk address and status flagged if it exceeds the drive limits. The data is stored in a sector buffer before transfer to the host or disk dive. This buffer eliminates any possibility of data overruns between the host and the disk.

Upon completion of the command, the controller will send completion status to the host. (Further delineation of the completion status may be requested by issuing the appropriate sense commands.)

Odd parity is generated by the SA1404 for all information that it puts on the I/O bus. If enabled, the SA1404 flags all information that it receives with bad parity.

2.3.1 Electrical Interface

The electrical interface to the SA4000 will conform to the requirements described in the SA4000 interface specification.

The electrical interface to the SA1404 Host Bus is shown in Fig.2.2.

3.0 SA1404 Host Bus

The SA1404 Host Bus is as a negative-logic, bidirectional 8-bit data bus utilizing odd parity. The electrical interface consists of an open collector bus terminated on each end by a 220/330 ohm resistor network. The controller regulates transfers across the bus which eliminates data overruns that could occur during data transfers.

The term asserted means that the signal on the host bus is between 0V and 0.8V. The term deasserted means that the signal on the host bus is between 2.5V and 3.5V (Negative or Low True logic).

3.1 Signal Definition

3.1.1 Unidirectonal Signals Driven By Controller

I/O — Input/Output. When asserted, the data on the bus is driven by the controller. When deasserted, the data on the bus is driven by the host adapter. The host adapter will use this line to enable its drivers onto the data bus.

C/D — Command/Data. When asserted, the data transmitted across the bus will be the command bytes. When deasserted, the data will be the disk data bytes.

BUSY — This bit is asserted as a response to the SEL line from the host adapter and to indicate that the host bus is currently in use.

MSG — Message. When asserted along with C/D and I/O, indicates that the command is completed. This bit is always followed with the assertion of REQ.

REQ — Request.
This bit operates in conjunction with I/O, C/D, & MSG. When asserted and I/O is asserted, REQ will mean that the data on the host bus is driven by the controller. When asserted and I/O is deasserted, REQ will mean that the data is driven by the h/a.

I/O	C/D	MSG	meaning
d	a	d	Get command fron H/A
d	d	d	Get data from H/A
a	d	d	Send data to H/A
a	a	d	Send status byte to H/A
a	a	a	Command done to H/A

a = asserted, d = deasserted

3.1.2 Unidirectional Signals Driven By Host Adaptor

ACK - Acknowledge
This bit is asserted as a response to REQ from the controller. The timing requirements on this signal with respect to the data is described in REQuest section. ACK must be returned for each REQ assertion. Once REQ has been asserted, the controller waits 256us for ACK return before timing out.

RST - Reset
When asserted, this bit forces the controller to the beginning of its microcode. Any error status request will result in invalid information after RST has been asserted. All signals to the drives are deasserted. RST must be asserted for a minimum of 250ns and a maximum of 10us.

SEL - Select
When asserted indicates the beginning of the command transaction. The h/a asserts SEL to gain the attention of the controller. A data bit on the host host bus must also be asserted during SEL time to determine which controller is selected. SEL must not be asserted on the host bus before the data bit. The controller will return BUSY within 1us. After the assertion of BUSY the host adapter will deassert SEL within 500ns.

3.1.3 Bidirectional Data

DB(7-0,P) - Data lines 7 thru 0 represent the eight data bits (DB0 = lsb). Parity is represented by P. The controller utilizes odd parity (the number of asserted bits on the host bus is always odd).

3.2 Theory of Operation

Whenever the host adapter has a command for the controller it performs a selection sequence to gain the attention of the controller. The sequence is as follows:

The host adaptor asserts SEL and DB0 (controller address bit) on the host bus. It then waits for the controller to respond with BUSY. Upon reception of BUSY the h/a deasserts SEL. The controller now has control of the host bus.

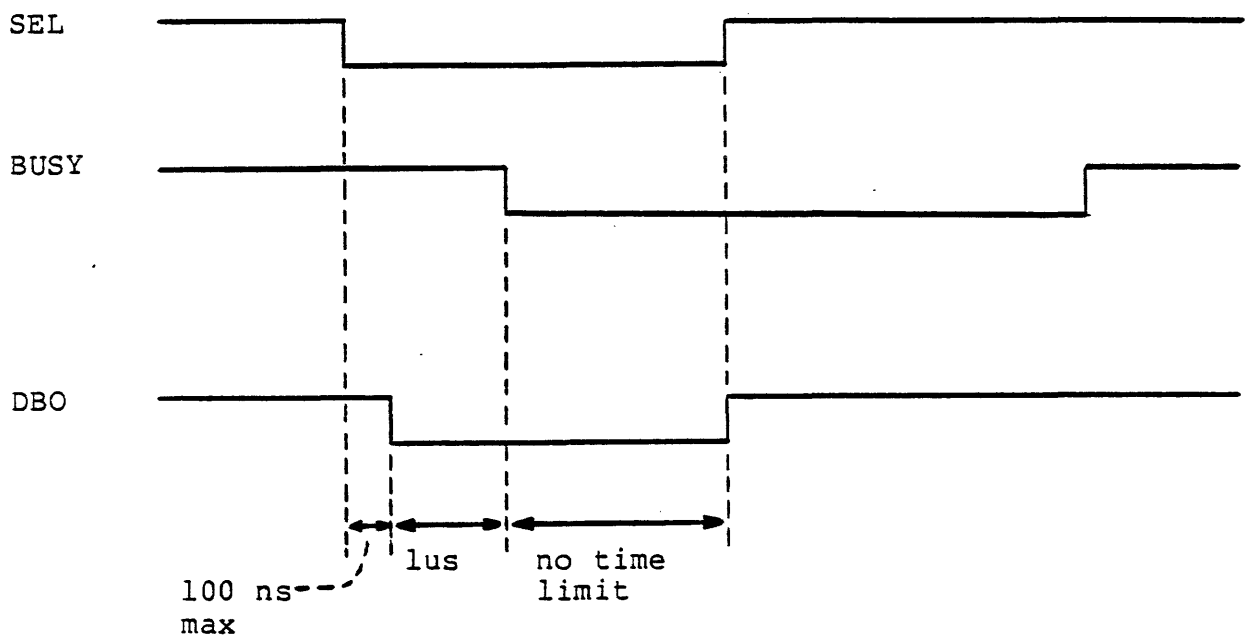
After the controller asserts BUSY it then asserts C/D (to indicate command mode transfer) and deasserts I/O (to indicate output from the host adaptor) to fetch the command bytes from the h/a. The command bytes are transfered over the host bus with the REQ/ACK handshake protocol until all command bytes are transferred to the controller. (The command byte fetch mode ends after the last REQ pulse from the controller is deasserted.)

For data transfer the controller deasserts the C/D line to indicate data mode. Depending on the command type (read/write disk) the I/O bit on the host bus is asserted or deasserted by the controller, and the data is transfered (a byte at a time) with the same REQ/ACK handshake protocol. After all the data bytes have been transfered, a completion status is placed on the data bus by the controller - C/D and I/O are asserted. REQ is asserted and the controller waits for ACK from the host adapter. After the status byte transfer the controller places zeros on the data bus and asserts C/D, I/O and MSG along with REQ to indicate to the host that the command is complete (this action can be used to generate an interrupt on the host system). After the h/a responds with ACK the controller deasserts REQ, BUSY and all other lines. This completes the command execution and the controller is now ready to be selected for the next command.

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	REV.	DESCRIPTION	DATE	APPROVED

3.2.1

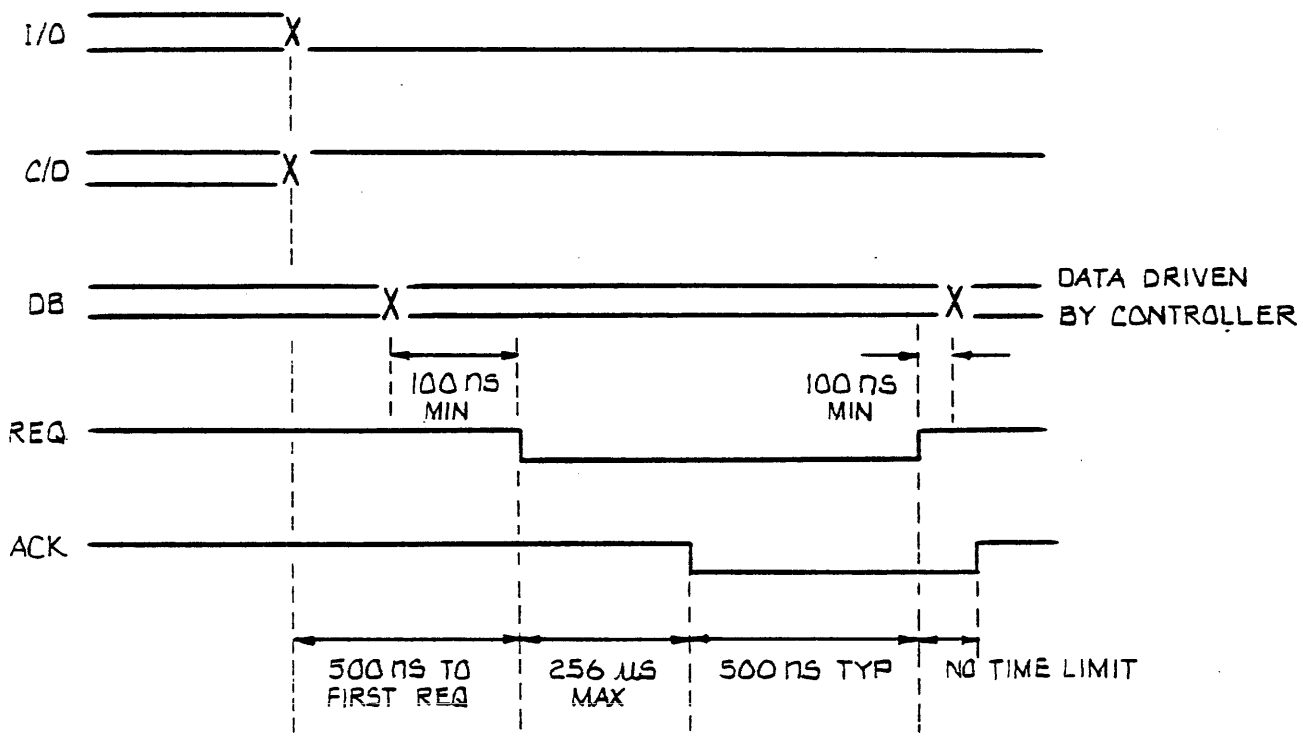
TIMING REQUIREMENTS FOR CONTROLLER SELECTION



Note: SEL must be deasserted before the controller will assert REQ.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±	CONTRACT NO.					
	APPROVALS	DATE				
MATERIAL	DRAWN					
	CHECKED					
FINISH	ISSUED		SIZE A	FSCM NO.	DWG. NO.	REV.
DO NOT SCALE DRAWING			SCALE		SHEET	

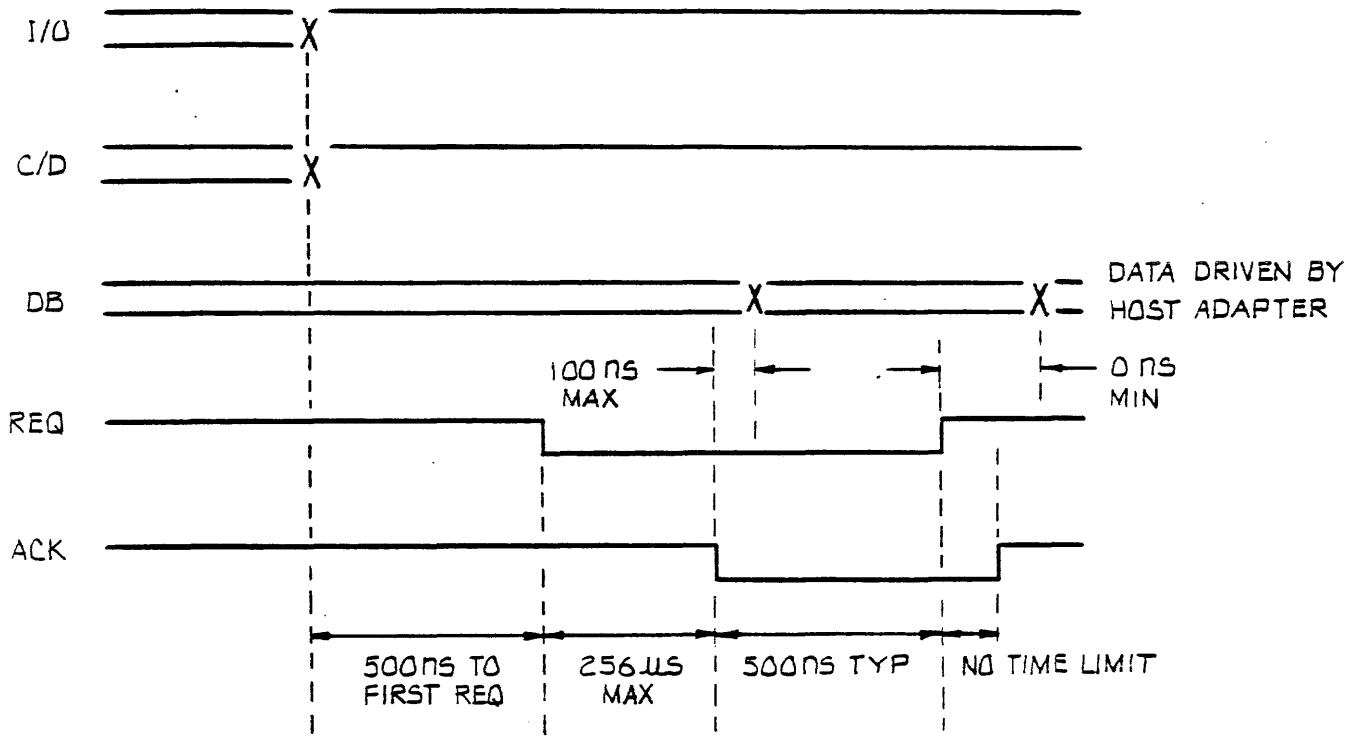
3.2.2 TIMING REQUIREMENTS FOR DATA TRANSFER
To Host Adapter - Typical Byte



NOTE: 1. For Status Byte Transfer (I/O, C/D asserted & MSG deasserted), or Interrupt Byte Transfer (MSG, I/O, C/D asserted), REQ is asserted 500ns (typical) after the assertion of any of the above bits.

2. Data driven by the controller is stable 100ns min at the host adapter end before REQ is asserted, and 100ns min after REQ is deasserted.

3.2.3 TIMING REQUIREMENTS FOR DATA TRANSFER
From Host Adapter - One Byte



NOTE: 1. Data driven by the host adapter must be stable 100ns (max) at the controller after ACK is asserted, and 0ns (min) after REQ is deasserted.

2. For command mode transfers, SEL must be deasserted before ACK is asserted. This sequence follows the selection protocol.

4.0 Commands

An I/O request to a disk drive is performed by passing a command descriptor block (CDB) to the controller. The first byte of a CDB is the command class and opcode. The remaining bytes specify the drive logical unit number (LUN), block address, control bytes, number of blocks to transfer or the destination device ID. The controller performs an implied seek and verify when required to access a block.

Commands are categorized into three classes as indicated:

Class 0	- Non-data Transfer, Data Transfer and Status Commands
Class 1	- Disk Copy Commands
Class 2-6	- Reserved
Class 7	- Diagnostic Commands

The command descriptor blocks in command class 0 and 7 are 6 bytes long and those in class 1 are 10 bytes long.

Command Description (Class 0)

Opcode (Hex)	Description
00	Test drive ready - Selects the drive and verifies drive ready
01	Recalibrate. Positions the R/W arm to Track00, clears possible error status in the drive.
02	Request Syndrome. Returns the offset and syndrome for data field error correction. The two bytes are as follows:

M.S. BIT OFFSET (8)		
L.S. BIT OFFSET (3)		SYNDROME (4)

The bit offset is relative from the 1st data bit. i.e., bit 7 of byte 0.

03	Request Sense. This command must be issued immediately after an error. It returns 4 bytes of drive and controller sense for the specified LUN. (See copy block for exception)
04	Format Drive. Formats all blocks with ID field according to interleave factor and data fields. The data field contains 6C Hex.
05	Check Track Format. Checks format on the specified track for correct ID and interleave. Does not read the data field.

06	Format Track. Formats the specified track with bad block flag cleared in all blocks of that track. Writes 6C Hex in the data fields.
07	Format Bad Sector. Writes the specified sector ID with bad block flag (Bit 7 in head byte) set.
08	Read. Reads the specified number of blocks starting from initial block address given in the CDB.
09	Write protect sector. Writes the specified sector ID field with write protected flag (Bit 6 in head byte) set.
0A	Write. Writes the specified number of blocks starting from initial block address given in the CDB.
0B	Seek. Initiates seek to specified block and immediately returns completion status before the seek is complete for those drives capable of overlap seek.

Command description (Class7)

Opcode (Hex)	Description
00	RAM Diagnostic. Performs a data pattern test on the RAM buffer.
01	Write ECC. Displaces data on the disk by three bytes so that the ECC bytes can be written from the data specified. Used to verify the ECC logic.
02	Read ID. Transfers the cylinder, head, sector and 3 ECC bytes for the specified block ID field.
03	Drive Diagnostic 0. Performs a drive diagnostic. Reads sectro 0 on all cylinders sequentially. Reads sector 0 on 256 random cylinders.

4.1 Command Format

4.1.1 Class 0 & 7 Commands

byte #	7 6 5	4 3 2 1 0
0	0 or 7	opcode
1	LUN	logical adr2
2	LOGICAL ADR1	
3	LOGICAL ADR0	
4	NUMBER OF BLOCKs	
5	CONTROL	

LUN = Logical Unit Number for the drive - 0, 1, 2, or 3.

LOGICAL ADR (0-2) = Logical Sector Address of specified sector. LOGICAL ADR0 is the LSB. Sectors start at zero (cyl = head = sector = 0). After the end of the track is reached, the next logical sector is located on the next track. If the end of the cylinder is reached, the next logical sector is located on the first track on the next cylinder. (See section 4.3 for Logical Address Computation).

The following example for the SA4008 drive (60 sectors per track, 8 movable heads, 8 fixed heads and 202 cylinders) and the SA4100 drive should clarify how Logical Address is assigned.

SA4008 Drive

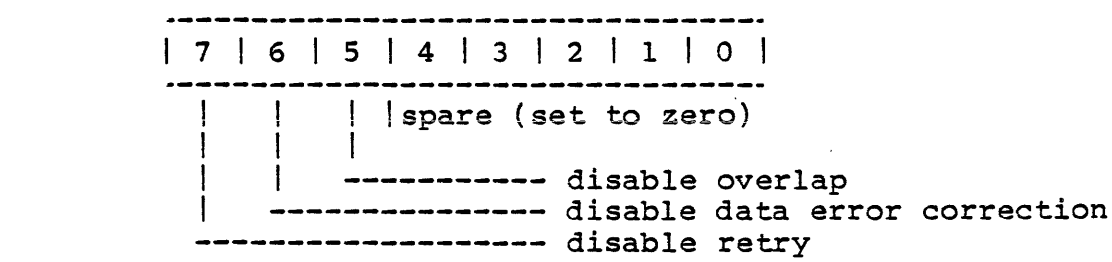
	CYL - HEAD - SECT	LOGICAL ADDRESS
Moveable Heads		
	000 - 0 - 00	0
	000 - 0 - 01	1
	000 - 1 - 00	60
	000 - 7 - 59	479
	001 - 0 - 00	480
	201 - 7 - 59	96959
Fixed Heads		
	xxx - 8 - 00	96960
	xxx - 8 - 01	96960 + 1
	xxx - 15 - 00	96960 + 420
	xxx - 15 - 59	96960 + 479

SA4100 Drive

	CYL	HEAD	SECT	LOGICAL ADDRESS
Moveable Heads				
	0	0	0	0
	0	15	59	959
	1	0	0	960
	201	0	0	192960
	201	15	59	193919
Fixed Heads				
	xxx	16	00	193920
	xxx	16	59	193979
	xxx	23	00	194340
	xxx	23	59	194399

NUMBER OF BLOCKS = Contains the number of blocks (sectors) to transfer per command. Also indicates the Interleave factor for Format, Check Track, and Read ID commands only.

CONTROL BYTE is defined as follows:



Commands in this group

a) NOP
b) Format Drive
c) Check Format
d) Request Sense
e) Request Syndrome
f) Recalibrate
g) Read Block(s)
h) Read ID
i) Write Block(s)
j) Format Track
k) Format Track (bad track flag)
l) Seek
m) Ram Diagnostic
n) Drive Diagnostic
o) Write ECC

4.1.2 Class 1 Commands

byte #	7	6	5	4	3	2	1	0
0	0	0	1	opcode				
1	LUN/s			logical adr2/s*				
2	logical adr1/s*							
3	logical adr0/s*							
4	number of blocks							
5	LUN/d			logical adr2/d*				
6	logical adr1/d*							
7	logical adr0/d*							
8	spare							
9	control							

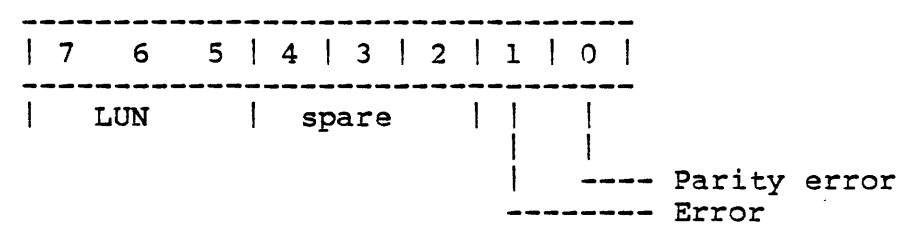
"s" indicates the source device
"d" indicates the destination device

*Refer to section 4.3 for Logical Address Computation

Command in this group - Copy Block

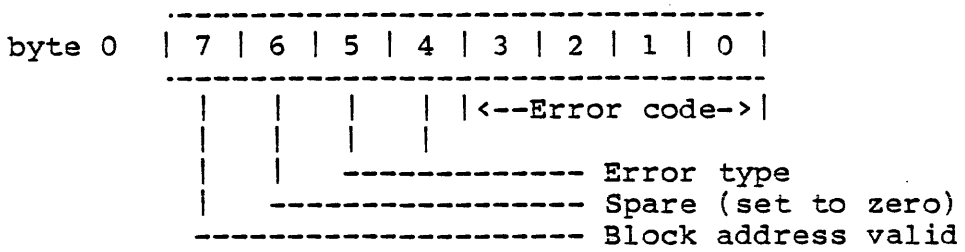
4.2 Status Format

4.2.1 Completion Status Byte



Bit 0 Parity error during transfer from host to controller.
Bit 1 Error occurred during command execution.
Bit 2-4 Spare (set to zero).
Bit 5-7 Logical unit number of the drive.

4.2.2 Drive and Controller Sense



byte #	7	6	5	4	3	2	1	0
1	LUN			logical adr2				
2	logical adrl*							
3	logical adr0*							

*Refer to section 4.3 for Logical Address Computation

4.3 Logical Address Computation

The logical address is computed as follows:

Logical Adr = (CYADR * HDCYL + HDADR) * SETRK + SEADR

Where: CYADR = cylinder address
HDADR = head address
SEADR = sector address
HDCY = number of heads per cylinder
SETRK = number of sectors per track

Bit 0 of Logical Adr0 = the least significant bit.
Bit 4 of Logical Adrl = the most significant bit.

4.3 ERROR CODES

Type 0 (Drive) Error codes.

0	No status
1	No Index signal.
2	No Seek Complete.
3	Write fault
4	Drive not ready
5	Drive not selected.
6	No Track00

Type 1 (Controller) Error codes.

0	ID read error. ECC error in the ID field.
1	Uncorrectable data error during a read.
2	ID Address Mark not found.
3	Data Address Mark not found.
4	Record not found. Found correct cylinder and head but not sector.
5	Seek error. R/W head positioned on a wrong cylinder and/or selected a wrong head.
6	DMA Data time out error. No acknowledge within 256us.
7	Write protected.
8	Correctable data field error.
9	Bad block found.

Type 2 (Command) Error codes.

0	Invalid Command received from the host.
1	Illegal disk address. Address is beyond the maximum address.

Type 3 (Misc) Error codes.

0	RAM error. Data error detected during Sector buffer RAM diagnostic.

5.0 Electrical/Mechanical Specification

Physical Parameters

Width	8.5	inches
Length	13.5	inches
Height	0.49	inches
Weight	1.12	lbs.

Environmental Parameters

	Operating	Storage
Temperature (degrees F/C)	32/0 to 131/55	-40/-10 to 167/75
Relative Humidity (@ 40 degrees F, wet bulb temp no condensation)	10% to 95%	10% to 95%
Altitude	sea level to 10K feet	sea level to 15K feet

Power Requirements

Voltage @ current	+5 VDC @ 4.6A (max)
	-5 VDC @ 500 mA (max)
	+24 VDC @ 100 mA (max)

6.0 DIAGNOSTIC PHILOSOPHY

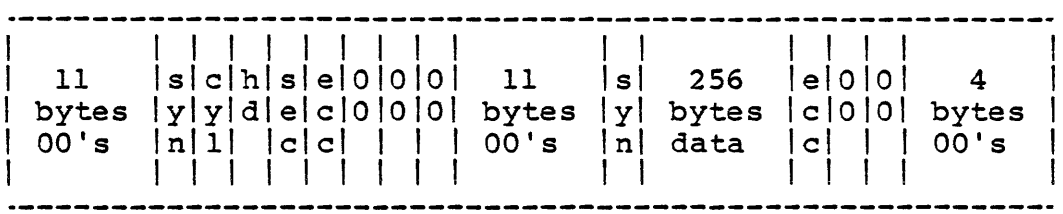
Fault Isolation Microdiagnostic (Optional)
The controller can be further checked out off-line by initiating explicit microdiagnostic routines via optional firmware diagnostic sets. The routines are initiated by a set of control switches. Errors will be displayed in a set of LED's. Each microdiagnostic checks the functionality of a particular section of the controller and is able to isolate failures in the following major categories:

- ALU
- Registers
- Sector Buffer
- ECC Logics

Fault-isolation techniques can be concentrated on the failing section.

7.0 SA4000 Sector Format

The track layout for the SA4000 (typical for 60 sectors) is shown below.



syn,cyl,hd,sec,00 = 1 byte
ecc = 3 bytes

Track Capacity = 18000

17880	= 298 x 60	Bytes/Sector
120	= 2 x 60	Index/Sector Gaps
18000		

298 bytes/sector

APPENDIX A

Host I/O Connector Pin Assignment.

The Host I/O Bus uses a 50-pin connector (AMP P/N 2-87227-5 or equivalent). The unused signal pins are considered to be spares for future use. The pin assignments are as follows :

Signal	Pin Number	
DATA0	2	
DATA1	4	
DATA2	6	
DATA3	8	
DATA4	10	
DATA5	12	
DATA6	14	
DATA7	16	
PARITY	18	
--	20	-----
--	22	|
--	24	|
--	26	Future
--	28	Usage
--	30	|
--	32	|
--	34	-----
BUSY	36	
ACK	38	
RST	40	
TDN	42	
SEL	44	
C/D	46	
REQ	48	
I/O	50	

NOTE: All signals are negative true and all odd pins are connected to ground. The signal lines are terminated with 220 ohms to 5V and 330 ohms to ground.

APPENDIX B

Prom Set Definitions and Switch Setting Definitions
Customer Firmware Dipswitch Setup Procedure

Location: 2J PRELIMINARY SETUP

	8 7	6 5	4 3	2 1	Switch Bits
Off	LUN 0 Drive Type	LUN 1 Drive Type	LUN 2 Drive Type	LUN 3 Drive Type	Field
					Definition
On					

Drive Type	Description	
0-on on	SA4004	4 moving hds, 201 cyl+8 fixed hds
1-on off	SA4008	8 moving hds, 201 cyl+8 fixed hds
2-off on	SA4100	16 moving hds, 201 cyl+8 fixed hds

All SA4000 drives are 60 sectors/track, 256 bytes/sector

Host Bus Parity jumper at 3P on controller board
A to B = enable odd parity checking/generation
B to C = disable odd parity

EXAMPLE:

Location: 2J

8 7	6 5	4 3	2 1	
LUN 0 Drive Type	LUN 1 Drive Type	LUN 2 Drive Type	LUN 3 Drive Type	OFF
on on	off on	on off	on on	ON

Drive 0 is set up for SA4004
Drive 1 is set up for SA4100
Drive 2 is set up for SA4008
Drive 3 is set up for SA4004

```
****************
*              *
*   WARNING    *
*              *
****************
```

The following voltages are required:

a) +24VDC

b) +5VDC

c) -5VDC

Do not use -15VDC on the SA1400. Serious Damage will result.

READ the Specification Before Attempting Power On !

APPENDIX C

JUMPER SETUP INSTRUCTIONS

The following information is contained in the SA4000 Fixed Disk Drive OEM Manual, Shugart Associates, 1978.

The SA4000 requires a control cable and radial cable.

Control PCB

J1 = 50 pins J2 = 20 pins

X	- open	drive selected only by SELECT line
DS	- 1,2,3,4 user selectable	Set to determine LUN
ST	- jumpered	Sector to J1 connector
RY	- open	Ready to radial connector only(J2 connector)
IX	- jumpered	Index to J1 connector
T	- jumpered	Drive Ready enabled after time delay.
C	- open	Seek Complete to J2 connector only
SC	- jumpered	Sector to J1 connector
BC	- open	no Byte Clock on J1
LSB	- jumper 1,4,16,64,128	60 Sectors/track
MSB	- jumper 512,1024,2048	60 Sectors/track
D	- open	Stepper Motor always enabled
E	- jumpered	Stepper Motor always enabled
S1	- open	Sector/Index generated simultaneously

Control PCB (continued)

J1 = 50 pins J2 = 20 pins

S2	- jumpered	Sector/Index generated simultaneously
4H	- shunt removed	R/W on radial cable only Seek Complete on radial cable

E1,E2,E3 - don't care

R	- jumpered	
S	- open	
F	- open	
SL	- jumpered	Status signals only when drive is selected

Data Separator PCB

C	- jumpered	sync on zeros field
D	- open	sync on zeroes field

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