SID-ADV11

Analog-to-Digital Converter

Installation Guide

Σ Sigma Information Systems

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ANAHEIM, CALIFORNIA - JULY 1987

MA400555 REV C

Contents

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ANALOG-TO-DIGITAL CONVERTER

USER'S GUIDE

1. INTRODUCTION

This User's Guide provides the information necessary to configure and calibrate the SID-ADV11 Analog-to-Digital converter manufactured by Sigma Information Systems in Anaheim, California. A general description and specifications of the module are included.

1.1. General Description

The SID-ADV11 is a 12-bit successive approximation analog-to-digital converter that samples analog data at specified rates and stores the digital equivalent value for processing. A multiplexer section can accommodate up to 32 single-ended or 32 quasi-differential or 16 full differential inputs.

A to D conversions are initiated by program command, clock overflow, or external events. The program control is determined by the control and status register (CSR). The clock overflow command is supplied by the LTC or the KWV11-A option. External event inputs can originate at the user's equipment or from the Schmitt trigger output on the KWV11-A clock. The digital data output is routed through a buffer register to the bus, from which it can be transferred into memory. This buffer optimizes the throughput rate of the converter.

1.2. Features

* 32 channel multiplexer
* Sample and hold function
* Buffered data output
* Sample or presample modes
* Offset binary or 2's complement data format
* Single ended, Quasi-differential (32 channel)
* Full differential format (16 channel)
* +5 volt only power required
* Selectable CSR address
* Selectable interrupt vector
* Selectable interrupt priority
* Dual wide board
* Patterned after DEC's ADV11-A and C

REF: ADV11A.WPS/DM4

2. SPECIFICATIONS

2.1. Analog Input Specifications

Number of Inputs	32 single ended, 16 differential, or 32 quasi-differential
Input Voltage Range	-10V to +10V, -5V to +5V, 0V to +10V. Alternate model available with 5.12V and 10.24V ranges
Input overvoltage protection	± 35V
Input clamp voltage	± 12V
Input Impedance (dynamic)	Shunt Resistance 100 megohms Shunt Capacitance 25 pF max Series Resistance 1000 ohms

2.2. ADC Conversion Specification

Accuracy	Resolution 12 bits System accuracy ±0.030% of FSR
Stability Temperature coefficient	±35 PPM/degree C
Conversion time	25 microseconds

2.3. Sample and Hold

Sample time (sample mode)	30 microseconds
Aperture uncertainty	15 ns
Cross talk	> 80db down at 1KHZ

2.4. Digital Input Specifications

Input low level	0.0 to +.7 volts
Input high level	+2.0 to +5.0 volts
Input current (low)	-.4 MA @.4 volts
Input current (high)	20 uA @2.7 volts
Logic input rise time	400 nanoseconds (MAX)

2.5. Q Bus Interface Specifications

CSR	Switch selectable 170000 to 177774
DBR	CSR address +2
VECTOR	Switch selectable 100 to 740

2.6. Control/Status Register (CSR)

BIT	MNEMONIC	DESCRIPTION
0	A/D START	Conversion start control
1.2.3.13		Not used
4	EXT TRIGGER	When set, this bit allows an external trigger to start an A/D conversion. Read/Write
5	RTC ENB	When set, this bit allows a real time clock (BEVNT) to start an A/D conversion. Read/Write
6	DONE INT ENB	When set, this bit enables an interrupt on A/D DONE (bit 7). Both bits are cleared by INIT. Read/Write
7	A/D DONE	This bit is set at the end of an A/D conversion; reset by reading A/D data buffer register (DBR). Read only
8-12	MUX ADDR	These bits select 1 of 32 channels. Read/Write
14	ERROR INT	When set, this bit enables an interrupt on an ERROR (bit 15). Both bits are cleared by INIT. Read/Write
15	ERROR	When set, this bit indicates that an error has occurred due to one of the following. This bit is cleared by wirting the CSR or by INIT. Read only.

- o Trying a start during an A/D conversion.
- o Reading DBR register without the DONE status set.
- o A/D conversion completion with DONE status set.

2.7. Data Buffer Register (DBR) - Read Only

BIT	DESCRIPTION
0-10	ADC conversion value
11	Sign bit for offset binary format
12-15	Always zero for offset binary format
11-15	0 = positive value of 2's complement format 1 = negative value of 2's complement format

2.8. J1 Edge Connector Pinouts

1 = GND	12 = CH 15	21 = CH 20	30 = CH 2
2 = PSUEO DIFF IN	13 = CH 22	22 = CH 4	31 = CH 26
5 = CH 24	14 = CH 6	23 = CH 28	32 = CH 10
6 = CH 8	15 = CH 30	24 = CH 12	33 = CH 17
7 = CH 32	16 = CH 14	25 = CH 19	34 = CH 1
8 = CH 16	17 = CH 21	26 = CH 3	35 = CH 25
9 = CH 23	18 = CH 5	27 = CH 27	36 = CH 9
10 = CH 7	19 = CH 29	28 = CH 11	39 = GND
11 = CH 31	20 = CH 13	29 = CH 18	40 = EXTCLK

2.9. Operating Temperature 0° to 70°C

3. INSTALLATION

The SID-ADV11 installation consists of verifying and/or reconfiguring the module for DC voltage range, channel input parameters, data format and mode of operation.

3.1. Factory Configuration

The SID-ADV11 comes calibrated from the factory and configured as follows:

Analog input voltage range: ±5 volts full scale

Sample mode

Offset binary data format

32 channel single ended input

CSR address: 170400

Interrupt vector 400

Interrupt level: 4

The factory set configuration is shown in Figure 1. If reconfiguration is desired use the following paragraphs.

3.2. Reconfiguration

The factory configurations are shown in Figure 1. Use the following paragraphs if the SID-ADV11 must be reconfigured to meet user specifications.

3.2.1. Interrupt Level Jumpers, CSR/Vector Address Switches

The SID-ADV11A is shipped with interrupt level set at 7, vector address set at 400 (octal) and CSR address set to 178400 (octal). These parameters can be changed by reconfiguring jumpers W4-W7 and/or switches SW1 or SW2 as described below.

The default CSR address 170400 selection is shown below, along with an example address selection of 175640.

	CSR ADDRESS BITS														
	21..12	11	10	9		8	7	6		5	4	3		2	1	0
CSR ADDRESS		SW1 POSITIINS														
		10	9	8		7	6	5		4	3	2		1		
170400	1..1	ON	ON	ON		OFF	ON	ON		ON	ON	ON		ON	0	0
175640	1..1	OFF	ON	OFF		OFF	OFF	ON		OFF	ON	ON		ON	0	0

OFF = 1, ON = 0

The vector interrupt level is selected by jumpers W4, W5, W6 and W7 as shown below.

INTERRUPT LEVEL	JUMPERS W4	W5	W6	W7
4 (LOWEST)	OUT	IN	IN	IN
5	OUT	OUT	IN	IN
6	OUT	OUT	OUT	IN
7 (HIGHEST)	OUT	OUT	OUT	OUT

Vector interrupt ranges from 000 to 740 (octal) in increments of 40. The default vector is 400 (octal). It is selected by switch SW2 as shown below.

	VECTOR INTERRUPT BITS								
	08	07	06	05	04	03	02	01	00
					ALWAYS 0				
VECTOR INTERRUPT	SW2 POSITIONS 1	2	3	4					
000	ON	ON	ON	ON	0	0	0	0	0
040	ON	ON	ON	OFF	0	0	0	0	0
100	ON	ON	OFF	ON	0	0	0	0	0
140	ON	ON	OFF	OFF	0	0	0	0	0
200	ON	OFF	ON	ON	0	0	0	0	0
240	ON	OFF	ON	OFF	0	0	0	0	0
300	ON	OFF	OFF	ON	0	0	0	0	0
340	ON	OFF	OFF	OFF	0	0	0	0	0
400	OFF	ON	ON	ON	0	0	0	0	0
440	OFF	ON	ON	OFF	0	0	0	0	0
500	OFF	ON	OFF	ON	0	0	0	0	0
540	OFF	ON	OFF	OFF	0	0	0	0	0
600	OFF	OFF	ON	ON	0	0	0	0	0
640	OFF	OFF	ON	OFF	0	0	0	0	0
700	OFF	OFF	OFF	ON	0	0	0	0	0
740	OFF	OFF	OFF	OFF	0	0	0	0	0

OFF = 1, ON = 0

3.2.2. Operating Parameters

In order to reconfigure operating parameters such as input range, sample/presample mode and data format, the cover shield must be removed. Use the following procedure to remove the shield and to reconfigure operating parameters.

1. Remove the analog shield from SID-ADV11 by removing the 4 (four) mounting screws.

2. Change the option jumpers to select the desired configuration using the following charts:

   Figure 2 +5 volt input range
   Figure 3 ±10 volt range
   Figure 4 0 to +10 volt input range
   Figure 5 32 channel single ended input
   Figure 6 32 channel Quasi-differential input
   Figure 7 16 channel full differential input
   Figure 8 Sample mode
   Figure 9 Presample mode
   Figure 10 Offset binary data format
   Figure 11 2's complement data format

3. Recalibrate if desired.

4. Replace analog shield.

5. Insert SID-ADV11 into 'Q' bus slot in system.

6. Connect appropriate input cable to J1.

7. Run system tests.

4. CALIBRATION

The following steps describe the procedure to do a full calibration adjustment on the SID-ADV11. Steps 1-11 are usually not critical and usually do not have to be redone from factory adjustments unless components are changed.

1. Remove analog shield cover by removing three (3) retaining screws.

2. Set up configuration jumpers as shown on Figure 12.

3. Place a digital voltmeter or scope at pin 2 of U37 (U37-2) and ground and adjust R21 so both that U37-2 and U37-3 measure approximately the same voltage (about zero millivolts).

4. Set up configuration jumpers as shown on Figure 13.

5. Place a digital voltmeter or scope at U38-2 and ground and adjust R22 so that both U38-2 and U38-3 measure approximately the same voltage (about zero millivolts).

6. Setup configuration jumpers as shown on Figure 15.

7. Run appropriate software to display ADC conversion value on the host terminal and adjust R16 for 0 volts conversion (4000 if configured for offset binary, 0000 if configured for 2's complement data format).

   NOTE: If R16 is out of zero adjustment range, use R15 to adjust to zero.

8. Setup configuration jumpers as shown on Figure 14.

9. Rerun appropriate software to display ADC conversion values on the host terminal and adjust R17 for 0 volts conversion (4000 if configured for offset binary, 0000 if configured for 2's complement data format).

   NOTE: Zero is the transition from -1 to 0 and zero adjustment should satisfactorily produce equal amounts of 0's and 1's.

10. Now configure the jumpers to the desired operational configuration.

11. Now replace analog shield and install in system without extender, turn power on and let system warm up for 30 minutes.

12. Connect a voltage standard to channel 1 and set voltage standard to 0 volts.

13. Run appropriate software to digitize and display channel 0 conversion value.

14. Set voltage standard to 0 volts and adjust R16 if configured for bipolar or R14 if configured for unipolar for 0 volts conversion.

    NOTE: Zero is the transition from -1 to 0 and zero adjustment should satisfactorily produce equal amounts of 0's and 1's.

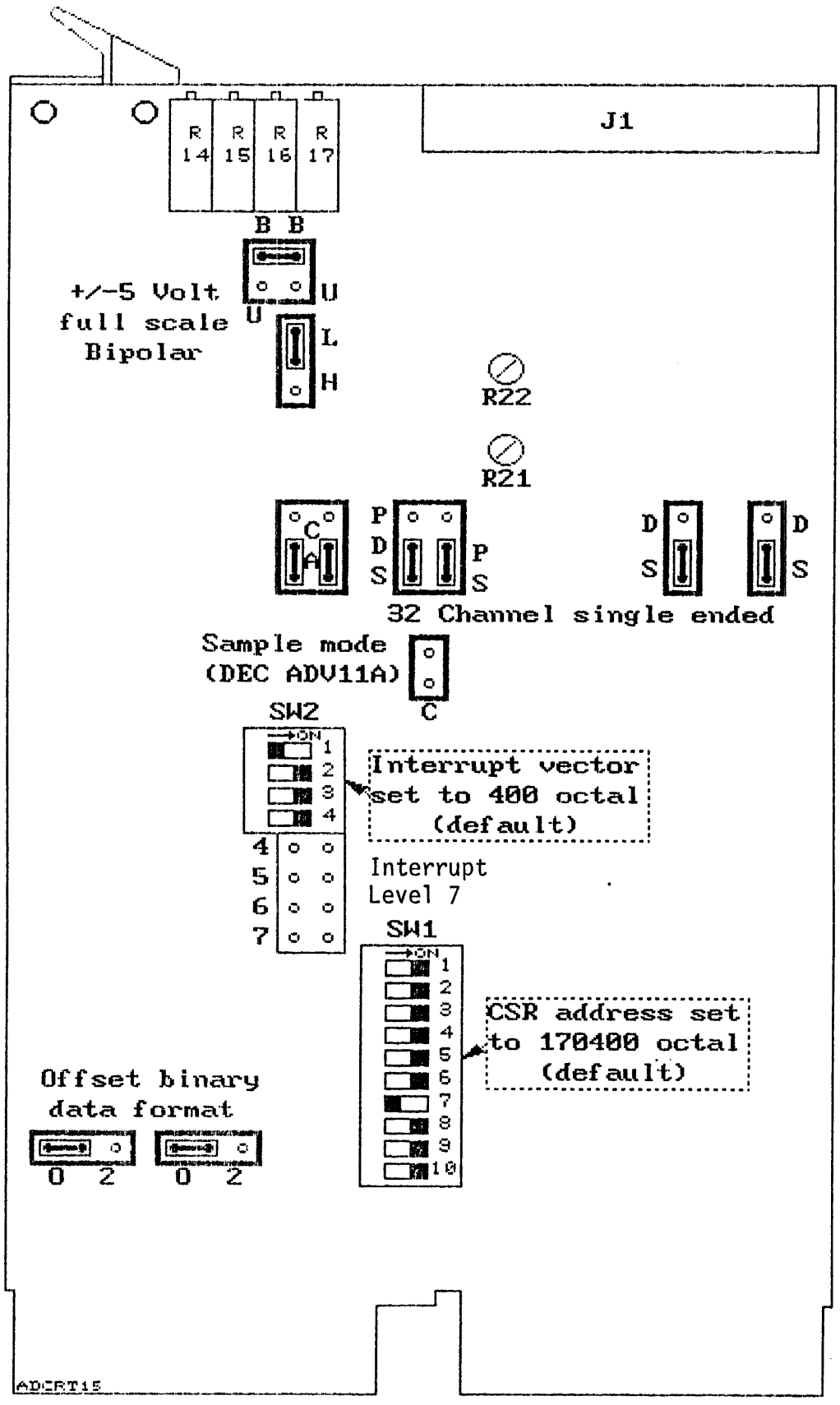
15. Change voltage standard for + full scale voltage and adjust R15 so that conversion value is just at full scale value.

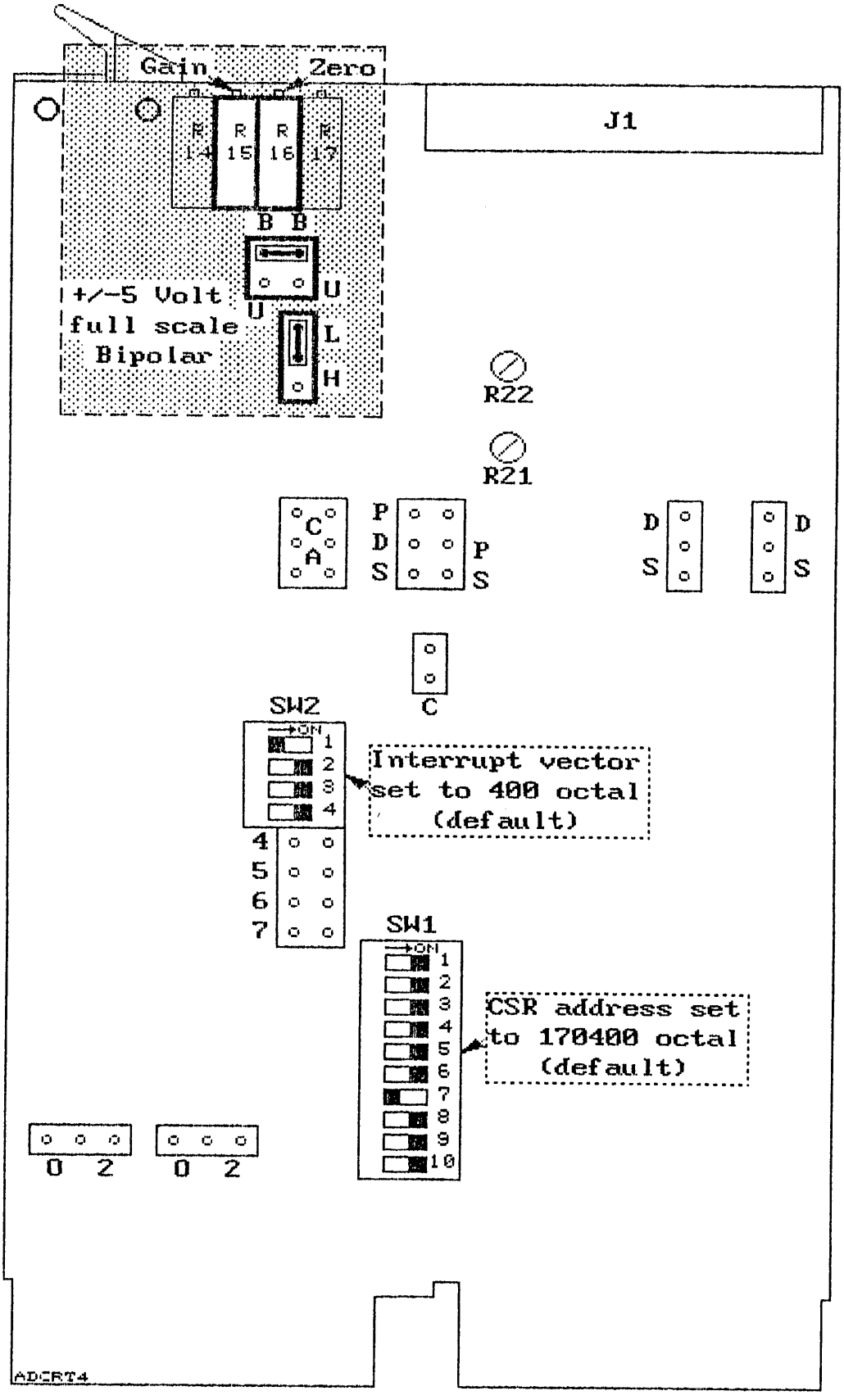
16. Loop alternately between the previous two steps until both adjustments are simultaneously correct.

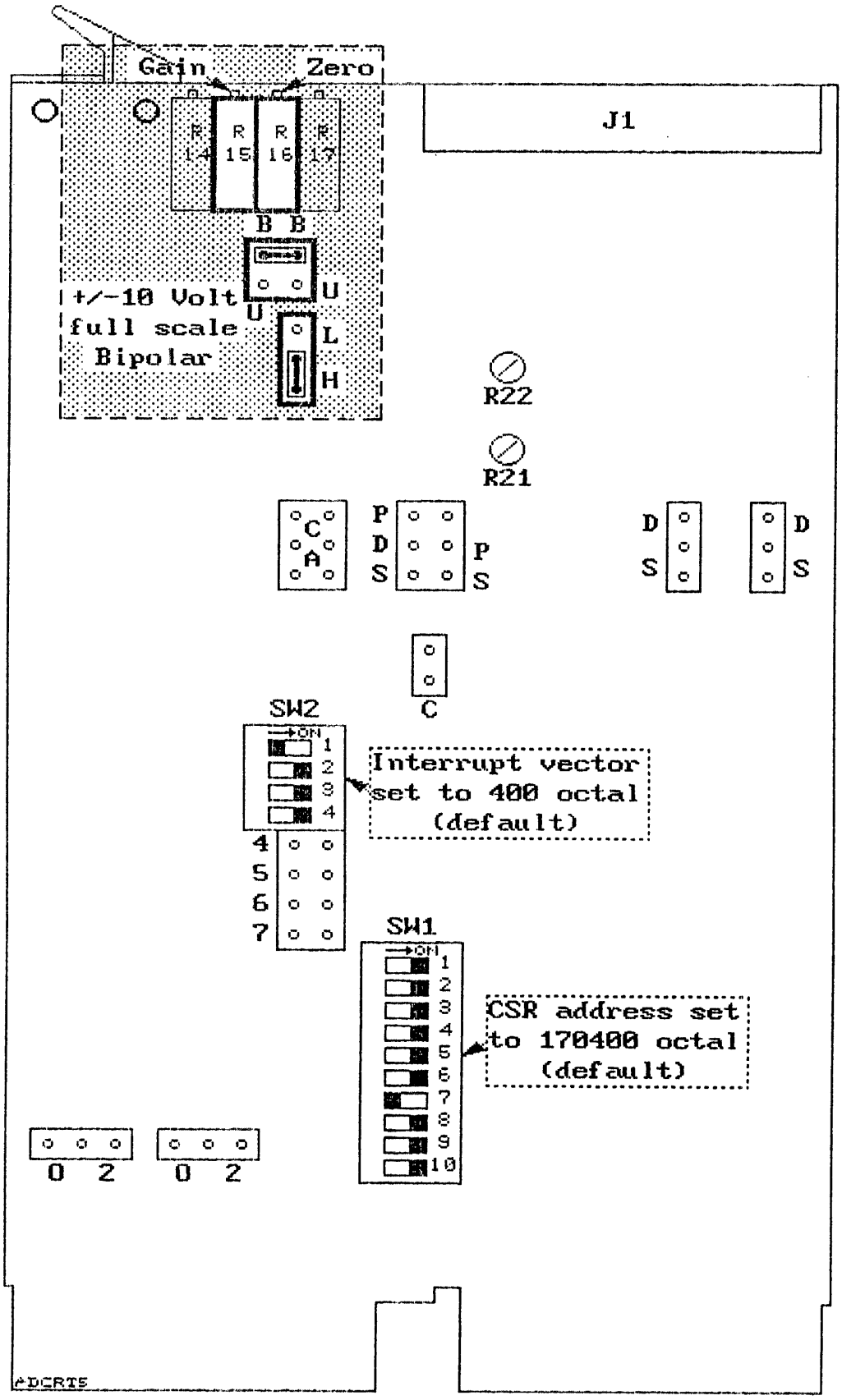
17. Now check minus full scale if configured for bipolar input and verify that the conversion value is minus full scale. (If it is off slightly, the previous adjustments can be fudged to balance the error among the full scale and zero data points.

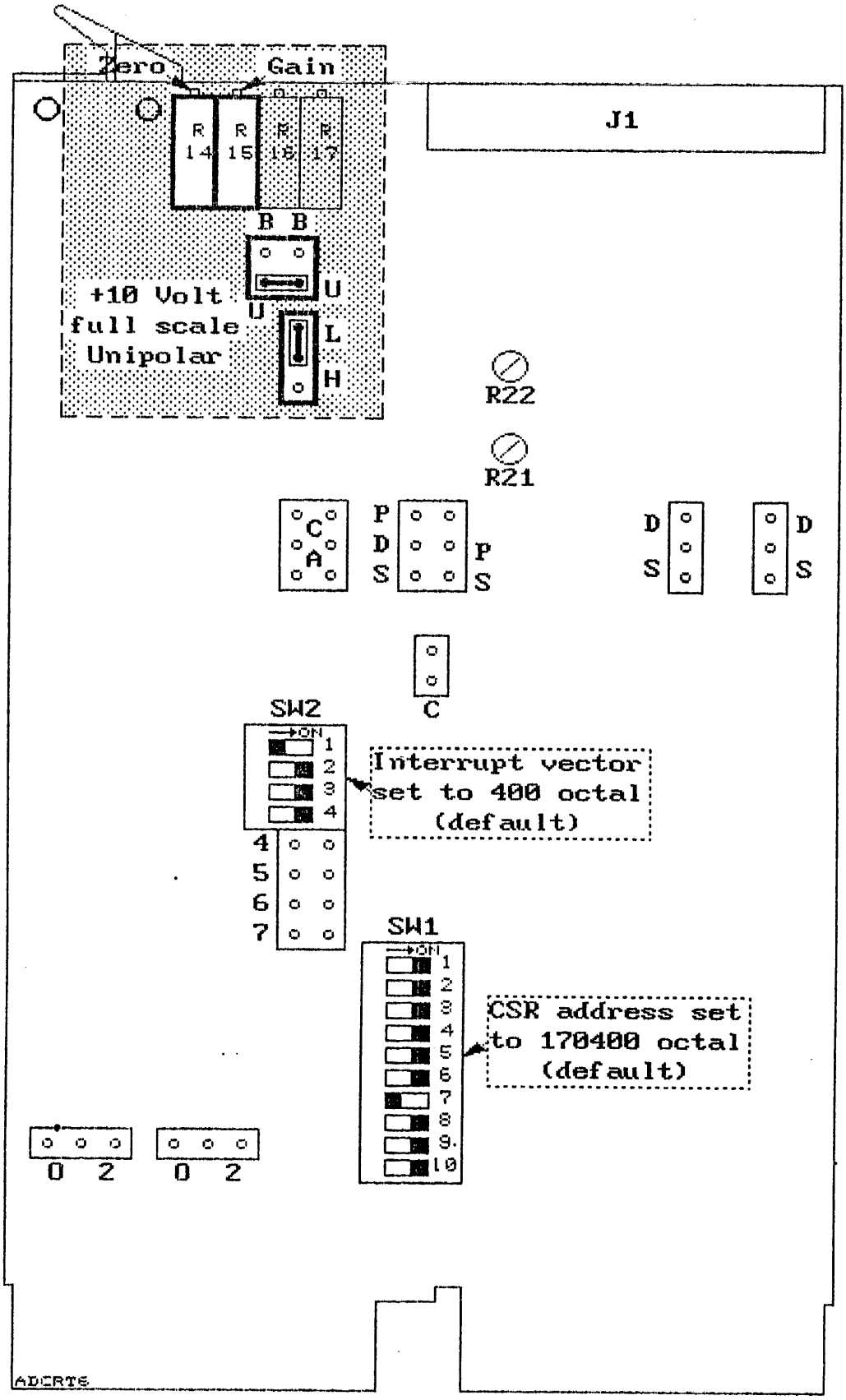
5. FIGURES

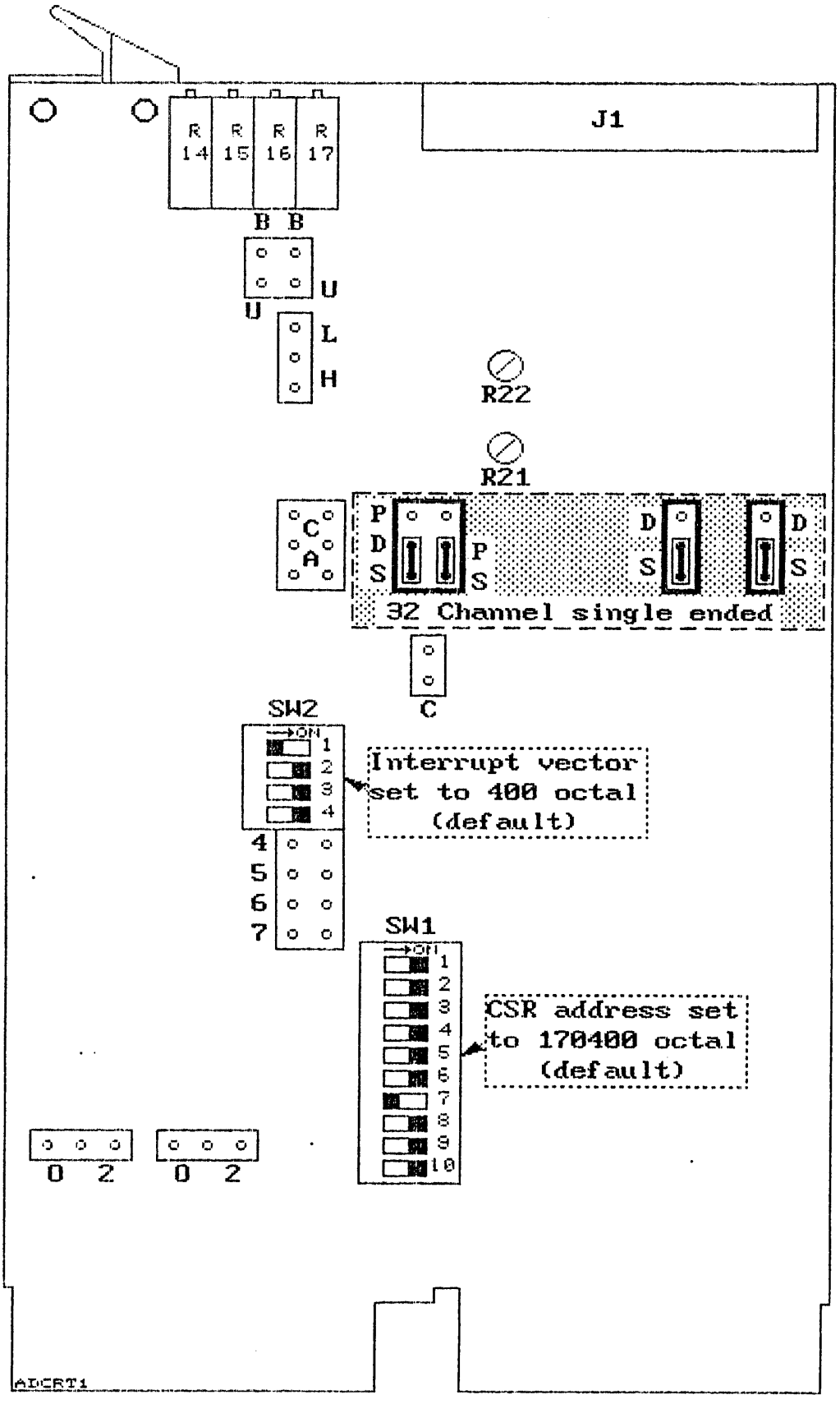
This section contains the figures that pertain to the various configurations and calibration procedures for the SID-ADV11.

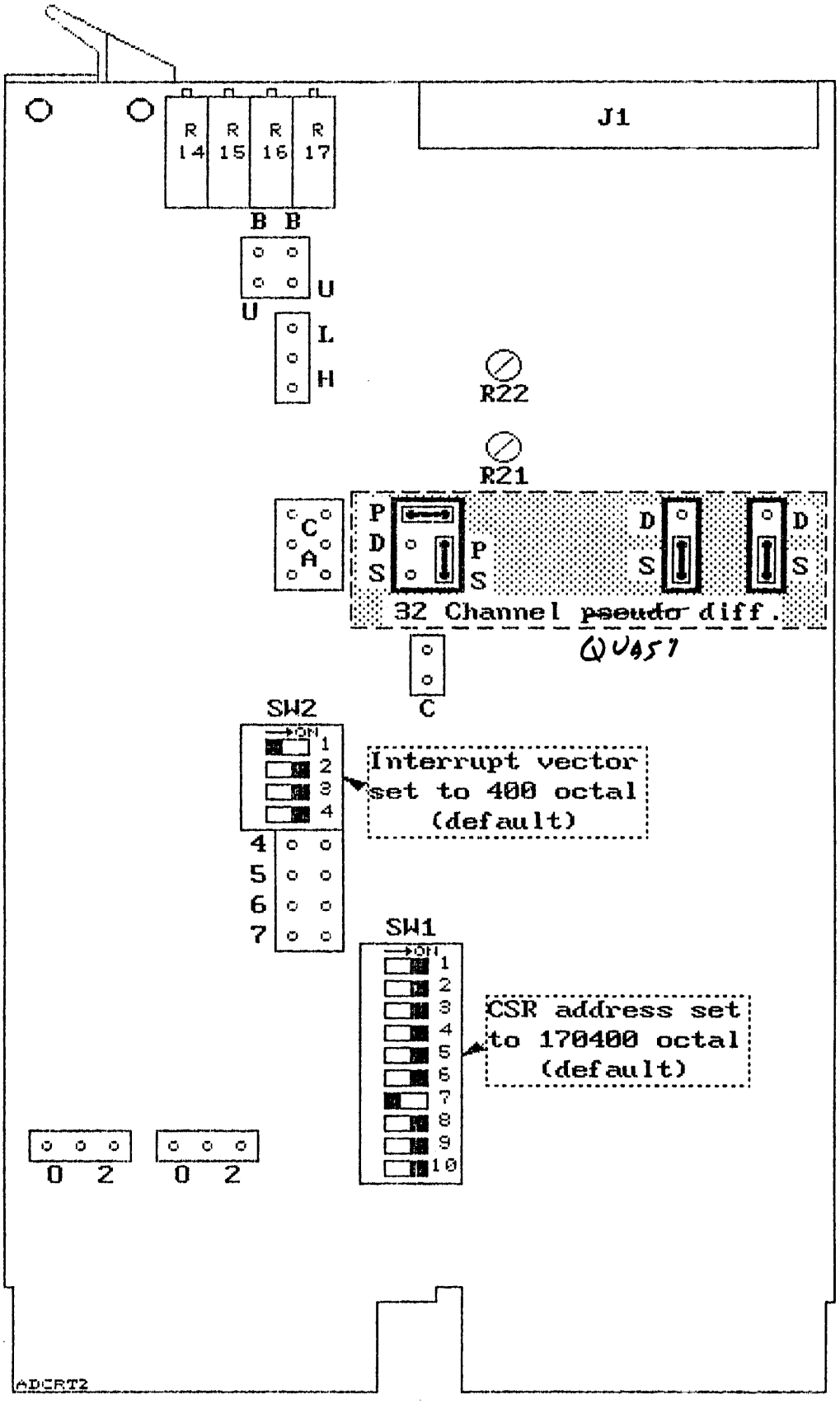

J1
R 14
R 15
R 16
R 17
B B
+/-5 Volt
full scale
Bipolar
U
U
L
H
R22
R21
C
A
P
D
S
P
S
D
S
D
S
32 Channel single ended
Sample mode
(DEC ADV11A)
C
SW2
ON
1
2
3
4
Interrupt vector
set to 400 octal
(default)
4
5
6
7
Interrupt
Level 7
SW1
ON
1
2
3
4
5
6
7
8
9
10
CSR address set
to 170400 octal
(default)
Offset binary
data format
0 2
0 2
ADCRT15

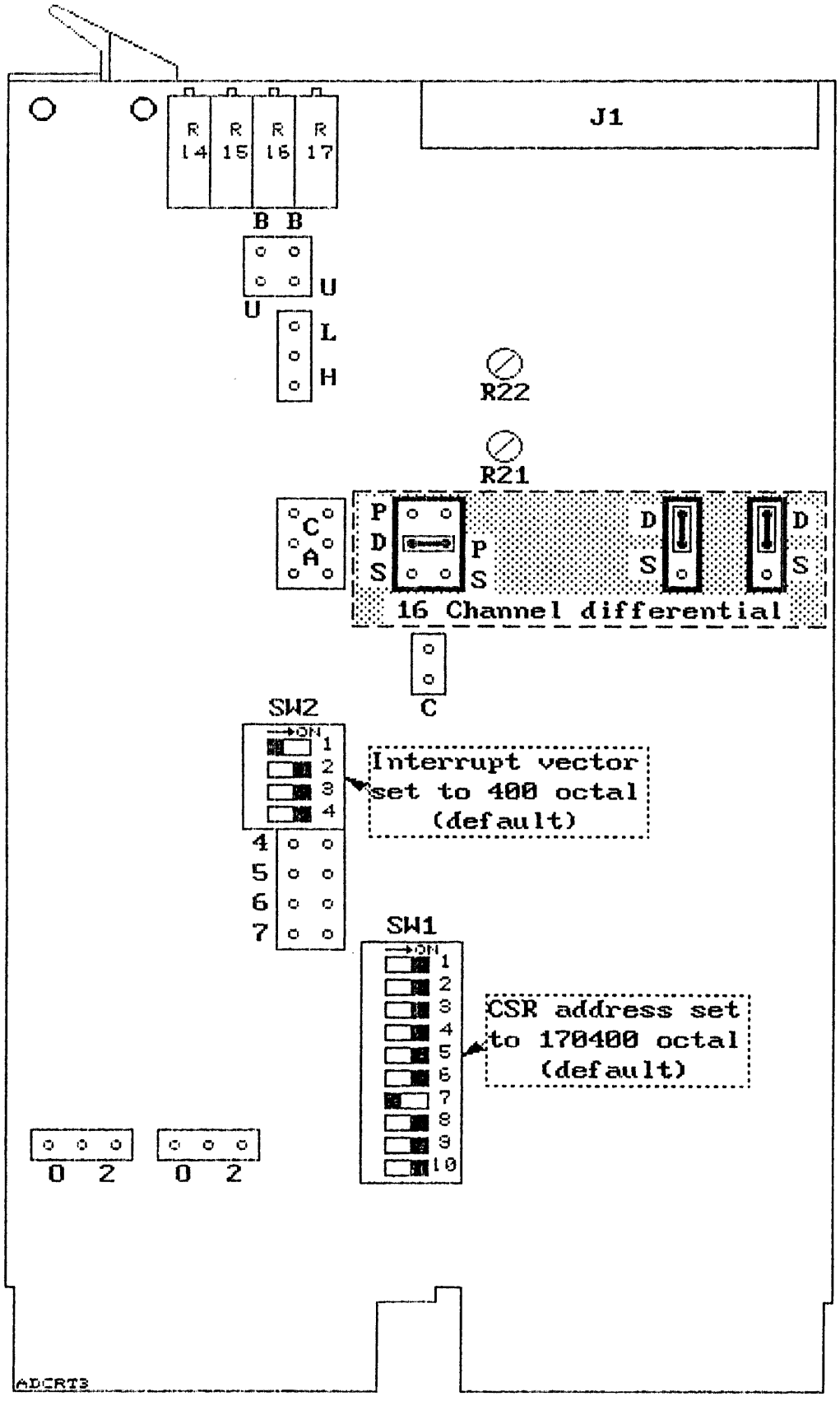

Gain
Zero
R 14
R 15
R 16
R 17
B B
U
U
+/-5 Volt
full scale
Bipolar
L
H
J1
R22
R21
C
A
P
D
S
P
S
D
S
D
S
C
SW2
ON
1
2
3
4
Interrupt vector
set to 400 octal
(default)
4
5
6
7
SW1
ON
1
2
3
4
5
6
7
8
9
10
CSR address set
to 170400 octal
(default)
0 2
0 2
ADCRT4

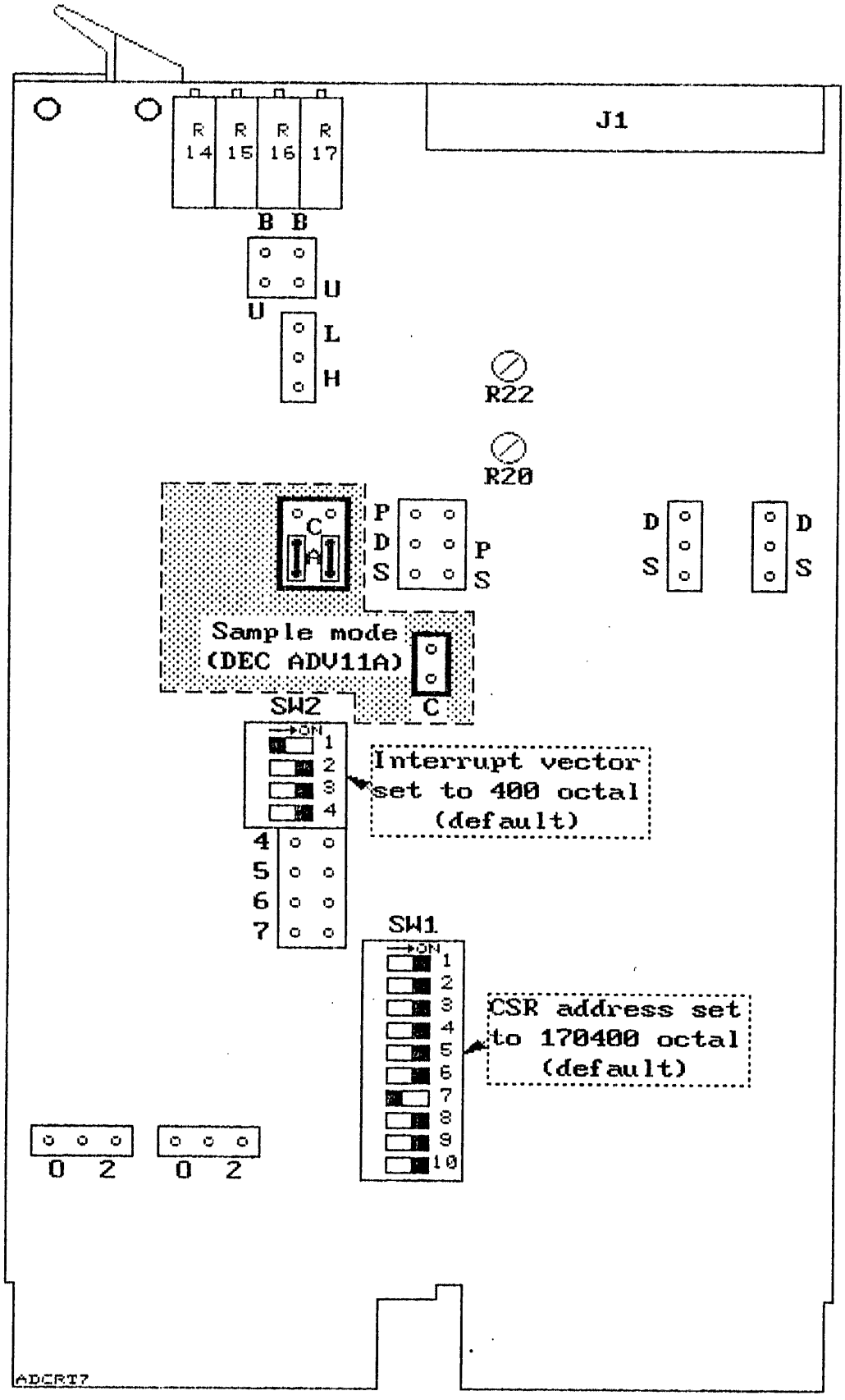

Gain
Zero
J1
R14
R15
R16
R17
B B
U
U
+/-10 Volt
full scale
Bipolar
L
H
R22
R21
C
A
P
D
S
P
S
D
S
D
S
C
SW2
ON
1
2
3
4
Interrupt vector
set to 400 octal
(default)
4
5
6
7
SW1
ON
1
2
3
4
5
6
7
8
9
10
CSR address set
to 170400 octal
(default)
0 2
0 2
DCRTS

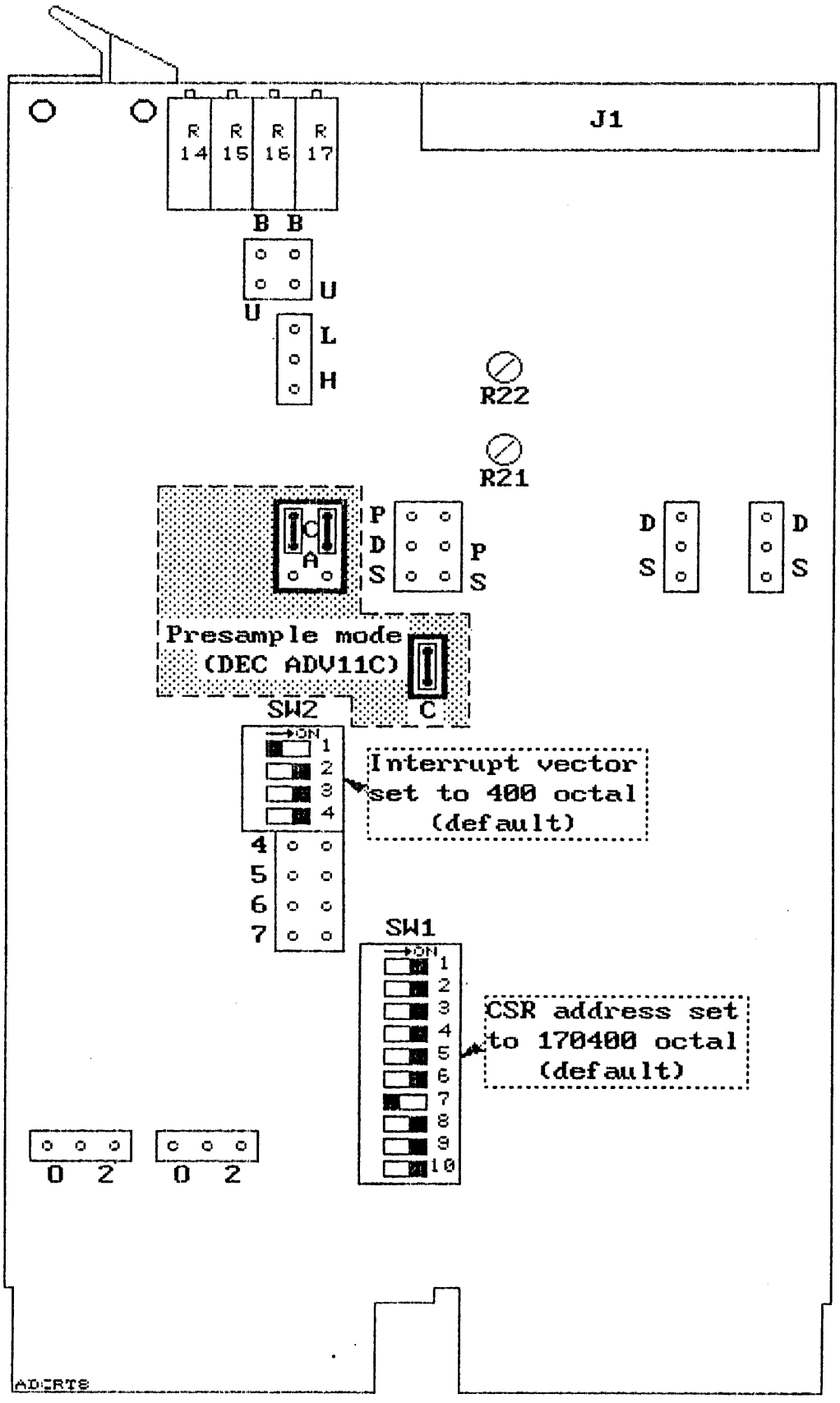

Zero
Gain
R 14
R 15
R 16
R 17
J1
B B
+10 Volt
full scale
Unipolar
U
U
L
H
R22
R21
C
A
P
D
S
P
S
D
S
D
S
C
SW2
ON
1
2
3
4
Interrupt vector
set to 400 octal
(default)
4
5
6
7
SW1
ON
1
2
3
4
5
6
7
8
9
10
CSR address set
to 170400 octal
(default)
0 2
0 2
ADCRTS

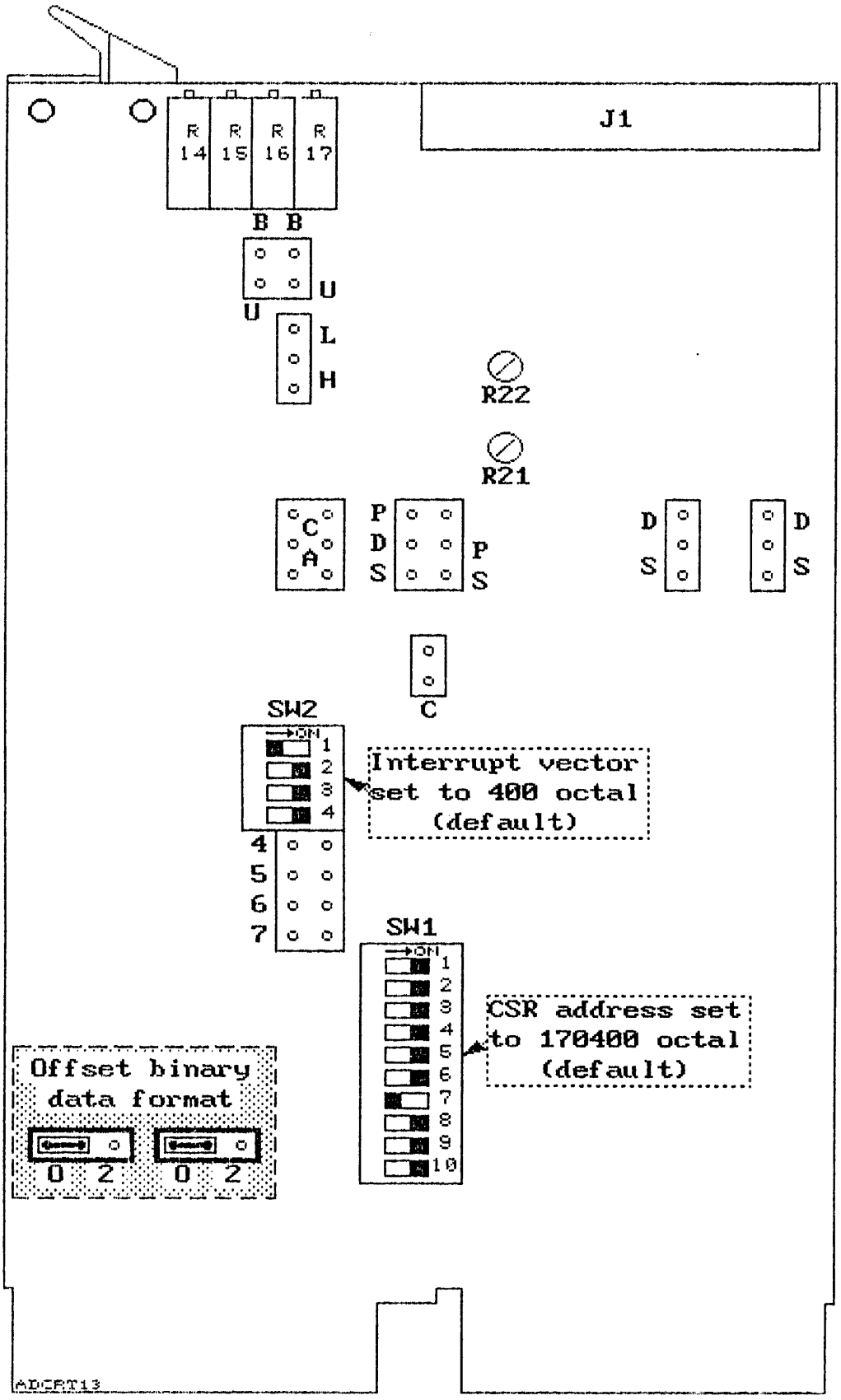

J1
R 14
R 15
R 16
R 17
B B
U
U
L
H
R22
R21
C
A
P
D
S
P
S
D
S
D
S
32 Channel single ended
C
SW2
ON
1
2
3
4
4
5
6
7
Interrupt vector set to 400 octal (default)
SW1
ON
1
2
3
4
5
6
7
8
9
10
CSR address set to 170400 octal (default)
0 2
0 2
AIDCRT1

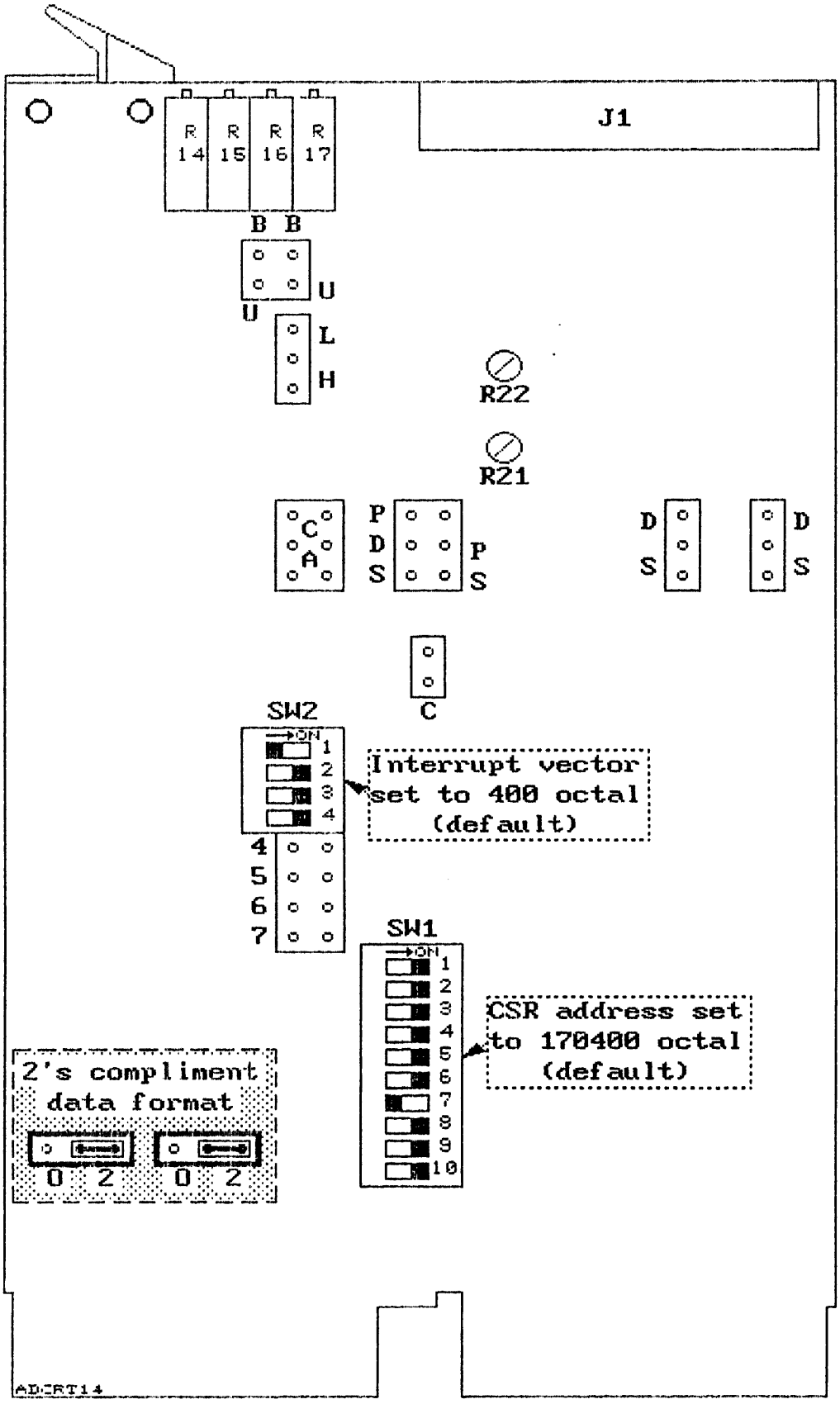

J1
R 14
R 15
R 16
R 17
B B
U
U
L
H
R22
R21
C
A
P
D
S
P
S
D
S
D
S
32 Channel pseudo diff.
QU457
C
SW2
ON
1
2
3
4
4
5
6
7
Interrupt vector set to 400 octal (default)
SW1
ON
1
2
3
4
5
6
7
8
9
10
CSR address set to 170400 octal (default)
0 2
0 2
ADCRT2

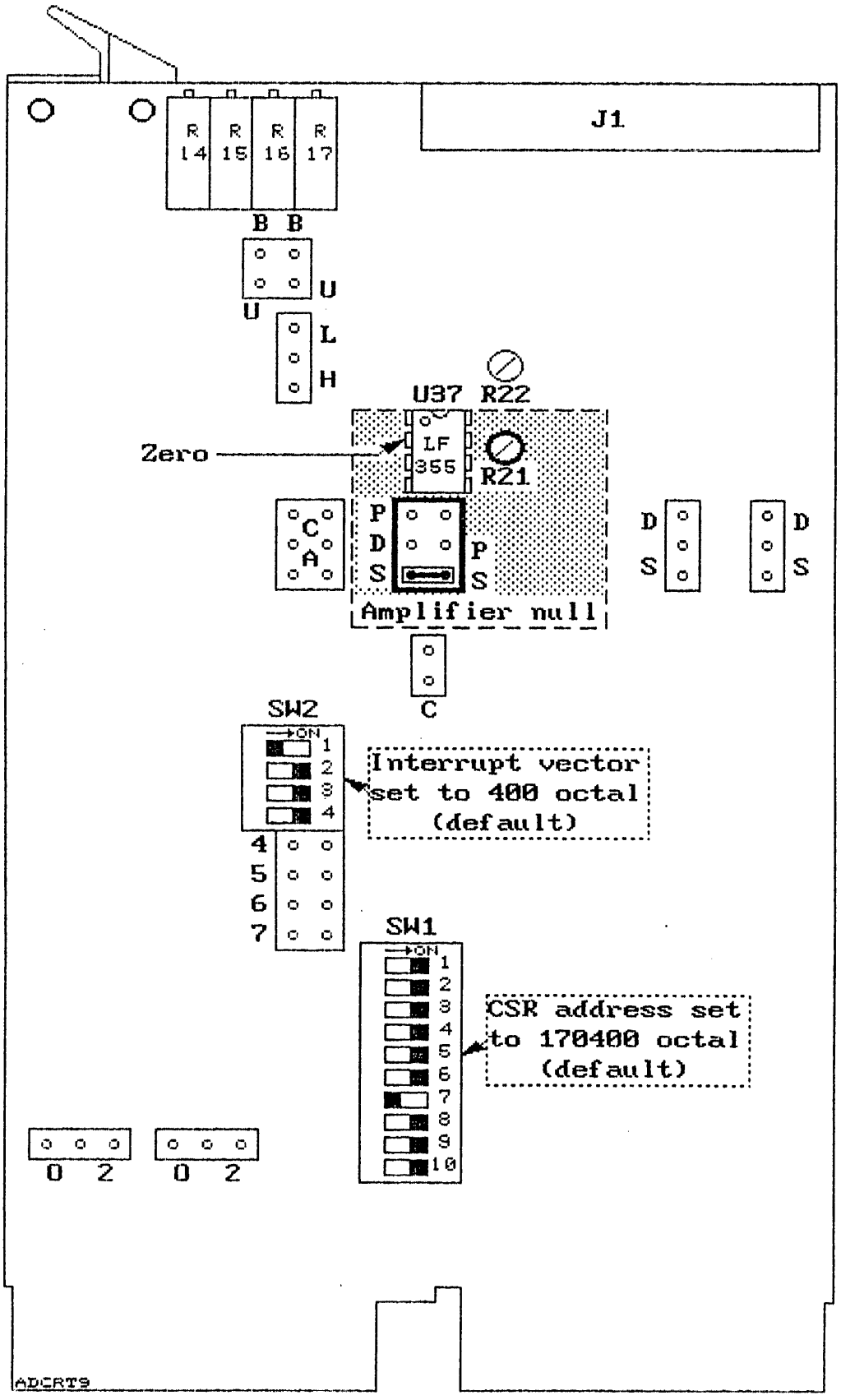

J1
R 14
R 15
R 16
R 17
B B
U
U
L
H
R22
R21
C
A
P
D
S
P
S
D
S
D
S
16 Channel differential
C
SW2
ON
1
2
3
4
Interrupt vector set to 400 octal (default)
4
5
6
7
SW1
ON
1
2
3
4
5
6
7
8
9
10
CSR address set to 170400 octal (default)
0 2
0 2
ADCRT3

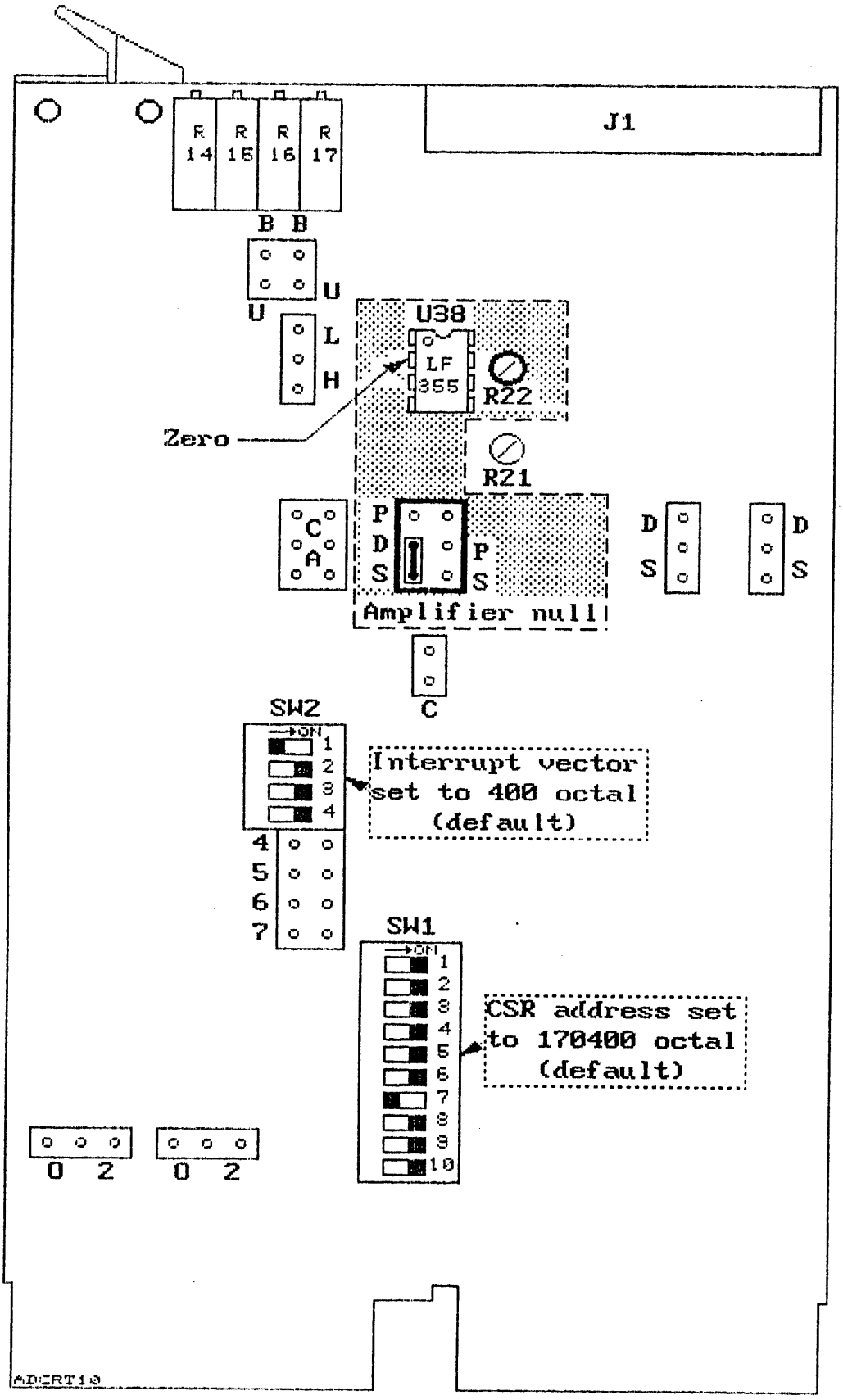

R 14
R 15
R 16
R 17
J1
B B
U
U
L
H
R22
R20
C
A
P
D
S
P
S
D
S
D
S
Sample mode
(DEC ADV11A)
C
SW2
ON
1
2
3
4
4
5
6
7
Interrupt vector
set to 400 octal
(default)
SW1
ON
1
2
3
4
5
6
7
8
9
10
CSR address set
to 170400 octal
(default)
0 2
0 2
ADCRI7

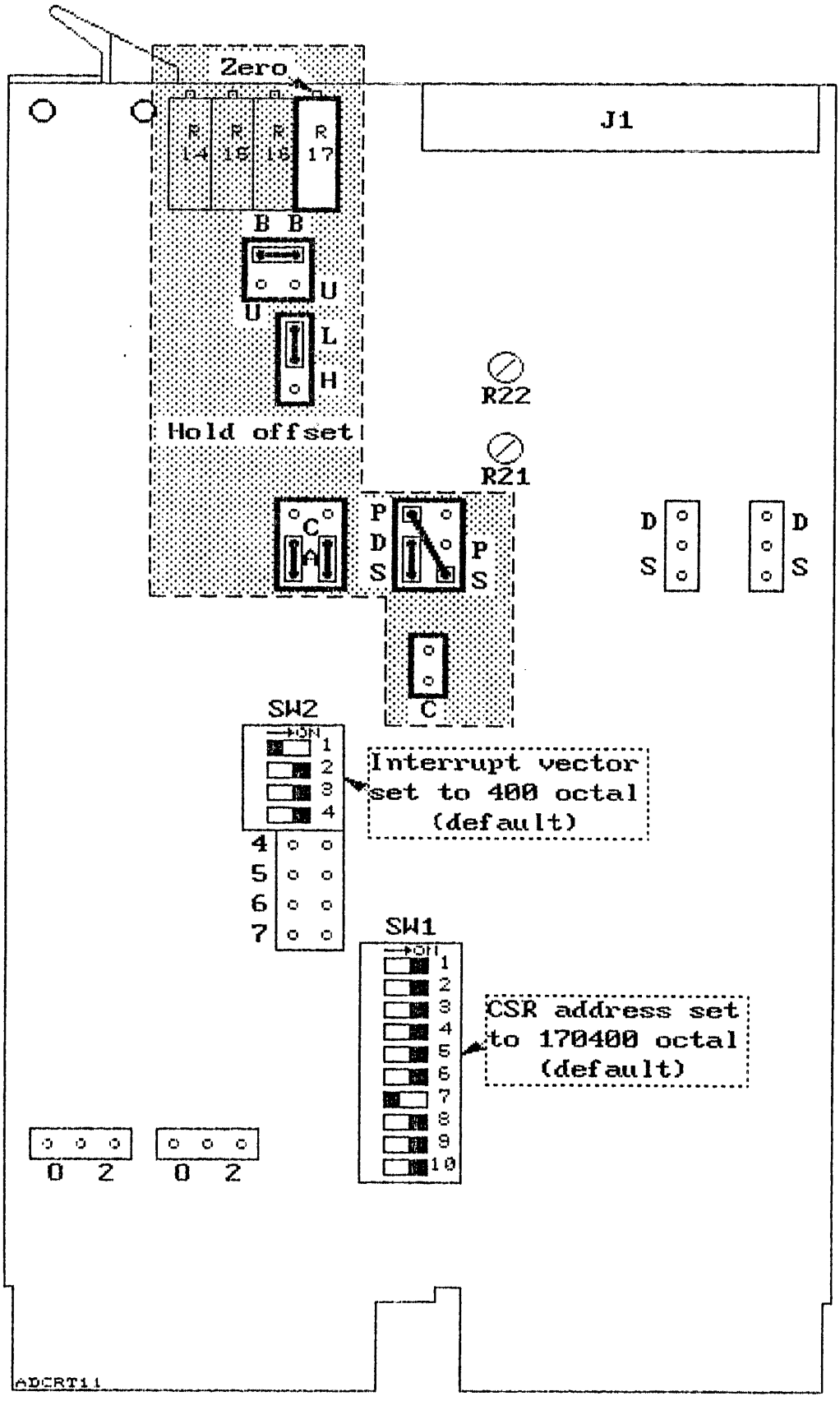

J1
R 14
R 15
R 16
R 17
B B
U
U
L
H
R22
R21
P
D
S
A
C
P
S
D
S
D
S
Presample mode
(DEC ADV11C)
C
SW2
ON
1
2
3
4
4
5
6
7
Interrupt vector
set to 400 octal
(default)
SW1
ON
1
2
3
4
5
6
7
8
9
10
CSR address set
to 170400 octal
(default)
0 2
0 2

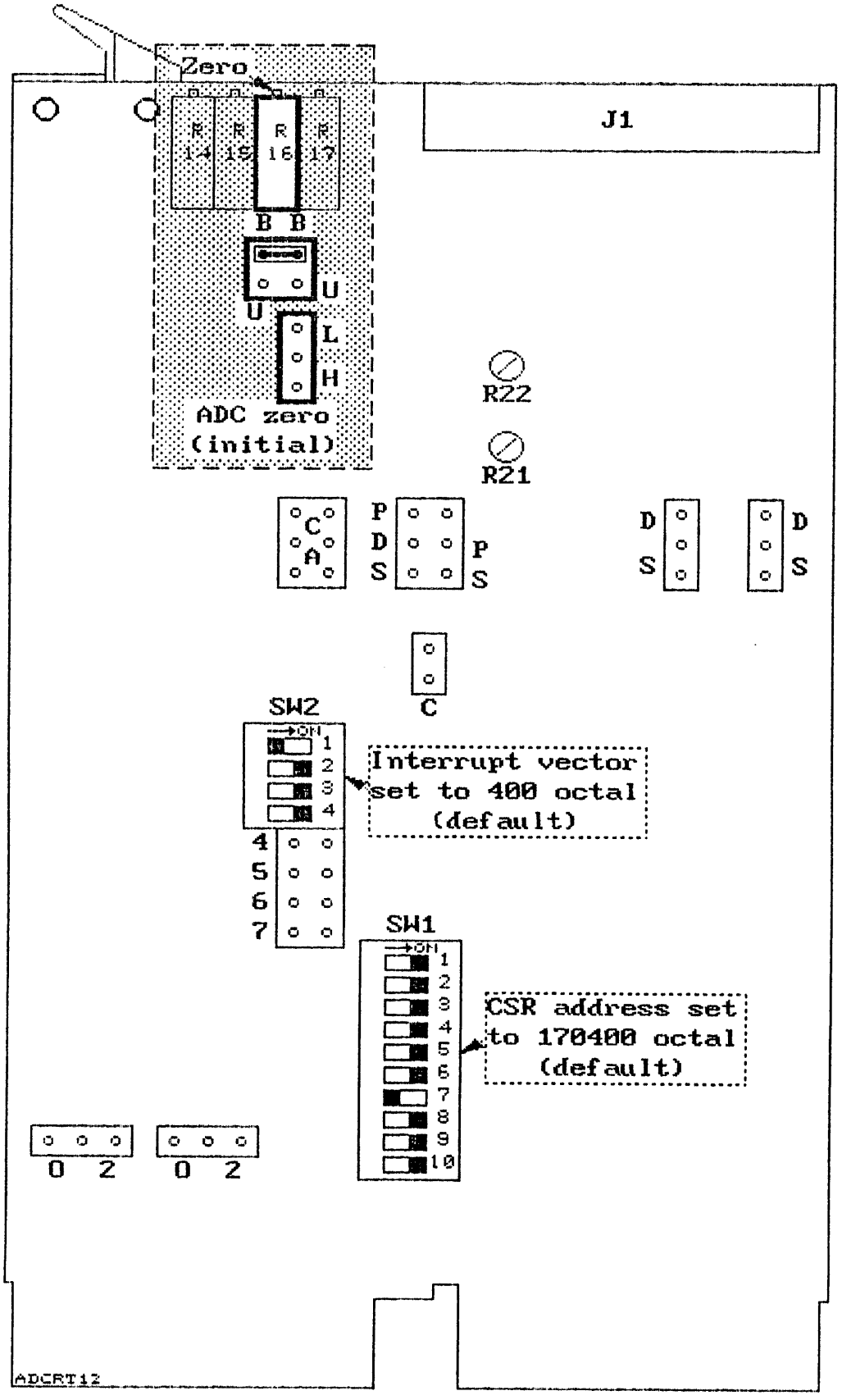

J1
R 14
R 15
R 16
R 17
B B
U
U
L
H
R22
R21
C
A
P
D
S
P
S
D
S
D
S
C
SW2
ON
1
2
3
4
4
5
6
7
Interrupt vector set to 400 octal (default)
SW1
ON
1
2
3
4
5
6
7
8
9
10
CSR address set to 170400 octal (default)
Offset binary data format
0 2 0 2
ADCRT13


J1
R 14
R 15
R 16
R 17
B B
U
U
L
H
R22
R21
C
A
P
D
S
P
S
D
S
D
S
C
SW2
ON
1
2
3
4
4
5
6
7
Interrupt vector set to 400 octal (default)
SW1
ON
1
2
3
4
5
6
7
8
9
10
CSR address set to 170400 octal (default)
2's compliment data format
0 2 0 2
AD-CRT14


J1
R 14
R 15
R 16
R 17
B B
U
U
L
H
U37
R22
LF 355
R21
Zero
P
D
S
C
A
Amplifier null
D
S
C
SW2
ON
1
2
3
4
Interrupt vector set to 400 octal (default)
4
5
6
7
SW1
CSR address set to 170400 octal (default)
0 2
0 2
ADCRT9


J1
R 14
R 15
R 16
R 17
B B
U
U
U
L
H
Zero
U38
LF 355
R22
R21
C
A
P
D
S
P
S
D
S
D
S
Amplifier null
C
SW2
ON
1
2
3
4
4
5
6
7
Interrupt vector set to 400 octal (default)
SW1
ON
1
2
3
4
5
6
7
8
9
10
CSR address set to 170400 octal (default)
0 2
0 2
AD:CRT10


Zero
R 14
R 15
R 16
R 17
J1
B B
U
U
L
H
Hold offset
R22
R21
C
P
D
S
P
S
D
S
D
S
C
SW2
ON
1
2
3
4
4
5
6
7
Interrupt vector set to 400 octal (default)
SW1
ON
1
2
3
4
5
6
7
8
9
10
CSR address set to 170400 octal (default)
0 2
0 2
ADCRT11


Zero
R 14
R 15
R 16
R 17
B B
U
U
L
H
ADC zero (initial)
J1
R22
R21
C
A
P
D
S
P
S
D
S
D
S
C
SW2
ON
1
2
3
4
Interrupt vector set to 400 octal (default)
4
5
6
7
SW1
ON
1
2
3
4
5
6
7
8
9
10
CSR address set to 170400 octal (default)
0 2
0 2
ADCRT12