sun microsystems

Field Service Manual
for the Sun-3/160 Workstation

Part Number 800-1258-05
Revision: 50 of 15 January 1986
Class 2

Credits and Trademarks

CAUTION

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are design to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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Preface

This manual is intended to provide information to aid field service engineers in board level troubleshooting and installation of field replaceable units for the Sun-3/160M, Sun-3/160C, and Sun-3/160G Workstation.

It is assumed that the reader is familiar with Transistor to Transistor Logic (TTL) and Emitter Coupled Logic (ECL), and with the Motorola MC68020 Microprocessor. The reader should also understand local area networks, Sun-3 virtual memory management architecture, and the VMEbus specification.

Summary of Contents

The contents of this manual are organized in this way:

Chapter 1 — *Sun-3/160 Functional Overview* — Provides a basic understanding of major component function and the interaction between those functional blocks, and defines differences and similarities between the Sun-3 models.

Chapter 2 — *Diagnostics and Troubleshooting* — provides troubleshooting and diagnostic information to aid in board level fault isolation.

Chapter 3 — *Component Removal and Replacement* — describes how to remove and replace printed circuit boards, the power supply, fans, and other subassemblies.

Appendix A — *Backplane Configuration* — provides backplane jumpering and slot designation information required for installation and configuration of additional printed circuit boards.

Appendix B — *PC Board Connector Pinouts* — gives pinouts for the CPU and SCSI board connectors.

Appendix C — *Degaussing the Monitor* — provides procedures for degaussing the monitor to remedy color distortion.

Appendix D — *Power Supply Voltage Adjustment* — shows location of DC output voltage adjustment potentiometers and terminal designations.

Appendix E — *ASCII/Hex Conversion Chart* — provides the hexadecimal equivalent of basic ASCII characters for use in EEPROM programming.

Applicable Documents

We emphasize that this manual outlines rather than exhausts many of the topics contained within. References to applicable documents are listed below, however, and we urge you to read these documents should you need further information.

Table 1 *Documentation*

Part Number	*Description*
800-1150	System Administration for the Sun Workstation
800-1314	Hardware Installation Manual for the Sun-3/160
800-1317	Installing UNIX on the Sun Workstation
800-1361	Sun Diagnostics Manual
813-1000	Sun Hardware Options Guide
813-2000	Sun Configuration Procedures
MC68020UM(ADI)	Motorola 68020 CPU Manual
MVMEB.7/D2	VMEbus Specification Manual, Rev. C, Feb. 1985
	SCSI Bus Specification
	Intel 82586 Ethernet Data Link Controller Technical Manual
	HM-4619 Color Monitor Installation, Operation and Maintenance Guide
	19" Video Display Unit, Model M19P114A/5102 Service/Operator Manual,Phillips Electronics Ltd., Video Display Products

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Sun-3/160 Functional Overview

1

Sun-3/160 Functional Overview

This chapter describes the function of the basic Sun-3/160M, Sun-3/160C and Sun-3/160G components and their interaction. The physical appearance of models 160M,160C and 160G Workstations are identical, with the exception of hardware present in the Sun-3/160C that relates to the function of the color monitor, and in the Sun-3/160G that relates to the gray scale monitor.

The three models are therefore treated as one in this manual. Subsections that deal with components present only in the Sun-3/160C and 160G, such as the color video board, are included under headings such as *The 160C/160G Color Video Board.*

The Sun-3/160M, Sun-3/160C, and Sun-3/160G are all stand-alone workstations that include a 19-inch monitor, keyboard and mouse, and a deskside pedestal that houses the microcomputer, memory subsystem, power supply, and associated circuitry. Each model can function as a node in a local area network.

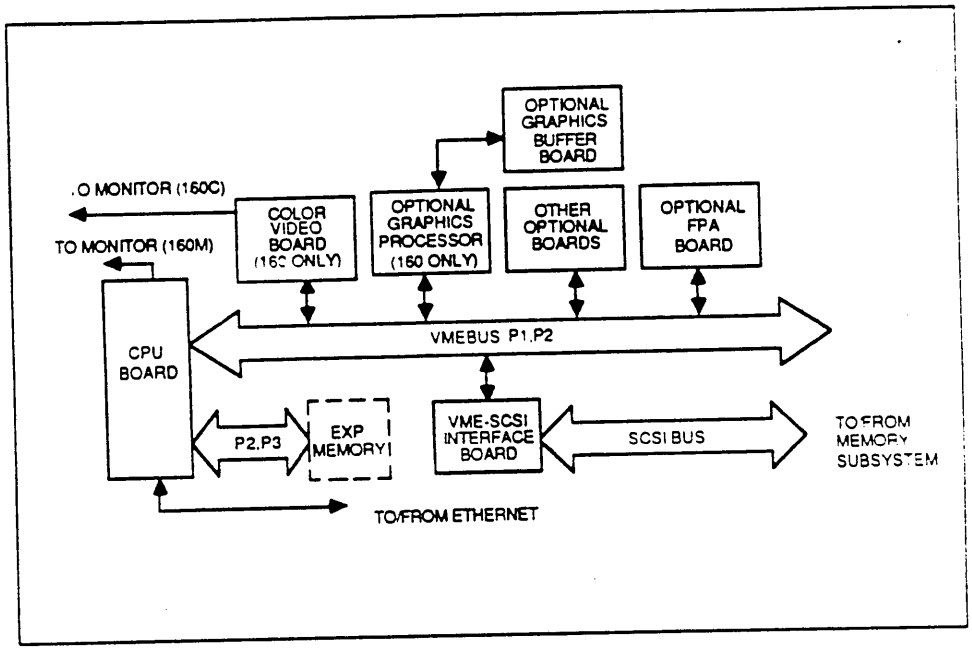
The list of applicable documents at the front of this manual refers to other sources of theory on components that are briefly described in this chapter.

This overview begins with the microcomputer boards that are housed in the 12-slot VME card cage inside the desk-side pedestal. The CPU and memory expansion boards are the heart of Sun-3 architecture, and are discussed first. Optional boards and the remaining major workstation subassemblies are described next.

Figure 1-1 illustrates the relationship of the components discussed in this chapter, which are presented in this order:

- CPU board
- VME Implementation
- Memory Expansion Board
- Color Video Board
- VME SCSI Board
- VME/Multibus Adapter Board
- VME/VME Adapter Board
- Optional Graphics Processor Board
- Optional Graphics Buffer Board
- Memory Subsystem (Mass Storage and Interfaces)
- Power supply and Monitors

Figure 1-1 *System Level Block Diagram*



1.1. The 2060 CPU Board

The 2060 board is a single board computer that is housed in a 12-slot card cage inside the pedestal. Appendices A and B provide information on physical characteristics of the and backplane CPU board connectors.

The board can be divided into functional blocks that are interconnected by the bus structure, as illustrated in Figure 1-2. Main 2060 board components are the MC68020 CPU, four Megabtyes of RAM, and interface circuitry that supports the VMEbus, Ethernet and serial ports.

This text provides a functional overview of these blocks in this order:

- CPU Board Overview
- Bus Architecture
- CPU/DVMA Devices
- Memory Management Unit (MMU)
- Main Memory
- Video Control Circuitry
- Serial Interface logic
- Ethernet Interface logic
- VME Interface logic

Figure 1-2 *CPU Board Overview*

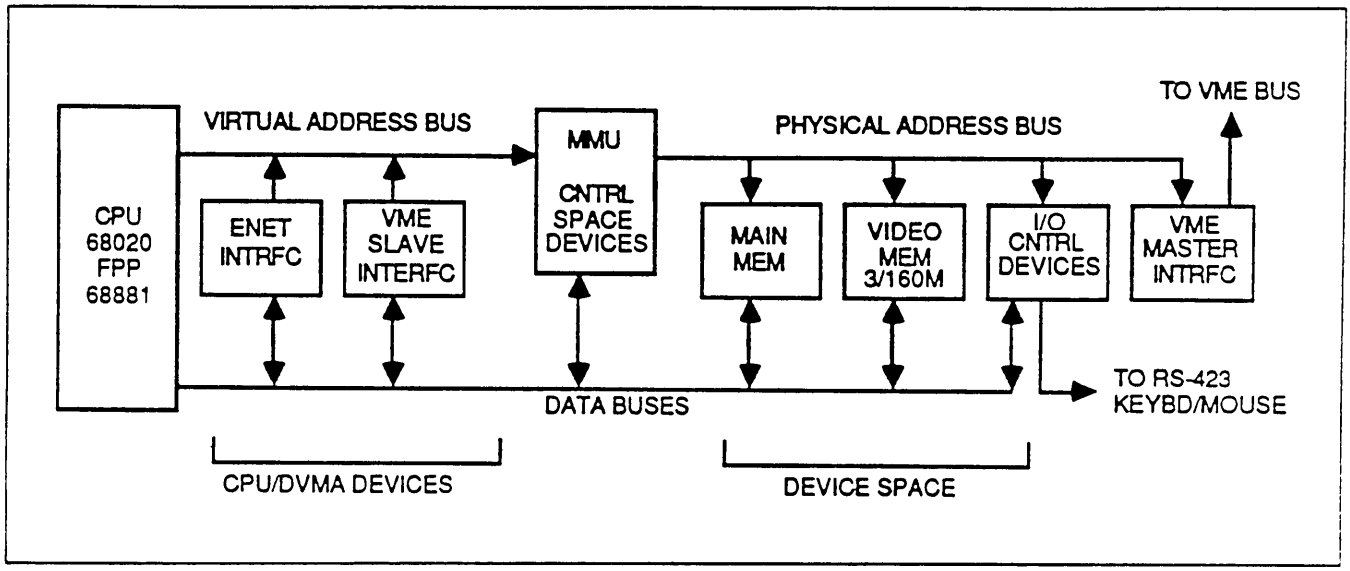


Figure 1-2 is a simplified block diagram of the 2060 CPU board. The CPU and DVMA devices depicted on the left side of the diagram supply virtual addresses to the MMU and arbitrate for control through the DVMA controller.

The MMU and control space devices (in the center of the diagram) are accessed in Function Code 3 space. Processor function codes further define virtual addresses and provide additional available address space.

The control space devices include processor extensions such as the bus error register, the system enable register, the diagnostic register, and the ID PROM.

The ID PROM stores basic information on the machine type; the node's unique 48-bit Ethernet address; a unique serial number for software licensing and distribution, the date the PROM was generated; and a checksum.

The MMU translates the virtual addresses into physical addresses to provide access to devices such as main and video memory, the VMEbus master interface, and I/O. It protects and manages these devices, and allows them to be shared.

The device space is divided into four types:

Type 0 — for main and video memory

Type 1 — for I/O and control devices (listed in MMU section)

Type 2 and 3 — for the VME master interface

2060 Bus Architecture

Figures 1-3 and 1-4 provide detailed diagrams of CPU board buses. The VMEbus interface is described in paragraphs following the Ethernet Interface subsection.

Data Buses

The 2060 board uses a 32-bit bus and two 8-bit buses for on-board data transfer. The 32-bit (P2) data bus provides a high-bandwidth path between both the CPU and DVMA devices and main memory. Two separate 8-bit buses segregate MOS and TTL devices.

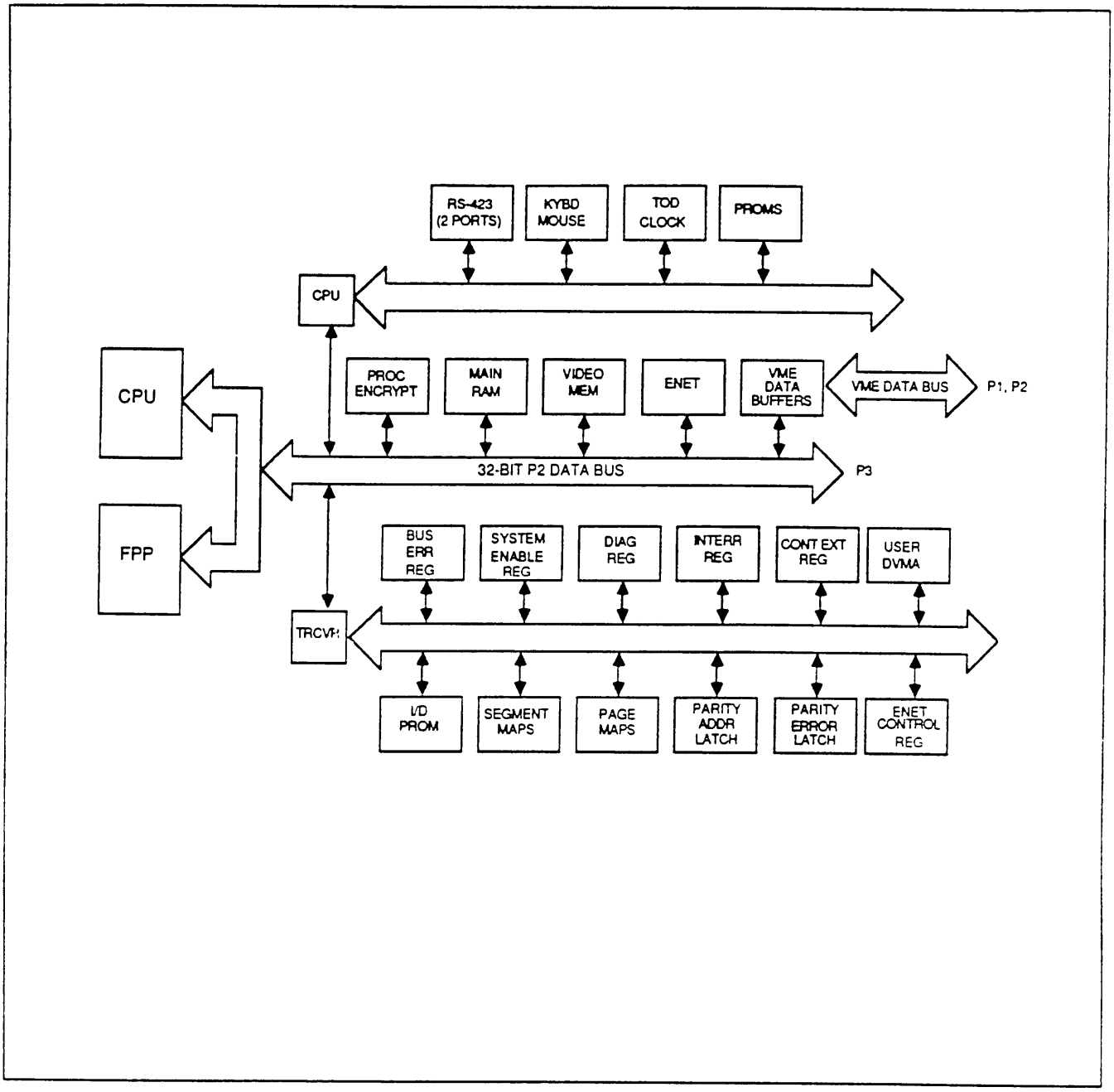
MC68020 dynamic bus sizing capability facilitates longword moves along the 8-bit bus to the parity address latch and page map interfaces. The dynamic bus sizing mechanism allows the processor to transfer operands to or from external devices while automatically determining device port size on a cycle by cycle basis.

The 8-bit buses service these components:

Table 1-1 *CPU Board 8-Bit Data Buses*

	MOS BUS	TTL BUS
Device Space Components	Keyboard/Mouse RS423 Ports Time of Day Clock EEPROM EPROM	Parity Error Register Parity Address Latch Ethernet Control Register Interrupt Register
Control Space Components (Processor Extensions)		I.D. PROM Segment/Page Maps Diagnostic Register User DVMA Register System Enable Register Bus Error Register Context Register

Figure 1-3 *Data Bus Block Diagram*

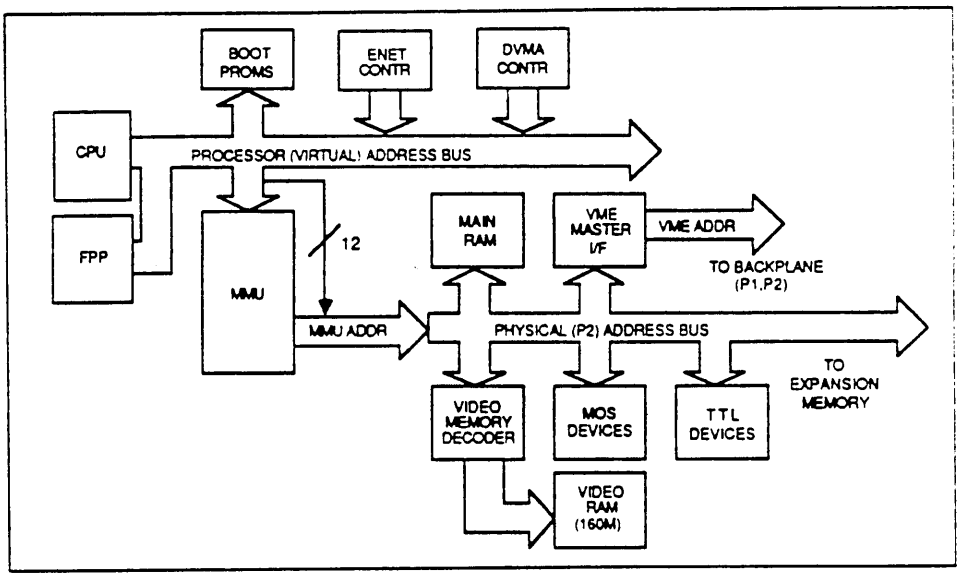


Address Buses

The CPU directly addresses the FPP, MMU, and boot PROMs by way of the 32-bit processor address bus.

Buffered address lines from the processor and MMU buses become the P2 address bus. The P2 address bus services the VME Master Interface, the Data Cyphering Processor, TTL devices, MOS devices, as well as main, video, and expansion memory. Figure 1-4 depicts the address bus structure of the 2060 board.

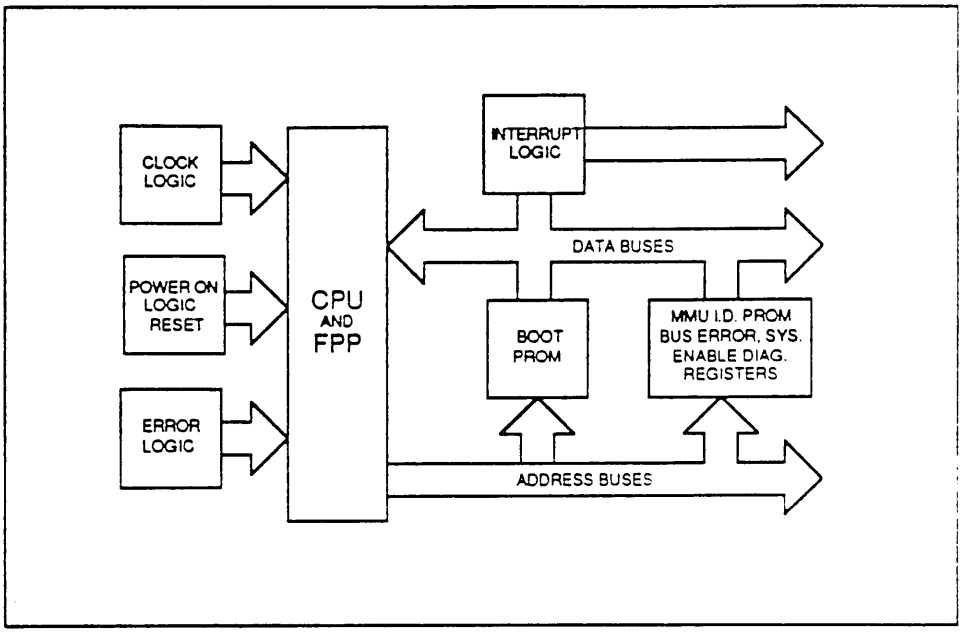
Figure 1-4 *2060 Board Address Bus*



CPU Logic and DVMA Devices

The functional blocks that comprise processor logic are shown in Figure 1-5, and discussed in the text that follows.

Figure 1-5 *Processor Logic Diagram*



The MC68020 CPU

The CPU board is based on the Motorola MC68020 virtual memory microprocessor, which runs at 16.67 Mhz and uses 32-bit addresses, as well as 32-bit registers and data paths. The CPU also features on-chip instruction cache and full IEEE floating point support (implemented with the 68881 FPP).

The MC68020 CPU uses sixteen 32-bit general-purpose data and address registers; a 32-bit program counter, a 16-bit status register, a 32-bit vector base register; two 3-bit alternate function code registers and two 32-bit cache handling registers.

On-Chip Cache Memory

The 256 byte direct mapped instruction cache is organized as 64 long-word entries. Each cache entry consists of a tag field made up of the upper 24 address bits, the Function Code 2 (user/supervisor) value, one valid bit, and 32 bits of instruction data.

The instruction cache stores a copy of previously executed instructions that are stored in main memory which effectively decreases main memory access time. The CPU first checks the cache for the next instruction; if the required instruction is found there, no instruction fetch is needed, thus increasing system performance.

Floating Point Processor

The MC68881 Floating Point Processor chip is a customer option and is software enabled. The MC68881 can also optionally run on an independent clock.

The 32-bit floating-point co-processor is designed for operation closely coupled with the MC68020 CPU. It performs mathematical calculations in strict accordance with the proposed IEEE specification *P754, Revision 10*, which guarantees support for all required operations, data types, rounding modes and rounding precision.

The chip also provides root value, trigonometric, exponential, and logarithmic functions, to name a few. It calculates all operations to 80-bit precision and eliminates inefficiencies associated with executing software envelopes through hardware implementation.

Optional Data Ciphering Processor

The Data Ciphering (Encryption) Processor (DCP) provides enhanced encryption capabilities that enable certification with governmental agencies. When used with the UNIX crypt utility, the encryption process is expedited.

To comply with U.S. Customs law, the DCP and its support PAL are socketed, and offered as a domestic option.

The algorithm processing unit of the DCP uses the National Bureau of Standards Data Encryption Standard (DES) to encrypt and decrypt data.

The chip supports three ciphering options:

- Electronic Code Book for disk applications
- Chain Block Cipher for high-speed telecommunications
- Cipher Feedback for low to medium speed, byte oriented communications.

Data bytes can be transferred through both Master and Slave ports on the chip, and key bytes can be written through Auxiliary and Master ports.

The Master Key, Encryption Key and Decryption Key each use a separate 56-bit, write-only key register. Eight-bit Mode, Command and Status registers provide MC68020 access through the Master Port.

Processor Supporting Logic

Logic supporting the MC68020 includes programmed array logic (PAL) chips that perform CPU space decoding, reset, bus error detection, data transfer acknowledge, and interrupt priority encoding/acknowledgment. Boot-up and diagnostic code is stored in 64Kbytes of erasable, programmable read-only memory (EPROM).

System Reset

The power-on/reset logic provides a means of starting a processor and/or system initialization sequence in response to fluctuations in supply voltage; a reset signal from an external bus or the watchdog reset switch; or a halt in the CPU processing cycle.

Power-on reset is active for a minimum 100 msec after the power supply voltage reaches 4.5V. Power-on reset results in the following:

- CPU Reset
- System Enable Register Clear
- Forced Boot State
- Diagnostic Register Reset (lights LEDs)
- FPP Reset
- Memory Error/Interrupt Register Reset
- Keyboard/Mouse; RS423 Port Reset
- VMEbus Reset
- Ethernet Interface Reset
- All State Machine PALs Reset

If the CPU board is jumpered to enable a VME bus arbiter other than the CPU board, the VME bus SYSRESET signal, initiated off-board, can cause a power-on reset.

A double bus fault that causes a CPU halt results in a watchdog reset, which results in execution of the PROM monitor program, or restart of system self-tests, depending on EEPROM programming. (Heading 2.9 in *Chapter 2* describes EEPROM programming.)

The User Reset Switch, located on the rear edge of the CPU board, provides a manual watchdog reset.

Interrupt Logic

The 2060 board interrupt logic determines the priority of interrupt requests that are directed to the CPU from internal and external logic groups.

The various levels of VME interrupts are mapped to the corresponding on-board levels.

On-board interrupts receive higher priority than off-board VME interrupts at the same level. On-board interrupts are autovectored on all levels, with the exception of level 6, which represents the serial communications controllers (SCC)s. SCCs provide their own vector for functions such as transmit and receive, which eliminates time that interrupt software would take to determine which part of the SCC originated the interrupt.

Priorities for on-board device interrupts are determined in this way:

Level	Device
7	NMI - Real time clock and parity error
6	Serial controllers (8530A chips)
5	Real Time Clock
4	Video vertical interrupt
3	Ethernet - System enable register 3
2	System enable register 2
1	System enable register 1

The order in which boards are placed in the card cage determines off-board interrupt priority.

System Clocks

Two crystal oscillators provide a main system clock and an optional FPP clock.

The clock generator logic takes the main clock 33.33Mhz frequency and divides it by two, to provide timing for internal data processing. The PALs stretch the high part of processor cycle state 4 for an extra 30 nanoseconds, which allows more time for data to be returned to the processor and for data acknowledge turnaround. The resultant 16.67Mhz clock may also be jumpered to provide FPP timing.

A second, 25Mhz crystal provides, through a flip-flop, a 12.5Mhz clock which can be jumpered to the FPP clock or used for 12.5MHz system clock timing. The *Configuration Procedures* manual, Sun PN 813-2000 describes CPU board jumper settings.

The Real Time Clock

The Real Time Clock is an Intersil 7170 time-of day clock with battery backup. The clock interrupt signal causes an interrupt request on Level 5 or 7 through the interrupt register.

The Boot PROM

Boot-up and diagnostic code is stored in 64Kbytes of eraseable, programmable read-only memory (EPROM). The CPU uses the boot code during reset and "boot state". Boot code execution bypasses the MMU and determines that the CPU board is ready for initialization of the operating system or for execution of diagnostic code. Chapter 2, *Diagnostics and Troubleshooting*, describes the boot-up and self-test sequence.

The EEPROM

An electrically eraseable PROM stores parameters that determine the following:

- Which device is the system console or primary terminal during a non-diagnostic boot-up.
- From which device UNIX will be booted during a boot with the diagnostics switch set on NORM.
- The quantity of memory to be tested by boot PROM diagnostics during a non-diagnostic boot.

- Whether the console display size will be 900x1152.
- What will happen following a Watchdog Reset: a self-test restart or display of the PROM monitor prompt.
- The boot device used for a diagnostic boot, and the location of a selected diagnostics program.
- Whether the Sun logo or a custom banner is displayed during boot-up.
- Whether or not the keyboard "click" is enabled.

A record of the board and storage device types present in the system is also stored on the EEPROM.

The *Diagnostics and Troubleshooting* section of this manual provides instructions on EEPROM programming, which is done through the PROM monitor at this time.

Direct Virtual Memory Access

Direct virtual memory access (DVMA) allows devices to use the MMU to read from and write to memory. DVMA devices include the Ethernet interface, the VMEbus slave interface, and refresh circuitry.

A DVMA cycle is initiated when inputs from either the memory refresh logic, the Ethernet control or the VMEbus slave interface are synchronized and presented to the DVMA controller. The controller then generates a processor bus request and waits for a bus grant signal. The CPU issues the bus grant, which the DVMA controller acknowledges by asserting a bus grant acknowledge and removing the bus request.

The DVMA controller then determines the priority level of the request; sends a DMA enable signal to the requester, and, for VME slave or Ethernet requests, asserts the P2 DVMA address strobe. Following an acknowledge from memory or video circuitry, the transaction is ended with removal of the address strobe and bus grant acknowledge, and then the DMA enable signal.

DVMA handling for refresh circuitry differs slightly from that for other DVMA devices, in that the controller does not issue a P2 address strobe and waits for a special R.SSAS refresh signal rather than an acknowledge signal.

The refresh circuitry receives highest priority, followed by the Ethernet and VMEbus slave interfaces. The Ethernet interface can issue a HOLD signal along with the bus request to retain bus mastership for the 82586 FIFO circuitry.

User DVMA

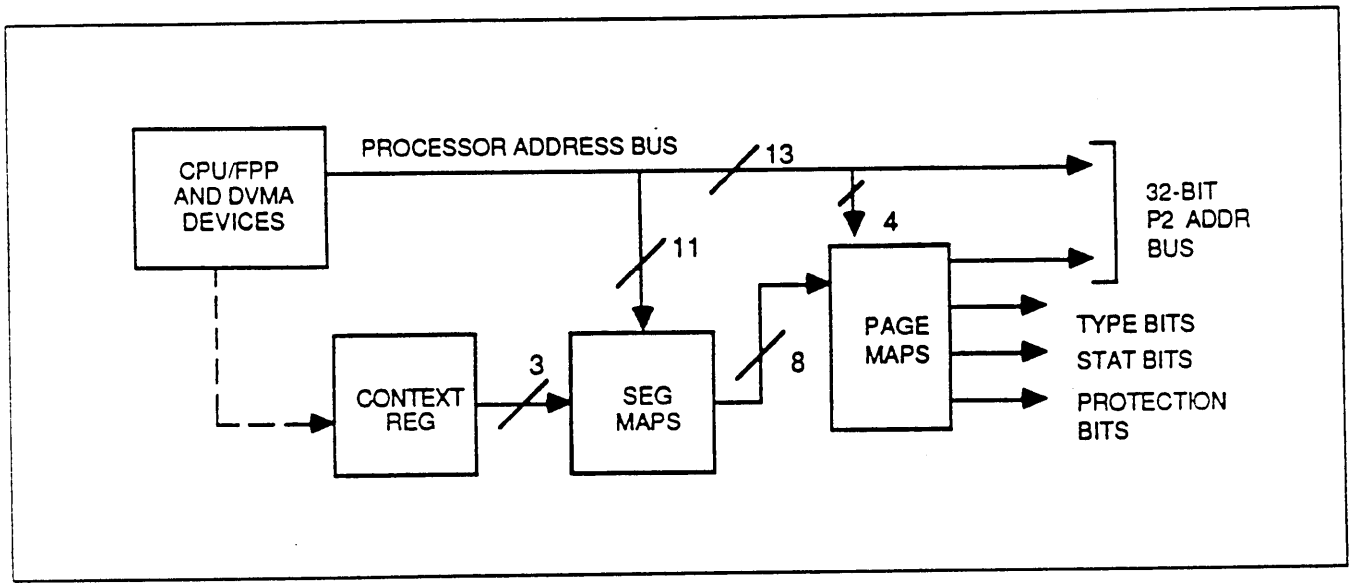
A User DVMA Enable Register provides an external VME device with 256 MBytes of accessible memory for each of eight contexts.

User DVMA occurs with user function codes when a VME device accesses the top two gigabytes of 32-bit address space on the VMEbus, provided that the corresponding context is enabled in the User DVMA Enable Register.

Memory Management

The memory management unit translates virtual memory addresses into physical ones. The MMU is composed of a user/supervisor context register, segment map RAMs, page map RAMs and associated logic, and allows devices to work in a shared and protected environment.

Figure 1-6 *MMU Block Diagram*



A context register appends three bits to the virtual address through the segment and page map RAMs to produce physical addresses.

The segment map RAMs use the context value, combined with a processor address, to produce a page map entry group (pmeg). The pmeg is, in turn, input to the page map RAMs, which generate an output composed of mapped address lines and a number of status and control bits. This output provides addresses to memory by way of the P2 address bus.

When an "s" protection bit is set for a page of memory, only supervisor accesses (for program or data fetches) are allowed. Otherwise, the memory address is accessible for user (application) as well as supervisor fetches.

Status and type bits further define and extend physical addressing capabilities. Status bits determine whether or not a page of memory has been accessed or modified in order to assist the swapping software.

Type bits divide memory addressing in this way:

Type 0: Main and Video Memory

Type 1: I/O and Control Devices

Keyboard/Mouse Interface
Serial I/O Ports
EEPROM
EPROM
Time of Day Clock
Parity Error Registers
Interrupt Register
Ethernet Control Register
Data Cyphering Processor

Type 2: 16-Bit Data VME Master Interface

Type 3: 32-bit Data VME Master Interface

On-Board Main Memory Logic

Sun-3 memory architecture is based on the concept of virtual memory, in which only a small portion of the total logical address space is mapped onto the physical memory resident on the boards. The balance of the maximum available memory space is located either on a secondary storage device (e.g. a large capacity disk drive) or on the network, and accessed through the DVMA scheme.

When the CPU attempts to access a virtual memory address location that is not currently residing in physical memory, a page fault occurs, and the data is fetched from the secondary storage device.

Memory Refresh Logic

The refresh logic provides a refresh cycle for memory every 15.7 usec. This logic is composed of a PAL and a pair of counters. The first (8-bit) counter generates a clock pulse, which is used by the DVMA control logic to produce an enable signal for the second (refresh) counter. The refresh counter then sends a refresh address to memory.

Main Memory

Main memory consists of 144 256Kx1, 120 nsec DRAMs, divided into four 1Mbyte banks. (Additional memory resides on up to three memory expansion boards.) *Sun Configuration Procedures* manual) enables four megabytes of additional memory.

The main memory address decode logic, which includes RAS and CAS PALs, and a row/column multiplexer, determines which bank of memory is being addressed. Memory access occurs when the write data and the read/write control signals are valid at the same time that CAS is valid.

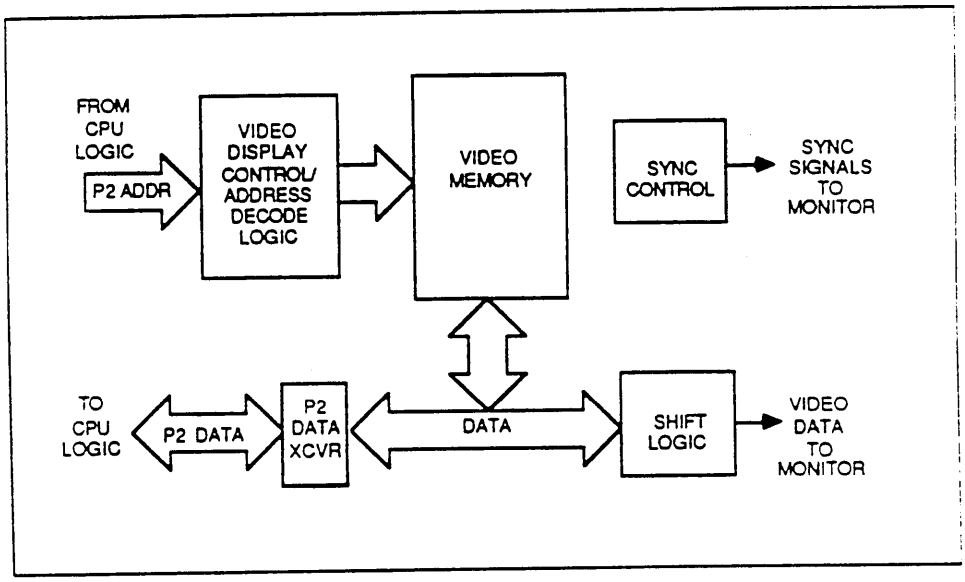
Video Interface Logic

This discussion of 2060 board video logic applies only to the Sun-3/160M Workstation.

The Sun-3/160C and 160G use the color board (described in Subsection 1.3) to control the function of its color monitor.

CPU board video logic generates and transmits differential ECL video signals, as well as TTL horizontal and vertical sync pulses, to the Sun-3/160M monochrome monitor. Video logic consists of video memory, with its associated control and address decoding circuitry, sync control logic and shift circuitry. Figure 1-7 provides a functional block diagram illustrating this logic.

Figure 1-7 *Video Logic Block Diagram*



Video Memory

Video memory is a 128K byte block configured as 16K, 64-bit words. The memory is dual ported to allow access by both the CPU and the video refresh logic.

The video memory bus provides a path for row and column address transmission from the CPU. Two address registers latch the addresses for input to video memory. A pair of address counters generate row and column addresses, which are latched and routed to memory for the video refresh cycle.

The video memory controller is a state machine that manages video memory operation. Memory controller outputs are used to select either the processor address or the video refresh address, allowing the controller to initiate any of three memory cycles: idle, processor update and video refresh.

A sequence of 16 states, continuously executed by the state machine, determines when the cycles are performed. Idle and processor update cycles are executed during the first eight states; the video refresh cycle is executed during the last eight.

Video Sync Control Logic

Video sync control logic is composed of horizontal and vertical state machines that generate horizontal and vertical sync signals, respectively. The video controller register latches state machine outputs, which are then transmitted to the video monitor.

Video Shift Logic

Video shift logic consists of a TTL-to-ECL converter and a 100MHz shift register. Video data is loaded from video memory into the TTL to ECL converter and clocked through the 100 Mhz shift register. The converter supplies differential ECL video to the monitor.

Serial Communications Interface

Two 8530 Serial Communication Controllers (SCCs) implement communication between the CPU board and the keyboard, mouse and the RS-423 interface.

One SCC is dedicated to the keyboard and mouse; the other to RS-423 communication. The SCCs function as Universal Synchronous/Asynchronous Receiver/Transmitters (USARTs) to serialize parallel data that is transmitted from the CPU board, and route it to the respective interfaces. The inverse is true for incoming serialized data.

Each SCC provides two high-speed, fully symmetrical, programmable serial channels with built-in baud rate generators.

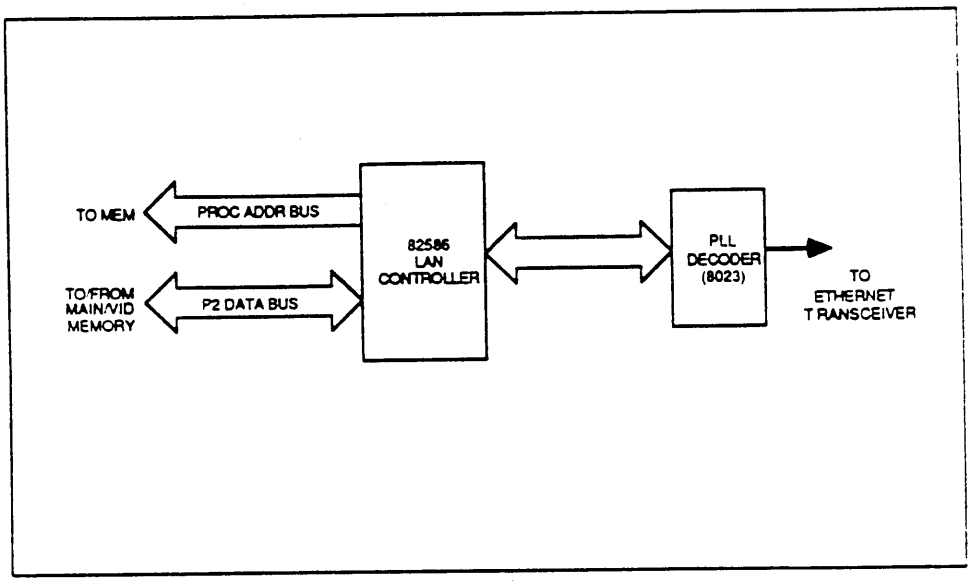
The SCC that supports the Sun-3/160 RS423 interface supplies serial I/O from Channel A to the rear panel serial port A, and serial I/O from Channel B to to the serial port B. Channels A and B can also be shared for synchronous transfers.

The SCC that services the keyboard and mouse functions as an asynchronous receiver/transmitter, using Channel A for the keyboard, and Channel B for the mouse.

Ethernet Interface

The primary components of the Ethernet interface are an Ethernet controller PAL, an Intel 82586 Ethernet Data Link Controller (EDLC), phase locked loop encoding/decoding circuitry, and address and data buffers, which interact to provide the hardware necessary for communication between the Sun-3/160 and other nodes connected to the Ethernet. Figure 1-8 illustrates Ethernet interface logic.

Figure 1-8 *Ethernet Interface*



The Ethernet Controller PAL holds random Ethernet logic, handling functions such as transmission of P2 bus mastership requests to the DVMA controller.

The 82586 (EDLC)handles most of the functions associated with the data link and physical link layers of local area network (LAN) architecture. It performs frame boundary delineation, addressing, bit error detection, and link management functions.

The EDLC controller shares Sun-3/160 memory space and can issue a HOLD signal in order to retain bus mastership when necessary for its FIFO operation

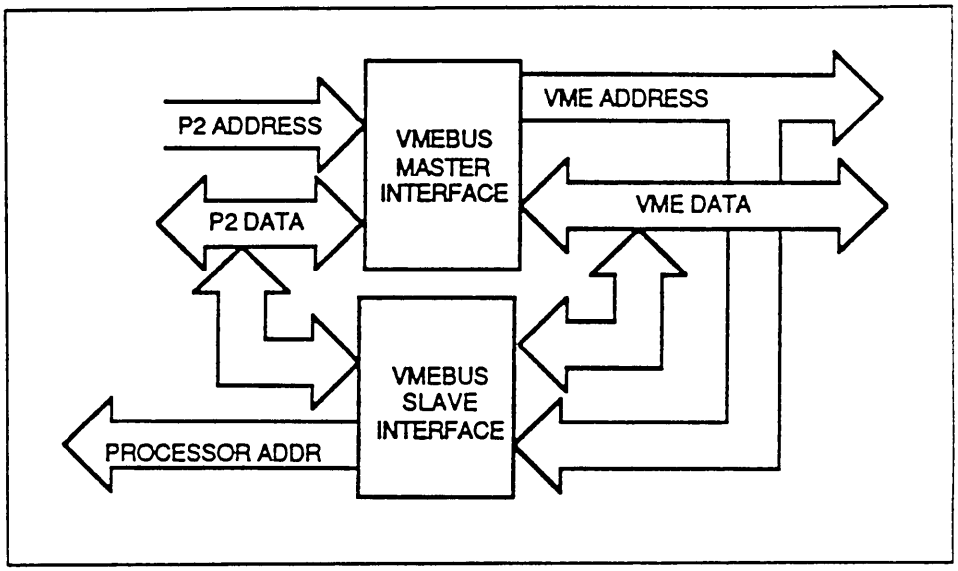
The 82586 receives serial data and handles address recognition and CRC checking in its receive unit. Its command unit executes instructions that come from the MC68020 CPU through a reserved portion of memory.

The 8023 encoder, or front end chip, translates clock and data from the Sun-3/160 into a single, self-clocking serial data stream. The encoder drives the transmit pair of transceiver cables, using Manchester encoding, and places a preamble on the frame to allow channel circuitry throughout the network to become stable before receiving valid input. The decoder removes the preamble from incoming frames and translates the incoming serial data stream into clock and data for the EDLC to process.

VMEbus Interface

The VMEbus interface provides bidirectional data access between the CPU board and any device connected to the VMEbus. The interface logic consists of bus arbitration and request circuitry, as well as logic that allows the CPU board to act as the bus master or as a bus slave. Figure 1-9 is a block diagram of VMEbus interface logic.

Figure 1-9 *VMEbus Interface*



VMEbus Arbitration

Two PALs and a pair of registers monitor bus request levels and arbitrate requests, using a level daisy chain. When the CPU requests the bus (in order to perform a read/write cycle, or to acknowledge an interrupt), it sends a bus select signal to one of the PALs.

If the arbitration logic does not control the bus, it will assert a VME bus request signal to request bus mastership. If the arbiter currently controls the bus, it will retain control until another bus master requests it.

When the arbitration logic has attained VME bus mastership, the CPU may access any slaves on the bus through the VMEbus master interface. When the CPU relinquishes bus mastership, it becomes a bus slave, and may be accessed by other VMEbus masters, through the VMEbus slave interface.

VME Master Read/Write Cycles

During a VME Master read or write cycle, the type bits coming out of the MMU indicate either an access to Type 2 or Type 3 space (refer to the MMU subsection). VME address and data strobes are then generated, and the CPU board waits for a DTACK signal from the VME device being addressed. Upon receipt of data transfer acknowledge, the VME bus master will negate the address and data strobes, ending the transfer.

If the VMEbus does not return a data transfer acknowledge signal within 3.3usec, a short time-out occurs, during which the CPU rearbitrates for the P2 bus, allowing refresh or Ethernet devices to use the bus. The VME Interface is frozen until the suspended cycle can be rerun. If a P2 data transfer acknowledge does not occur within 256 tries, the CPU receives a bus error and the VME master controller enters idle mode, retaining bus mastership, and waiting for another VME select signal to come in.

VME Interrupt Acknowledge

During a VME interrupt acknowledge cycle, the VME bus master will acknowledge the interrupt and negate the address and data strobes. The interrupt acknowledge signal is transmitted to the cardcage, where it is daisy-chained to each of the boards resident there. Each board is polled, in turn, to determine which one is the source of the interrupt. When the board generating the interrupt is located, it drives a vector address onto the VME bus, along with the data transfer acknowledge signal.

VME Slave Mode

A VME slave mode cycle begins when an external device asserts a bus request. The arbiter eventually grants the VMEbus to the requesting device, at which point the device enables its addresses and data onto the VMEbus and asserts address and data strobes. The addresses are then latched on the CPU board.

The slave space decoders then look at the latched address. If the address refers to the CPU board, the decoders generate either a supervisor or user DMA signal that indicates that a valid access request has come from a VME slave.

A transfer request now tells the DVMA controller that the slave interface wants to use the P2 bus, and the controller in turn asserts a processor bus request. The transfer is enabled onto the P2 bus, and a memory read or write cycle occurs, after which the address strobe and DMA enable signals are removed, and a data transfer acknowledge is asserted.

VME Implementation

The tables that follow show how Sun-3/160 backplane circuitry and CPU board VME interface circuitry comply with the VMEbus Specification, and which options are implemented.

Table 1-2 *Master Capabilities*

Data Bus Size	D32 MASTER 32/16/8 bit data
Address Bus Size	A32 MASTER (DYN) 32/24/16 bit addresses
Timeout Option	TOUT(737) 737 microsecond timeout period
Sequential Access	None
Interrupt Handler	IH(1-7)(STAT) Levels 1-7, independently jumperable
Requester Option	ROR R(3) Release on request, level 3
Bus Busy Option	Releases BBSY after AS assertion when releasing bus
Read/Modify/Write	Will not release VMEbus during Read/Modify/Write Cycles

Table 1-3 *Slave Capabilities*

Data bus Size	D32 SLAVE (DYN) 32/16/8 bit data
Address Bus Size	A32 SLAVE (DYN) 32/24 bit addresses (no 16-bit addresses)
Sequential Access	None
Special Access Mode	A high-speed access mode is engaged if the time from DTACK assertion to the next AS and DS assertion is less than 200ns.
Interrupter Options	None

Table 1-4 *System Controller Capabilities*

Clock Option	SYSCLK 16 Mhz, jumperable (not used on board)
Arbiter Option	ONE Bus Request/Grant, Level 3 only, or External Arbiter
Bus Time Out Module	None
Sysreset Option	SYSRESET MASTER or SYSRESET SLAVE, including manual button
Sysfail Option	Not monitored
ACfail Option	Not implemented (ACFAIL is connected to SYSRESET)

The table below shows which 96-pin connectors and rows of pins on the backplane service the VMEbus, and which serve the "P2" Physical Address Bus:

Table 1-5 *Backplane Connector Function*

Connector	*Row*	*Function*
P1	A	VME
	B	VME
	C	VME
P2	A	"P2"
	B	VME
	C	"P2"
P3	A	Power
	B	"P2"
	C	Power

1.2. Memory Expansion Board

The 2061 memory expansion board is available in two configurations, which provide either 2 or 4 MBytes of additional memory to the Sun-3/160 workstation.

Expansion memory is organized identically to the memory section of the 2060 CPU board. Memory address decoding is also virtually identical. Refer to the *Sun Configuration Procedures*, Sun PN 813-2000, for expansion board component layout and jumper select options and dip switch settings.

1.3. The 160C/160G Color Board

Both the Sun-2 and Sun-3 color board provide high resolution color graphics for the Sun-3/160C workstation. This board replaces the monochrome video logic resident on the CPU board, which is enabled only when a monochrome monitor is part of the workstation. The color board provides the Sun-3/160G monitor with 256 levels of white through the green and sync cables. Because color board function is basically the same for the Sun-2 and Sun-3 boards, the majority of this text applies to both versions, with references to minor variations when necessary.

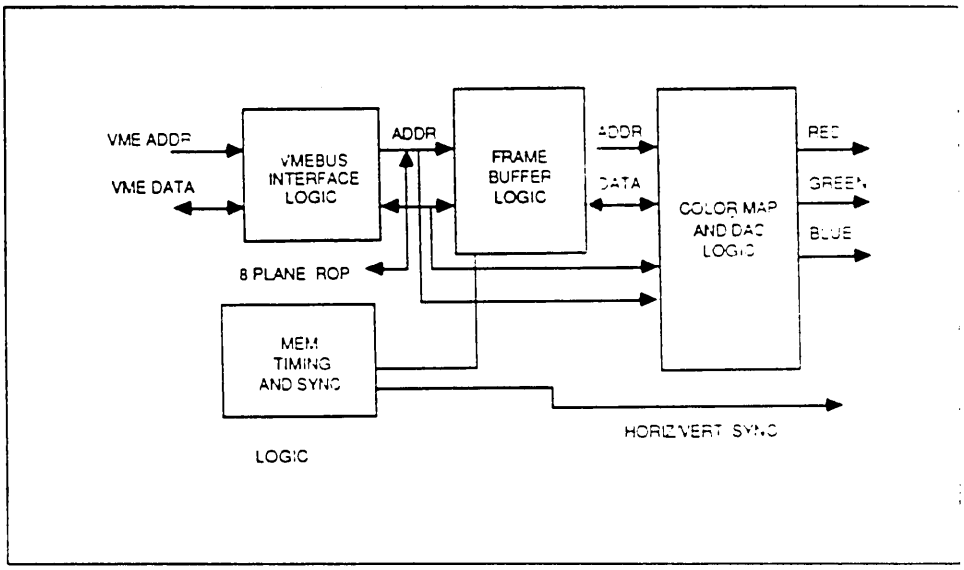
The board is a bit-mapped graphics subsystem that features a 1152x900x8, 66Hz non-interlaced display; a frame buffer that appears as a million 8-bit-deep pixels that each define one-out-of-256 shades of red, blue or green; and 8-plane "RasterOp" support.

Color board logic is separated into the following functional blocks:

- VMEbus interface
- frame buffer logic
- memory timing and synchronization circuitry
- color maps
- digital-to-analog converters (DACs).

Figure 1-10 presents a functional block diagram of color video board logic.

Figure 1-10 *Sun-3/160C/160G Color Video Board Logic*

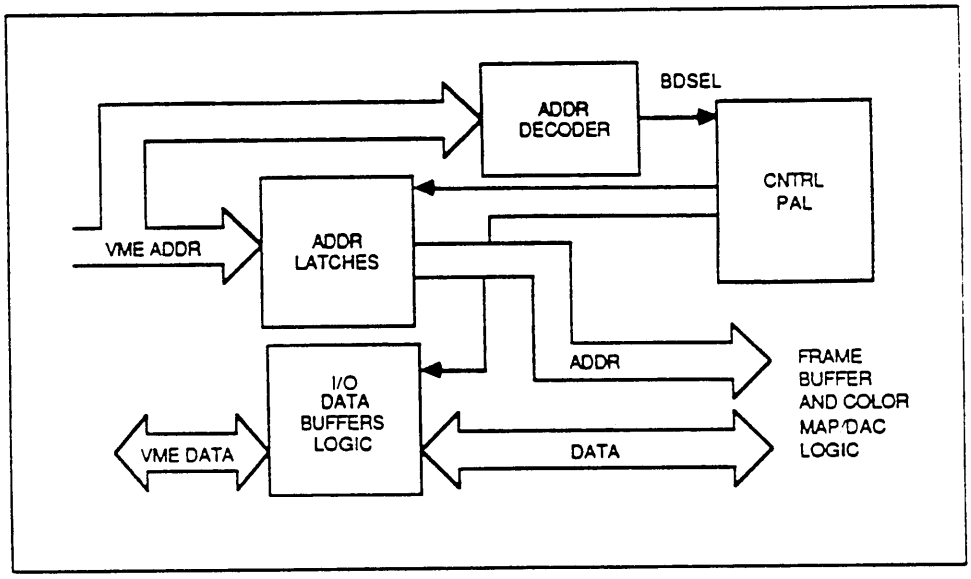


Color Board VMEbus Interface

The color board VME bus interface manages the transfer of VME bus addresses and data, and provides control signals to the frame buffer address decode circuitry. This logic operates asynchronously with the state machines and responds to VME bus read, write and interrupt acknowledge cycles.

The VME bus interface consists of address latches, data input and output buffers, an address decoder and a control PAL. Figure 1-11 provides a block diagram supporting the VME bus interface logic.

Figure 1-11 *VMEbus Interface Logic*

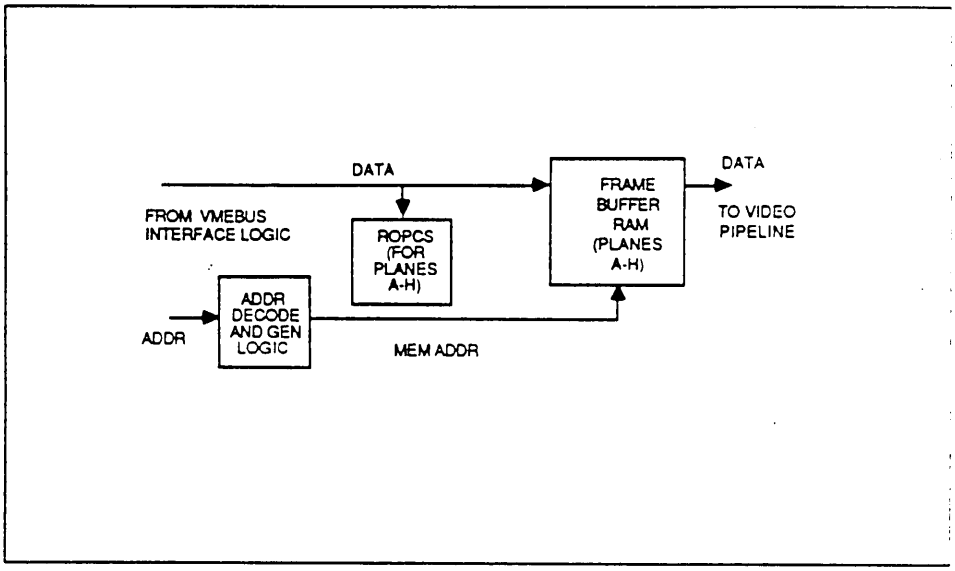


Frame Buffer Logic

Frame buffer logic consists of frame buffer memory, the address decode and generation circuitry, the video refresh logic and the RasterOp chips (ROPCs).

The *Sun Configuration Procedures* manual, Sun PN 813-2000, contains jumper setting information. Refer to Figure 1-12 for a block diagram of frame buffer logic.

Figure 1-12 *Color Board Frame Buffer Logic*



Frame Buffer Memory

The frame buffer is separated into eight planes, labeled A through H. The Sun-2 frame buffer consists of 128 64K nibble-mode RAM chips, while 32 64Kx4 Video DRAMs make up the Sun-3 frame buffer.

Frame Buffer Addressing

The frame buffer receives addresses from either of two sources: the VME address bus or the video refresh logic. During updates to the frame buffer memory, the VME address lines are multiplexed to form the CAS and RAS addresses.

Specific bits in the VME address are also used to select the possible addressing modes: word mode, pixel mode, or ROP mode. The word mode and pixel mode counters each generate an address, which, when selected, is driven to the frame buffer inputs. Video refresh memory cycles and inactive read/write cycles take their addresses from a pair of 16-bit counters and the Word-Pan Base Address register.

Address Modes

The data input to the frame buffer is dependent upon the frame buffer addressing mode. Ten addressing modes are available: word-mode memory, pixel-mode memory and four word and four pixel modes controlled by the RasterOp chips (ROPCs).

Raster and other operations that use less than eight bits per pixel use word mode accesses, while drawing, shading algorithms and other imaging related applications use pixel mode accesses.

Raster Op Modes

RasterOp means that rectangular areas of display data (Raster) are modified or combined according to a preselected operation (OP). ROP chips are used to speed the combination of text with graphics and the ROP modes provide the ability to access a variable number of planes or pixels within the frame buffer memory.

Either frame buffer memory or the VME data bus loads ROPC source registers, sometimes on a read and sometimes on a write.

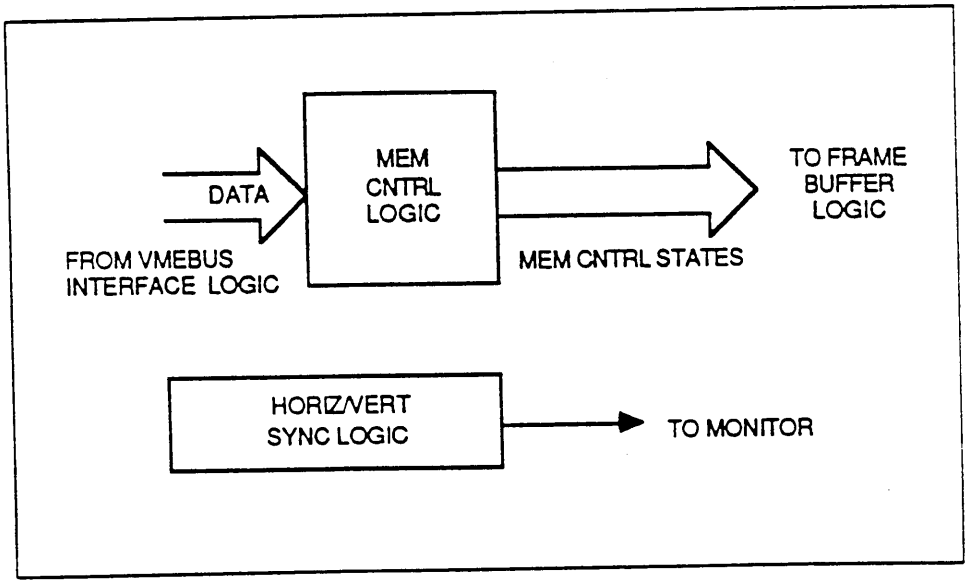
Each memory plane in the frame buffer has a separate RasterOp unit. These units can function individually or in parallel to update as many as 128 frame buffer bits simultaneously. Data from the frame buffer is converted from TTL to ECL.

The DAC address inputs are connected to an internal color map, which translates the address to a 24-bit data value. The translated value drives three video DACs, whose outputs are routed to the red, green and blue BNC connectors.

Memory Timing and Sync Logic

This logic group consists of the memory control logic (which controls the timing for the frame buffer memory) and the horizontal and vertical sync circuitry (which transmits horizontal and vertical sync pulses to the monitor). Figure 1-13 is a functional block diagram that illustrates this logic.

Figure 1-13 *Memory Timing and Synchronization Logic*

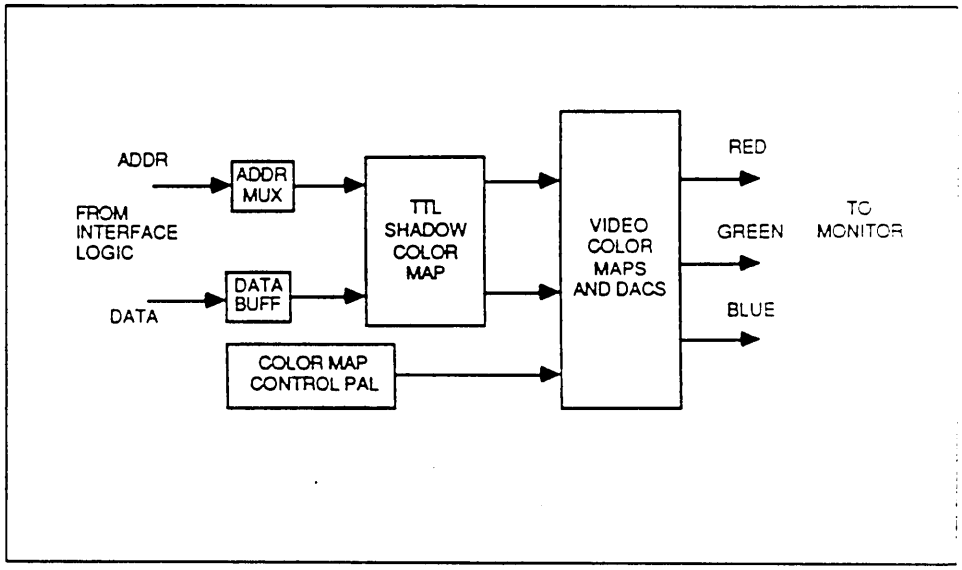


The horizontal and vertical sync circuitry is composed of a pair of state machines, which generate horizontal and vertical sync pulses for use by the monitor.

Color Maps and DACs

Color map and DAC logic consists of the color map video translation tables, the video digital-to-analog converters (DACs), the TTL shadow color map, the color map control PAL and associated circuitry. Figure 1-14 illustrates this logic.

Figure 1-14 *Color Map and DAC Logic*



The color map video translation tables and the video digital-to-analog converters are housed in a single hybrid ECL device. The DACs send red, green and blue color signals to the monitor.

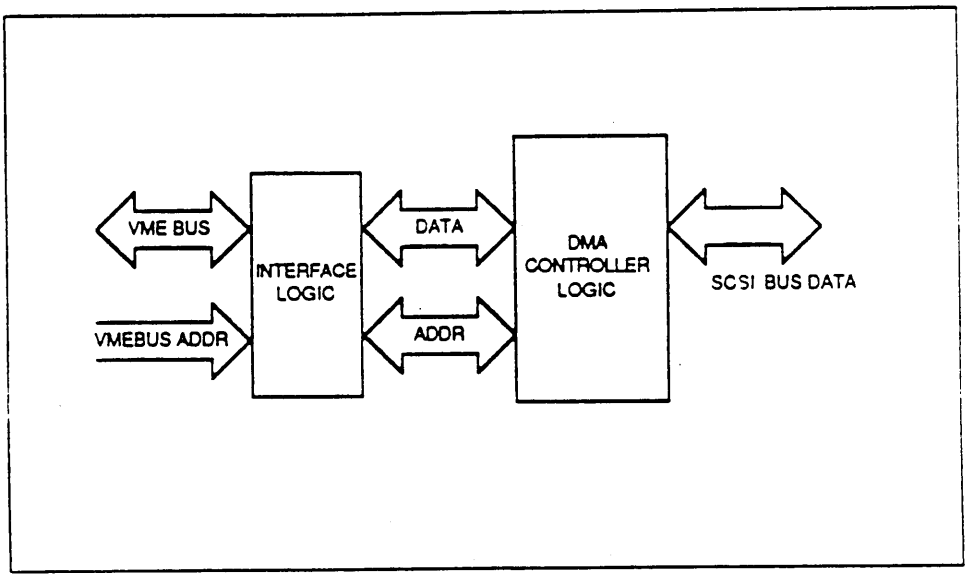
The TTL color map consists of a pair of 1K x 4-bit static RAMs. Because of the real-time constraints involved in updating the internal ECL color maps, the TTL color map is used to provide read/write access. Transmission of TTL color mapped data and addresses to the ECL color map occurs during vertical retrace.

The VME address bus routes color mapped addresses to the TTL shadow color map. The shadow color map also receives 8 bits from the VME data bus. During the vertical blanking interval, data stored in the shadow color map is routed to the DAC color maps. The color map control PAL selects from the red, green or blue color maps.

1.4. VME SCSI Board

The VME Small Computer System Interface (SCSI) board allows the Sun-3/160 to access the tape and/or disk drives that make up its internal memory subsystem. VME SCSI board logic is separated into two principle groups: the SCSI bus interface and the DMA controller. Figure 1-15 provides an overview of the VME SCSI board logic.

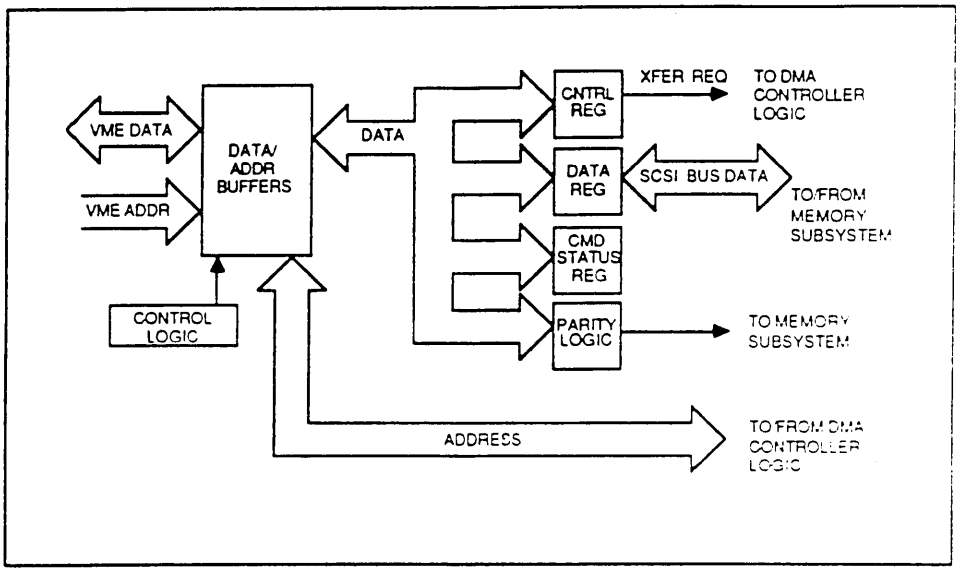
Figure 1-15 *VME SCSI Board Logic*



SCSI Bus Interface Logic

The SCSI bus interface logic consists of the interface control, data and command/status registers, as well as the parity logic and control circuitry. The SCSI bus interface logic is illustrated in the block diagram in Figure 1-16.

Figure 1-16 *SCSI Bus Interface Logic*



The interface control register manages the interface between the VME bus and the SCSI bus by means of 8 bits from the VME data bus and 8 control lines from the SCSI bus. The control lines and data bits are input to the control PAL, which generates control signals for use by the SCSI board. The original control and data bits are then buffered back onto the VME data bus.

The data register is used to transfer data between the VME and SCSI buses. The mechanics of data transfers between the VME bus and the 8-bit SCSI bus are described in the paragraph that discusses byte sequencing.

The command/status register transfers commands and status between the two buses. The command/status register is 8 bits wide on both the VME and SCSI bus sides.

The parity logic generates odd parity for data being output onto the SCSI bus and verifies the odd parity of incoming SCSI bus data. The control PAL latches parity errors and the control interface register buffers them back to the VME data bus.

The SCSI bus interface circuitry is responsible for byte sequencing, the SCSI bus request/acknowledge handshake and interrupt generation. This circuitry operates under the influence of two modes: DMA enable or word mode.

DMA enable mode determines whether or not data transfers use DMA. Word mode, when enabled, allows two SCSI data bytes to be transferred over the VMEbus at once. With word mode disabled, each byte of data requires its own separate transfer operation. During normal operation, both DMA and word mode are enabled.

Byte sequencing is used when word mode is enabled. It manages the transfer of data between the 8-bit SCSI bus and the VMEbus. SCSI data, to be output onto the VME bus, is "packed" into the data register two bytes at a time, allowing both bytes to be transferred over the VMEbus in a single operation. Incoming VMEbus data is "unpacked" in the correct order for transmission over the SCSI bus.

Each byte of data transferred over the SCSI bus requires a bus request/acknowledge handshake. The drive controller asserts a request signal and the SCSI interface logic responds with an acknowledge signal. An acknowledge is also asserted whenever the VMEbus accesses the data or command/status register.

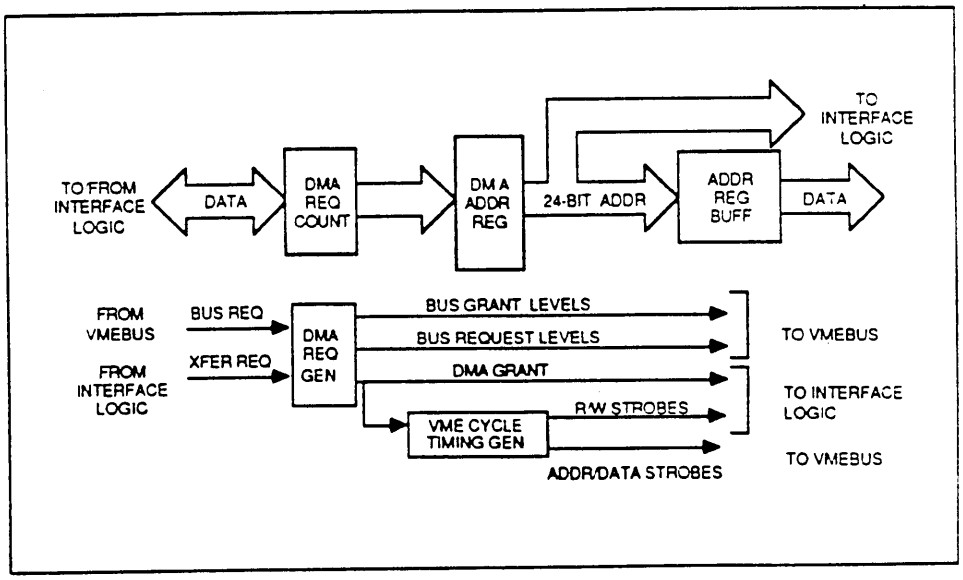
Note that in word mode, half the data bytes are transferred over the VME bus without any register access and thus do not meet the criteria for the handshake. In this mode, the interface control logic generates an automatic acknowledge in response to the request.

The SCSI board will generate an interrupt during requests for status, messages or data with DMA enable mode off. The SCSI interrupt is driven onto the VME bus. which then responds with an acknowledge signal. The level of the acknowledge signal is compared to the SCSI board's interrupt level, with a successful match resulting in an interrupt acknowledge out signal being sent to the CPU board.

DMA Controller

The DMA controller logic generates DMA addresses and timing signals for the SCSI board. This logic consists of the DMA address and count registers, the DMA cycle timing generator and the DMA request generation logic. Figure 1-17 is a functional block diagram that illustrates this logic.

Figure 1-17 *DMA Controller Logic*



The DMA count register is a 16-bit counter which may be written to or read from the VME bus. Its function is to determine how many bytes of data have been transferred utilizing DMA, and to enforce a maximum count. Sixteen bits of data

are passed through the counter to provide inputs for the DMA address register. Because of the counter's tracking function, it increments in unison with the address register.

The DMA address register is 24 bits wide. It produces a 24-bit address from the 16-bit data bus by utilizing the lower 8 bits twice. The register output is placed on an internal address bus, where it is routed to both the VME address bus and the SCSI board's internal data bus.

The DMA cycle timing generator runs the DMA cycle. The generator is primarily composed of two PALs, which supply read/write strobes for the data register as well as data and address strobes for the CPU board.

The control register sends a transfer request signal to initiate a DMA request. This signal is input to the bus requester PAL, which then transmits the appropriate bus request level to the VME bus.

All bus arbitration capability for the SCSI board resides in the CPU board arbiter logic (refer to the CPU board functional overview). The CPU arbiter logic asserts a bus-grant-in signal at the appropriate level, which is presented to the bus requester PAL. The PAL then grants control of the bus to the SCSI board.

Refer to the *Sun Configuration Procedures* manual for select jumper options.

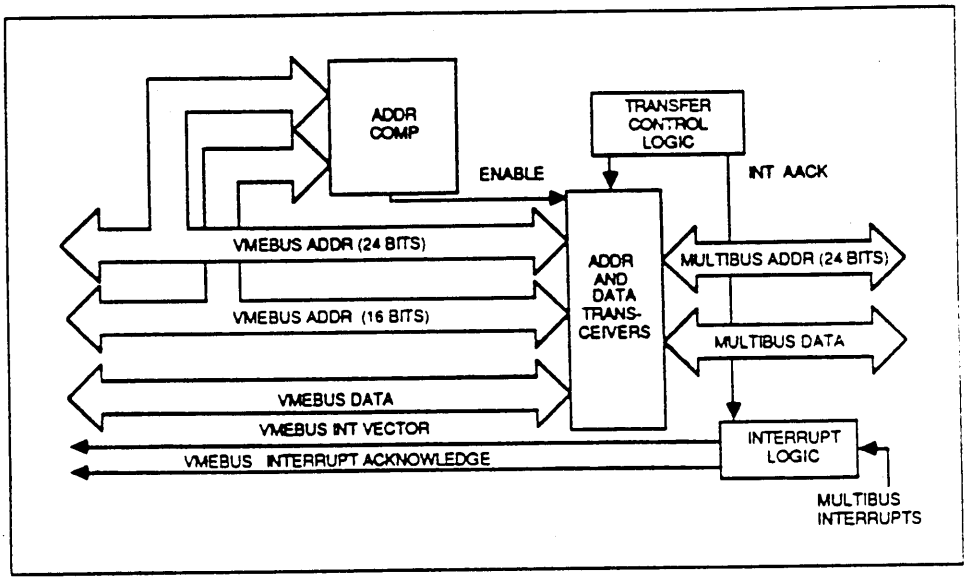
1.5. Optional Printed Circuit Boards

The VME/Multibus Adapter, Graphics Processor and Buffer Boards, and VME VME Adapter are among the optional boards that are offered as Sun-3 workstation enhancements. This subsection contains an overview of each of these boards.

VME-Multibus Adapter Board

The VME-Multibus adapter board allows Multibus boards to interface with the Sun-3/160 VMEbus. VME signals are routed through the adapter board logic, enabling Multibus boards to be written to, read from and interrupted. Refer to Figure 1-18 for a functional block diagram depicting this logic.

Figure 1-18 *VME-Multibus Adapter Board Logic*



The adapter board may be configured to respond to blocks of addresses in both the 24- and 16-bit VME address spaces. Dip switches on the adapter board set base addresses for these address blocks. Refer to the *Sun Configuration Procedures Manual*, Sun PN 813-2000, for information on dip switch settings.

Incoming VME bus addresses are checked to determine if they are within the dip switch selected block of addresses. A valid address initiates a data transfer sequence.

Data is transferred between the VMEbus and Multibus through a bank of bidirectional data transceivers. The data may be transferred either as a 16-bit word or as an 8-bit byte.

All adapter board data transfers, as well as the bus request/bus grant handshake, are controlled by a group of PALs. These PALs receive bus control signals from both the VMEbus and Multibus.

The adapter board must translate VMEbus vectored interrupts, even though Multibus does not support them. The adapter board generates a vectored interrupt by means of DIP switch settings. The interrupt occurs when the Multibus board interrupts on only one level or if a multi-level interrupt vectors to the same place. If the Multibus board interrupts on more than one level and a separate vector is required for each level, a PROM generates the vector.

Adapter board jumpers enable bus and constant clock signals for Multibus boards that require them. Refer to the *Sun Configuration Procedures Manual*, Sun PN 813-2000, for jumper options.

VME-VME Adapter Board

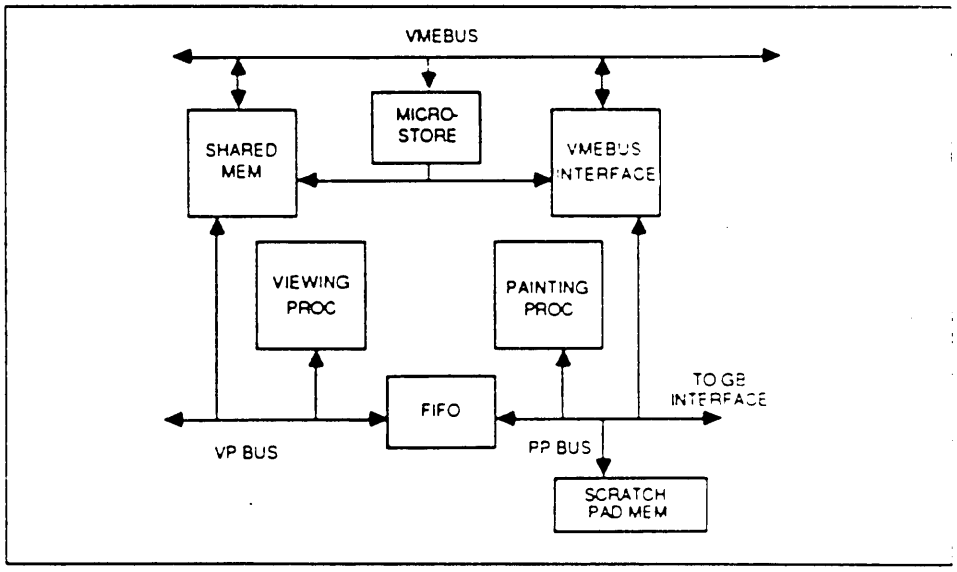
The VME-VME adapter board functions as an interface between triple-height and double-height board configurations. There are no components on the board.

The 160C Graphics Processor Board

The optional Graphics Processor (GP) board is designed to enhance the graphics performance of the Sun-3/160C. The GP runs in parallel with the host processor (located on the CPU board) and performs many of the image display tasks currently done by the host, while remaining under host processor control.

Graphics Processor board logic is designed as two pipelined processors: the viewing processor and the painting processor. These processors, along with their associated logic, are illustrated in Figure 1-19.

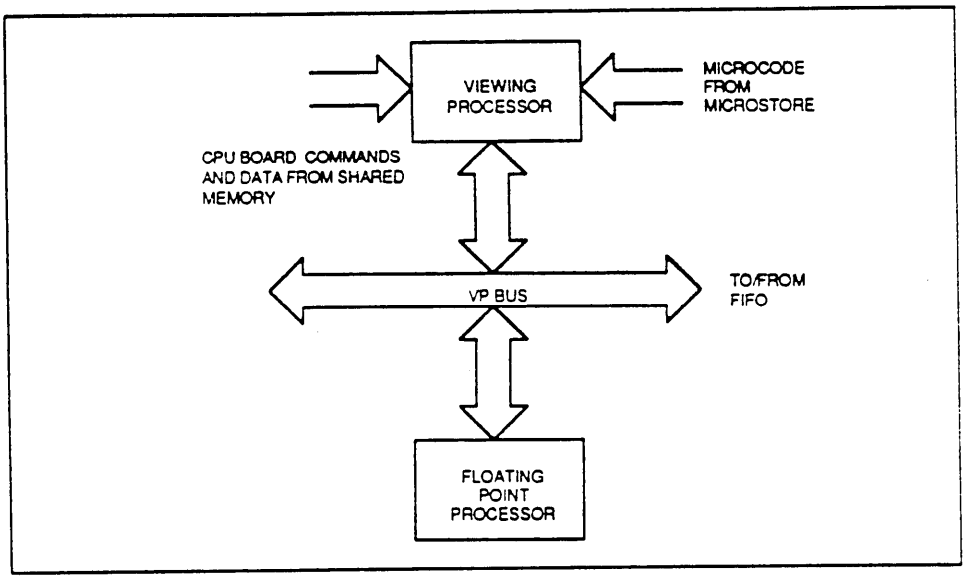
Figure 1-19 *Graphics Processor Board Logic*



Viewing Processor

The viewing processor is made up of two devices: one that interprets commands from the host processor, and one that performs the floating point operations required to translate the image from real world coordinates to screen coordinates. Refer to Figure 1-20 for a block diagram illustrating viewing processor logic.

Figure 1-20 *Viewing Processor Logic*

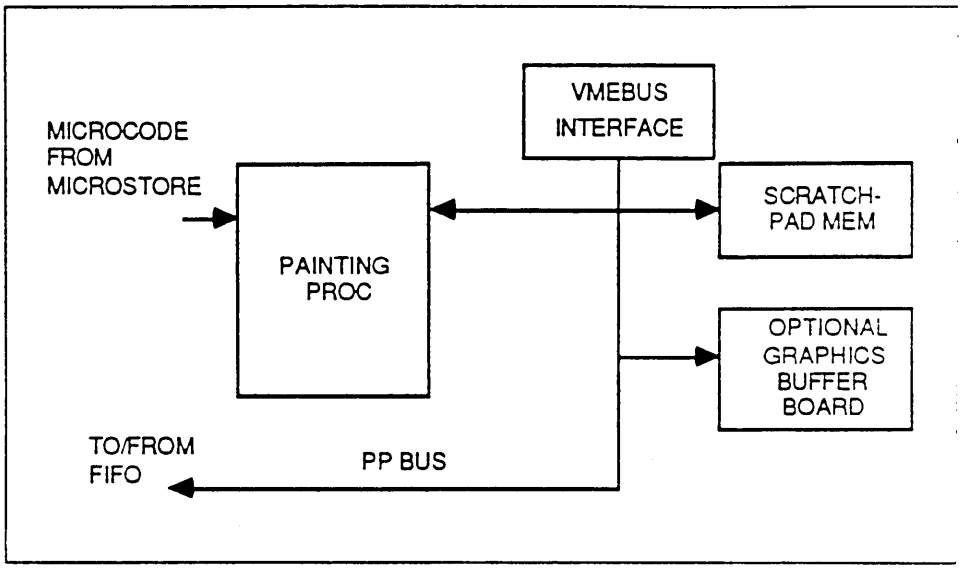


The CPU board and viewing processor use GP board shared memory to exchange commands and data. This memory is made up of 16K x 16 dual-ported static RAM. Information and instructions are passed between the various logic components of the viewing processor by way of the 16-bit VPBUS.

Painting Processor

The painting processor is used to transfer the graphic data, in pixels, into the frame buffer on the color video board. Painting processor logic includes the processor itself, the VME bus interface logic, the scratchpad memory and the optional Graphics Buffer board. Refer to Figure 1-21 for a block diagram of painting processor logic.

Figure 1-21 *Painting Processor Logic*



The painting processor uses the board's VMEbus interface logic to access the color board's frame buffer. While the VME interface is primarily used as a link between the GP and the color board, it may be used to access any other device on the VMEbus, including the host memory and the viewing processor's shared memory. The VMEbus interface also allows the GP board to generate and transmit an interrupt to the host processor.

Static RAM scratchpad memory is provided by 4Kx16 bit static RAM chips, and used to perform various algorithms necessary to painting processor function.

The 16-bit PPBUS transfers commands and data between the various painting processor components.

Processor Associated Logic

Viewing processor and painting processor logic share microstore logic and the FIFO buffer. Refer to the overview of the GP board logic in Figure 1-19 for an illustration of the relationship of this logic to the processors.

Microstore logic holds microcode for both the viewing and the painting processors. The two processors run 180 degrees out of phase, and therefore may share the microstore. A third port is available to allow access through the VME bus, but is active only when both the viewing and painting processors are halted.

The FIFO buffer is the pipeline mechanism between the viewing and painting processors. It provides 512 x 16 bits of transfer storage and is "reversible", allowing data to be transmitted back and forth between the VPBUS and the PPBUS.

The *Sun Configuration Procedures* manual contains jumper and switch settings for various GP and GB configurations.

The 160C Graphics Buffer Board

The graphics buffer (GB) board facilitates graphic applications that require the generation and display of solid images. This board consists of 2Mbytes of dynamic RAM, a 16-bit integer multiplier and a PROM for the storage of numerical constants.

The dynamic RAM is used in graphic operations such as the hidden surface elimination algorithm, which require large amounts of storage. The integer multiplier and its associated PROM increase the performance of advanced shading operations.

The graphics processor board and graphics buffer board communicate over the PPBUS. This bus is extended to the buffer board, which allows the painting processor to access GB board logic.

The *Sun Configuration Procedures* manual contains jumper and dip switch settings for various GP and GB configurations.

1.6. Memory Subsystem

The Sun-3/160 internal memory subsystem provides mass storage in these configurations:

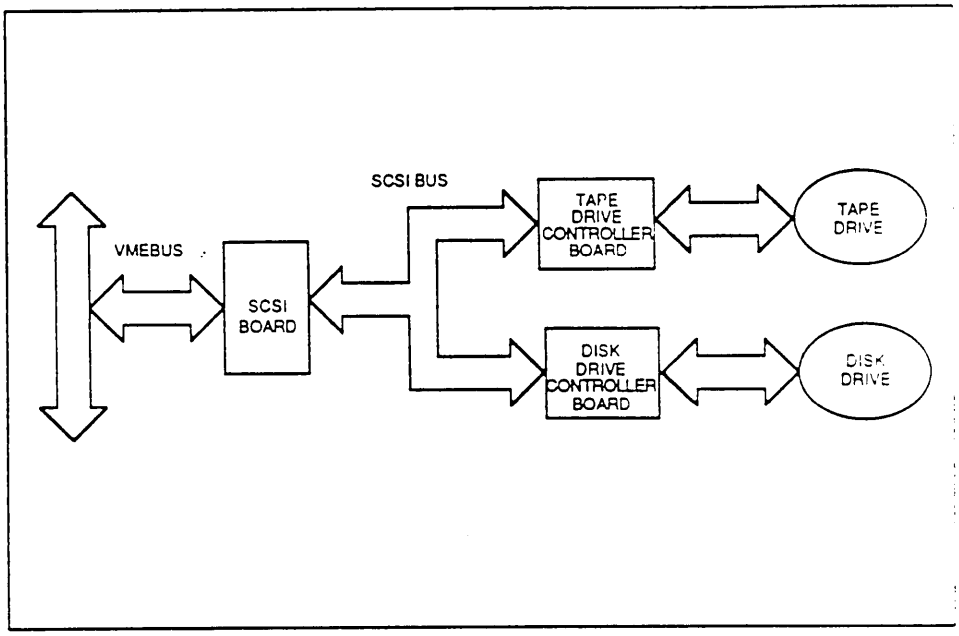
- One Disk Drive and One 1/4-inch Tape Drive
- Two Disk Drives and One Tape Drive
- One or Two Disk Drives with no Tape Drive
- Tape Drive only

The disk drive is a 5 1/4" winchester with an 85 MByte unformatted storage capacity. The tape drive type is a 9-track, streaming tape, with 45 MBytes of storage capacity.

Separate drive controller boards in the option tray allow communication between the drives and the VME SCSI board that resides in the system cardcage. Figure 1-22 illustrates the memory subsystem and its relationship to the Sun-3/160.

Addition of large capacity disk drives requires external integration and an SMD controller board. Information on these other mass storage options may be found in the *Sun Hardware Options Guide*, Sun PN 813-1000.

Figure 1-22 *Memory Subsystem*



During a write to the memory subsystem, the SCSI board (as described earlier) transmits data and commands through the SCSI bus to either the tape drive or disk drive controller board. Each of the controller boards functions as a translator between the SCSI board and its respective tape or disk drive. The reverse of this operation occurs in order to read data and status from the subsystem.

The drives and their associated controller boards are mounted on a tray, located in the top of the Sun-3/160 pedestal. Chapter 3 of this manual provides information required for removal and replacement of these assemblies.

1.7. The Power Supply

The 850 Watt power supply is located in the front end of the Sun-3/160 pedestal. This supply generates four regulated voltages, available at the backplane:

- +5VDC
- -5VDC
- +12VDC
- -12VDC

The power supply removal procedure in chapter 3 provides a wiring diagram that shows the supply inputs and outputs and their respective voltages.

The power supply operating specifications are:

Table 1-6 *850 Watt Power Supply Input Specs*

	Inputs	*Frequency*
AC Inputs	115/230 Vrms, Field Selectable	47 to 63 Hz
Operating Range	90–132 Vrms 180–264 Vrms	

Table 1-7 *850 Watt Power Supply Output Specs*

DC Load Regulation		
Voltage	*Tolerance*	*Current*
+5VDC Output	±1%	from 10-120 amps constant current
-5.2VDC Output	±1%	from 0-10 amps constant current
+12VDC Output	±1%	from 0-15amps constant current, 20 amps peak for min. 30 sec
-12VDC Output	±1%	from 0-5 amps constant current

The supply must shutdown or limit voltage if any output exceeds the value shown below. Input voltage may be recycled to restart the supply.

Table 1-8 *DC Overvoltage Limits*

Output	*Shutdown Voltage*
+5V	+6.2V ± 0.3V
–5.2V	–6.2V ± 0.3V
+12V	+13.5V ± 0.3V
–12V	–13.5V ± 0.3V

The supply can withstand 125% of the nominal line voltage for 60 msec. without damage, thermal shutdown, or loss of output regulation. Overheating causes a

thermal shutdown and requires recycling of the AC input voltage before operation is resumed.

Sun-3/160 Power Consumption

This table provides information on power consumed by the basic Sun-3/160 boards and subassemblies. For power consumption information on optional components, refer to the appropriate Sun Hardware Options Guide, PN 813-1000 or Sun Configuration Procedures, PN 813-2000.

Table 1-9 *Typical Sun-3/160 Component Power Consumption*

Part Number	*Component*	*Amps @+5V*	*Amps @-5.2V*	*Amps @+12V*	*Amps @-12V*	*Total Watts*
501-1094	2060 CPU board 4 Mbyte	13.7	0.8	–	–	72.7
501-1096	2061 Expansion board 2 Mbyte	2.7	–	–	–	13.5
501-1097	2061 Expansion board 4 Mbyte	3.5	–	–	–	17.5
370-1034	5-¼ inch Winchester 85 Mbyte	1.3	–	3.8	–	52.1
370-1037	¼ inch tape drive	2.7	–	4.3	–	65.1
540-1252	Fans (each)	–	–	0.4	–	4.8

1.8. Monitors

This text includes specifications for the Model 160M black and white monitor, the Model 160G gray scale monitor, and the Model 160C color monitor. Refer to the list of reference documents at the beginning of this manual for sources of hardware descriptions and maintenance and adjustment information concerning these monitors. Chapter 3 provides information to aid in monitor installation or removal, and Appendix C provides degaussing procedures for the color monitor.

Sun-3/160C Color Monitor

The Sun-3/160C is configured with an Hitachi 19" color monitor. The monitor receives these inputs:

- Red Video (RED)
- Green Video (GRN)
- Blue Video (BLU)
- Composite Sync (CSYNC)
- 120/220VAC Tap Selectable

These are the operational characteristics of the color monitor:

- Visual Display— 900 x 1152 pixels
- Horizontal Scan Frequency—61-65KHz
- Vertical Scan Frequency—55-65Hz
- Horizontal Retrace—3.3usec max.
- Vertical Retrace—450usec max.

Sun-3/160M Black and White Monitor

The Sun-3/160M workstation uses either a Phillips or Moniterm brand monitor. There are minor differences between the two; however, both monochrome monitors receive these inputs:

- Horizontal Sync (HSYNC)
- Vertical Sync (VSYNC)
- ECL Video (VIDEO +,-)
- 120/230 VAC

The monochrome monitors share these operational characteristics:

- Visual Display— 900 x 1152 pixels*
- Horizontal Scan Frequency—62.5KHz
- Vertical Scan Frequency—66.67Hz
- Horizontal Retrace—4.48usec
- Vertical Retrace—600usec

* Display size can be changed to 1024 x 1024 pixels with EEPROM programming and CPU board PAL changes. (Refer to the EEPROM programming section.)

Gray Scale Monitor

The gray-scale monitor shares physical characteristics with the monochrome monitor, yet requires installation of a color board in the pedestal. The color board provides the monitor with 256 levels of white through the green and sync cables.

The gray scale monitor also requires a special cable for connection to the green and sync jacks, which is described in the Removal and Replacement procedures (*Chapter 3* of this manual).

Gray Scale monitor characteristics are:

- RS-170 compatible Video input
- Combined TTL sync input
- Visual Display— 900 x 1152 pixels
- Horizontal Scan Frequency—61.8KHz
- Vertical Scan Frequency—66Hz
- Horizontal Retrace—3.3usec max.
- Vertical Retrace—450usec max.

2

Diagnostics and Troubleshooting

2

Diagnostics and Troubleshooting

2.1. Scope of This Chapter

This section provides:

- A description of a normal boot-up sequence, and procedures to follow when power-up self test fails;
- interpretation of the LED code that indicates which self-test is in progress or failed during boot-up;
- the information necessary to interact with an auxiliary terminal during a boot with the diagnostic switch in DIAG (up) position;
- information on EEPROM programming and
- a basic troubleshooting flowchart to be used in conjunction with the diagnostics manuals referenced there.

This chapter is intended to aid in Sun-3/160 Workstation fault isolation, during the course of which you may need to reload the UNIX operating system from the distribution tapes, and reconfigure the system. *Installing Unix*, Sun PN 800-1317 provides the information needed to perform such tasks.

This section is not intended to be a complete troubleshooting guide; it merely aids the operator or service personnel in utilization of existing workstation capabilities when additional resources are unavailable.

2.2. Related Documents

For information on the use of more sophisticated diagnostic tools, more information on the PROM monitor program, and for help with UNIX refer to these documents:

- *Sun Diagnostics Manual*, Sun PN 800-1361
- *Sun-3 Boot PROM Diagnostic User's Document*, Sun PN 800-1309
- *Writing Device Drivers for the Sun Workstation*, Sun PN 800-1195
- *System Administration for the Sun Workstation*, Sun PN 800-1150
- *Installing Unix on the Sun Workstation*, Sun PN 800-1317

2.3. Conventions Used in This Chapter

Anything printed in typewriter font in this text is a reproduction of a screen display, such as:

```
Autoboot in progress...
```

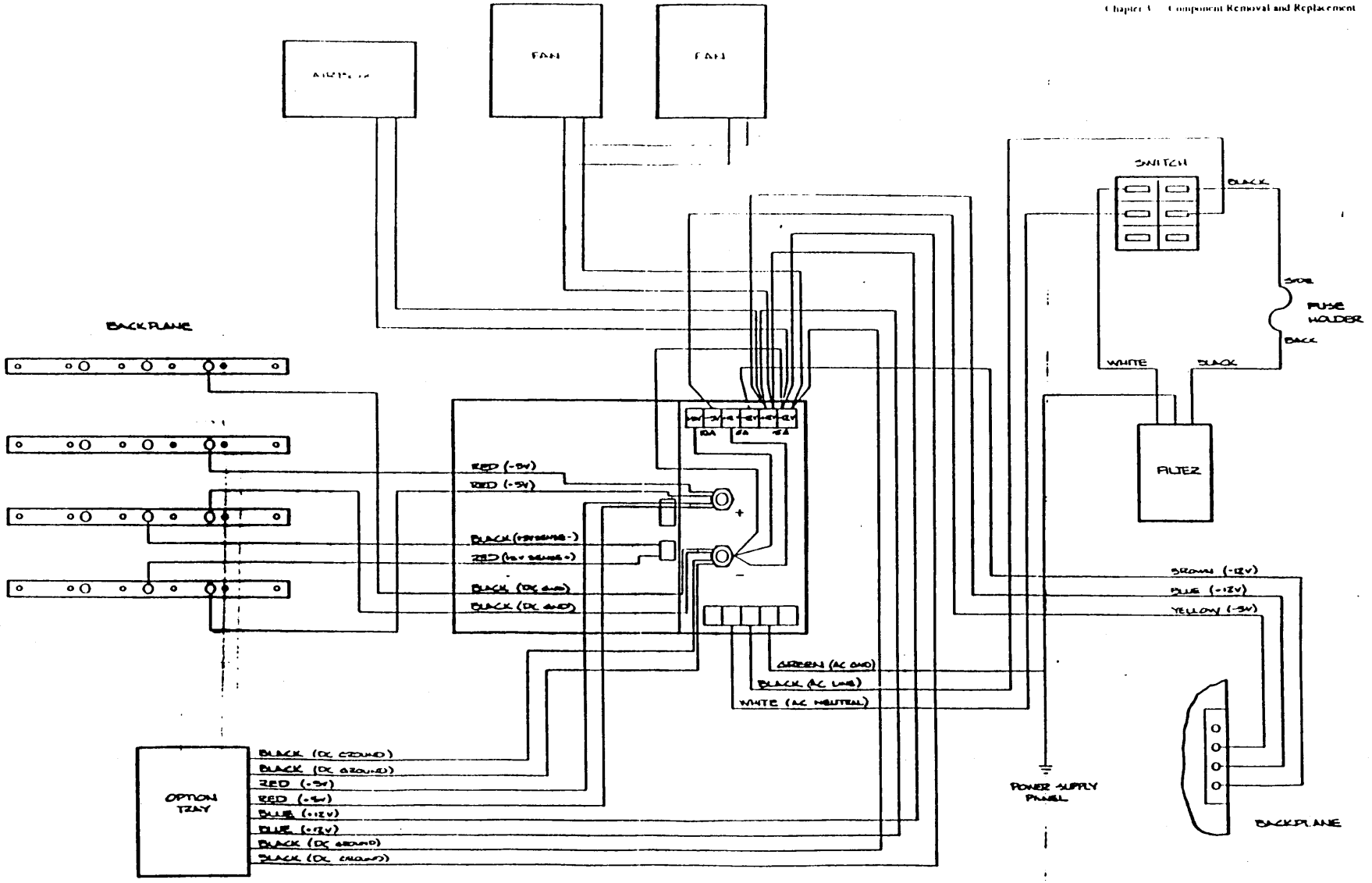


Figure 3-7 *Pioneer Power Supply Connections*

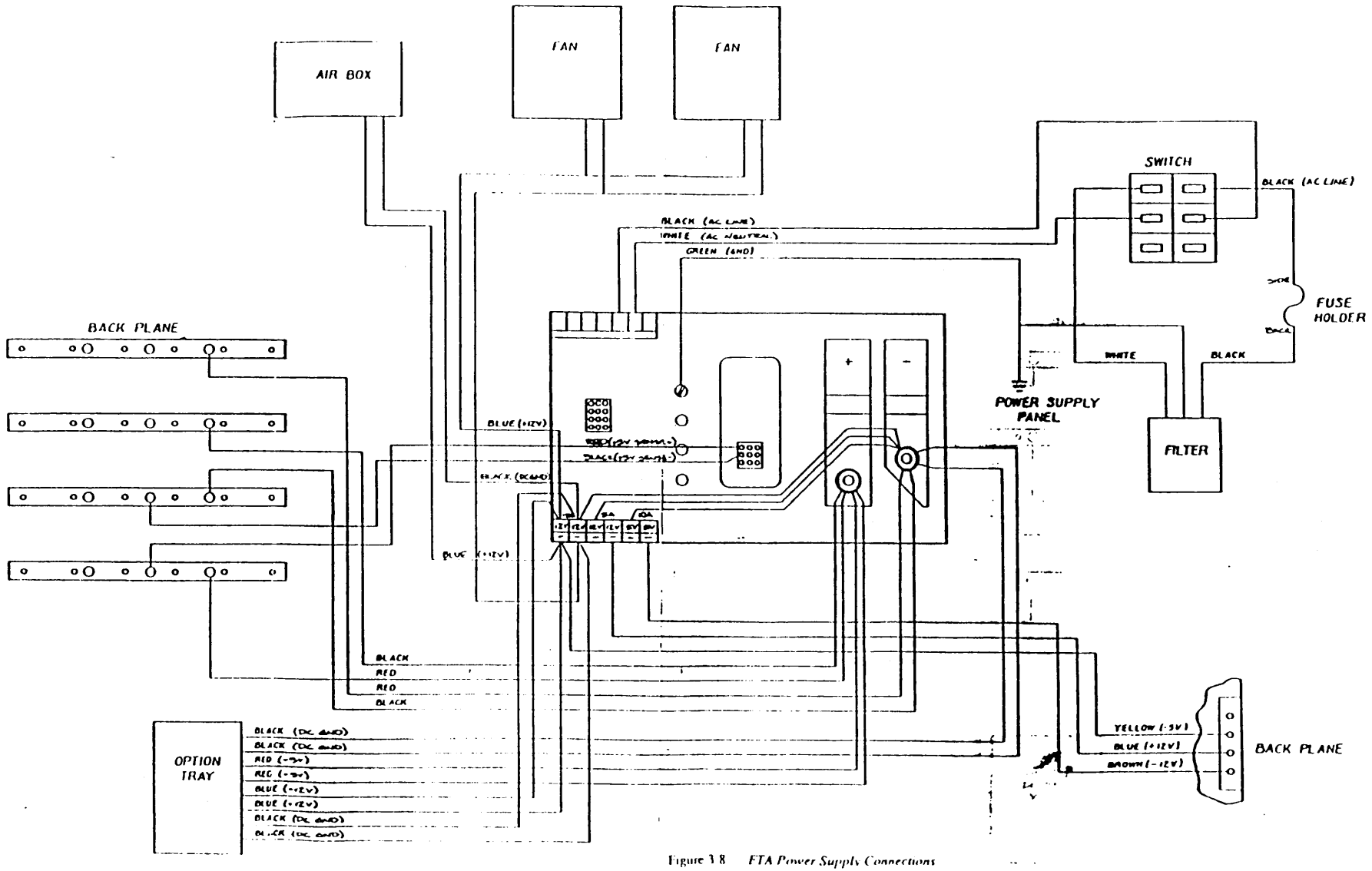


Figure 3-8 *FTA Power Supply Connections*

Boldfaced text within that display means that you must enter that information exactly as shown. For example:

```
>b sd (0,0,0)
```

Text printed in italic typewriter font indicates that the display may vary (the login prompt, for example), or that your input will vary (your login name, for instance). For example:

```
Hostname#:  your.login.name
```

Roman Italic font is used for titles of or chapters within documents, and boldfaced Roman font is used for emphasis:

Chapter 2 of *The Sun-3/160 Field Service Manual.*

The bottom LED always lights.

Hexadecimal values in the text are preceded with *0x*, and the leading zeros (in memory addresses, for example) are not shown:

0x18

2.4. Graceful Power-Down

If the system is running and you want to power-down, ensure that the system administrator has warned clients or other workstation users to log out, and, as super-user, entered a command such as:

```
/etc/halt
```

on the console keyboard. The program called by this command ensures that all data in the buffers is written to disk before UNIX is halted.

When UNIX† is halted, turn system power off.

2.5. The Reset Button

Pressing the reset button, located on the CPU board edge (refer to Figure 2-1), invokes a watchdog reset. What happens after that depends on EEPROM programming (described in Subsection 2.9):

- Self-tests restart, or
- The system invokes the PROM monitor program and this display:

  ```
  Watchdog Reset
  >
  ```

  Once in monitor mode, you may use any of the PROM monitor commands, which are described in Subsection 2.8.

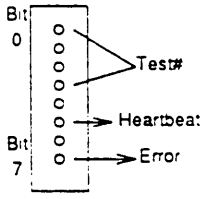
† UNIX is a trademark of AT&T Bell Laboratories.

2.6. Normal Start-up

This subsection begins with a normal startup, then briefly describes the interactive diagnostic boot-up that is used for troubleshooting when the system refuses to boot. The *Sun-3 Boot PROM Diagnostic User Document* provides a comprehensive view of the latter boot.

Under normal or default circumstances, during which the diagnostic switch is in the NORM (BOOTSTRAP on some early systems) position when the system is powered up, the monitor program performs a self-test of CPU functions that are necessary for program loading and execution (booting UNIX or stand-alone diagnostic programs).

Normal LED Patterns



The eight LEDs, located on the edge of the CPU board and visible from the rear of the pedestal, all light briefly, then very rapidly flash a binary code to indicate which self-test is running. Table 2-1 interprets LED self-test codes; Figure 2-1 shows their location on the edge of the CPU board.

After a successful self-test, the "monitor heartbeat" LED in bit position five pulses steadily to indicate that the CPU is receiving clock interrupts. At this point the monitor is in quiescent state and/or UNIX is in boot state. Once UNIX is running, the LEDs light sequentially, in rapid order, from the topmost LED to the bottom LED and then back to the top, and continue to do so as long as the CPU is processing or waiting to process instructions.

NOTE *The last self-test will consume a variable amount of time, dependent on the quantity of memory that is tested. (The LEDs may appear to freeze when a large quantity of memory is tested.)*

Automatic Boot-up

After a successful self-test, the system performs a non-interactive, automatic boot-up, provided that you did not abort the auto-boot.

The example below represents the sort of display that comes up on the console screen during an automatic boot following power-up. Italicized values will vary, depending on the unique characteristics of the workstation:

```
Selftest completed successfully.

        Sun Workstation, Model 1234567, Sun-3 keyboard
        ROM Rev 1.0, 4 MB memory installed, Serial #1234
        Ethernet address 11:22:33:44:55:66

Autoboot in progress...
Boot: sd (0,0,0)
Boot: sd (0,0,0) vmunix
```

The display of the Sun logo, workstation model number and keyboard type are software selectable options that are determined by an EEPROM parameter. (Subsection 2.9 describes EEPROM programming.)

The message:

```
sd (0,0,0) vmunix
```

indicates the type of device from which UNIX is booting (the example represents a SCSI disk based workstation), and indicates the controller, drive, and partition or file numbers in parentheses. The acronym "vmunix" stands for "virtual memory UNIX", which is booted automatically if you have not specified a particular file that you want booted. If you were booting from tape and specified a file after the parentheses, the name of that file would appear in place of `vmunix`.

A number of informative messages concerning the automatic boot-up process scroll by on the console screen while UNIX is booting.

Following the

```
Autoboot in progress...
```

message, a program checks to ensure file system integrity, and attempts to repair any inconsistencies. If the program makes any repairs, they are listed in the message. This condition is most likely to occur if the system was powered down or reset without using the `/etc/halt` command.

Unless you abort the process and invoke the monitor program, you will receive a login prompt when UNIX is booted.

To Abort the Auto-Boot

On the system console keyboard, hold down the [L1] key while pressing the **a** key following the self-test sequence to abort the auto-boot and invoke the monitor program.

If you are using a terminal as the console, press [BREAK] to abort the auto-boot. If you abort the auto-boot process, you will receive the monitor prompt:

```
>
```

At this point you may enter any of the PROM monitor commands, followed by the appropriate argument, as described under Heading 2.8.

Redirecting Console I/O

When booting with the diagnostic switch in NORM position, EEPROM programming determines whether the autoboot display attempts to come up first on the color or monochrome monitor, or on a terminal that is connected to Serial Port A or B.

If the system is a 160M or 160C and the boot PROM does not find the presence of a console keyboard, it will expect input from Serial Port A, although the console screen will still display the boot-up messages.

You can also program the EEPROM to cause the system to look for user interaction only from a terminal keyboard that is connected to Serial Port A or B, or you can use the monitor **u** command to temporarily change I/O devices (refer to Heading 2.8 on monitor commands).

No Console Display?

If the EEPROM is programmed for output to a monitor that is not functioning, the LEDs will indicate that UNIX is booting, but nothing will appear on the console screen. If this should occur:

- Check to make sure that the diagnostics switch is in NORM position, then
- wait until the LEDs are lighting in the "walking ones" pattern (described under *Normal LED Patterns*) and abort the auto-boot to invoke the PROM monitor program. You may now either:

1. use the PROM monitor **q** command to change the contents of the EEPROM address location that specifies the console device (in case it is programmed incorrectly) even though you have no display;
2. Use the monitor **ua** command to temporarily redirect the display to serial port A (provided you have a terminal attached to it);
3. or you may reboot with the diagnostic switch in the DIAG position and interact with an auxiliary terminal (refer to the *Diagnostic Boot-Up* subsection).
4. If the workstation is a Sun-3/160C and the color monitor is not working, you may power-down and remove the monitor and the color board, and connect a monochrome monitor. When you reboot, the display will default to the monochrome monitor when the program does not find the presence of a color board.

The *Setting up Console I/O* heading under *EEPROM Programming* explains how to change the identity of the console device or primary terminal — the device through which you and the processor communicate.

Failure to Boot

If an error is found during self-test, CPU board diagnostic LEDs, visible from the rear of the pedestal (refer to Figure 2-1), freeze in a pattern that indicates which self-test failed.

The bottom LED (Bit 7) always lights when an error occurs. NOTHING APPEARS ON THE CONSOLE SCREEN; THE SYSTEM DOES NOT BOOT-UP. If this happens, record the pattern of the lighted LEDs as well as you can, if the pattern is repeating, and follow the procedures outlined in the following paragraphs to reboot with the diagnostic switch in DIAG position.

2.7. Diagnostic Boot-Up

Boot-up with the diagnostic switch in the DIAG (up) position in order to:

- repeat the self-tests and view informative messages on the auxiliary terminal;
- verify that the CPU board is at fault when the system refuses to boot;
- determine which part of the CPU board is failing;
- finish the self-tests and attempt to boot UNIX in spite of self-test errors;
- choose from a menu of Ethernet, drive interface, serial port, memory and video tests; or
- invoke an EEPROM selected diagnostic program.

Prerequisites

If you wish to repeat certain self-tests, view self-test error messages or continue self-tests in spite of error messages, you must:

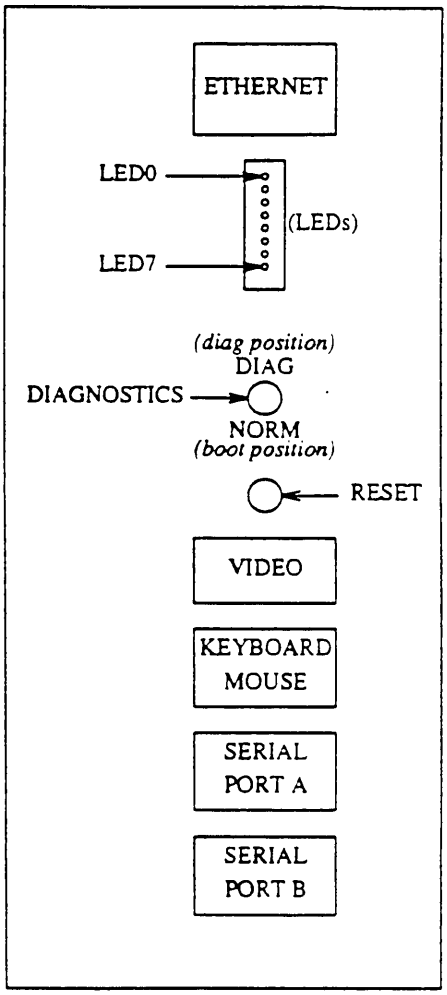
1. Use a null modem cable (Sun PN 530-1056) to connect a video display terminal to Serial Port A on the pedestal before booting.
2. Set the terminal attributes for 9600 BAUD, 8 data bits, one stop bit, and no parity.

To perform a diagnostic boot-up from either a terminal or the workstation console:

1. Switch the diagnostic switch on the back of the CPU board to the DIAG position.
2. Switch the pedestal and monitor power ON. Do not use the `L1-A` sequence or a reset prior to initiating a diagnostics boot-up; doing so may cause self-test errors. If the system is already running, power-down and then power-up again.

Figure 2-1, below, shows the location of the connectors, LEDs, and diagnostic switch on the CPU board edge, viewed from the rear of the pedestal.

Figure 2-1 *CPU Board Connector Edge*



Null Modem Cable Wiring

The null modem cable is wired as follows:

Pins 2 and 3 are crossed

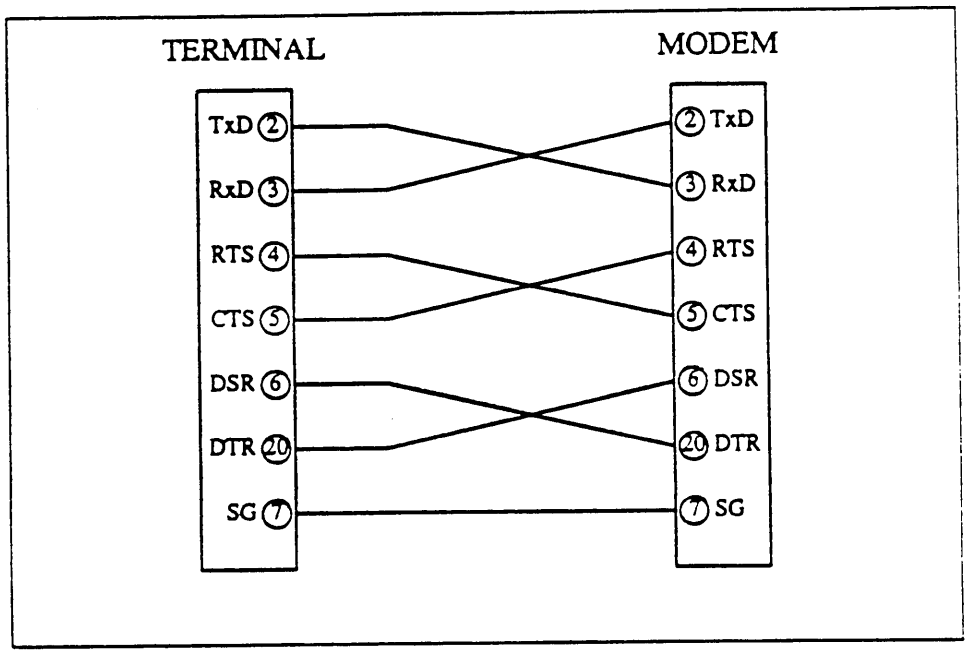
4 and 5 are crossed

6 and 20 are crossed

and pin 7 is wired straight through.

"Pins 2 and 3 crossed" means that the signal entering the cable on pin 2 emerges on pin 3, and vice versa (see the figure below). The connector on the left is the Serial I/O Port on the CPU board; the connector on the right is the terminal (DTE).

Figure 2-2 *Null Modem Cable Pin Arrangement*



Refer to the manual that comes with the terminal to make certain that the signals needed to operate the terminal are provided at the correct pins of the serial port. Refer also to *System Administration for the Sun Workstation*, part number 800-1150. and *Installing UNIX on the Sun Workstation*, part number 800-1317, which detail connecting to a terminal.

Self-Test Interaction

When the diagnostic switch is in the DIAG (up) position and workstation power is switched ON, the auxiliary terminal display identifies the self-tests that the program is running, as each test starts (refer to Figure 2-3).

If you wish to restart the automatic self tests at any point prior to the display

```
Selftest Completed Successfully.
```

on the terminal screen, enter **s** on the terminal keyboard.

To cause the tests to continuously cycle, enter **b** at this point.

Successful Self-Test Display

The example below is the message that will appear on the terminal (connected to Serial Port A) screen when the CPU has passed all the self-tests.(The memory size reported is dependent on system configuration.)

NOTE *If no terminal is connected to the serial port, you will not be able to interact with the self-tests, and you won't see the Diagnostic Boot-Up Display shown below. If self-test is successful, however, the Extended Test Menu (shown on the following page) will be offered for selection on the console screen. During self-test, the console screen will remain dark, and the LEDs will be the only indication of self-test status.*

Figure 2-3 *Diagnostic Boot-Up Display*

```
BootPROM Selftest

PROM Checksum Test
DVMA Register Test
Context Register Test
Segment Map RAM Wr/Rd Test
Segment Map Test
Page Map Test
Memory Path Data Test
NXM Bus Error Test
Interrupt Test
MMU Protection/Status Tests
Parity Error Tests
Sizing memory (size = 00000004 MBytes)
Memory Test (Testing 00000004 MBytes)

Selftest Completed Successfully

Optional Menu Tests
Type a character within 10 seconds to enter Menu Tests...
```

At this point you may press any key on the terminal keyboard to view the Extended Test Menu on the terminal screen, or wait 10 seconds for this display to appear on the console screen:

If you do not select the Extended Test Menu, the boot PROM will first attempt to display this message on a color monitor. If it finds no color board, but does find the presence of a workstation keyboard, it will direct output to a monochrome monitor. Finding neither, the program looks for input from a terminal keyboard connected to Serial Port A. I/O parameters stored in EEPROM are ignored during a diagnostic boot.

```
Selftest Completed Successfully

        Sun Workstation, Model 1234567, Sun-3 keyboard
        ROM Rev 1.0, 4 MB memory installed, Serial #1234
        Ethernet address 11:22:33:44:55:66

Optional Menu Tests
Type a character within 10 seconds to enter Menu Tests...
```

If you do not press a key on the console keyboard, the Boot PROM program checks parameters stored on EEPROM that tell it to do one of the following:

- Boot a specific (diagnostics) program from a specific device
- Boot UNIX.
- Drop into the monitor mode (PROM monitor commands are listed in Table 2-2).

If you press a key, the Extended Test Menu will be offered:

```
Extended Test Menu: (Enter 'q' to return to Monitor)

Cmd - Test

ie - Intel Ethernet Test
kb - Keyboard Input Test
me - Memory Test
mk - Mouse/Keyboard Ports Test
tm - TapeMaster bootpath
rs - Serial Ports Test
sd - SCSI disk Bootpath
st - SCSI tape Bootpath
vi - Video Test
xt - Xylogics Tape Bootpath
xy - Xylogics Disk Bootpath

Cmd=>
```

The *Sun-3 Boot PROM Diagnostic User's Document* and the *Sun Diagnostics Manual* contain detailed descriptions of each extended test and submenu. You will need a special loopback connector (described in the Diagnostics documents) to perform the serial port tests on the extended test menu.

A diagnostic boot-up automatically tests all memory that is present in the system. For this reason, there is a slight pause during the display

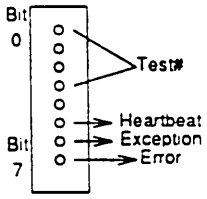
```
Memory Test (Testing 4 MBytes)
```

and prior to the message

```
Selftest Completed Successfully.
```

The LED pattern for Test 15 also remains lighted until the memory test is complete.

When the CPU Fails a Test



If the CPU board fails one of the boot PROM self-tests, the program continuously repeats that test and displays an error message on the auxiliary terminal that describes the fault. This cycling process is called a scope loop, and provides an opportunity to study the problem with test equipment.

When a test detects an error, the bottom LED lights, and the top five LEDs freeze in a pattern that represents the failed test number. (Refer to the example to left of this text.)

If the LED in bit position 6 (second from the bottom) lights, an exception class failure, such as a bus or address error trap, or an unexpected interrupt has occurred.

When self-tests begin, all the LEDs light briefly, and then the top LED (bit 0) lights when Test 1 begins. If Test 1 fails, LED 7 also lights. (Table 2-1, *LED Interpretation*, illustrates the pattern displayed for each test.

To Go On Testing

If an error message indicates that a test has failed, and you want to continue to the next test regardless, press the space bar on the terminal. In this way, you may continue through the remainder of self-tests, and attempt to boot UNIX in spite of the error; or, after the remaining tests complete successfully you may press BREAK to enter the monitor program.

To Read the LED Table

Table 2-1 provides a brief interpretation of the patterns displayed by the LED indicators on the edge of the CPU board. The LEDs are actually arranged on the CPU board vertically, rather than horizontally as presented in this table. The LED depicted on the left in this table is located at the top of the display; the LED on the right is at the bottom of the display.

Table 2-1 *LED Interpretation*

LEDs ● = ON, ○ = OFF 0							7	*What the System is Doing When These LEDs Are Cycling*	*What Might Be Bad If This Indication Stays On And LED 7 Lights*
●	●	●	●	●	●	●	●	A reset sets LEDs to this state	CPU or PROMs bad
●	○	○	○	○	○	○	○	Test 1 checking the boot PROM	Boot PROM
○	●	○	○	○	○	○	○	Test 2 checking DVMA Register	CPU Board
●	●	○	○	○	○	○	○	Test 3 checking the Context Register	CPU Board (MMU)
○	○	●	○	○	○	○	○	Test 4 Segment Map RAM Rd/Wr Test	CPU Board (MMU)
●	○	●	○	○	○	○	○	Test 5 checking Segment Map RAM	CPU Board (MMU)
○	●	●	○	○	○	○	○	Test 6 checking Page Map RAM	CPU Board (MMU)
●	●	●	○	○	○	○	○	Test 7 checks memory data path	CPU Board
○	○	○	●	○	○	○	○	Test 8 checks bus error detection	CPU Board
●	○	○	●	○	○	○	○	Test 9 checks interrupt capabilities	CPU Board
○	●	○	●	○	○	○	○	Test 10 checking MMU read access	CPU Board
●	●	○	●	○	○	○	○	Test 11 checking MMU write access	CPU Board
○	○	●	●	○	○	○	○	Test 12 writing to invalid page	CPU Board
●	○	●	●	○	○	○	○	Test 13 tries to write to protected page	CPU Board
○	●	●	●	○	○	○	○	Test 14 performs parity error check	CPU Board
●	●	●	●	○	○	○	○	Test 15 performs parity error check	CPU Board
○	○	○	○	●	○	○	○	Test 16 performs memory tests	CPU Board
○	○	○	○	○	○	○	●	Self-Tests have found an error	CPU Board
○	○	○	○	○	○	●	○	An Exception Class error was found	CPU Board
○	○	○	○	○	●	○	○	Self-Test done, UNIX in boot-state (LED is blinking)	CPU Board
● ⇒	○⇒	○⇒	○⇒	○⇒	○⇒	○⇒	○	"Walking Ones" pattern	UNIX running okay

2.8. The PROM Monitor

The boot PROM stores a program known as the "monitor" that contains self-tests and controls system operation during boot-up until the UNIX kernel takes over. The monitor program is invoked when you use the **L1-a** command, and is identified with the > prompt.

This subsection provides information on commands entered following the monitor prompt to perform a variety of tasks, such as booting from alternate devices, changing the console output to a serial port, and so on. Commands that are self explanatory on the Monitor Help Menu are not included in this discussion; commands that require arguments and further understanding are explained following the Help menu example. Access the monitor as previously described, then enter **h** to view a "Help" table of monitor commands that looks something like this:

Table 2-2 *Monitor Help Menu*

Cmd	*Parameters*	*Description*
a	*digit*	open CPU address registers (0-7)
b	*device (cont,unit,part or file)*	bootload a file and start it
c	*address*	continue program at this address
d	*digit*	open CPU data registers (0-7)
e	*address*	open address as 16-bit word
f	*start_adr end_adr patrn_size*	fill memory with pattern
g	*address*	go to given address
h		display this help table
k	*number*	reset (0) CPU (1) mmu ,(2) system
l	*address*	open address as a 32-bit long word
m	*address*	open the Segment Map
o	*address*	open address as an 8-bit byte
q	*address*	open the EEPROM
r		open CPU registers (i.e. PC,SR)
s	*digit*	set or query Function Code (0-7)
t	*command*	trace (y)yes,(n)no,(c)continuous
u	*argument*	use different console devices
v	*start_adr end_adr size*	display memory in Hex and ASCII
w		vector
x		Extended Diagnostic Tests
z		set a breakpoint

Monitor Command Syntax

If no argument or parameter is entered after the **a, c, d, e, f, g, l, m, o, q, or r** commands listed in Table 2-2, the action is performed on a default location. For instance, if you enter the **q** command alone, the first address assigned to the EEPROM is displayed.

Entering [RETURN] immediately following the display of the contents of a location causes the contents of the next location to be displayed. A space and then [RETURN] returns the monitor prompt.

Other commands, such as **u**, require arguments and therefore will display a menu of argument choices.

The next few paragraphs provide additional information on parameter choices that affect the function of the commands listed in the Help Menu. Note that any changes made with these commands (with the exception of the **q** command for EEPROM programming) are valid only until the system is powered down. Parameters changed with the **q** command take effect when you power cycle the system, and remain in effect until you use the **q** command again to change them.

NOTE *You may use either upper or lower case to enter these commands and values.*

Monitor Command **b**

In order to boot from a device other than that specified in EEPROM, the **b** command must be followed with one of these abbreviations:

xy — Xylogics 440/450 disk
sd — SCSI disk
ie — Intel Ethernet
st — SCSI tape
xt — Xylogics 472 Tape
mt — Tape Master 9-Track Tape

The *sd, st and xy* arguments are followed with parentheses that optionally enclose the controller number, unit number, and partition or file number:

```
>b sd(0,0,0)
```

The default values 0,0,0 are used if you do not enter values inside the parentheses. You may also add a filename after the parentheses, to boot only the specified file.

You may boot from SCSI tape without entering anything between the parentheses, to receive a boot prompt, after which you enter the location of the file you have selected.

```
>b st()
boot: st(0,0,0)
boot: st(0,0,1)
```

Monitor Command **k**

The **k** command argument is a number that specifies the desired reset level:

0 = CPU instruction reset
1 = CPU instruction and MMU (Segment and Page Maps) Reset
2 = CPU instruction, MMU and memory reset

Note that, in systems that contain a Version 1.4 or older Boot PROM, the **k2** command does not initialize the Ethernet control register or the SCC chip on the CPU board. For this reason, press the User Reset button on the CPU board edge before you use this command. The reset button invokes a watchdog reset, which reinitializes the register and the SCC. (Note that EEPROM programming may cause the system to reboot following a watchdog reset.)

Monitor Command **q**

The **q** command opens the EEPROM to allow examination or modification of configuration parameters. If you do not enter an address following the command, the content of the first address assigned to the EEPROM is presented. (EEPROM addresses are off-set, rather than complete addresses.)

```
>q[RETURN]
>EEPROM 000:some value?
```

Subsection 2.9 lists the addresses and values that must be entered in order to change various aspects of workstation configuration, such as Sun Logo display during boot-up, the default boot device, and so on.

To change the value of a specific EEPROM address, simply enter **q**, the address, and [RETURN]. When the program displays the contents of that register, enter the new value, and [RETURN]:

```
>q 1f[RETURN]
>EEPROM 01f: 10? 11  [RETURN]
```

The value present in the next location will now be displayed.

To exit from the modify mode after an entry, enter a period and [RETURN] or press [RETURN], the space bar and then [RETURN] again.

To exit from the modify mode when you have not entered a new value, simply press [SPACE] and [RETURN] after the question mark.

Monitor Command **s**

The **s** command sets or queries the address space to be used by subsequent memory access commands. The processor function codes decode the address spaces, which are described in Chapter 1 of this manual. Argument choices represent the function codes:

0 = Reserved
1 = Device Space (User Data)
2 = Device Space (User Program)
3 = Control Space
4 = Reserved
5 = Device Space (Supervisor Data)
6 = Device Space (Supervisor Program)
7 = CPU Space

If you do not enter a function code number, the current setting (either 1 or 5) is displayed, and entry of the monitor **o** command, for example, would cause the program to look for the specified address in either user or supervisor data space. Conversely, if you reset the function code number, you could query registers in the space represented by the number entered. For example, entering

```
>s 3
```

would allow you to read the bus error or system enable register, which are located in Control Space.

Monitor Command t

A **y** argument to the **t** command causes the monitor to display one instruction at a time. The **c** argument causes a continuous display of program instructions, which can be momentarily stopped with [CTRL] s and restarted with [CTRL] q. This command is not necessary for field service diagnostics, and would primarily be used for development purposes.

Monitor Command u

The **u** command requires an argument to specify from which device(s) you want the system to expect input or which device(s) will display output.

If you do not enter an argument after the u command, the program will display the current settings. If no serial port is specified when changing baud rates, the baud rate of the current input device is changed. The default serial port baud rate is 9600.

Upon normal power-up (diag switch is in NORM position), the default console input device is the Sun keyboard, unless the EEPROM has specified another default input device. If the keyboard is unavailable, the system looks to serial port A for for input.

The default console output device is the Sun monitor (subject to change through EEPROM programming). If the workstation is a Sun-3/160C and a color board is unavailable, the program will look for a monochrome monitor as an output device.

You may alter the existing I/O settings while you are in the monitor mode, using the commands listed below; however, the default settings will be reinstated when the system is power cycled.

Monitor Commands to Change I/O:

- Enter **u a** or **u b** to select serial port A or B as the input and output device.
- Enter **u aio** or **u bio** to select serial port A or B as the input and output device.
- Enter **u ai** or **u bi** to select serial port A or B for input only.
- Enter **u ao** or **u bo** to select serial port A or B for output only.
- Enter **u k** to select the keyboard for input.
- Enter **u ki** to select the keyboard for input.
- Enter **u s** to select the screen for output.
- Enter **u so** to select the screen for output.
- Enter **u ks, sk** to select the keyboard for input and the screen for output.
- Enter **u a***baud rate* or **u b***baud rate* to set the serial port speed.
- Enter **u e** to cause the output to echo the input.
- Enter **u ne** to cause the output not to echo the input.
- Enter **u** *address* to set the serial port virtual address.

Monitor command **v**

This command allows you to view the hexadecimal values, as well as the ASCII equivalent, present in the addresses you enter. You must enter the complete address, as opposed to an offset address such as an EEPROM address. You specify the format with a second argument, selected from these:

b for byte format
w for word (16-bit) format
l for long word (32-bit) format

For example, to view the contents of locations 00 to ff in 16-bit format, enter:

```
>v 0 ff w[RETURN]
```

If you do not specify a format, the display will be in long-word format.

To suspend scrolling of the display, press [RETURN], then press it again to restart the display. To quit out of the viewing process and display the monitor prompt, press the [SPACE] bar.

Monitor Command **w**

The **w** command should be used for programming purposes to cause the specified arguments to be passed to your routine. The command is not necessary for field service diagnostics.

Monitor Command **x**

The **x** command presents the menu of Extended Diagnostic Tests that can also be accessed during diagnostic boot-up. Subsection 2.7 provides more information on those tests.

2.9. EEPROM Programming

The CPU board has an electrically erasable, programmable memory (EEPROM) chip that can be accessed through the boot PROM monitor in order to change system configuration parameters.

NOTE *These procedures are for systems that have a Version 1.4 or higher Boot PROM installed on the CPU board.*

This heading covers entry of EEPROM parameters that control these functions:

- vary the quantity of memory tested during self-test;
- change the console display size parameters;
- change the action that follows a watchdog reset;
- boot from a specified device with diagnostics switch on NORM, or poll the devices;
- recognize the specified device as the primary terminal or console;
- display the Sun logo or a custom banner during power-up;
- turn the keyboard "click" on or off;
- boot a selected program from a specific device with diagnostics switch on DIAG;
- Store a system configuration record on EEPROM.

Table 2-3 shows the EEPROM address locations for the parameters listed above.

Table 2-3 *EEPROM Address Space Allocation*

Location	*Function*
0x14	MBytes of installed memory
0x15	MBytes memory tested
0x16	Display screen size
0x17	Watchdog reset function
0x18 to 1D	Choose polling or specify boot device
0x1F	Set console (primary terminal) I/O
0x20	Choose boot display banner
0x21	Turn keyboard "click" on or off
0x22 to 0x26	Select diagnostic boot device
0x28 to 0x4f	Store diagnostic boot path
0x68 to 0xb7	Store custom banner
0xbc to 0x123	Store system configuration

NOTE *You may need to use the Installing UNIX manual (shipped with this workstation) in conjunction with some of these procedures, which require information on disk or tape partitions, file numbers, and so on.*

These paragraphs will describe how to open the offset addresses shown in Table 2-3 in order to read and modify the contents. You will first gracefully power-down the system as described at the beginning of this section, then power-up and enter the monitor program after self-tests are successful: Simultaneously press the **L1** key (upper left-hand corner of the keyboard) and the **A** key. You have now aborted your present session and accessed the monitor program. The monitor displays as its characteristic prompt the "greater than" symbol:

```
>
```

To access the EEPROM now, type the letter **q**, followed by the EEPROM address that you want to examine or modify. You may user either upper or lower case characters to enter monitor commands or write to the EEPROM.

```
>q 1f
```

NOTE *You may use either upper or lower case characters to enter the* **q** *command or any of the hexadecimal values needed for EEPROM programming.*

The program will now display the contents of address 0x1f in the EEPROM, which is the value that determines which device is considered the system console:

```
>EEPROM 01F: some value?
```

To update the contents of this location, enter the new value immediately following the displayed value, and then a carriage return. You have now written the new value to address 0x1f — and automatically incremented to the next address. In this example, you are replacing the value 0x00 with the value 0x10:

```
>EEPROM 01F: 00? 10 [RETURN]
>EEPROM 020: some value?
```

Now, to stop incrementing EEPROM addresses and receive the monitor prompt again, press [SPACE] and [RETURN]. Now you can open a new EEPROM address, or verify the change you just made:

```
>EEPROM 020: some value? [SPACE] [RETURN]
>q 1f [RETURN]
>EEPROM 1F: 10? . [RETURN]
>
```

To see the effect of your EEPROM programming, you must reinitialize the system. The next few headings show you how to change the parameters listed at the beginning of this section.

Setting Quantity of Memory Tested

The quantity of memory present in the system is recorded at EEPROM location 0x14, and can be viewed when that location is opened:

```
>q 14 [RETURN]
EEPROM 014:some value? [RETURN]
```

The quantity of memory to be tested during boot-up with the diagnostic switch in NORM position is recorded in location 0x15, and should agree with the value in location 0x14, if all of memory is to be tested. To view the contents of address 0x15, press [RETURN] immediately after the quantity of memory is displayed, and the prompt will look like this:

```
EEPROM 015:some value?
```

To change the value of location 0x15, simply enter the new value after the question mark, enter a period and [RETURN], for the monitor prompt.

Changing Monitor Display Size

The contents of EEPROM address 0x16 help determine whether the video monitor display size will be the standard 900x1152, or 1024x1024 pixels. The contents of address 0x16 will read 0x00 for the standard display, and 0x12 for the 1024x1024 display. To change to the 1024x1024 display, enter:

```
>q 16 [RETURN]
EEPROM 016:00?12 . [RETURN]
>
```

To complete the display size change, PROM U2208 at location A-24, and PROM U2202 at location A-27 on the CPU board must be changed. To obtain the replacement PROMs, contact a Sun sales office.

Changing Action that Follows Watchdog Reset

EEPROM address 0x17 determines what happens after a watchdog reset:

- Write 0x12 in location 0x17 to restart self-tests and reboot after a watchdog reset.
- Write 0x00 to that location to invoke the monitor after a watchdog reset.

Selecting the Boot Device

Ordinarily, when the system boots with the diagnostic switch in NORM position, (BOOTSTRAP on early workstations) and EEPROM address 0x18 contains the value 0x00, the monitor program polls boot devices in this order:

- It first checks to see if a disk controller is present, and if so, attempts to boot from it.
- If the polling sequence does not find a disk controller, the Ethernet controller on the CPU board is polled and becomes the boot device.

Boot Device Codes:
xy = Xylogics 440/450 disk
sd = SCSI disk
ie = Ethernet
st = SCSI tape
mt = Tape Master 9-Track
xt = Xylogics 472 Tape

To delete the polling sequence and change the normal boot device, you must open the EEPROM to address location 0x18 and change the contents from 0x00 (which causes polling) to 0x12 (to delete polling). You must then fill the next two address locations with a two-byte ASCII string that represents the new boot device. (Device codes are shown in the left margin.) Finally, you must open the next three addresses and write values that represent the controller, unit and partition or file number.

For example, this read/write sequence would make Ethernet the default boot device:

ASCII equivalent of hex values shown here:

69 = i
65 = e

```
>q 18[RETURN]
EEPROM 018:some value? 12[RETURN]
EEPROM 019:some value? 69[RETURN]
EEPROM 01A:some value? 65[RETURN]
EEPROM 01B:some value? 0[RETURN]
EEPROM 01C:some value? 0[RETURN]
EEPROM 01D:some value? 0[RETURN]
EEPROM 01E:some value? .[RETURN]
>
```

The sequence shown above represents the entry: ie(0,0,0).

Setting Up Console I/O

To open the EEPROM address that determines which device will display the boot-up dialogue and act as console or the primary terminal — the device over which you and the processor will communicate — enter:

```
>q 1f[RETURN]
```

After the program displays the contents of EEPROM address 0x1f, enter the hexadecimal value assigned to the device you want to act as the console, then press RETURN. Choose from:

00 = monochrome monitor
10 = serial port A
11 = serial port B
12 = color monitor

To test this set-up, press the space bar and [RETURN], then reboot with the diagnostic switch in NORM position. If you selected one of the serial ports, the boot-up informative messages should appear on the screen belonging to a terminal that is connected to the indicated port.

If you selected the color monitor, a color board must be present in the pedestal cardcage, with the appropriate cables connected.

Changing the Banner

To change the Sun banner that appears during boot-up, enter

```
>q 20 [RETURN]
```

which will open the EEPROM address that pertains to that display. The monitor will echo the address you entered and display some value (0x00 for Sun Logo display), which you must change to the hex value 12, to delete the Sun banner display during boot-up:

```
>EEPROM 020:00 12          [RETURN]
```

You have just instructed the monitor program not to display the banner that includes the Sun Logo. To create a new banner, you must now write the hex value for ASCII blanks (0x20) or the hex equivalent of a new ASCII string into locations 0x68 to 0xb5.

NOTE *If you do not fill locations 0x68 to 0xb7 (80 characters) with appropriate hex numbers after you have changed the contents of address 0x20 to 0x12, you may see garbage in place of the Sun banner when you boot-up.*

The last two addresses, 0xb6 and 0xb7, must contain 0x0d and 0x0a, which represent the ASCII code for carriage return and line feed.

To create a custom banner, after you have written the value 12 into address 0x20, press the space bar and then return, and access address 0x68:

```
>q 68 [RETURN]
>EEPROM 068:some value?
```

Then begin entering the hexadecimal code for the new banner immediately after each address is displayed. Appendix E contains an ASCII conversion chart to aid you in selecting values that represent the characters you want displayed in place of the Sun banner.

You can use the monitor v (view) command to view the characters you have just written, but you must enter the complete address where the logo begins, rather than the offset address 0x68. The complete address for this EEPROM location begins at 0xfe04000.

NOTE *The banner you have created will be displayed the next time you power-up and reboot the system. If you entered all blanks (except for the carriage return and line feed values), there will be no banner upon power up.*

'urning Keyboard Click On r Off

The value in EEPROM location 0x21 determines whether or not the keyboard will make a "clicking" noise when you type. Use the procedures described at the beginning of this EEPROM section to access location 0x21 and view or change the contents:

To turn the keyboard click OFF:

```
>q 21
EEPROM 021:012 00
```

To turn the keyboard click ON:

```
>q 21
EEPROM 021:000 12
```

Selecting the Diagnostic Boot Device

If you switch the diagnostic switch to the DIAG position and then boot without specifying either `vmunix` or a boot device and path that indicates where the diagnostic program is located, the system may drop into monitor mode, displaying the ">" prompt.

You can program the EEPROM so that, when the diagnostic switch is in DIAG position, and you enter

```
>b
```

with no arguments, the monitor program will be able to find a specified diagnostic program your file systems, or will automatically boot UNIX. To do this, you must first enter parameters that specify whether to boot from Ethernet, disk or tape. Then you must enter the path that tells the boot PROM where it can find the selected program in your file systems (see the heading, *Setting the Diagnostic Boot Path*).

If you want to invoke the monitor program during a diagnostic boot, you simply enter zeroes in addresses 0x22 through 0x4f.

The EEPROM addresses 0x22 and 0x23 contain the hexadecimal values that represent the selected boot device. For example, locations 0x22 and 0x23 might contain the values 0x73 and 0x64, respectively — the hex equivalent of ASCII "sd", for SCSI disk.

The next three bytes (0x24 through 0x26) contain the hexadecimal values that literally represent the controller, unit and partition or file numbers specific to the chosen device. In other words, these bytes represent the part of the boot command that is enclosed in parentheses:

```
>b sd (0,0,0)
```

To set the "diagnostic boot device", obtain the monitor prompt as described at the beginning of this section, and access EEPROM address 0x22:

```
>q 22
EEPROM 022:00
```

A hexadecimal value will be displayed as the contents of address 0x22, as shown above.

To specify a diagnostic boot device, simply enter the hex equivalent of the first letter that represents the new device — you can use the ASCII/Hex Conversion Chart in Appendix E — press [RETURN] and then, when the contents of location 0x23 are displayed, enter the value for the second letter than represents the device. (Entering **b ?** after the **>** prompt will give you a list of possible boot device choices.)

NOTE *To ensure that diagnostics are* **not** *invoked after self-test, and that the system drops into monitor mode during a boot-up with the diagnostic switch in DIAG position, enter zeroes instead of hex values.*

If you have entered values to specify a boot device, press [RETURN] again and write the controller, unit and partition or file numbers into addresses locations 0x24, 0x25 and 0x26, respectively. You do not need to use ASCII characters for these values. Simply enter one hexadecimal value in each location, and press [RETURN].

If you have specified the monitor mode, enter zeroes in all three locations.

Now, if you have specified a boot device, you are ready to use up to forty bytes, beginning with EEPROM address 0x28, to represent your complete diagnostic boot path. The values you enter represent any of the following:

1. the location that you have chosen to store the selected diagnostic program.
2. the acronym *vmunix*, which means "virtual memory UNIX,
3. or, zeroes to invoke the monitor program after self-test, during a diagnostic boot.

Setting the Diagnostic Boot Path

You have just programmed the EEPROM to tell the boot PROM monitor program what device, controller, unit and partition or file number to boot from during a diagnostic boot-up.

Now you must use the same method to tell the monitor one of the following:

1. Where in your file systems the selected diagnostic program is located;
2. that you want UNIX to boot after self-test when the diagnostic switch is in DIAG position and you have not selected Extended Tests;
3. or that you want the monitor program to be invoked after self-test when you do not select Extended Tests.

For example, if you want to tell the monitor that the selected diagnostic program is located in the `/usr/stand` directory, you would first open EEPROM address 0x000028:

```
>q 28 [RETURN]
```

The program would then display the contents of location 0x000028, after which you would begin entering the hexadecimal equivalent of your diagnostic path. (Appendix E can help you with ASCII/Hex conversions.) You are allowed forty bytes, or the equivalent of forty characters for your path name, and the last value you enter must be 0x00.

To enter `/usr/stand`, for example:

```
EEPROM 028: some value 2f[RETURN] (for /)
EEPROM 029: some value 75[RETURN] (for u)
EEPROM 02A: some value 73[RETURN] (for s)
EEPROM 02B: some value 72[RETURN] (for r)
EEPROM 02C: some value 2f[RETURN] (for /)
EEPROM 02D: some value 73[RETURN] (for s)
EEPROM 02E: some value 74[RETURN] (for t)
EEPROM 02F: some value 61[RETURN] (for a)
EEPROM 030: some value 6e[RETURN] (for n)
EEPROM 031: some value 64[RETURN] (for d)
EEPROM 032: some value 00[RETURN] (to end)
```

To select UNIX, use Appendix E to determine the hexadecimal equivalent for each character in the acronym `vmunix`, and enter those values in the addresses beginning with 0x28. All other locations in the forty-byte block should be zeroes.

If you are specifying that the monitor program is invoked during a diagnostic boot, ensure that locations 028 through 0x4f contain zeroes.

Recording System Configuration

EEPROM locations 0xbc through 0x123 contain values that represent the types of factory installed printed circuit boards present in the system as well as information on the internal configuration of those boards and external devices that they control.

This subsection describes the type of information that can be encoded and stored in these address locations. If a board is not discussed here, the only byte used at this time is the first byte of the block assigned to that board, which identifies it.

The configuration information is contained in 13 eight-byte blocks, to allow for the 12 card cage slots, with one extra block to be used as a sentinel to flag the end of the system configuration.

If there are only four boards in the system, then only the four eight-byte blocks are used, and the sentinel flag is in the fifth block. For example, if one of the four boards is the SCSI board, and it is in slot 7, you do not have to place the SCSI board information in the 7th configuration block.

In this way, when new boards are added to the system, you simply write the configuration information in the location that contains the sentinel block, and then move the sentinel block to the beginning of the next eight-byte block.

If the configuration information is entered to match the board slot assignments, then blocks representing empty slots must contain all zeroes.

The first byte of each eight-byte block refers to the pc board type. Hexadecimal values 0x1 through 0xc identify the various boards that may be installed in the card cage. Values 0x80 through 0xfe are to be used to identify boards other than those installed by Sun. Values 0x0d through 0x7f are reserved for future expansion. The remaining seven bytes contain information that varies, dependent on

the board type.

The block following the last board in the card cage should contain the value 0xff in the first byte, to indicate that this is the end of the configuration.

The value in the first byte of each block is decoded as follows:

1 = CPU
2 = Memory Expansion
3 = Color
4 = Reserved
5 = Floating Point
6 = SMD Disc
7 = 1/2" Tape Controller
8 = Ethernet Controller
9 = Asynchronous Line Multiplexer
a = Graphic Processor/Graphic Buffer
b = SCP
c = SCSI Controller
ff = Sentinel block, indicating the end of the configuration.

The starting addresses for the 12 blocks are:

Block #	*Starting Address*
1	bc
2	c4
3	cc
4	d4
5	dc
6	e4
7	ec
8	f4
9	fc
10	104
11	10c
12	114

The next few paragraphs explain the meaning of other values found in the the eight bytes within the blocks assigned to various boards.

CPU Board Block

If the CPU board block is located at 0xbc, and you use the **q** command to open that location, the contents might look like this:

```
>q bc[RETURN]
EEPROM 0BC: 01?
```

In the example above, the value 0x01 represents the CPU board.

If you immediately press [RETURN], the display presents the contents of the next byte, which represents the quantity of memory (in Megabytes) present on the CPU board (not the whole system), like this:

```
EEPROM 0BD: 04?
```

To change this value, simply enter the new value after the question mark, then [RETURN], to view the contents of then next byte.

The next byte, 0xbe, contains a binary code that represents options present on the board. The two options are:

bit 0 = 68881 FPP chip
bit 1 = DCP (encryption processor) chip

If the option is present on the board, the value of its assigned bit is 1; otherwise the value is zero. If the board has a 68881 installed, but not a DCP, the value at address 0xbe would be 1. If both chips are on the board, the value would be 0x03, which is the binary sum of a "1" in both bit 0 and bit 1. And, of course, if neither option is present on the board, the value would be 0.

Option	*Value*
None	00
FPP only	01
DCP only	02
Both	03

The remaining bytes in this block, at locations 0xbf through 0xc3, are unused at this time, and should contain zeroes.

Memory Expansion Board

Memory Expansion board information begins with the value 0x02. If the location assigned to the memory board is 0xc4 (the first address in the second configuration block), then the first byte should read:

```
EEPROM 0C4: 02?
```

The next byte represents the quantity of memory installed on this board only, and will contain the value 0x04 if four Megabytes of memory are present on the board:

```
EEPROM 0C5: 04?
```

The remaining bytes in this 8-byte block should contain zeroes.

Color Board

The first byte of the color board block contains the value 0x03. The second byte contains the value 0x02 for a Color-2 board, or 0x03 for for a Color-3 board. The remaining six bytes should be filled with zeroes.

SMD Disk Controller Board

The first byte in the SMD Controller block contains the value 0x06. The second byte contains the value 0x01 to represent a Xylogics board.

The third byte contains either 0x00 or 0x01 to represent the controller board number.

The fourth byte represents the number of disks controlled by the board.

Tape Controller Board

The first byte of the Tape Controller Board block contains 0x07.

Values in the second byte are decoded as follows:

0x01= Xylogics board
0x02= other mfg.

The third byte contains either 0x00 or 0x01, depending on the controller board number. The fourth byte represents the number of tape drives controlled by the board.

Asynchronous Line Multiplexer

The first byte of the ALM board block contains 0x09.

The second byte contains a hex value that represents the number of terminals connected to the board.

SCSI Board

The first byte in the SCSI board block contains the value 0x0c.

The next byte differentiates between a SCSI 2 or a SCSI 3 board.

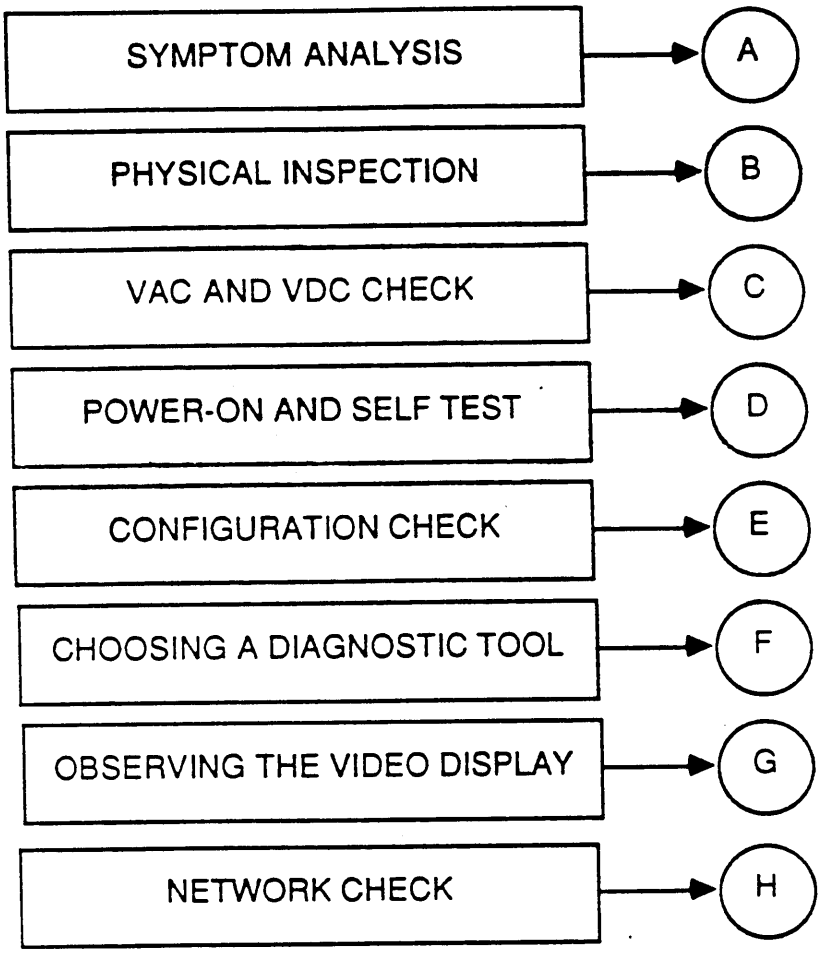
0x2 = SCSI 2
0x3 = SCSI 3

The third byte represents the number of tape drives that are present.

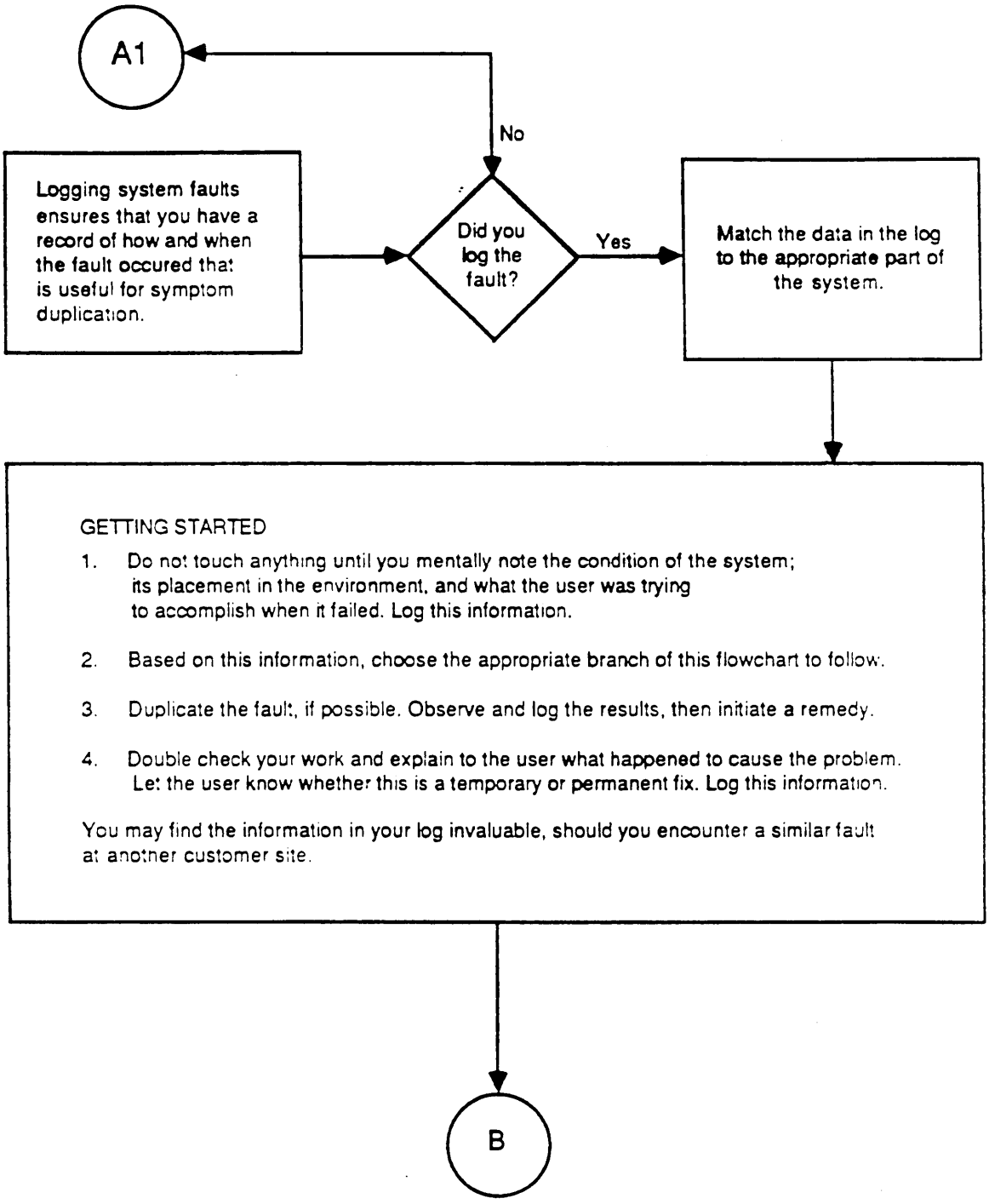
The fourth byte contains the number of disk drives present in the system.

2.10. Troubleshooting Flow Chart

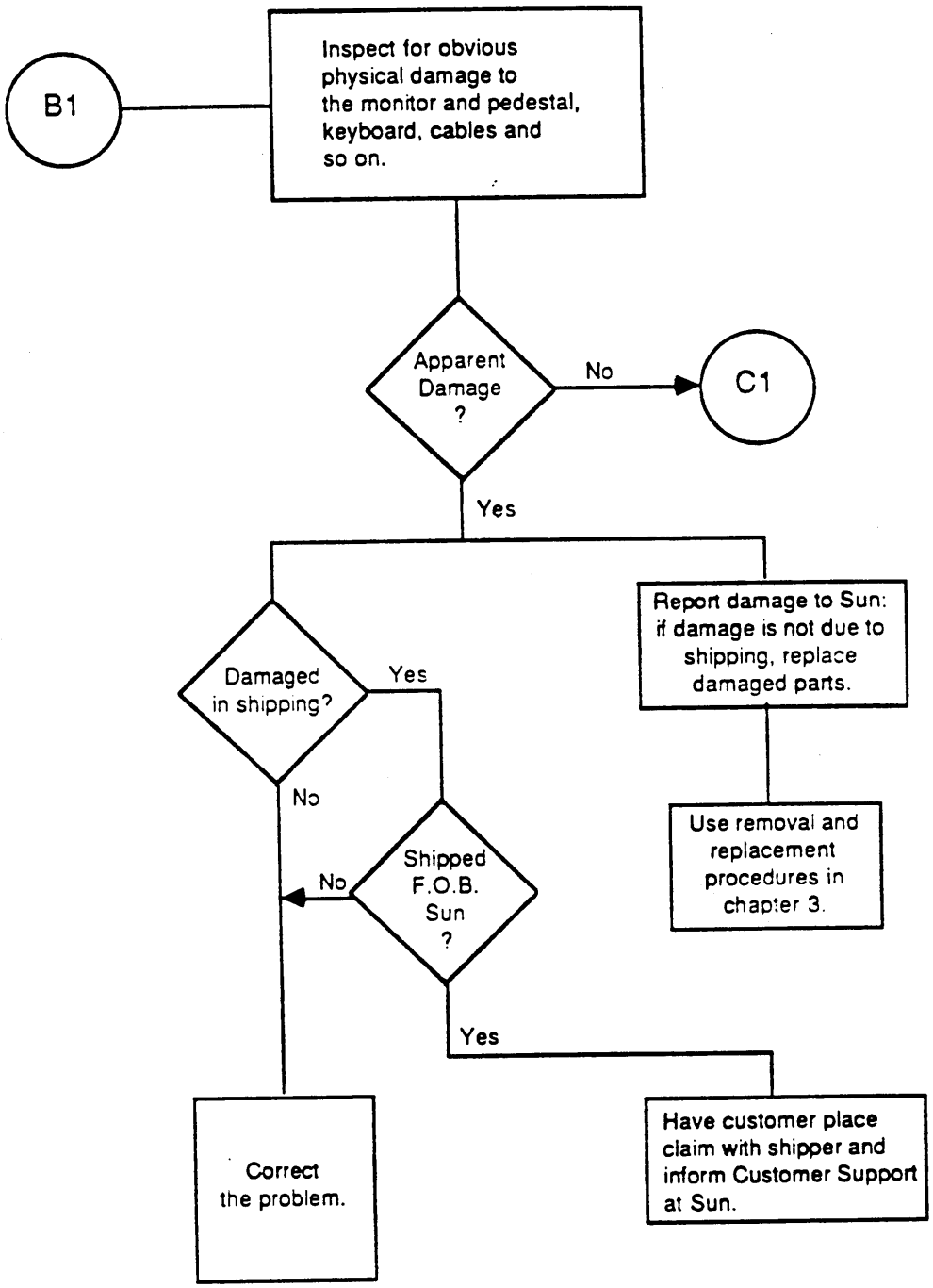
This flowchart is intended for use with the diagnostics that are presently available on the Boot PROM and in the directory specified on EEPROM (refer to Heading 2.9 on EEPROM programming). It is intended to aid you in using the system's diagnostic capabilities and is by no means a complete guide to troubleshooting the Sun-3/160.



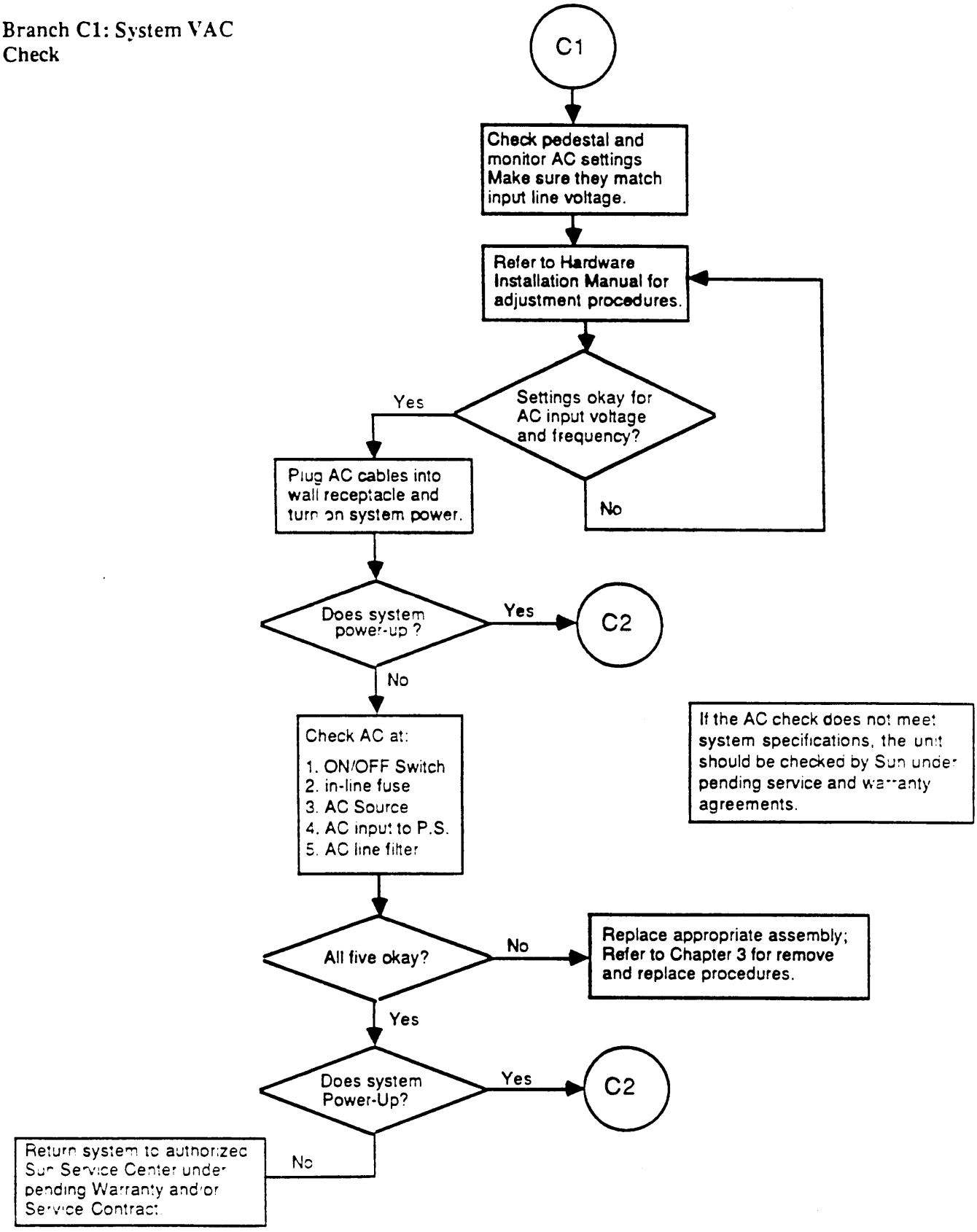
Branch A: Symptom Analysis
Log



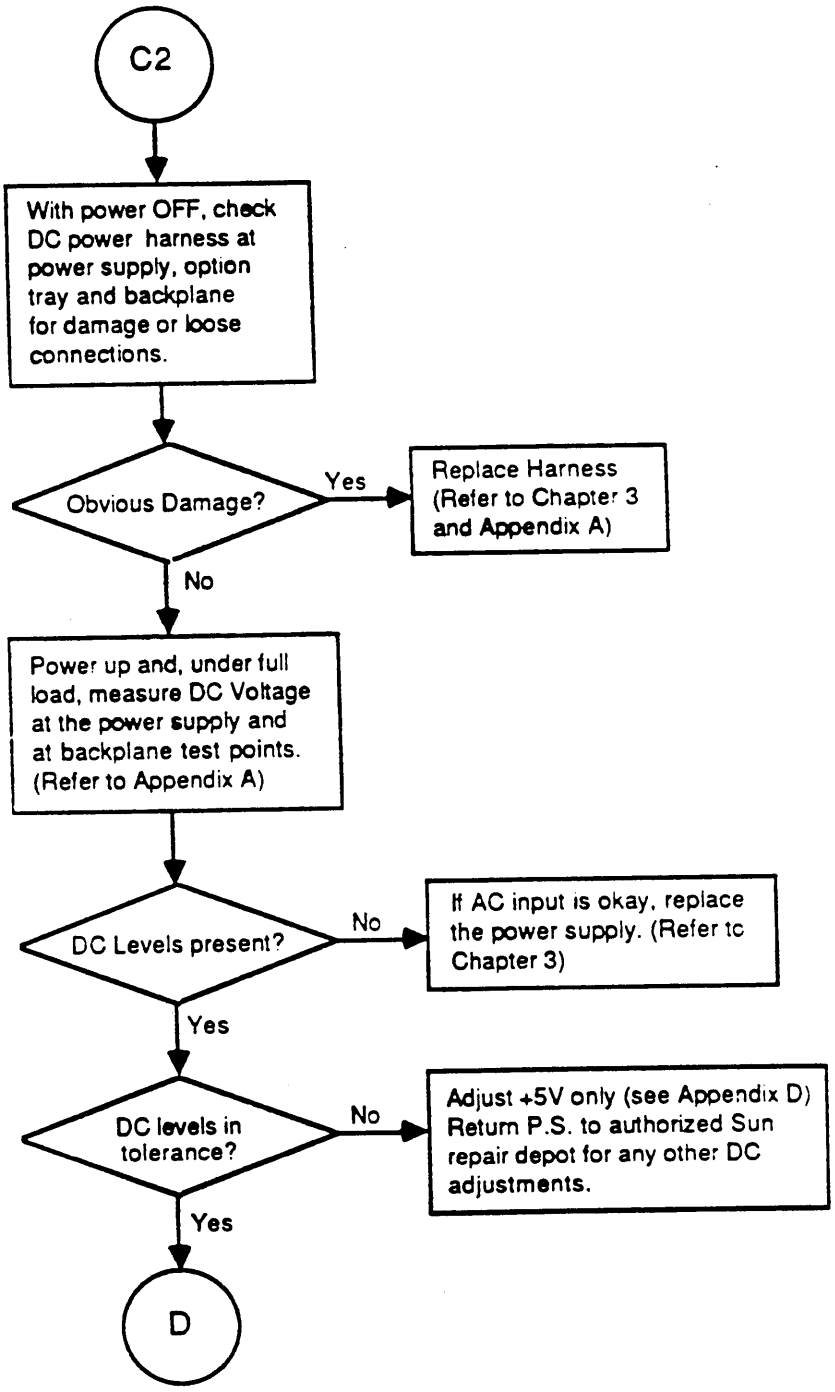
ranch B: Physical Inspection



Branch C1: System VAC Check

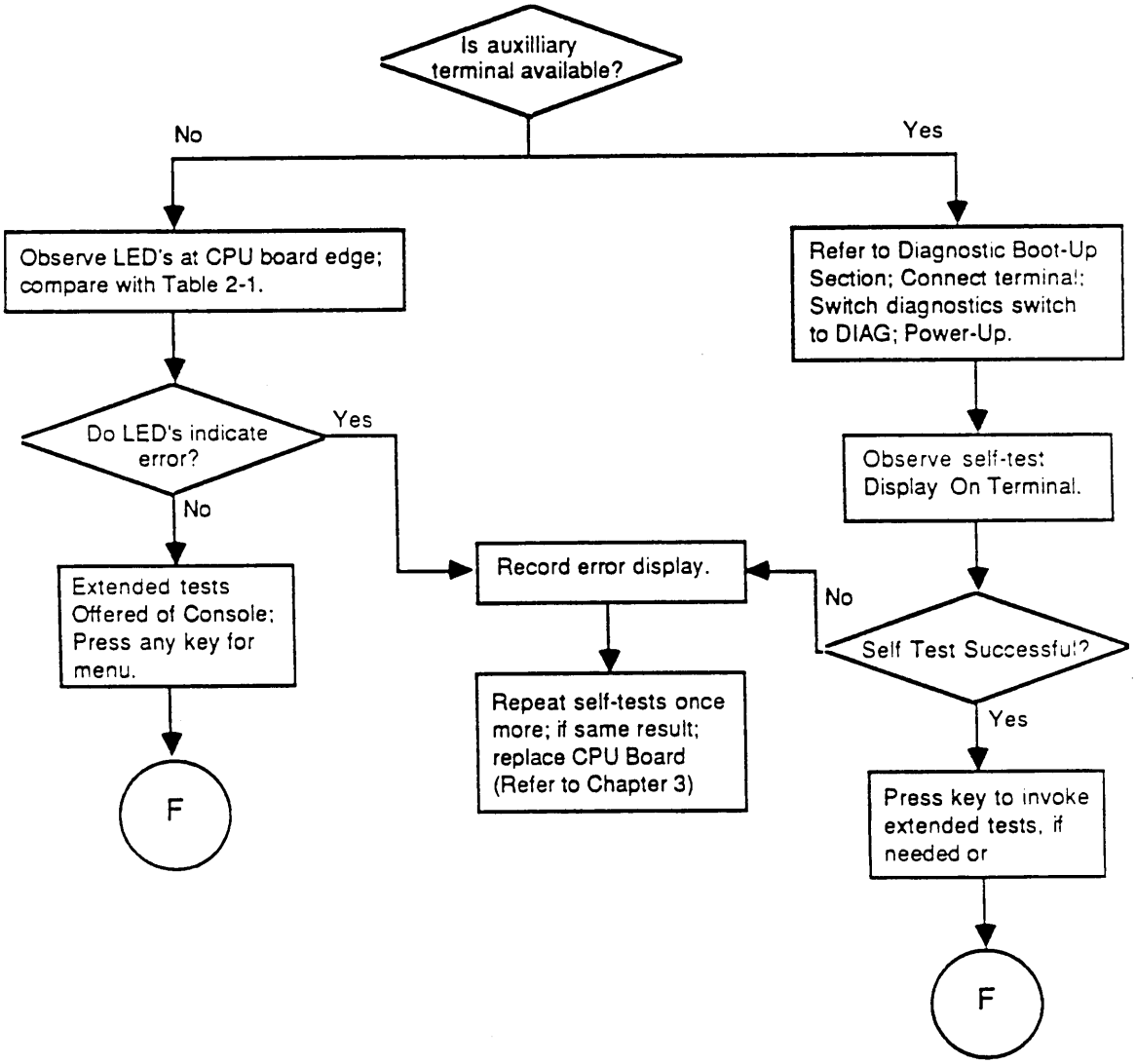


3ranch C2: System VDC Check

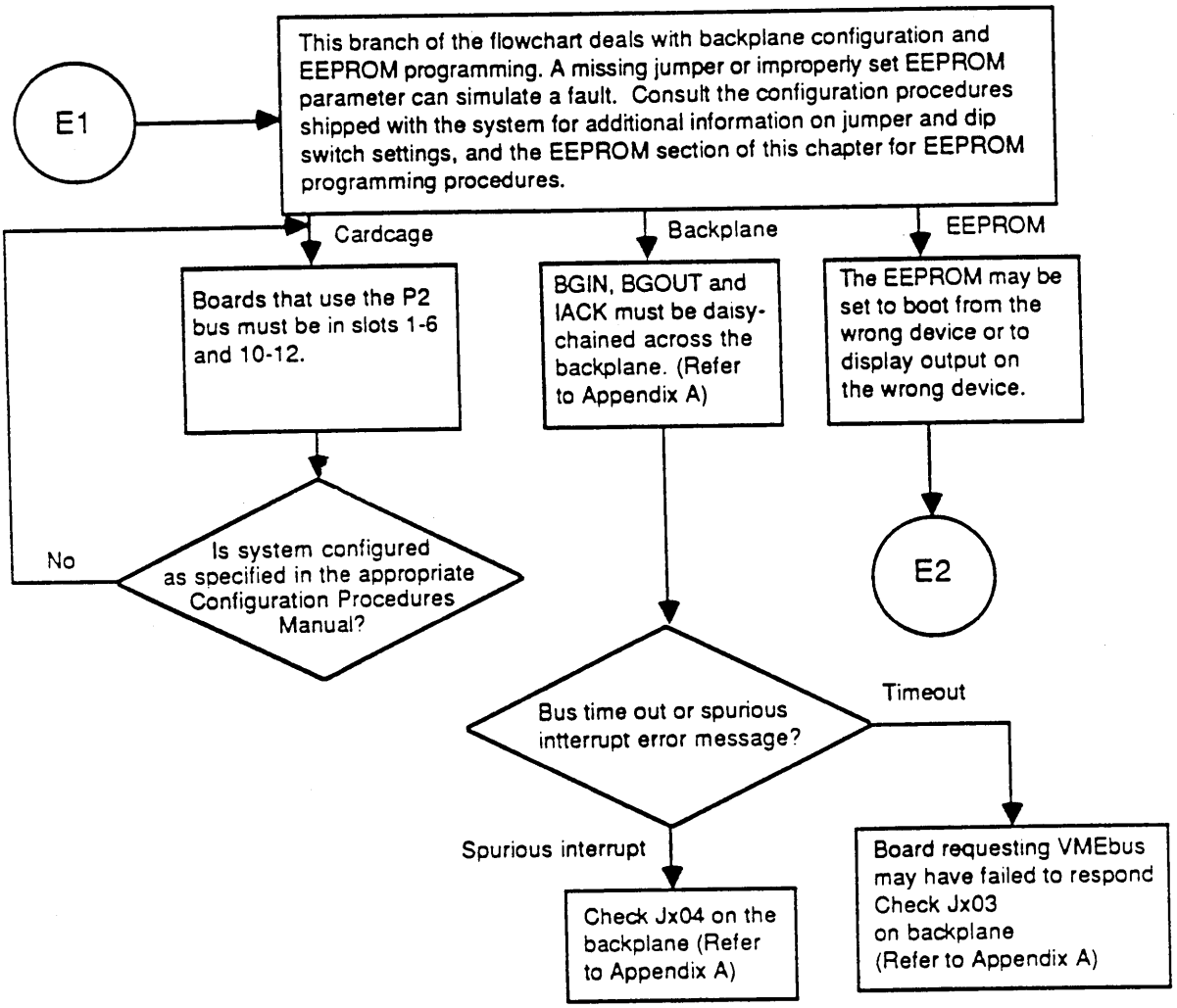


(Refer to P.S. Heading, Chapter 1)

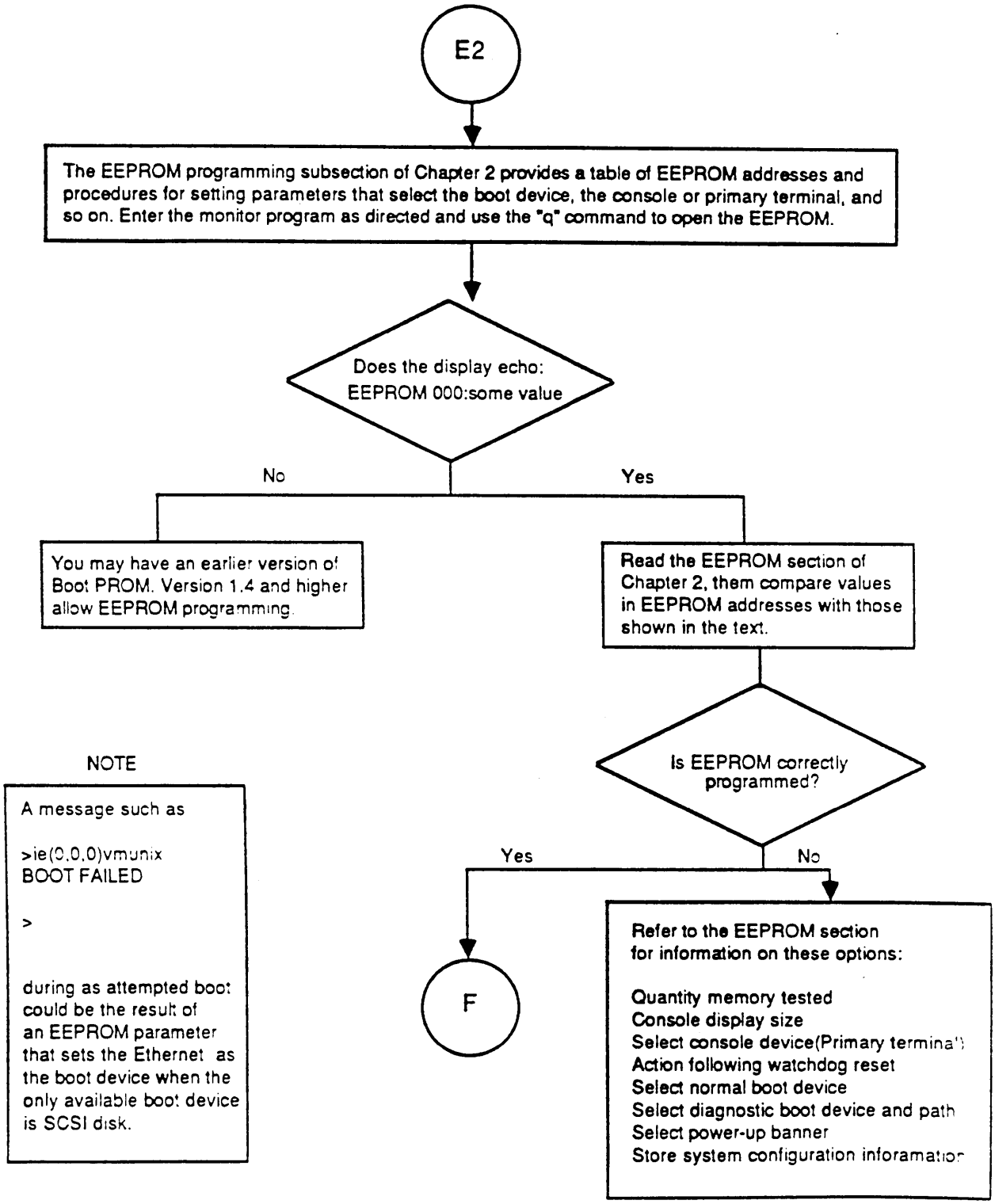
Branch D: Power-On and Self-Test



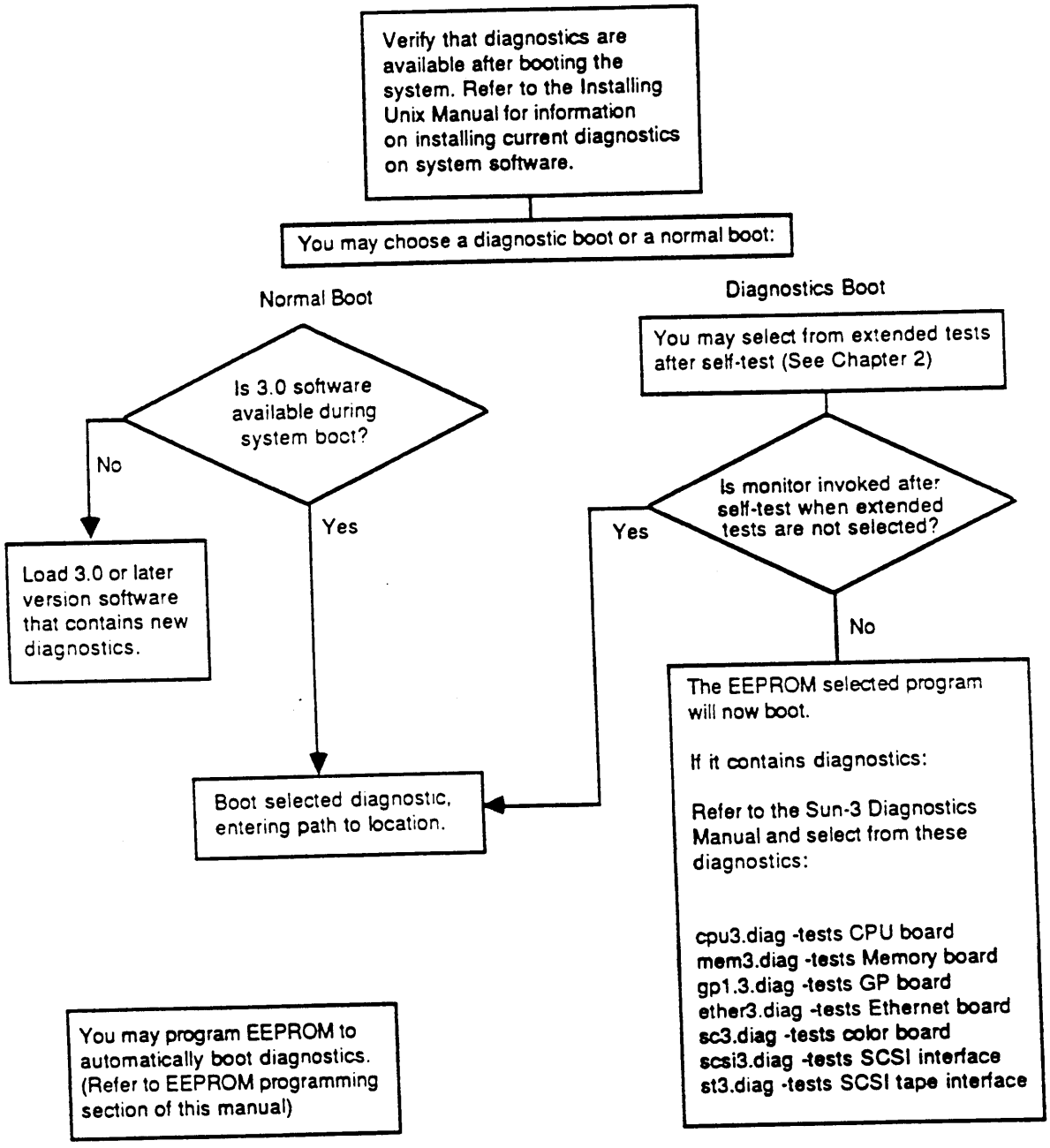
Branch E1: System Configuration Check



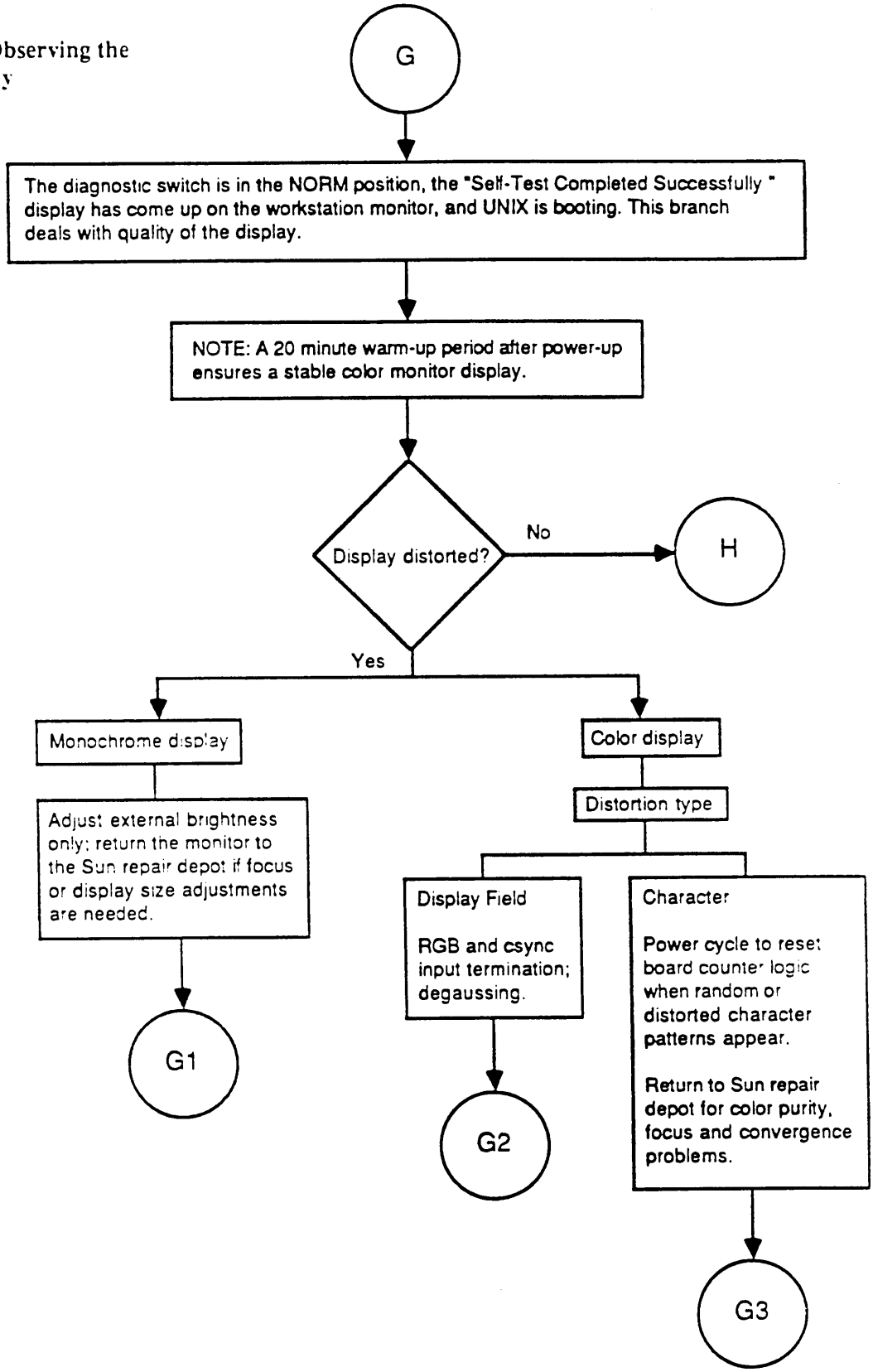
Branch E2: EEPROM Check



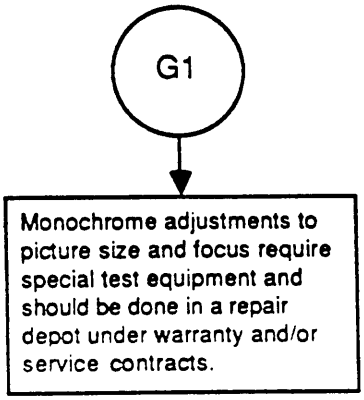
Branch F: Choosing the Applicable Diagnostic Tool



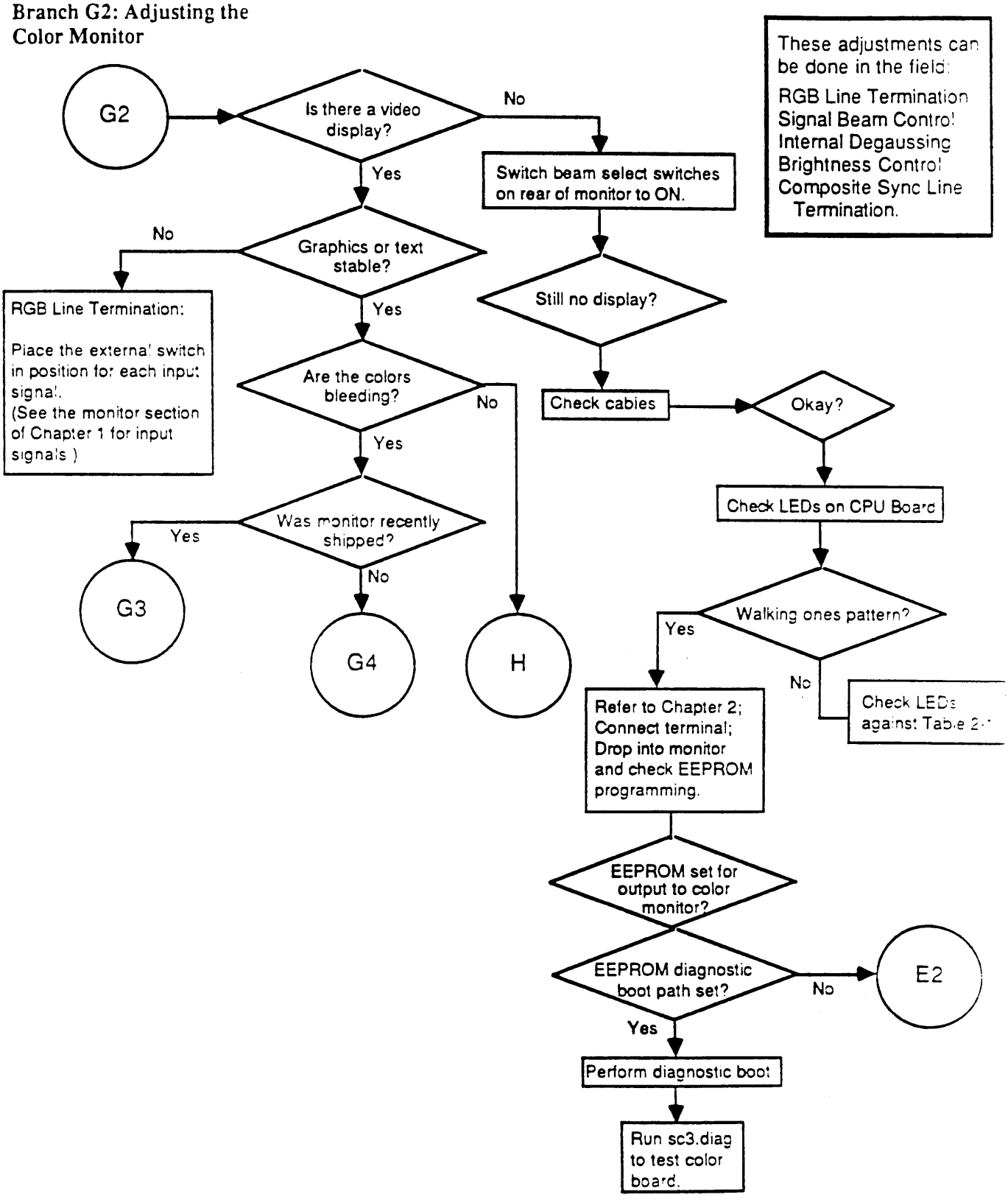
Branch G: Observing the Video Display



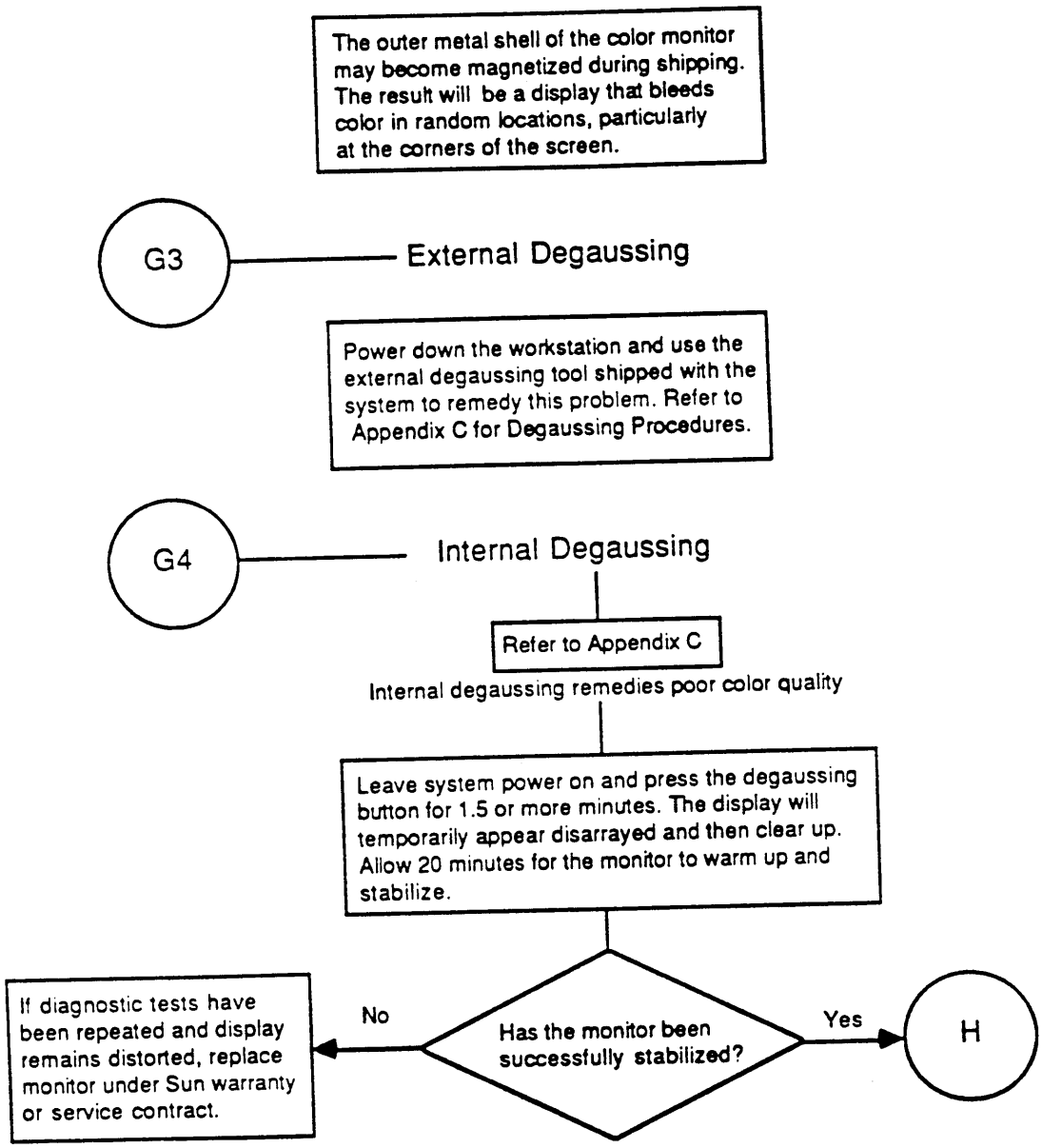
Branch G1: Adjusting the Monochrome Monitor



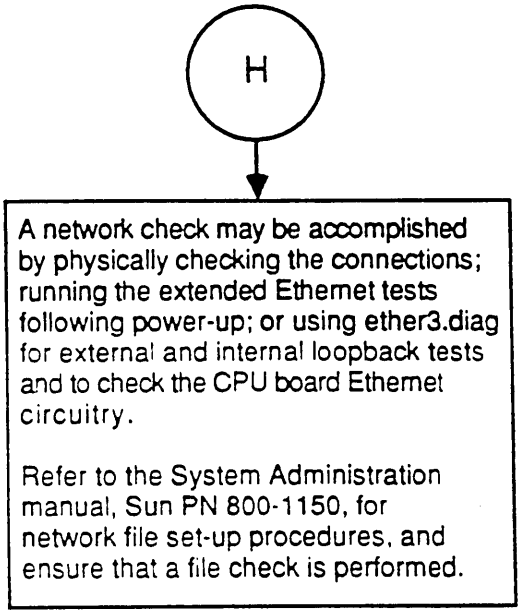
Branch G2: Adjusting the Color Monitor



Branch G3 and G4: Degaussing the Color Monitor



Branch H: Network Check



3

Component Removal and Replacement

3

Component Removal and Replacement

This chapter supplies the information necessary to remove and replace all Sun-3/160 assemblies designated as field replaceable units (FRUs).

There are a relatively small number of Sun-3/160s in the field that differ from the majority of production units in several minor details. When these differences affect the remove-and-replace procedures, this text covers both the standard and the variation.

NOTE *Prior to performing any of these procedures, ensure that the system administrator has performed a system backup, and that the workstation is properly powered down.*

3.1. Graceful Power-Down

Ensure that the system administrator has warned clients or other workstation users to log out, and, as super-user, brought the system down gracefully with a command such as:

/etc/halt

The program called by this command ensures that all data in the buffers is written to disk before UNIX is halted.

When UNIX is halted, turn system power off and unplug the power cord from the wall receptacle.

For more information on system administration, such as shut-down methods and backups, refer to *System Administration for the Sun Workstation*, Sun PN 800-1150.

CAUTION **Before removing any panels or subassemblies, follow the *Graceful Power-Down* procedures and unplug the workstation power cord from the wall.**

3.2. Monitor Removal

To replace a Sun-3/160M or Sun-3/160C monitor (CRT):

1. Power down the monitor and pedestal, then
2. disconnect the pedestal cables from the old monitor and reinstall them onto the new monitor.

To replace the Sun-3/160G monitor:

1. Power down the monitor and the pedestal.
2. Disconnect the video signal and video power cables from the rear of the gray scale monitor, and remove the monitor and its base.
3. Now reconnect the cables to the rear of the new monitor.
4. Ensure that a color video board is present in the system before installing a grey-scale monitor, and that the "Y" end of the video cable is connected as follows:

- The P2, BNC connector labeled SYNC goes to the SYNC jack on the back of the color board.
- The P1, VIDEO connector goes to the jack on the color board that is labeled GREEN.

If the Sun-3/160C color monitor needs external degaussing, refer to Appendix C for the degaussing procedure.

3.3. Printed Circuit Board (PCB) Removal

All PCBs (with the exception of the tape and SCSI-type disk drive controller boards) are located in a cardcage and can be removed from the rear of the pedestal. The following procedure describes how to physically remove a PCB from the cardcage.

Appendix A contains information on backplane jumper configuration, should you add boards or change the location of boards in the card cage. The *Configuration Procedures* manual provides information on jumper settings and card cage slot assignments. Such system reconfiguration also requires software procedures that can be found in the *System Administration for the Sun Workstation* manual.

CAUTION **These boards contain components that are sensitive to damage from electrostatic discharge, which can occur when you walk across a carpet and then touch the board. Before handling the board, make sure that you have placed your hand on a conductive surface that is grounded to a common earth ground, (such as the metal screw or plate on the AC wall receptacle) to discharge any static electricity present in your body.**

To remove a printed circuit board:

1. Turn power off and disconnect any cables from the edge of the board.
2. Unfasten the two recessed hex-head screws located at the top and bottom of the PCB to be removed (see Figure 3-1).

3. Move the arms on the extraction levers outward to release the PCB from the backplane connectors (see Figure 3-1).

4. To install PCBs, follow this procedure in reverse.

NOTE *The component side of the PCB should face the right side of the cardcage.*

If additional PCBs are to be installed, remove the blank plate (Sun PN 340-1407-01) that covers the unused cardcage slots, and the air flow restrictor that is installed in the empty slot.

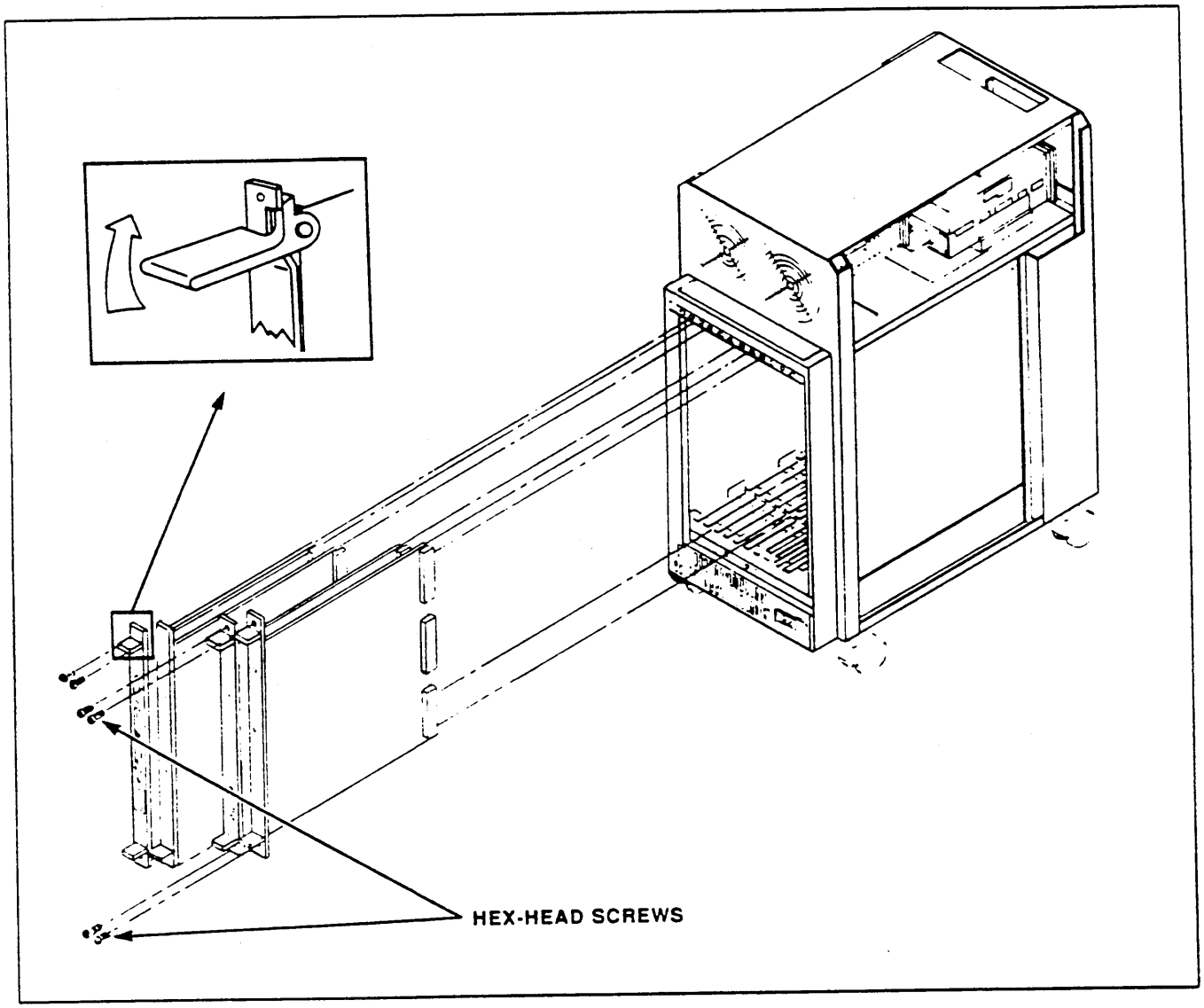
To do so, unfasten the recessed hex-head screws that secure the plate to the cardcage, remove the blank panel, then slide the restrictor out (refer to *Illustrated Parts Breakdown #3*).

CAUTION **An air flow restrictor must be present in each un-used slot to ensure proper system operation. If a board is removed from one system and installed in another system, make sure to also swap the restrictor and blank panel that you take out of the "destination" system, so that the system from which the board was removed now has a restrictor and blank panel in place of the board.**

ID PROM Replacement

When you replace the CPU board, be sure to take the ID PROM from the old board (located at coordinates B-10.5) and insert it in the new board at the same location. Be sure that the pin 1 indicator (usually a small dot or indentation at one end of the chip) is facing the correct way (toward the diagnostics switch on the board edge). Additional IC insertion tips follow under the heading *Socketed IC Removal and Insertion.*

Figure 3-1 *Sun-3/160 Cardcage*



For a view of the cardcage with air flow restrictors, see *Illustrated Parts Breakdown #3* at the end of this chapter.

Socketed IC Removal and Insertion

CAUTION **These components are sensitive to damage from electrostatic discharge, which can occur when you walk across a carpet and then touch them. Before handling the boards and ICs, make sure that you have placed your hand on a conductive surface that is grounded to a common earth ground, such as the metal screw or plate on the AC wall receptacle, to discharge any static electricity present in your body.**

When removing and inserting socketed ICs, such as the Boot PROM, an appropriate tool should be used to prevent damage to the IC pins and damage from electrostatic discharge.

Always extract the IC slowly and smoothly. If the chip is to be reused, store it in conductive foam to prevent damage from electrostatic discharge.

Avoid handling the IC pins during insertion, and be careful not to bend the pins.

Remember to match the Pin 1 identifier on the chip (usually an indentation or a dot on the edge of one end) with the identifier on the socket.

3.4. Trim Removal

Sun-3/160 trim consists of:

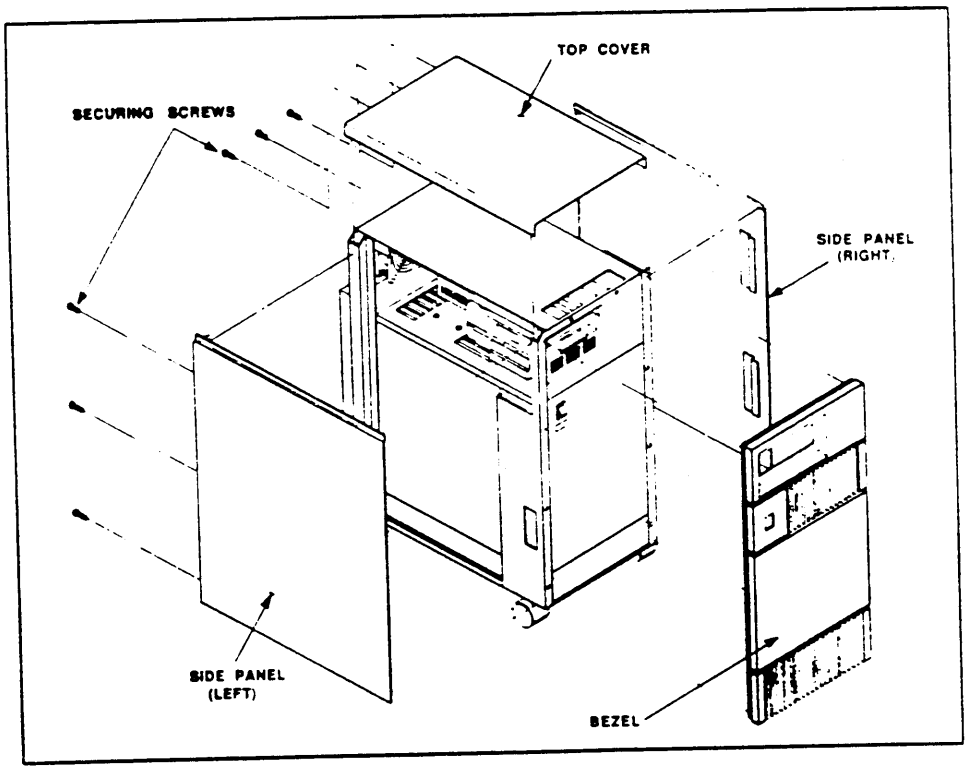
- the front bezel (Sun P/N 540-1141)
- the top cover (Sun P/N 340-1138)
- the right side panel (Sun P/N 340-1261)
- and the left side panel (Sun P/N 340-1262)

The front bezel simply snaps on and off. Remove the balance of the trim as described in the following paragraphs.

Top Cover Removal

1. Remove the three cross-head securing screws located at the rear of the top cover. Refer to Figure 3-2.
2. Slide the top cover back, toward the rear of the pedestal, and then lift up to remove it.
3. To replace the cover, reverse this procedure.

Figure 3-2 *Trim Removal*



Side Panel Removal

To remove either the right or left side panel:

1. Remove the top cover as previously described.
2. Unfasten the the three cross-head screws that secure the rear of the panel to the pedestal (refer to Figure 3-2).

3. Pull the panel toward the rear of the pedestal to release the locating hooks.
4. To reinstall the panels, reverse this procedure.

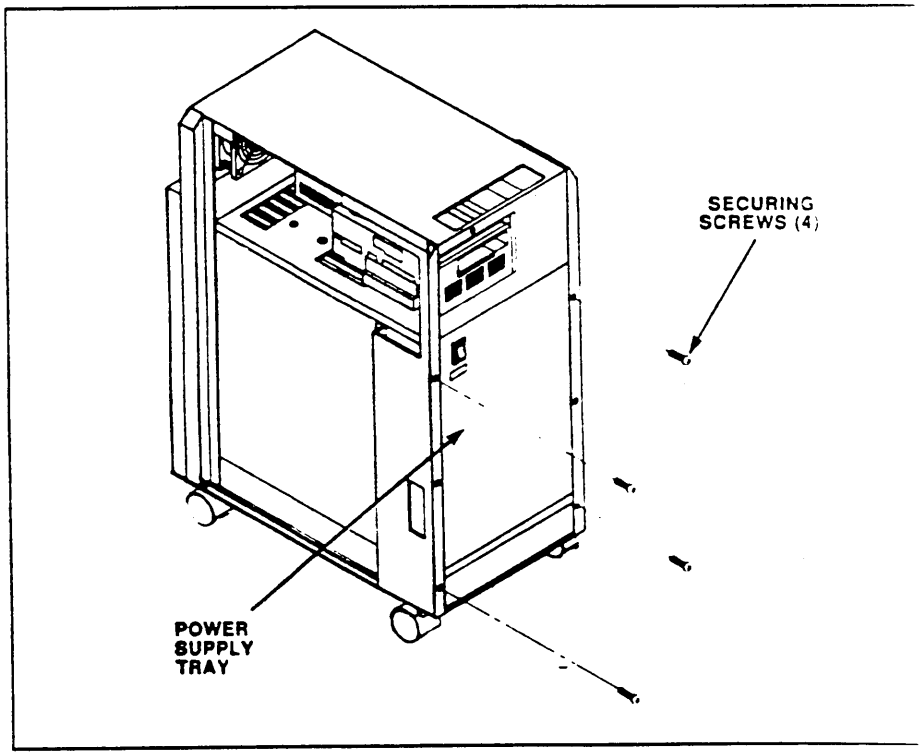
NOTE *This text refers to the right and left side panels as viewed from the front of the pedestal.*

3.5. Power Supply Removal

To remove the power supply (Sun P/N 540-1311):

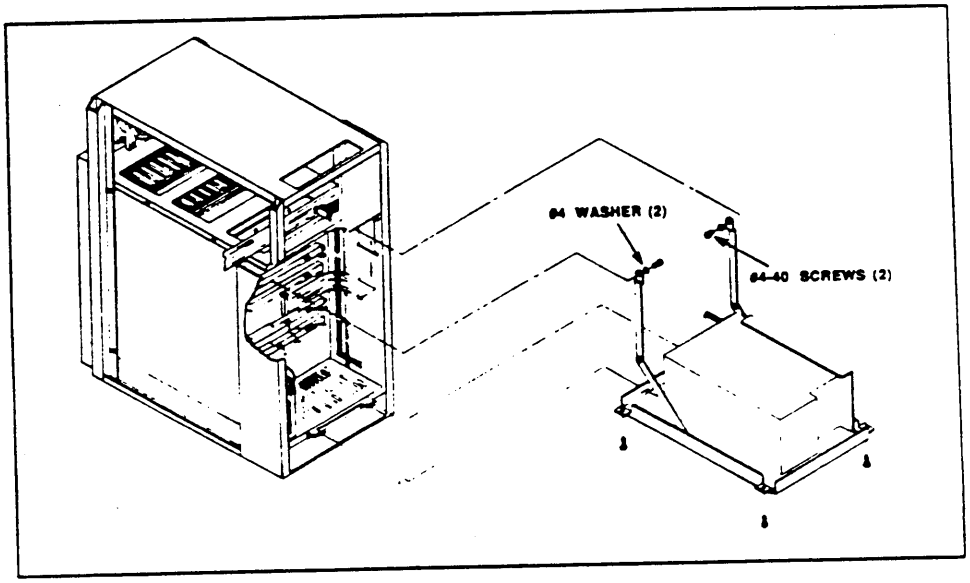
1. Ensure that the workstation is properly powered down as described in Subsection 3.1 of this manual.
2. Disconnect the AC power cord from the rear of the pedestal.
3. Remove the bezel as described in the trim removal section.
4. Unfasten the four cross-head screws that secure the hinged power supply panel to the pedestal (see Figure 3-3). Remove the lower screws first to prevent damage to the hinge assembly.

Figure 3-3 *Power Supply Panel Securing Screws*



5. Gently lower the power supply panel down until the retainers on either side (see Figure 3-4) support it.

Figure 3-4 *Power Supply Panel Retainers*



NOTE *Sun-3/160 pedestals are shipped with supplies built by Pioneer or ETA. Both supplies are supported in this text due to minor differences between the two supplies.*

6. Disconnect the AC line and load cables from the AC line filter (refer to Figure 3-5).
7. Remove the kepnut that attaches the AC ground wire to the lug on the left side of the power supply tray (near the hinged edge), and disconnect the AC ground wire.
8. If a cable restraint bracket is present, remove the two #8-32 screws that mount the cable restraint bracket to the supply, and remove the bracket (see Figure 3-6).
9. Label and disconnect all cabling from the power supply connector panel.
10. Support the supply and unfasten the two #4-40 screws and washers that secure the power supply retainers to the sides of the pedestal.
11. Place the power supply on a suitable work area with the panel facing upward. Unfasten the four cross-head screws that secure the power supply to the panel and lift the panel off (see Figure 3-6).
12. To install the power supply, reverse this procedure, ensuring that the AC and DC harnesses are not pinched when the hinged panel is secured to the pedestal, and that the DC harness can be moved around inside the cable restraint bracket (if installed).

CAUTION Make sure you use only 1/4 inch screws to mount the power supply to the tray. Longer screws could short out components within the power supply.

13. Reconnect the DC distribution harness to the power supply as shown in Figure 3-5, 3-6, 3-7 or 3-8.

CAUTION **When reinstalling the hinged panel into a pedestal that contains a disk drive, grasp the rear of the pedestal with one hand and gently push on the tray with the other hand until the tray can be fastened to the pedestal. (Pounding on the tray, which fits tightly in the pedestal, could cause damage to the disk drive.)**

Figure 3-5 *DC Distribution Harnesses*

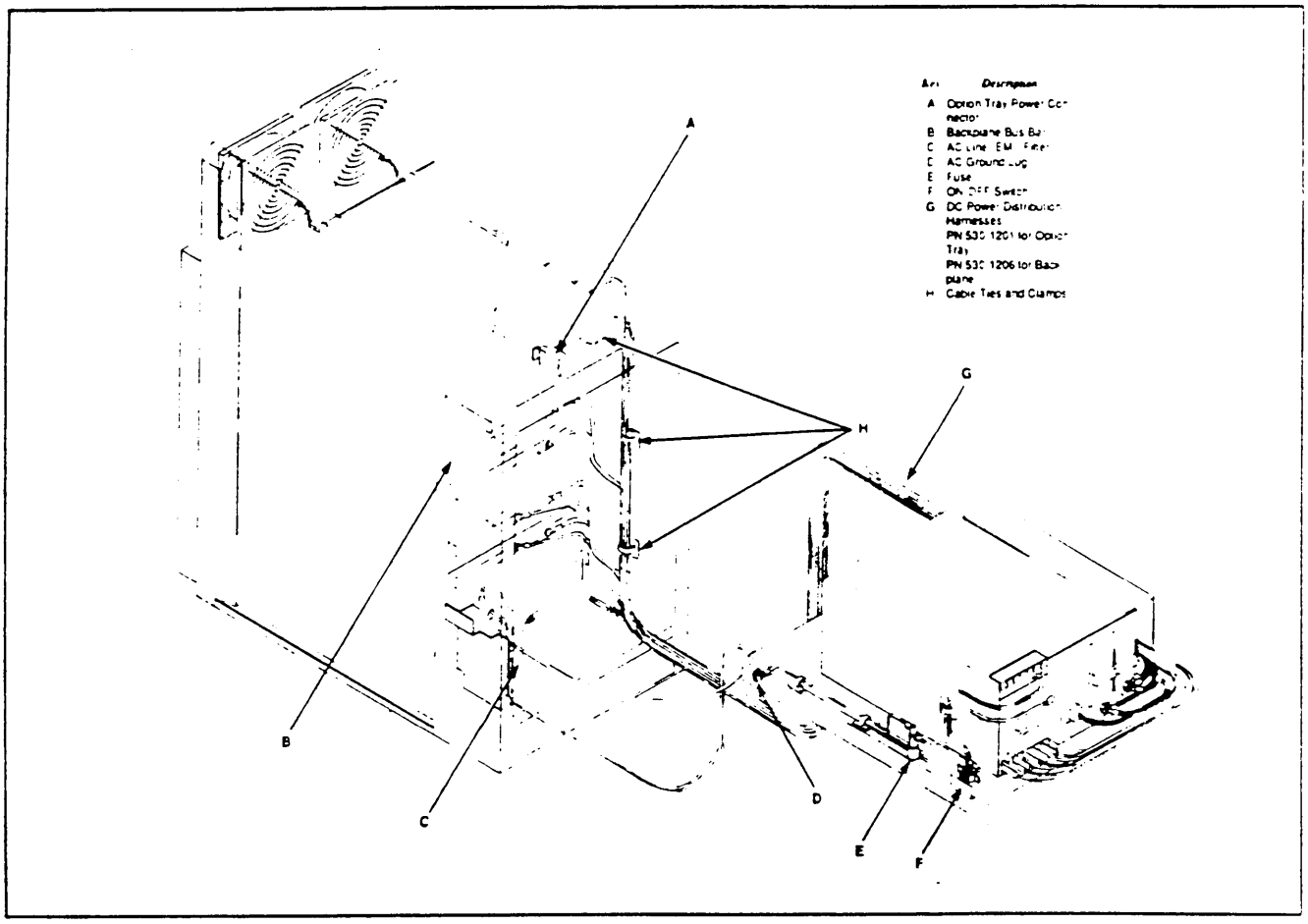
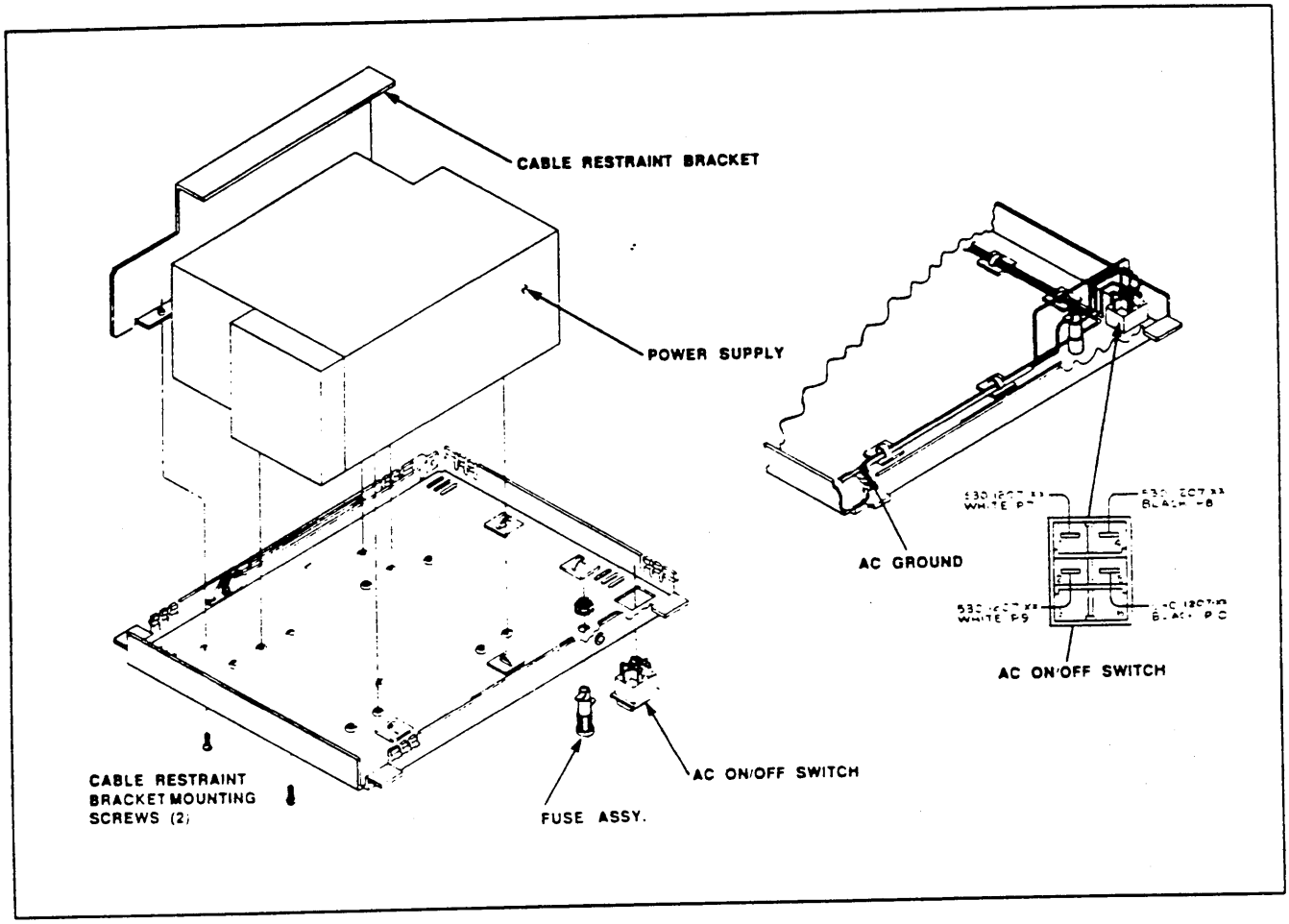


Figure 3-6 *Power Supply-to-Panel Mounting*



NOTE *Note that the drawing depicts a Pioneer power supply installation. The mounting screws for the ETA supply are closer to the edge of the panel, due to the slight difference in dimensions (refer to the Illustrated Parts Breakdown at the end of this chapter for ETA mounting).*

Also, the cable restraint bracket shown above may not be present on all Sun-3/160 power supply assemblies.

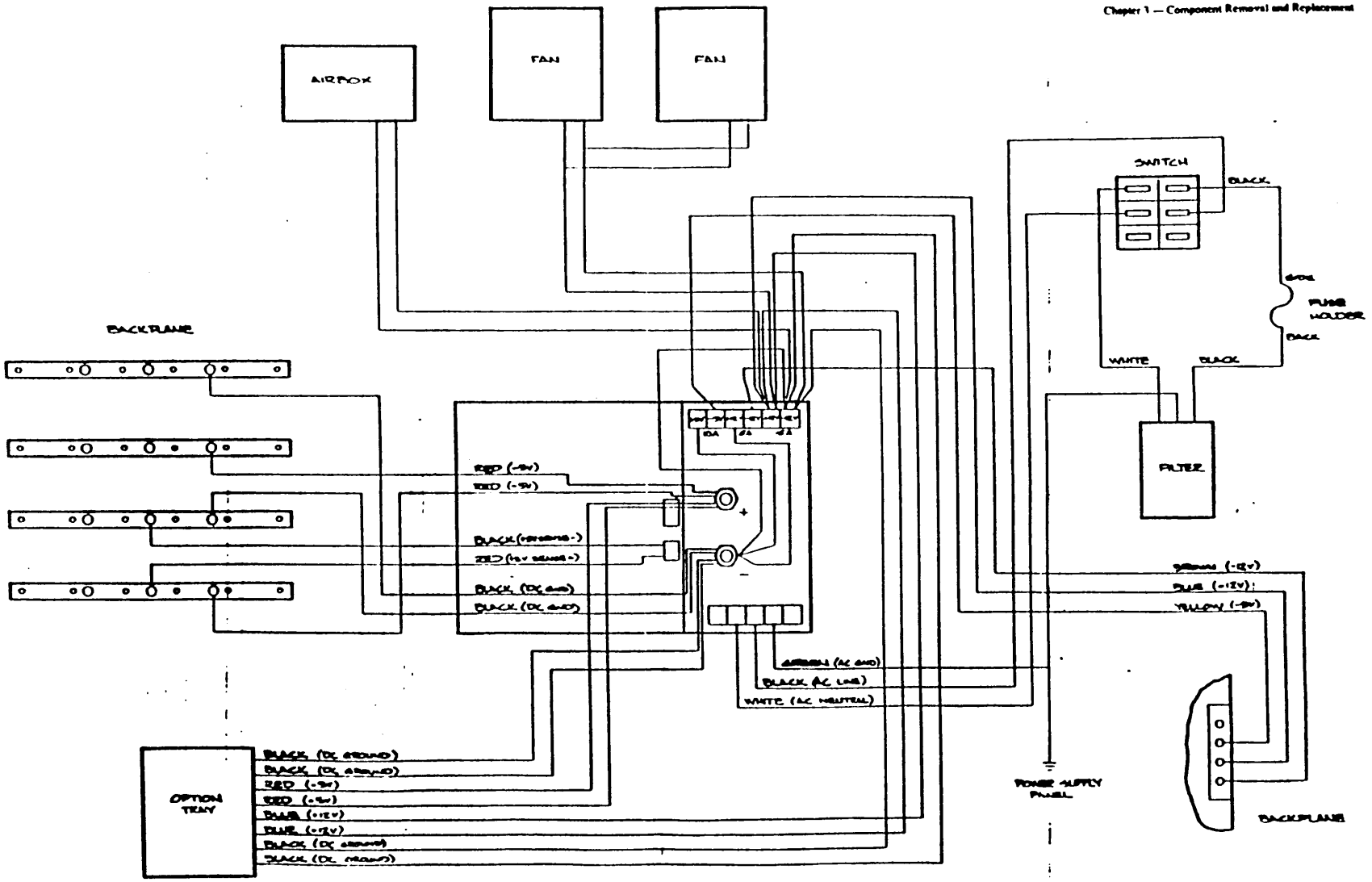


Figure 3-7 *Pioneer Power Supply Connections*

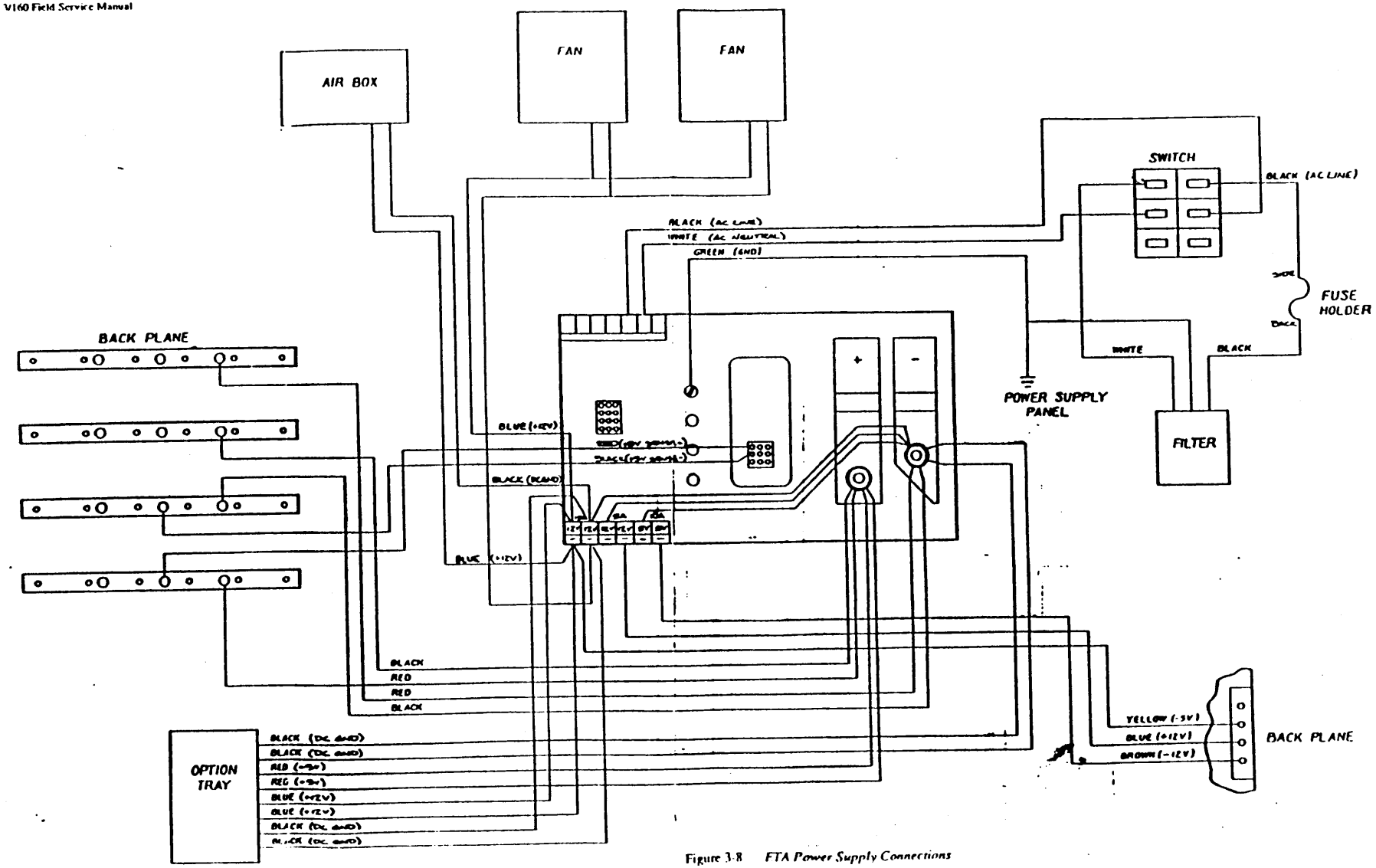


Figure 3-8 *FTA Power Supply Connections*

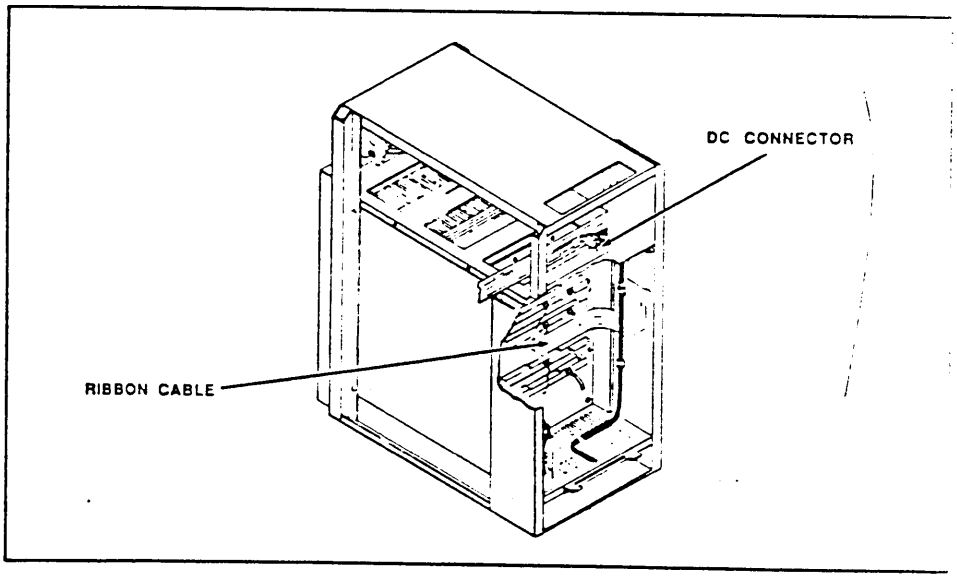
3.6. Option Tray Removal

The option tray houses the Sun-3/160 disk and tape subsystems. The option tray is located in the upper half of the pedestal. Follow power down procedures as described at the beginning of the chapter, then:

1. Remove the bezel, top cover and side panels as described in the section on trim removal.
2. Lower the power supply tray as described in the section on power supply removal.
3. Unfasten the connector on the DC distribution harness that supplies power to the option tray (see Figure 3-9).

CAUTION **If a "Version B" option tray is present (refer to Figure 3-13), moving the DC harness may cause the address switch on the tape controller board to change position. Check to make sure that the setting is correct after the option tray is removed. (Refer to the *Sun Hardware Options Guide*, Sun PN 813-1000 for jumper and dip switch setting information.)**

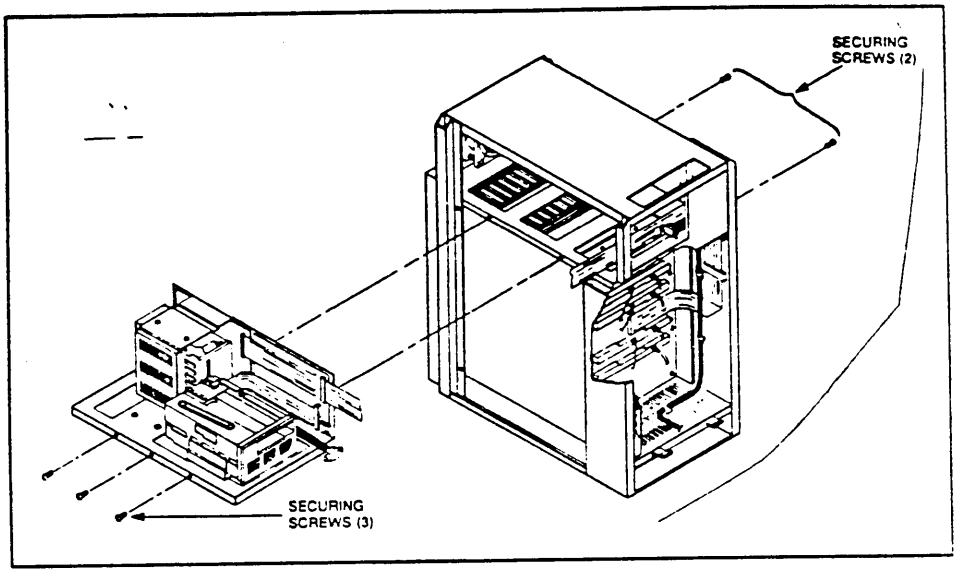
Figure 3-9 *DC Power to the Option Tray*



4. Disconnect the SCSI ribbon cable connector from the backplane (refer to Figure 3-9), and release the cable from the cable clamps.
5. Unfasten the two cross-head screws that secure the option tray to the right side of the pedestal (refer to Figure 3-10).
6. Unfasten the three cross-head screws securing the option tray to the left side of the pedestal.
7. Carefully withdraw the option tray from the left side of the pedestal.
8. Feed the ribbon cable, disconnected in step 4, up into the option tray cavity and remove it with the option tray.

Figure 3-10 *Option Tray Mounting*

If the tray does not come out smoothly, check to make sure that the ribbon cable or the option tray DC distribution harness is not caught on obstructions inside the pedestal.



To replace the option tray, reverse these procedures.

3.7. Removing Drives From the Option Tray

The option tray is available in these configurations:

- Single tape drive and single disk drive,
- Single tape drive and dual disk drives,
- Single or dual disk drives without the tape drive, or
- Tape Drive only.

Either one or both of the corresponding controller boards will be present on the tray. Variations in mounting brackets and controller board location are illustrated in these procedures.

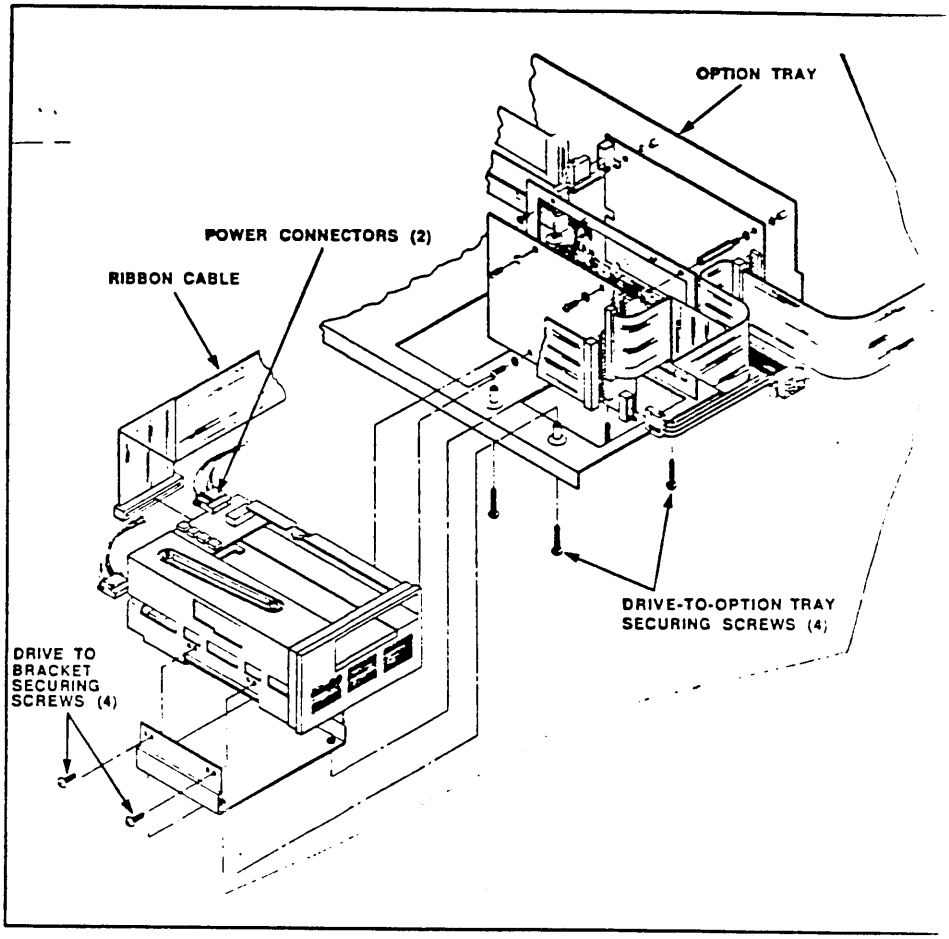
Use the same procedure to remove the tape drive from any configuration.

Tape Drive Removal

To remove the tape drive (Sun P/N 370-1037-02) from the option tray:

1. Remove the option tray from the pedestal as described in the section on option tray removal.
2. Place the option tray on its back and, while supporting the drive, unfasten the four #6-32 cross-head screws that secure the tape drive and mounting bracket to the option tray (refer to Figure 3-11).

Figure 3-11 *Tape Drive to Option Tray Mounting*



3. Partially withdraw the drive from the tray, then remove the two four-pin male power connectors and the ribbon cable from the rear of the drive.
4. Remove the drive from the tray.
5. If the drive is to be replaced, unfasten the four cross-head screws (refer to Figure 3-11) that secure the mounting bracket, and remove the bracket.
6. To install a tape drive, reverse this procedure.

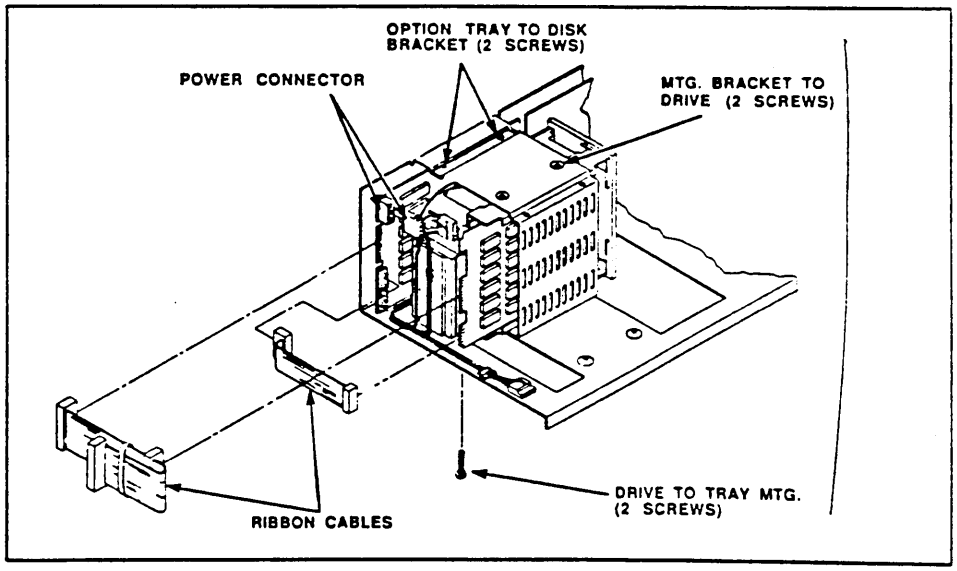
Disk Drive Mounting

You may encounter two types of single disk drive installations in Sun-3/160 workstations. The first, which we will call Assembly "A", shown in Figure 3-12, has the drive controller board mounted behind the drive. A small bracket mounts the disk mounting bracket to the side of the option tray.

A second configuration, shown in Figure 3-13 as Assembly "B", mounts the single drive in the same bracket that is used for mounting dual drives. In this assembly, the controller boards are located behind the tape drive. Removal instructions for Assembly B follow Figure 3-13.

CAUTION **These components are sensitive to damage from electrostatic discharge, which can occur when you walk across a carpet and then touch them. Before handling the drives and boards, make sure that you have placed your hand on a conductive surface that is grounded to a common earth ground, such as the metal screw or plate on the AC wall receptacle, to discharge any static electricity present in your body.**

Figure 3-12 *Single Disk Drive Removal (Version A)*



Single Disk Drive Removal (Version A)

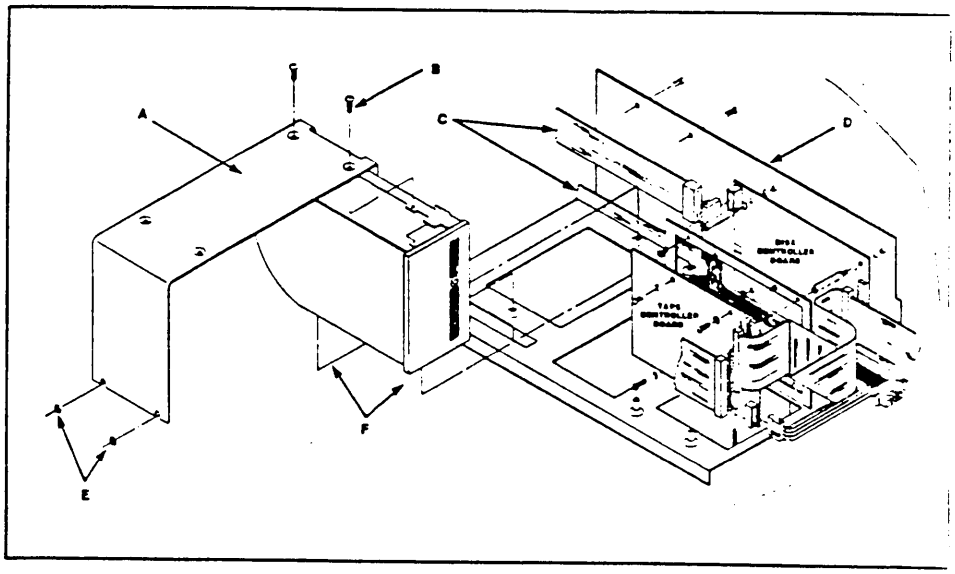
To remove the single disk drive (Sun P/N 370-1034-02) from the option tray shown in Figure 3-12:

1. Remove the option tray from the pedestal as described in the section on option tray removal.
2. Label and remove the four-pin male power connector and the two ribbon cables from the rear of the drive (see Figure 3-12).
3. Remove the two cross-head screws that secure the disk mounting bracket to the side of the option tray.
4. Place the option tray on its back and, while supporting the drive, unfasten the cross-head screws that secure the disk drive to the tray (see Figure 3-12).

5. Remove the drive and bracket from the tray.
6. If the drive is to be replaced, unfasten the cross-head screws that secure the mounting bracket (Sun PN 340-1244-01) to the drive, and remove the bracket.
7. Reverse this procedure to install a single disk drive. Refer to the *Sun Hardware Options Guide* for drive address switch settings and terminator locations, and to *Installing Unix on the Sun Workstation* for disk formatting information.
8. Replace the old defect list with the new one.

Figure 3-13 *Single Drive Removal (Version B)*

Key	*Description*
A	Mounting Bracket
B	Bracket-to-Drive Mounting Screws (2)
C	Ribbon Cable to Rear of Drive
D	Option Tray
E	Tray to Bracket Mounting Nuts
F	Drive to Tray Mounting Screws



Single Disk Drive Removal (Version B)

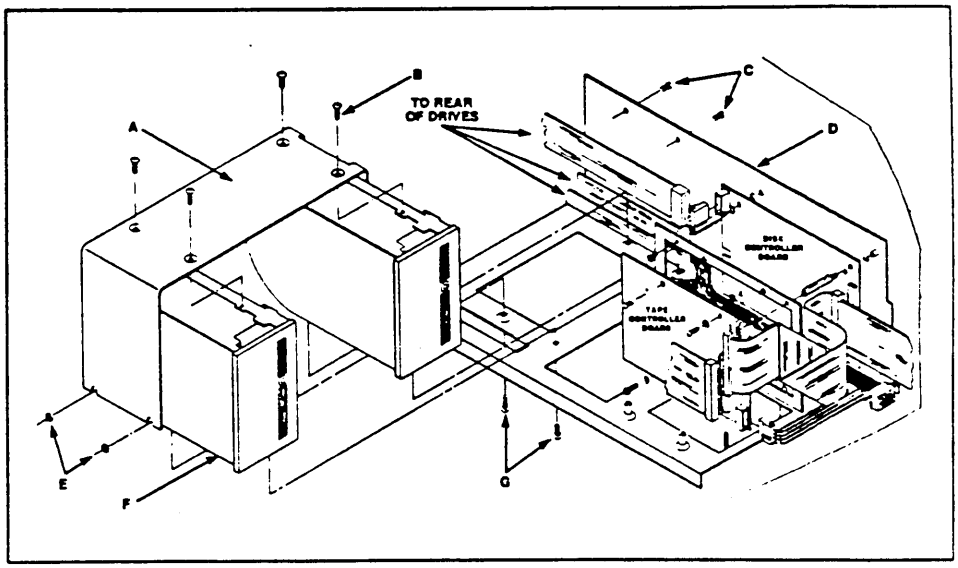
To remove the single disk drive from the option tray shown in Figure 3-13:

1. Remove the option tray from the pedestal as described in the option tray removal subsection.
2. Label and remove the four-pin male power connector and the two ribbon cables from the rear of the drive.
3. Remove the two screws that mount the disk bracket (Sun PN 340-1244-02) to the sides of the option tray.
4. Unfasten the two nuts that secure the disk bracket to the option tray studs.
5. Turn the option tray over, and support the drive while removing the two screws that secure the drive to the bottom of the tray.
6. Remove the drive and bracket from the tray.
7. If the drive is to be replaced, remove the two cross-head screws that attach the disk mounting bracket to the drive, and remove the bracket.

8. To install a single disk drive, reverse this procedure. Ensure that the terminator resistor and address switch settings on the drive circuit board are correct for this configuration (refer to the *Sun Hardware Options Guide*). For disk formatting information, refer to *Installing Unix on the Sun Workstation.*
9. Replace the old defect list with the new one.

Figure 3-14 *Dual Disk Drive Mounting (Version B)*

Key	*Description*
A	Mounting Bracket
B	Bracket-to-Drive Mounting Screws
C	Bracket-to-Option Tray Mounting Screws
D	Option Tray
E	Bracket-to-Option Tray Mounting Nuts
F	Disk Drive
G	Drive to Tray Mounting Screws (4)



Dual Disk Drive Removal

You may encounter one of two types of dual disk option trays in the field; Dual Drive Tray "A", in which both controller boards are mounted to the back of the tray, as in Figure 3-17; or Dual Drive Tray "B", in which the controller boards are mounted in a bracket behind the tape drive, as shown in Figure 3-14;

This text supports both tray versions, including variations in dual drive mounting bracket characteristics.

To remove a pair of vertically-mounted disk drives from the option tray:

1. Remove the option tray from the pedestal as described in the section on option tray removal.
2. Label and remove the four-pin male power connector and the two ribbon cables from each drive (see Figure 3-15 or 3-16).

For Option Tray A

1. Remove the two screws that mount the disk bracket (Sun PN-1244-01) to the bracket that fits over the side of the option tray.
2. Place the option tray on its back and, while supporting the drives, unfasten the four cross-head screws that secure the mounting brackets to the bottom of the option tray.

For Option Tray B

1. Remove the two screws that mount the disk bracket (Sun PN-1244-02) to the back of the option tray.
2. Remove the two nuts that secure the disk bracket to the studs on the option tray edge.

For Either Option Tray

3. Remove the drive/mounting-bracket assembly from the tray.
4. If one or both of the drives are to be replaced, unfasten the four cross-head screws that secure the mounting bracket(s) (Sun P/N 340-1244-01 or 340-1244-02) to the drives, and remove the bracket(s) (refer to Figure 3-14 or 3-15). Note that the Version A assembly has separate brackets for each drive, which are joined together in the center with two screws.

Figure 3-15 *Dual Disk Drive Cabling (Option Tray A)*

Key	*Description*
A	Ribbon Cables
B	Drive Controller Board
C	Power Connectors
D	Bracket-to-Option Tray Securing Screws
E	Bracket-to-Disk Securing Screws (4)
F	Mounting Bracket

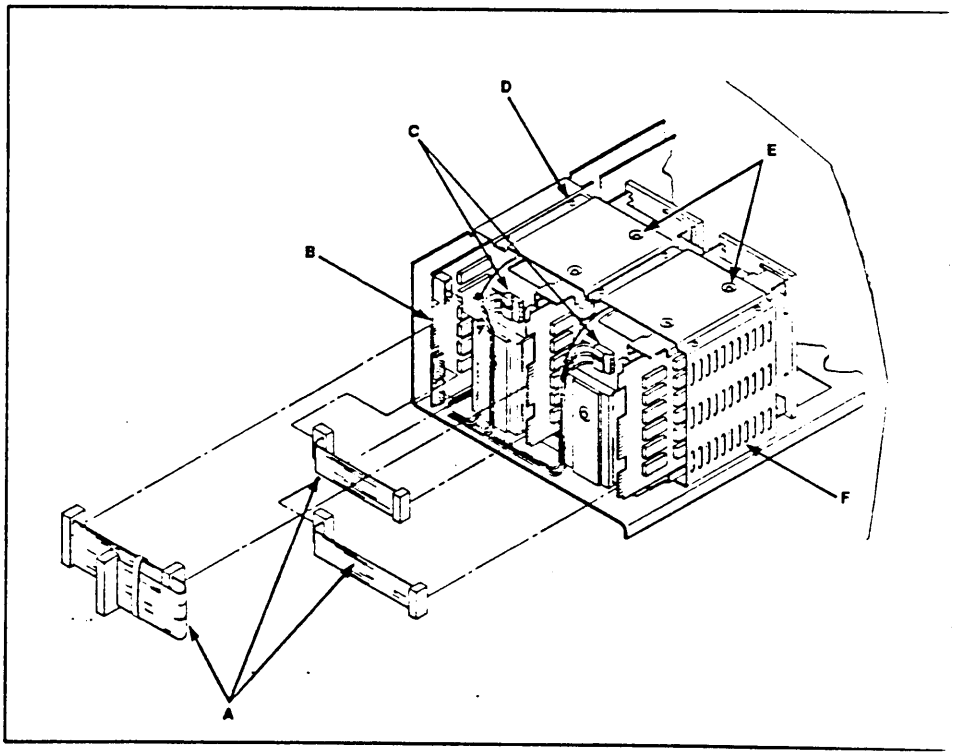
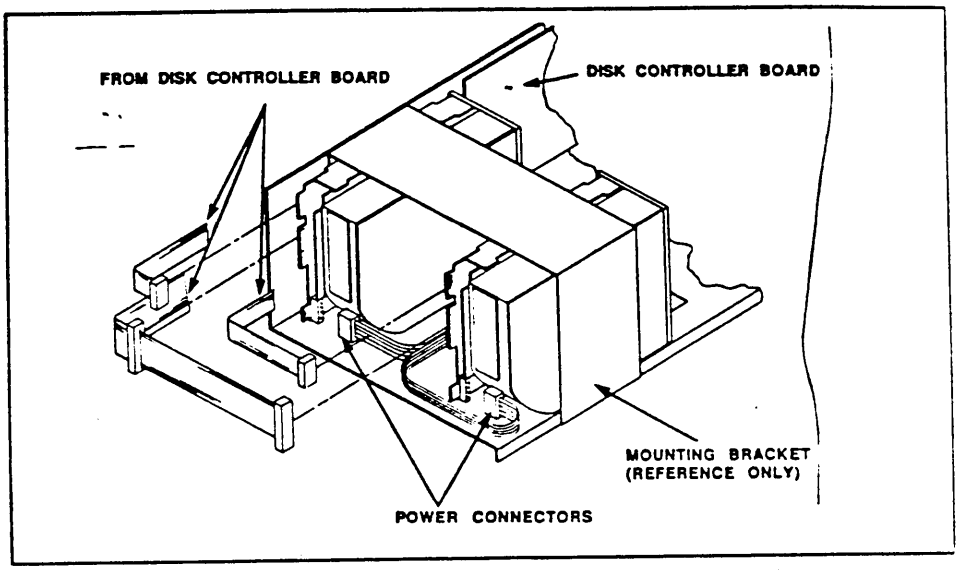


Figure 3-16 *Dual Disk Drive Cabling (Option Tray B)*



5. To install dual disk drives, reverse this procedure. When replacing drives, ensure that drive address switch/jumper settings and terminator resistors on the new drive electronics boards are set as shown in the *Sun Hardware Options Guide*. For disk formatting information, refer to *Installing Unix on the Sun Workstation*.
6. Replace the old defect map with the one belonging to the new drive.

3.8. Drive Controller Board Removal

CAUTION **These boards contain components that are sensitive to damage from electrostatic discharge, which can occur when you walk across a carpet and then touch the board. Before handling the board, make sure that you have placed your hand on a conductive surface that is grounded to a common earth ground, such as the metal screw or plate on the AC wall receptacle, to discharge any static electricity present in your body.**

To remove either the disk drive controller board (Sun P/N 370-1010-05 and 370-1010-06) or tape drive controller board (Sun P/N 370-1011-01):

Remove the option tray from the pedestal as described in the subsection on option tray removal.

To remove either controller board from option trays with controller boards located side by side, behind the disk drive (Option Tray A):

1. Release the four plastic standoffs (Sun P/N 230-1007-01) that secure each controller board to the back of the option tray (refer to Figure 3-17).

2. Disconnect the four-pin male power connectors and the ribbon cable connectors from each board and remove the boards from the tray.

3. Installation is the reverse of this procedure. When reinstalling the controller boards, ensure that they are cabled as shown in Figure 3-17 and 3-18, and that the terminator resistors are installed only on the last board connected to the SCSI cable (which is the Disk Controller board when both disk and tape controllers are installed). Set the jumpers or dip switches as indicated for this system configuration in the *Sun Hardware Options Guide*.

For option trays with both controller boards located behind the tape drive (Option Tray B):

Remove the tape drive as described in the tape drive removal subsection.

To remove the tape drive controller board (refer to Figure 3-19):

1. Remove the four screws that mount the board to its bracket.

2. Label and disconnect the four-pin male power connector and the ribbon cable connectors from the board, and remove the board. Note the orientation of the colored wire on the ribbon cable, which connects to pin one on the connector.

To remove the disk drive controller board:

1. Remove the tape drive and tape controller board as previously described.

2. Remove the four screws and washers that secure the standoffs between the board and the tape controller board mounting bracket. Save the screws and washers for use in reinstalling the board.

3. Remove the four standoffs (Sun P/N 240-1327).

4. Label and disconnect the four-pin male power connector and the ribbon cables attached to the board. Note the orientation of the colored wire on the ribbon cable, which connects to pin one.

5. Remove the board from the tray.

To install the controller boards, reverse these procedures, and ensure that they are cabled as shown in Figure 3-19 and 3-20. Make sure that the terminator resistors are in place only on the last controller board connected to the SCSI cable (which is the Tape Controller board when both tape and disk controllers are installed). Also, when replacing a board, make sure that the jumpers and dip switches are set as indicated for this system configuration in the *Sun Hardware Options Guide*.

Figure 3-17 *Controller Board Mounting For Option Tray Version A*

Key	*Description*
A	Stand-offs (8)
B	Board-to-Stand-off Mounting (8)
C	Disk Drive Controller Board
D	Tray-to-Drive Bracket Mounting
E	Tape Drive Controller Board
F	Cable to Tape Drive
G	DC Power In
H	To Backplane
I	Option Tray

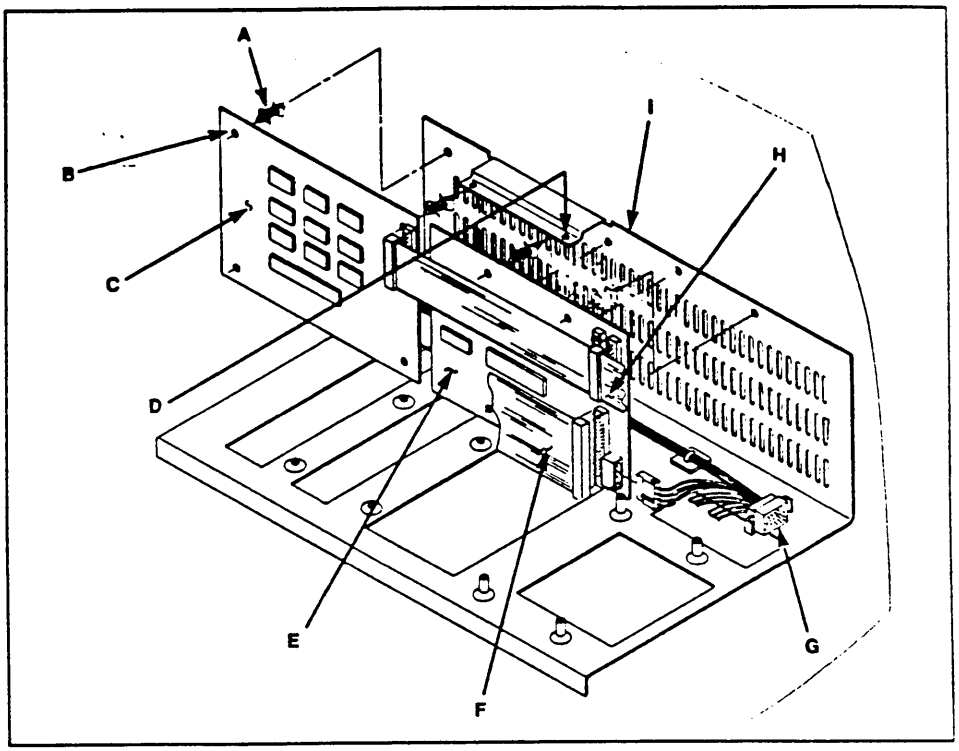


Figure 3-18 *Controller Board Cabling For Option Tray A*

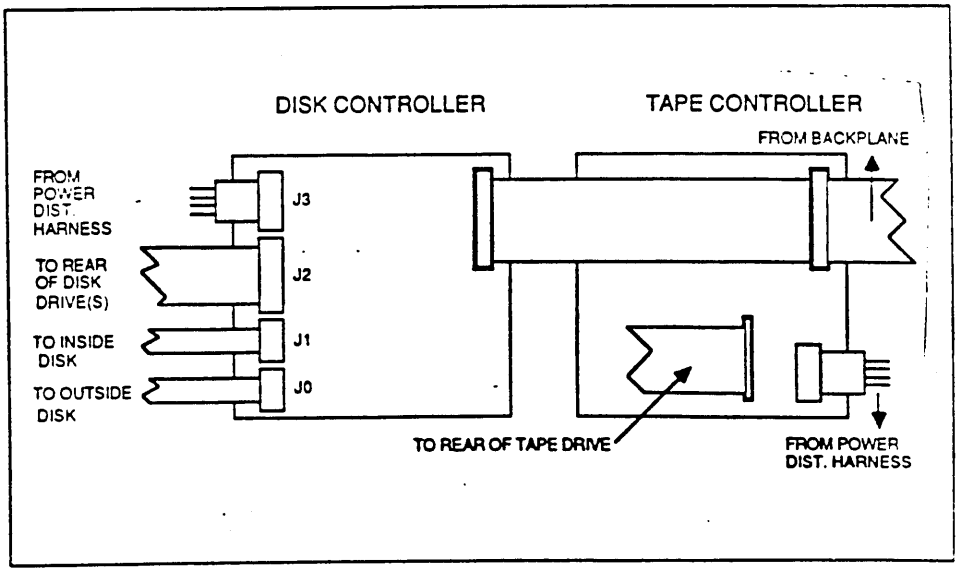


Figure 3-19 *Controller Board Mounting For Option Tray B*

Key	*Description*
A	Tape Controller Mounting Screw (4)
B	Tape Controller Board
C	To Power Distribution Harness
D	To Backplane
E	Washer (12)
F	Stand-off (4)
G	Tape Controller Mounting Bracket
H	Disk Controller Board
I	J3 (Power)

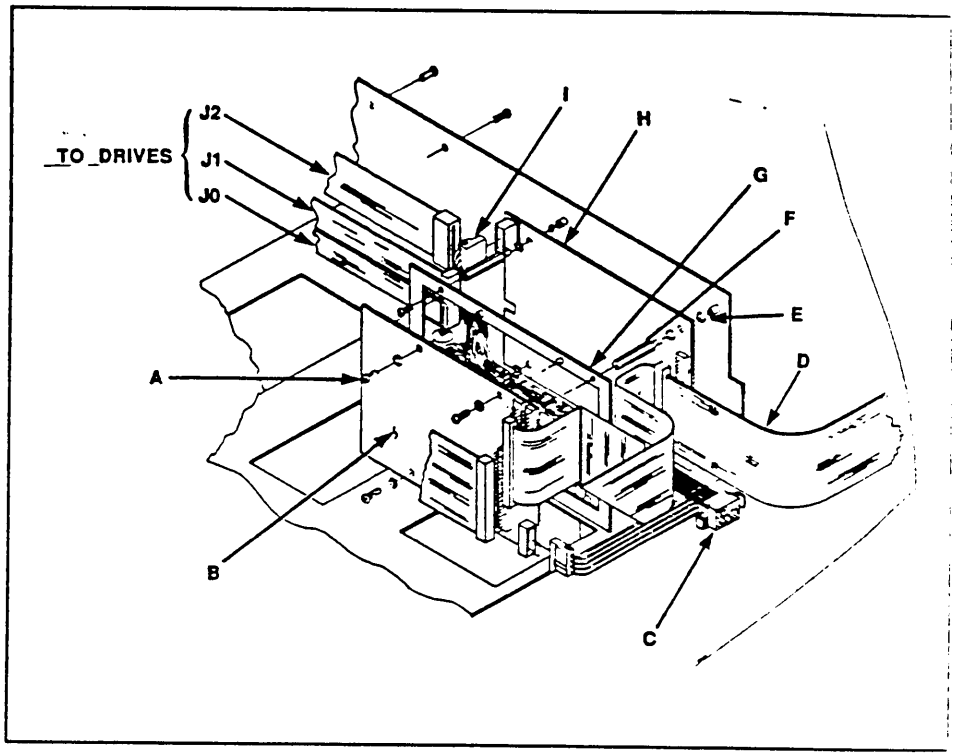
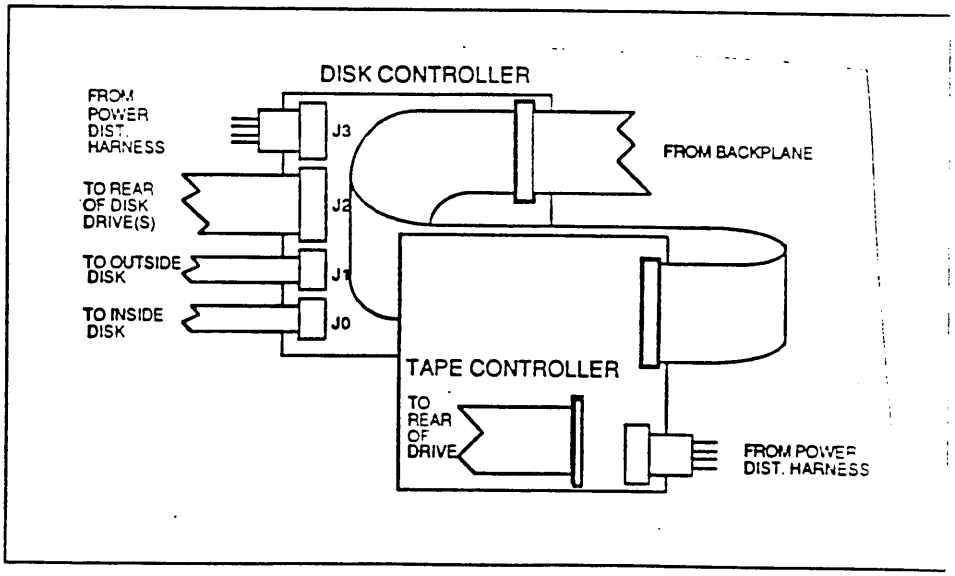


Figure 3-20 *Controller Board Cabling For Option Tray B*



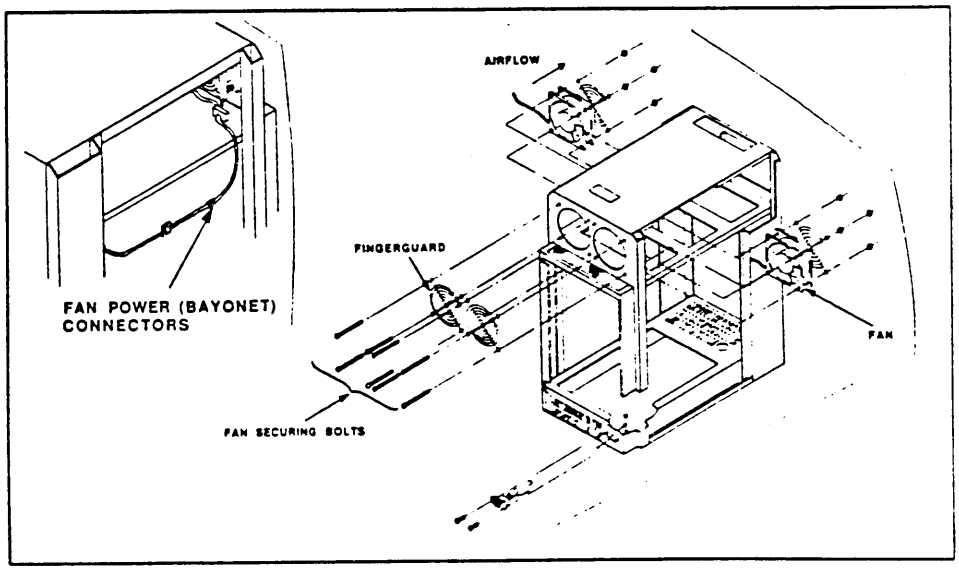
3.9. Upper Fan Assembly Removal

The upper fan assembly is composed of two fans (Sun P/N 540-1252-01) located at the rear of the option tray cavity in the machine pedestal. Remove these fans as follows:

1. Remove the option tray from the pedestal as described in the section on option tray removal.
2. Disconnect the two bayonet connectors located on the right side of the pedestal, below the option tray cavity (see Figure 3-21).

CAUTION **Do not pull on the wires. Use two tools (such as needle-nosed pliers) to separate the the bayonet connectors.**

Figure 3-21 *Upper Fan Assembly Mounting*



3. Unfasten the four cross-head screws, nuts and washers that secure each fan to the rear of the pedestal, and remove the fan(s) (refer to Figure 3-21).
4. To install the fan assemblies, reverse this procedure.

NOTE *When installing the fan(s), observe the pitch of the blades to ensure that air is being drawn INTO the top of the pedestal.*

3.10. Lower Fan Assembly Removal

The lower fan assembly consists of four fans (Sun PN 540-1252-01) mounted to a tray. The assembly (Sun PN 540-1082-02) is located in the bottom of the pedestal, below the cardcage (see Figure 3-22).

To gain access to the fans:

1. Refer to the Subsection 3.5, *Power Supply Removal*, and remove the four screws that secure the power supply tray to the chassis.
2. Lower the power supply tray assembly until the hinged arms support it.

3. Disconnect the cable that supplies +12VDC to the fan assembly (refer to Figure 3-22).
4. Remount the power supply tray to the pedestal chassis.
5. Unfasten the two cross-head screws that secure the fan tray to the pedestal. These screws are located directly beneath the hinge for the power supply tray (see Figure 3-22).
6. Withdraw the fan tray from the front of the pedestal.
7. Unfasten the screws that secure the faulty fan(s) and its fingerguard to the fan tray (see Figure 3-23).
8. To remove the faulty fan from the tray, disconnect the two bayonet connectors that supply power to that fan from the harness.

CAUTION **Do not pull on the wires when disconnecting the fan. Use a tool such as needle-nosed pliers to disconnect the bayonet connectors.**

9. To reinstall, follow this procedure in reverse, ensuring that rear edge of the tray is resting on the lip located at the rear of the pedestal, and that the airflow arrow on the fans points downward.

Figure 3-22 *Fan Tray Mounting*

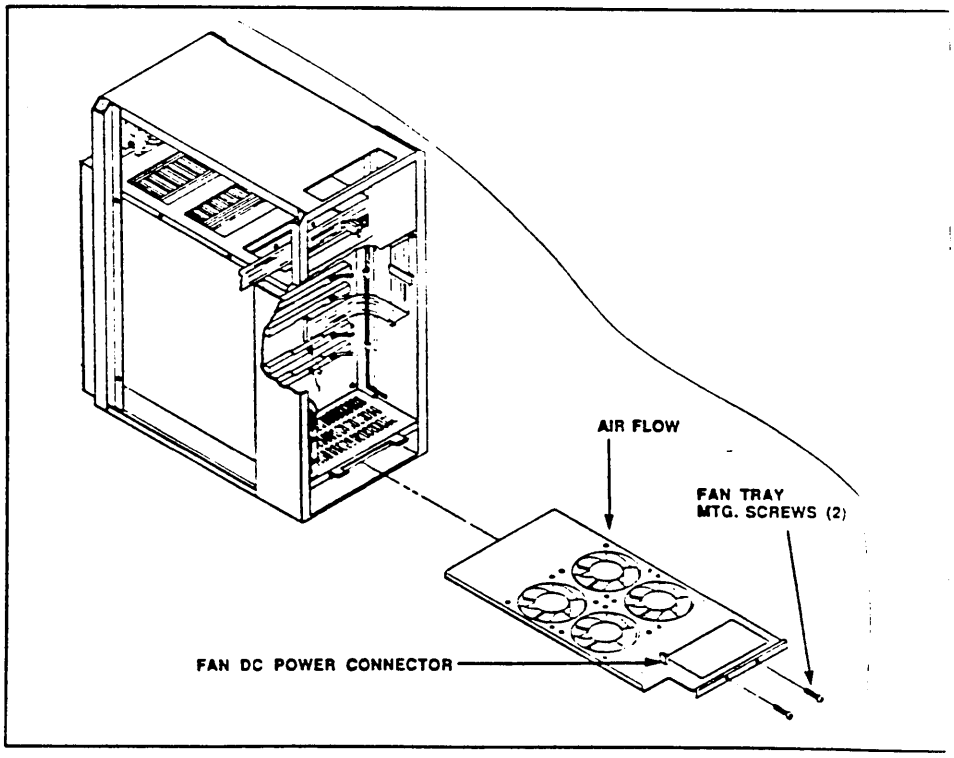
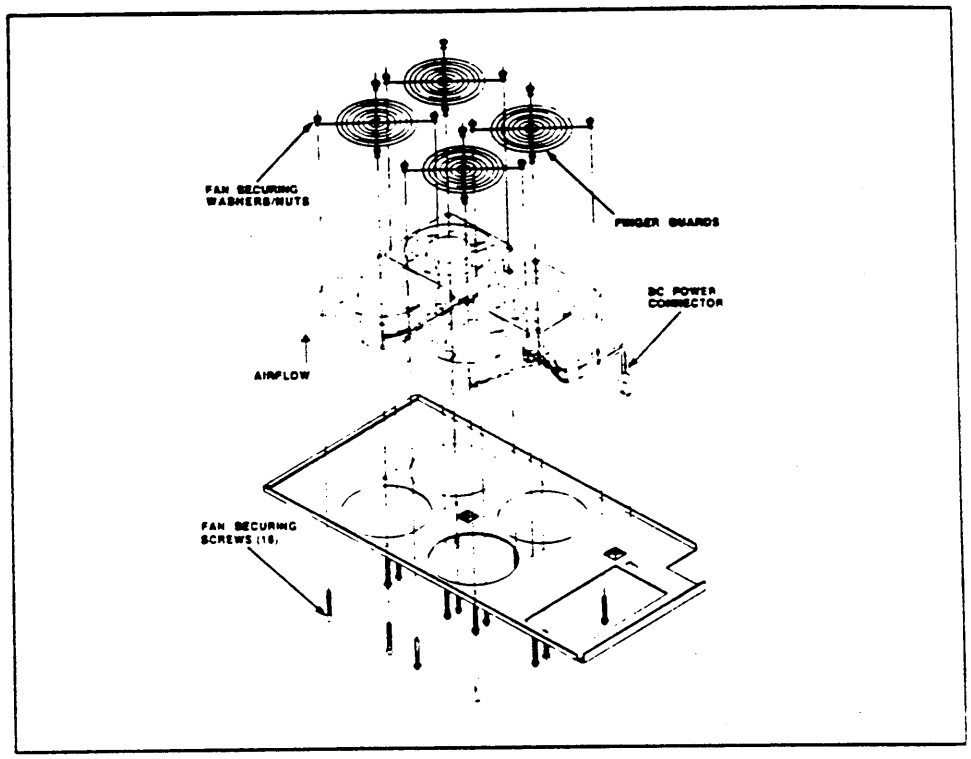


Figure 3-23 *Fan Removal*

NOTE *Orientation of the fan assembly is reversed when installed.*

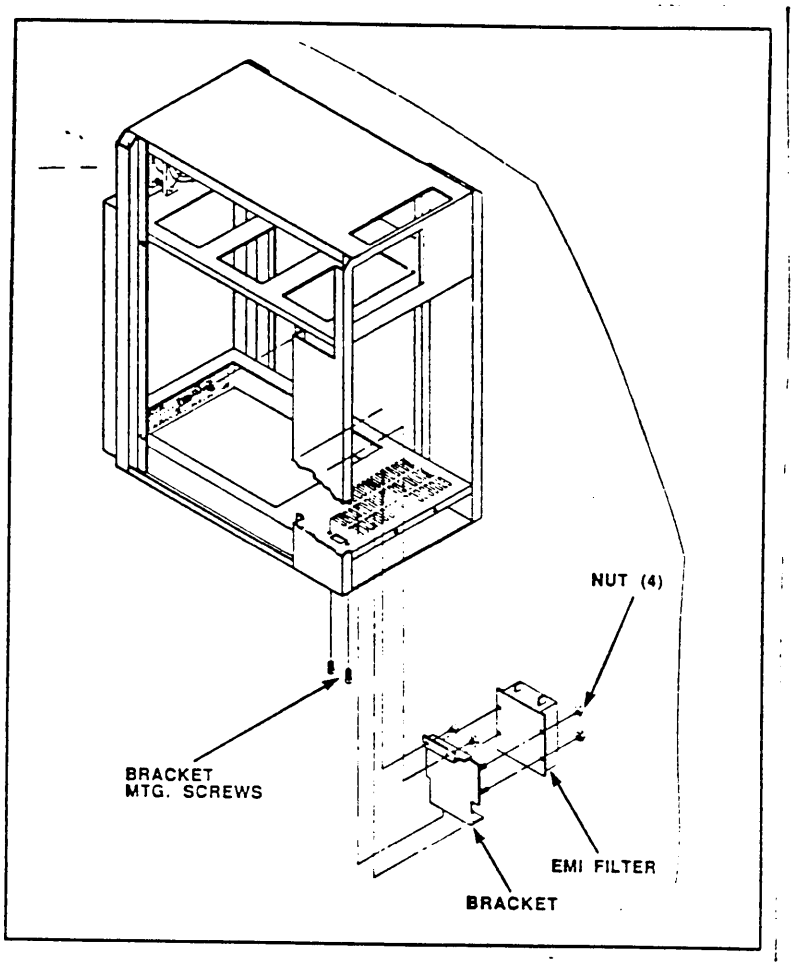


3.11. Cardcage/Backplane Removal

Follow these procedures to remove the card cage and backplane (Sun P/N's 370-1086-02 and 501-1092 respectively):

1. Remove the bezel, top cover and left and right side panels as described in the section on trim removal.
2. Follow the power supply removal procedures to remove the power supply and tray assembly from the front of the pedestal.
3. Remove all PCBs from the cardcage.
4. Unfasten the four nuts that attach the EMI filter (Sun PN 150-1129-01) to the bracket on the side of the pedestal.
5. Disconnect the AC power connector from the bottom of the filter and remove the filter (refer to Figure 3-24).

Figure 3-24 *Cardcage and EMI Filter Mounting*



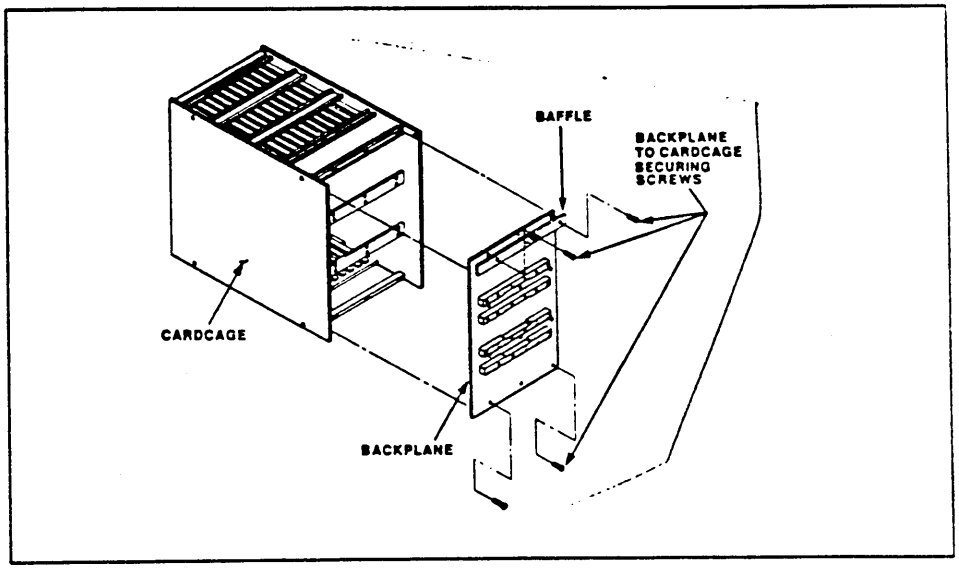
6. Label and disconnect the molex connector that provides +12VDC to the lower fan assembly.
7. Label and disconnect the two bayonet connectors that supply power to the upper fan assembly.
8. Cut the tie-wrap and remove the adhesive tie-wrap anchor from the right side of the cardcage.
9. Disconnect the 24-pin molex power supply to option tray connector.
10. Carefully disconnect the SCSI bus ribbon cable from the backplane.
11. Cut any remaining tie-wraps that secure the DC distribution harness to the pedestal and disconnect the harness from the backplane.
12. Unfasten the eight cross-head screws that secure the cardcage to the pedestal. Withdraw the cardcage. (See Figure 3-31, Illustrated Parts Breakdown #6, for more detail.)

13. To remove the backplane, unfasten the cross-head screws that secure it to the cardcage (refer to Figure 3-25).

14. To install the card cage, reverse this procedure.

CAUTION **If the AC wiring is "crossed" at the line filter output, the AC line will no longer be fused, which would create an electric shock hazard.**

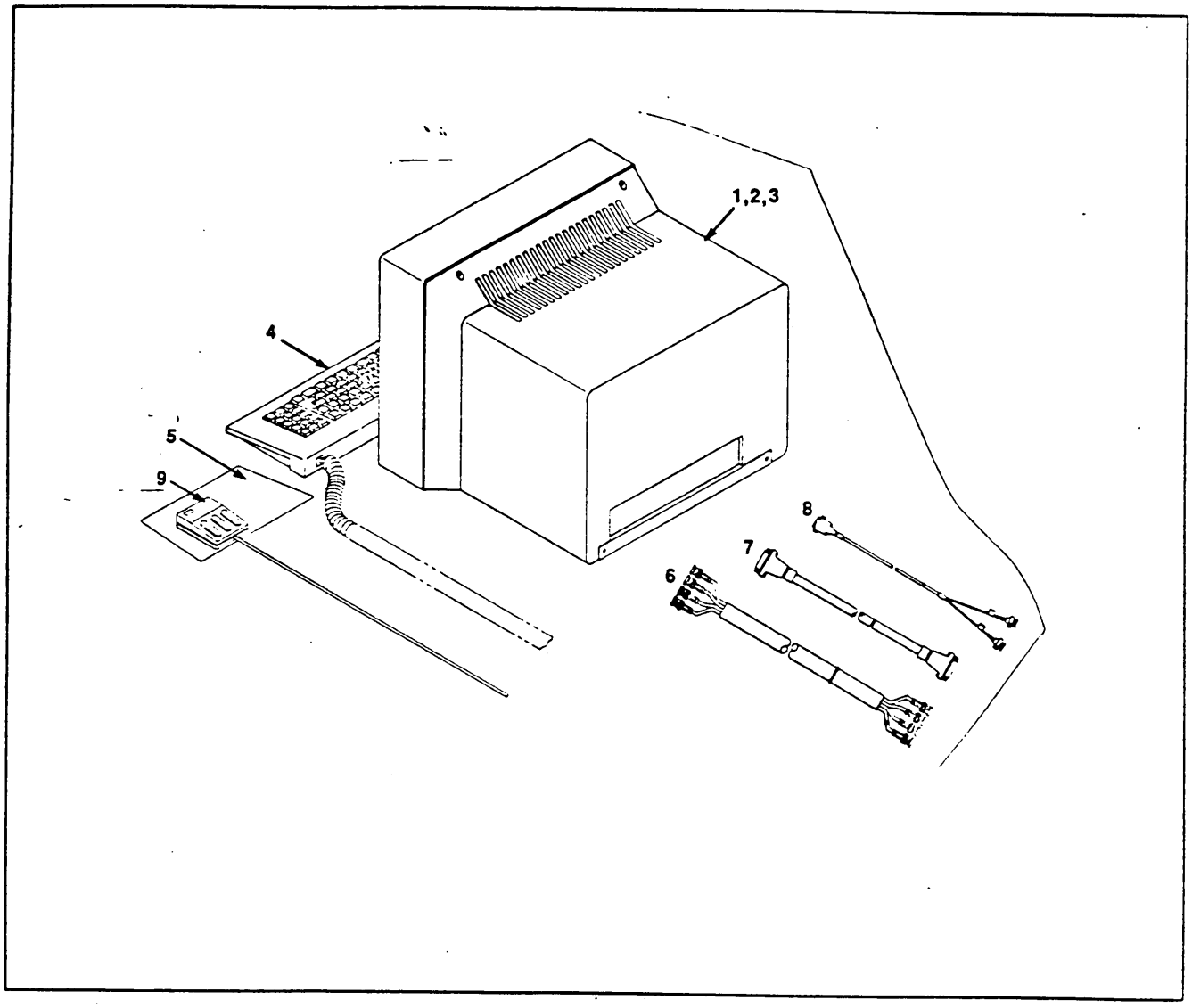
Figure 3-25 *Backplane-to-Cardcage Mounting*



3.12. Illustrated Parts Breakdown

The preceding paragraphs do not provide part numbers for all the components you may need to replace. The Illustrated Parts Breakdown (Figures 3-26 through 3-38) on the pages that follow is intended to help you identify and replace those components.

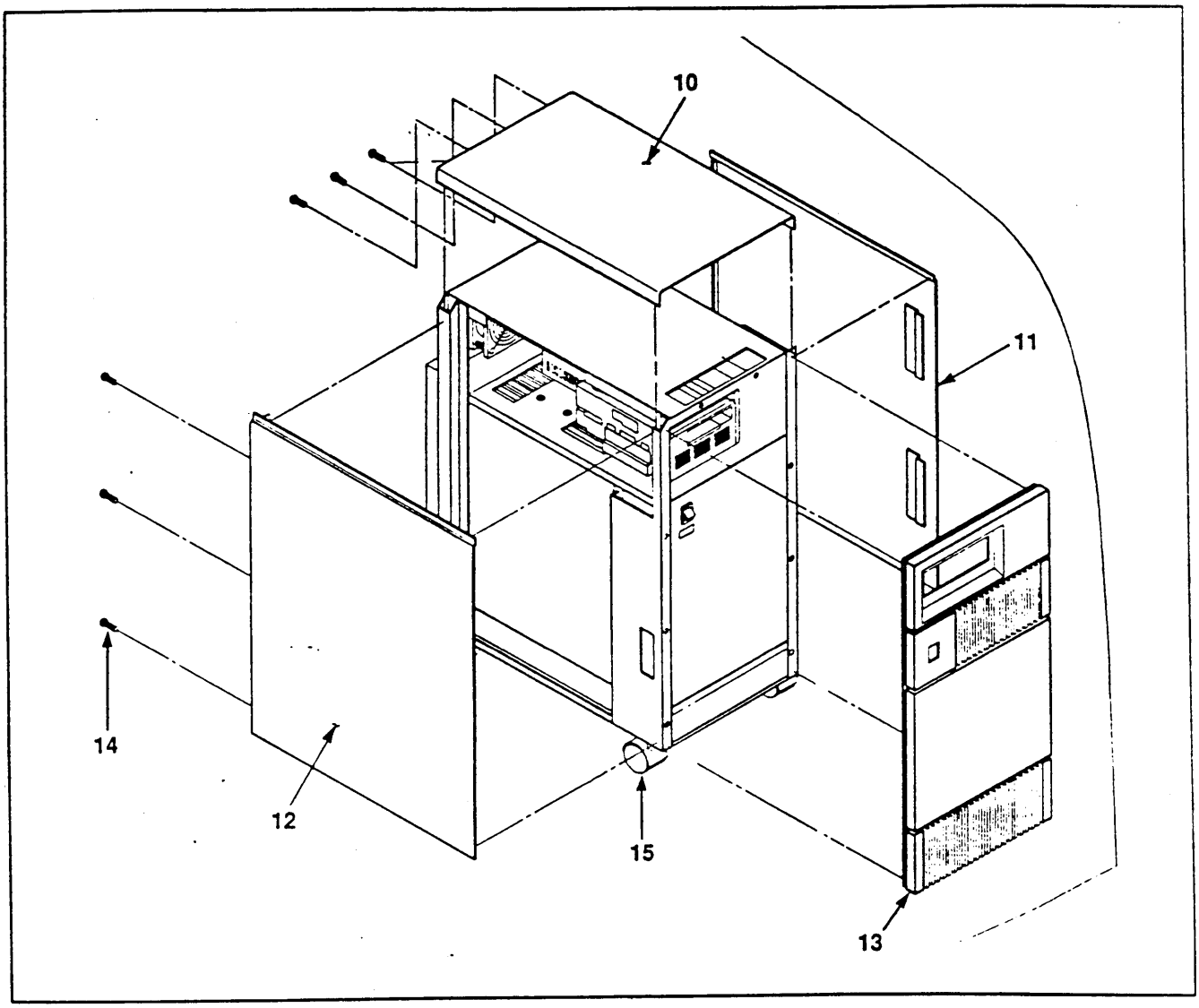
Figure 3-26 *Sun-3/160 Illustrated Parts Breakdown #1: Monitor, Keyboard/Mouse*



Key	*Description*	*Part Number*	*Key*	*Description*	*Part Number*
1	color video monitor*	540-1094	6	color video cable	530-1138
2	monochrome (b/w) monitor	540-1240	7	b/w video cable	530-1133
3	gray scale monitor*	360-1012	8	gray scale video cable	530-1221
4	keyboard	540-1263	9	mouse	530-1058
5	mouse pad	340-1001			

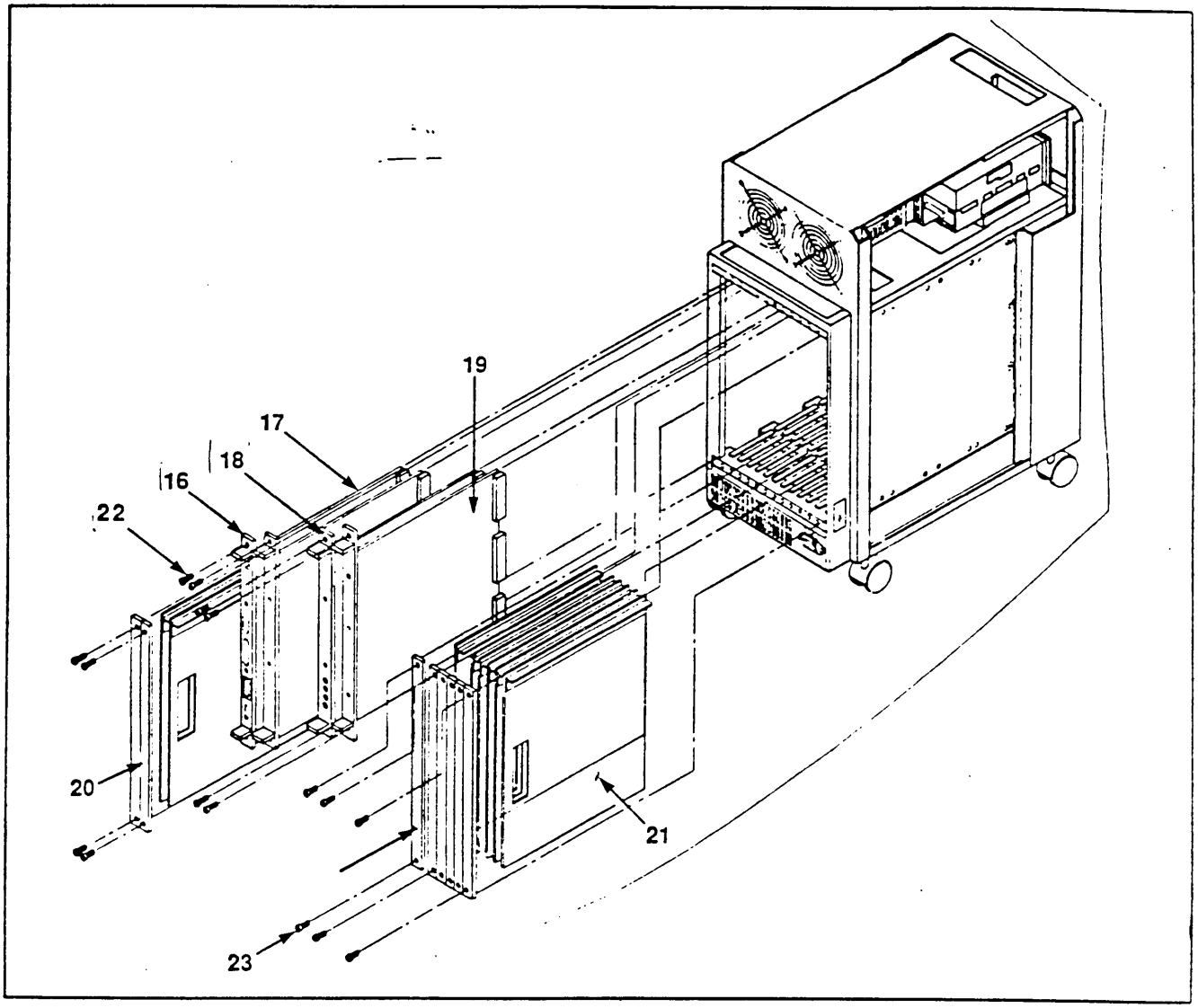
*the color and gray-scale monitors are not shown

Figure 3-27 *Illustrated Parts Breakdown #2: Cover and Panels*



Key	*Description*	*Part Number*
10	top cover	340-1138
11	side panel (right)	340-1261
12	side panel (left)	340-1262
13	bezel	340-1141
14	6-32 x 3/8" Phillips screw (9)	240-1186
15	swivel castor	240-1048

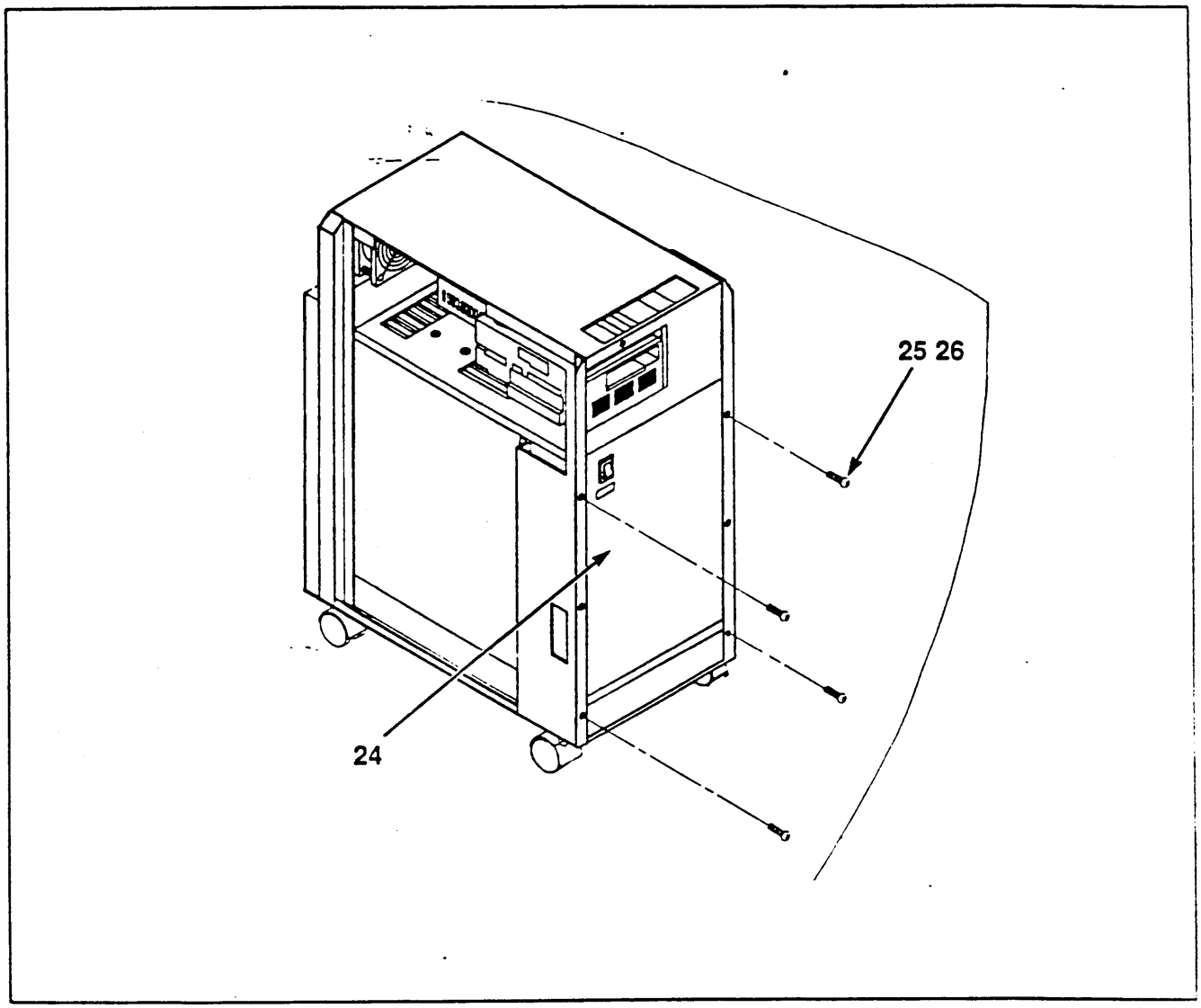
Figure 3-28 *Illustrated Parts Breakdown #3: PC Boards in Card Cage*



Key	*Description*	*Part Number*
16	CPU board (4MB)	501-1094
17	Expansion Memory Board	501-1096(2 Meg) 501-1097(4 Meg)
18	Color Video Board†	501-1014
19	VME SCSI Board	501-1045
20	blank face plate	340-1184
21	air flow restrictor	340-1407
22	hex-head screw	240-1287
23	hex-head screw	240-1292

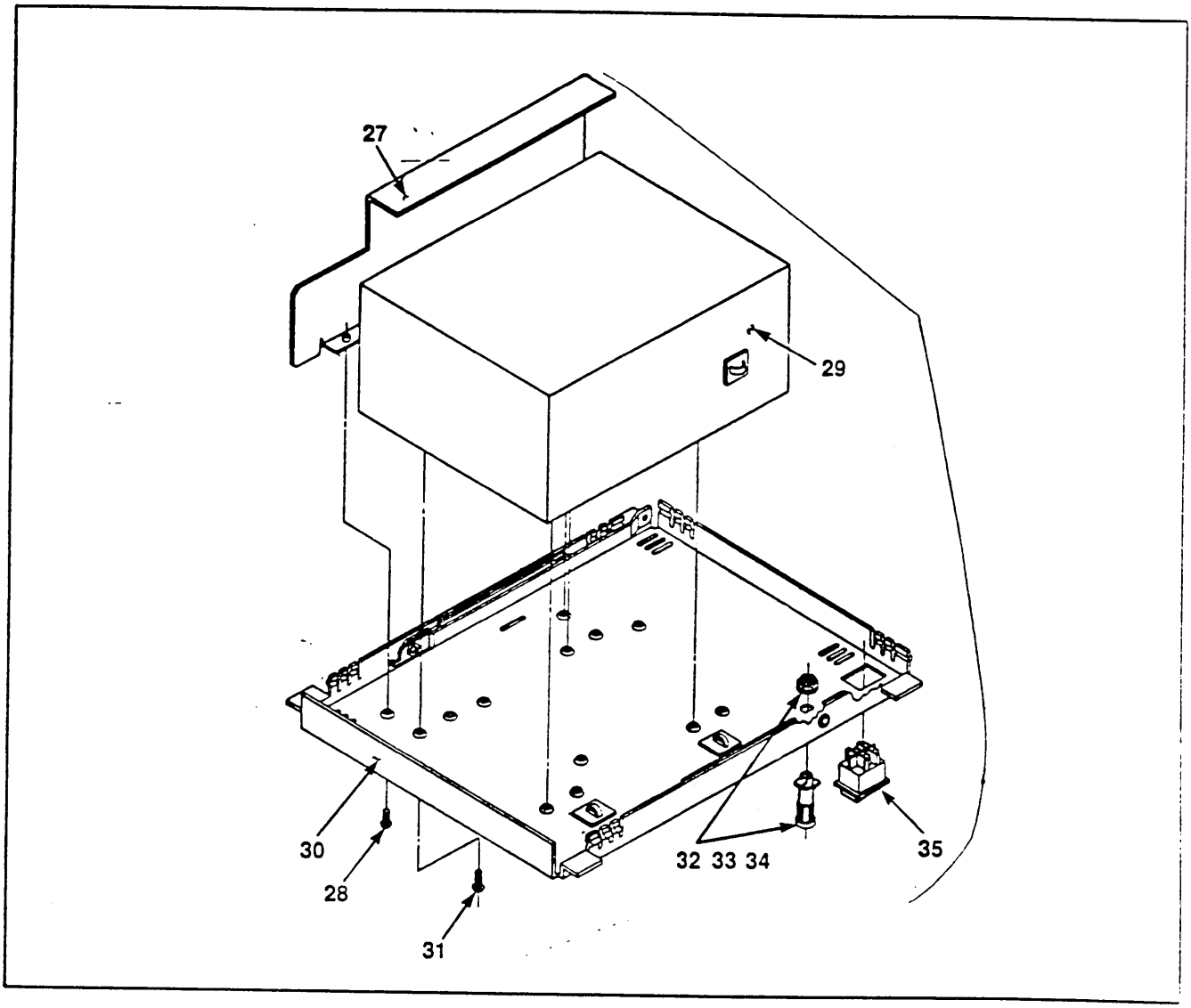
†Note that the color board is shown in this location for reference only. Refer to the *Configuration Procedures* manual for recommended slot assignments.

Figure 3-29 *Illustrated Parts Breakdown #4: Front Door and Castors*



Key	*Description*	*Part Number*
24	power supply panel	340-1363
25	4-40 screws	240-1292
26	4-40 washers	240-1036

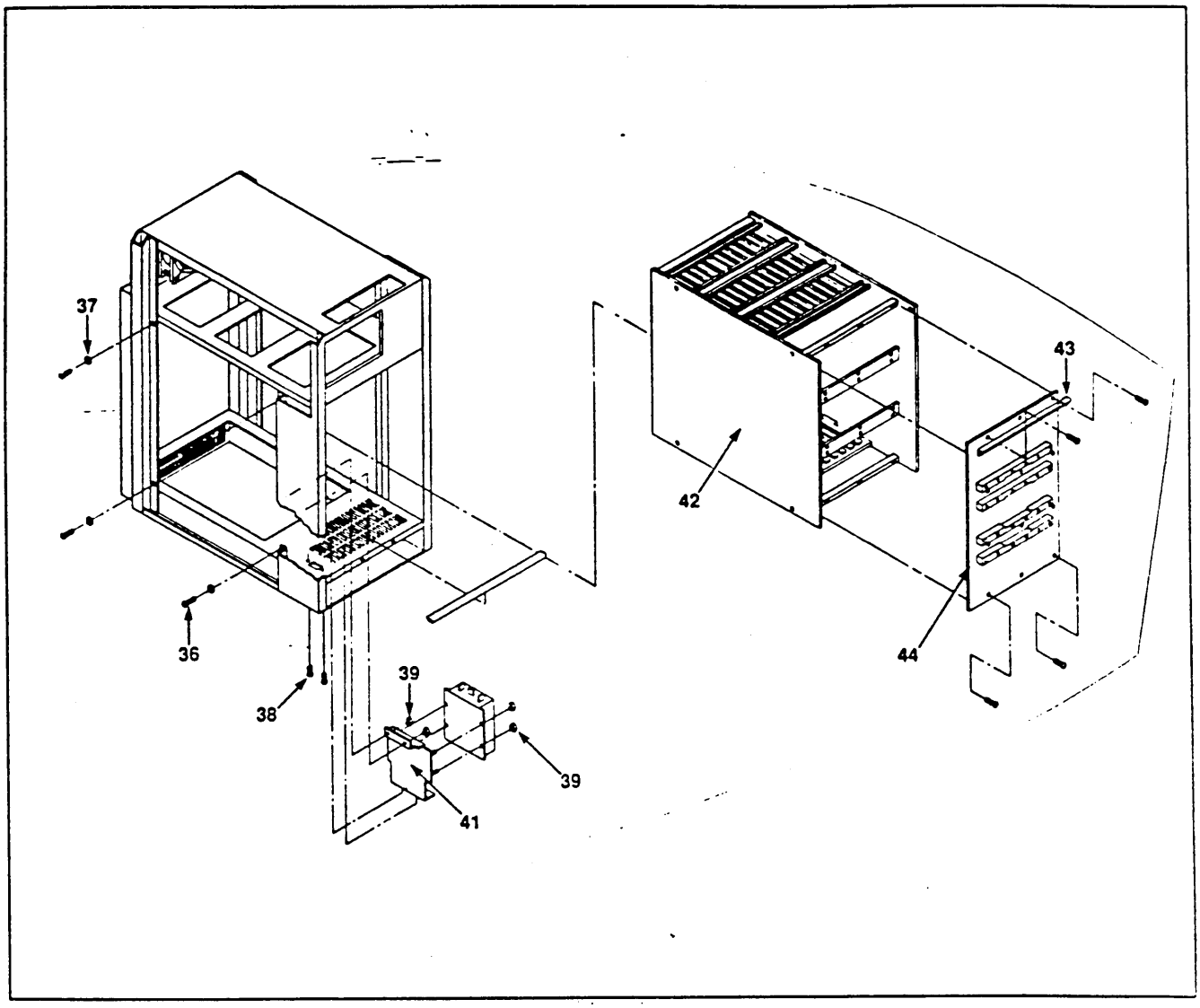
Figure 3-30 *Illustrated Parts Breakdown #5: ETA Power Supply Mounting*



(For Pioneer Power Supply Mounting, refer to Figure 3-7)

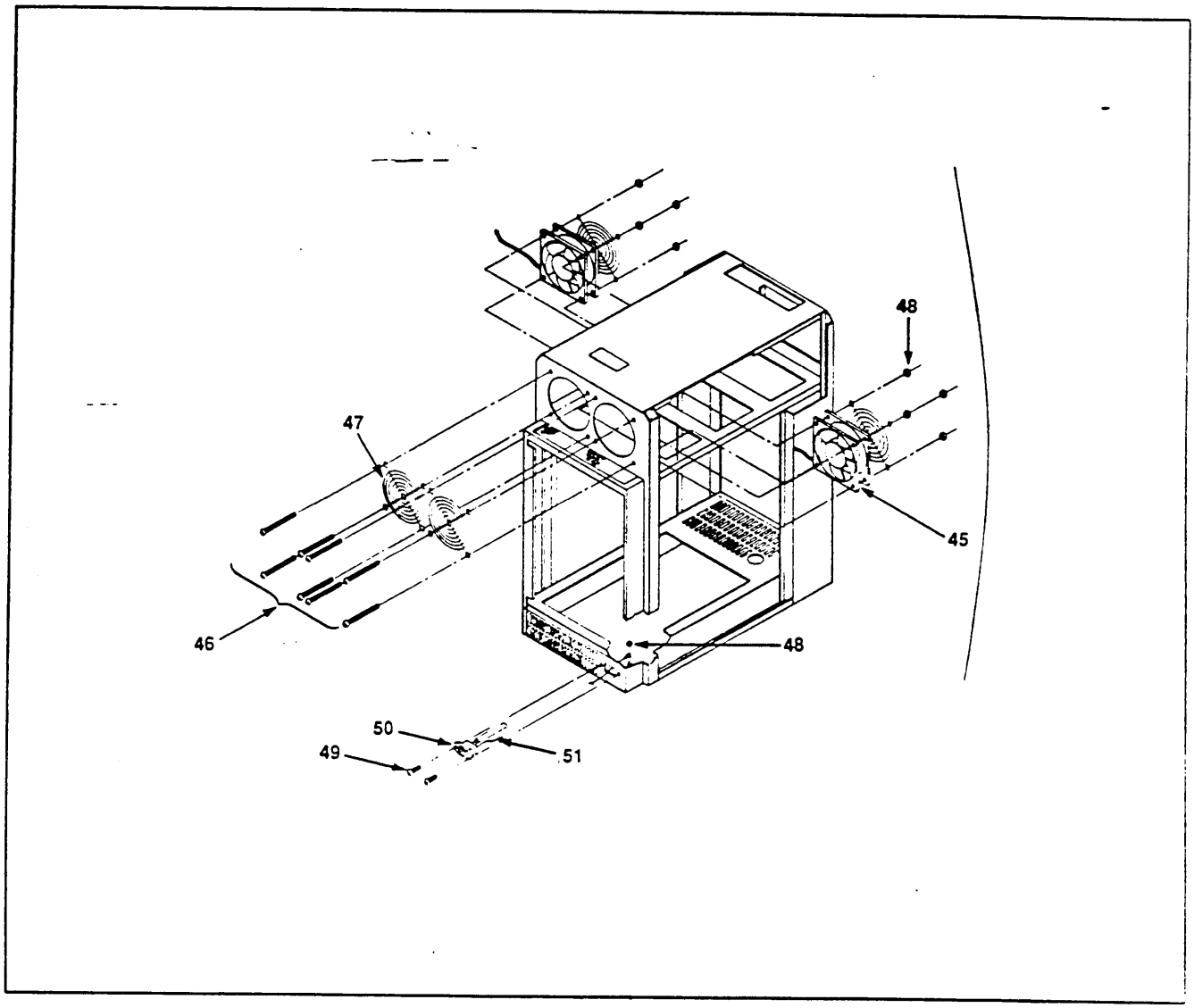
Key	*Description*	*Part Number*
27	cable restraint bracket	340-1373
28	6-32 Phillips screw (2)	240-1186
29	850W power supply (ETA)	300-1016
30	power supply panel	340-1363-03
31	8-32 Phillips screw (4)	240-1203
32	15 Amp, 250V fuse	140-1019-01
33	fuse holder	150-1041
34	fuse carrier	150-1042
35	rocker switch, DPST	150-1018

Figure 3-31 *Illustrated Parts Breakdown #6: Cardcage and EMI Filter*



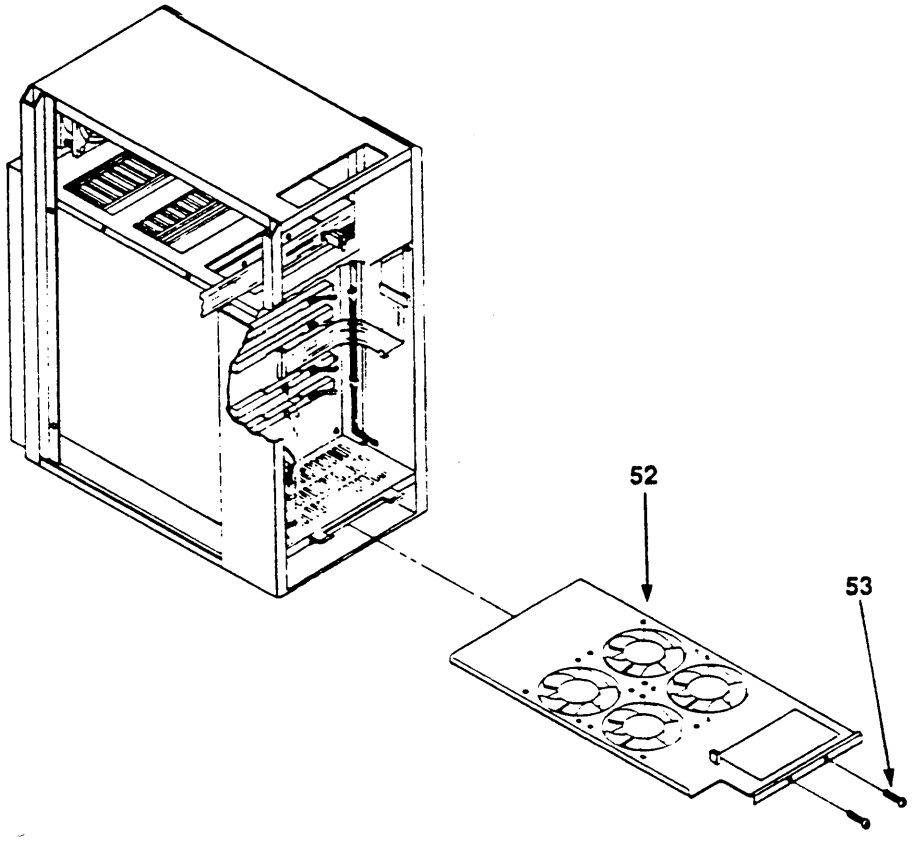
Key	*Description*	*Part Number*
36	cardcage mounting screws (8)	240-1186
37	cardcage mounting washers (8)	240-1036
38	EMI filter mounting screws	240-1291
39	EMI filter mounting nuts (6)	240-0254
40	EMI filter (AC line filter)	150-1129
41	line filter bracket	340-1364-03
42	card cage	370-1086
43	baffle	340-1314
44	backplane	501-1092

Figure 3-32 *Illustrated Parts Breakdown #7: Upper Fan and AC Receptacle*



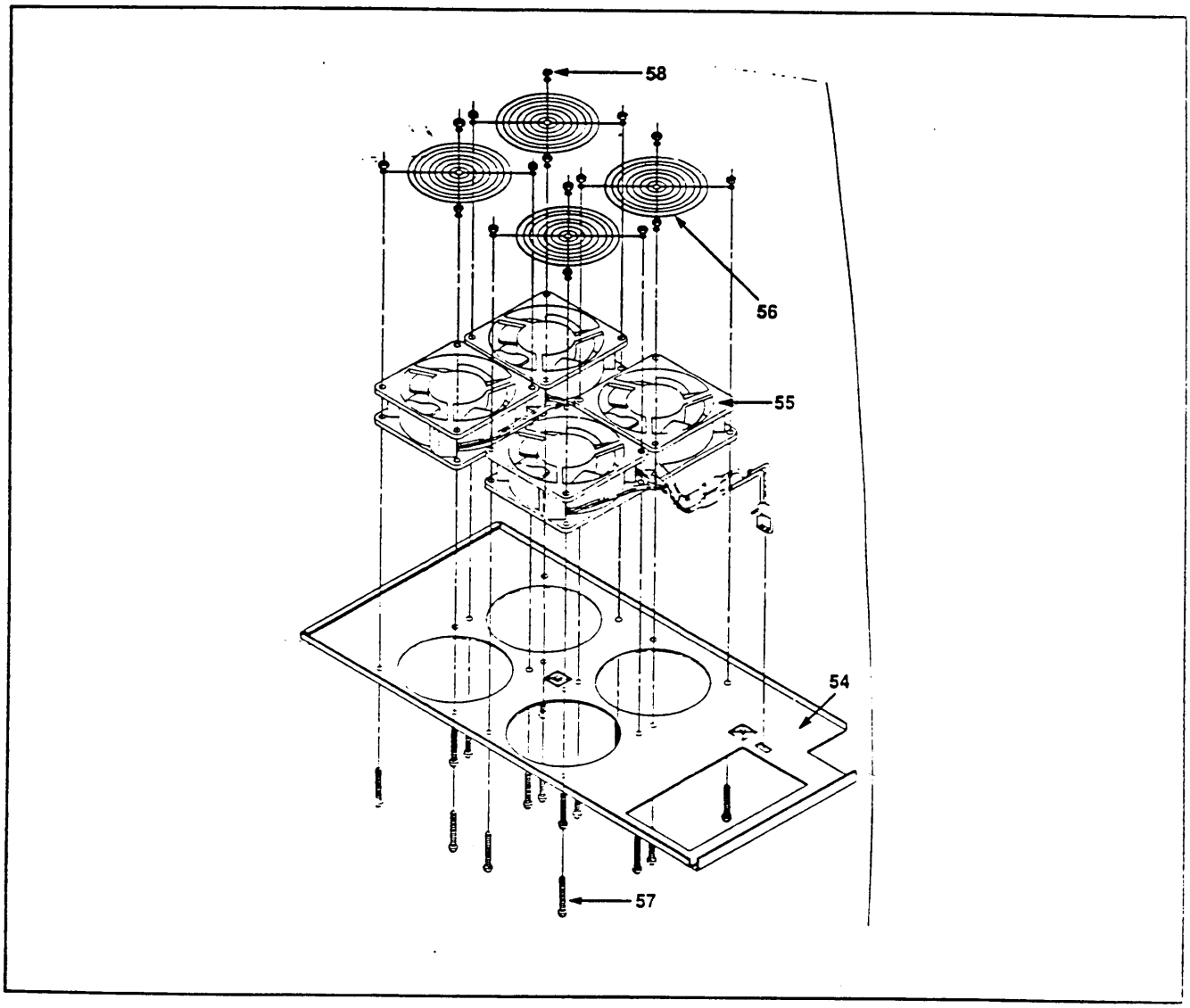
Key	*Description*	*Part Number*
45	upper fan assembly (2)	540-1252
46	6-32 x 2 fan mounting screws (8)	240-1293
47	fingerguard (4)	340-0265
48	6-32 kepnuts (9)	240-0254
49	6-32 screws (2)	240-1186
50	A/C receptacle	530-1230
51	A/C internal harness	530-1231

Figure 3-33 *Illustrated Parts Breakdown #8: Lower Fan Mounting*



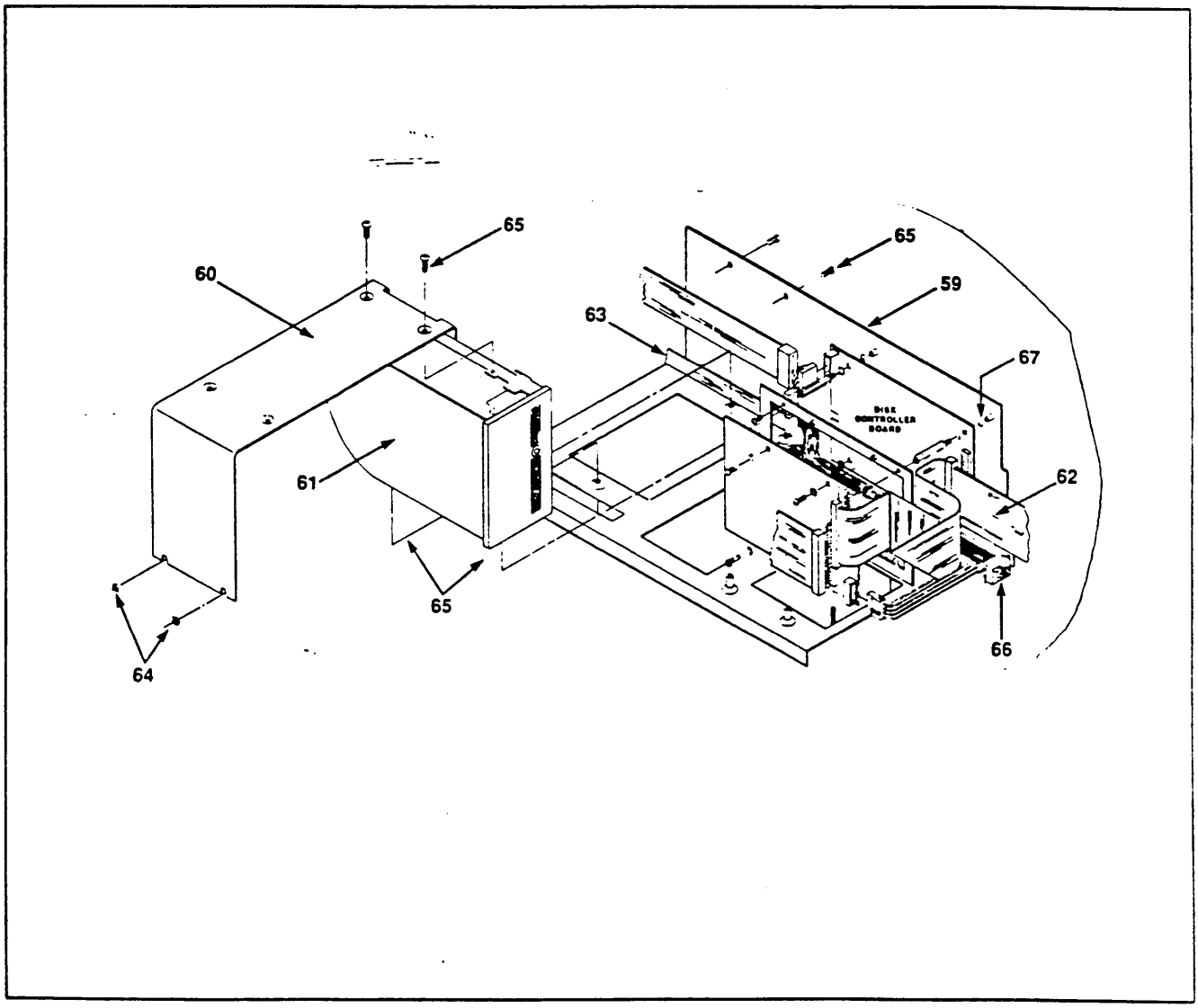
Key	*Description*	*Part Number*
52	air box assembly	540-1082-02
53	airbox mounting screws (2)	240-1186

Figure 3-34 *Illustrated Parts Breakdown #9: Airbox Assembly*



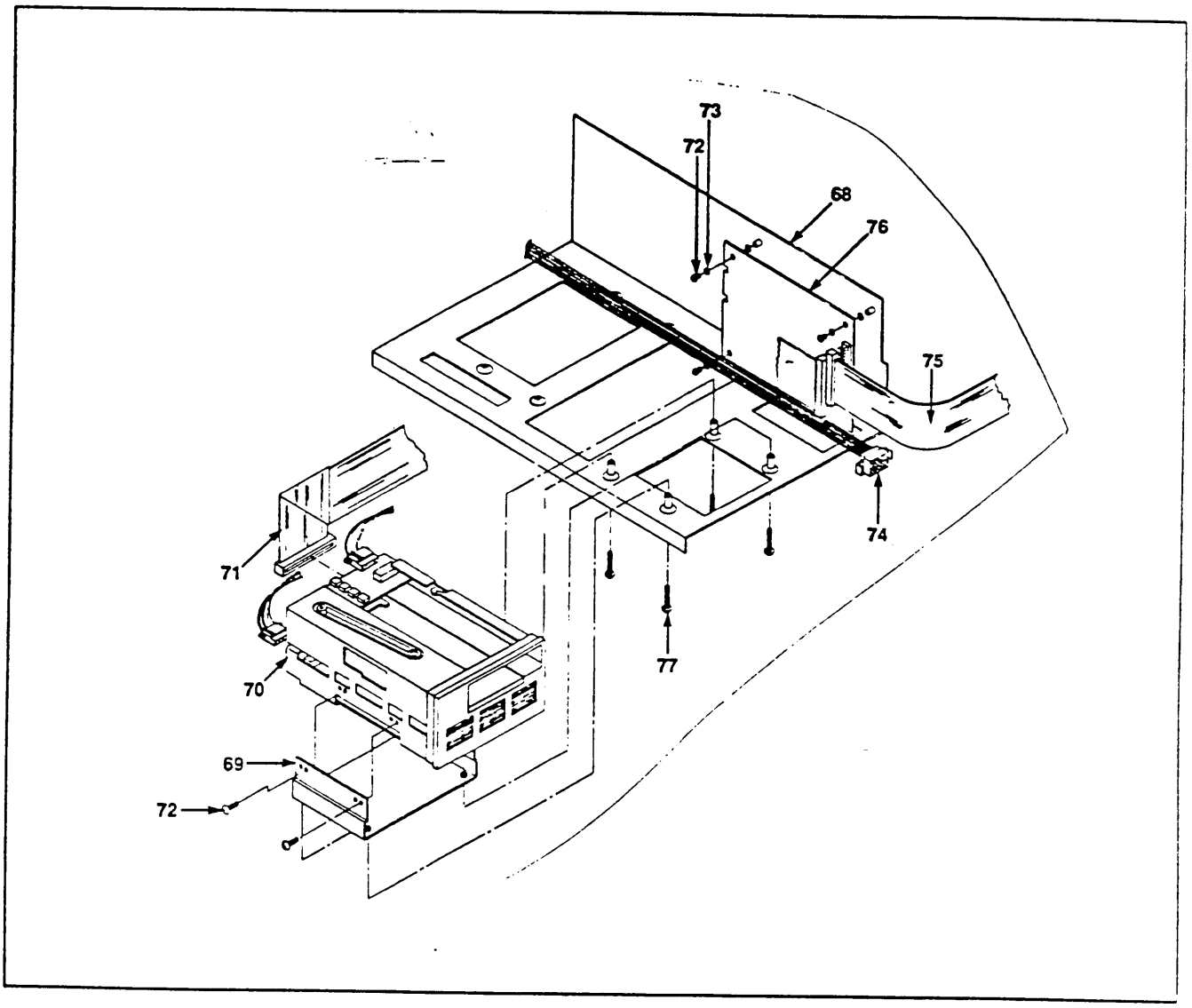
Key	*Description*	*Part Number*
54	fan tray (inverted when installed in pedestal)	540-1147-03
55	fan assembly (4)	540-1252
56	fingerguard (4)	340-0265
57	6-32 screw (16)	240-1293
58	6-32 lock nut (16)	240-0254

Figure 3-35 *Illustrated Parts Breakdown #10: Option Tray With Single Disk (PN 540-1247)*



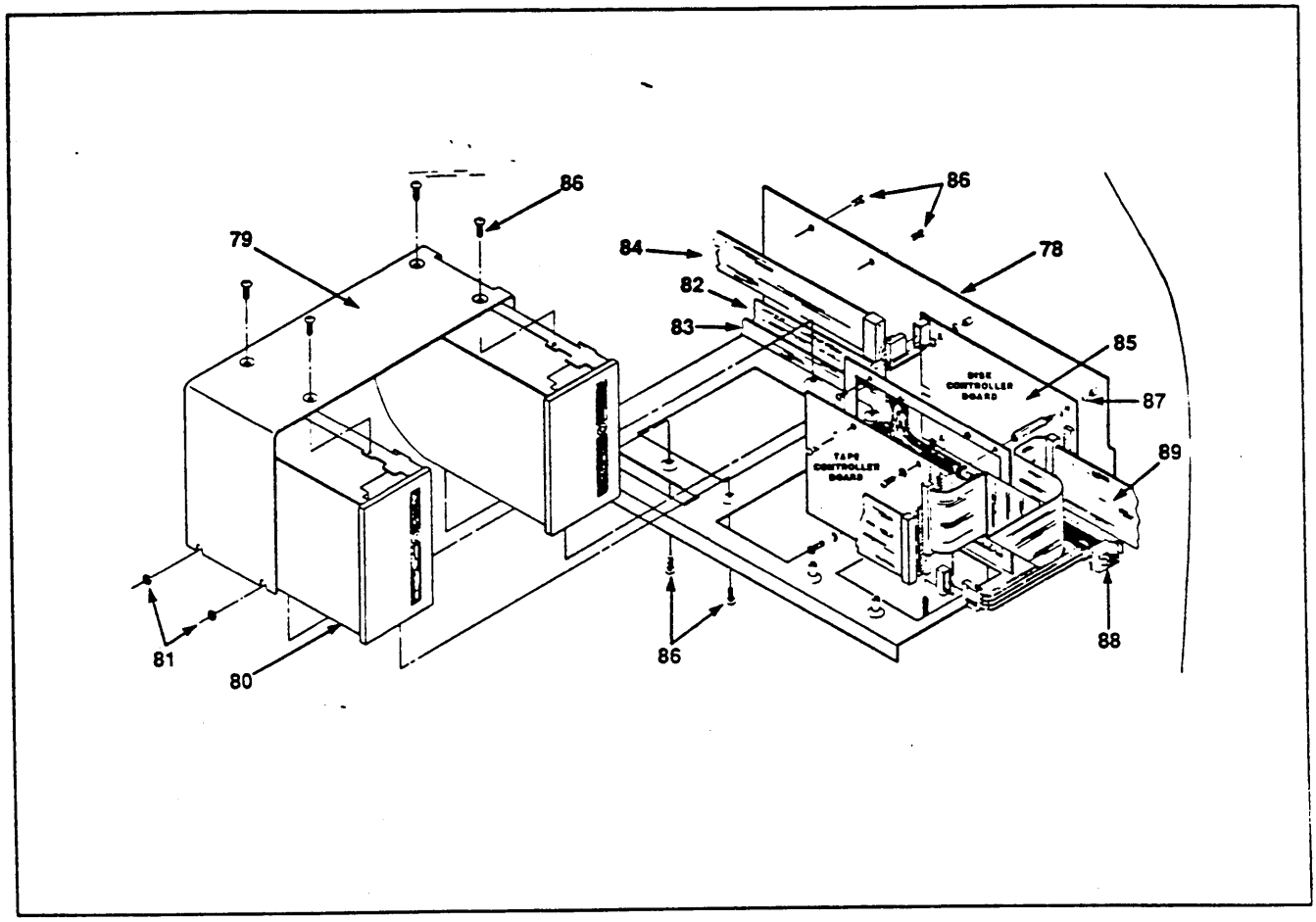
Key	*Description*	*Part Number*	*Key*	*Description*	*Part Number*
59	slide tray	340-1205	65	6/32 x 3/8 pan-head screws	240-1186
60	disk mounting bracket	340-1244-02	66	power harness	530-1135
61	disk drive	370-1034-02	67	flat nylon washers	230-1046
62	data harness (SCSI)	530-1134-03			
63	dual disk command cable	530-1157			
64	6-32 lock nut	240-0254			

Figure 3-36 *Illustrated Parts Breakdown #11: Option Tray With Tape Only (PN 540-1117)*



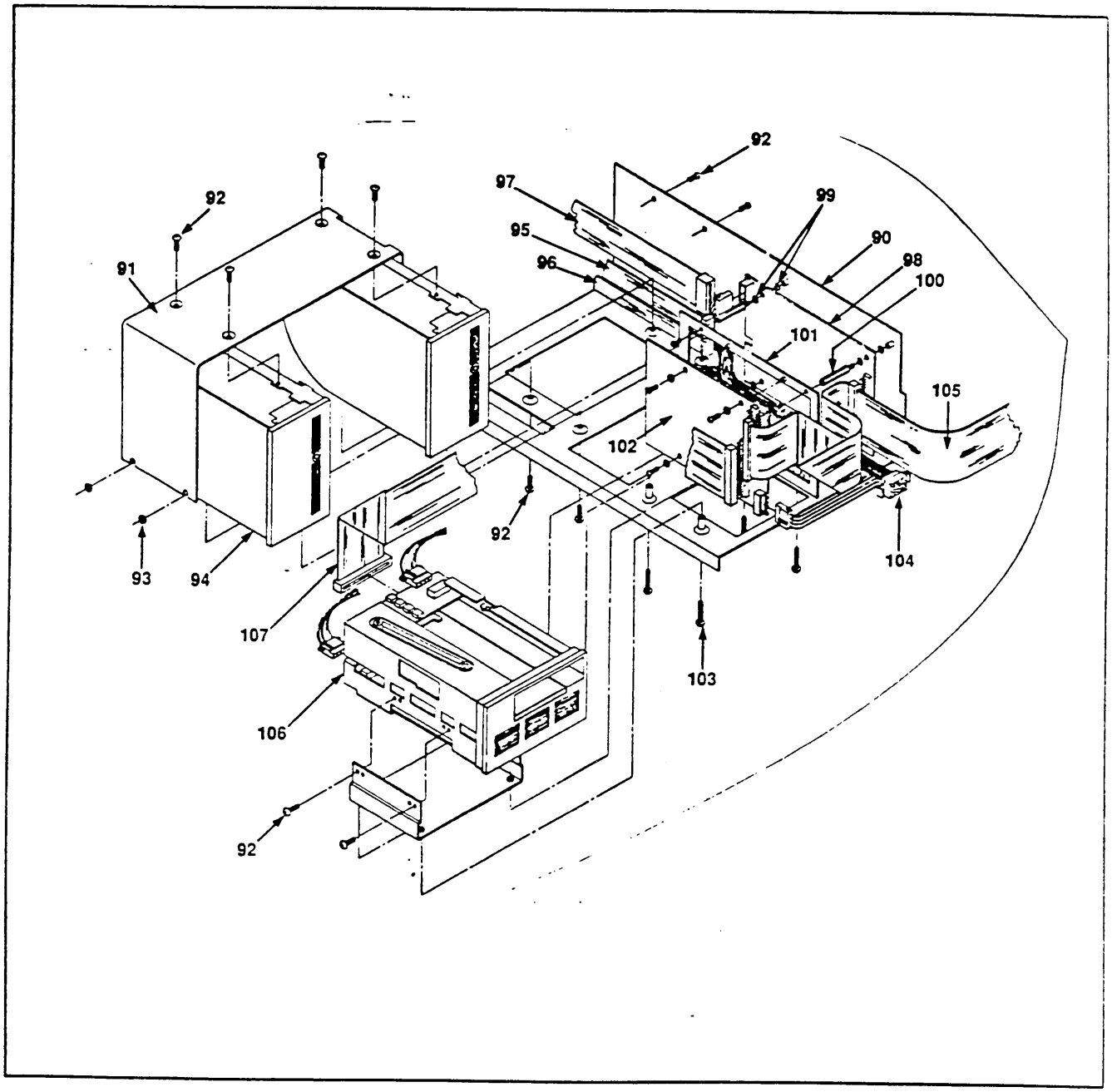
Key	*Description*	*Part Number*
68	slide tray	340-1205-07
69	drive mounting support	340-1218-05
70	tape drive	370-1037-02
71	tape signal I/F cable	530-1141-03
72	6/32 x 3/8 screws (8)	240-1186
73	flat nylon washers	130-1046
74	power harness	530-1135
75	data harness (SCSI cable)	530-1134-03
76	tape controller board	370-1011
77	6-32 x 1" pan-head screws	240-1316

Figure 3-37 *Illustrated Parts Breakdown #12: Option Tray With Dual Disks (PN 540-1246)*



Key	*Description*	*Part Number*
78	slide tray	340-1205-07
79	disk mounting bracket	340-1244-02
80	disk drive	370-1034-02
81	6-32 lock nut (2)	240-0254
82	double disk data cable (outside drive)	530-1145-02
83	inside disk data cable	530-1142-02
84	dual disk command cable	530-1157-02
85	disk controller board	370-1010
86	6-32 x 3/8" screws	240-1186
87	flat nylon washers (12)	130-1046
88	power harness	530-1135-02
89	data harness (SCSI cable)	530-1134-02

Figure 3-38 *Illustrated Parts Breakdown #13: Option Tray, Dual Disks and Tape (PN 540-1130)*



Key	*Description*	*Part Number*
90	slide tray	340-1205-07
91	disk mounting bracket	340-1244-02
92	6/32 x 3/8" screws	240-1186
93	6-32 lock-nuts	240-0254
94	disk drive	370-1034-02
95	double disk data cable (outside drive)	530-1145-02
96	inside disk data cable	530-1142-02
97	dual disk command cable	530-1157-02
98	disk controller board	370-1010-06
99	flat nylon washers (12)	230-1046
100	stand-offs (4)	240-1327-01
101	PC plate	340-1317
102	tape controller board	370-1011
103	6-32 x 1" pan head screws (4)	240-1316
104	power harness	530-1135-02
105	option tray data harness	530-1134-03
106	tape drive	370-1037-02
107	tape signal I/F cable	530-1141

A

Cardcage Configuration

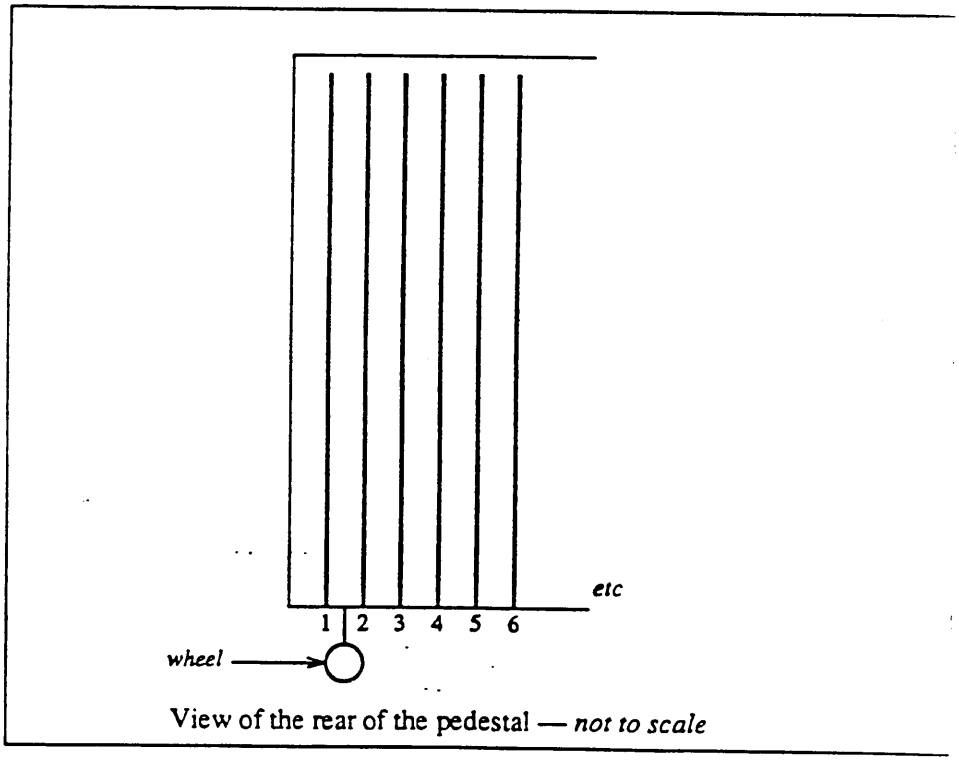
A

Cardcage Configuration

A.1. Cardcage Slot Numbering and Board Locations

The following figure and tables illustrate how the Sun-3/160 cardcage slots are numbered and which boards are slot dependent. Refer to the *Sun Configuration Procedures* manual for more information.

Figure A-1 *Card Slot Numbering Viewed from Rear of Pedestal*

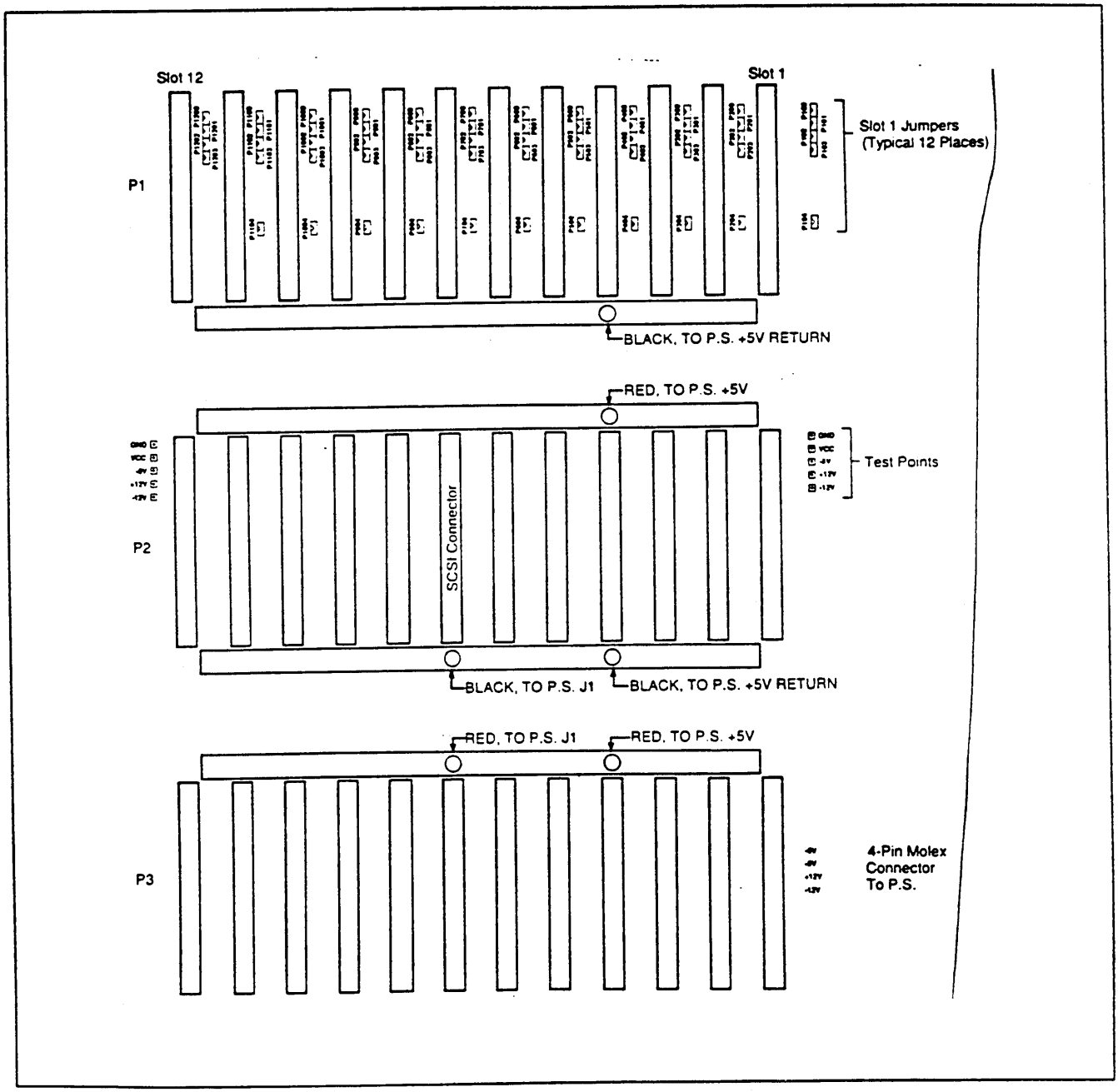


View of the rear of the pedestal — *not to scale*

A.2. Backplane Connectors/Jumpering

The following figure illustrates the relationship between the backplane's P connectors and the cardcage slot numbering. All 12 slots are connected via P1, while only slots 1-6 and 10-12 are connected via P2 and P3.

Figure A-2 *Slot Numbering and P Connectors — As Seen From the Front of Pedestal*



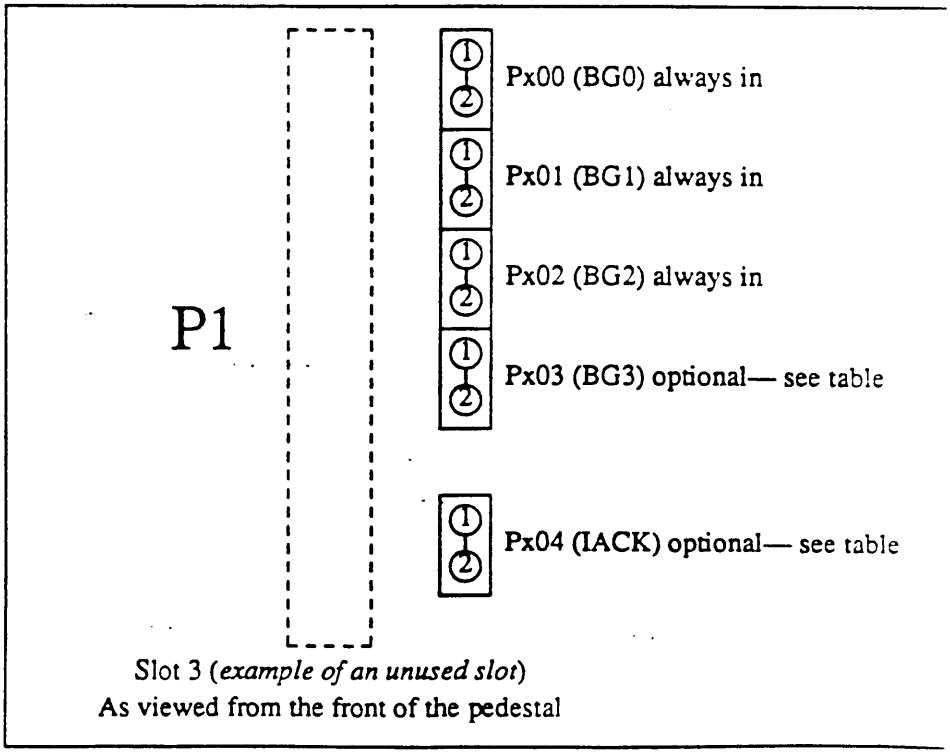
Backplane Connector Function

This table shows which type of bus is serviced by each row of pins on the 96-pin P1, P2 and P3 connectors located on the backplane. The "P2" bus is the memory or physical address bus described in Chapter 1 of this manual, and is not to be confused with the P2 connector.

Connector	*Row*	*Function*
P1	A	VMEbus
	B	VMEbus
	C	VMEbus
P2	A	"P2 bus"
	B	VMEbus
	C	"P2 bus"
P3	A	Power
	B	"P2 bus"
	C	Power

The following figure illustrates jumpering an unused cardcage slot. These jumpers are also used when the slot contains a board that does not use or pass the BG3IN/BGOUT signals. For more information on backplane configuration, refer to the *Configuration Procedures* manual.

Figure A-3 *Jumpering Unused Cardcage Slots*



Jumper IN or OUT		Board
Jumper Jx03 *Bus Grant*	*Jumper Jx04* *Interrupt Acknowledge*	
OUT	OUT	SUN-3 CPU
IN	IN	SUN 2nd Expansion board
IN	IN	SUN 3rd Expansion board
IN	IN	SUN 4th Expansion board
IN	IN	SUN VME FPA
OUT	OUT	VME SCSI Ctlr
OUT	OUT	SUN GP
IN	IN	SUN GB
OUT	OUT	2nd Ethr Ctlr
OUT	OUT	1/2" Tape Ctlr
OUT	OUT	1st SMD Ctlr
OUT	OUT	2nd SMD Ctlr
IN	OUT	SUN VME Color
OUT	OUT	SUN ALM Ctlr

All boards are inserted or extracted from the back of the Sun-3/160. The CPU and Expansion boards must be in slots 1 to 4 (slots are numbered from left to right, when facing the rear of the pedestal). This is because the CPU and Expansion boards must share a common memory (P2) bus, available in the 1-4 slot arrangement.

Slots 1 through 6 and slots 10, 11, and 12 share a common P2 bus.

Bus priority is determined by the board's position in the card cage; a board in slot 4 has a higher bus priority than a card in slot 5. Consult the *Configuration Procedures* manual for information on recommended cardcage slot assignments for various configurations.

B

CPU Board and VME-SCSI Board Connector Pinouts

B

CPU Board and VME-SCSI Board Connector Pinouts

This appendix provides connector pinouts for the 2060 CPU and VME-SCSI boards.

B.1. CPU Board Connector Pinouts

- Mouse/Keyboard Connector
- Serial Port(s)
- Ethernet Connector
- Video Connector

Table B-1 *Pinout of Keyboard/Mouse DB-15 Connector*

Pin	*Signal*	*Pin*	*Signal*
1	RXD0 (keyboard)	8	GND
2	GND	9	GND
3	TXD0 (keyboard)	10	VCC
4	GND	11	VCC
5	RXD1 (mouse)	12	VCC
6	GND	14	VCC
7	TXD1 (mouse)	15	VCC

Table B-2 *Pinout of Serial Ports A and B*

Pin	*Signal*	*Pin*	*Signal*
2	TXD	8	DCD
3	RXD	15	DB
4	RTS	17	DD
5	CTS	20	DTR
6	DSR	24	DA
7	GND	25	VERR

Table B-3 *Pinout of Ethernet Connector*

Pin	*Signal*	*Pin*	*Signal*
2	E.COL+	9	E.COL-
3	E.TXD+	10	E.TXD-
5	E.RXD+	12	E.RXD-
6	GND	13	+12V
7	VCC		

Table B-4 *Pinout of Video Connector*

Pin	*Signal*	*Pin*	*Signal*
1	VIDEO+	6	VIDEO-
3	HSYNC	7	GND
4	VSYNC	8	GND
5	VCC	9	GND

B.2. VME-SCSI Board Cable Pinout

This table provides the pinout for the cable that connects the VME-SCSI board with the drive controller boards that reside in the option tray.

Table B-5 *VME-SCSI Board Cable Pinout*

Signal	*Pin*	*Signal*	*Pin*
-DB(0)	2	GND	1
-DB(1)	4	GND	3
-DB(2)	6	GND	5
-DB(3)	8	GND	7
-DB(4)	10	GND	9
-DB(5)	12	GND	11
-DB(6)	14	GND	13
-DB(7)	16	GND	15
-DB(P)	18	GND	17
GND	20,22,24	GND	19
TERMPWR	26	GND	21
GND	28,30	GND	23
-ATN	32	GND	25
GND	34	GND	27
-BSY	36	GND	29
-ACK	38	GND	31
-RST	40	GND	33
-MSG	42	GND	35
-SEL	44	GND	37
-C/D	46	GND	39
-REQ	48	GND	41
-I/O	50	GND	43
		GND	45
		GND	47
		GND	49

C

Degaussing the Monitor

C

Degaussing the Monitor

CAUTION **The degaussing coil demagnetizes EVERYTHING. Make certain that ALL TEST EQUIPMENT, MAGNETIC PERIPHERALS AND MEDIA are at least five feet from the degaussing coil before plugging it in, or else you will erase your media!**

1. Remove the degaussing coil from its container.
2. Before plugging it in, make doubly certain that:

   - All magnetic peripherals, media and test equipment are AT LEAST FIVE FEET away from the coil, and that
   - the coil is AT LEAST SIX FEET from the monitor.

NOTE *Remember, it is the coil itself that does the demagnetizing; the area in the center of the coil does nothing. All available sides, the top, rear and the front of the monitor need to be degaussed.*

3. Hold the coil perpendicular to the monitor, at least six feet away, and plug the coil in.
4. Press the coil switch and turn it parallel to the monitor screen, bringing the coil to within three inches of the screen.

NOTE *The coil may become too warm to hold after about two minutes of degaussing.*

5. With the coil parallel to and about three inches from the surface of the screen, move the coil in six inch circular motions over the screen. Do this for 15 to 30 seconds.

CAUTION **DO NOT RELEASE THE SWITCH OR PULL THE PLUG!**

6. Move to the sides of the monitor. Move the coil in short circular motions over each surface — sides, top and rear; 15 to 30 seconds per surface. Finally, degauss the monitor screen again.
7. When you have degaussed the monitor, keep the the switch pressed ON and the coil parallel to the screen. Slowly move the coil away from the monitor, moving it in 12 inch circular motions, until you are six feet away.
8. Turn the coil perpendicular to the screen and release the switch or pull the plug.

C.1. Internal Degaussing

If color distortion persists, the monitor may need internal degaussing. To accomplish internal degaussing, turn the monitor power ON and press the DEGAUSSING button. Hold the button in until the image ceases to shimmer, which should take no longer than 30 seconds. Allow a cooling period of at least eight minutes following internal degaussing and prior to initiating a maximum strength magnetic field degaussing cycle.

D

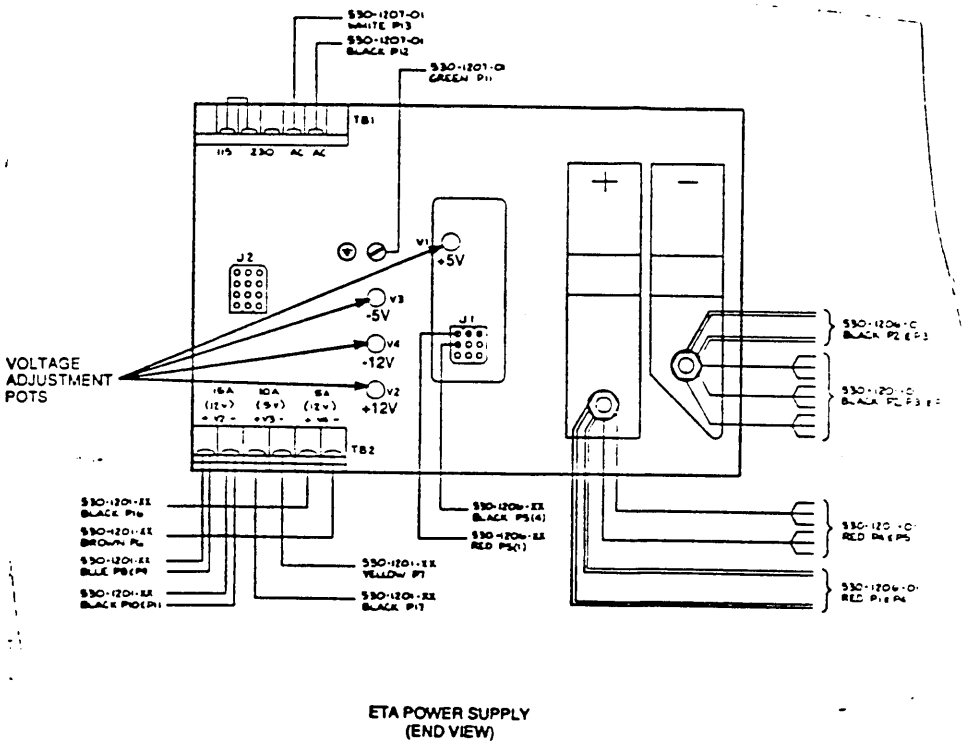
Power Supply Voltage Adjustment

D

Power Supply Voltage Adjustment

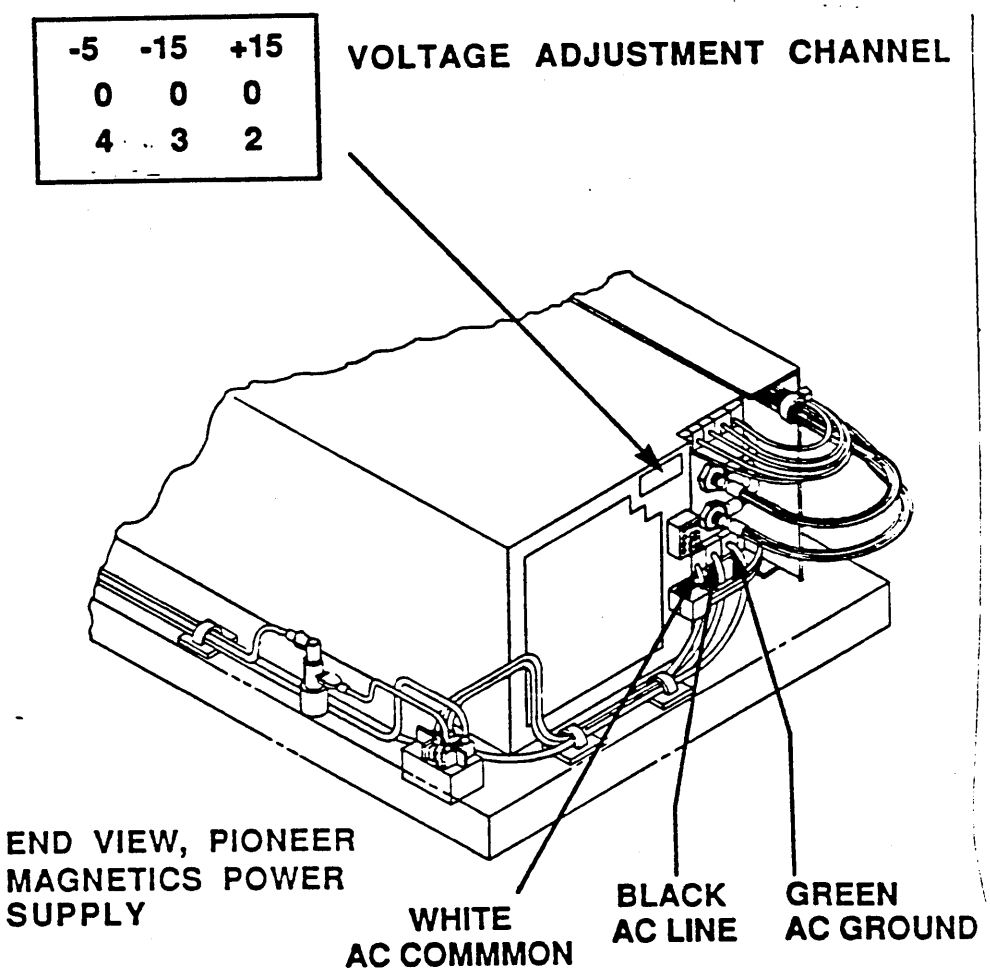
This appendix shows the location of the VDC output adjustment potentiometers on both power supply types found in Sun-3/160s. We recommend that you adjust +5V only, and refer any other adjustments to a Sun repair depot.

Figure D-1 *ETA Adjustment Pot Locations*



ETA POWER SUPPLY
(END VIEW)

Figure D-2 *Pioneer Adjustment Pot Locations*



E

ASCII/Hex Conversion Chart

E

ASCII/Hex Conversion Chart

E.1. Use of the ASCII/Hex Conversion Chart

This table is intended to aid you in entering EEPROM parameters that require the hexadecimal equivalent to ASCII characters.

Table E-1 *ASCII/Hex Conversion*

ASCII	*Hex*	*ASCII*	*Hex*	*ASCII*	*Hex*	*ASCII*	*Hex*
nl (line feed)	0A	6	36	N	4E	f	66
cr (return)	0D	7	37	O	4F	g	67
sp (space)	20	8	38	P	50	h	68
!	21	9	39	Q	51	i	69
"	22	:	3A	R	52	j	6A
#	23	;	3B	S	53	k	6B
$	24	<	3C	T	54	l	6C
%	25	=	3D	U	55	m	6D
&	26	>	3E	V	56	n	6E
'	27	?	3F	W	57	o	6F
(	28	@	40	X	58	p	70
)	29	A	41	Y	59	q	71
*	2A	B	42	Z	5A	r	72
+	2B	C	43	[	5B	s	73
,	2C	D	44	\	5C	t	74
-	2D	E	45	]	5D	u	75
.	2E	F	46	^	5E	v	76
/	2F	G	47	_	5F	w	77
0	30	H	48	`	60	x	78
1	31	I	49	a	61	y	79
2	32	J	4A	b	62	z	7A
3	33	K	4B	c	63	{	7B
4	34	L	4C	d	64	|	7C
5	35	M	4D	e	65	}	7D
						~	7E
						del	7F

Revision History

Revision	*Date*	*Comments*
1	15 July 1985	First draft; Chapters 1 and 3 Only
2	26 July 1985	First draft including Chapter 2
3	15 August 1985	Second draft for Carrera Special; review comments incorporated
4	15 October 1985	Beta Version; Updated Boot PROM diagnostics and included EEPROM programming; Added VME compliancy data, power consumption table and GP jumper options.
50	15 January 1986	FCS Release of this Field Service Manual; Added Illustrated Parts Breakdown; Transferred jumper information to Configuration Procedures Manual; Added to Troubleshooting Flow Chart; Beta comments incorporated.

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