LM-2 Unibus I/O

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1. LM-2 Unibus I/O

1.1 Introduction

The LM-2 contains a Unibus (trademark of Digital Equiptment Corp.) for connection of I/O devices. The standard LM-2 configuration includes several I/O devices that are connected to the Unibus; the interfaces for all of these standard devices are located on the Input/Output Board ("IOB"). This document describes the hardware related to the Unibus, explaining how to attach new devices, and what is included on the IOB.

It is assumed that the reader understands the basic concepts of the Unibus, what kinds of signals it includes, and what a Small Peripherals Controller Slot ("SPC slot") is.

1.2 Unibus Card Slots

The LM-2 has several slots into which Unibus interfaces may be plugged. These slots are located in the I/O/Memory card cage (the big card cage, toward the rear of the machine, as opposed to the six-card cage that holds the processor). Slots 1 through 10 (inclusive) are configured as Unibus SPC slots and can hold Unibus interfaces. The rest of the slots in the cage are for devices that interface to the LM-2's 32-bit Xbus, and Unibus devices should *not* be plugged into those slots. The two parts of the card cage are separated by the Bus Interface ("BUSINT") wire-wrap board, which occupies slot 11 (and uses up slot 12) of the card cage.

The LM-2 Input/Output Board ("IOB") occupies slot 2, and since it is a wire-wrap board, it uses up slot 3 as well. This board has several standard I/O devices; it will be described below.

The Unibus can be extended by plugging a Unibus cable into one of the slots; it is recommended that slot 1 be used for this purpose. Paddles A and B of slot 10 contain a Unibus terminator; a quad-high I/O interface board can still be plugged into this slot. The remaining slots, 4 through 9, are available for new I/O devices. When an LM-2 is fitted with the color option, Color DAC boards occupy paddles A and B of slots 8 and 9; quad-high I/O interface boards can still be plugged into these slots while the Color DACs are present.

You can attach Qbus (Qbus is a trademark of Digital Equiptment, Corp.) devices to an LM-2 by using a Qniverter (available from Able Computer, order #10067). The Qniverter plugs directly into an LM-2 Unibus slot and provides a Qbus. (So far, nobody has tried running a DMA Qbus device this way, but regular program controlled access and interrupts are known to work correctly.)

The SPC slots in the LM-2 are not completely compatible with the standard definition of the SPC slot. The +15 and -15 volt power supplies are not provided (but the +12 and -5 are). The ACLO and DCLO signals do not exist; you may need to pull up either or both of these lines if your device responds to them. The PA and PB signals do not exist. Although the C0 and C1 signals both exist, the LM-2 never performs DATOB nor DATIP cycles. The duplicate data lines on paddle F, which some devices use for interrupts, are not present. The NPG.IN signal is on CA1 and the NPG.OUT signal is on CB1; the location of these signals is not well-standardized among various implementations of SPC backplanes. There are no bus-grant jumpers, and so plugging in standard bus-grant continuity cards is not sufficient to move the bus-grant signals across the backplane; all the bus-grant signals must be wire-wrapped on the backplane. On a standard LM-2, BG5 is wired to slot 2 (the IOB), and the other grant lines are not connected. They may be found at slot 11; see the drawing labelled "CUBUS" in the documentation of the BUSINT.

The pin assignments of the SPC slots can be found from the drawing labelled "HEXSPC" in the documentation of the IOB; see this drawing for complete details.

1.3 Addressing

The Unibus appears in the physical address space of the LM-2 at locations 17400000 through 17777777, which is 77400000 through 77777777 in the virtual address space. Each 16-bit word (pair of byte addresses) of the Unibus appears as the low half of a 32-bit LM-2 word. However, programs do not need to know these numbers. To read or write a Unibus location, a program should use the functions `%unibus-read` and `%unibus-write`, which are documented in *The Lisp Machine Manual*.

Locations 766040 through 766136 are used by the Bus Interface (BUSINT) board for various purposes, such as the machine diagnostic features (the SPY bus and debug interface), an error status register, and control over interrupts. The meanings of these locations are given in the *CADR* document.

Locations 764100 through 764176 are used by the Input/Output Board (IOB). The meanings of these locations are detailed below.

In order to allow a device on the Unibus to do Direct Memory Access (DMA), it must be able to access memory. The main memory of the LM-2 is located on the Xbus, not on the Unibus. To allow Unibus devices to address memory, a mapping feature is provided. Unibus locations 140000 through 177777 are divided into 16 pages which can be independently mapped into anywhere in the Xbus address space. Each page is 1024 8-bit bytes, or 512 16-bit words, or 256 32-bit words, in length; this is the same as the LM-2 page size.

Each 32-bit Xbus location occupies four Unibus byte addresses. It takes two 16-bit Unibus cycles to read or write an Xbus location. 16 buffers (one for each page), each 16 bits long, are provided to hold the data between the two Unibus cycles. As long as each page is only in use by a single Unibus bus-master, so that no other device messes up the contents of the buffer, you can use two successive Unibus cycles to access an Xbus location. To read an Xbus location, right read the lower Unibus address, which maps to the low half of the Xbus word; then read the upper Unibus address, which maps to the high half of the Xbus address. The second Unibus cycle will actually read the contents of the buffer, which was loaded with the high half of the Xbus word during the first Unibus cycle. To write an Xbus location, first write the lower Unibus address, which maps to the low half of the Xbus word; then write the upper Unibus address, which maps to the high half of the Xbus address. The second Unibus cycle will cause an Xbus write cycle that will write both halves into the Xbus. Furthermore, if you use one of the high eight mapped pages, and *write-through mode* is enabled, then the first Unibus cycle will write to the Xbus as well, writing undefined bits in the high half of the Xbus location. Write-through mode is sometimes useful for DMA devices that may write an odd number of 16-bit words. It is controlled by the 200 bit (bit 7) of Unibus location 766044 (the Error Status register in the Bus Interface); this bit can be read and written.

The map is controlled by 16 mapping registers, located in Unibus addresses 766140 through 766176. These are initialized to random contents when power is applied to the LM-2. Their layout is as follows:

100000 (Bit 15)

Map-valid bit. If this is zero, this mapping register is not set up. Any attempt to access the corresponding page will not respond to the Unibus; NXM (Non-Existent

Memory) timeout will occur and an Error Status bit will be set.

40000 (Bit 14) Write-permit bit. If this is zero, the corresponding page is "read-only". Any attempt to write to the page will not respond to the Unibus; NXM (Non-Existent Memory) timeout will occur and an Error Status bit will be set.

37777 (Bits 13-0)
Xbus page number. These bits are concatenated with bits 9-2 of the Unibus address to produce the mapped 22-bit Xbus address.

The three highest mapped pages are reserved for use by LM-2 diagnostic hardware and software; you should not use these three pages.

1.4 Input/Output Board

The Input/Output Board (IOB) contains a variety of peripheral devices that are addressed using the Unibus. This board is a standard part of the LM-2. It is plugged into slot 2 in the I/O/Memory card cage, and uses up slot 3 because it is a wire-wrap board. It responsds to locations 764100 through 764176; none of those locations should be used for anything else.

The following devices are part of the IOB:

General Purpose I/O Port
A 16-bit parallel bi-directional general purpose port. There is no Symbolics-supplied software for this device; user programs simply access it using `%unibus-read` and `%unibus-write`. There is a 16-bit register that can be written at Unibus location 764126, whose outputs appear on lines on the J05, J07, and J08 connectors on the IOB. There are other lines on these connectors that can be read from Unibus location 764126. Some lines appear on more than one of these connectors. Connector J05 is convenient for attaching a bi-directional data path of up to ten bits to the IOB; pins J05-1 through J05-10 are input bits 0 through 9, and pins J05-11 through J05-20 are output bits 0 through 9, respectively. Connector J07 is convenient for attaching a full 16-bit input device; pins J07-1 through J07-16 are connected to input bits 0 through 15, and J07-17 through J07-20 are connected to output bits 0 through 3, respectively. Connector J08 is convenient for attaching a full 16-bit output device; pins J08-1 through J08-16 are connected to output bits 0 through 15, and J08-17 through J08-20 are connected to input bits 0 through 3, respectively.

Serial I/O Port A serial general purpose port, capable of synchronous or asynchronous serial data transmission. The hardware and software for this device are sufficiently complex to warrant a separate document; they are described in detail in the *LM-2 Serial I/O* document. The Serial I/O Port occupies Unibus addresses 764160 through 764166, and its interrupt vector number is 264.

Interval Timer A 16-bit register that counts up by one every sixteen microseconds and generates a Unibus interrupt when it reaches zero. Currently, no software uses this device. You can load the timer by writing Unibus location 764124 with `%unibus-write`, but to handle the Unibus interrupt you must alter the microcode. The interrupt vector number is 274.

Microsecond Clock
A 32-bit register that counts up by one every microsecond. Its value can be accessed from software using the functions `time:microsecond-time` and `time:fixnum-microsecond-time`, which work by reading the low 16 bits from

Unibus location 764120 and then reading the high 16 bits from Unibus location 764122 (in that order).

60-Hz Clock — A 16-bit register that counts up by one every sixtieth of a second. This clock is driven by the AC power line, and so its short-term accuracy is poor but its long-term stability is very good. Currently, no software uses this device. You can read its value by reading Unibus location 764124 with `%unibus-read`. This clock is not synchronized, so you have to read it repeatedly until you get the same value twice in a row, or else you may get invalid values by reading the clock while it counting.

Keyboard — The keyboard on the console. The Lisp Machine system software interprets all input from this device; you should *not* use it directly. The keyboard data is encoded as a 32-bit word, which is read by first reading the high part from Unibus location 764102, and then reading the low part from Unibus location 764100, in that order. The encoding into 32 bits would take a long time to describe and should never be seen by users, so it is not documented here. The interrupt vector number is 260.

Mouse — The mouse on the console. The Lisp Machine system software interprets all input from this device; you should *not* use it directly. The X-position of the mouse as a relative 16-bit number can be read from Unibus location 764106, and the Y-position and the buttons from 764104. The mouse can be enabled to interrupt, using vector number 260 (the same as the keyboard), when its state changes. The software currently does not use thie feature; instead, the mouse is polled 60 times per second.

Speaker — The speaker inside the keyboard. There is a one-bit register whose value is amplified and attached to a small loudspeaker, to allow the console to produce audible beeps. The most useful way to access this device is with the `beep` function (see *The Lisp Machine Manual*), but you can access it directly if you want: reading Unibus location 764110 inverts the state of the bit, causing a click, or call the microcode primitive `sys:%beep` directly.

Chaosnet — The Chaosnet is a local computer network. The hardware and software for this device are sufficiently complex to warrant a separate document; they are described in detail in the *Chaosnet* document. The interface occupies Unibus addresses 764140 through 764152, and the interrupt vector number is 270. The IOB contains two DIP switches, which are used to set the Chaosnet interface's network address. The subnet number is controlled by the switch in location D10, and the host number within the subnet is controlled by the switch in location D12. The individual switches in those locations are numbered 1 through 8; the one numbered 1 is the least-significant bit, and the one numbered 8 is the most significant bit. (In some cases there may be 10 switches rather than 8; in that case switches 2 through 9 are the active ones.) One of the two directions is labelled "ON"; putting a switch into this direction corresponds to a *zero* bit in the subnet/host number (this is the reverse of what you might think). The address, with the subnet number in the high 8-bit byte and the host number in the low 8-bit byte, can be read from Unibus location 764142.

The following table summarizes the locations of the Unibus used by IOB devices. If there is no description of what happens when you write the location, then writing the location either does nothing or is the same as reading.

764100 — Read the low part of the encoded keyboard data.

764102 Read the high part of the encoded keyboard data.

764104 Read the Y-position of the mouse.

764106 Read the X-position of the mouse.

764110 Reading this location clicks the audio output device.

764120 Read the low part of the microsecond clock.

764122 Read the high part of the microsecond clock.

764124 Read the 60-Hz Clock or write the Interval Timer.

764126 Read or write the General Purpose I/O Port.

764140 Read or write the Chaosnet Control/Status Register.

764142 Read the Chaosnet My Address register, or write the Chaosnet Write Buffer.

764144 Read the Chaosnet Read Buffer.

764146 Read the Chaosnet Bit Count.

764152 Reading this location begins transmission of a packet.

764160 Read the receiver holding register, or write the transmitter holding register.

764162 Read the status register, or write the SYN1/SYN2/DLE registers.

764164 Read or write mode registers 1 and 2.

764166 Read or write the command register.

Other addresses in the range 764100-764176 are undefined, and may be unused or may be copies of some of the functions listed above.

The following Unibus locations are also used, by the BUSINT itself. The Xbus-to-Unibus map is described earlier in this document; the rest of these locations are described in the *CADR* document.

140000-177777
These addresses are mapped to the Xbus under control of the mapping registers, as described above.

766000-766036
SPY bus (for hardware diagnosis).

764040 Read and write interrupt status.

764042 Write other interrupt status bits.

764044 Read or reset error status bits; read or write "write-through mode".

766100 Read or write debuggee Unibus location.

764104 Read debuggee status.

766110 Write modifier bits.

766114 Write debuggee Unibus address.

766140-766176
Unibus-to-Xbus mapping registers.

The following Unibus interrupt interrupt vector numbers are used by IOB devices:

260 The Keyboard and Mouse.

264 The Serial I/O Port.

270 The Chaosnet.

274 The Interval Timer.

The following connectors of the IOB are used:

J01 The Chaosnet transceiver.

J03 The console, for the keyboard and mouse. The signal to the TV also passes through here.

J05, J07, and J08
The General Purpose I/O Port. See above for details.

J09 The Serial I/O Port. See the *LM-2 Serial I/O* document for details.