Tektronix®

COMMITTED TO EXCELLENCE

8001/8002A

μPROCESSOR LAB

SERVICE

(For #B032000 and up)

INSTRUCTION MANUAL

Tektronix®
COMMITTED TO EXCELLENCE

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

8001/8002A

μPROCESSOR LAB

SERVICE

(For #B032000 and up)

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

Serial Number _____

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WARRANTY

The 8001/8002A μProcessor Lab System and options, excluding customer supplied equipment, is warranted against defective materials and workmanship, under normal use, for a period of ninety (90) days from date of shipment. CRTs found to be defective after the ninety (90) day period and up to twelve (12) months from date of shipment will be exchanged at no charge for the material. Tektronix will repair or replace, at its option, those System components which Tektronix determines to be defective within the warranty period.

In addition, in those areas where Tektronix has service centers available for this system, on-site warranty repair is provided at no charge during the first ninety (90) days from date of shipment.

Tektronix shall be under no obligation to furnish warranty service if:

a. Attempts to install, repair, or service the equipment are made by personnel other then Tektronix service representatives.

b. Modifications are made to the hardware or software by personnel other than Tektronix service representatives.

c. Damage results from connecting the 8001/8002A μProcessor Lab System to incompatible equipment.

There is no implied warranty for fitness of purpose. Tektronix is not liable for consequential damages.

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DOCUMENTATION OVERVIEW

The 8001/8002A μProcessor Lab support documentation consists of two groups of manuals: user's manuals and service manuals. User's manuals explain the procedures required to operate the 8001/8002A μProcessor Lab system and its peripheral devices. They are identified by their gray covers and are a standard part of the system package.

Service manuals provide the information necessary to perform system testing and repair. Service manuals are identified by their blue covers and may be purchased as optional accessories.

The following manuals contain service information for the 8001/8002A μProcessor Lab System:

8001/8002A μProcessor Lab Service Manual

8001/8002A μProcessor Lab Installation Guide

8002A μProcessor Lab Flexible Disc Unit Service Manual (optional)

118-0195-00 Flexible Disc Drive Service Manual (optional)

Service manuals for
8001/8002A μProcessor Lab Emulator Processors (optional)

Service manuals for
8001/8002A μProcessor Lab optional modules (optional)

Service manuals for
8001/8002A μProcessor Lab peripheral equipment (optional)

PREFACE

ABOUT THIS MANUAL

This manual is organized into 12 text sections and a schematic diagram section.

Text sections 1 and 2 provide a general overview of the 8001 and 8002A μProcessor Labs. Section 1 also contains a brief synopsis of each standard module's operation within a μProcessor Lab. The end of Section 1 contains an example of module interaction during a software TRACE operation.

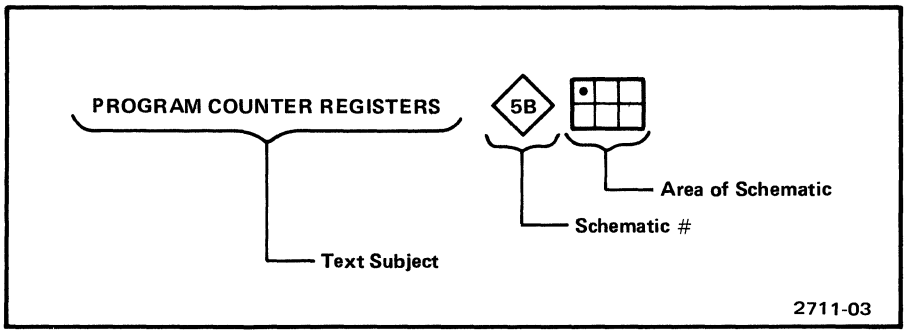
Sections 3 through 10 describe each module's theory of operation down to the logical block level. Each section is keyed to schematics located at the rear of this manual.

Some system troubleshooting information is included in Section 11; however, this manual is not presented as a comprehensive troubleshooting guide.

MANUAL CONVENTIONS

TEXT AND SCHEMATICS

We have provided guideposts to help you find the schematic diagrams relating text in this manual. Headings in the text tell you on which schematic the circuitry under discussion can be found. The following example shows a text heading.



The example tells you three things:

- The text will discuss program counter registers.
- The program counter registers can be found on schematic 5B.
- The grid shows the general area of schematic 5B that contains the program counter registers.

Using the example, you can tell that the program counter registers are located on the upper left corner of schematic 5B.

SLASHED ZEROS (Ø)

Throughout this manual, zeros are slashed (Ø) only where needed for clarity.

HEXADECIMAL NOTATION

All addresses are represented in this manual by hexadecimal numbers (i.e., 40AC). Subscripts denoting base sixteen are not used.

UNITS COVERED IN THIS MANUAL

This manual presents service information on the mainframe and standard system modules of the 8001 and 8002A μProcessor Lab systems. The standard modules are:

—System Processor module
—System and Program Memory modules
—System Communications module
—Assembler Processor module
—Debug and Front Panel I/O module

Optional system modules and peripherals have separate service manuals.

CHANGE INFORMATION

Change information is located in the back of this manual in the CHANGE section. Change information should be entered into the body of the manual when the manual is received.

REVISION HISTORY

Revision history information is included in the text and diagrams as they are revised and reprinted. Original manual pages have an "@" symbol at the bottom of the page. Existing pages of a manual when revised, have a revision code and date in place of the "@" symbol. New pages added to a section, whether they contain old, new, or revised information, will have the "@" symbol.

INSTALLATION INFORMATION

A minimum of installation material is given in this manual. Refer to the 8001/8002A μProcessor Lab Installation Guide for information regarding the installation of 8001/8002A μProcessor Lab modules and options. Module configuration information is also given in the Installation Guide.

OPTIONS

Options for the 8001/8002A μProcessor Lab system are documented by individual manuals. See the Tektronix Products catalog or contact your local Tektronix Field Office or representative for a list of options.

RELATED MATERIAL AND TEST EQUIPMENT

To make the most effective use of material in this manual, the service facility should have access to the following documents and equipment:

1. Service manuals and user's manuals for all options and peripherals installed in the system.
2. A Signetics 2650 technical manual, for interpreting System Processor machine code.
3. An 8001/8002A Maintenance Front Panel.
4. Logic analyzer—TEKTRONIX 7000 series mainframe with a 7D01F plug-in.
5. Technical data sheets for devices used in this instrument. These data sheets are best obtained from the local distributor or direct from the device manufacturer. The Replaceable Electrical Parts list at the rear of this manual provides a reference to the manufacturer, and the manufacturer's part number for each device used in this instrument.

TABLE OF CONTENTS

TABLE OF CONTENTS (cont)

TABLE OF CONTENTS (cont)

TABLE OF CONTENTS (cont)

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TABLE OF CONTENTS (cont)

TABLE OF CONTENTS (cont)

TABLE OF CONTENTS (cont)

TABLE OF CONTENTS (cont)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (cont)

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LIST OF TABLES

OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

In This Manual

This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment

DANGER — High voltage.

Protective ground (earth) terminal.

ATTENTION — refer to manual.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the power input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.
Use only a power cord that is in good condition.

Refer cord and connector changes to qualified service personnel.

Use the Proper Fuse

To avoid fire hazard, use only the fuse specified in the parts list for your product, and which is identical in type, voltage rating, and current rating.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an atmosphere of explosive gases unless it has been specifically certified for such operation.

Do Not Remove Covers or Panels

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

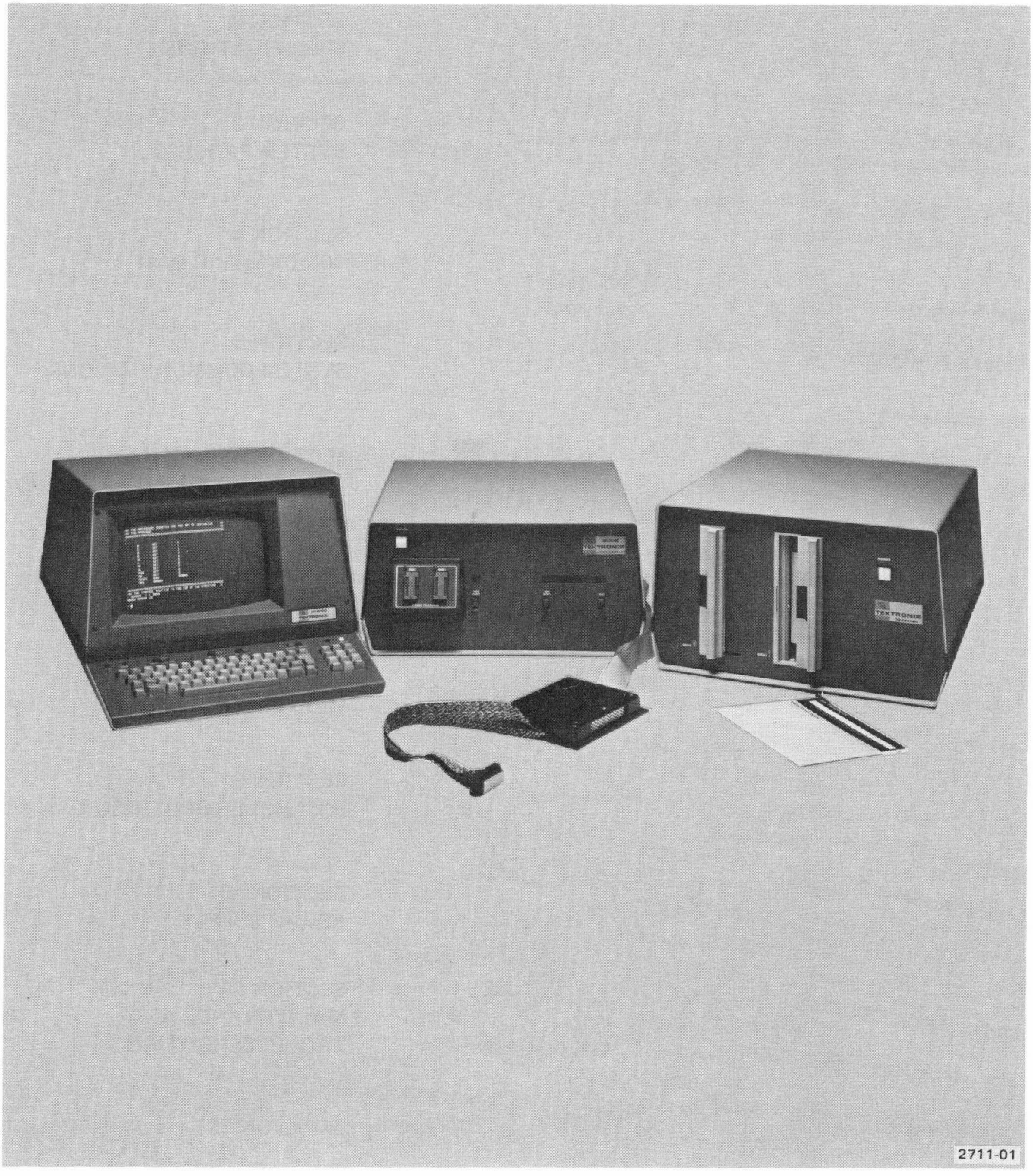

Fig. 1-1. The 8002A μProcessor Lab with Optional CT8100 CRT Terminal and Prototype Control Probe.

8001/8002A
SERVICE MANUAL
SECTION INDEX

Section 1

SYSTEM OVERVIEW

This section gives a brief introduction to the 8001 and 8002A μProcessor Lab systems.

The 8002A μProcessor Lab system is a complete, stand-alone, hardware and software development system for microprocessor-based design projects.

The 8001 μProcessor Lab system is intended primarily for software testing, hardware development, and integration of both software and hardware. Software to be tested on the 8001 μProcessor Lab is usually developed on a host computer.

Both the 8001 and 8002A μProcessor labs use a common mainframe. However, the 8002A μProcessor Lab also includes a Flexible Disc Unit for mass storage. A typical 8002A μProcessor Lab system is shown in Fig. 1-1.

In this section, the 8002A μProcessor Lab is discussed first, followed by the 8001 μProcessor Lab. The functions and operations of each module in the two systems are discussed in the last portion of this section.

8002A μPROCESSOR LAB SYSTEM

The 8002A μProcessor Lab system provides tools to edit, assemble, and link together software programs for a wide variety of microprocessor and microcomputer devices. Additionally, through the use of selected emulator processor modules, the 8002A μProcessor Lab system can execute the developed software.

With an optional prototype control probe added, the software routine may be run on a prototype system developed by the user.

8002A μProcessor Lab System Hardware

A complete 8002A μProcessor Lab system consists of an 8002A μProcessor Lab mainframe with its standard complement of plug-in modules, a Flexible Disc Unit, and some form of operator console or a host computer.

The internal architecture of the 8002A μProcessor Lab centers around a system microprocessor. This System Processor uses other microprocessors to perform software and hardware support functions. The system contains 16K bytes of RAM system memory, and 32K bytes (expandable to 64K bytes) of RAM program memory. The system also supports two flexible disc drives, with approximately 315K bytes of storage on each disc.

A block diagram of a typical 8002A μProcessor Lab system is shown in Fig. 1-2. The system contains three microprocessors: the System Processor, the Assembler Processor, and the selected emulator processor. Each microprocessor resides on a separate plug-in module in the system mainframe. Other system modules are the System Communications module, the Debug and Front Panel I/O module, System and Program Memory modules, and the optional modules for the Real-Time Prototype Analyzer and PROM programmers. Modules are connected to each other through a common system bus. Figure 1-2 will be referred to as each individual module is discussed. The Flexible Disc Unit is housed in a separate cabinet. It communicates with other system components through the System Processor.

8002A μProcessor Lab System Software

The operating system for the 8002A μProcessor Lab is the TEKTRONIX Disc Operating System (TEKDOS). TEKDOS resides in flexible disc storage. A ROM-based bootstrap routine loads the operating system into the 8002A μProcessor Lab System Memory immediately after power-on, or upon command from the front panel SYSTEM RESTART switch.

TEKDOS provides file management and utility programs for the 8002A μProcessor Lab. All the major software features—assemblers, linkers, text editors, etc.—operate under the supervision of TEKDOS. Refer to the 8002A μProcessor Lab System User's Manual for a complete discussion of TEKDOS software.

8001 μPROCESSOR LAB SYSTEM

8001 μProcessor Lab System Hardware

The 8001 μProcessor Lab system offers all the hardware development capabilities of the 8002A μProcessor Lab system, but not all the software features. The 8001 μProcessor Lab uses the same mainframe as the 8002A, and all the standard modules, with three exceptions. The 8001 μProcessor Lab contains only 16K bytes of Program memory rather than 32K as in the 8002A; the Assembler Processor module is not used, and System Memory is a ROM-based memory containing the TEKOPS operating system, rather than disc-based as in the 8002A. The 8001 μProcessor Lab does not use the Flexible Disc Unit.

8001 μProcessor Lab Operating System

The operating system for the 8001 μProcessor Lab is the TEKTRONIX Operating System (TEKOPS). TEKOPS resides in ROM on the 8001 μProcessor Lab System Memory module. For a discussion of TEKOPS software features, refer to the 8001 μProcessor Lab System User's Manual.

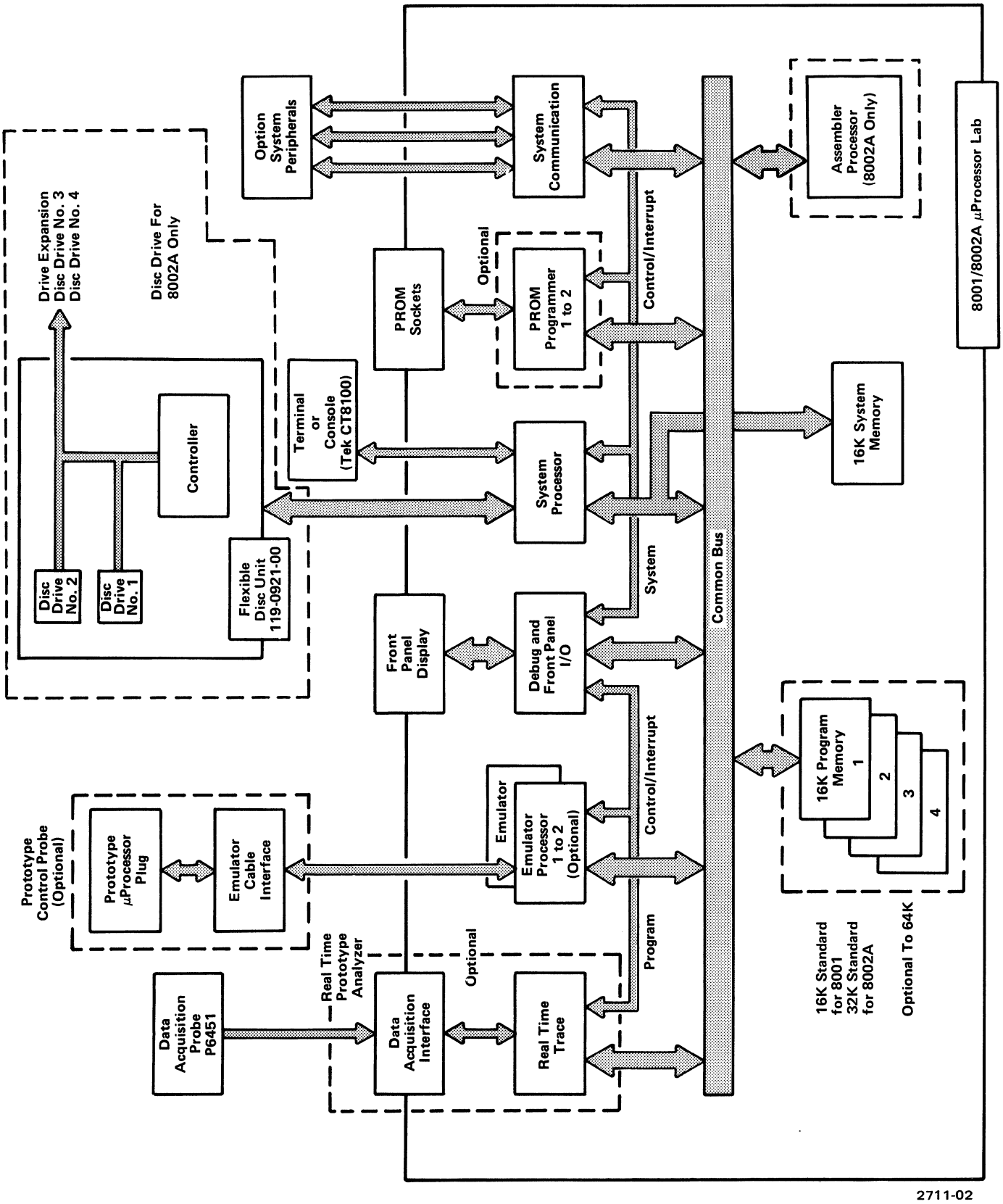

Fig. 1-2. Functional Block Diagram of the 8001/8002A μProcessor Lab System.

MODULE OVERVIEW

Complex systems like the 8001 and 8002A μProcessor Labs depend on communication between the various modules that make up the system. The following pages explain the interrelationships between the various modules within the μProcessor Lab systems. Each module is discussed first in terms of its functions, then in terms of its relationship with other modules. Refer to Fig. 1-2, the System Block Diagram, while reading this section.

In the following text, those functions or operations associated with the 8002A μProcessor Lab only are noted with an asterisk (*).

System Bus

As can be seen in Fig. 1-2, the μProcessor Lab is a bus-oriented computer. All the modules within the mainframe communicate to one another via the system bus. The bus contains 16 data lines, 16 address lines, and two groups of control lines. Some of the control lines are dedicated to the System Processor side of the mainframe, others are dedicated to the emulator processor side, and certain control lines are common to both sides. A schematic of the μProcessor Lab bus is located at the rear of this manual. The schematic provides a clear view of this separation within the bus. Details of each bus line are given in Appendix A.

System Processor Module

The μProcessor Lab system may be viewed as two systems, one the master (or controller) and the other the slave. In this arrangement, the System Processor serves as the master. The System Processor has overall control of the μProcessor Lab system. The System Processor provides supervisory functions in both hardware and software. Figure 1-2 shows the relationship of the System Processor to the rest of the μProcessor Lab. A simplified block diagram of the System Processor is shown in Fig. 1-3. The block diagram shows the major blocks of logic that will be discussed here.

Software Functions

Those software functions controlled by the System Processor include:

System Input/Output—directs all I/O activity for the system peripherals, such as the flexible disc, the console, and the line printer.

File Management*—organizes, stores, and retrieves user programs and system programs from the disc drives.

Text Editing*—executes the text editor program and maintains text files on the Flexible Disc Unit.

Debugging—executes the debug program and controls the emulator processor through separate debug hardware.

System Utilities—performs all system utility functions, such as processing messages between system peripheral devices.

PROM Programming—monitors and controls all PROM activity.

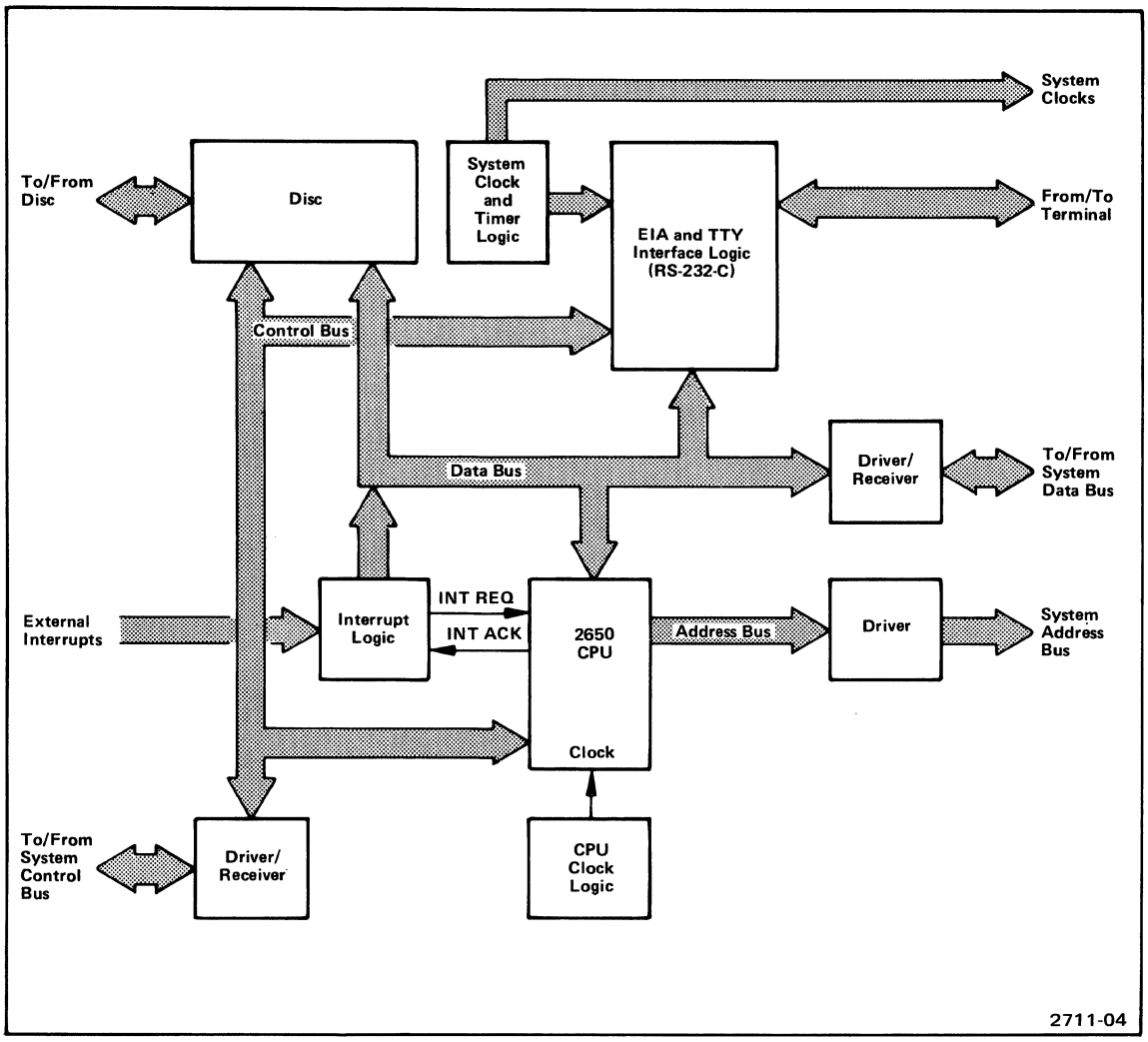

Fig. 1-3. 8001/8002A μProcessor Lab System Processor Block Diagram.

The System Processor provides overall control of the μProcessor Lab. This block diagram shows the 2650 microprocessor used in the System Processor module, and the other logic that controls the disc drive unit, RS-232-C interfaces, and the remainder of the μProcessor Lab.

CONTROL BYTES

HARDWARE FUNCTIONS

In order to perform its software functions, the System Processor must be able to communicate with other modules and with peripheral equipment. The System Processor maintains control of the other modules in the system by issuing control or command bytes to each module, as required. (This is accomplished in part by the Driver/Receiver block (Fig. 1-3), which interfaces the System Processor internal control lines with the system control lines.) The control byte contains the information needed by a module to perform a required function. For example, during debugging routines, the System Processor sends a control byte to inform the Debug module that a debug operation is being performed. The command byte issued to the Debug module contains information such as the beginning and ending software trace addresses (which the Debug module will store in registers) and the breakpoint addresses.

RS-232-C I/O PORTS

The System Processor module also has two RS-232-C compatible I/O ports (refer to Fig. 1-3). These I/O ports are used in communicating with the system terminal and printer. Using the system terminal as an example, when the user entered a character on the terminal, the character is converted to the proper code by the terminal. The character is then sent to the System Processor by way of the I/O port, and is acted upon by the System Processor. If the System Processor is performing another task, it can be interrupted by the terminal (or by any other module in the system, for that matter), and the interrupt-requesting device will be serviced.

FLEXIBLE DISC INTERFACE

Another function of the System Processor is to control the operation of, and transfer information to and from the Flexible Disc Unit* (Disc Interface block, Fig. 1-3). When the system is first started, the System Processor goes to the address of the boot PROM and begins execution of the bootstrap routine. The routine forces the System Processor to load TEKDOS from the Disc Unit into the System Memory module. Once TEKDOS is loaded into memory, the System Processor then goes to TEKDOS and begins an initialization routine located there.

FILE MANAGEMENT

Along with controlling the Flexible Disc Unit, the System Processor must also be able to transfer data files from Program Memory onto disc. The user may have developed a program and stored it within Program Memory. The System Processor can access Program Memory, read the information stored there, and transfer it to disc storage.

INTERRUPT LOGIC

The System Processor module is an interrupt-driven processor. That is, for any other module or exteenal equipment to obtain the services of the System Processor, it must generate an interrupt request. The requests are received by the Interrupt Logic block shown in Fig. 1-3. The System Processor can handle 16 different requests. These include such interrupts as a printer requesting another line of data, or issuing data to a PROM Programmer module during its activities. When a device or module issues an interrupt request, the System Processor responds with an interrupt acknowledge. This acknowledge tells the requesting device that it has the System Processor's complete attention. The System Processor module then waits to perform whatever action is required of it.

These examples do not list all the functions of the System Processor module, but do indicate some of the responsibilities of the module.

Emulator Processor Module

The emulator processor is discussed here to show its relative importance in system operations. Recall that the System Processor module was described as the master processor in a multi-processor system. In such a system, the next most important processor is the emulator processor. Figure 1-4 shows a simple block diagram of an emulator processor. Figure 1-2 shows the relationship of the emulator processor to the rest of the system.

IMPORTANCE OF EMULATOR PROCESSOR

The emulator processor is one of the main reasons for using a μProcessor Lab in microprocessor-based development. The emulator processor is required to run software designed for a specific microprocessor or microcomputer device. Without an emulator processor, both software and hardware development would be impractical, if not impossible.

RESEMBLANCE TO SYSTEM PROCESSOR

The emulator processor bears a considerable resemblance to the System Processor module. Both are microprocessor-based. Both are connected to the motherboard bus of the μProcessor Lab. Both have dedicated memories. (The exception here is that the System Processor can access both System Memory and Program Memory, while the emulator processor can access only Program Memory.) The emulator processor can (in a limited fashion) access prototype circuits with the use of its prototype control probe. Figure 1-4 illustrates the use of the prototype control probe in transferring information to a prototype instrument.

FUNCTIONS OF EMULATOR PROCESSOR

The emulator processor serves two purposes in the μProcessor Lab. First, it has the ability to run a program written for a specific microprocessor or microcomputer. With the help of the Debug and Front Panel I/O module and the System Processor module, such a program can be checked for run-time errors and program logic errors. Second, by adding a prototype control probe to the emulator processor, a prototype circuit under development can be debugged and stepped through the final design stages to completion.

EMULATION FUNCTION

The emulator processor emulates the operation of a target microprocessor. The target microprocessor is the device that will be used in the final version of a prototype microprocessor-based system. The emulator processor module reacts to software in the same way as the target microprocessor, but at the same time allows software debugging.

PROTOTYPE CONTROL PROBE

The prototype control probe carries this debugging ability one step further. The prototype control probe allows the emulator processor to be connected directly to the socket in the prototype system where the target microprocessor or microcomputer would normally be. Figure 1-4 shows this connection. In this way the user can exercise the prototype I/O, clock, and memory, and still maintain control of all operations within the 8001 or 8002A μProcessor Lab.

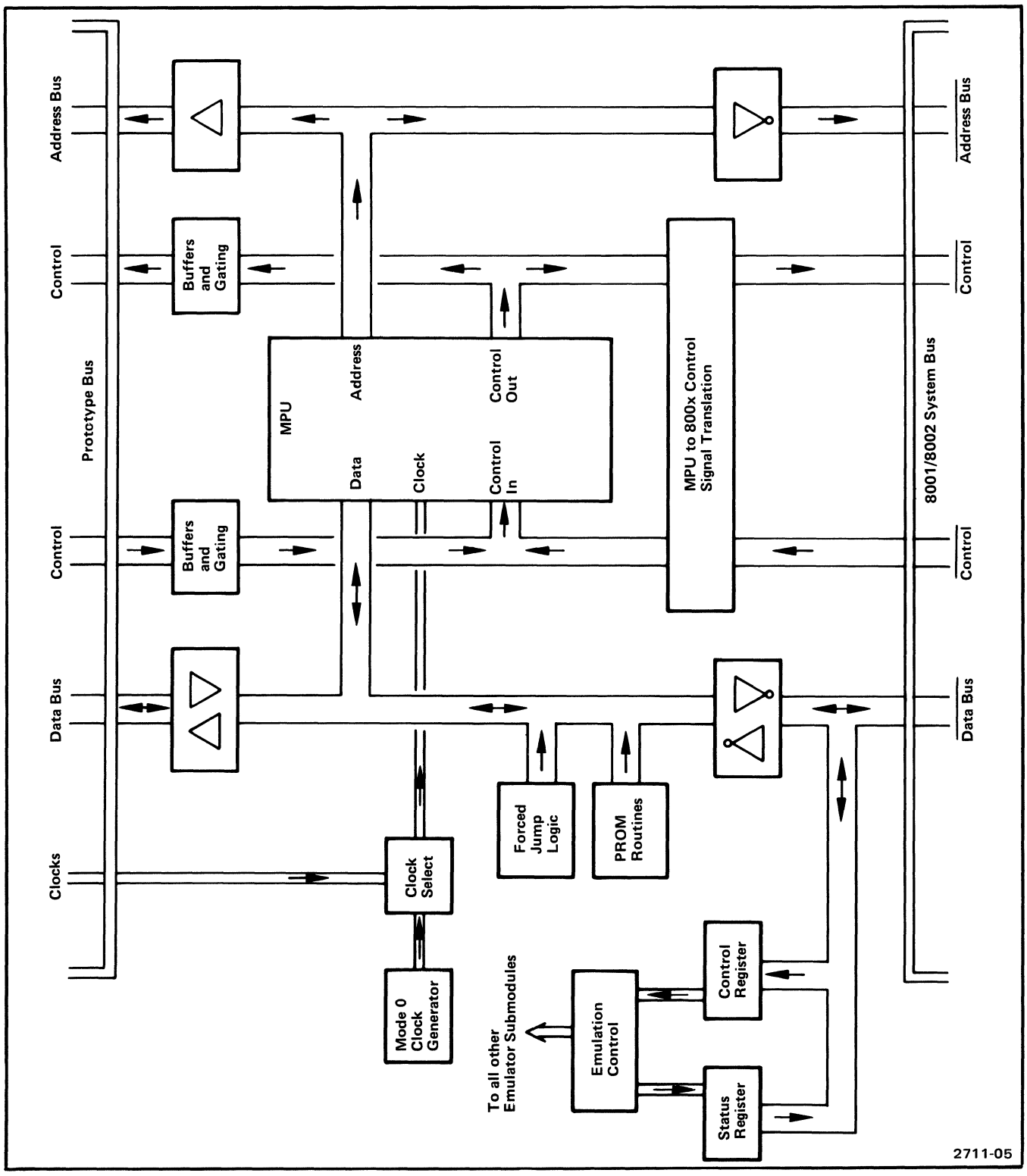

Fig. 1-4. 8001/8002A μProcessor Lab Emulator Processor Block Diagram.

The emulator processor is a tool used to develop both hardware and software. This block diagram illustrates the general blocks of logic used in most emulator processors. The emulating microprocessor is usually a refined version of the target microprocessor to be used in a prototype system. The emulator processor uses a PROM to hold a dump and restore routine. This PROM, used in conjunction with the forced jump logic, allows the Debug and Front Panel I/O module to direct the emulator processor during debugging operations.

Emulation Modes

EMULATION MODE 0

The emulator processor may operate in one of three modes. In emulation mode 0, all activity takes place within the μProcessor Lab. Mode 0 allows the emulator processor to execute a program stored in Program Memory. All software debugging features are available in this mode.

EMULATION MODE 1

In emulation mode 1, the emulator processor is used in conjunction with the optional prototype control probe. The prototype control probe is connected to a prototype system. In this mode the program is still executed from Program Memory; however, the I/O and clock functions are furnished by the prototype system. Another capability of emulation mode 1 is that memory locations can be "mapped" between the Program Memory module or the prototype memory. Memory mapping allows different parts of a program to be stored in either Program Memory or in the prototype's memory, and executed as though the program resided in a single memory.

MODE 1 EXAMPLE

For example, suppose that a program has been developed and stored in PROM devices on the prototype system. After a trial run through the program, the user discovers that an error exists in a subroutine. That subroutine can then be written from the prototype system into Program Memory. By placing the subroutine into Program Memory, the user can alter the routine or set breakpoints; any of the debugging capabilities of the μProcessor Lab may be used on the subroutine.

The beginning and ending addresses of the subroutine are placed into a memory mapping RAM located on the System Communications module. Then, when the user begins program execution out of prototype memory, execution will proceed until the beginning address of the mapped subroutine is reached. At that time, execution switches to the debugged subroutine in Program Memory. At the end of the subroutine, execution switches back to prototype memory.

EMULATION MODE 2

The third emulation mode is mode 2. Emulation mode 2 allows all operations to be run by the prototype system, while allowing the user to monitor and debug those operations with the μProcessor Lab. The program is executed entirely out of prototype memory. Prototype I/O and clock are also exercised.

CONTROL BY SYSTEM PROCESSOR

During all the operations of the emulator processor (only a few of which are listed here), control is maintained by the System Processor module. Recall that the System Processor module issues command or control bytes to all other modules in the μProcessor Lab. The emulator processor receives a control byte each time it is reset or the emulation mode is changed. The control byte contains the emulation mode in binary form, as specified by the System Processor. The control byte from the System Processor also contains other information necessary to the operation of the emulator processor. The Control Byte register is shown in Fig. 1-4.

TRACE OPERATION

During some debugging operations (like a TRACE operation) the emulator processor is required to single-step through the software program. The TRACE operation works (in general terms) in the following manner:

The system user enters a command that instructs the System Processor to initiate a TRACE operation. TRACE allows certain information to be stored or displayed during each step of a routine. The System Processor issues a new control byte to inform the emulator processor that a debugging routine is to begin. One bit of the control byte is set to indicate a debugging operation. The System Processor loads the starting and stopping addresses of the TRACE operation into registers on the Debug and Front Panel I/O module (discussed later in this section). The emulator processor then begins execution.

DUMP EMULATOR REGISTERS

The emulator processor fetches the first instruction from Program Memory. When execution of that instruction is complete, the emulator processor is halted by the Debug module. The Debug module then forces the emulator processor to execute a forced jump to a register dump routine. This routine, located in PROM on the emulator processor, causes the emulator processor to dump its register contents to a location in Program Memory.

STORE INFORMATION

After the emulator processor dumps its register contents into Program Memory it is paused again. At that time, the Debug module activates the System Processor module. The System Processor module obtains the emulator register values from Program Memory and transfers them to System Memory. The System Processor then outputs the information to the device requested, either to disc storage, a line printer, or a terminal. The System Processor replaces the register information in Program Memory. The Debug module then pauses the System Processor and starts the emulator processor.

RESTORE EMULATOR REGISTERS

The emulator processor is force-jumped to its on-board PROM, which contains a restore routine. The emulator processor reads the location in Program Memory and restores its registers to their original value. The emulator processor then continues to the next instruction. This process is repeated for each instruction within the range set by the user.

Although this is a simplified version of the actual events that take place during TRACE, it illustrates the cooperation required between modules within the μProcessor Lab.

Debug and Front Panel I/O Module

SYSTEM BUS CONTROL

The Debug module is, among other things, the "traffic cop" of the μProcessor Lab. Recall that all modules in the μProcessor Lab share the same address bus, data bus, and part of the control lines. (Refer back to Fig. 1-2.) Bus contention could become a problem without the Debug module. The Debug module insures that only one processor (either the System Processor or the emulator processor) has control of the bus at any time. As its name implies, the Debug module also controls debugging operations and controls the front panel. Figure 1-5 illustrates a block diagram of the Debug and Front Panel I/O module.

DEBUGGING FUNCTIONS

The debugging responsibilities of the Debug module have been explained in part in the discussion of the emulator processor. The Debug module has several registers dedicated to debugging operations. Breakpoint addresses are stored in registers on the Debug module (see Fig. 1-5). The stored addresses are compared to the

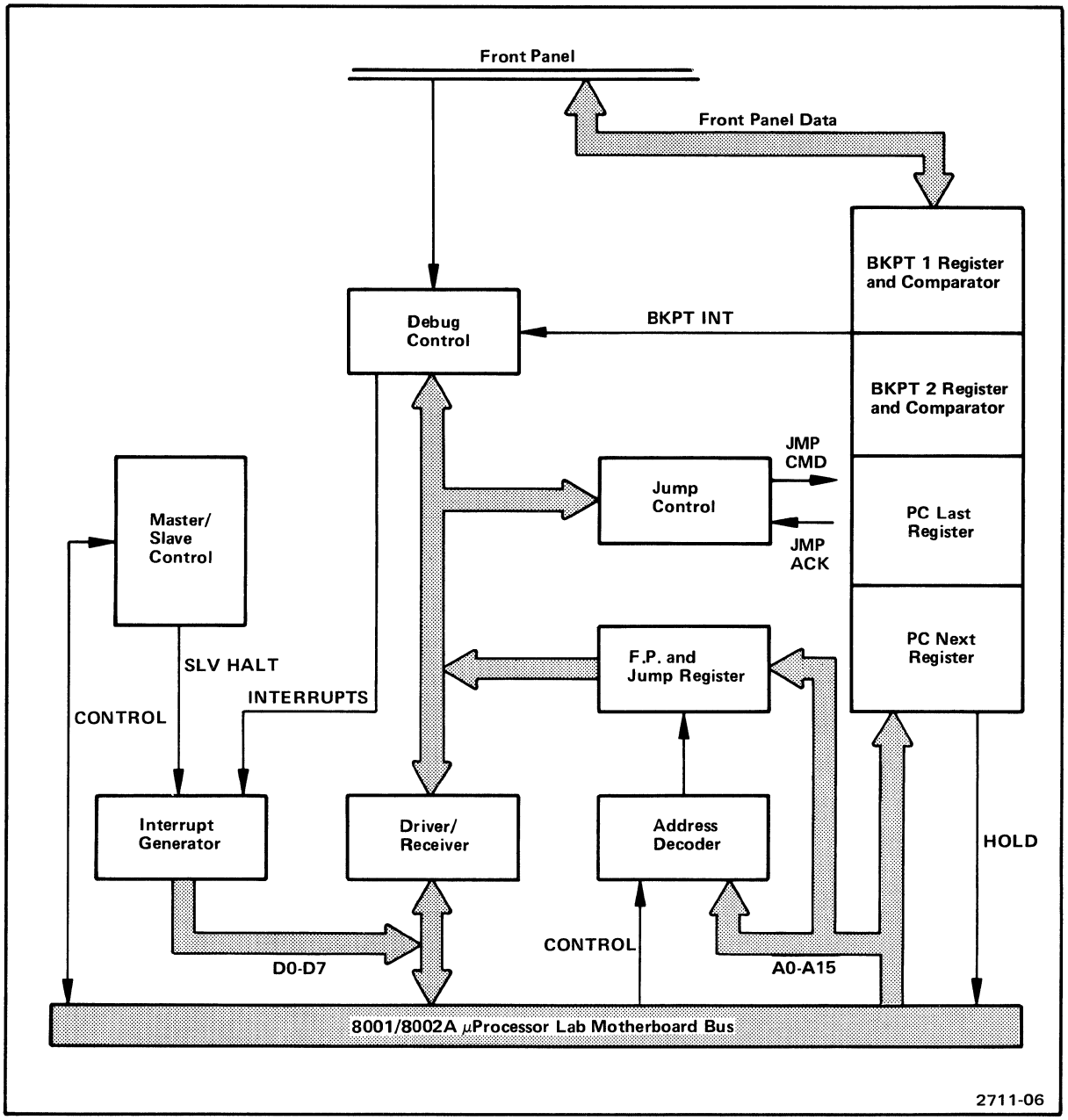

Fig. 1-5. 8001/8002A μProcessor Lab Debug and Front Panel I/O Module Block Diagram.

This module prevents bus contention, controls debugging operations, and provides an interface to the μProcessor Lab front panel. The Debug module contains breakpoint, forced jump, and program counter registers used during debugging operations. The Debug module is under direct control of the System Processor module.

addresses placed on the system address bus by the emulator processor. If the addresses match, the Debug module informs the System Processor. The trace functions of the Debug module were discussed in the emulator processor text.

FRONT PANEL INTERFACE

The Debug module interfaces the front panel (either the standard or Maintenance Front Panel) to the rest of the μProcessor Lab system. This function is shown in Fig. 1-5. The Maintenance Front Panel allows the user complete control of the μProcessor Lab, indicates the states of the address and data buses, and allows debugging operations to be set and exercised without the use of a terminal.

System and Program Memory Modules

8001 SYSTEM MEMORY

The memory modules in the 8001/8002A μProcessor Lab are simple enough in themselves that they will not be discussed in any great detail. Figure 1-2 shows their relationship to the rest of the system. Recall that the software operating system for the 8002A μProcessor Lab (TEKDOS) is stored on disc, and placed in System Memory as required. Since the 8001 μProcessor Lab does not have disc drive capability, the 8001 μProcessor Lab system software (TEKOPS) must reside in the 8001 System Memory module. The 8001 System Memory module is made up of 6K of ROM (containing TEKOPS) and 2K of RAM. An additional 32K of ROM space is available.

MEMORY ACCESS

One other comment about memories: Keep in mind that while the System Processor module can access both System Memory and Program Memory, the emulator processor can access only Program Memory.

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Assembler Processor*

The Assembler Processor module is basically a translator. It translates assembly code into machine code. In very simplified terms, it works as described in the following paragraphs.

LOADING ASSEMBLER SOFTWARE

The system user writes an assembly language program for a specific microprocessor or microcomputer. The program is stored in Program Memory as it is written, and then transferred to disc on the 8002A μProcessor Lab Flexible Disc Unit. Before the user can use the program, it must be translated into machine code to be understood by the emulator processor. To accomplish this translation, the user types ASM on the system terminal. TEKDOS loads the assembler program into System Memory, where it will reside during the entire assembly operation. The System Processor module then loads an assembler table into Program Memory. Each emulator processor has a different assembler table. The assembler table contains the correct machine code for translating assembly language into machine language.

ASSEMBLER OPERATION

After it has loaded the assembler table into Program Memory, the System Processor reads the first line of assembly code from the disc into System Memory. The Assembler Processor reads a command from the first field of the assembly language, and translates the command into machine code for storage in Program Memory. The Assembler Processor then reads and translates a command from the second field. The System Processor then reads the second line of assembly code from disc and the translation takes place again. This action is repeated until the entire file is assembled and stored in Program Memory. At that point, the emulator processor can begin execution of the program.

Remember that this is a simplified explanation of the assembly operation. More information can be obtained by reading the 8002A μProcessor Lab Assembler and Emulator User's Manual that corresponds to your emulator processor.

*8002A only

System Communications Module

A block diagram of the System Communications module is found in Fig. 1-6. The System Communications module gives the μProcessor Lab system the capability to communicate with other computers, or to run a line printer, a terminal, or a paper tape reader/punch. This communication is accomplished with three RS-232 compatible I/O ports. The ports are accessible on the rear panel of the μProcessor Lab. See Fig. 1-2.

SOFTWARE DOWNLOADING

One of the uses of the System Communications module is to download software from another computer system. This feature is particularly useful in the 8001 μProcessor Lab. Software can be developed on an external computer, transferred to the 8001 μProcessor Lab via the System Processor, and stored in Program Memory. Information transfer is accomplished by using the COMM command.

HARDWARE OPERATION DURING DOWNLOADING

Once an information transfer link (such as a modem) is established, the user can enter the COMM command from the system console. The System Processor then writes a command byte to the System Communications module, setting up operating parameters. One of three asynchronous communication devices (ACIA) on the System Communications module is activated, allowing information to be placed on the system data and address buses. The System Processor then writes the information to the Program Memory module. The System Processor also handles protocol for the System Communications module.

MEMORY MAPPING INSTRUCTIONS

A secondary function of the System Communications module is memory mapping. Recall that in emulation mode 1 the emulator processor may selectively execute out of Program Memory or prototype memory. The System Communications module contains a bit map RAM. See Fig. 1-6. The bit map RAM is loaded by the System Processor when the MAP command is used. The bit map defines whether the emulator processor is to work out of Program Memory or prototype memory for each address.

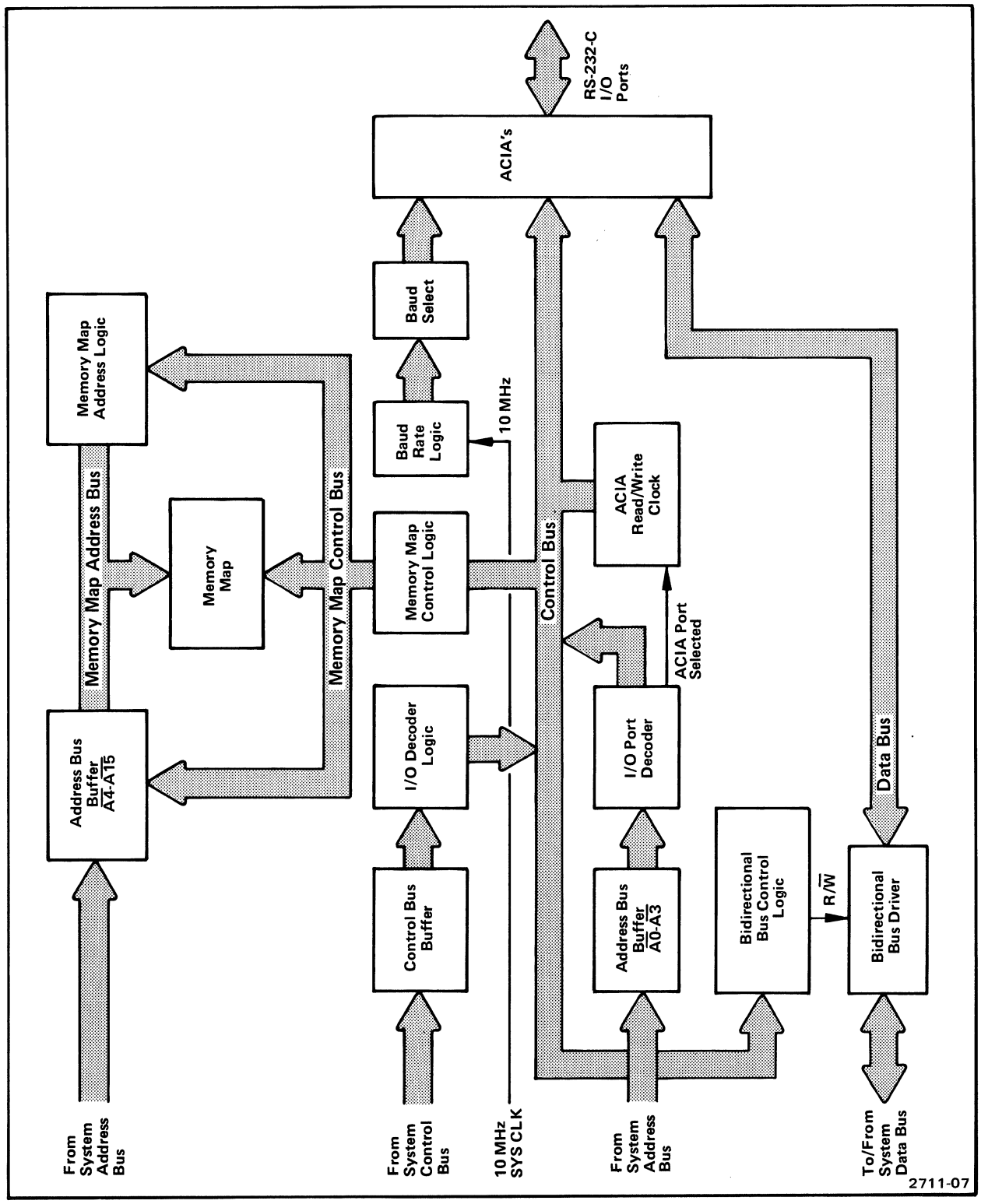

Fig. 1-6. 8001/8002A μProcessor Lab System Communications Module Block Diagram.

The System Communications module provides two services to the μProcessor Lab: communications with external peripherals or a host computer, and memory mapping control for the emulator processor.

SOFTWARE

Both the 8001 and 8002A μProcessor Labs have software operating systems. The 8001 operating system (TEKOPS) is contained in PROM on the 8001 System Memory module. The 8002A operating system (TEKDOS) is disc-based: the operating system software is contained on disc, and portions of it are transferred to RAM memory in the 8002A System Memory module as needed. The major difference between TEKDOS (8002A) and TEKOPS (8001) is that TEKDOS has greater software manipulation capabilities than does TEKOPS. In this discussion, we will describe TEKDOS, keeping in mind that TEKOPS performs many of the same functions, only in a different manner.

TEKDOS is a module, or block, oriented software system. The reason for this is size. The amount of memory that would be required to contain all of TEKDOS is far greater than the 16K bytes available. Therefore, TEKDOS is organized into blocks, or software modules, that can be transferred from disc to System Memory.

When an 8002A μProcessor Lab is booted up, several blocks of software are loaded from disc to System Memory. These blocks are the basic operating system and can be thought of as a system monitor. More information on TEKDOS can be found in the 8002A μProcessor Lab System User's manual.

When TEKDOS is loaded, it takes up all of System Memory, excluding a portion from address 1500H to 1BFFH. Figure 1-7 shows a map of System Memory with TEKDOS loaded.

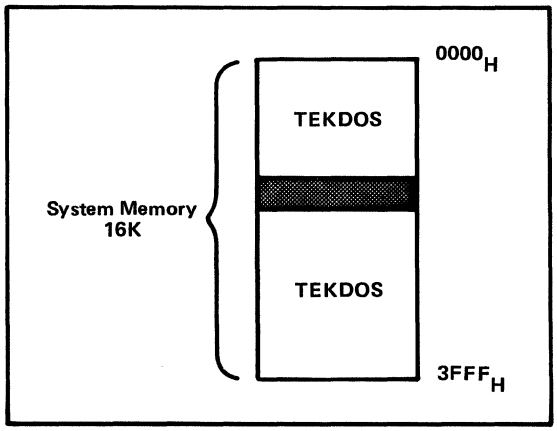

Fig. 1-7. TEKDOS as it appears in 8002A System Memory.

Notice the grey area in Fig. 1-7 near the center of the System Memory address range. This grey area represents that area of System Memory not filled by TEKDOS. This area is called the overlay area. The next few paragraphs will explain the use of the overlay area.

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Overlay Area

Recall that when TEKDOS is loaded, only a portion of TEKDOS is transferred to System Memory. Portions remaining on the disc include:

most of the TEKDOS commands;
all debug commands; and
all special commands, including RTPA and emulator processor commands.

When a command is entered from the terminal, TEKDOS receives the command and looks for the command in a list called the command table. The command table is a list of every valid command for a particular version of TEKDOS. Also within the command table is an internal file name for each command.

Let's suppose that the DEBUG command is entered. TEKDOS receives the command from the terminal, then looks for DEBUG in its command table. The command table tells TEKDOS that DEBUG is a valid command, and gives TEKDOS the internal file name for DEBUG. Since DEBUG is a valid command, TEKDOS goes out to disc, and searches the internal file directory for the internal file name of DEBUG. When the file is located, TEKDOS transfers the file to the overlay area in System Memory. Figure 1-8 shows an expanded view of the overlay area.

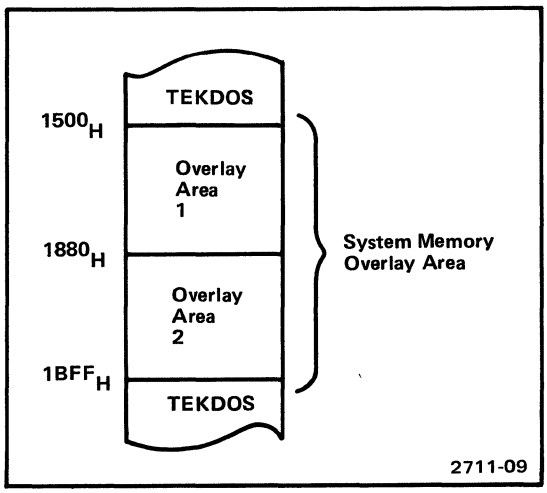

Fig. 1-8. System Memory Overlay Area.

As you can see, the overlay area is divided into two parts. When the internal file containing DEBUG is retrieved from disc, the debug routine, called debug control, is placed into overlay area 1. TEKDOS then turns system control over to this routine. Debug control initializes the system to work in a debug mode, and then returns control to TEKDOS. TEKDOS then waits for the next command from the terminal.

When the next command is a debug command, like TRACE ALL, the same procedure is repeated for the new command. TEKDOS searches its command table, then retrieves the internal file containing TRACE ALL from disc. The program for TRACE ALL is stored in overlay area 2. During all debug operations, the debug control software remains in overlay area 1; the contents of overlay area 2 change with each debug command change.

You should understand that debug commands and operations are not the only software functions that use the overlay areas in System Memory. The 8002A μProcessor Lab System Reference Booklet shows each command that uses an overlay, and the overlay area used. The 8002A μProcessor Lab User's Manual also lists each system command and the overlay areas used.

To summarize, the debug control routine is loaded from disc into overlay area 1 as an overall control element. Then each debug command entered at the terminal is loaded into overlay area 2. Once a specific debug command is loaded, execution of the user program can be started with GO or a similar command. Execution of the program by the emulator processor then falls under control of the debug command in overlay area 2.

What Happens When You Enter TRACE ALL?

Up to this point we have discussed the general hardware capabilities of each module in the 8001/8002A μProcessor Lab. And we have briefly covered the operation of the 8002A μProcessor Lab operating software, TEKDOS. Now, we will examine the operation of the μProcessor Lab as a whole.

The following example describes most of the operations occurring within an 8002A μProcessor Lab when TRACE ALL is entered at the terminal. The TRACE ALL command involves single-step execution of a program contained in Program Memory. At the end of each instruction, the active emulator processor is halted, and its register contents are either stored on disc, or displayed to the user. In this way, the program is "traced", step by step.

In order for this example to be useful, some assumptions must be made. First of all, we assume that you have some knowledge of TEKDOS—its command structure, general operation, etc. For more information concerning TEKDOS, see the 8002A μProcessor Lab System User's Manual. Secondly, this example is built around an operating 8002A μProcessor Lab, with a current TEKDOS disc loaded. We assume that an emulator processor module is plugged into the mainframe of the 8002A.

Because a number of hardware control lines are mentioned in the following text, it may be valuable to study the theory of operation sections located later in this manual.

As a convention, those commands that would be entered by the user are all uppercase and underlined.

Command: LOAD (filename)

Action:

1. The System Processor (under control of TEKDOS) searches the command table to determine which system file to load (in this case, the internal file name for LOAD). Then, from the file directory, the System Processor calculates where that file resides on the disc.

2. The system Processor reads the LOAD program into System Memory overlay area 1. TEKDOS turns execution over to LOAD.

3. LOAD issues a SVC (service call) to the operating system (TEKDOS) to determine the location of (filename).

LOAD USER'S PROGRAM FILE

4. The LOAD program reads (filename) (in Tektronix Hexadecimal format) into System Memory, then causes the System Processor to transfer (filename) (in object code) into Program Memory.

Command: EMULATE Ø

Command: DEBUG

Action:

LOAD DEBUG SOFTWARE

5. The System Processor (TEKDOS) searches the command table and finds the internal file name for DEBUG. DEBUG is then loaded into System Memory overlay area 1.

6. TEKDOS turns control over to DEBUG. DEBUG directs the system to operate in a debug mode. DEBUG then returns control to TEKDOS.

Command: TRACE ALL

Action:

LOAD TRACE SOFTWARE

7. The System Processor (TEKDOS) searches the command table, finds the internal file name for TRACE, and loads TRACE into System Memory overlay area 2.

8. TEKDOS turns control over to the TRACE program. TRACE sets up the Debug and Front Panel I/O module for single-step operation.

Command: GO 3ØØ
Action:

MOVE EMULATOR REGISTER VALUES TO SYS. MEMORY

9. The System Processor swaps the register save area of System Memory with the first few bytes of Program Memory. The register save area contains random data if this swap is performed before the emulator processor is initialized. The primary purpose of this action is to allow the user to set the emulator processor registers before execution begins, by using the DSTAT or SET commands. If these commands are used, the register values set by the user are stored in the register save area of System Memory. The number of bytes in the register save area is emulator-dependent.

10. The debug control routine writes the address of the emulator processor register restore routine into the Jump Address Register on the Debug module.

11. The debug control routine causes the System Processor to write a command byte to the Debug module. The command byte has bit 2 asserted. Bit 2 tells the Debug module to force jump the emulator processor the next time the emulator processor is activated.

12. DEBUG causes the System Processor to halt. The Debug module immediately releases the SLV PAUSE line, allowing the emulator processor to become active. As soon as the emulator processor is started, the Debug module forces the JMP CMD (jump command) line low.

JUMP TO RESTORE ROUTINE

13. When the JMP CMD line goes low, jump logic on the emulator processor forces an unconditional absolute jump code onto the emulating microprocessor's data bus during its fetch cycle. The emulator processor then forces the JMP ACK control line low, acknowledging to the Debug module that its jump command is received.

14. When the Debug module receives JMP ACK from the emulator processor, it places the contents of the Jump Address Register (previously loaded by the debug control routine) on the system address bus.

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15. Jump logic on the emulator processor forces the high and low bytes of the jump address onto the emulating microprocessor's data bus one at a time (for 8-bit microprocessors) and in the proper order. The emulator processor then restores JMP ACK high.

16. The absence of the JMP ACK signal causes the Debug module to remove the Jump Address Register contents from the system address bus.

NOTE

At this point, the debug control software has been loaded into System Memory. The control software has transferred a portion of Program Memory into System Memory for storage and possible alteration. The System Processor has issued a forced jump address (containing the address of the register restore routine) to the Debug module. The Debug module has passed the address on to the emulator processor.

EMULATOR PROCESSOR BEGINS RESTORE ROUTINE

17. The emulator processor has now received the address of the beginning of the restore routine located in PROM on the emulator processor. The emulator processor begins execution of that routine by fetching the first byte.

18. The restore routine loads the register contents back into their proper locations. The register contents may have been changed by DSTAT or SET.

19. The emulator processor executes a debug SVC 1 resulting in an access to the Debug module I/O port F1. This causes a SVC interrupt of the Debug module.

20. The SVC interrupt causes the Debug module to force the SLV PAUSE control line low. SLV PAUSE forces the emulator processor off the system bus. The emulator processor responds by forcing its RUN line high.

21. Upon seeing RUN removed, the Debug module removes MSTR PAUSE, thereby allowing the System Processor to resume execution, and to also respond to the SVC interrupt.

22. The System Processor swaps the register save area in System Memory with the first few bytes of Program Memory. This action restores the Program Memory to its original state.

23. After System Memory and Program Memory have been restored to their original condition, the debug control routine loads the destination address of the previously entered GO command (in this case 0300H) into the Jump Address Register on the Debug module.

JUMP EMULATOR TO USER ADDRESS AND EXECUTE

24. Steps 11 through 17 are repeated for the GO address. However, at step 17, the emulator processor fetches the instruction located at address 0300.

25. Recall that when TRACE ALL is active, the emulator processor is performing single-step operations. Each time the emulator processor executes an instruction, the program counter registers on the Debug module must be updated. The SLV OPREQ and FETCH control lines (generated by the emulator processor during the address fetch) cause the Debug module to store the contents of the address bus in the P.C. Last register. SLV OPREQ and FETCH also cause the Debug module to issue a single-cycle interrupt to the System Processor.

26. The System Processor, even though it is paused, acknowledges the single-cycle interrupt by forcing the MSTR INTD line low.

27. At the same time the System Processor acknowledges the single-cycle interrupt, the Debug module lowers the JMP CMD line, thus issuing a jump command to the emulator processor.

UPDATE P.C. REGISTERS

28. On the next emulator processor fetch, rather than fetching the next user instruction, the emulator processor fetches a jump instruction. At the same time, the Debug module stores P.C. Next (the next program counter value).

29. When the emulator processor fetches the forced jump instruction which is hard-wired on the emulator processor itself the Debug module asserts SLV PAUSE. This causes the emulator processor to remove itself from the system bus. The emulator processor RUN line is forced high.

30. The Debug module, upon seeing that RUN is high, allows MSTR PAUSE to go high. This allows the System Processor to run and respond to the single-cycle interrupt.

31. The System Processor now asserts the INTACK and DEBUG VEN (Debug Vector Enable) lines.

32. DEBUG VEN causes the Debug module to place the single-cycle interrupt vector address on the data bus.

33. The System Processor now enters the single-cycle interrupt service routine.

NOTE

At this point, the emulator processor has executed the first instruction in the user program. Now, the System Processor module will cause the emulator processor to dump its new register contents into Program Memory.

34. The System Processor writes a control byte to the emulator processor. This enables the emulator processor dump and restore PROM, and activates the module in the special MEMSW mode. However, if the emulator processor was in emulation mode 0, it does not enter the MEMSW mode but remains in mode 0.

EMULATOR PROCESSOR DUMPS REGISTERS

35. The System Processor swaps the register save area of System Memory with the first few bytes of Program Memory.

36. The System Processor forces the emulator processor to execute the forced jump routine.

37. The emulator processor stores the contents of its registers in the first few locations of Program Memory. The emulator processor then executes the debug SVC 1.

38. The System Processor swaps the register save area of System Memory with the first few bytes of Program Memory; this returns Program Memory to its original condition.

39. The debug control program causes the System Processor to read P.C. Last and P.C. Next from the program counter registers on the Debug module. The System Processor then reads the instruction just executed from Program Memory. If the last instruction was executed from prototype memory, the System Processor performs a UGET operation to retrieve the instruction from prototype memory.

    The Program Counter values, instruction, and register values previously stored constitute a line of trace data.

40. The System Processor then either displays the trace data on an output device or stores the data in a disc file.

41. The debug control routine loads the next address into the jump address register on the Debug module. Steps 11 through 17 are repeated for this address. However, at step 17, the emulator processor fetches the instruction located at the new address.

    The sequence from step 25 through step 41 is repeated for each instruction in the user program. In this way, the program counter values for each instruction, the emulating microprocessor's register values, and the instruction itself can be stored or displayed.

We have just followed an emulator processor through a complete cycle of instruction execution while in the debug mode of operation. This provides a good example of the interaction between the System Processor, the Debug module, the emulator processor, Program Memory, and System Memory.

Section 2

SPECIFICATIONS

INTRODUCTION

The specifications in this section apply to the basic 8001/8002A μProcessor Lab, consisting of the following units:

8001 μProcessor Lab
Standard Modules
- System Processor
- System Memory
- System Communications
- Debug and Front Panel I/O
- Program Memory (one module)

Power Supplies
- +5.2 Vdc
- +12.0 Vdc 30 Vac
- −12.0 Vdc 60 Vac

8002A μProcessor Lab
Standard Modules
- System Processor
- System Memory
- System Communications
- Debug and Front Panel I/O
- Assembler Processor
- Program Memory (two modules)

Power Supplies
- +5.2 Vdc
- +12.0 Vdc 30 Vac
- −12.0 Vdc 60 Vac

μPROCESSOR LAB CHARACTERISTICS

The input power requirements (list 1, following) are for the basic configuration only. The electrical, environmental, and physical characteristics are general. For details on environmental test procedures, including failure criteria, contact your local Tektronix Field Office or representative.

1. Electrical Characteristics

Input Voltage	115 Vac ±10% or 230 Vac ±10%. A switch S2 on the back panel selects the two operating voltages.
Frequency	60 Hz ±10% (50 Hz ±10% special order)
Input Power	3.6 Amps (max) at 115 Vac, 60 Hz.

Fuses	
Primary (F4)	6A at 115 Vac, 3A at 230 Vac
±12 Vdc	
Supply (F3)	2A at 115 Vac, 1A at 230 Vac
60 Vac (F1)	0.5 Amps
50 Vac (F2)	0.5 Amps

GND and AUX BUS

A terminal block (TB2) on the back panel of the μProcessor Lab has connections for an (AUX BUS), Logic Ground (LOGIC GND) and earth ground (CHASSIS) GND. CHASSIS GND and earth ground are connected together internally. A shorting strap on the terminal block provides a single common tiepoint between logic ground and chassis ground. If the shorting strap is removed, a 1 MΩ bleeder resistor maintains a limited potential difference between logic ground and chassis ground. Logic ground is the ground bus for the μProcessor Lab modules. AUX BUS and LOGIC GND are connected to separate lines on the motherboard. The AUX BUS may be used to apply auxiliary power if desired.

2. Environmental Characteristics

Temperature (in degrees)	
Operating	0°C to +40°C (+32°F to +104°F)
Storage	−40°C to +75°C (−40°F to +167°F)
Humidity	To 90% relative non-condensing
Altitude	
Operating	To 15,000 feet (4.572 km)
Storage	To 50,000 feet (15.24 km)

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3. Physical Characteristics

Dimensions (Overall)	
Height	24.66 cm (9.62 inches)
Width	48.31 cm (18.842 inches)
Length	57.3 cm (22.347 inches)
Weight	Approximately 30 kg (66 lbs)

μProcessor Lab Power Supplies

1. Electrical Characteristics

Output Power	
+5.2 Vdc	25 Amps
+12 Vdc	3.4 Amps
−12 Vdc	3.4 Amps
Overload Protection	Automatic current limit foldback.
Line regulation	
+5.2 Vdc	
+12 Vdc	Within .05% for 10% line voltage change.
−12 Vdc	
Load Regulation	
+5.2 Vdc	
+12 Vdc	Within .05% for 50% load change.
−12 Vdc	

μProcessor Lab Standard Module Power Requirements

1. System Processor

	Current	
Voltage	**Typical**	**Maximum**
+5.2 Vdc	2A	2.5A
+12 Vdc	0.05A	0.08A
−12 Vdc	0.05A	0.08A

2. 16K Dynamic RAM

+5.2 Vdc	1.2A	1.5A
+12 Vdc	0.085A	0.6A

3. System Communications

+5.2 Vdc	1.6A	1.9A
+12 Vdc	0.128A	0.385A
−12 Vdc	0.128A	0.385A

4. Debug and Front Panel I/O		
+5.2 Vdc	2A	2.5A
5. 8001 System Memory		
+5.2 Vdc	1.1A & 65 mA/2K bank	1.7A & 90 mA/2K bank
6. High-Speed Memory		
+5.2 Vdc	1.2A	1.8A
+12 Vdc	0.085A	0.9A
−12 Vdc	0.014A	0.018A
7. Assembler Processor		
+5.2 Vdc	0.5A	undefined

ACCESSORIES

8001 μProcessor Lab Standard Accessories

8001/8002A μProcessor Lab Installation Guide
8001 μProcessor Lab System User's Manual
8001 μProcessor Lab System Reference Card

8002A μProcessor Lab Standard Accessories

8001/8002A μProcessor Lab Installation Guide
8002A μProcessor Lab System User's Manual
8002A μProcessor Lab System Reference Card

Optional Accessories

For an up-to-date listing of the available optional accessories and support items, refer to the Tektronix Products catalog or contact the nearest Tektronix Field Office or representative.

PERIPHERAL EQUIPMENT

Standard Peripheral Equipment

Flexible Disc Unit (8002A μProcessor Lab only)

Optional Peripheral Equipment

Tektronix CT8100 CRT Terminal
Tektronix CT8101 Printing Terminal (TTY)
Tektronix LP8200 Line Printer

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Section 3

SYSTEM PROCESSOR MODULE

INTRODUCTION

The System Processor module handles processing tasks, controls other modules, and performs I/O transfers with the Flexible Disc Unit and the system terminal.

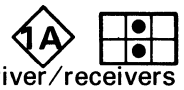
CIRCUIT DESCRIPTION

General

The System Processor Module is divided into five major sections for this discussion:

- the 2650 microprocessor and its supporting logic
- interrupt priority decoding and interrupt vector generation logic
- I/O logic for communication with the Flexible Disc Unit and the system terminal
- baud rate and interval timer logic
- program memory bank select logic

2650 Microprocessor and Supporting Logic



The 2650 microprocessor supporting logic consists of clock logic, bus driver/receivers that interface with the 8001/8002A system buses, system control signal logic, and some logic associated with the microprocessor itself.

For detailed information about the 2650 microprocessor, refer to the Signetics 2650 Reference Manual.

The support logic for the 2650 microprocessor is discussed in the following order:

- 2650 Clock Logic
- Bidirectional Data Bus Buffers
- Address Bus Buffers
- System Bus Control Logic and Buffers
- System Processor Pause Logic
- System Processor Read and Write Timing
- Power-on Reset

2650 CLOCK LOGIC

The 2650 clock is generated by a 10 MHz oscillator. The 10 MHz oscillator uses a series-resonant crystal as a feedback element across two cascaded inverting amplifiers. The 10 MHz output is buffered onto the system bus as SYS CLK for Emulator Processor use.

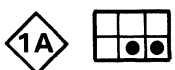
The 10 MHz clock is also divided by eight in two stages to produce the 2650 clock. The first stage consists of a divide-by-four circuit, which divides the 10 MHz oscillator frequency into a 2.5 MHz clock. The second stage consists of a flip-flop (U5030) that divides the 2.5 MHz output by two, resulting in the 1.25 MHz clock used by the 2650. The flip-flop is also controlled by an external hold signal (FP HOLD). FP HOLD provides a means for stopping the 2650 clock in the low state for any number of half cycles. FP HOLD is generated from the Maintenance Front Panel during a single-step or a breakpoint operation.

BIDIRECTIONAL DATA BUS BUFFERS 

The 2650 data lines are buffered by bidirectional bus driver/receivers (U5060, U5070). The receivers collect data from the system bus and transmit it to the 2650. The drivers take data from the 2650 and transmit it to the bus. The bus driver/receivers are controlled by the ANDed result of the RUN and R/W outputs from the 2650. When the 2650 is in a 'run' state, RUN is high and the driver/receivers are enabled by the R/W output. If the 2650 is not running, RUN is low and the bus is in the input mode. In this state, the data bus has a high input impedance and can be driven by other modules in the system.

ADDRESS BUS BUFFERS 

Tristate drivers buffer the address outputs from the 2650 and drive the system address bus. These drivers (U4040, U4050, U5040) are controlled by an inverted RUN output from the 2650. When the 2650 is running, RUN is high and the drivers are enabled, thus passing signals to the address bus. If the 2650 is halted, RUN is low and the drivers are disabled and put into a high-impedance state. The address bus is then controlled by external devices, such as an emulator processor.

SYSTEM BUS CONTROL LOGIC AND BUFFERS 

Appendix A contains a list defining all system bus lines. Refer to this list while reading the following text.

This circuit block contains the logic that converts 2650 control signals into system control signals. The buffers in this circuit place the signals on the system bus.

Tristate drivers buffer the signals INTACK, FLAG, WRP, and M/$\overline{IO}$ from the 2650. RUN is inverted and brought out to the system bus as two signals: RUN and MAST RUN. OPREQ is ANDed with INTACK and delayed 250 ns by an RC network (R2171, C2162). The resultant signal is squared by a Schmitt trigger and then input to a tristate driver (U3080) which is enabled by the inverted RUN output. The 250 ns delay guarantees that all system bus address, data, and control lines are valid when the system bus control line OPREQ goes low.

Two bus control lines, not in the Bus Control Logic block, are inputs to the 2650; the System Processor control bus signals HOLD and SENSE. These two control lines are inverted and drive the OPACK and SENSE inputs of the 2650, respectively.

SYSTEM PROCESSOR PAUSE LOGIC

The System Processor is paused when the $\overline{\text{MST PSE}}$ control line is brought low by the Debug and Front Panel I/O module (refer to Section 6). When this line goes low, the 2650 finishes its current instruction, then makes its RUN output go low. The low state of the RUN line puts the address and data bus buffers into a high-impedance state. Emulator processor modules can then control the address and data buses.

SYSTEM PROCESSOR READ AND WRITE TIMING

Timing diagrams for Read and Write operations are shown in Fig. 3-1. HOLD is generated by the memory or I/O device when data is not read or written within 200 ns of OPREQ going low. HOLD remains until read-data is valid, or write-date is received.

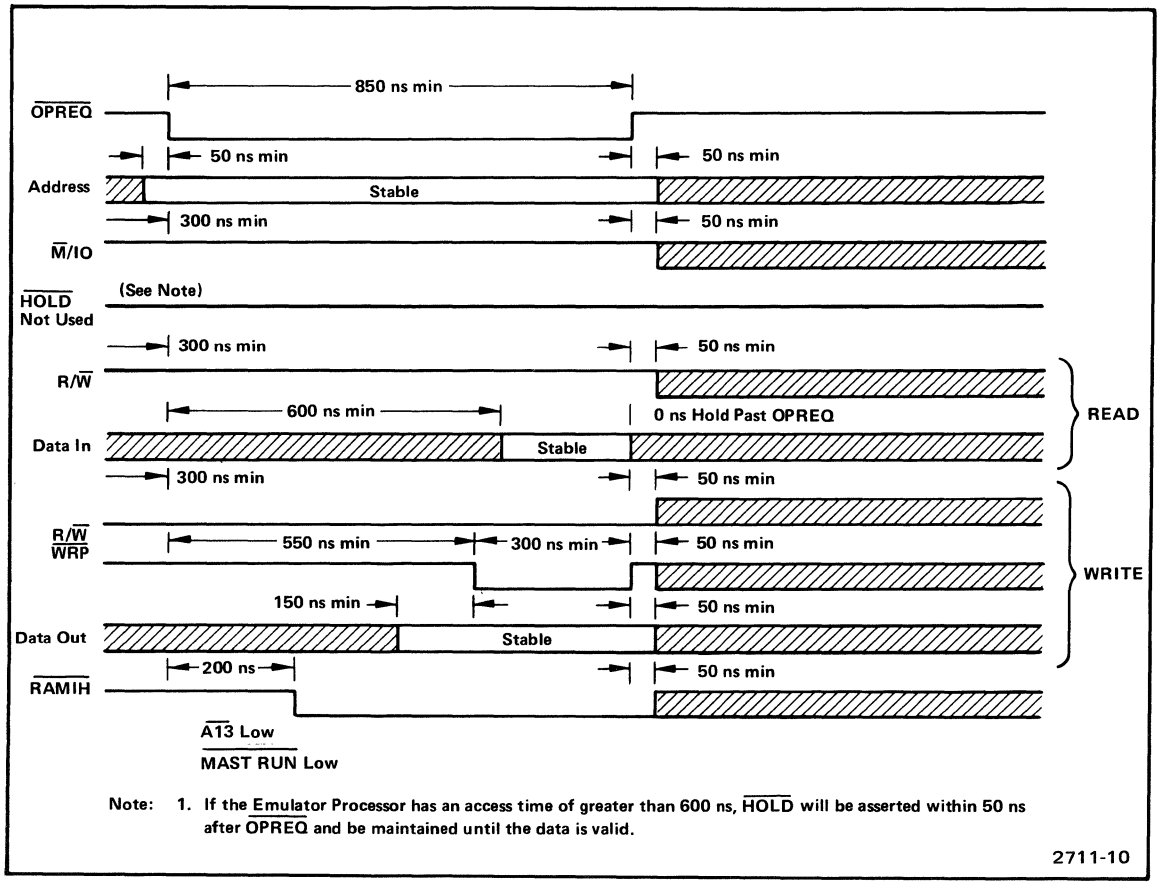


Fig. 3-1. System Processor M/IO Read and Write Timing Diagram.

POWER-ON RESET 

The Reset Logic is provided to initialize the system and to restart the 2650 during power-up. When the 5.2 V power supply reaches its operating level, the power-on detector (U2150A) initiates a reset signal (RESET). RESET causes the 2650 to fetch and execute the instruction at address 0000 in system memory.

RESET is inverted and becomes PON in the rest of the System Processor module. RESET is also sent system-wide to reset the rest of the modules.

The Power-On Reset circuit consists of a series RC circuit, which charges during power-up, and a Schmitt trigger, which provides a high 50 ms pulse. The Schmitt trigger output is buffered by an inverting open-collector driver which drives the system bus control line RESET. This allows a high PON to be initiated from the Power-On Reset circuit or by RESET.

Interrupt Logic 

GENERAL

The 8001/8002A μProcessor Lab operates with an interrupt-driven System Processor. An interrupt suspends normal program execution to execute a higher-priority service routine. After completing the service routine, the interrupted program is restored to the point where it was interrupted. The System Processor module is capable of servicing up to 16 interrupts from other modules and devices in the μProcessor Lab. An additional 16 interrupts are generated on the Debug module.

The starting address of the service routine is called an interrupt vector. Priority and enabling of these vectors is controlled by logic on the System Processor module. Table 3-1 lists the interrupting devices, priorities, and vector addresses.

Interrupt Logic circuitry is discussed in the following order:

- Interrupt Input Logic
- Interrupt Sample and Hold Logic
- Priority Encoder and Vector Generator Logic
- Interrupt Vector Address Buffer
- Interrupt Vector Decoder
- System Processor Interrupt Control Logic

Table 3-1
INTERRUPT VECTORS

Priority	Vector Address	Function
0	0000	Reset
1	0002	System Memory Parity Error
2	0004	NA
3	0006	Program Memory Parity Error
4	0008	Console In
5	000A	Console Out
6	000C	System Communications 1
7	000E	System Communications 2
8	0010	System Communications 3
9	0012	Timer
10	0014	NA
11	0016	Flexible Disc
12	0018	NA
13	001A	PROM Programmer 1
14	001C	PROM Programmer 2
15	001E	NA
16	0020	Emulator SVC 1
17	0022	Emulator SVC 2
18	0024	Emulator SVC 3
19	0026	Emulator SVC 4
20	0028	Emulator SVC 5
21	002A	Emulator SVC 6
22	002C	Emulator SVC 7
23	002E	Emulator SVC 8
24	0030	Breakpoint 1
25	0032	Breakpoint 2
26	0034	Single Cycle
27	0036	Emulator Halted
28	0038	Diagnostic Interrupt
29	003A	Real-Time Prototype Analyzer
30	003C	Debug Interrupt 30
31	003E	Debug Interrupt 31

NA = Not Assigned

INTERRUPT INPUT LOGIC 

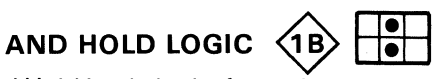
Each interrupting device has a dedicated flip-flop called in Interrupt Flip-Flop associated with it. When a device requests an interrupt, the corresponding Interrupt Flip-Flop is set. The System Processor services 16 Interrupt Flip-Flops. Seven of these are located on the System Processor module (see Table 3-2A). The remaining nine Interrupt Flip-Flops are located on other modules of the μProcessor Lab (see Table 3-2B). All Interrupt Flip-Flop outputs appear on the system bus.

Table 3-2A
INTERRUPT FLIP-FLOPS ON THE SYSTEM PROCESSOR MODULE

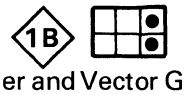
Interrupt	Function
$\overline{\text{INT 0}}$	Reset
$\overline{\text{INT 2}}$	Tape Interrupt
$\overline{\text{INT 4}}$	Data Available Interrupt
$\overline{\text{INT 5}}$	TBMT Interrupt (Transmitter Buffer Empty)
$\overline{\text{INT 29}}$	RTPA Interrupt
$\overline{\text{INT 30}}$	Printer Interrupt
$\overline{\text{INT 31}}$	Disc Interrupt

Table 3-2B
INTERRUPT FLIP-FLOPS THROUGHOUT THE 8001/8002A μPROCESSOR LAB

Interrupt	Function
$\overline{\text{INT 1}}$	System Memory Parity Error
$\overline{\text{INT 3}}$	Program Memory Parity Error
$\overline{\text{INT 6}}$	System Communications Interrupt 1
$\overline{\text{INT 7}}$	System Communications Interrupt 2
$\overline{\text{INT 8}}$	System Communications Interrupt 3
$\overline{\text{INT 12}}$	Not Assigned
$\overline{\text{INT 13}}$	PROM Programmer Interrupt
$\overline{\text{INT 14}}$	Not Assigned
$\overline{\text{INT 15}}$	Not Assigned

INTERRUPT SAMPLE AND HOLD LOGIC 

The Interrupt Sample and Hold Logic looks for an interrupt every 100 ns as long as there are no interrupts being serviced. No new interrupts will be recognized while an interrupt is being serviced. The interrupt acknowledge line, INTACK, is held high by the 2650 microprocessor while it is servicing an interrupt.

PRIORITY ENCODER AND VECTOR GENERATOR LOGIC 

The latched Interrupt Flip-Flop output is input to the Priority Encoder and Vector Generator Logic. An interrupt vector is immediately generated for the Interrupt Flip-Flop with the highest priority. The order of importance of the interrupting devices has been preassigned, and is hardwired to reflect this priority. The interrupt vector that is generated corresponds to the highest-order bit position that is true. All lower-order bits are ignored. Table 3-1 lists priorities and vector addresses for the interrupts.

INTERRUPT VECTOR ADDRESS BUFFER 

The interrupt vector is gated onto the system data bus by the Interrupt Vector Address Buffer during INTACK. (See Interrupt Sample and Hold Logic description.) Interrupt detection is repressed during INTACK. This prevents the interrupt vector from changing while it is read by the 2650.

The Interrupt Vector Address Buffer consists of tristate drivers (U4080, U4090) that drive the system bus. When the Priority Encoder and Vector Generator Logic senses an input line as low (interrupt present), the System Interrupt output line ($\overline{\text{SYS INT}}$) immediately goes low. $\overline{\text{SYS INT}}$ is inverted and ORed together with the Debug module interrupt input line ($\overline{\text{DBG INT}}$) from the system control bus. The resultant output is the 2650 interrupt request (INTREQ) and MST INTD. The 2650 microprocessor sets INTACK (from schematic 1A) high when it is ready to receive the interrupt vector and service the interrupting device. When SYS INT and INTACK are both high, the output of the NAND gate U3170B is low. This enables the tristate drivers of the Interrupt Vector Address Buffer.

INTERRUPT VECTOR DECODER 

The interrupt vector is also sent to the Interrupt Vector Decoder (U2110, U2120). The Interrupt Vector Decoder is used to reset the seven Interrupt Flip-Flops located on the System Processor module (see Table 3-2A). When an interrupt vector is detected, the Decoder generates an output to reset the corresponding flip-flop.

SYSTEM PROCESSOR INTERRUPT CONTROL LOGIC 

There are also 16 interrupt vectors generated on the Debug module. The Debug module interrupts have a lower priority than the System Processor module interrupts. This priority is established by the System Processor Interrupt Control Logic. Interrupts and their priorities are listed in Table 3-1.

When $\overline{\text{SYS INT}}$ is high, the $\overline{\text{DBG INT}}$ input generates the 2650 INTREQ. The Debug Vector Enable ($\overline{\text{DBG VEN}}$) system bus control line controls the Interrupt Vector Address Buffer on the Debug Module. When $\overline{\text{INTACK}}$ is low and E0 of U4110 (schematic 1B,, center) is low, $\overline{\text{DBG VEN}}$ is low and enables the interrupt vector onto the data bus.

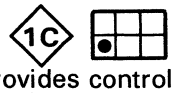
I/O Logic

GENERAL

The system terminal and the Flexible Disc Unit communicate with the μProcessor Lab via the System Processor mmodule I/O Logic. The I/O Logic contains a serial interface for the system terminal (an RS-232-C compatible terminal or current loop TTY), and a parallel interface for the Flexible Disc Unit. Also provided are a buffered bidirectional data bus for System Processor I/O transfers, I/O port decoding logic, output data latches, and input gating.

The I/O Logic will be discussed in the following order:

- I/O Decoder Logic
- Read Decoder
- Write Decoder
- Data Bus Buffers
- System Terminal Interface
- Serial Control Register
- Serial Interface Input Logic
- Serial Interface Output Logic
- Flexible Disc Unit Interface
    - Parallel Control Register
    - Parallel Input/Output Data
    - Parallel Output Latch
    - Flexible Disc Status Buffer

I/O DECODER LOGIC 

The I/O Decoder Logic provides control signals to the Read Decoder, Write Decoder, and Bidirectional Data Bus Buffer. The I/O Decoder Logic is enabled when I/O ports E8—EF are addressed. Table 3-3 shows which inputs are sensed to enable the I/O Decoder Logic.

Table 3-3

I/O DECODER LOGIC ENABLE CHART

Inputs / Outputs	System Control Bus Lines					System Address Bus Lines					
			I/O Decoder Logic Enabling Inputs								
	$\overline{WRP}$	R/$\overline{W}$	$\overline{MAST}$ $\overline{RUN}$	$\overline{OPREQ}$	$\overline{M}$/IO	$\overline{A13}$	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$
Read $\overline{RD}$		1	0	0	1	0	0	0	0	1	0
Write $\overline{WR}$		0	0	0	1	0	0	0	0	1	0
Write Pulse $\overline{WRP}$	0	0	0	0	1	0	0	0	0	1	0

0 = Low
1 = High
When $\overline{RD}$, $\overline{WR}$, $\overline{WRP}$ is 0, then output is enabled (active state).

The I/O Decoder Logic is enabled by NAND gate U2100. Control line $\overline{MAST\ RUN}$ is low when the 2650 is fetching and executing instructions. Control line $\overline{OPREQ}$ is low when the system address and data buses are valid and can be read. Address line $\overline{A13}$ is low and control line $\overline{M}$/IO is high during the execution of an I/O instruction. The address states of A3—A7 correspond to I/O ports E8—EF. See Table 3-4.

Table 3-4

I/O PORT ADDRESS VALUES

Address Bits Decoded By:	I/O Decoder Logic					Read or Write Decoders		
Address Bits:	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$
I/O Port	0	0	0	1	0	x	x	x
E8						1	1	1
E9						1	1	0
EA						1	0	1
EB						1	0	0
EC						0	1	1
ED						0	1	0
EE						0	0	1
EF						0	0	0

Address Bits A7-A3 are the same

x = don't care
0 = Logic low
1 = Logic high

When the I/O Decoder is enabled, three control outputs are activated. The first control output, $\overline{RD}$ (Read), is low when the 2650 is performing a 'Read' operation. The second control output, $\overline{WR}$ (Write), is low when the 2650 is performing a 'Write' operation. The last control output is labeled $\overline{WSTB}$ (Write Strobe), and is the ANDed result of WRITE and the control bus line WRP. WRP is a high-low-high timing pulse. It is initiated from the 2650 during a write operation and used for clocking output latches and memory.

READ DECODER 

The Read Decoder has four output lines, labeled E8, E9, EA, and EB. Each line goes low when the corresponding I/O port (E8—EB) is read. The inputs to the Read Decoder are the system address bus lines A0—A2 and the RD (Read) output from the I/O Decoder Logic. When I/O ports E8—EB are read by the 2650, RD (Read) is low and the Read Decoder is enabled. See Table 3-4 for the value of address bits A0—A2 when I/O ports E8—EB are addressed.

WRITE DECODER 

The Write Decoder has six output lines labeled E8, E9, EA, EB, $\overline{TINT}$, and $\overline{BNK}$. I/O ports E8—EB correspond to Write Decoder output lines E8—EB. Write Decoder output lines $\overline{TINT}$ and $\overline{BNK}$ correspond to I/O ports EC and ED, respectively. The inputs to the Write Decoder are the system address bus bits A0—A2 and the WSTB (Write Strobe) output from the I/O Decoder Logic. When the 2650 writes to I/O port E8—ED and control line $\overline{WRP}$ is low, WSTB (Write Strobe) is low and enables the Write Decoder. Refer to Table 3-4 for the EC and ED address bit pattern.

DATA BUS BUFFERS 

The I/O Logic bidirectional data bus buffers allow data transfers between the system data bus, the system terminal, and Flexible Disc Unit. The buffer is controlled by two inputs: Read ($\overline{RD}$) and Write ($\overline{WR}$) outputs from the I/O Decoder Logic. When $\overline{RD}$ is low, data is placed onto the system data bus from the I/O Logic. When $\overline{WR}$ is low, the I/O Logic inputs data from the system data bus.

SYSTEM TERMINAL INTERFACE

The System Terminal Interface provides an RS-232-C compatible interface and a TTY current loop for serial communications between the μProcessor Lab and the system terminal. An RS-232-C terminal and a TTY current loop terminal may not be used at the same time. The serial interface uses a Universal Asynchronous Receiver Transmitter (UART) to perform the serial-to-parallel and parallel-to-serial conversion for the system terminal.

SERIAL CONTROL REGISTER 

The Serial Control Register Latches control bits from the bidirectional data bus to enable the TTY Interrupt Flip-Flops, select UART parity, and control a paper tape reader. The 2650 writes the control bits to I/O port E9. During the 'write' operation, Write Decoder output E9 goes low. (This output is a pulse, since WRITE STROBE, the enabling input, to the Write Decoder, is a pulse. Recall that WRITE STROBE is the ANDed result of output WRITE and input WRP of the I/O Decoder Logic.) It is this pulse (E9, $\overline{\text{TTY WRITE CONT}}$) that clocks the Serial Control Register. The register then latches the control bits that were written by the 2650.

The Serial Control Register consists of three J-K type flip-flops. The first flip-flop (U3140) is used to control a TTY paper tape reader. This flip-flop is set high or low under program control, and is reset to low upon receipt of the start bit. One character is allowed to be read at a time. U4120 drives the output of U3140 (RDR CTRL(—)). The next flip-flop (U2140A) when set high, permits the UART (schematic 1C, center) to generate and check even parity. The last flip-flop (U2140B), when set high, enables the TTY Interrupt Flip-Flops (schematic 1B, left). The Interrupt Flip-Flops are set high or low under program control.

Table 3-5 shows the control bit locations in the 8-bit data byte that is placed on the data bus during a 2650 'write' operation to port E9.

Table 3-5

SERIAL INTERFACE I/O LOGIC PORTS

Ports \ Data Bits		7	6	5	4	3	2	1	0
Read	E8 Serial to Parallel Data	← Data →							
	E9 UART Status	← Not Used →			PE Parity Error	FE Framing Error	DO Data Overrun	TBMT Transmit Buffer Empty	DA Data Available
Write	E8 Parallel to Serial Data	← Data →							
	E9 Serial Control	← Not Used →					Enable TTY Interrupts	Even Parity	Reader On

SERIAL INTERFACE INPUT LOGIC 

Serial data transmitted by the system terminal to the μProcessor Lab is input by the Serial Interface Input Logic. The Serial Interface Input Logic accepts either RS-232-C or current loop logic and converts it into parallel TTL logic.

When serial data is to be received by the μProcessor Lab, the 2650 must first enable the TTY Interrupt Flip-Flops (schematic 1B, center). The TTY Interrupt Flip-Flops are enabled by the Serial Control Register. The UART (schematic 1C, center) shifts the serial data into this register and sets the Data Interrupt (DA INT) output to a high when a complete character has been received. The transition of the DA INT output from low to high clocks a TTY Interrupt Flip-Flop, which causes the 2650 to be interrupted. I/O port E9 is then read by the 2650. This causes Read Decoder output E9 to go low and enables the UART Status Buffer (schematic 1C, center). The UART status outputs DA, TBMT, OR, FE, and PE are then placed on the bidirectional data bus and input to the 2650.

If no status errors are detected, I/O port E8 is read next. Read Decoder output E8 goes low and enables the UART Output Buffer, which gates the parallel data onto the bidirectional data bus for input to the 2650. At the same time, Read Decoder output E8 is used as the UART Reset Data Available (RDA) line. Output DA INT is then reset low and the UART is ready to receive another serial data character.

SERIAL INTERFACE OUTPUT LOGIC 

Serial data transmitted by the μProcessor Lab to the system terminal is output by the Serial Interface Output Logic. The Serial Interface Output Logic converts the UART TTL serial output into RS-232-C output and current loop logic. An open-collector driver (U1120) is used for the current loop, and a bipolar driver (U4120B) for the RS-232-C output.

When serial data is to be transmitted by the μProcessor Lab, the 2650 must first enable the TTY Interrupt Flip-Flops (schematic 1B, center). The 2650 then places the character to be transmitted onto the bidirectional data bus during a write to I/O port E8. Next, the Write Decoder output line E8 goes from high to low to high, which corresponds to the time $\overline{WRP}$ (from the 2650) is low. This output is used to enable the UART to latch the character from the bidirectional data bus. The actual latching of the character into the UART port (DB0—DB7) occurs on the high-to-low transition of output E8. On the low-to-high transition, the UART shifts the character out serially. When a complete character has been shifted out, the UART sets the Transmit Buffer Empty (TBMT) output to high. The transition of the TBMT output from low to high clocks a TTY Interrupt Flip-Flop, which causes the 2650 to be interrupted. The 2650 sends the next character to the UART. This process is repeated until all characters have been transmitted.

The system terminal connector (a 25-pin connector conforming to RS-232-C standards) is mounted on the 8001/8002A μProcessor Lab rear panel. This connector is connected by a ribbon cable to plug P2 on the top edge of the System Processor module.

@

To interface the system to an RS-232-C compatible terminal, certain signal lines are permanently pulled up high. These signal lines are Clear To Send, Data Set Ready, Signal Detect, Data Terminal Ready, and Request To Send. For further interface information, refer to the 8001/8002A μProcessor Lab Installation Guide.

Flexible Disc Unit Interface

The Flexible Disc Unit Interface provides parallel communication channels between the 8002A μProcessor Lab and the Flexible Disc Unit.

The Flexible Disc Unit Interface circuitry will be discussed in the following order:

- Parallel Control Register
- Parallel Input/Output Data
- Parallel Output Latch
- Flexible Disc Status Buffer

PARALLEL CONTROL REGISTER 

The Parallel Control Register (U2040) latches control bits from the bidirectional data bus to direct the Flexible Disc Unit. The Control Register consists of six D-type flip-flops and four tristate buffers. Two flip-flop outputs enable the Disc and Printer Interrupt Flip-Flops in the Interrupt logic (schematic 1B). The four remaining flip-flops output signals to the tristate buffers that drive the Flexible Disc Unit control inputs.

Table 3-6

PARALLEL INTERFACE I/O LOGIC PORTS

Ports \ Data Bits		7	6	5	4	3	2	1	0
Read	EB Input Parallel Data	← Data →							
	EA Flexible Disc Unit Status	Flag = 1	← Not Used →					Printer Fault = 0	Printer
Write	EB Output Parallel Data	← Data →							
	EA Flexible Disc Unit Control	Not Used	Not Used	PNTR INT EN	DISC INT EN	CTRL Not Used	C1	C0	$\overline{\text{STRB}}$

The process in which control bits are latched into the Parallel Control Register (Table 3-6) is the same as the process for the Serial Control Register. The only difference is that the 2650 now writes to I/O port EA rather than to I/O port E9.

PARALLEL INPUT/OUTPUT DATA 

The Flexible Disc Unit input data lines (DID0—DID7) are terminated by a Parallel Input Network and are received by the Parallel Input Buffer. The Parallel Input Buffer consists of tristate drivers (U2060B, U2070) that gate the data onto the bidirectional data bus during a read of I/O port EB. The tristate drivers are enabled when Read Decoder output line EB is low.

PARALLEL OUTPUT LATCH 

Output data is strobed into the Parallel Output Latch (U1040, U1060). The Parallel Output Latch consists of an 8-bit data register (U1040, U1060) and drivers that buffer the outputs. Output data is stored in the 8-bit data register during a 2650 write to I/O port EB. Write Decoder output line EB supplies the clocking signal.

FLEXIBLE DISC STATUS BUFFER 

The Flexible Disc Unit status lines (PBZY, PFLT, TAPE, and FLG) are terminated with a Shaping Network (schematic 1D, lower center) and are received by the Flexible Disc Status Buffer (U2060A). The Flexible Disc Status Buffer consists of tristate drivers (U2060A) that gate the status bits onto the bidirectional data bus during a read to I/O port EA. The tristate drivers are enabled when the Read Decoder output line EA (schematic 1C, upper center) is low.

The three Flexible Disc Unit lines PBZY, TAPE, and FLG are also used as Flexible Disc Unit controller signals. These signals are input to the Shaping Network (schematic 1D, lower center) which consists of an RC filter and a Schmitt trigger. The Shaping Network converts the three signals into interrupts. PBZY, TAPE, and FLG become Printer Interrupt (PNTR INT), Paper Tape Reader Interrupt (TAPE INT), and Flexible Disc Unit Interrupt (DISC INT), respectively. The TAPE INT signal is provided so that a high-speed paper tape reader may replace the Flexible Disc Unit. Normally only the FLG signal is used.

Baud Rate and Timer Logic

The Baud Rate and Timer Logic will be discussed in the following topics:

- 10 MHz Oscillator
- Divider Network
- UART Clock and Number of Stop Bits
- Interrupt Timer Logic

10 MHz OSCILLATOR 

A crystal-controlled oscillator identical to that used in the 2650 Clock logic is used for the baud rate clock and interval timer generators. The 10 MHz output of the oscillator is buffered onto the system bus as SYS CLK (System Clock).

DIVIDER NETWORK 

The 38.4 kHz system I/O clock is provided by a circuit that divides the 10 MHz oscillator output by 260 (see Fig. 3-2).

The UART (schematic 1C, center) requires clock frequencies of 16 times the available baud rates. The 38.4 kHz output is the clock frequency for 2400 baud. The 38.4 kHz output is further divided by a series of divide-by-two circuits to provide clocks for 1200, 600, 300, and 150 baud. The clock for 1200 baud is also input to a divide-by-11 circuit, to provide the clock for 110 baud. The clock for 150 baud (2.4 kHz) is divided down by 24 to a 10 ms interval timer clock. The 10 ms interval timer clock is further divided down to a 100 ms interval timer clock. Both the 10 ms and the 100 ms interval timer clocks are jumper-selectable. Figure 3-2 shows the Baud Rate Clock Divider chain.

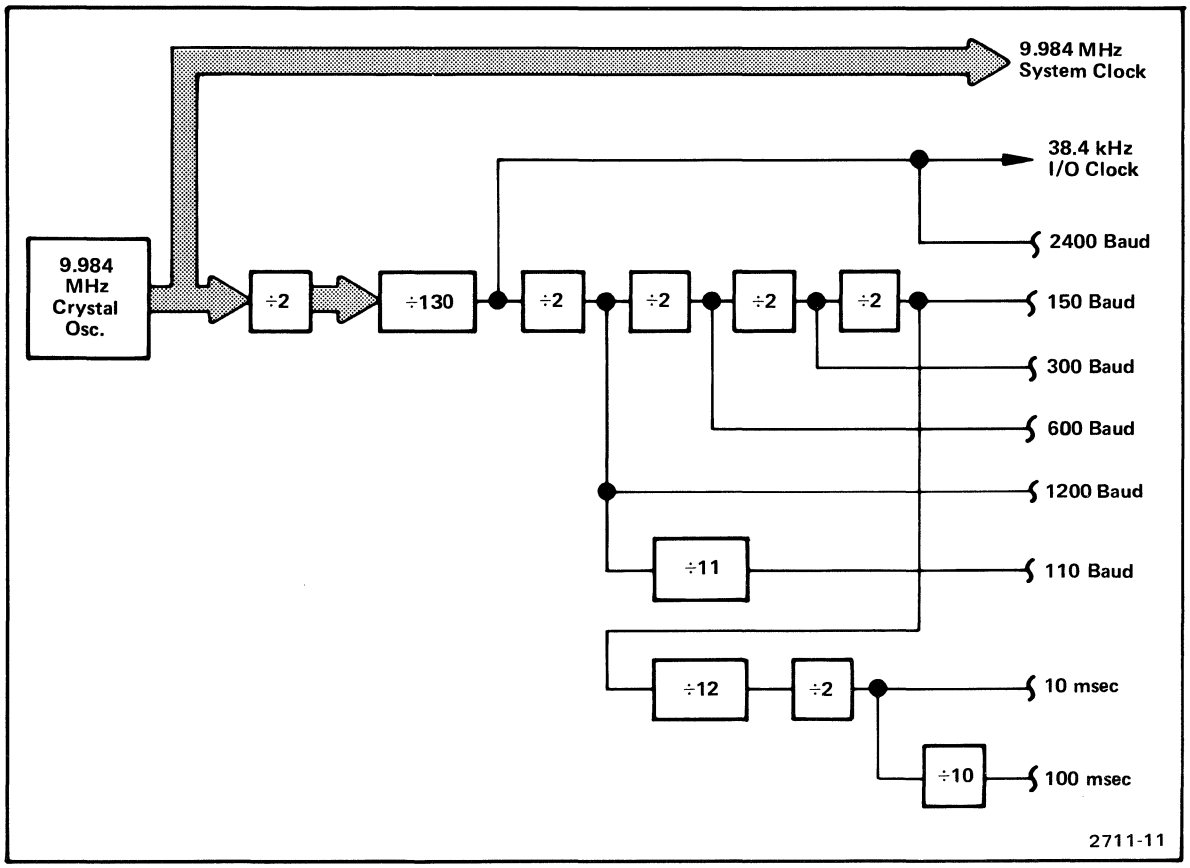


Fig. 3-2. Baud Rate Clock Divider.

UART CLOCK AND NUMBER OF STOP BITS 

The receive and transmit portions of the Universal Asynchronous Receiver/Transmitter (UART) are clocked by the UART CLOCK line from U1160 of the UART Clock circuitry. The UART CLOCK line operates the UART at various baud rates.

The outputs from the Divider Network (schematic 1E, center) are fed to the UART CLOCK multiplexer (U1160). Refer to Fig. 3-2 for a list of outputs from the divider network. The frequency selected as UART CLOCK is determined by the Baud Rate Thumbwheel Switch (S1141). The outputs of S1141 control the multiplexer to generate the desired frequency. A truth table for the thumbwheel switch (S1141) is shown on schematic 1E. Table 3-7 shows the baud rate for each switch position.

In addition to selecting the baud rate, the thumbwheel switch (S1141) is used to determine the number of stop bits used by the UART. Outputs from the switch are applied to a gating circuit (U1150A, U1150B) to determine the number of stop bits used. The circuit also determines the use of parity bits by the UART at different baud rates. Table 3-7 shows the number of stop bits and the use of parity for each available baud rate.

Table 3-7
BAUD RATE THUMBWHEEL SWITCH SELECTION AND FORMAT

Thumbwheel Position	Baud Rate	START Data Format STOP
9	110	S 0 1 2 3 4 5 6 P S S
8	110	S 0 1 2 3 4 5 6 7 S S
7	150	S 0 1 2 3 4 5 6 P S
6	300	same as 150
5	600	same as 150
4	1200	same as 150
3	2400	same as 150

INTERRUPT TIMER LOGIC 

The Interrupt Timer Logic allows the 2650 to be controlled by a jumper-selectable 100 ms or 10 ms interval timer. The Interrupt Timer consists of two up-down counters (U5130, U5120). The counters divide the baud rate clock into 100 Hz and 10 Hz signals. See Fig. 3-2. On the low-to-high transition of the interval timer output (TIME INT), the Timer Interrupt Flip-Flop is clocked and the 2650 is interrupted.

Program Memory Bank Select Logic 

The Program Memory Bank Select Logic allows the 2650 to access Program Memory. The System Processor accesses Program Memory by bank switching one 16K block of Program Memory (of a possible four 16K blocks) into the System Memory 16K-32K address space. The 16K block is specified by two control bits in a system I/O command.

Table 3-8 shows the control bit positions in the data byte that is placed on the data bus during a 2650 'write' operation to port ED. When I/O port ED is written to, the Write Decoder (schematic 1C, center) outputs a signal called $\overline{\text{BNK}}$.

The 2650 address bit 14 (ADR 14) output controls the system address bus lines A14 and A15 (U3060A, U3060B), and also becomes the System/Program Memory Select line (CMEM). When the system address is 16K or above, ADR 14 is high and enables the latched control bits onto system address bus lines A14 and A15. Program Memory is also enabled by the CMEM output. If ADR 14 is low, System Memory is enabled: address bus lines A14 and A15 are forced high, thus addressing the first 16K block of System Memory.

Table 3-8

TIMER INTERRUPT AND PROGRAM MEMORY BANK SWITCH I/O PORTS

Ports \ Data Bits		7	6	5	4	3	2	1	0
Write	EC Timer Interrupt	← Not Used →							DB0
	ED Program Memory Bank Switch	← Not Used →						DB1	DB0

Section 4

16K DYNAMIC RAM MODULE

INTRODUCTION

The 16K Dynamic RAM module is used as Program Memory for the 8001 and 8002A μProcessor Labs, and as System Memory for the 8002A μProcessor Lab. The 16K Dynamic RAM module contains 16K X 8-bit words of memory, with a ninth bit used for parity. The 16K Dynamic RAM module can be configured for use with 16-bit microprocessors.

This section describes the following functions of the 16K Dynamic RAM module:

- 16K RAM Configuration
- RAM Memory
- Bootstrap PROM
- Data and Parity Control
- Address Control
- Configuration Logic
- Byte/Word Control
- Refresh Request Logic
- Operation Control and Timing

CIRCUIT DESCRIPTION

Refer to the 16K Dynamic RAM schematics while reading this text.

16K RAM Configuration 

The 16K Dynamic RAM module is configured for use in System or Program memory, and for 8-bit oriented processors (byte mode) or 16-bit oriented processors (word mode), through the use of four switches and four jumpers. The functions and uses of these switches and jumpers are given in Tables 4-1 and 4-2.

Table 4-1
SWITCH AND JUMPER POSITIONS AND FUNCTIONS

Switch Number	Switch Name	Switch Function
S4163-1	A14	When this switch is ON, the module will respond to memory addresses in which A14 = 1, provided all other selection conditions are met.
S4163-2	A15	When this switch is ON, the module will respond to memory addresses in which A15 = 1, provided all other selection conditions are met.
S4163-3 J11, J12	Sys/Prog	Setting this switch to the ON position configures the module for Program Memory. Setting this switch to the OFF position configures the module for System Memory operation. Note that for System Memory, jumper J11 must be added and J12 deleted; for Program Memory, jumper J12 must be added and J11 deleted.
S4163-4 J9 J10	HI/LO	To configure the module for byte-oriented processors, jumper J10 is installed and J9 is deleted. For use with work-oriented processors, J9 is installed and J10 is deleted. J10 allows the module to work as part of the memory pair required for word-oriented operation. Switch S4163-4 is used only when a pair of memory modules is set for 16-bit word mode operation. If the switch is OFF, the module accepts bits DØ—D7 of the 16-bit data bus. Setting this switch ON configures the module to serve as bits D8—D15 of a 16-bit data bus, when memory modules are used in pair for 16-bit word mode operation.

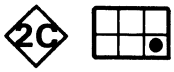
Table 4-2
MODULE ADDRESS SWITCHES

Program Memory Module	Memory Address	Switches	
		A15	A14
A	0000 – 3FFF	OFF	OFF
B	4000 – 7FFF	OFF	ON
C	8000 – BFFF	ON	OFF
D	C000 – FFFF	ON	ON

RAM Memory 

The data storage of the 16K Dynamic RAM module is accomplished by a RAM array capable of storing 16,384 9-bit words; the ninth data bit is the parity bit. The memory is physically arranged in four rows of 4K X 1 dynamic RAM devices, with nine devices to each row. Each of the four rows is enabled by a Chip Enable input (CE1—CE4) from the Address Control circuitry (schematic 2B, top). Twelve address lines (AØ—A11) access the RAMs.

On each of the 22-pin RAM devices, address lines AØ—A5 access the 64 internal rows; lines A6—A11 address the 64 columns. To write, read, or refresh a row of devices, the respective Chip Enable signal (CE1, CE2, CE3, or CE4) is applied to the CE Clock input of each RAM device in that row.

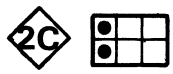
Bootstrap PROM 

The 16K Dynamic RAM module has the capacity to contain 256 bytes of PROM (Programmable Read Only Memory). When the module is used for 8002A System Memory, a 1702A PROM device is inserted in socket U6010. The PROM overrides the first 256 bytes of RAM address space, and is enabled when the System/Program switch (S4163-3, schematic 2A, lower left) is in the System position. (See Table 4-1.) The PROM contains the bootstrap routine to load TEKDOS from flexible disc into System Memory and to initialize the μProcessor Lab system at power-up or system reset. The PROM is used only for 8002A System Memory.

For 8002A System Memory modules, the PROM Address Decoder (U2100, schematic 2B, left) decodes $\overline{\text{PROM ADR}}$ to operate the PROM memory. $\overline{\text{PROM ADR}}$ is produced when A8—A15 and $\overline{\text{CMEM SW}}$ are all low.

Address lines to the PROM (AØ—A7) are run directly from the system address bus, through the PROM address buffers (U6030 and U6040), to the PROM (U6010). These lines are separate from the RAM address lines (ADØ—AD11), which go through the Address Control circuitry. PROM address lines are designed this way to allow refresh addressing of the RAM while the PROM is being accessed. The RAM may be refreshed at this time because Chip Enable (CE) is not in use.

When this module is used as System Memory, data from the Bootstrap PROM is read through the data output registers. The PROM Access one-shot multi-vibrator (U3170A, System Request Logic, schematic 2A, center) controls Read Strobe (RDSTR) to clock the data registers.

Data and Parity Control 

Data to and from the 16K Dynamic RAM module is routed and checked for parity by the Data and Parity Control circuitry.

DATA WRITE

The memory module receives data lines DØ—D15 from the system data bus (labeled P1 on schematic 2C). These lines are received and buffered by tristate transceivers U4120 and U5120 (for lines DØ—D7) and U4130 and U5130 (for D8—D15). Only lines DØ—D7 are used with byte-oriented emulator processors. D8—D15 are used when two memory modules are used in pair for 16-bit word-oriented emulator processors.

In word (16-bit) mode, one module is designated as the low-byte module (bits DØ—D7), and the other as the high-byte module (bits D8—D15). In byte mode, or for the low byte of word mode, the buffers for DØ—D7 are enabled by the Write Low signal (WH) to receive data from the data bus. The buffers for D8—D15 are enabled to write data by Write High ($\overline{WH}$).

Data from the bus is stored in the data registers (U4110 and 5110). It is then clocked by Write Data Strobe (WDSTR) to the Data In (DIN) inputs of the RAMs. When the RAM receives Write Enable (WE) signal (from the Timing Generator on schematic 2A), the data is written into the selected memory address. As data leaves the registers, even parity is generated by the parity generator (U3110, schematic 2C, upper left) and is stored in the ninth bit (parity) of the selected row of RAM. The parity RAMs are U1080, U2080, U3080, and U4080.

DATA READ

Data is read out of memory when the desired row of RAM is enabled. When the array is addressed, the selected data is read into the output registers (U4140 and U5140, schematic 2C, right). Upon receipt of Read Data Strobe (RDSTR from schematic 2A, right), data is latched from the output registers to the four data bus buffers (U4120, U5120, U4130, and U5130, schematic 2C, left). The data is put on the data bus either through data lines DØ—D7 (low byte or lines D8—D15 (high byte). If the module is configured for byte mode operation or low byte of word mode, Read Low (RL from Byte/Word Control on schematic 2A) enables the buffers for lines DØ—D7 (U4120 and U5120). Read High (RH) causes data to be placed on the bus through lines D8—D15 (U4130 and U5130) when the module is configured for the high byte of word mode.

When data is read out of the data output registers (U4140 and U5140), its validity is checked by the parity checker (U3140, schematic 2C, right). Even parity denotes valid data. When parity is found to be odd, an error signal is sent from the parity checker to the parity error detector (U2110 schematic 2C, lower right). If there is a parity error, the error detector (U2110) issues a parity interrupt ($\overline{PARITY\ INT}$) signal when the detector is clocked by Parity Strobe ($\overline{PARITY\ STR}$ from the Timing Generator, schematic 2A). Parity interrupt signals are received by interrupt decode circuitry (U4170, U5170, schematic 2C, bottom), which sends a Master Interrupt 1 in System Memory operation, or a Master Interrupt 3 in Program Memory operation. The $\overline{PARITY\ INT}$ flip-flop is reset when the proper I/O vector (address 0002 or 0006) appears on the data bus during a Master Interrupt Acknowledge (INTACK). The I/O decoder output (U3120) and RESET combine to reset the parity error detector (U2110).

Address Control 

The Address Control circuitry controls address lines AØ—A15 to accomplish module selection and byte/word shifting, and provides refresh cycle addresses for the 16K Dynamic RAM module. Chip Enable lines CE1—CE4 are generated with this circuitry.

8-BIT OPERATION

In byte mode operation, address lines AØ—A15 have the following functions:

A14 and A15	select the module. (Up to four Program Memory modules may be present in the μProcessor Lab.)
A12 and A13	select one of the four 4K X 9-bit rows of RAM on the specified module.
AØ and A11	select addresses within the specified 4K X 9-bit row.

Address lines A14 and A15 are sent to a multiplexer (U5100). The multiplexer output is used for module selection in the Module Configuration Logic (schematic 2A, left center).

Address lines A12 and A13 are output from a multiplexer (U1090) as N1 and N2, and are sent to a decode and driver circuit (U1100, U1120, and U1110) which provides the four Chip Enable signals (CE1—CE4).

For normal byte mode operation, address lines AØ—A11 are taken from the bus to the address inputs of the RAMs.

16-BIT OPERATION

When a 16-bit word-oriented emulator processor is used, two Program Memory modules are required. One module of the pair is configured to store the lower eight bits of the 16-bit word (low byte). The other module is configured to store the upper eight bits (high byte).

The modules are configured as high or low byte by switch S4163-4 of each module (as explained in Table 4-1). The address lines for word mode operation are the same as for byte mode operation. Table 4-3 shows module addressing in word mode.

If memory has been configured for 16-bit word operation, and is then accessed by an 8-bit byte-oriented processor, the modules of the word pair are addressed in alternating fashion (see Table 4-3). Both modules access only the low data byte. Alternation between modules of the word pair is designated by a HI/LO bit enabling either the high-byte module or the low-byte module. For byte-oriented access of a word pair, AØ is used as the HI/LO bit instead of being used as an address bit. To use AØ as the HI/LO bit, all address lines must be shifted down. The shift is performed by the address multiplexers (U1090, U2090, U3090, U4090, and U5090). The shift occurs when the address multiplexer receives the signal combination (WD ACCESS + $\overline{\text{WDMEM}}$) · $\overline{\text{RUN}}$ at U2140. A1 becomes ADØ (AØ), A2 becomes AD1 (A1), etc. AØ becomes the HI/LO bit, alternating the addressing between modules. During a front panel access, no address line shift takes place; A15, rather than AØ, is used for high/low byte selection.

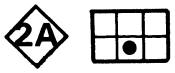
Table 4-3

MODULE ADDRESSING IN WORD MODE

	16-Bit Emulator Processor	8-Bit Emulator Processor	
	Data	Data	
	LO Module & HI Module 0 15	LO Module 0 7	HI Module 8(0) 15(7)
ADDRESS	0000	0000	0001
	0001	0002	0003
	0002	0004	0005
	0003	0006	0007
	0004	0008	0009
	0005	000A	000B

SIX-BIT REFRESH ADDRESS MULTIPLEXER 

The RAMs must be refreshed sufficiently often to keep stored data valid. One row address of each individual RAM device must be refreshed every 31.25μs; all six row addresses must be refreshed within a 2 ms period. The Refresh Request logic insures that sufficient refresh cycles occur. A six-bit refresh multiplexer, consisting of U3090, U4090, and U5090, accesses the six row addresses of the RAM devices to refresh them. During the refresh cycle, normal address lines to the RAMs are inhibited. Figure 4-1 shows Refresh timing relationships.

Refresh Request Logic 

When refresh begins, REF OP (from Refresh Request Logic, schematic 2A) strobes U1090 and U2090; this inhibits addresses A6—A11. The six-bit Refresh Address Multiplexer (schematic 2B) is shifted by SYS OP to provide addresses from the Refresh Address Counter (U3100 and U4100). The refresh counter increments after each refresh cycle to assure that all rows have been addressed within a 2 ms period. All four Chip Enable lines, CE1—CE4, are activated when the Chip Enable driver (U1110) is reset by SYS OP.

SYSTEM MODE REFRESH REQUEST

Every 26μs, the I/O CLOCK rising edge clocks the Refresh Pending flip-flop (U3160B). The falling edge of I/O CLOCK triggers the 20μs Refresh one-shot multivibrator (U3170). The falling edge of the following OPREQ causes the Refresh Request flip-flop (U3160A) to issue the refresh request to the Operation Control logic. When the present memory cycle is finished, the Operation Control flip-flop (U2170A) is clocked, issuing REF OP to activate RAM refresh. If OPREQ does not occur within 20μs of the I/O CLOCK, the 20μs one-shot will unconditionally cause a refresh request and begin the RAM refresh cycle.

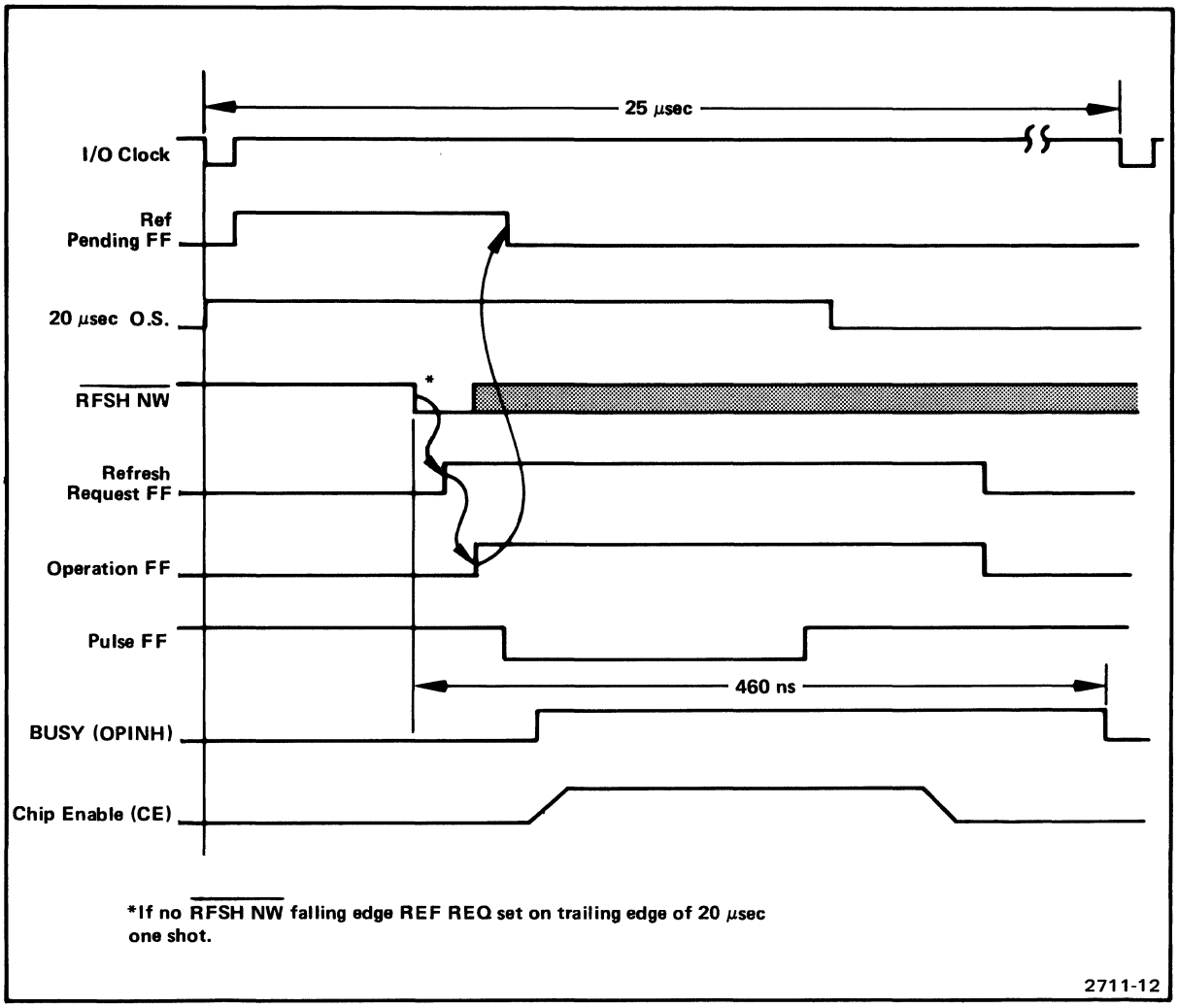


Fig. 4-1. 16K Dynamic RAM Refresh Operation.

PROGRAM MODE REFRESH REQUEST

For Program Memory modules, the rising edge of I/O CLOCK sets the Refresh Pending flip-flop (U3160B), and the falling edge of I/O CLOCK triggers the 20 μs Refresh one-shot multivibrator (U3170). For Program Memory, jumper J11 is disconnected from the refresh request flip-flop (U3160A) and jumper J12 is connected to the clock input (see Table 4-1). J12 allows RFSH NW (Refresh Now) to clock the refresh request flip-flop. RFSH NW is a signal from the emulator processor, indicating that the processor will not need the bus and that there is time for a refresh cycle. When RFSH NW occurs, a refresh request is sent to the Operation Control circuitry. As soon as the present memory cycle is finished, the Operation Control logic clocks the Operation Control flip-flop (U2170A), causing REF OP to activate chip refresh. If RFSH NW does not occur within 20 μs of I/O CLOCK, the 20 μs one-shot will unconditionally cause a refresh request. The refresh will begin as soon as the present memory cycle is completed. Refresh is not seen by the emulator or by the System Processor.

Operation Control and Timing Generator 

The Operation Control circuitry receives system access requests and refresh requests, resolves contention between these requests, and generates all timing signals for write, read, and refresh operations.

Operation Control receives system and refresh requests through U2160. Because of the importance of refresh, a refresh request has priority over a system request, and therefore controls the state of the operation control flip-flop (U2170).

Read, Write, and Refresh timing signals are created by the Timing Generator circuitry. When the Operation Control logic accepts a system or refresh request, it sets the AD STR flip-flop (U1160); this sends a low-going signal down the 200 ns delay line (DL1140). At the end of the 200 ns delay, the low-going signal resets the AD STR flip-flop, and a positive-going signal is sent down the delay line. In this way, the 400 ns required for the memory cycle is derived. The timing pulses for Read, Write, and Refresh operations are taken from taps along the delay line, through logic gates, and through a multiplexer (U2130) which provides the required timing. The Write flip-flop (U2170B) controls the multiplexer to provide either Write or Read timing. During refresh, timing signals are inhibited by applying REF OP to the gating input of the multiplexer.

The following paragraphs explain the activities of the Operation Control logic in Read, Write, and Refresh modes.

READ

Figure 4-2 shows the memory Read timing relationships.

When the module is selected, a System Pending signal will be produced when the next OPREQ clocks the System Pending flip-flop (U2150B). System Pending allows HOLD to be produced.

The System Pending flip-flop (U2150) directly resets the System Request flip-flop (U2110). U2110 immediately issues a System Request signal to the Operation Control logic. Unless a refresh is pending, the system request is gated through to clock the Write (U2170B) and Operation (REF OP, U2170A) flip-flops. Bus line R/W instructs the Write flip-flop to set the timing multiplexer (U2130) to select Read operation outputs when clocked. The system request also sets the AD STR flip-flop (U1160). After an 80 ns delay, the Chip Enable flip-flop (U2150A) is clocked to output $\overline{CE}$ for 240 ns. Memory data is sampled (RDSTR) and HOLD is reset 220 ns into the cycle; this tells the system that data is valid.

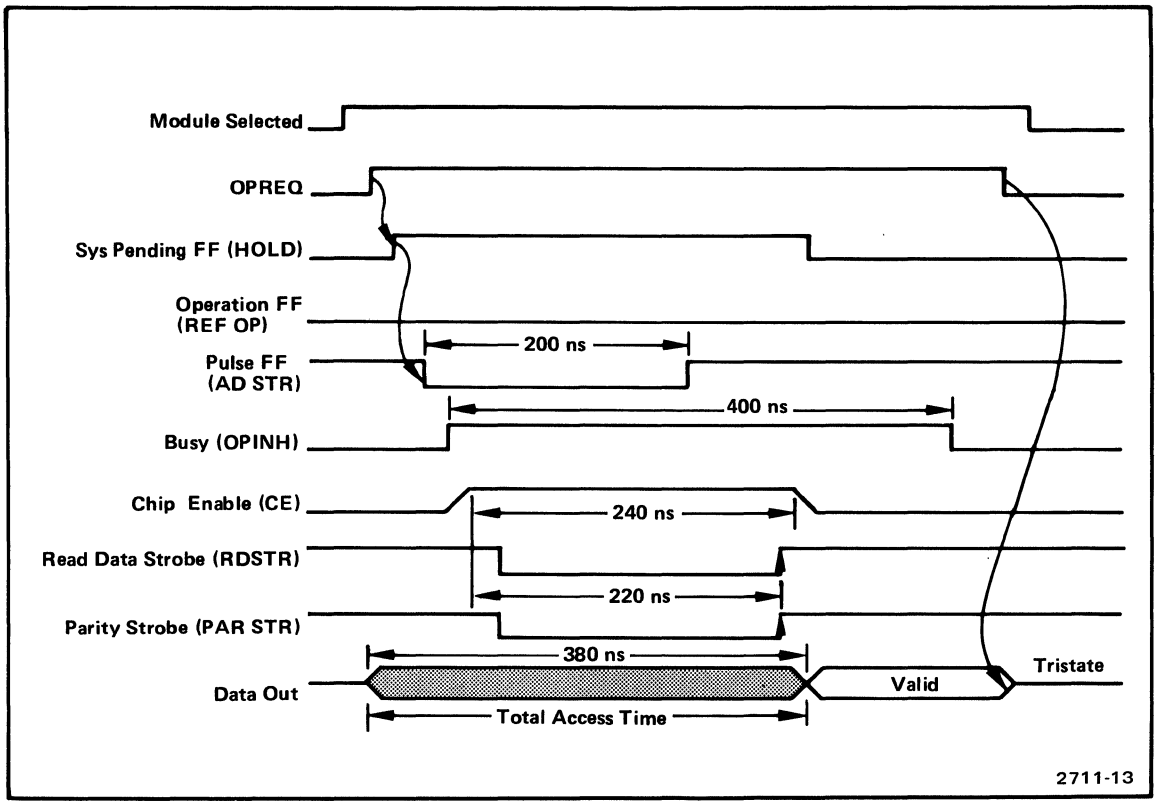


Fig. 4-2. 16K Dynamic RAM Memory Read Operation.

WRITE

Figure 4-3 shows the memory Write timing relationships.

In the Write mode, OPREQ clocks the System Pending flip-flop (U2150B); this allows $\overline{\text{HOLD}}$ to be generated. Although the Write command is on the bus (R/$\overline{\text{W}}$), no system request is issued until $\overline{\text{WRP}}$ is received, indicating valid data. When $\overline{\text{WRP}}$ is received, the System Request flip-flop (U2110) is set, producing a system request. The system request will clock the Write and Operation (REF OP) flip-flops. Bus line R/W provides the conditions for the Write flip-flop (U2170B) to output a Write signal. The Write signal from the Write flip-flop will instruct the timing multiplexer to select the Write operation outputs.

System Request also sets the AD STR flip-flop (U1160), thus starting the timing sequence. Chip Enable is generated and data is sampled (WD STR) 40 ns into the cycle. Write Enable is generated 80 ns into the cycle. Because the write data is stored and the memory chips store the address, the HOLD signal is reset early in the cycle, allowing the processor to proceed.

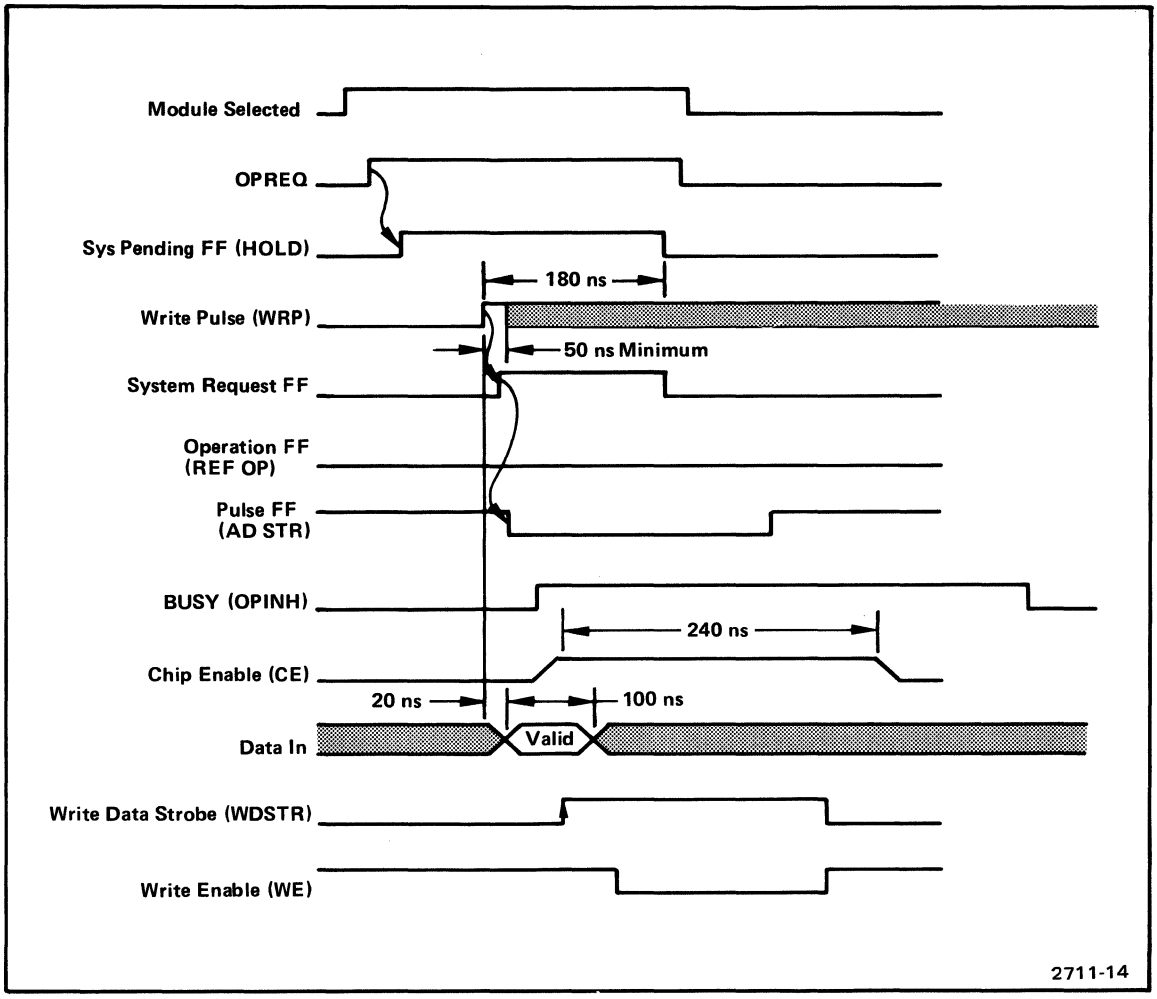


Fig. 4-3. 16K Dynamic RAM Memory Write Operation.

REFRESH OPERATION

Refer back to Fig. 4-1 for the memory Refresh timing relationships.

A refresh cycle begins when the I/O CLOCK leading edge triggers the 20 μs Refresh one-shot multivibrator (U3170). The Refresh Pending flip-flop (U3160B) is clocked by the trailing edge of I/O CLOCK, thus generating Refresh Pending. The next $\overline{\text{RFSH NW}}$ (OPREQ for System Memory modules) will clock the Refresh Request flip-flop (U3160A) to produce a refresh request to the operation control. If $\overline{\text{RFSH NW}}$ (Program Memory) or OPREQ (System Memory) does not occur within 20 μs, the 20 μs one-shot (U3170) will unconditionally set a Refresh Request. The 20 μs one-shot insures that a refresh cycle occurs every 26 μs. As soon as the memory completes its present cycle, the refresh request will set the AD STR flip-flop (U1160), and clock the Operation Control flip-flop (REF OP, U2170A) to output a REF OP. REF OP will inhibit the timing multiplexer (U2130 in the Timing Generator, schematic 2A, right), assuring that no Read or Write timing signals will be output during refresh. REF OP also switches the Address Control to the refresh

address mode and enables all four CE lines. At 320 ns into the 400 ns cycle, the Operation Control (REF OP, U2170A) and Refresh Request (U3160A) flip-flops are reset to allow address set-up time for a system request.

Configuration Logic 

Module Configuration logic designates the standard 16K Dynamic RAM module as either System or Program Memory. In Program Memory mode, Module Configuration logic additionally designates the module address and detects module addressing from the emulator or from the System Processor.

The module is selected as either System or Program Memory by setting two jumpers (J11, J12) and one switch (S4163-3). The two jumpers, J11 and J12, select the clock (OPREQ or $\overline{\text{RFSH NW}}$) for the Refresh Request flip-flop. (See Table 4-1.)

When the System/Program switch (S4163-3) is in the System position (open), the Bootstrap PROM circuit is enabled. The PROM Access one-shot (U3170), triggered by OPREQ, is activated by the System/Program switch to produce $\overline{\text{PROM CS}}$.

In Program Memory, up to four memory modules may be used. Each module is given an individual address by the programming switches S4163-1 and S4163-2. S4163-1 and S4163-2 allow A14 and A15 to control the enabling of the four memory modules. (See Tables 4-1 and 4-2).

Byte/Word Control 

Byte/Word Control circuitry is used to configure the modules for either byte-oriented or word-oriented emulator processors. Byte/Word Control circuitry controls the address line shift, data line selection, and HI/LO byte module selection.

To set up the module for word-oriented emulators, jumper J9 is installed. The HI/LO switch (S4163-4) designates the module as high or low byte of word pair.

Data bus buffers are selected and enabled by the data buffer control (U1120B). When bus line $\overline{\text{WD ACCESS}}$ goes low, signalling access by a word-oriented emulator, the high-byte module data bus buffers (D8—D15) will be enabled by $\overline{\text{WH}}$ or RH, depending on whether bus line R/$\overline{\text{W}}$ signals a Read or Write operation. The low-byte module data bus buffers (DØ—D7) are enabled by WH or RL. These enabling signals are the inverted result of the data buffer control (U1120) outputs $\overline{\text{WH}}$, $\overline{\text{RH}}$, and $\overline{\text{RL}}$.

System bus line R/W enables the data bus control to output either Read enables or Write enables. In word mode, $\overline{\text{WD ACCESS}}$ and the HI/LO switch determine if the control will enable high or low byte buffers. Only RL and WH are generated for byte mode operation. RH and $\overline{\text{WH}}$ are generated only during word mode to enable the high-byte buffers. During some operations, both the read and write buffers will be enabled at the same time.

In word mode, when a word pair is accessed by a byte-oriented emulator, WD ACCESS will not be present, indicating byte access. Only one module of the word pair will be accessed at a time, in alternating fashion as shown in Table 4-3.

9900 WORD MODE HARDWARE MODIFICATION

This hardware modification is only to be performed on those memory modules to be used in word mode with the 9900 Emulator Processor. Once the modules have been modified, byte-oriented processors can still be used, provided both memory modules are used together. In that case, the modified modules are accessed by reading from or writing to each one alternately.

Refer to Fig. 4-4 for the locations of the following runs.

Modification Procedure:

1. Cut runs to pins 1 and 2 of U5150.
2. Cut run to pin 12 of U4170.
3. Cut jumper J10 (located between U5150 and U5160).
4. Connect jumper between pins 2 and 4 of U5150.
5. Connect jumper between pin 1 of U5150 and pin P1-80.
6. Connect jumper between pin 3 of U5150 and pin 12 of U4170.
7. Connect a 560-ohm resistor between pins 3 and 14 of U5150.

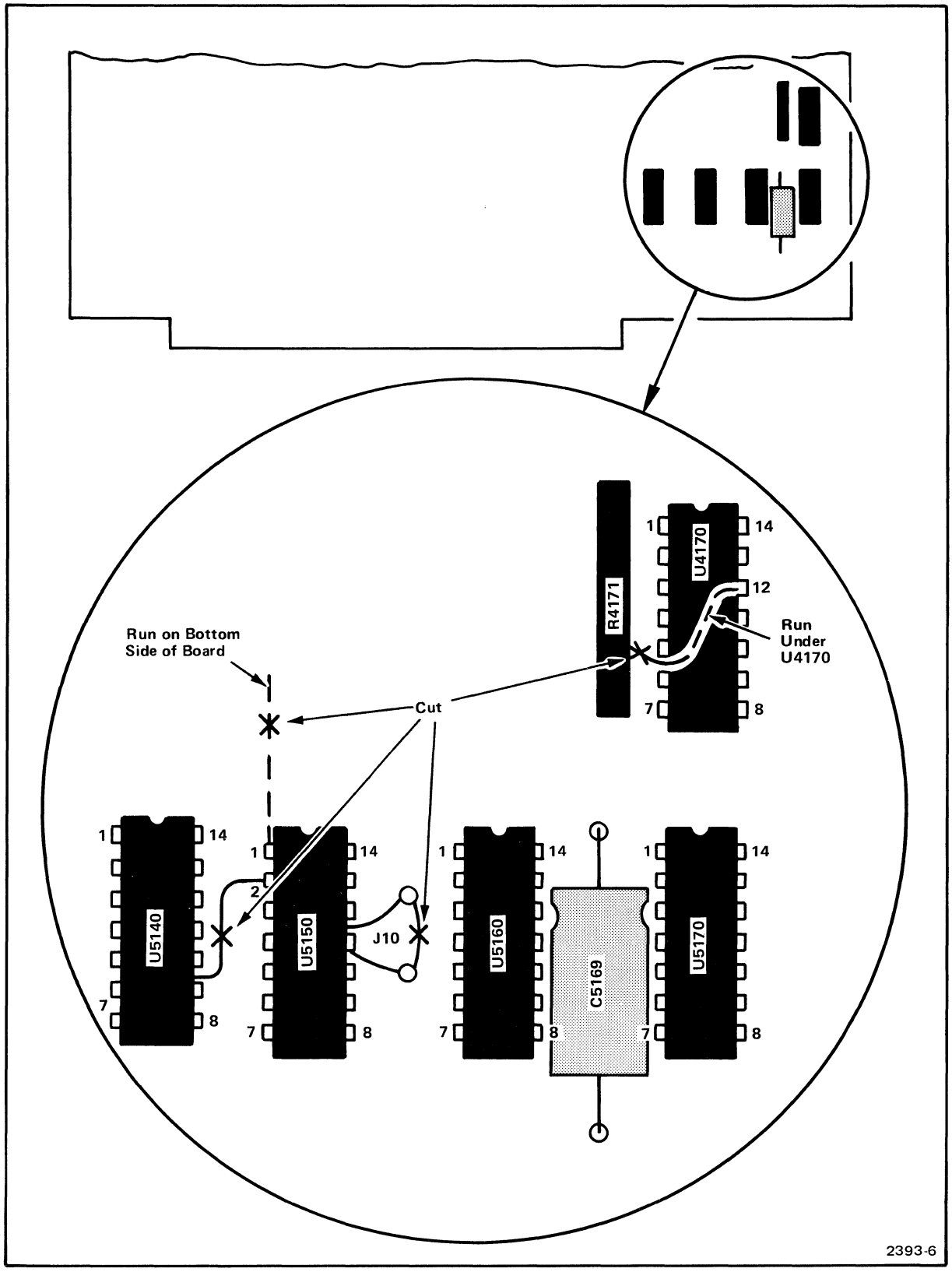


Fig. 4-4. Program Memory—9900 Word Mode Modification.

Section 5

SYSTEM COMMUNICATIONS

INTRODUCTION

The System Communications module provides two services to the 8001/8002A μProcessor Labs: external RS-232-C I/O communications, and Memory Mapping.

Three external I/O ports are controlled by the System Communications module. Each I/O port is connected to an RS-232-C compatible connector on the rear panel of the μProcessor Lab. Each port also has a specific device assignment. Table 5-1 shows a list of the connectors and their assignments. For a more complete description of the RS-232-C connectors, see the 8001/8002A μProcessor Lab Installation Guide.

Table 5-1

JACK AND DEVICE ASSIGNMENTS

Jack Number	Input Device	Output Device	Device Description
J101	REMI*	REMO*	Communications Modem
J102	---	LPT1*	Line Printer
J103	PPTR*	PPTP*	Paper Tape Reader/Punch

*Software device name.

Memory mapping allows the user to define active address space as being either in Program Memory (within the μProcessor Lab), or prototype memory, or some combination of the two.

For our discussion, the System Communications module can be divided into three functional elements:

- System I/O functions
- External I/O functions
- Memory Mapping functions

Refer to the schematic diagrams at the back of this manual while reading the following text.

SYSTEM I/O FUNCTIONS

Recall that each module in the μProcessor Lab is controlled by the System Processor module. The System I/O functions allow the System Processor to control the operation of the System Communications module.

The following circuitry is involved in the System I/O functions:

- I/O Decoder Logic
- Address Bus Buffer
- Control Bus Buffer

I/O Decoder Logic 

The I/O Decoder logic allows the System Communications module to be accessed through its system I/O ports by the System Processor module. The System Communications module is assigned I/O addresses F0—FF, although only F9—FF are used. See Tables 5-2 and 5-3.

Table 5-2

I/O DECODER ENABLE CHART

Inputs / Outputs	System Control Bus Lines					System Address Bus Lines				
			I/O Decoder Logic Enabling Inputs							
	$\overline{WRP}$	R/$\overline{W}$	$\overline{MSTR\ RUN}$	$\overline{M}$/IO	$\overline{OPREQ}$	$\overline{A13}$	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$
$\overline{Select}$ 0	x	x	0	1	0	0	0	0	1	1
Emulator Run 1	x	x	1	0	x	x	x	x	x	x
WRP 1	0	x	x	x	x	x	x	x	x	x
$\overline{R}$/W 0/1	x	1/0	x	x	x	x	x	x	x	x

x: don't care
1: high
0: low
The logic shown for the outputs is the enable state

The I/O Decoder is basically a large AND gate (see schematic 3A, left center). When all the inputs of U3040 are high, the output goes low, indicating that the System Communications module has been selected by the System Processor for operation.

All the inputs to U3040 are constantly enabled from the μProcessor Lab bus. A4—A7 indicate the I/O address range being selected (F9—FF) by the System Processor. A13 is another address range indicator generated by the System Processor. The control lines (OPERQ, $\overline{M}$/IO, and MSTR RUN) allow the System Communications module to be sure that the System Processor is running, and performing an I/O operation.

When low, the $\overline{\text{SELECT}}$ output of U3040 indicates that the System Communications module has been activated by the System Processor. $\overline{\text{SELECT}}$ is used in both the External I/O functions and the Memory Mapping functions of the System Communications module. The Memory Mapping functions are explained later in this section.

When high, the output of U2060 in the I/O Decoder logic indicates that an I/O operation is not in progress and that the Memory Mapping function can be used by an emulator processor.

Table 5-3

I/O DECODER LOGIC

I/O PORT ENABLE			LOWER ORDER ADDRESS BITS			
I/O Address	Output	Function	$\overline{A0}$	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$
FA,FB	$\overline{PS1}$ 0	Modem ACIA	x	0	1	0
FC,FD	$\overline{PS2}$ 0	Line Printer ACIA	x	1	0	0
FE,FF	$\overline{PS3}$ 0	Paper Tape Reader/ Punch ACIA	x	0	0	0
F9	$\overline{\text{MEM MAP}}$ 0	Memory Map	0	1	1	0

Address Bus Buffers 

The Address Bus Buffers (U4040, U3050) control the admission of address lines A6—A15 from the μProcessor Lab address bus to the System Communications module internal address bus. A6, A7, and A13 are constantly enabled. A8—A12, A14, and A15 are enabled only when the System Communications module is performing a Memory Mapping function. Memory Mapping is discussed in detail later in this section.

Control Bus Buffers 

The Control Bus Buffers (U4070 and U4080) are constantly enabled. Their outputs are used in both the I/O Decoder logic and the Memory Mapping Control logic.

EXTERNAL I/O FUNCTIONS

The External I/O functions control information flow between the System Communication module's three external I/O ports and the rest of the μProcessor Lab. Basically, external I/O communications are handled by three Asynchronous Communication Interface Adapter (ACIA) devices and their control logic. For this discussion, the External I/O functions will be divided into these major segments:

- I/O Port Decoder
- Bidirectional Bus Control Logic
- Bidirectional Bus Drivers
- Baud Rate Logic
- Baud Select Logic
- ACIAs
- ACIA Read/Write Clock

I/O Port Decoder 

U2040 within the I/O Port Decoder logic is used in conjunction with the Memory Map Control logic (schematic 3A, center). Recall that when the System Processor accesses internal I/O addresses F0—FF (see Table 5-2), the I/O Decoder logic (U3040, schematic 3A) asserts the $\overline{\text{SELECT}}$ line. If the Internal I/O address accessed is F9, U2040 comes into use. F9 is the internal I/O address that indicates a Memory Map operation. $\overline{A0}$—$\overline{A3}$ are constantly enabled from the μProcessor Lab bus. When the bit pattern of $\overline{A0}$—$\overline{A3}$ indicates a hexadecimal 9, U2040 generates the $\overline{\text{MEM MAP}}$ signal. $\overline{\text{MEM MAP}}$ is used in combination with $\overline{\text{SELECT}}$ to enable the Memory Mapping function. Table 5-2 illustrates the bit pattern for an access to F9 through FF.

U2030 is a BCD-to-decimal converter. Its function is to select one of the ACIA devices for operation. Depending upon the bit pattern of $\overline{A1}$—$\overline{A3}$, either $\overline{PS1}$, $\overline{PS2}$, or $\overline{PS3}$ will be asserted, enabling the port 1 ACIA (U2100), the port 2 ACIA (U2120), or the port 3 ACIA (U2130).

U2030 and U3060 detect any access to ports FA—FF. As can be seen in Table 5-2, each ACIA device has its own set of internal I/O addresses. Any I/O access to ports FA—FF will result in one of the three ACIAs being enabled.

To summarize, the I/O Port Decoder tells the rest of the System Communications module when one of the ACIAs is being accessed by the System Processor or when Memory Mapping operations have been selected.

Bidirectional Bus Control Logic 

The Bidirectional Bus Control logic directs data either from the μProcessor Lab data bus to the ACIAs, or vice versa. The NORed combination of $\overline{PS1}$—$\overline{PS3}$ and $\overline{\text{MEM MAP}}$ at U2040 indicates that one of the external I/O ports is being accessed. The output of U2040 is connected to U2070. When the System Communications module is selected ($\overline{\text{SELECT}}$ is low), and the external I/O ports are being enabled (the output of U2040 is low), the system $\overline{R}$/W line controls the direction of data flow through U4050 and U4060 (the Bidirectional Bus Drivers). When $\overline{R}$/W is low, data is transferred from the ACIAs to the system data bus. When R/W is high, data is transferred from the system data bus to the ACIAs.

Bidirectional Bus Drivers

The Bidirectional Bus Drivers (U4050, U4060) control the data flow to and from the ACIAs. Active control is provided by the Bidirectional Bus Control logic (see the preceding discussion).

Baud Rate Logic

The baud rate clocks for the ACIA devices are supplied by the Baud Rate Logic. The Baud Rate Logic can supply the following baud rates to the ACIAs:

2400 baud
1200 baud
600 baud
300 baud
110 baud

The Baud Rate Logic is basically a clock divider with five different frequency taps. The ACIA devices on the System Communications module require that the receive and transmit input frequencies (at pins 3 and 4) be 16 times the actual baud frequencies. For example, to produce a baud rate of 2400 baud, the input clock frequency must be 16 times that value, or 38.4 kHz (16 X 2400 = 38,400). A simplified block diagram is shown in Fig. 5-1.

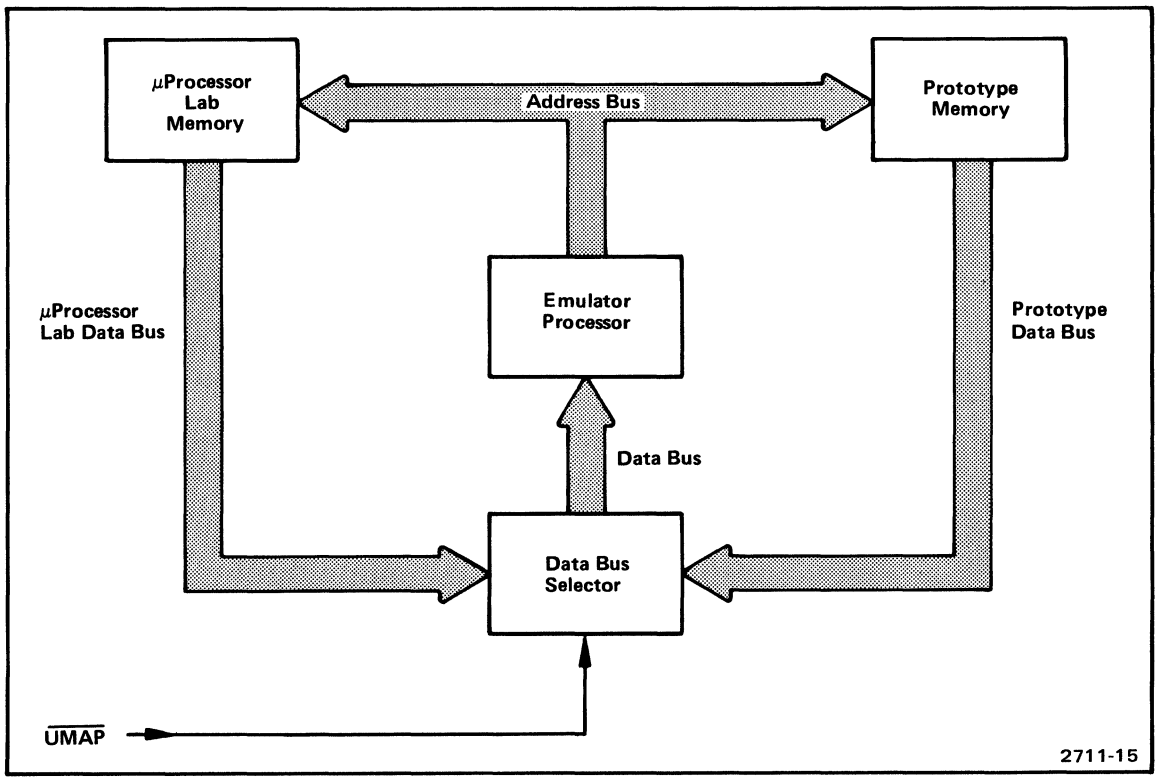


Fig. 5-1. Memory Map Functional Control.

The source of the baud clock is the 10 MHz System Clock (SYS CLK) from the µProcessor Lab bus. The 10 MHz clock is fed to a divide-by-130 network (U4110, U4120) to produce a 76.8 kHz clock. The 76.8 kHz clock happens to be 16 times the 2400 baud rate, and therefore is used as the 2400 baud clock.

The 76.8 kHz clock is also fed to an up-down counter (U3130). The up-down counter provides all

the baud clock frequencies, except the 110 baud clock. The 110 baud clock (1.76 kHz) is produced by U4130.

Baud Select Logic

The Baud Select logic is basically a series of wire jumpers that allow the user to select baud rates for each individual ACIA device.

The baud clocks generated by the Baud Rate Logic are fed to one side of a set of wire jumpers. The user can select the transmit and receive baud rates for port 1 (U2100) and for port 2 (U2120). The port 3 transmit and receive clocks are selected individually.

ACIAs

Three Asynchronous Communication Interface Adapter (ACIA) devices are located on the System Communications module. A simplified block diagram of the ACIA is given in Fig. 5-2. All three are RS-232-C compatible; however, each is configured to work with a specific device. The Modem ACIA (U2100) is configured to work best with a modem for telephone data communication. The Line Printer ACIA (U2120) will work best with a line printer. The Paper Tape Reader/Punch ACIA (U2130) works best with a paper tape reader/punch.

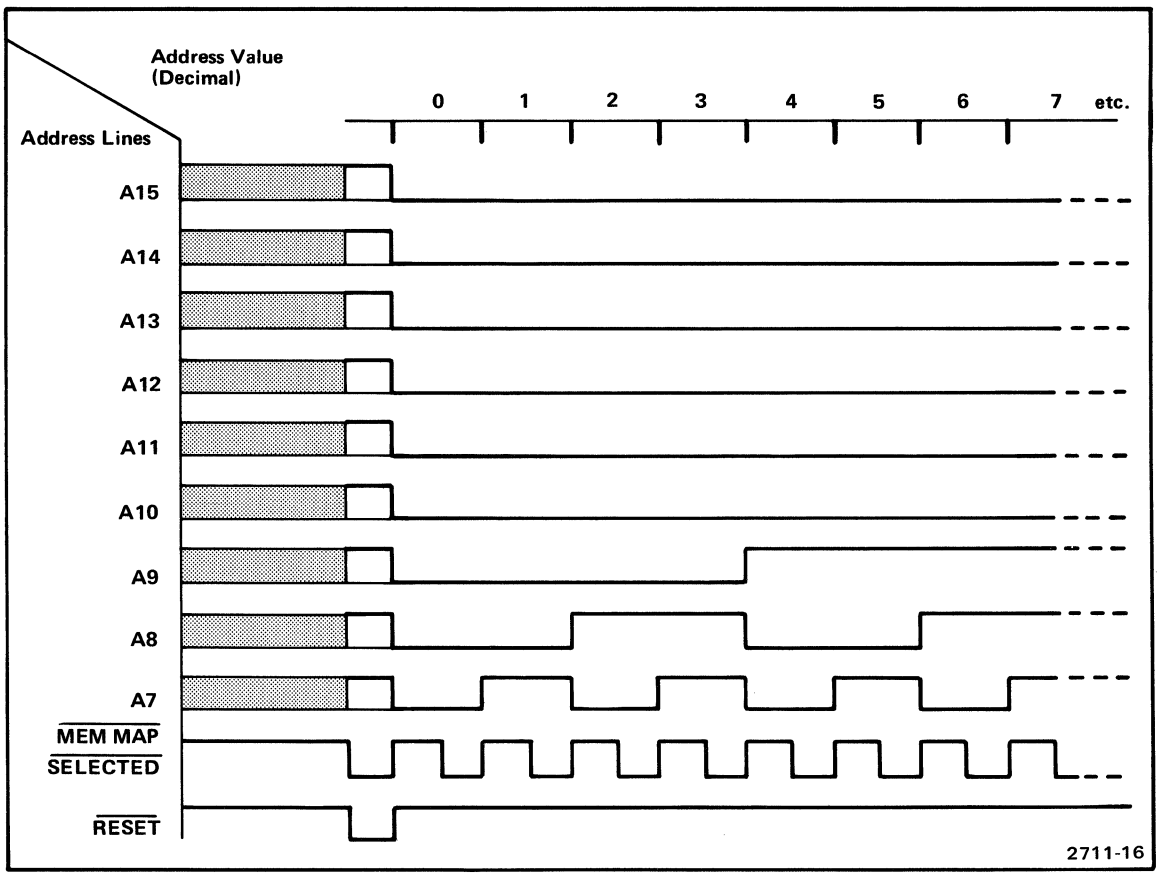


Fig. 5-2. Memory Map Address Logic Timing.

The ACIA can be viewed as a complex parallel-to-serial converter. Each ACIA externally transmits and receives data serially. When data is transmitted, the byte structure is as follows: one start bit, eight data bits, and one stop bit. Any additional stop bits received by the ACIA are ignored, and no parity bits are used. For a detailed description of the ACIA devices, refer to the appropriate manufacturer's literature.

Each ACIA is connected to its own RS-232-C jack at the rear panel of the μProcessor Lab (see Fig. 5-3). Jack J101 is usually connected to a modem. Jacks J102 and J103 can be connected to a line printer and paper tape reader/punch, respectively.

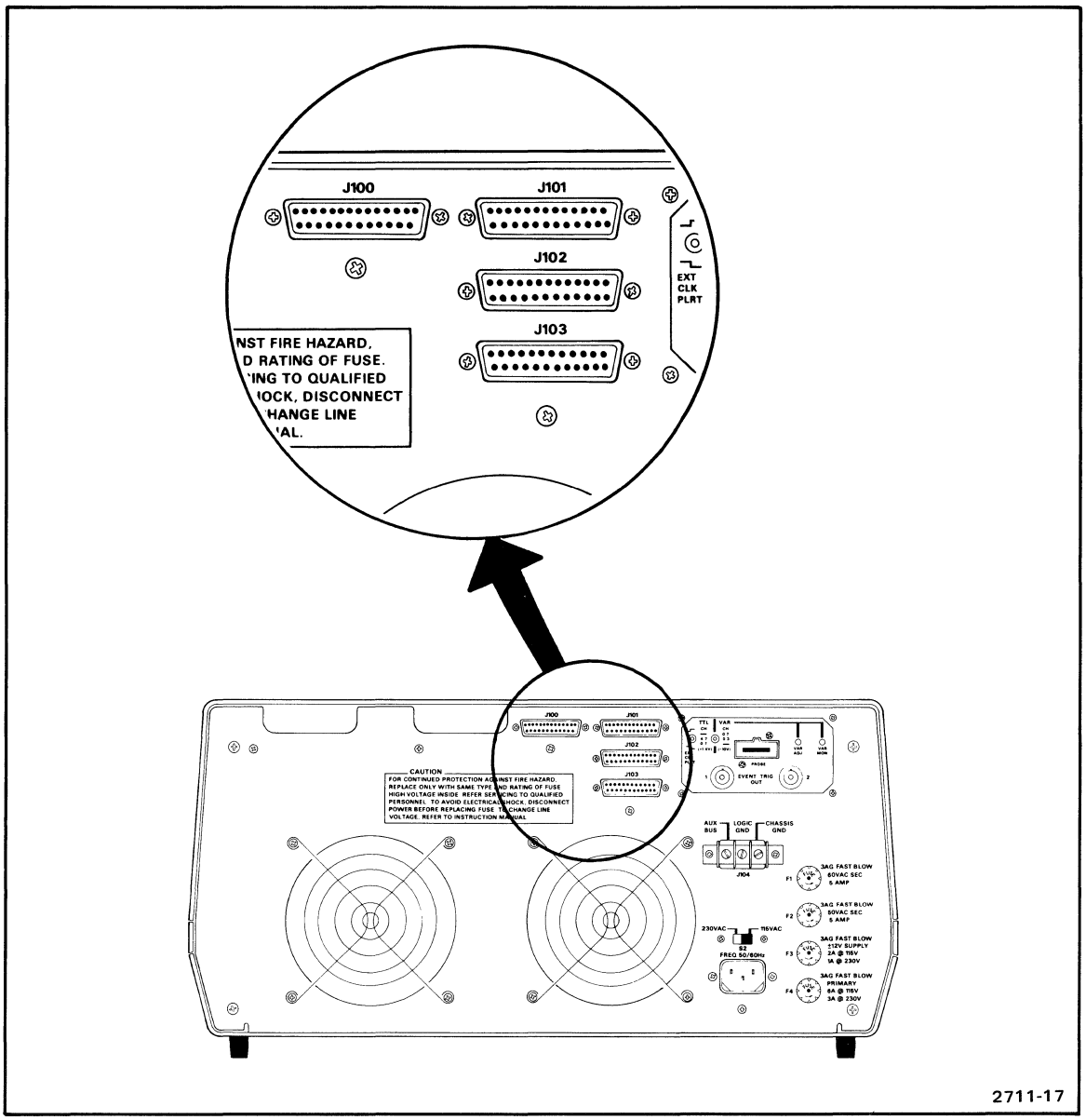


Fig. 5-3. 8001/8002A μProcessor Lab RS-232-C I/O Ports.

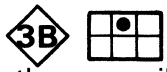
Two of the three Chip Select inputs (CS0 and CS1) on each ACIA are constantly enabled. The third input ($\overline{CS2}$) is used to select one of the ACIAs. Recall that the I/O Port Decoder (schematic 3B, upper left corner) detects when the System Processor is accessing one of the external I/O ports. The outputs of the I/O Port Decoder ($\overline{PS1}$, $\overline{PS2}$, $\overline{PS3}$) indicate which ACIA is being selected. $\overline{PS1}$ selects the Modem ACIA, $\overline{PS2}$ selects the Line Printer ACIA, and $\overline{PS3}$ selects the Paper Tape ACIA.

All three ACIAs are enabled at once by the ACIA Read/Write Clock (discussed later). Read/write control for each ACIA is provided by the R/W control line from the μProcessor Lab bus. When a read is selected by the R/W line, a pair of registers within the ACIA (receive data register and control register) are enabled. However, both registers cannot be used simultaneously. Therefore, the A0 line from the system address bus is used to select the proper register. ACIA register addressing is shown in Table 5-4.

Table 5-4

ACIA REGISTER ADDRESSING

ACIA REGISTER / I/O PORT	ACIA R/$\overline{W}$	MODEM	LINE PRINTER	PAPERTAPE READER/ PUNCH
FA	1	Status R.		
	0	Control R.		
FB	1	Receive Data R.		
	0	Transmit Data R.		
FC	1		Status R.	
	0		Control R.	
FD	1		Receive Data R.	
	0		Transmit Data R.	
FE	1			Status R.
	0			Control R.
FF	1			Receive Data R.
	0			Transmit Data R.

ACIA Read/Write Clock 

The ACIA Read/Write Clock circuitry has the responsibility of enabling the ACIAs long enough to ensure that data will remain stable while being written to or read from the μProcessor Lab data bus.

The ACIA Read/Write Clock basically consists of a dual one-shot multivibrator (U3080), and an RS flip-flop (U3070, U2080). U3080B, when triggered, has a pulse width of 120 ns. U3080A, when triggered, has a pulse width of 600 ns. These two pulses satisfy the timing requirements of the ACIAs and the System Processor.

The read/write operations of the ACIA devices will be discussed next, in order to more fully explain the operation of the ACIA Read/Write Clock and the ACIA.

ACIA WRITE

Recall that when the System Processor accesses internal I/O ports F0—FF, the I/O Decoder Logic output SELECT (schematic 3A, left center) goes low. $\overline{\text{SELECT}}$, in combination with $\overline{\text{PS1}}$, $\overline{\text{PS2}}$, or $\overline{\text{PS3}}$, clocks both one-shots of U3080. At the same time, $\overline{\text{SELECT}}$ resets the RS flip-flop (U3070).

When U3080A is clocked by $\overline{\text{SELECT}}$, its $\overline{\text{Q}}$ output goes low, generating a System Processor $\overline{\text{HOLD}}$. U3080A will maintain $\overline{\text{HOLD}}$ for 600 ns. At the same time the Q output of U3080A is NANDed together at U2080 with the $\overline{\text{Q}}$ output of U3080B. At the end of the 120 ns pulse from U3080B, U2080 generates a pulse that sets the RS flip-flop (U3070). When the RS flip-flop is set (120 ns after $\overline{\text{SELECT}}$ was applied) its output goes high, allowing data to be written into the selected ACIA when the HOLD is removed.

When $\overline{\text{HOLD}}$ is removed (600 ns following $\overline{\text{SELECT}}$), the System Processor causes the system bus line $\overline{\text{WRP}}$ to go low. The system R/$\overline{\text{W}}$ and $\overline{\text{WRP}}$ lines are NANDed together (U3070, schematic 3A, MEM MAP control logic). The output of U3070 is called $\overline{\text{WRITE}}$. $\overline{\text{WRITE}}$ resets the RS flip-flop (U2060), ending the ACIA write operation.

ACIA READ

All operations performed in an ACIA write are performed in an ACIA read, with the exception of resetting the RS flip-flop. When an ACIA read operation is completed, $\overline{\text{SELECT}}$ goes high. This action resets the RS flip-flop.

MEMORY MAPPING FUNCTIONS

Memory Mapping involves both Program Memory and the memory in a prototype system. Memory Mapping is used in the manner described below. Refer to Fig. 5-4.

Suppose that a program had been written for a prototype microprocessor-based system and had been stored in the memory of the prototype. Let's assume that a problem was found in the program and that a portion of the program had to be corrected or revised. Memory Mapping allows that portion of the program to reside in Program Memory in the μProcessor Lab. When program execution begins, the prototype will operate out of its own memory until the program area is reached. At that time, execution will switch to Program Memory for the duration of the revised portion of the program, then switch back to prototype memory.

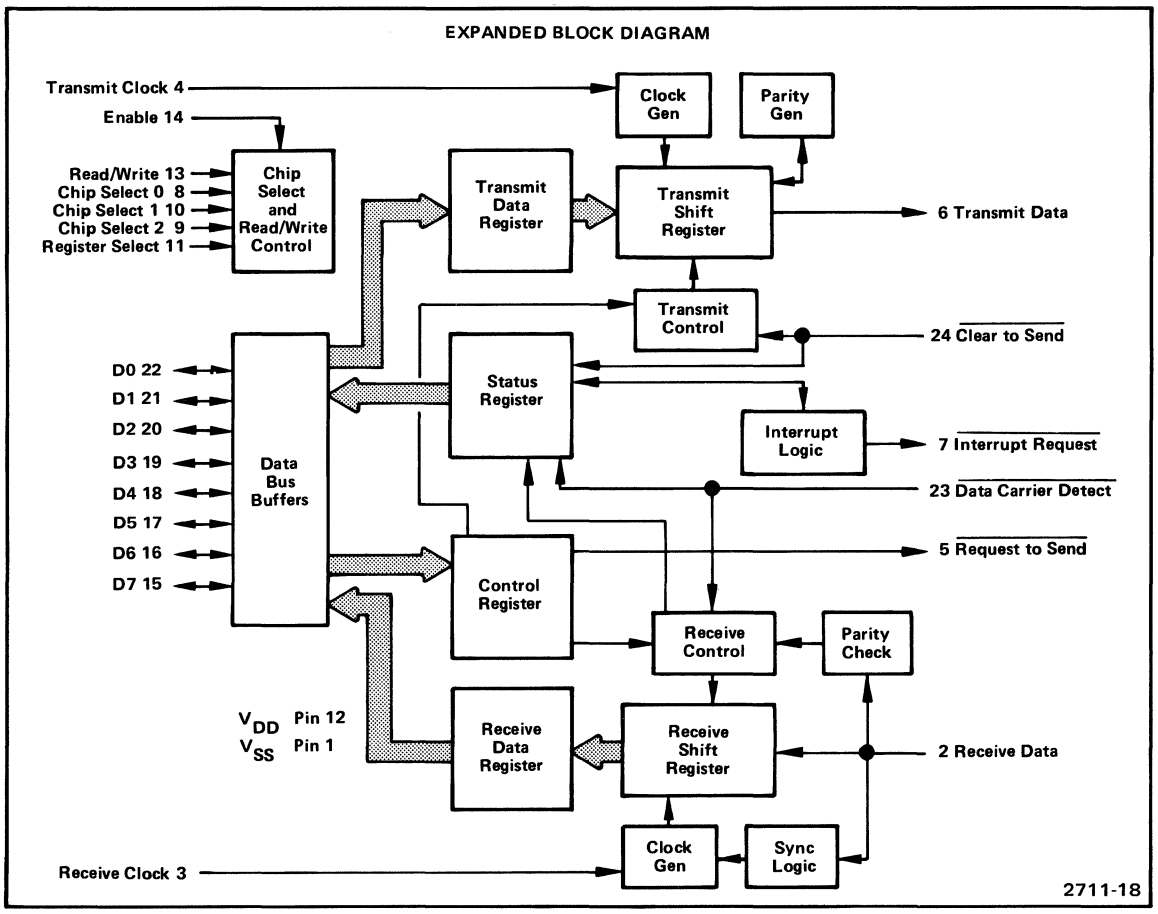


Fig. 5-4. ACIA Block Diagram.

The Memory Mapping functions of the System Communications module permit this switching operation to occur. The Memory Mapping functions can be divided into the following blocks:

- Memory Map
- Memory Map Control Logic
- Memory Map Address Logic

Memory Map

The Memory Map consists of two 256 X 1-bit RAM devices, for a total of 512 bits of storage. The Memory Map is used in the following way: The largest amount of Program or prototype memory allowed by the μProcessor Lab is 64K X 8 bits. Those 64K bytes of addressable space can be divided into 512 blocks of 128 bytes each. Each of the 128-byte blocks can be represented by one bit in the 512-bit Memory Map.

Therefore, one bit in the Memory Map can be used to define each of the 512 blocks as coming from Program Memory or prototype memory.

On the 16-bit address bus, A7—A15 define the 512 blocks of address space, each containing 128 bytes of memory. Lines A0—A6 define a particular byte within a 128-byte block of address space. For this reason, lines A7—A15 are tied to the address inputs of the Memory Map RAMs. This configuration allows the Memory Map to store one bit defining each 128-byte block. The Memory Map is written to initially by the System Processor to define each block as coming from Program Memory or prototype memory. When the Emulator Processor is executing a program, the Memory Map is constantly being read, supplying the Emulator Processor with the correct memory source for each 128-byte block.

Memory Map Control Logic

Memory Map Control Logic controls the Memory Mapping functions of the System Communications module. When the System Communications module is accessed by the System Processor, the $\overline{\text{SELECT}}$ line from the I/O Decoder Logic goes low. If the internal I/O address accessed by the System Processor is F9, the $\overline{\text{MEM MAP}}$ line (from the I/O Port Decoder on schematic 3B) also goes low. The combination of $\overline{\text{SELECT}}$ and $\overline{\text{MEM MAP}}$ is NANDed together by U2060 to produce $\overline{\text{MEM MAP SELECT}}$. $\overline{\text{MEM MAP SELECT}}$ is used in several enabling circuits.

For example, when the user enters MAP R on the system terminal, $\overline{\text{MEM MAP SELECT}}$ is NANDed at U3070 with the system bus line R/$\overline{\text{W}}$. The result is $\overline{\text{RAM}}$ RD. $\overline{\text{RAM}}$ RD enables U4080, allowing the outputs of the Memory Map RAMs to be placed on the system data bus line D0. In this way, the System Processor can display the contents of the Memory Map RAMs.

$\overline{\text{MEM MAP SELECT}}$ is also used to enable the Address Bus Buffers (schematic 3A, upper left). The buffers transfer data from the system address bus onto the Memory Map RAM address bus.

$\overline{\text{MEM MAP SELECT}}$ is also used in the $\overline{\text{RESET}}$ circuitry. $\overline{\text{RESET}}$ is generated by U3060 within the Memory Map Control Logic. When $\overline{\text{MEM MAP SELECT}}$ is high, and the System Processor initiates an internal I/O write to F9, $\overline{\text{RESET}}$ is generated. $\overline{\text{RESET}}$ is used in the Memory Map Address Logic and by the Memory Map RAMs.

Memory Map Address Logic 

Notice on schematic 3A that the Memory Map RAMs can receive addresses from one of two places: from the μProcessor Lab System bus (via the Address Bus Buffer) or from the Memory Map Address Logic. Both the System Processor and the Emulator Processor access the Memory Map RAMs, but in different ways. Figure 5-5 shows Memory Map Address Logic timing.

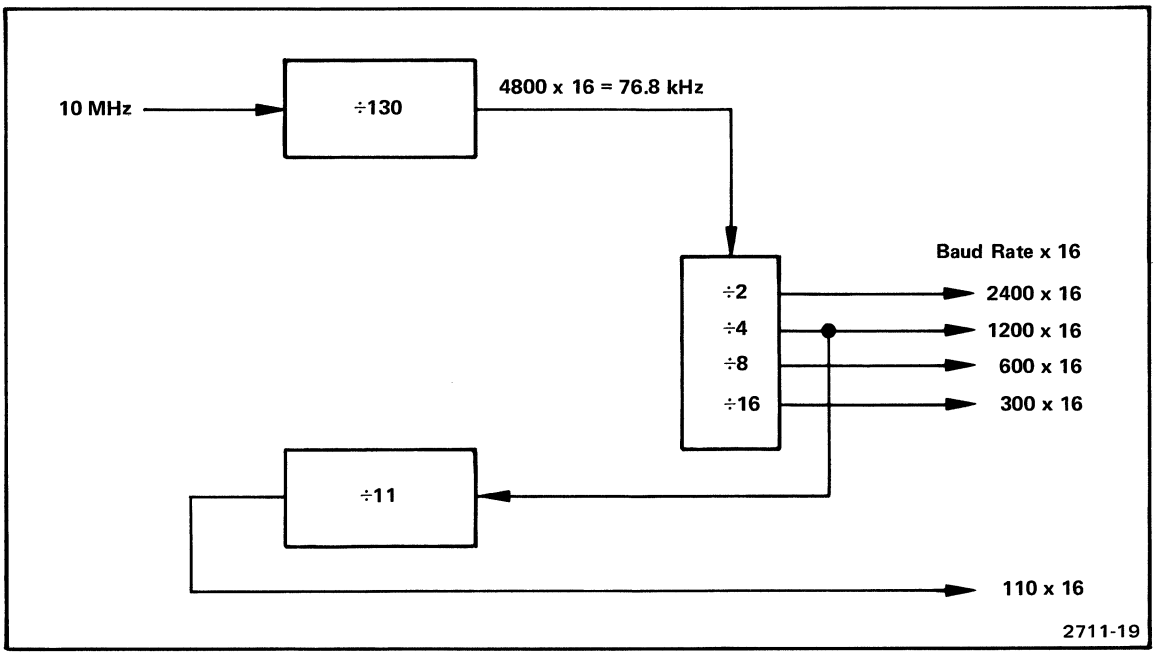


Fig. 5-5. Baud Rate Logic.

When the System Processor loads the Memory Map into the RAM devices, it starts at RAM addresses 00 and continues to RAM address FF. The actual addressing is not performed by the System Processor, however. The Memory Map Address Logic provides the addresses. The same situation occurs when the System Processor reads the Memory Map. The Memory Map Address Logic sequentially provides the RAM addresses.

Two up-counters provide the addresses. When the System Processor reads or writes to the Memory Map RAMs, it accesses I/O address F9. When F9 is accessed, the $\overline{\text{RESET}}$ line from Memory Map Control Logic is forced low. $\overline{\text{RESET}}$ initializes two up-counters (U4010, U4020). At

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the same time as $\overline{\text{RESET}}$ is forced low, $\overline{\text{MEM MAP SELECT}}$ is forced low. Notice that $\overline{\text{MEM MAP SELECT}}$ is inverted, then fed to address bus buffer U3020, and to the UP input of U4020 as COUNT. When the System Processor completes its access to F9, $\overline{\text{MEM MAP SELECT}}$ goes high, clocking the up-counter to the next RAM address to be written to or read. $\overline{\text{MEM MAP SELECT}}$ also enables the address buffer U3020.

When the active Emulator Processor is using the memory map, it provides the address directly through the Address Bus Buffer. When the Emulator Processor is running, the Memory Map RAMs are constantly fed A8—A15 from the system address bus. In this way, the Memory Map RAMs can output the UMAP signal for each address accessed by the Emulator Processor. When low, UMAP tells the Emulator Processor that the current address is to be sent to prototype memory. When UMAP is high, the current address is sent to Program Memory.

Section 6

DEBUG AND FRONT PANEL I/O MODULE

INTRODUCTION

The Debug and Front Panel I/O module performs three distinct functions within the 8001/8002A μProcessor Lab: it controls the interaction and system bus time-sharing between the System Processor and emulator processor; it supports software features such as breakpoint, trace, and emulator processor jumps to any memory location; and it provides the interface to either the Standard or Maintenance Front Panel. The Debug module is centrally located in the system bus structure, providing a dividing line between the system and program sections. Unique control lines are connected to the System Processor and emulator processor modules in each section of the bus.

Although the logic sections of the module are interrelated, they are divided here into eight major functional groups:

- System Processor/Emulator Processor Control Logic
- I/O Decoder Logic
- Debug Interrupt Logic
- Service Request Logic
- Address Trace and Compare Logic
- Debug Control Logic
- Forced Jump Logic
- Debug Module Control

For convenience, the Debug and Front Panel I/O module is hereafter referred to as the Debug module.

The Debug module schematic diagrams have been partitioned to block the related circuitry for each of the above functions.

- System Processor/Emulator Processor Control Logic assigns control to either the System Processor or the emulator processor at all times.
- The I/O Decoder Logic consists of I/O port decoding for storing breakpoint values, loading the Debug command and control bytes, and reading the stored program counter address values.
- The Debug Interrupt Logic and Service Request Logic blocks assign interrupt priority and vector-encode eight Service Request interrupts (SVCs) and eight Debug interrupts.
- The Address Trace and Compare Logic and Debug Control Logic blocks allow for storage of the emulator processor address value (program counter) during an instruction fetch of the last instruction or the present instruction. Also included are two breakpoints storage registers with address comparison logic.

- The Forced Jump Logic allows the emulator processor to be started from any memory location.
- The Debug Module Control senses all necessary Maintenance Front Panel and system bus control signals for directing the Debug Module.

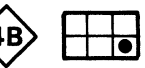
CIRCUIT DESCRIPTION

The following circuit descriptions refer to logic blocks as outlined on the schematics.

System Processor/Emulator Processor Control Logic 

GENERAL

The System Processor/Emulator Processor Control Logic directs which of the two processors is allowed to access the system address, data, and control buses. Since both processors share these bus lines, only one is allowed to run at a time. This type of system is referred to as a Master/Slave arrangement. The System Processor has a higher priority than the emulator processor because it provides control for the μProcessor Lab. For this reason, the System Processor may be referred to as the Master and the emulator processor as the Slave. The System Processor/Emulator Processor Control Logic can be divided into three parts: Master/Slave Control Logic, Master/Slave Status Logic, and Master/Slave Halt Detection.

MASTER/SLAVE CONTROL LOGIC 

The Master/Slave Control Logic (MSTR SLV CONTROL) is capable of directly pausing the System Processor and emulator processor. The control logic outputs two signals, Master Pause ($\overline{\text{MST PSE}}$) and Slave Pause ($\overline{\text{SLV PAUSE}}$). The two signals are sensed by the System Processor and emulator processor, respectively. When $\overline{\text{MST PSE}}$ or $\overline{\text{SLV PAUSE}}$ is low, the corresponding processor is paused. $\overline{\text{MST PSE}}$ and $\overline{\text{SLV PAUSE}}$ are output from two 4-input AND gates (U3160). When an input to one of these gates is low, the corresponding output is low. Therefore, each processor can be directly paused by any one of four inputs.

One line accessed by both processors is the $\overline{\text{PAUSE}}$ line. The ANDed result of the system bus line PAUSE and the Maintenance Front Panel Bus Control switch ENABLE/NORM causes both processors to be paused. When the Bus Control switch is in the ENABLE position ($\overline{\text{ACCESS}}$ is low) or when $\overline{\text{PAUSE}}$ is low, $\overline{\text{MST PSE}}$ and $\overline{\text{SLV PAUSE}}$ are forced low. Each processor stops running and the corresponding inputs to the system bus are put into a high-impedance tristate mode. The user then has access to the system address, data, and control bus lines.

One input to the $\overline{\text{SLV PAUSE}}$ AND gate (U3160A) is $\overline{\text{U PAUSE}}$. $\overline{\text{U PAUSE}}$ is an output from the prototype system. When $\overline{\text{U PAUSE}}$ is low, the emulator processor is directly paused. $\overline{\text{SLV PAUSE}}$ is forced low to prevent a System Processor interrupt from occurring. (Refer to the Master/Slave Halt Detection discussion later in this section.) When $\overline{\text{PAUSE}}$ or $\overline{\text{U PAUSE}}$ is discontinued (returns to a high state) or the control switch is returned to the NORM position ($\overline{\text{ACCESS}}$ is high), the previous run state of the processors is resumed.

Another set of inputs sensed by the pause AND gates are the direct pause lines, discussed in the following paragraphs. These inputs, and the last pair of inputs, Q and Q of the Master/Slave Flip-Flop (MSTR/SLV FF), determine which processor is allowed to run.

MASTER/SLAVE STATUS LOGIC 

The Master/Slave Status logic ensures that only one of the two processors may run at a time. This logic consists of a J-K flip-flop (U2150) that is continuously clocked by the 38.4 kHz I/O CLK. The MSTR/SLV FF senses inputs from the Maintenance Front Panel (SET SLV, SET MSTR, MSTR CPU TEST, and ACCESS), Master Halt Detector (U2130B), and the system control bus line $\overline{\text{MSTR INTD}}$.

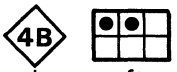
When the System Processor is interrupted ($\overline{\text{MSTR INTD}}$ is low) or when the Maintenance Front Panel CPU Control switch SYS/PGRM is in the SYS position ($\overline{\text{SET MSTR}}$ is low), the output of a corresponding two-input NAND gate (U1150D) is high. This results in the Master/Slave Control Logic forcing the $\overline{\text{SLV PAUSE}}$ output low and pausing the emulator processor.

When the system control bus line $\overline{\text{RUN}}$ goes high, the MSTR/SLV FF is allowed to change states. As long as one of the processors is running, $\overline{\text{RUN}}$ is low and the MSTR/SLV FF J and K inputs are held low and high respectively. For this reason, the MSTR/SLV FF cannot change states until both processors are out of the run mode. This guarantees that one processor is not allowed to run until the other processor is off the system bus.

When the SYS/PGRM front panel switch is set in the PGRM position ($\overline{\text{SET SLV}}$ is low), the Master/Slave Control Logic forces the $\overline{\text{MSTR PSE}}$ output low and pauses the System Processor. Again, when the system control bus line $\overline{\text{RUN}}$ is high, the MSTR/SLV FF changes state and the emulator processor is allowed to run.

The normal method for the System Processor to release the system bus and turn control over to the emulator processor is through the execution of a software HALT instruction. The Q output of the MSTR HALT FF (schematic 4B, upper left) is then set high, (This function is discussed in the next topic, Master/Slave Halt Detection.) When $\overline{\text{MSTR CPU TEST}}$ from the front panel is high (switch off), the System Processor is directly paused by forcing $\overline{\text{MST PSE}}$ low. The emulator processor is then put in control and allowed to run, as previously described. However, if $\overline{\text{MSTR CPU TEST}}$ is low, then the MSTR HALT FF Q output is masked. The MSTR/SLV FF is not allowed to change states and turn control over to the emulator processor. Both processors remain paused.

Notice that $\overline{\text{MSTR CPU TEST}}$ and the MSTR HALT FF Q output are NANDed together and result in a low output. This output is used by a NAND gate in the Forced Jump Logic (schematic 4B, upper right) to set output EN ADDR high. This forces the address bus to contain the last address executed and to allow its display by the Maintenance Front Panel.

MASTER/SLAVE HALT DETECTION 

The Master/Slave Halt Detection indicates that a software HALT instruction had been executed by the last processor in control of the system bus. The halt detectors sense the system control bus line $\overline{\text{RUN}}$ and the respective $\overline{\text{MST PSE}}$ or $\overline{\text{SLV PAUSE}}$ output from the Master/Slave Control Logic. Operation of the two halt detectors (U2130B, U3150B) is identical. Each consists of two cascaded J-K flip-flops, configured as D-types, which are continuously clocked by the 38.4 kHz I/O CLK. The first FF of each detector senses $\overline{\text{MST PSE}}$ and $\overline{\text{SLV PAUSE}}$, respectively. The RESET of each FF also senses the same input. The second FF of each detector senses the output of the first FF. The corresponding RESET inputs sense the system control bus line RUN.

When $\overline{\text{RUN}}$ is high, both processors are paused. The halt detectors sense whether $\overline{\text{MST PSE}}$ or $\overline{\text{SLV PAUSE}}$ is high. The corresponding halt detector is set after one I/O CLK cycle if $\overline{\text{RUN}}$ does not return low (indicating that a processor has accessed the system bus). Recall that the MSTR/SLV FF cannot change states unless both processors are out of the run mode. The delay of one I/O CLK cycle allows the MSTR/SLV FF to change states without indicating a software HALT condition.

A System Processor HALT is the normal mechanism for relinquishing the system bus. An emulator HALT indicates a programming error and immediately causes a System Processor interrupt ($\overline{\text{SLV HLT INT}}$).

I/O Decoder Logic

This section describes both the software and hardware functions of the I/O Decoder logic. The software functions are described first.

GENERAL

The I/O Decoder Logic allows the System Processor to access eight I/O ports. These I/O ports enable various operations that are performed between the System Processor and emulator processor. Tables 6-1A and 6-1B list the I/O port addresses and their respective software functions. The paragraphs following the tables describe each function. The hardware circuit descriptions for this section follow the function descriptions.

Table 6-1A

DEBUG MODULE OUTPUT PORTS AND FUNCTIONS

I/O PORT OUTPUT	PORT FUNCTION
F8	Command Byte
F9	Debug Control Byte
FA	Jump Addr. Low Byte
FB	Jump Addr. High Byte
FC	Breakpoint 1 Low Byte
FD	Breakpoint 1 High Byte
FE	Breakpoint 2 Low Byte
FF	Breakpoint 2 High Byte

Table 6-1B

DEBUG MODULE INPUT PORTS AND FUNCTIONS

I/O PORT INPUT	PORT FUNCTION
FC	Program Counter Last Low Byte
FD	Program Counter Last High Byte
FE	Program Counter Next Low Byte
FF	Program Counter Next High Byte

6

COMMAND BYTE

A command byte is written to port F9 by the System Processor to enable various command options. The command byte consists of five individual command bits and three unused bits. Their format is shown in Fig. 6-1. The function of each bit is described in the following paragraphs.

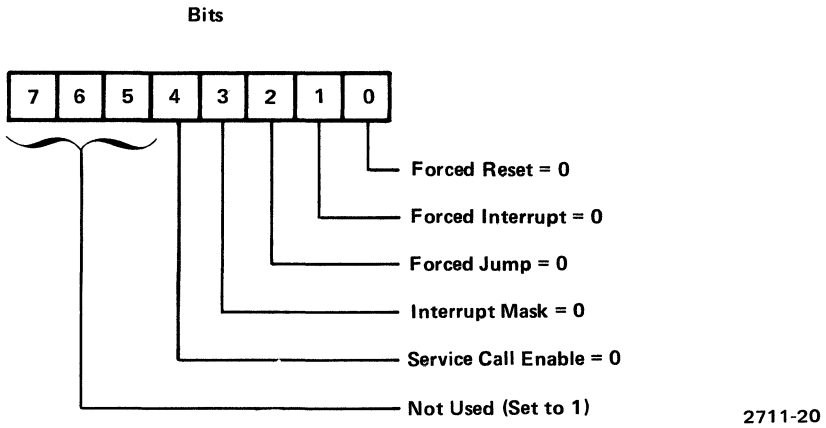


Fig. 6-1. Command Byte Format.

Forced Reset Bit—This bit causes the Debug module to reset the emulator processor. The emulator processor will start instruction execution at address 0000. This bit can be used together with the forced interrupt or forced jump bit.

Forced Interrupt Bit—This bit causes the Debug module to force an emulator processor interrupt. When the emulator processor is restarted, a forced branch instruction to address 0000 is issued.

Forced Jump Bit—This bit forces the emulator processor to branch unconditionally to the address contained in the Forced Jump Address Register located in the Address Trace and Compare Logic (schematic 4C). The register must be set before this bit is issued.

Interrupt Mask Bit—This bit prevents any Debug hardware interrupt from occurring. The masked interrupts are allowed to stack and occur when the mask bit is reset.

Service Calls Enable Bit—This bit allows the emulator processor to obtain input/output (I/O) service from the system peripherals, including the system terminal and flexible disc drives.

DEBUG CONTROL BYTE

The System Processor writes a control byte to port F8. This control byte enables the Debug mode and controls Single Cycle and Breakpoint operation. The control byte uses six individual bits. Figure 6-2 illustrates the bit format. These bits are non-exclusive; any combination may be used. Bits 0—3 correspond to Breakpoint control. Bits 0 and 2 enable Breakpoints 1 and 2, respectively, during an emulator read cycle. Bits 1 and 3 enable Breakpoints 1 and 2, respectively, during an emulator write cycle. Bit 4 enables the Single Cycle operation during the TRACE ALL command. Bit 5 enables the Debug sequence and thus allows Breakpoint and Single Cycle operation. The Debug control byte is examined in further detail in the Address Trace and Compare Logic discussion later in this section.

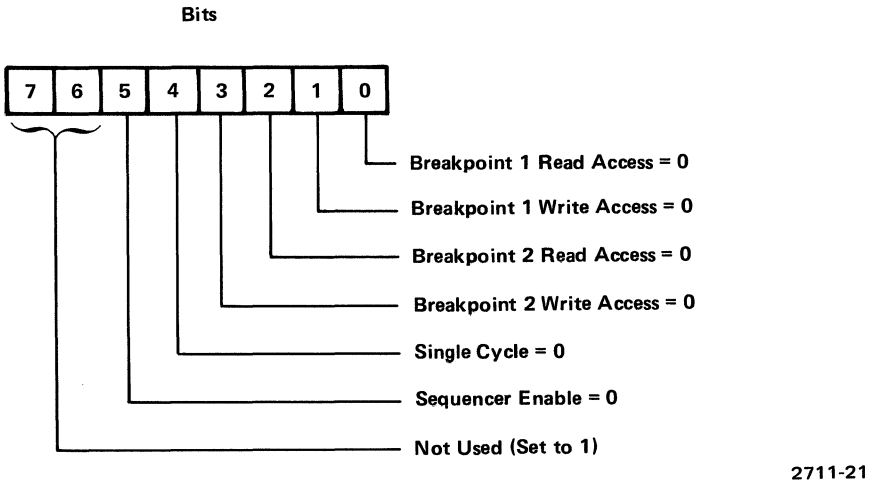


Fig. 6-2. Debug Control Byte Format.

JUMP ADDRESS BYTES

The low and high bytes of a forced jump address are loaded through output ports FA and FB and into the Forced Jump Address Register in the Address Trace and Compare Logic (schematic 4C). The forced jump address may be loaded to execute a "GO" command from the user or to jump the emulator processor to or from a trace routine.

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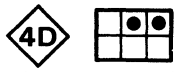
BREAKPOINT BYTES

I/O port output addresses FC and FD are the addresses for Breakpoint 1 Low Byte and Breakpoint 1 High Byte, respectively.

I/O port output addresses FE and FF are the addresses for Breakpoint 2 Low Byte and Breakpoint 2 High Byte, respectively.

PROGRAM COUNTER

Input port pairs FC, FD and FE, FF correspond, respectively, to the emulator processor program counter values of the 'last' instruction executed and of the 'next' instruction to be executed. These ports are read only during trace or after detecting a breakpoint.

CIRCUIT DESCRIPTION 

The I/O Decoder Logic generates an output, $\overline{\text{SELECT}}$, that is low when any of the ports F0—FF are accessed by either the System Processor or emulator processor. Table 6-2 shows the system address and control bus lines that enable $\overline{\text{SELECT}}$. Control line $\overline{\text{OPREQ}}$ is low when the system address and data buses are valid and can be read. Address line A13 and control line $\overline{\text{M}}$/IO are high during the execution of an I/O instruction. The address lines A4—A7 correspond to I/O ports F0—FF.

Table 6-2

I/O DECODER LOGIC

Inputs / Outputs	System Control Bus Lines			System Address Bus Lines				
	$\overline{\text{OPREQ}}$	OPREQ' (Same as $\overline{\text{OPREQ}}$)	$\overline{\text{M}}$/IO	A13	A7	A6	A5	A4
$\overline{\text{SELECT}}$ 0	1	1	1	1	1	1	1	1

1: high
0: low
The logic shown for the outputs is the enable state

Two other inputs to the I/O Decoder Logic are MSTR and system address line A3. The MSTR input is the Q output of the MSTR/SLV FF (U2150A) in the Master/Slave Status logic (schematic 4B, lower center). The MSTR line is high when the System Processor has control of the system bus. MSTR and address bit A3 are NANDed together (U1160D) to form an output which is NORed with $\overline{\text{SELECT}}$. $\overline{\text{SELECT}}$ is low and inputs MSTR and A3 are high when I/O ports F8—FF are addressed by the System Processor. The NAND result of MSTR and A3 is low, and is NORed (U1100C) with SELECT to produce a high output, Ports Enabled (PRTEN). This output corresponds to the System Processor access of I/O ports F8—FF, and is used to enable all functions related to the decoding of these I/O ports F8—FF.

System Processor output ports F9, FA, and FB are decoded by a binary-decimal decoder (U4010). Address lines A0, A1, and A2 are sensed by the decoder, along with the NANDed result of PRTEN and $\overline{WRP}$. The output of U3100B is used to enable the decoder. PRTEN is gated by the system control bus line R/$\overline{W}$ in the write mode (when R/$\overline{W}$ is low), and by the $\overline{WRP}$ line. $\overline{WRP}$ is a high-low-high timing pulse initiated by the System Processor or emulator processor during a write operation, and is used for clocking output latches and memory.

When PRTEN and $\overline{WRP}$ are high and low, respectively, the binary-to-decimal decoder is enabled. Since this decoder is enabled when I/O ports F9—FB are addressed, address bits A0—A2 represent the ports that are accessed. The decoder output line (1, 2, 3, or 4) that corresponds to the binary value of bits A0—A2 is low during the period $\overline{WRP}$ is low. The appropriate output is then used to strobe a register or flip-flop to latch the corresponding data bits.

WRITE BREAKPOINT

The Breakpoint Storage Register File is enabled when the System Processor output ports FC—FF are decoded into a write breakpoint strobe ($\overline{WRT\ BP}$ from U3110, pin 6). The Breakpoint Storage Register File is located in Address Trace and Compare Logic (schematic 4C, lower center). There are four registers in this file, which store the high and low address bytes of the two breakpoints. System address lines A0 and A1 address the file containing the register that corresponds to the output ports of the selected breakpoint (see Table 6-1). $\overline{WRT\ BP}$ is the NANDed result of PRTEN, address line A2, and system control bus lines R/$\overline{W}$ and $\overline{WRP}$. When R/$\overline{W}$ and $\overline{WRP}$ are low, and PRTEN and address A2 are high, $\overline{WRT\ BP}$ is low and the file register is enabled into the Write mode.

$\overline{I/O\ READ}$

System Processor input ports FC—FF are decoded into an input, $\overline{I/O\ READ}$ (from U3110B). This output enables the Program Counter Storage Register File (U3050) in the Address Trace and Compare Logic (U3050, schematic 4C, lower left). There are four registers in this file, which store the high and low address bytes of PC-Next and PC-Last. Address lines A0 and A1 address the file containing the register that corresponds to the input ports of the selected Program Counter (see Table 6-2). $\overline{I/O\ READ}$ is the NANDed result of PRTEN, address bit A2, and the system control bus line R/W. When R/W, PRTEN and address line A2 are high, $\overline{I/O\ READ}$ is low and the file register is enabled into the read mode.

$\overline{I/O\ WRITE}$

The NANDed result of PRTEN and the system control bus line R/$\overline{W}$ is presented as an output, $\overline{I/O\ WRITE}$ (from U3100D). $\overline{I/O\ WRITE}$ and $\overline{I/O\ READ}$ control the input/output mode of the Driver/Receiver Buffer in the Address Trace and Compare Logic (schematic 4C). $\overline{I/O\ WRITE}$ and $\overline{I/O\ READ}$ gate the data to and from the two file registers.

Interrupt Logic 

The Debug Module services up to 16 interrupts. For purposes of this discussion, these interrupts are divided into two groups. The first group of eight are Service Request interrupts (SVCs) serviced for the System Processor module. The second group of eight are debugging and Real-Time Prototype Analyzer (RTPA) interrupts. They are discussed later in this section.

The Debug Module assigns priorities to each of the 16 interrupts. First, all System Processor SVC interrupts have priority over debugging and RTPA interrupts. The priority setting circuitry will allow debugging or RTPA interrupts only if no SVCs are pending. Additionally, each set of interrupts (either SVCs or debugging) has internal priorities.

In the descriptions below, functional descriptions precede the hardware discussions.

SVC INTERRUPT LOGIC

One of the functions of the System Processor is to provide all input/output requirements for the emulator processor. The emulator processor has no provision for direct access to peripheral equipment, such as the system console. Therefore, the emulator processor requests access from the System Processor.

The emulator processor notifies the System Processor of the request by issuing a service call (SVC).

The SVC is a two-byte address included in the users software program. Six SVCs may be defined in the users software program.

As shown in Table 6-3, two of the eight SVCs are reserved for debugging operations, including dump and restore routines.

The SVC is a two-byte address. Table 6-3 illustrates the SVC format and priorities for the eight SVCs. The XX portion of the I/O address varies with the individual emulator processor.

Table 6-3
SVC FORMAT AND PRIORITIES

	SVC	Interrupt Priority	Vector Address	I/O Address
User	1	16	0020	XXF7
	2	17	0022	XXF6
	3	18	0024	XXF5
	4	19	0026	XXF4
	5	20	0028	XXF3
	6	21	002A	XXF2
Debug	7	22	002C	XXF1
	8	23	002E	XXF0

SVC HARDWARE BLOCK DESCRIPTION

The SVC logic can be divided into two sections: EMULATOR/DEBUG SVC logic and Debug INTERRUPT logic.

EMULATOR/DEBUG SVC LOGIC

The EMULATOR/DEBUG SVC logic is asserted when the emulator processor accesses I/O ports F6 or F7. The output of the EMULATOR/DEBUG SVC logic is a line called $\overline{\text{SPRTEN}}$ (from U1160A). $\overline{\text{SPRTEN}}$ is low when the emulator processor is executing an SVC instruction.

$\overline{\text{SPRTEN}}$ has two functions: to assert the Debug Interrupt Request ($\overline{\text{DBG INT}}$) signal, which is placed on the system bus; and to act as a clock input for the SVC Vector Latch (U2090).

The SVC vector latch uses address bits A0—A2 from the system address bus as inputs. When both $\overline{\text{SPRTEN}}$ and the Debug Vector Enable ($\overline{\text{DBG VEN}}$) line are asserted, the interrupting vector is transferred from A0—A2 to the internal vector address bus Q1—Q6 (in the Debug Interrupt Logic). The actual interrupt vector will be found on Q1, Q2, and Q6 (inputs to U2080A, U2080B, and U2080D). The Q5 output of the SVC vector latch is used to disable the interrupt priority encoder. The reason this is necessary will be explained later.

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DEBUG INTERRUPT LOGIC 

In addition to SVCs, the Debug module services eight interrupts that may be generated while debugging a software routine, or while using the Real-Time Prototype Analyzer. Notice in schematic 4D (bottom) that eight J-K flip-flops have their Q outputs tied to the input of a priority encoder (U2100). Each of these flip-flops corresponds to one of the eight interrupts. The six Debugging interrupt flip-flops are:

- Breakpoint 1—U2120A
- Breakpoint 2—U2120B
- Single Cycle Interrupt—U2110A
- Emulator Halt (SLV HLT INT)—U2110B
- Diagnostic Interrupt—U2140B
- Front Panel Halt—U4150B

The two RTPA interrupt flip-flops are U1080A and U1080B.

A complete listing of interrupt vectors and interrupt priorities is given in Appendix C.

When one of these flip-flops detects an interrupt, its $\overline{Q}$ output is set low. The priority encoder looks at all eight flip-flops simultaneoulsy. When more than one flip-flop is set by interrupts, the priority encoder outputs the vector for the interrupt having the highest priority.

Recall from the previous discussion that the Q5 output of the SVC Vector Latch (U2090) disables the priority encoder (U2100). Notice that the SVC Vector Latch outputs and the priority encoder outputs are both tied to the inputs of three NAND gates (U2080). When an SVC interrupt occurs, Q5 of U2090 goes high, forcing the priority encoder EI input high. This in turn causes the priority encoder to force its outputs high. This action allows the vector from the SVC Vector Latch (U2090) to be placed on the system data bus.

If no SVC interrupts are present, the priority encoder EI input is low, allowing the debug or RTPA interrupt vector onto the data bus.

Address Trace and Compare Logic 

BREAKPOINT/PROGRAM COUNTER REGISTERS

The Debug module internal 8-bit bus is connected to two register files: one register file stores breakpoint addresses, while the other register file stores program counter values. Each file stores two 16-bit words.

BREAKPOINT REGISTERS

The Breakpoint Register File is used during breakpoint operations. A breakpoint 1 address and a breakpoint 2 address are stored in the breakpoint register by the System Processor. Access to these registers is controlled by the I/O Decoder Logic (schematic 4D, upper center and right). As the user program is executed, each current address is compared with the stored breakpoint address. If an address match occurs, the emulator processor is halted.

PROGRAM COUNTER REGISTERS

The program counter register is used concurrently with the breakpoint register. As each new address is compared with the preset breakpoint address, the new address is stored in the program counter register. The address is stored in the event that a breakpoint is reached. In that case, the current program location must be saved so that program execution may continue following the break.

The Program Counter Storage Registers (U2050, U3050) contain the addresses of both the last instruction executed (P.C. Last) and the next instruction to be executed (P.C. Next). When the System Processor is interrupted, P.C. Last contains the address of the instruction that was just completed, and P.C. Next contains the address of the instruction to which emulator processor must return.

The P.C. Last Register is normally written into during an instruction FETCH when a System Processor interrupt is not pending. During an instruction at which a breakpoint occurs, a P.C. Last is written into during the instruction fetch before the breakpoint occurs. The P.C. Next Register is written into on the subsequent cycles of the next instruction.

BUS SEQUENCER 

Notice Figures 6-3A and 6-3B represent the sequence of events that occur during breakpoint comparison and program counter storage. The Bus Sequencer controls the timing of this sequence.

The Bus Sequencer is made up of four J-K flip-flops (U5100, U5110, schematic 4C, center). These flip-flops generate the basic timing sequence. The following description presents an overview of the major bus sequence states.

When the debug mode of operation is enabled, the Debug Control Byte register (U3020) output Q3 is high. This output, labeled TR, in combination with the Debug module Master/Slave circuitry (schematic 4B), enables the Bus Sequencer. (Trace Enable block, schematic 4C, upper left.) The Bus Sequencer is triggered by the leading edge of OPREQ.

During time state 1, as shown in Fig. 6-3A, the low-order byte of the system address bus is clocked onto the Debug module internal bus. This value is stored in the Program Counter Storage Registers (U2050, U3050, schematic 4C, center). At the same time, the previously stored low-order Breakpoint 1 address byte is read from its storage register (U2030, U3030 schematic 4C, center) and compared with the byte from the system address bus. The address comparator is made up of a series of exclusive-OR devices (U2040, U3040 schematic 4C, center). If the comparison is true, the result of the comparison is clocked into the first stage of a compare circuit (U4090).

During time state 2, the high-order address byte is latched onto the internal bus and written into the Program Counter Storage Registers (U2030, U3030, U2050, U3050). Concurrently, the high-order byte is compared with the upper order byte of the previously stored Breakpoint 1 address. The result of that comparison (if true) is also clocked into the compare flip-flop (U4090).

In time state 3, as shown in Fig. 6-3B, the result of the comparison is clocked into the Mask Debug Interrupt logic (schematic 4C, upper right). At the same time, the Program Counter storage and compare operation is repeated for the low-order byte of Breakpoint 2.

In time state 4, the high-order bytes are compared for Breakpoint 2.

In time state 5, the result of the Breakpoint 2 comparison is gated to the interrupt circuitry.

Time state 6 represents the reset state that stops the sequencer.

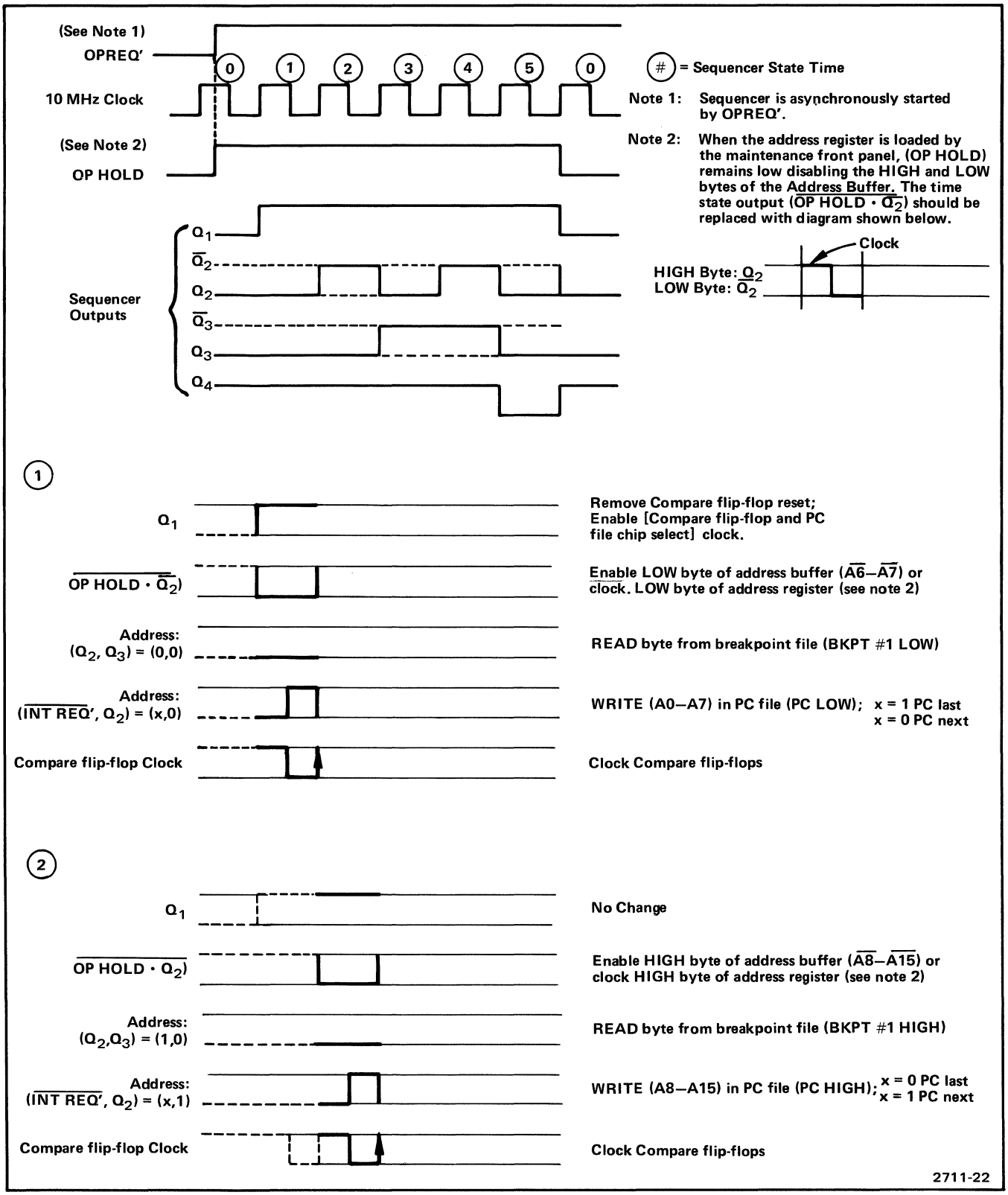


Fig. 6-3A. Sequencer State Timing Diagram.

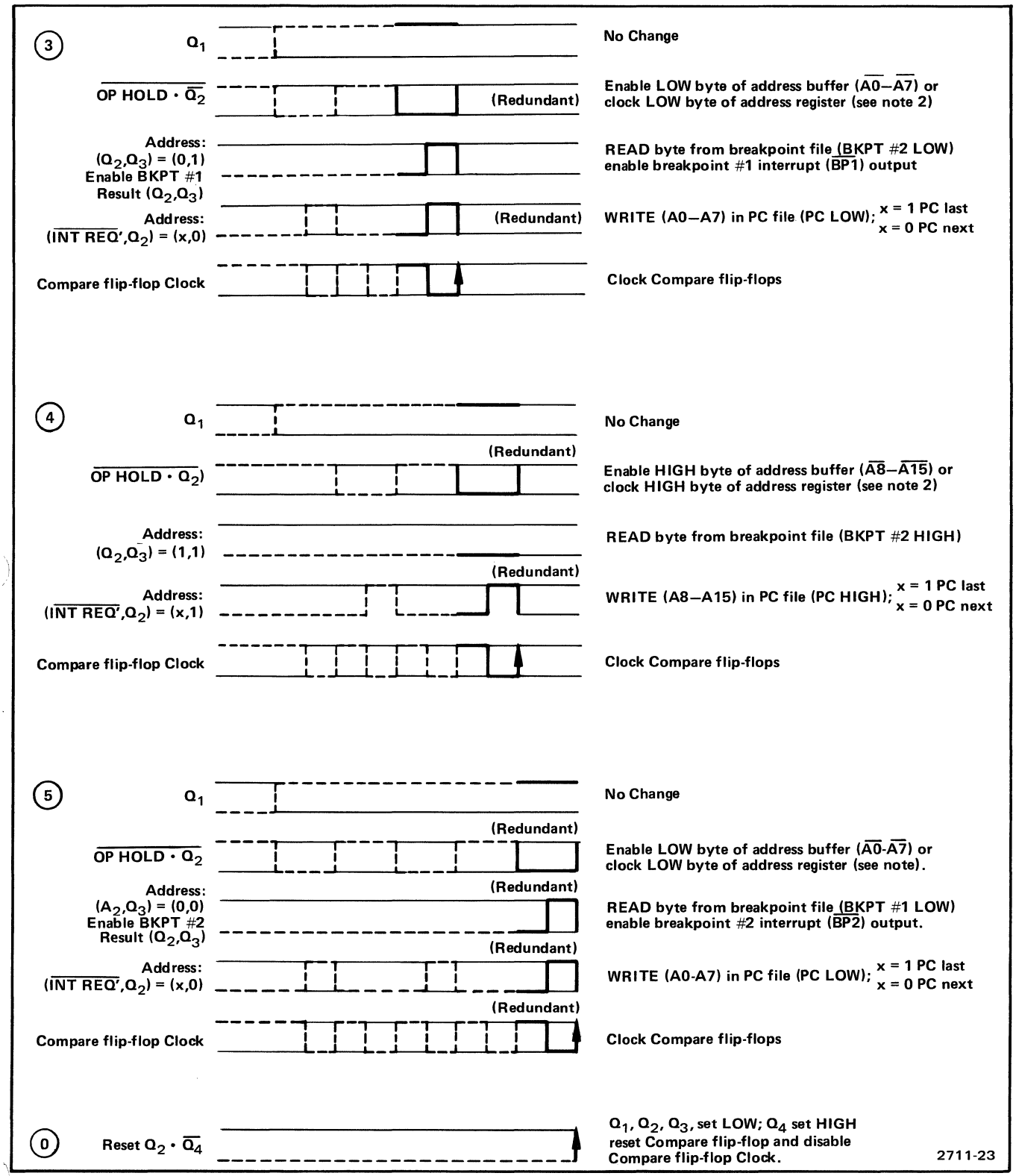


Fig. 6-3B. Sequencer State Timing Diagrams.

BREAKPOINT COMPARISON LOGIC 

During the Bus Sequencer operation, the Breakpoint Register Files are sequentially accessed for the high and low bytes of two breakpoint addresses. When each byte of the breakpoint addresses is read, it is sensed by the Address Comparator (U2040, U3040). At the same time, the internal 8-bit bus is also input to the Address Comparator. The breakpoint values are stored in the Breakpoint Register File in complementary form. Therefore, a valid comparison is made between two values that are the complement of each other. The next paragraph begins the hardware discussion.

The eight exclusive-OR gates (U3040, U2040) of the Address comparator (schematic 4C, center) are of open-collector type and are hardwired together. The output of the Address Comparator is high only if the address inputs are the complement of each other. This output is sensed by two cascaded J-K flip-flops (U4090), configured as D-type, in the Debug Control Logic (schematic 4C, upper center). Notice from the State Timing Diagram (Fig. 6-3) that these flip-flops are clocked at the end of each time state.

During time states 1 and 2, Breakpoint 1 is compared; during time states 3 and 4, Breakpoint 2 is compared. The Q output of U4090A will be high at the beginning of time state 3 or 5 if a valid comparison was made. This output is sensed by U4080, which is used to enable a multiplexer (U3010) in the Debug Control Logic. The Select input to this multiplexer is the system control bus line R/$\overline{W}$. R/$\overline{W}$ selects between two pairs of inputs latched in the Debug Control Byte Latch (U3020). These inputs are set by the user as breakpoints for Read operations, Write operations, or both. The multiplexer output is sensed by U4100, which generates the Breakpoint results (BP1, BP2). BP1 and BP2 interrupt the System Processor via the Debug Interrupt Logic (schematic 4D, lower center and right).

During time states 3 and 5, U4100 is enabled by Sequencer outputs Q_3 and $\overline{Q_3}$. During the same time state the four-input NAND gate (U4080) is enabled by Sequencer output Q_2.

The two other inputs to U4080 are the 9.984 MHz clock and the system control bus line $\overline{MEM}$/IO. It is the $\overline{MEM}$/IO line that guarantees that breakpoint interrupts occur only for memory addresses and not for addresses. Notice that the $\overline{MEM}$/IO input is sensed by U4110B, which is normally enabled. However, if a Maintenance Front Panel LOAD ADDR or TEST operation is performed, the $\overline{MEM}$/IO input is masked and U4080 cannot be enabled. During such a Maintenance Front Panel operation, breakpoint interrupts are thus disallowed.

The Forced Jump Address Register (U4020, U5020, U4030, and U5030, schematic 4C, lower right) may also be incremented or decremented by the Maintenance Front Panel INCR ADDR/DECR ADDR switch. The control signals from the Maintenance Front Panel INCR ADDR/DECR ADDR switch are sensed by $\overline{INC}$ and $\overline{DEC}$ (schematic 4C, lower left), respectively, and direct the Forced Jump Address Register.

Debug Control Logic 

The Debug Control logic coordinates the following operations: address breakpoints, emulator processor registers, and forced jump operations.

The Debug Control logic includes a multiplexer (U5010), which controls access to the Forced Jump Address Register, and the Breakpoint Compare flip-flop (U4090A), which stores the result of the breakpoint exclusive-OR comparison.

Associated with the Debug Control logic are the Debug Control Byte Latch (U3020, U3010, U4100) and the Trace Enable flip-flop (U5120C, U4120D). These two areas are discussed in the following paragraph. Following these discussions is a description of two Maintenance Front Panel switch functions that utilize the Debug Control Logic.

DEBUG CONTROL BYTE LATCH

All debugging operations are controlled by the System Processor. The System Processor issues a control byte (see Fig. 6-2), which contains all debug operating conditions. The control byte is latched into U3020 by $\overline{\text{OUT CNTRL}}$ from the I/O Decoder Logic (schematic 4C, upper right).

TRACE ENABLE FLIP-FLOP 

The Trace Enable FF is enabled by two inputs. The first input, $\overline{\text{SLV TR}}$ is the result of TR (output Q_3 of the Debug Control Byte Latch) NANDed with the inverted ANDed result of two other inputs: the Q output of the MSTR/SLV FF, and $\overline{\text{RUN}}$·ACCESS. (All of these signals are shown on schematic 4B.) This gating sets $\overline{\text{SLV TR}}$ low if the Debug mode has been enabled (TR is high) and the MSTR/SLV FF is set for a System Processor pause. Thus only the emulator processor may be traced. If the Maintenance Front Panel ENABLE/NORM switch is in the ENABLE position ($\overline{\text{ACCESS}}$ is low), the $\overline{\text{SLV TR}}$ input is forced high and the Trace Enable FF is disabled.

The second enabling input to the Trace Enable FF is $\overline{\text{MSTR CPU TEST}}$ (Maintenance Front Panel TEST switch is ON).

Maintenance Front Panel Operations

Debug Control logic and the bus Sequencer are affected by two Maintenance Front Panel operations: Maintenance Front Panel Access and Maintenance Front Panel TEST switch operations.

Refer to schematic 4C. During a Maintenance Front Panel access, the Sequencer begins operation when the LOAD ADDR switch is toggled. The Address Bus Buffer is inhibited and the low and high bytes from the Maintenance Front Panel address switches are multiplexed onto the internal bus. Instead of the Program Counter Register File (U2050, U3050) being loaded, the low and high bytes of a Forced Jump Address Register (U4020, U4030, U5020, U5030, schematic 4C, lower right) are loaded.

When the Maintenance Front Panel TEST switch is in the ON position, the Sequencer operates normally, except that the Forced Jump Address Register (U4020, U4030, U5020, and U5030) is loaded from the address bus at the same time the Program Counter Register File is loaded. Emulator processor operation is not required.

MAINTENANCE FRONT PANEL LOAD ADDR SWITCH

The Q output of the Trace Enable FF is one input to an inverting OR gate (U5120A). The other input is the Q output of the LOAD FF. The LOAD FF input is hardwired such that, when it is clocked by the Maintenance Front Panel switch LOAD ADDR, the Q output is set low. The LOAD ADDR switch is used for loading the Forced Jump Address Register (U4020, U5020, U4030, U5030) with the address value designated by the Maintenance Front Panel address switches. When either of these two inputs to U5120A is set low, the output is set high. This results in removing the Sequencer reset and following it to perform the sequence of operation discussed under the Sequencer/Breakpoint/P.C. Register Timing heading. When the sixth and last time state is reached, the AND result of Sequencer outputs $\overline{Q_2}$ and Q_4 is low and resets the Trace Enable, Program Counter, and LOAD FFs. (The Program Counter FF is discussed at the end of this topic.) The corresponding inverted OR result of the LOAD FF Q and Trace Enable $\overline{Q}$ outputs is low; this immediately resets the Sequencer flips (U5100, U5110).

When the Maintenance Front Panel LOAD ADDR switch is used, the ENABLE/NORM switch must be in the ENABLE position (ACCESS is low). As just discussed, the $\overline{\text{SLV TR}}$ input to the Trace Enable FF is set high. Once the ENABLE/NORM switch has been placed in the ENABLE position, the LOAD ADDR switch may be depressed. Two high output pulses (OPREQ' and LOAD) are immediately generated. OPREQ' clocks the Trace Enable FF; since $\overline{\text{SLV TR}}$ is high, and the Maintenance Front Panel TEST switch is OFF the Q output (OP HOLD) is set low. LOAD clocks the LOAD FF and sets its Q output low; this removes the Sequencer reset via U5120A. The Sequencer is thus allowed to run until it generates the next reset condition. Recall that outputs Q_2 and $\overline{Q_2}$ of the Sequencer are used to enable the low and high bytes of the address buffer when OP HOLD is high (see Fig. 6-3). Notice that Q_2 and $\overline{Q_2}$ are input to two NAND gates (U4100C, U4100D) which are enabled by OP HOLD. Since OP HOLD is low, the NAND gate inputs are forced high and the address buffer remains disabled.

Outputs Q_2 and $\overline{Q_2}$ of the Sequencer are also input to U5090 (schematic 4C, upper center) together with the 9.984 MHz clock. The U5090 outputs are used by the Multiplexer (U5010) to control access to the Forced Jump Address Register (U4020, U5020, U4030, U5030, schematic 4C, lower right). The two U5010 outputs are used to clock the low and high byte registers of the Forced Jump Address Register.

The second set of inputs to the Multiplexer are generated by the I/O Decoder Logic (schematic 4D). These signals correspond to the low and high byte registers of the Forced Jump Address Register. Thus, the System Processor may load the Forced Jump Address Register directly (with a software GO command). The Multiplexer is normally enabled to allow the I/O Decoder Logic to access the Forced Jump Address Register.

Remember that the LOAD FF Q output is set low (enabling the Sequencer via U5120A) and Sequencer output Q_1 is set high when the sequence of operations begins. It is the NAND result of these two inputs that directs the Multiplexer to select the Sequencer—10 MHz clock inputs.

The Maintenance Front Panel logic enables the high and low bytes of the address switches onto the internal 8-bit bus sequentially via the F.P. Address Buffer. This operation is controlled by Sequencer output Q_2. Output $\overline{Q_2}$ is inverted by U2070A (schematic 4C, upper right) and called $\overline{\text{LD SEL}}$. When $\overline{\text{LD SEL}}$ is low, the high address byte is selected. When $\overline{\text{LD SEL}}$ is high, the low address byte is selected.

MAINTENANCE FRONT PANEL TEST SWITCH

When the Maintenance Front Panel TEST switch is in the TEST position ($\overline{\text{MSTR CPU TEST}}$ is low) and the Trace Enable FF is clocked by OPREQ', OP HOLD is set high. Recall that $\overline{\text{MSTR CPU TEST}}$ and the Q output of the Load FF are ORed together (U5120D). The Multiplexer (U5010) is enabled to select the Sequencer—10 MHz clock input when either input to U5120D is low. Therefore, when the Maintenance Front Panel TEST switch is in the TEST position, the Forced Jump Address Register is loaded with the address on the system bus. This operation occurs independent of which processor is running.

A second function of the TEST switch is to mask the result of the MSTR HALT FF (U2150A, schematic 4B) when the System Processor executes a software HALT instruction. The emulator processor is prevented from running because the MSTR/SLV FF cannot change states, due to the mask (see System Processor/Emulator Control Logic). Also recall that the NAND result of the Q output from the MSTR HALT FF (U2150A) and an inverted $\overline{\text{MSTR CPU TEST}}$ force the address bus to contain the last address executed. This allows the Maintenance Front Panel to display the address.

To summarize, when the Maintenance Front Panel TEST switch is placed in the TEST position, a System Processor software HALT instruction can become a breakpoint, and the display of the last address executed by either processor may be displayed. At that point, both processors remain paused.

Forced Jump Logic 

GENERAL

The Forced Jump Logic allows the emulator processor to be started from any memory location. A forced jump is initiated by any one of several sources: during single cycle operation, at either breakpoint, through the Maintenance Front Panel, or by a System Processor I/O command. The Forced Jump logic is located partially on the emulator processor and partially on the Debug module.

The emulator processor contains a jump sequencer and data multiplexing logic which, when triggered, substitutes an unconditional branch for the next instruction fetched. The jump sequencer controls the high and low bytes of the jump address that is placed on the emulator processor data bus. This jump address is stored in the Forced Jump Address Register on the Debug module (schematic 4C, lower right). On System Processor I/O commands, the jump address is loaded and a jump command trigger is given to the emulator processor. During the jump sequence, the Debug module places the jump address on the system address bus for use by the emulator processor.

CIRCUIT DESCRIPTION

The operation of the Forced Jump Logic is discussed in the following paragraphs. First this discussion describes how the emulator processor is force-jumped by a System Processor I/O command. Single cycle, breakpoint, and Maintenance Front Panel forced jumps are discussed thereafter.

The System Processor normally relinquishes control to the emulator processor by executing a software HALT instruction. Recall that when control is turned over to the emulator processor, the status of the MSTR/SLV FF (U2150A, schematic 4B, lower center) is changed; the Q output goes low. This output is labeled MSTR. MSTR is inverted and sensed by U5140C (schematic 4A, left center). The other input to U5140C is the Q output of the Forced Jump Enable FF (schematic 4A, center left). The System Processor enables this flip-flop by the command byte output to port F8 as described in the I/O Decoder Logic. Therefore, if the Forced Jump Enable FF is enabled, MSTR is presented as the output from U5140C. Otherwise, the output is high. The output of U5140C is fed to U1120.

When control is turned over to the emulator processor, MSTR goes low and the output of U1120 goes high. The resulting low-to-high transition clocks the SLV JMP INIT FF (U2150B, schematic 4A, center). This flip-flop is hardwired such that when it is clocked, its Q output ($\overline{\text{SLV JMP INIT}}$) goes high. $\overline{\text{SLV JMP INIT}}$ is latched into U4160B (schematic 4B, upper right) by the 10 MHz SYS CLK. The resulting Q output (SLV JMP) is inverted, fed to U1070 (schematic 4A, upper right), and output as a Jump Command ($\overline{\text{JMP CMD}}$) to the emulator processor control bus. (The second input to U1070 has the same effect but is caused by the RTPA module.) Together, these two flip-flops (U2150B, U4160B) generate a 100 ns $\overline{\text{JMP CMD}}$ which arms the jump mechanism of the emulator processor. Notice that SLV JMP is ORed with the system $\overline{\text{RESET}}$ line and, therefore, resets the SLV JMP INIT FF when it is high. This sets $\overline{\text{SLV JMP INIT}}$ low and causes SLV JMP to be set low on the next rising edge of the 10 MHz clock.

After receipt of the 100 ns Jump Command, the emulator processor generates a forced branch instruction on the data bus during the next instruction fetch. On the leading edge of the following OPREQ (in which the Emulator receives the high byte of the jump address), $\overline{\text{JMP ACK}}$ is generated. $\overline{\text{JMP ACK}}$ is sensed by U5160 (schematic 4B, upper right). The resulting output (EN ADDR) is high when $\overline{\text{JMP ACK}}$ is low. EN ADDR enables the tristate address buffer (schematic 4C, lower right). This allows the latched address output by the Forced Jump Address Register to be placed onto the system address bus. The emulator processor multiplexes the high and low bytes of the address bus onto its data bus as required for the particular JUMP instruction. The emulator processor then resets $\overline{\text{JMP ACK}}$.

Single Cycle Interrupt

SINGLE STEP ENABLE LOGIC 

During the single cycle mode of operation, the emulator processor is paused after execution of a single instruction, and the System Processor is interrupted. When paused, the emulator processor stops after fetching the first byte of the next instruction. Since it is necessary to jump the emulator processor to a register dump routine without any intervening instructions, the

forced unconditional branch command must be received before the emulator processor stops. The System Processor then takes control and loads the Debug module Forced Jump Address Register with the jump address. The System Processor then halts, reenabling the emulator processor, which jumps to the register dump routine.

CIRCUIT DESCRIPTION

The Single Cycle enable logic (schematic 4A, center right) consists of a flip-flop (U5130) enabled by the System Processor control byte (see I/O Decoder Logic). An emulator processor Fetch clocks U5130, setting the Q output ($\overline{\text{S/CY INT}}$) low. This causes a System Processor interrupt, which automatically pauses the emulator processor at the end of a single instruction. Notice that $\overline{\text{S/CY INT}}$ is also fed to U1120 (schematic 4A, center) which is used in the Forced Jump Logic to initiate the emulator processor forced jump. The emulator processor thus receives a $\overline{\text{JMP CMD}}$ and forces the emulator processor to receive an unconditional jump instruction before it is paused.

Notice that when a $\overline{\text{JMP ACK}}$ is issued, a Jump Pending flip-flop (U4150A, schematic 4B) is set. The $\overline{\text{Q}}$ output (JMP PEND) is used to mask the SIN/CY EN bit from the Debug Control Byte Register. The next single cycle interrupt is inhibited due to the fetch of the next instruction (unconditional jump).

6

Maintenance Front Panel and Breakpoint Forced Jump Logic 

The Maintenance Front Panel switch JUMP and the breakpoint interrupts (BP1, BP2) cause a forced jump operation identical to that previously described. A forced jump is initiated by U1120 (schematic 4A, center) whenever any of its inputs go low. If the input is a breakpoint (BP1 or BP2) the System Processor is also interrupted. The emulator processor is paused after it receives the unconditional jump instruction. The System Processor loads the jump destination into the Forced Jump Address Register (U4020, U5020, U4030, and U5030, schematic 4C) and then returns control to the emulator processor. The emulator processor completes its jump to the desired location. The Maintenance Front Panel jump destination must be loaded into the Forced Jump Address Register via the LOAD ADDR switch before the JUMP switch is depressed.

Debug Module Control

The Debug Module Control logic senses the system bus and Maintenance Front Panel control signals that direct the operation of the Debug Module. An understanding of these control signals and the corresponding functions clearly defines the operation of the Debug Module Control Logic. A listing of the system bus signals is given in Appendix A.

Section 7

8001 SYSTEM MEMORY MODULE

INTRODUCTION

The 8001 System Memory module contains the operating system software (TEKOPS) for the 8001 μProcessor Lab. This module consists of 6K bytes of ROM (Read Only Memory) for the operating system, 2K bytes of RAM (Random Access Memory), and can contain sixteen 2K-byte banks of bank-selectable ROM. More ROM may be gained by installing up to three more memory modules, each containing the sixteen 2K-byte banks of selectable ROM.

An additional 1K bytes of PROM are available to allow the 6K-byte operating system or the bank-selectable ROM to be patched. Patches are made to update, or to fix firmware errors. Patch PROM Logic is discussed later in this section.

The 8001 System Memory module will be discussed in the following order:

- Select Logic
- Address Decoder
- Read/Write Control Logic
- Hold Logic
- Bank Switch Logic
- 2K RAM and Parity Control Logic
- Patch PROM Logic
- 6K ROM and Patch Address Logic
- Patch Address Identifier

CIRCUIT DESCRIPTION

Select Logic

IO/SYSTEM MEMORY DECODER 

The IO/System Memory Decoder detects when the System Processor is accessing System Memory. The IO/System Memory Decoder converts addresses A13—A15 and the appropriate system control signals to either an Input/Output ($\overline{IO}$, U2010A) or System Memory ($\overline{M}$, U1020B) signal. When the System Processor is accessing an input/output port, the $\overline{IO}$ line is low. When the System Processor is accessing System Memory, the $\overline{M}$ line is low.

Address Decoder 

The Address Decoder converts addresses A10—A13 to a signal that enables the selected memory field. Table 7-1 shows the address bit patterns for each of the four memory fields.

Table 7-1

8001 SYSTEM MEMORY ADDRESS SELECTION

Address Bits \ Memory Field	6K ROM	2k RAM	Patch ROM	Bank Switch ROM
A10	X	X	1	X
A11	0 1 0	1	0	0
A12	0 0 1	1	1	0
A13	0	X	1	1

X: don't care

Read/Write Control Logic 

The Read/Write Control Logic controls the input/output mode of the Bidirectional Data Bus Buffer (U5060, U5070 schematic 5A, lower left) to System Memory. When M is low, the Read/Write Control Logic allows the $\overline{R}/W$ signal to control the Bidirectional Data Bus Buffer. When $\overline{M}$ is high, the Buffer is in the input mode. When the Bank Switch ROM is accessed, the Buffer is controlled by Board Select (BD SEL). The Bank Switch ROM (schematic 5D) consists of one to four modules. The selected module of Bank Switch ROM will generate a BD SEL (Board Select) signal. The BD SEL is sensed by the Read/Write Control logic. When BD SEL is high, signals $\overline{M}$ and $\overline{R}/W$ control the operation, as previously described. If BD SEL is low and the Bank Switch ROM has been addressed, the Bidirectional Bus Buffer is in the input mode.

Hold Logic 

The Hold Logic is reserved for future needs but is not used at this writing.

Bank Switch Logic 

Bank Switch Logic allows selection of a 2K-byte bank of ROM from one of up to four modules; each module consists of 16 banks. The individual bank is selected by the System Processor. The System Processor issues a 6-bit (B0—B5) Bank Select command to I/O port C8.

The I/O port decoder (U5100B, U5110A; schematic 5D, upper left) detects the I/O address write and generates a write strobe. The write strobe latches the Bank Select command in the bank select register (U2070). The module selector (U2100) decodes bits B4 and B5 of the Bank Select command into the BD SEL signal, which enables the selected module. The 0 output of U2100 is

selected if only one System Memory module is used. If more than one System Memory module is used, each has a unique output. For example, the second System Memory module would use output 1 of U2100 to generate BD SEL.

Bit B3 of the Bank Select command is used by the upper/lower bank selector (U2080, U2090) to enable either the upper eight or lower eight banks on the selected module. The Bank Decoder uses bits B0—B2 to select one of these eight banks. Refer to Table 7-2.

Table 7-2

BANK SELECTION

Function / Bits	Module	Upper/Lower Banks		Bank Select							
	0 1 2 3	Banks 0-7	Banks 8-15	8 0	9 1	10 2	11 3	12 4	13 5	14 6	15 7
B0	– – – –	–	–	0	1	0	1	0	1	0	1
B1	– – – –	–	–	0	0	1	1	0	0	1	1
B2	– – – –	–	–	0	0	0	0	1	1	1	1
B3	– – – –	0	1	–	–	–	–	–	–	–	–
B4	0 1 0 1	–	–	–	–	–	–	–	–	–	–
B5	0 0 1 1	–	–	–	–	–	–	–	–	–	–

The upper/lower bank selector is controlled by the $\overline{\text{BK SW ROM}}$ line. When the Bank Switch ROM is addressed, $\overline{\text{BK SW ROM}}$ goes low and bit B3 from the bank select register is decoded. The selected bank is then addressed.

2K RAM and Parity Control Logic

The 2K RAM consists of two 1K X 9-bit memory fields. Each field is made up of two 1K X 4-bit RAMs and one 1K X 1-bit RAM. Two 4-bit devices are used to make up a 1K X 8-bit RAM, with a 1-bit device used as parity RAM. When the 2K RAM is addressed, the RAM decoder (U1050, U2050) uses address A10 to select one of the two 1K X 9-bit memory fields.

2K RAM WRITE

During a Write operation, data D0—D7 is stored in the selected 1K RAM and is sensed by P1—P8 of the parity generator (U2110). The R/$\overline{\text{W}}$ control line is in the Write mode (low) and keeps bit P9 of the parity generator high. When the parity line EVEN OUT is high, even parity is sensed. If EVEN OUT is low, odd parity is sensed. The generated parity is stored in the parity RAM (U1070 or U1080).

2K RAM READ

During a Read operation, data D0—D7 is read by the System Processor and sensed by P1—P8 of the parity generator. The parity bit from the parity RAM is inverted and sensed by P9 of the parity generator. The parity line EVEN OUT should always be low when checking parity. The status of EVEN OUT is latched by the parity interrupt logic (U1040A, U2040D) at the end of a read cycle. If EVEN OUT is high, an interrupt is generated, indicating non-valid data.

Generation of a Parity Interrupt causes the Priority Interrupt Encoder on the System Processor module to put an interrupt vector onto the system data bus. This interrupt vector is converted by the interrupt vector decoder (U5080, U2030, and U2020) into a signal used in resetting the parity interrupt logic (U1040A, U2040D).

Patch PROM Logic 

The 8001 System Memory module contains the TEKOPS operating system. If, in the future, it becomes necessary to alter a small segment of the operating system, Patch PROM Logic will support the modification.

Basically, when an error needs correction, a PROM programmed with the correction can be plugged into location U3020. Then, whenever the bad area of memory is accessed, the Patch PROM would be enabled, thus replacing the bad portion of System Memory.

6K ROM and Patch Address Logic 

The patch PROM (U3020) allows the 6K ROM or Bank Switch 32K ROM to be altered. The Patch Address selector (PAS, U4010) allows the Patch Address Identifier (PAI, U4020, U4030) to monitor either the Bank Switch ROM or the 6K ROM address space.

The Patch Address Selector (U4010) is controlled by the Bank Switch (BS) signal line from the Bank Switch Logic. When BS is high, the Bank Switch ROM addresses (B0—B3) are selected. When BS is low, the 6K ROM addresses ($\overline{\text{6K ROM}}$, A1, A11, A12) are selected.

Patch Address Identifier 

A Patch Address Identifier (U4020 and U4030) is preprogrammed to identify an address to be patched. When the address is identified, a preprogrammed byte is presented by the Patch PROM Address Logic (U5010 and U5020) to the Patch PROM. The Patch PROM then generates the corrected data.

The Patch Address Identifier consists of two Field Programmable Logic Arrays (FPLA) in parallel (U4020 and U4030). Each FPLA can be viewed as a conditionally addressable memory, identifying preprogrammed address combinations. This FPLA can scan a total address field of up to 16K 14-bit words and select 48 eight-bit preprogrammed bytes within that address space. Using two FPLAs in parallel allows a total of 96 address patches to be made. Programming of the FPLAs is done at the factory.

When the Patch Address Identifier identifies an address to be patched, a preprogrammed data byte is output as F0—F7. Bit F7 controls the patch PROM selector; when bit F7 is high, the Patch PROM may be addressed directly by the System Processor. When bit F7 is low, the Patch PROM is addressed by bits F0—F5 and addresses A0—A2. The 6K ROM and Bank Switch ROM are selected when bit F7 is high. When bit F6 is high, it complements address A2. Complementing A2 allows for a high density of patches in the patch PROM.

Section 8

HIGH-SPEED MEMORY MODULE

INTRODUCTION

The High-Speed Memory module provides Random Access Memory (RAM) for the 8001/8002A μProcessor Lab. The High-Speed Memory module is used as Program Memory for the 8001 and 8002A μProcessor Labs, and as System Memory for the 8002A μProcessor Lab. The 8001/8002A μProcessor Lab will accept up to four Program memory modules (64K bytes of memory).

The High-Speed Memory module RAM is arranged into a 16K X 9-bit word configuration. The ninth bit is used as a parity bit.

The High-Speed Memory module is used as 8002A System Memory by changing a few switch settings and adding one PROM. These switch settings are discussed later in this section. The PROM contains a bootstrap program, which initializes the system and loads TEKDOS from flexible disc into System Memory when the system is first turned on or is reset. The PROM replaces the first 256 bytes of RAM.

The High-Speed Memory module is designed for use with byte-oriented emulator processors. By configuring two modules as a pair (providing 16 data bits), the High-Speed Memory may be used with 16-bit word-oriented emulator processors.

The High-Speed Memory module is described in the following order:

- Module Configuration
- RAM Memory
- PROM Memory
- Data and Parity Control
- Address Control
- Module Configuration Logic
- Refresh Request Logic
- Operation Control and Timing

MODULE CONFIGURATION

The High-Speed Memory module is configured for use as System or Program Memory and for byte or word mode through the use of six switches. The functions of each switch are given in Table 8-1. Tables 8-2 and 8-3 summarize address selection options. Switch S4140 is shown on schematic 6A.

Table 8-1

SWITCH FUNCTIONS FOR MODULE CONFIGURATION

S4140-1	A15	Switch in the ON position indicates that the module will respond to memory addresses in which A15 = True, provided all other selection conditions are met.
S4140-2	A14	Switch in the ON position indicates that the module will respond to memory addresses in which A14 = True, provided all other selection conditions are met. When two or more memory modules are used in the byte mode, module addresses are determined by the A14 and A15 switches. If a system is set up with 32K of memory (two modules), module A will be configured with both A14 and A15 switches OFF; module B will have switch A14 ON and switch A15 OFF. Module A will contain addresses 0000H-3FFFH, module B will contain addresses 4000H-7FFFH. Since switch A14 of module A is set for OFF, all addresses with address bus lines A14 False and A15 False will enable module A; all addresses with A15 False and A14 True will enable module B. When only two modules are used (32K), all addresses above 7FFFH will cause a memory space error message to occur.
S4140-3	Byte/ Word	Switch in the ON position configures the module to serve as one module in a 16-bit word mode pair. The module will provide either bits D0—D7 or bits D8—D15 of the 16-bit data bus, depending on the setting of switch S4140-6. If switch S4140-3 is in the ON position, S4140-1 (A15) is ignored.
S4140-4	Sys/ Prog.	Switch in the ON position configures the module for operation in the Program side of the μProcessor Lab. Switch in the OFF position configures the board for 8002A System Memory operation.
S4140-5	PROM	Switch in the ON position indicates that a 82S115 PROM is installed at location U7050, as required for 8002A System Memory operation.
S4140-6	HI/LO	Switch in the ON position configures the module to provide bits D8—D15 of a 16-bit data bus. If the switch is set in the OFF position, the board will provide bits D0—D7 of the 16-bit bus. This switch works in conjunction with switch S4140-3. When the module is not used as part of a 16-bit word mode pair, the switch must be set in the OFF position.

Table 8-2
MODULE ADDRESS SWITCHES

Program Memory Module	Memory Address	Switches	
		A15	A14
A	0000 – 3FFF	OFF	OFF
B	4000 – 7FFF	OFF	ON
C	8000 – BFFF	ON	OFF
D	C000 – FFFF	ON	ON

Table 8-3
SYSTEM/PROGRAM MEMORY CONFIGURATION

Switch	Switch Setting For System Memory Use	Switch Setting For Program Memory Use
S4140-4 (SYS/PROG)	OFF	ON
S4140-5 (PROM RESIDENT)	ON	OFF

8

Table 8-2 shows the address range assigned to each Program Memory module. When more than one module is used in a system, the settings of switches S4140-2 determine the address range of each module. For example, when the system is configured for 48K or 64K of Program Memory, the third module would have switch S4140-1 in the ON position and switch S4140-2 in the OFF position. The memory address range of this third module would be from 8000H—BFFFH.

Table 8-3 shows the setting of switches S4140-4 and S4140-5 for System Memory and Program Memory use.

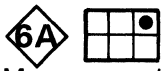
CIRCUIT DESCRIPTION

RAM Memory 

Data is stored in an array of 4K X1-bit RAM devices on the High-Speed Memory module. The memory array is composed of four banks of eight devices each. The module thus provides 16K X 8 bits of Random Access Memory (RAM).

Each 16-pin RAM device uses six multiplexed address lines, MA0—MA5, to address the 64 internal rows and 64 internal columns. Another address line, MA6, is the Chip Select ($\overline{CS}$) line to each device. The seven lines MA0—MA6 are generated by an Address Control circuit that derives them from A0—A13 of the system address bus. This Address Control circuit is explained later in this section.

The RAM devices on this module are thus addressed by six lines, rather than the 12 address lines used by many types of memory devices. Two clocks, RAS and CAS, are used to activate the devices. Each of the four banks of devices is enabled by its respective row address strobe ($\overline{RAS0}$, $\overline{RAS1}$, $\overline{RAS2}$, or $\overline{RAS3}$) and by its column address strobe ($\overline{CAS1}$ or $\overline{CAS2}$). $\overline{CAS1}$ and $\overline{CAS2}$ each clock two of the four banks of devices.

PROM Memory 

When the High-Speed Memory module is used as 8002A System Memory, the bootstrap PROM (U7050) replaces the first 256 bytes of RAM. This 256-byte PROM stores the routine that initializes the system and loads TEKDOS from the Flexible Disc Unit into System Memory at a power-up or system reset.

For use as System Memory, the High-Speed Memory module is inserted in the System side of the μProcessor Lab (usually slot J7); the System/Program switch (S4140-4) is turned OFF; and the PROM Resident switch (S4140-5) is turned ON. (See Tables 8-1 and 8-3.)

The PROM (U7050) is addressed by lines A0—A7 of the system address bus. Data from the bootstrap PROM is output through the module data bus lines D0—D7.

When the module is configured for Program Memory, the PROM circuitry is essentially removed from the circuit, and the PROM itself may be removed from the module.

Data and Parity Control

Data to and from the memory module is routed and checked for parity by the Data and Parity Control circuitry.

DATA WRITE 

The High-Speed Memory module receives data lines D0—D15 from the μProcessor Lab system bus. These lines are received and buffered by transceivers U6070 and U6080 (for lines D0—D7), and U6090 and U6100 (for D8—D15). Only lines D0—D7 are used with byte-oriented emulator processors.

Two memory modules are required for 16-bit word-oriented emulator processors. In word mode, one module is designated as the low-byte module (the lower eight bits, D0—D7) and the other as the high-byte module (the upper eight bits, D8—D15). In byte mode, or as low byte of word mode, the buffers for D0—D7 are enabled by Write Low ($\overline{WL}$) to receive data from the system data bus; the buffers for D8—D15 are held in the high-impedance state. As high byte of word mode, the D0—D7 buffers are held in the high-impedance state, while those for D8—D15 are enabled by Write High ($\overline{WH}$) to write in data.

DATA READ 

Data is read out of memory by addressing the desired bank of RAM. The selected data is read into data registers U6040 and U6030 (schematic 6C) through lines D0—D7 from the RAM devices. The data is retained in the registers until the LATCH pulse occurs. Data is latched through the registers to the data bus buffers (U6070, U6080, U6090, and U6100, schematic 6B, left) on data lines LATCH 0—LATCH 7. If the module is being used in byte mode or as low byte of word mode, Read Low (RL) will enable U6070 and U6080 to output the data on D0—D7. A module configured for high byte of a word mode pair will output the data on D8—D15. Data on D8—D15 is output through data bus buffers U6090 and U6100. Data bus buffers U6090 and U6100 are enabled to output data to the bus by Read High (RH).

PARITY 

To assure that data stored in memory is valid, the stored data is checked by the parity circuitry. The parity circuitry of the High-Speed Memory module generates, stores, and checks parity of data input to the module. The following paragraphs describe the operation of the parity logic.

As data is written into RAM, R0—R7 are sampled by the parity generator (U6110). The even-sum output of the parity generator is stored in four RAM devices (U2020, U3020, U4020, and U5020), of the same type as those of the RAM Memory array. Each of these four devices corresponds to one of the four banks of the RAM memory array. These devices are addressed in the same manner as the selected bank of RAM. Data in, however, is from the parity generator rather than the system data bus.

When a bank of RAM is selected to be read, the corresponding parity bit RAM will also be read. The parity bit RAMs are read directly to the parity checker (U6020), while the data memory is first read into the data latches (U6030 and U6040) and then into the parity checker. The parity checker (U6020) compares Latch 0—Latch 7 with the parity bit, checking for even parity, to determine data validity. A High at the odd-sum output (pin 6) of the parity checker indicates even parity and that the stored data is valid.

If the parity checker finds odd parity, the odd-sum output will go Low, indicating a parity error. The output of the parity checker is connected as an input to the parity error detector flip-flop (U5160B). If the signal from the parity checker is Low, the parity error flip-flop will toggle when clocked by Parity Strobe (PAR STR, a signal from the timing circuitry of the module, schematic 6D). The output of this flip-flop will be the parity error signal.

PARITY ERROR SIGNAL

The parity error signal performs two tasks. The first task is to remove reset from flip-flop U5160A, allowing it to receive Master Interrupt Acknowledge (MST INTACK). The second function of the parity error signal is to cause an interrupt to be generated by the module.

PARITY INTERRUPT

The parity error signal is input from U5160B to the parity error multiplexer (U5150). The multiplexer outputs are selected by $\overline{\text{PMEM}}$ (from the Module Configuration circuitry, schematic 6A). $\overline{\text{PMEM}}$ indicates that the module is configured for Program Memory use and causes the multiplexer to select the A inputs. When the module is configured for System Memory, B inputs are selected. The multiplexer will produce the parity error signal either as a Master Interrupt 1, $\overline{\text{MST INT1}}$ (when the module is used as System Memory) or Master Interrupt 3, MST INT3 (when the module is used as Program Memory). When the System Processor receives the interrupt, it will respond with an interrupt vector on the data bus, and will produce a Master Interrupt Acknowledge ($\overline{\text{MST INTACK}}$) to acknowledge the interrupt.

The interrupt vector on the data bus is decoded by the interrupt decoder (U6120A schematic 6C, center). The decoder has four inputs: R1; the wired-OR function of R4, R5, and R6; D3; and D2 or R2 (depending on the module configuration). When the decoder receives either interrupt vector 0002 (in System Memory) or 0006 (in Program MMemory) from the system, a flag reset signal is generated, and input to flip-flop U5160A. Upon receiving the $\overline{\text{MST INTACK}}$, U5160A will toggle, setting U5160B to remove the parity error signal. This circuitry does not correct the parity error; its function is only to detect the error and signal the System Processor.

Refresh Clock

The parity multiplexer also generates a signal, Refresh Clock (REF CLK). REF CLK is not related to parity, but is used by the Refresh Request circuitry. Refresh operations are discussed later in this section.

Address Control 

The Address Control logic controls address lines A0—A15 to accomplish module selection, byte/word shifting, and refresh operation on the High-Speed Memory module. Row address clocks $\overline{\text{RAS0}}$—$\overline{\text{RAS3}}$ are generated within the Address Control circuitry.

In byte mode operation, the address lines have the following responsibilities:

A14 and A15 select the module. (Up to four Program Memory modules may be present in the μProcessor Lab.)

A12 and A13 select one of the four 4K banks of RAM on the specified module.

A0—A11 select addresses within the specified 4K banks of RAM on the module.

Address bus lines A0—A15 are input to address bus multiplexers (U6130, U6140, U6150, and U6160). Lines BA0—BA15 are output by the multiplexer. When a 16-bit word-oriented emulator processor is used, two Program Memory modules are required. However, the address lines are the same as for byte mode operation.

If memory has been configured for 16-bit word operation, and is then accessed by an 8-bit byte-oriented processor, the modules of the word pair are addressed in alternating fashion. Table 8-4 shows that when two memory modules are used as a word pair with a 16-bit emulator processor, both modules respond to the same address. When those two memory modules are used with an 8-bit emulator processor, however, they respond in an alternating fashion to each address. Both modules access only the low data byte. Alternation between modules of the word pair is designated by a HI/LO bit, which enables either the high-byte module or the low-byte module. For byte-oriented access of a word pair, A0 is used as the HI/LO bit, rather than as an address bit. To use A0 as the HI/LO bit all address lines must be shifted down. The shift is performed by the address multiplexers. A1 becomes A0 (BA0), A2 becomes A1 (BA1), etc. A0 becomes the HI/LO bit (BA15), alternating the addressing between modules. During a front panel access, no address line shift takes place; HIGH BYTE (line BA15) is used for HI/LO selection. The shift is caused when the module is configured for word mode and the system bus $\overline{\text{WD ACCESS}}$ line indicates that a byte-oriented emulator processor is running.

Address lines BA0—BA13 are input to the single-device address multiplexer and refresh controller (U4120). This multiplexer/controller provides the seven multiplexed address lines MA0—MA6 to the RAM devices. The multiplexer/controller also serves as the refresh counter and multiplexer for the RAM memory devices. It presents the 7-bit refresh address to the memory devices during a refresh cycle.

BANK SELECTION 

Selection of one of the four banks of memory devices on the module is controlled by address lines BA12 and BA13. The block decoder (consisting of decoder U3130A and gates U2130 and U2120) decodes BA12 and BA13 into four signals which enable the RAMs. (A third signal is input to decoder U3130A; this signal inhibits the output when the bootstrap PROM is being accessed.)

The decoder (U3130A) creates four signals from the two address inputs. The four signals are input to four 3-input NAND gates (U2120) along with RAS1 and RAS2 from the Operation Control and Timing circuitry (schematic 6D, upper right). The outputs of the NAND gates are $\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{RAS2}}$, and $\overline{\text{RAS3}}$; these four row address strobes enable the RAM banks. A $\overline{\text{REFOP}}$ signal (from schematic 6D, upper right) enables all four strobes simultaneously during a refresh cycle.

PROM Select Decoder 

The PROM Select Decoder logic is also part of the Address Control circuitry. The PROM Select Decoder (U7140, schematic 6A, center) receives address lines $\overline{A8}$—$\overline{A13}$, M/IO, and $\overline{PMEM}$ to detect System Memory PROM addresses. The PROM RESIDENT switch indicates whether the PROM (containing the bootstrap routine) is installed. If the module is configured for 8002A System Memory use and the first 256 bits of memory are addressed, all inputs to the PROM Select Decoder will be High, indicating that the PROM has been addressed. The decoder (U7140) will then generate the signal, PROM, through U5170A to inhibit the RAM enable clocks and enable the PROM.

Module Configuration Logic 

Recall that the High-Speed Memory module may be used as either Program Memory or 8002A μProcessor Lab System Memory, in byte mode or word mode, and multiple modules may be used to expand Program Memory. The High-Speed Memory module can be programmed for any of these choices through the use of switch settings and the Module Configuration logic.

The Module Configuration logic basically consists of a multiplexer (U4160), a comparator (U4150), and a decoder (U3130B). Remember that the user sets S4140 to specify the kind of operation required. These switch settings, in conjunction with certain control lines, determine the operating parameters for the High-Speed Memory module.

MULTIPLEXER

The multiplexer (U4160) is controlled by a SELECT line, the NANDed combination of the Word Memory switch and the Program Memory switch. The Program Memory switch acts as the qualifier in this case. (See Table 8-4.) If the S4140-4 is closed, the multiplexer A and B inputs are selected by the Word Memory switch. The A inputs are selected if S4140-3 is open. If S4140-3 is closed, the B inputs are selected.

Table 8-4

MODULE ADDRESSING IN WORD MODE

	16-bit Emulator Processor	8-bit Emulator Processor	
	Data	Data	
	LO Module & HI Module 0 15	LO Module 0 7	HI Module 8(0) 15(7)
ADDRESS	0000	0000	0001
	0001	0002	0003
	0002	0004	0005
	0003	0006	0007
	0004	0008	0009
	0005	000A	000B

The 1Y output of multiplexer U4160 indicates whether the module is in word mode or byte mode. The 2Y output indicates whether the module, if in word mode, is addressed by a byte-oriented or word-oriented processor. This is indicated by the state of the $\overline{\text{WD ACCESS}}$ line from the motherboard. The 4Y output indicates a byte-oriented access, when high. When 4Y is low, the output is WD ACCESS.

COMPARATOR

The switch settings of S4140 and the conditions of other control lines are used by the select comparator (U4150) to generate the SELECT signal. Four comparisons are made in order to determine that the module is being accessed.

First, $\overline{\text{CMEM}}$ (input A1) from the motherboard is compared with S4140-4 (input B1). Both inputs must be in the same state for comparison to occur. Second, internal address line BA14 is compared with the A14 switch setting of S4140. Third, S4140-1 is compared with the 1Y output of the multiplexer (U4160). Fourth, BA15 is compared with the High Byte switch (S4140-6).

The $\overline{\text{M}}$/IO line from the motherboard indicates whether memory is indeed being accessed, and is thus used to determine if a comparison should be made. If all comparisons are true, the select comparator generates the SELECT signal.

DECODER

The third component of the Module Configuration logic is the data buffer enabling decoder (U3130B). The decoder uses two inputs to determine which buffers are to be enabled. The A input to the decoder is the WRITE line from the timing circuitry (schematic 6D, lower right). The B input is NANDed combination of the 4Y output of U4160 and the exclusive OR of $\overline{\text{SWAP}}$ and S4140-6. $\overline{\text{SWAP}}$ is used only with the 9900 Emulator Processor module.

A truth table for the decoder appears on schematic 6A.

Refresh Request Logic 

To keep stored data valid, the RAMs must be refreshed sufficiently often. This is accomplished by meeting the device refresh requirements: one row address of the individual RAM device must be refreshed every 31.25 μs; all six row addresses must be refreshed every 2 ms. The Refresh Request logic insures that sufficient cycles occur, and that they occur at times when memory is not otherwise being used. Figures 8-1 and 8-2 show refresh timing relationships.

A refresh request cycle begins with the falling edge of the I/O CLOCK. (See Fig. 8-1.) A NOR combination of the I/O CLOCK and 19.2 μs division of SYS CLK clocks the refresh pending flip-flop (U3180A). Refresh Pending establishes the conditions that determine the output of the refresh request flip-flop (U7150). The refresh request flip-flop will generate a Refresh Request when clocked. Refresh Clock (REF CLK), from the Data and Parity Control circuitry, is the clock for the refresh request flip-flop. REF CLK is dependent on whether the module is used as Program Memory or 8002A System Memory.

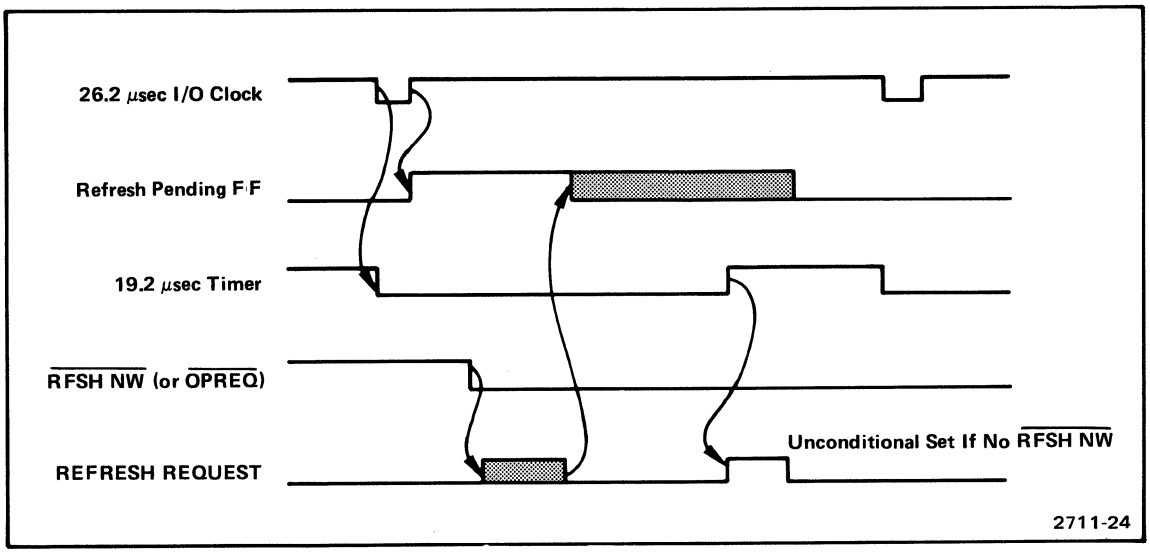


Fig. 8-1. Refresh Timing for High-Speed Memory.

If REF CLK does not trigger a Refresh Request within 19.2 μs of I/O CLOCK, a 19.2 μs timer will cause an asynchronous refresh to occur. The timer, made up of a counter (U2180) and an AND gate (U5180A), divides the 10 MHz SYS CLK down to a 19.2 μs pulse. The rising edge of the 19.2 μs pulse (see Fig. 8-2) will cause the refresh request flip-flop (U7150) to unconditionally generate Refresh Request. The timer insures that the dynamic memory will be refreshed to keep data valid when the system is accessed by the front panel, the System Processor or emulator processor is halted, or a REF CLK is not received for some reason.

The 19.2 μs timer pulse is also gated through U7180C with Refresh Pending and an inhibiting line from timing control. The purpose of this gate is to ensure that a refresh is pending and that other operations involving memory cycles have been completed before an asynchronous refresh is requested. Whether synchronous or asynchronous, Refresh Request is input to the Operation Control and Timing circuitry to initiate the refresh cycle.

Operation Control and Timing Logic

The Operation Control circuitry receives requests for refresh, read, and write operations, resolves contention between them and generates the timing signals for refresh, read, and write operations. Access time of the High-Speed Memory is 215 ns (worst case). Figure 8-3 shows the timing relationships.

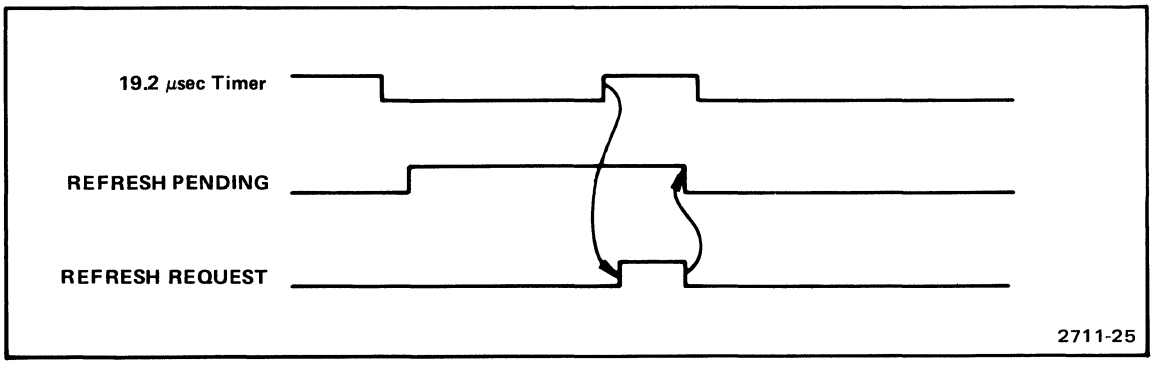


Fig. 8-2. Asynchronous Refresh Timing for High-Speed Memory.

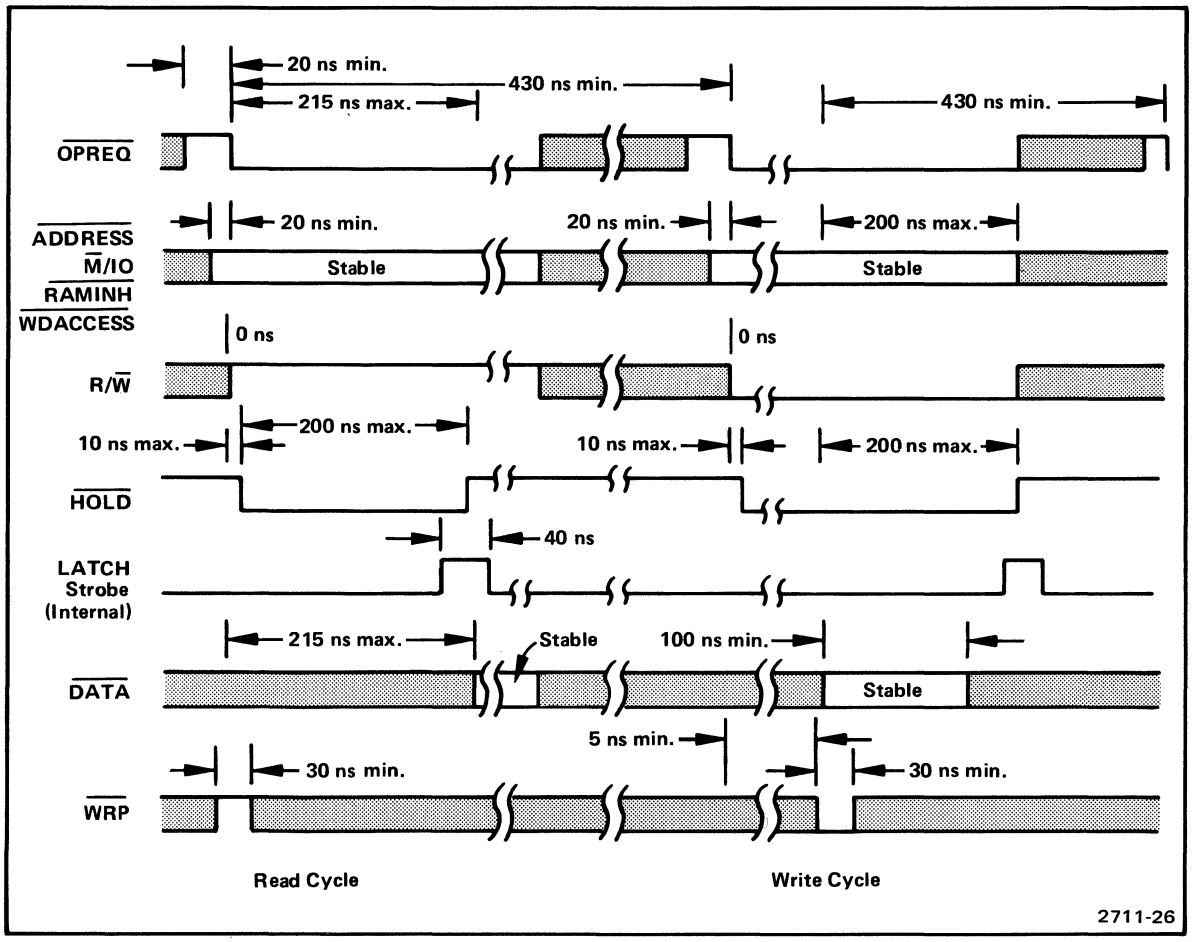


Fig. 8-3. High-Speed Memory Timing.

8

REFRESH

Refer to Fig. 8-4 for refresh operation timing diagrams. Refresh Request is input to NOR gate U5170B and flip-flop U3160A. A 100 ns inhibit pulse from the timing delay line (DL2140) is also input to the NOR gate. This 100 ns pulse will inhibit a request for any operation within 100 ns following the previous memory cycle. The RAMs require 100 ns to recover from a refresh, read, or write operation. If a refresh request were to occur before 100 ns had elapsed, the inhibit pulse would hold it off until the recovery period was completed.

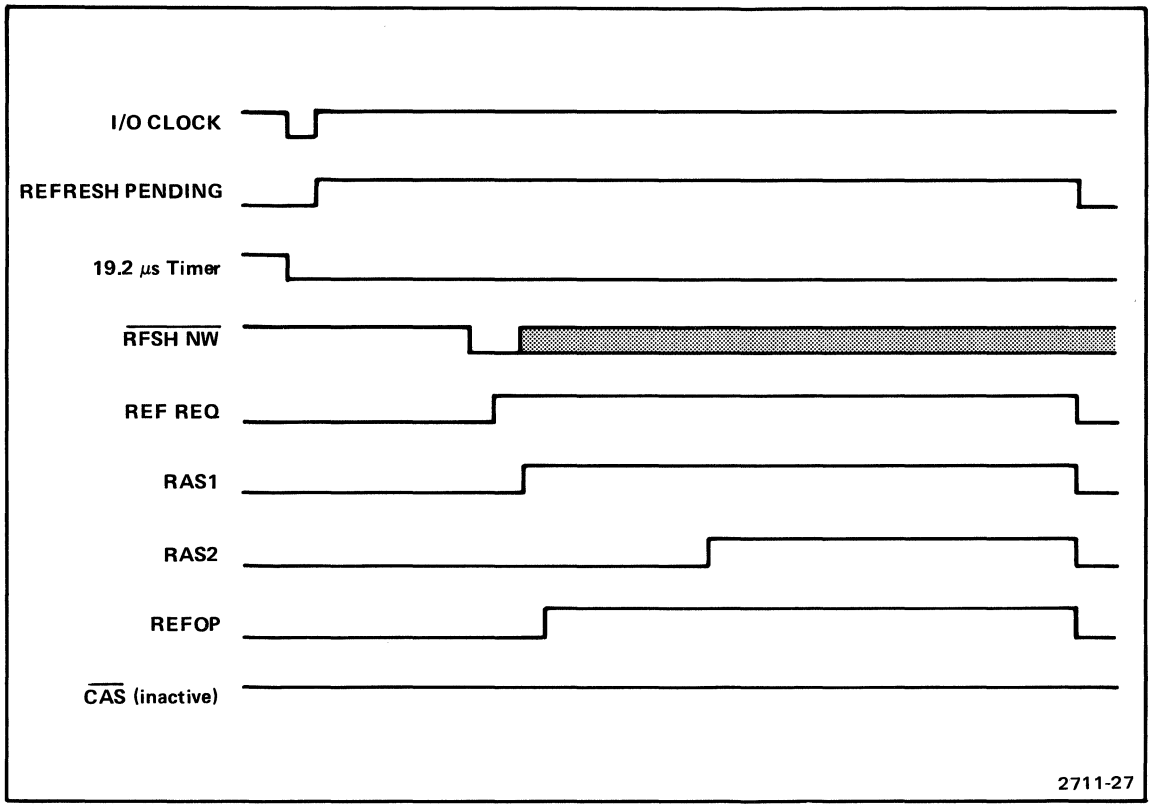


Fig. 8-4. High-Speed Memory Refresh Operation.

From NOR gate U5170B, the refresh request is input to NOR gate U5170D, along with the input for the read or write request. The output of this NOR gate represents a valid operation request. The operation request will clock both flip-flops U3160A and U3170B. In the event that a refresh request and a read or write request occur at the same time, the refresh arbitration circuit (U3160A and U3170B, U5170) will give the refresh request priority. When Refresh Request is generated, flip-flop U3160A will generate a refresh operation when clocked by an operation request.

When an operation request clocks the flip-flops, U3170B will produce RAS1, the first component of the $\overline{RAS}$ clock generator. RAS1 clocks flip-flop U3160B, which (in a refresh request) is set by U3160A to produce REFOP. When RAS1 is generated, REFOP sets up the Address Control.

Once RAS1 is produced, the following series of timing events takes place. RAS1 is coupled to the input of the delay line (DL2140). The timing signals are derived from the pulses, as they occur along the delay line at the various output taps. $\overline{CAS1}$ and $\overline{CAS2}$, the column address strobes, are

enabled from the 20 ns tap of the delay line. To do a refresh, only the row address strobes (RAS) are needed; CAS1 and CAS2 are inhibited by REF OP during this operation. The pulse from the 60 ns tap is gated with REFOP to set U3160A, removing the refresh request and creating RAS2. For refresh operations, the other taps are disregarded until the 200 ns tap is reached. The 200 ns tap is NANDed with REF OP, the 60 ns output, and the 100 ns output at U2160A to generate a reset pulse for the refresh request and refresh arbitration circuits. Resetting the refresh arbitration circuitry (U5170B, U4170D, U3160A, and U3170B) removes RAS1 and RAS2. Removing RAS1 sends a positive-going pulse through the delay line, and produces the 100 ns pulse used to inhibit operations during the required 100 ns recovery time. This concludes the refresh operation. The remaining circuitry of the Operation Control and Timing logic is explained in the read and write description that follows.

WRITE

To write into memory, a write operation request is made and the timing operation is begun. The following paragraphs describe the write request and timing. Timing diagrams are in Fig. 8-5. The timing for the write operation, described here, is also used to perform a read operation. Differences between the operations are discussed in the description of the read operation.

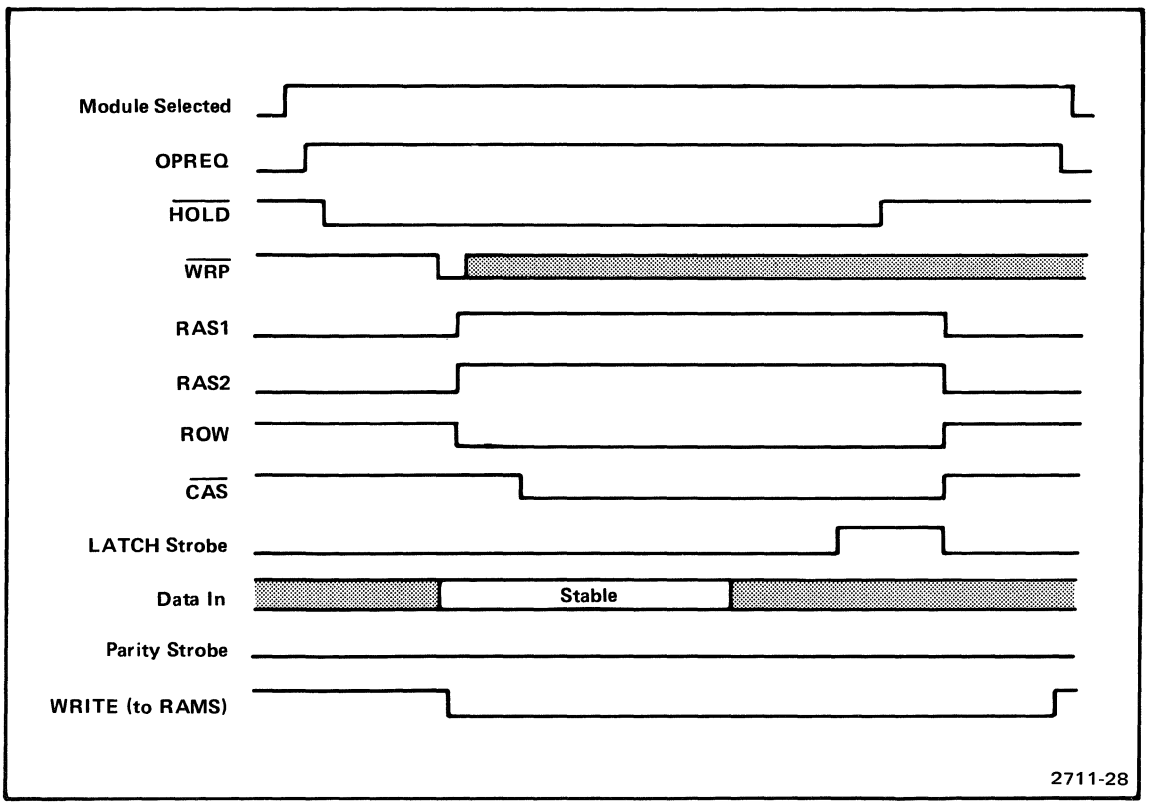


Fig. 8-5. High-Speed Memory Write Cycle.

A memory read or write operation is begun by selecting the module, as previously described. $\overline{\text{OPREQ}}$ is used to initiate either a read or write operation and to indicate to the module that an operation is underway. $\overline{\text{HOLD}}$ is generated to pause the emulator processor when $\overline{\text{OPREQ}}$ clocks U3180B (schematic 6D, lower right). The module is instructed by the system bus R/$\overline{\text{W}}$ line to do a write operation. For a write, the sequence is held at this point until Write Pulse ($\overline{\text{WRP}}$) is received. Because of its high speed, $\overline{\text{WRP}}$ is caught in latch U4180C (schematic 6D, lower left). The latched version of $\overline{\text{WRP}}$ is gated with $\overline{\text{OPREQ}}$ and R/$\overline{\text{W}}$ at U7180B to create Write Enable ($\overline{\text{WRT EN}}$). The latched WRP is also gated through U6170B (schematic 6D, lower left) to U2160B where it is gated with SELECT, the 100 ns recovery pulse, and the Previous Cycle Ended pulse (from U4180D). The output of this gate is the operation request to the refresh arbitration circuit.

The operation request signal from U2160B is input to NOR gate U5180D to clock refresh arbitration flip-flops U3160A and U3170B. If no refresh request is present at U3160A (schematic 6D, upper right) the flip-flop will output a set condition when clocked. RAS1 and RAS2 will be output simultaneously. REFOP flip-flop U3160B will remain reset; no REFOP will be output. ROW is output at the same time as RAS1.

RAS1 is input to the delay line (DL2140) to begin the timing sequence. The RAM column address strobes, $\overline{\text{CAS1}}$ and $\overline{\text{CAS2}}$, are generated at U3120B and U3120C by the pulse from the 20 ns tap of the delay line. The pulse from the 140 ns tap is gated at U4170B with REFOP, Previous Cycle Ended, and the 200 ns tap to produce LATCH. LATCH appears 140 ns after RAS. In the write operation, LATCH is purely a timing pulse; in a read, however, LATCH strobes the data-out latches. The signal from the 200 ns tap is input to the gate producing LATCH to shut LATCH off. (LATCH lasts for 60 ns.) LATCH also causes U3180B to reset the refresh arbitration flip-flops and to reset $\overline{\text{HOLD}}$, allowing the emulator processor or System Processor to proceed. LATCH essentially ends the operation; RAS and CAS clocks are reset and the 100 ns recovery time pulse to complete the cycle is produced by the delay line.

The Previous Cycle Ended signal comes from latch U4180D to indicate that the cycle is running or that the cycle is completed. The latch is reset when $\overline{\text{OPREQ}}$ occurs; the end of the cycle is indicated by the falling edge of LATCH.

READ

The basic timing pulses for a read operation are the same as for a write operation. The differences for the read operation are noted here. Refer to Fig. 8-6.

For a read operation, bus R/$\overline{\text{W}}$ line will be high, causing READ. As soon as $\overline{\text{OPREQ}}$ is received, READ is gated with SELECT, Previous Cycle Ended, and the 100 ns recovery pulse at gate U2160B to produce the operation request. The request does not have to be delayed, as in the write cycle. Write Pulse ($\overline{\text{WRP}}$), Write Enable ($\overline{\text{WRT EN}}$), and WRITE are inactive. The request for a read cycle and the resultant timing are the same as for the write operation. In a read cycle, LATCH will strobe the data-out latches in addition to its timing responsibilities.

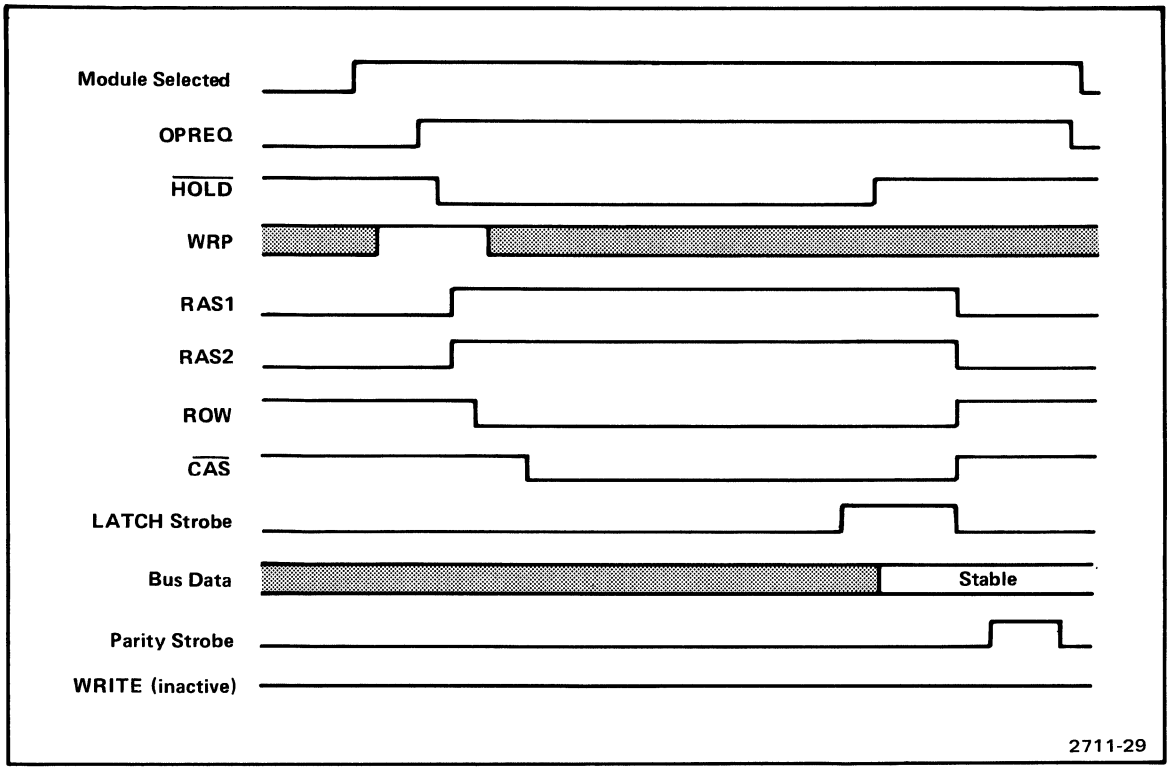


Fig. 8-6. High-Speed Memory Read Cycle.

Parity Strobe (PAR STR) is produced by U4170A (schematic 6D, center right) at the falling edge of LATCH. PAR STR clocks the parity error detector circuitry, enabling the circuit to check the validity of the data from RAM. PAR STR is the gated result of the ACTIVE, PROM, Previous Cycle Ended, and WRT EN signals, and indicates that the module is doing a read cycle.

If the module is being used as 8002A System Memory, the pulse from the 60 ns tap of the delay line is gated at U6120B with OPREQ, SELECT, and PROM to create PROM Chip Enable (PROM CE) when the PROM is addressed.

It should be noted here that when a reset is caused by LATCH at the end of an operation, only the refresh arbitration and timing control circuits are reset. Refresh request flip-flops are not reset, as resetting them could prevent a refresh from occurring. After a refresh operation the entire circuit is reset.

Reset Protection

A system reset should not disrupt data stored in memory. A problem arises when the front panel RESET switch is held in the reset position for too long. When this happens the module is not allowed to refresh and stored data decays. To overcome this problem, U7150, U4180 and U7180 (schematic 6D, lower left) are used as a reset protection circuit. This circuit prevents the reset from being carried to the memory module until the instant the reset switch is released. RESET will then be a pulse clocked by the System Clock.

Section 9

ASSEMBLER PROCESSOR MODULE

INTRODUCTION

The Assembler Processor utilizes a Z80 microprocessor to run the macro, assembler, and linker software of the 8002A μProcessor Lab System.

The Assembler Processor operates much like an emulator processor module. The Assembler Processor uses Program Memory to translate source input code (assembly language) to binary object code (machine language) for use by the emulator processor. The software that implements this translation is stored on the appropriate flexible disc for the emulator processor in use. The Assembler Processor operates as a slave to the System Processor, and is invoked when the ASM (Assemble) or LINK command is entered at the system console.

CIRCUIT DESCRIPTION

The functions of the Assembler Processor module can be divided into the following five areas:

- Control Byte Decoder and Latch
- Module Stop and Start
- Z80 Clock
- Address and Data Bus Buffers
- Control Signal Conversion

The following circuit descriptions refer to logic blocks as outlined on the schematics.

Control Byte Decoder and Latch 

Two actions are required to enable the Assembler Processor for operation. First, the System Processor must write a command byte to the Assembler Processor I/O address E7. The write to E7 is detected by U5030 and U3030. When the write to E7 occurs, U3030 generates an enabling pulse called UPE7.

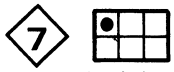
The second requirement for Assembler Processor operation is that the command byte must have bit 7 (the Active bit) asserted. The Assembler Processor module detects this bit and uses it to set up the J-K inputs of U5090.

The UPE7 signal clocks U5090, causing the $\overline{\text{ACTIVE}}$ line to go low. $\overline{\text{ACTIVE}}$ pulses the reset input of the Z80 microprocessor device. This reset causes the Z80 to go to address 0000 and begin execution.

Module Stop and Start 

The Assembler Processor module may be halted and started by either of two bus signals from the system. Module stop and start is carried out by $\overline{\text{SLV PAUSE}}$ (from the emulator processor) and $\overline{\text{F.P.HOLD}}$ (from the System Processor).

$\overline{\text{F.P. HOLD}}$ causes a wait condition during the $\overline{\text{OPREQ}}$ in which it occurs. $\overline{\text{SLV PAUSE}}$ stops the Z80 at the end of the current operation and activates $\overline{\text{BUSAQ}}$. NAND gates U4100A and U4100D keep $\overline{\text{RESET}}$ from going inactive until $\overline{\text{BUSRQ}}$ is inactive. Z80 RESET is held high when the module is inactive.

Z80 Clock 

The 10 MHz system clock is used to derive the clock for the Assembler Processor. A divide-by-four circuit (U4090) creates the 2.5 MHz clock used by the Z80.

Address and Data Bus Buffers 

Data and address lines from the Assembler Processor Z80 microprocessor are fed to the respective buses by tristate buffers. The data transferred through these buffers is also inverted.

Data lines are buffered to the bus by U3060 and U4060. When the Z80 is reading, Z80 WRITE is low and data can only be transmitted from the bus to the Z80. When the Z80 is in the Write mode, Z80 WRITE is high, and data can only be transferred from the Z80 to the bus. In Write mode, the portion of the buffer that transfers data from the bus to the Z80 is set to the high-impedance state.

When the Assembler Processor is active, the Z80 address lines are buffered to the system address bus by inverter-buffers U4030, U5040, and part of U5050. The buffers are set to the high-impedance state by Z80 RUN when the module is not running.

Control Signal Conversion 

The Z80 control signals of the Assembler Processor undergo conversion before being interfaced to the rest of the system. The signals are inverted by output buffers U5060 and part of U5050. These buffers are enabled by $\overline{\text{Z80 RUN}}$ when the Assembler Processor is running. The timing diagrams in Figs. 9-1 through 9-5 illustrate the control signal operation in the various modes of operation. Table 9-1 lists these control signal conversions.

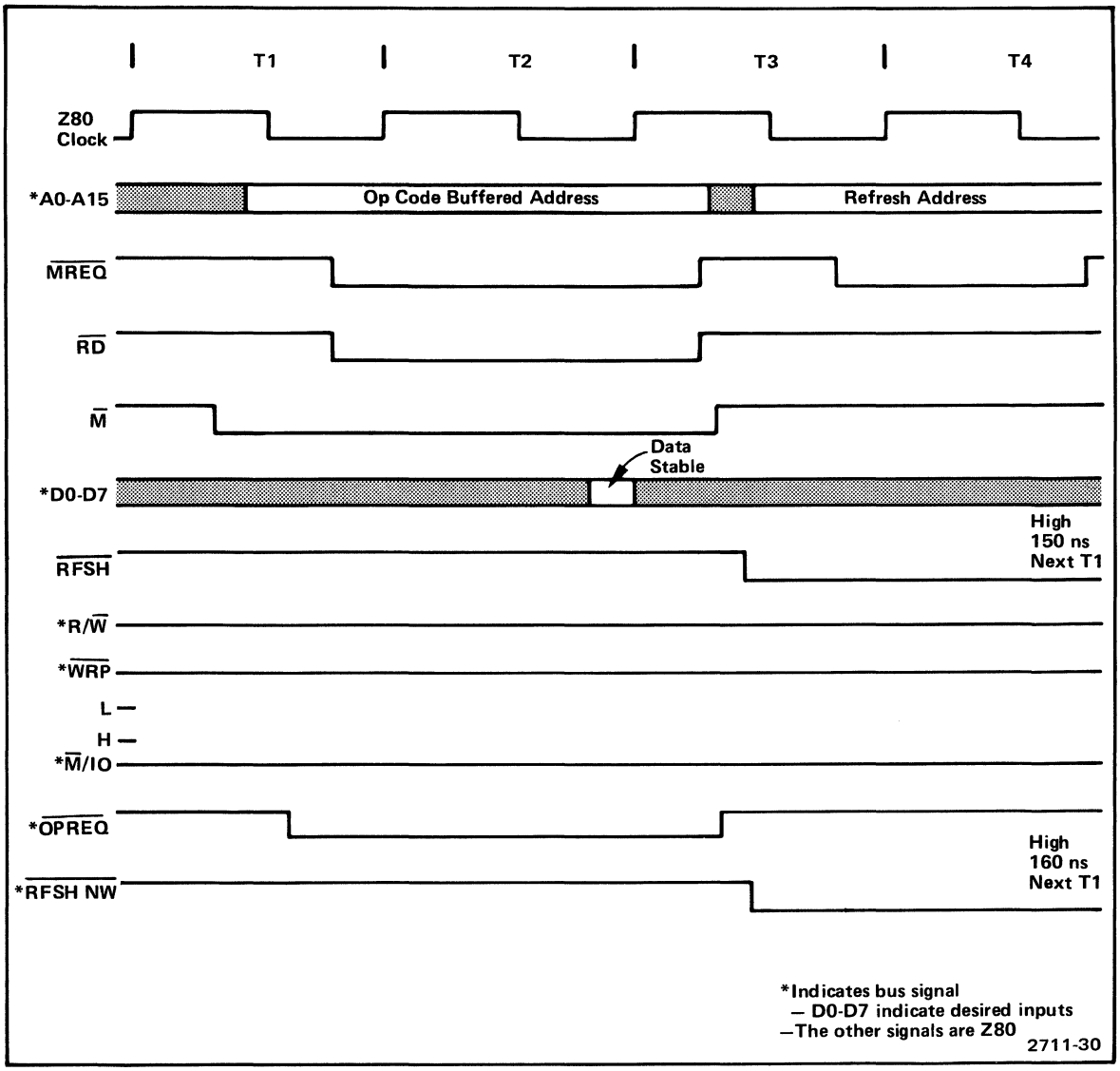


Fig. 9-1. Assembler Processor Operation Code Read Timing.

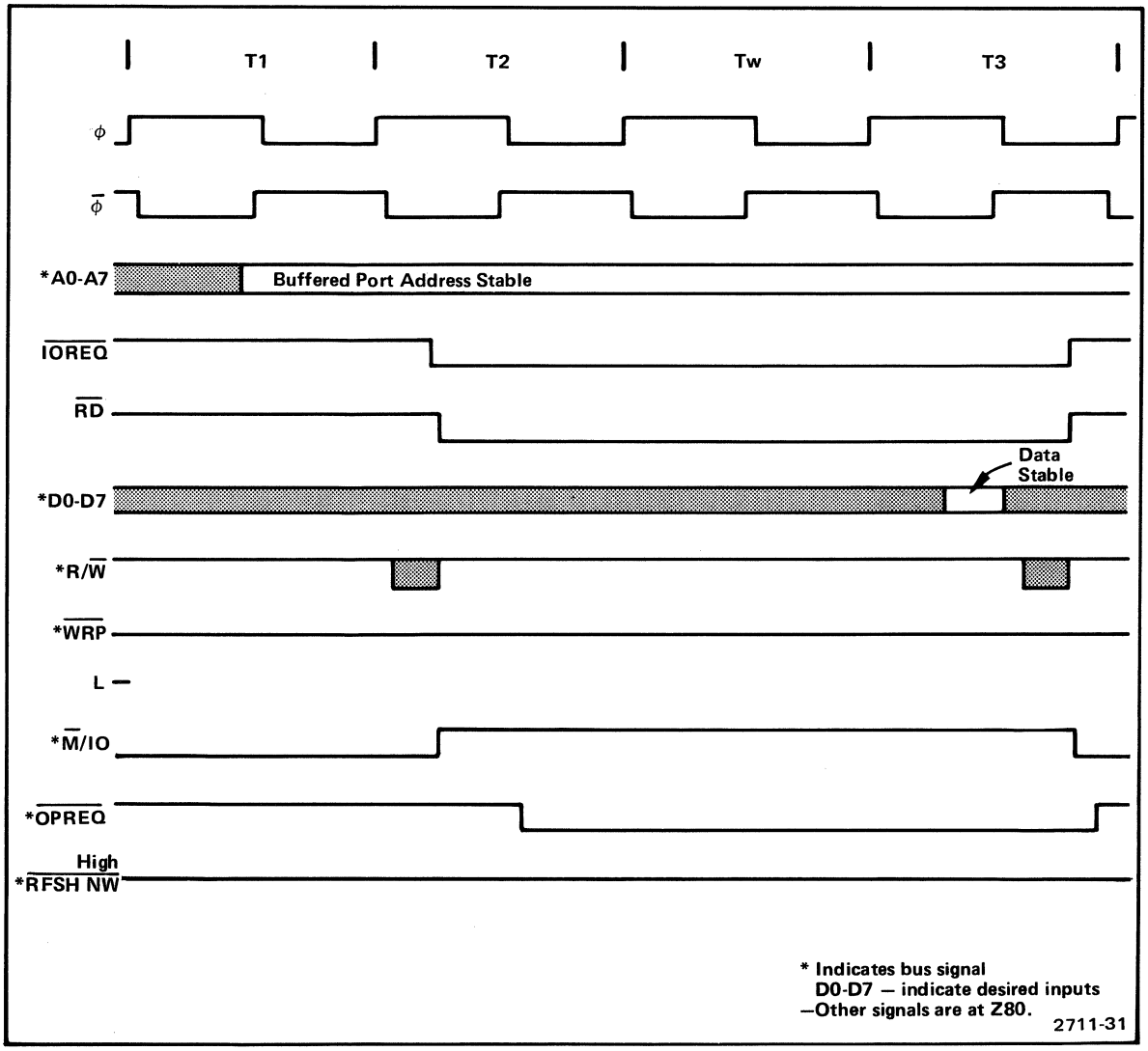


Fig. 9-2. Assembler Processor I/O Read Timing.

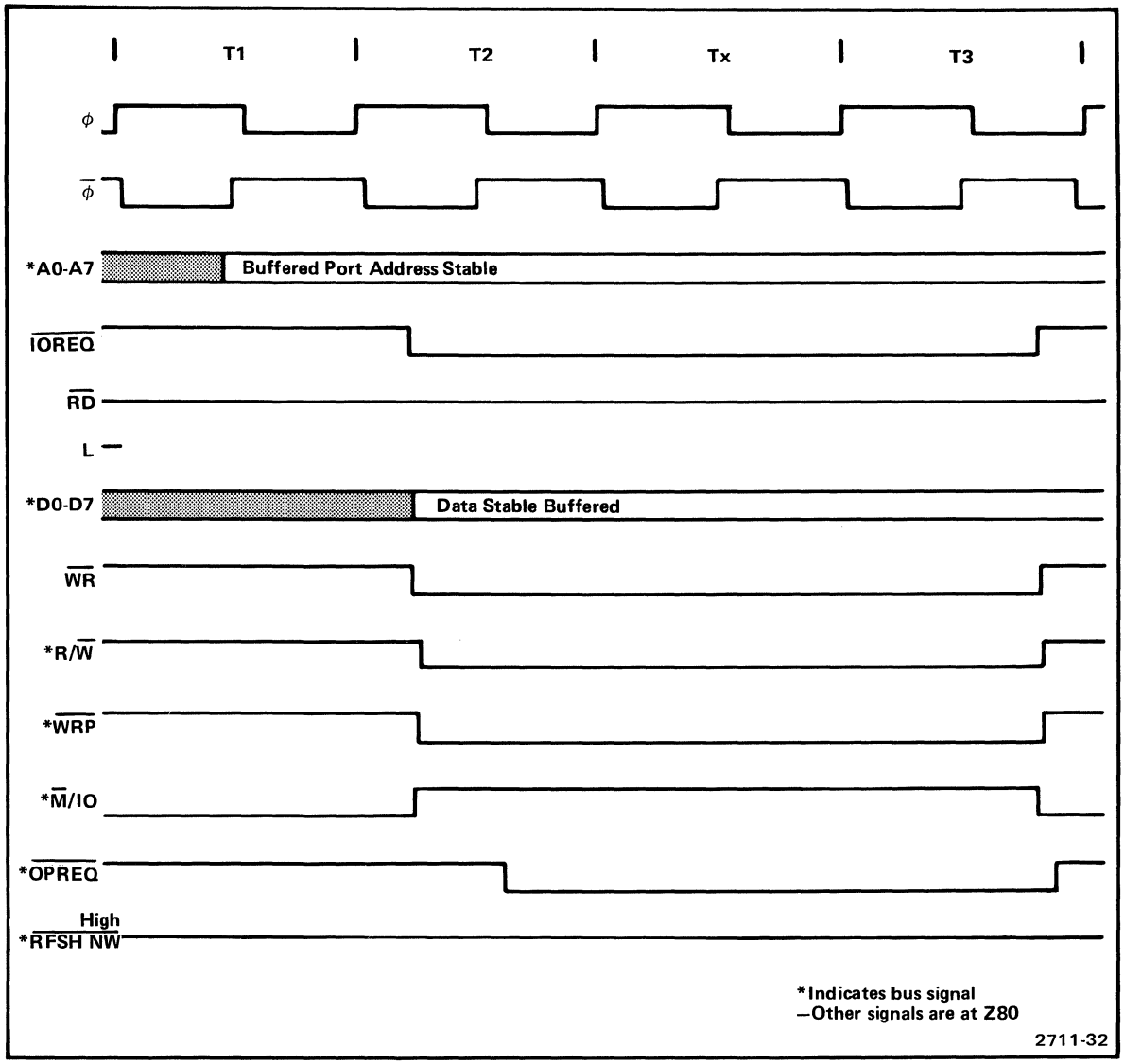


Fig. 9-3. Assembler Processor I/O Write Timing.

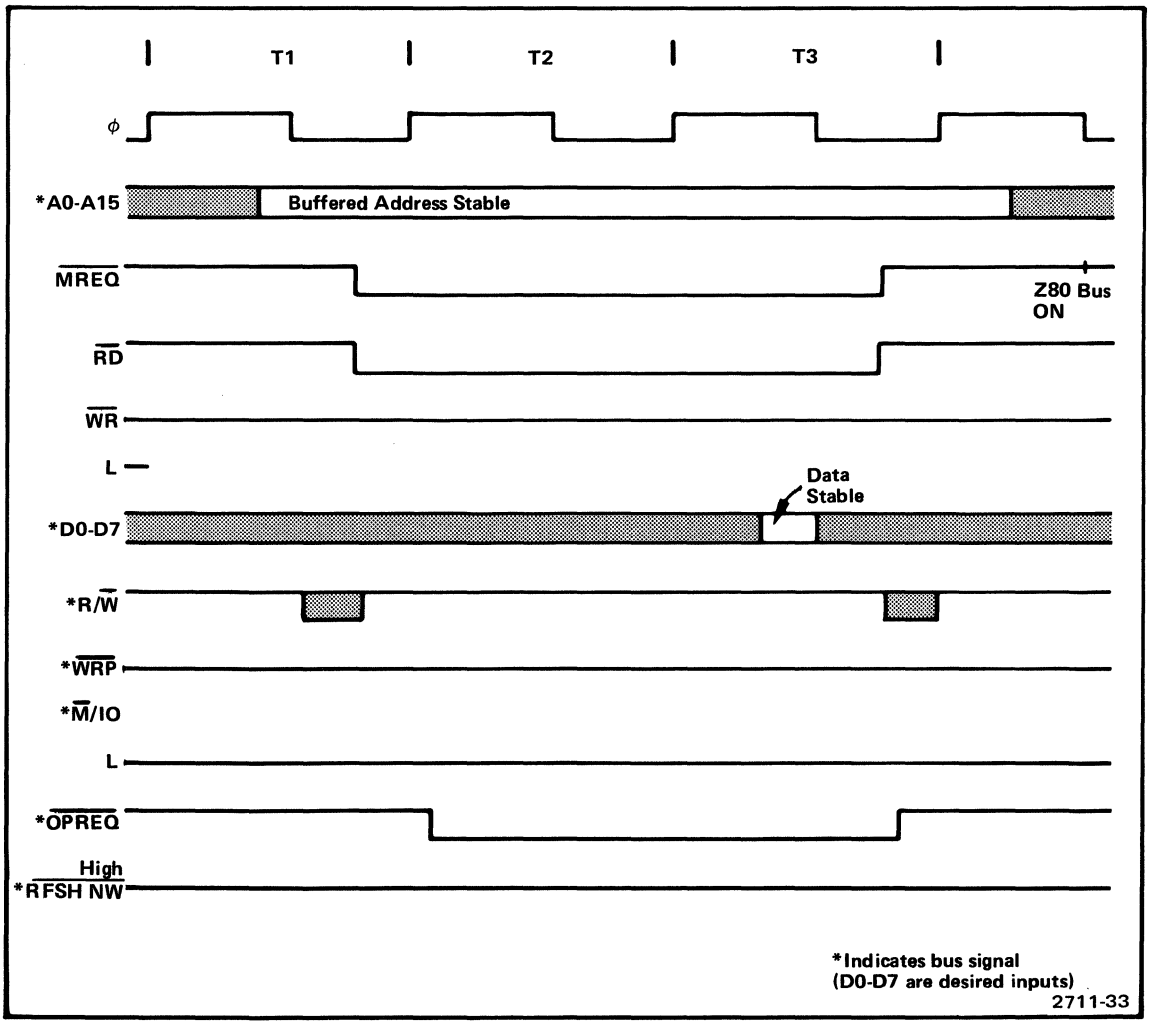


Fig. 9-4. Assembler Processor Memory Read Timing.

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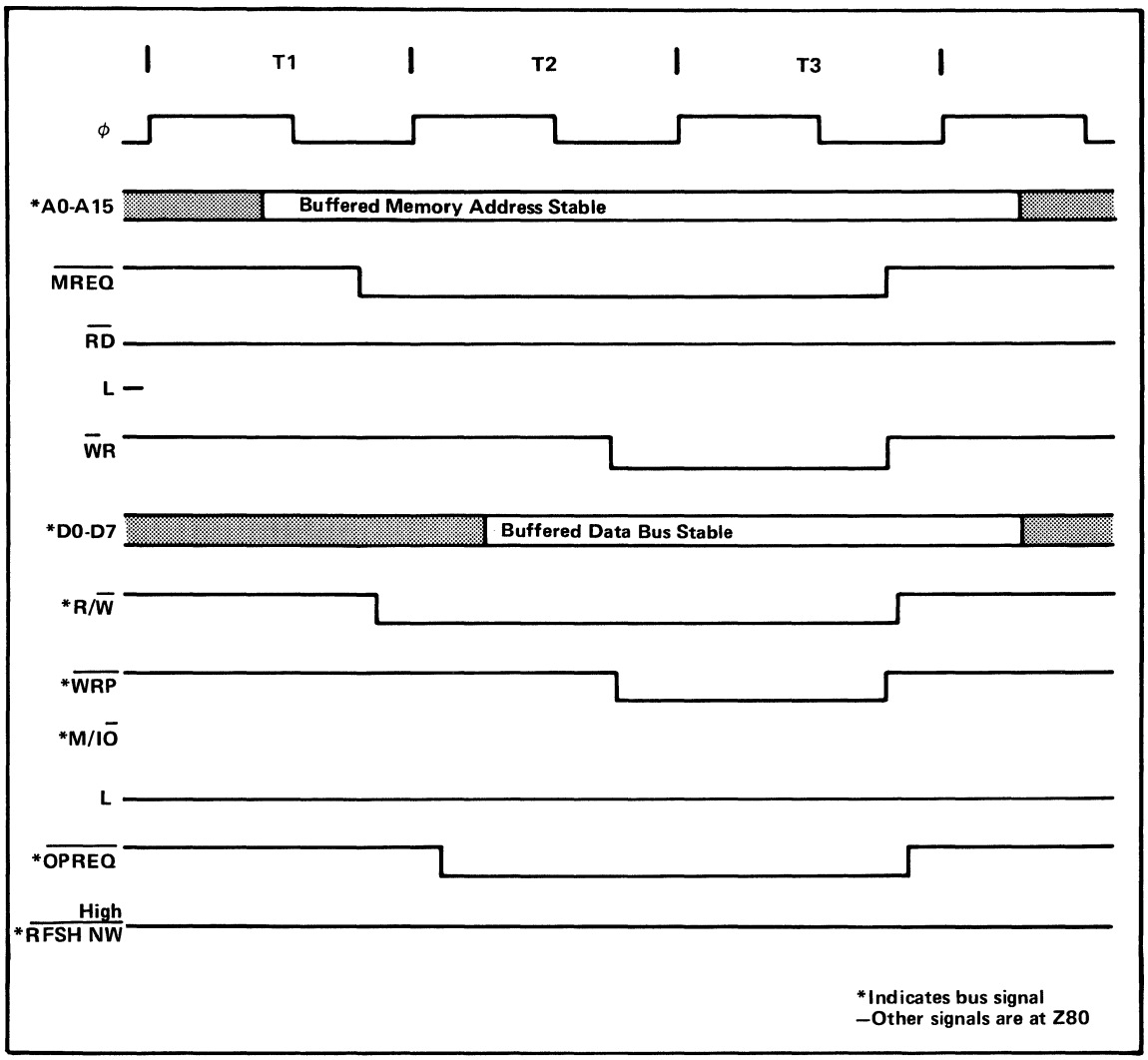

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Fig. 9-5. Assembler Processor Memory Write Timing.

Table 9-1
CONTROL SIGNAL CONVERSION

8002A CONTROL SIGNALS	Z80 CONTROL SIGNALS
$\overline{RUN}$	$\overline{HALT}$
$\overline{M}/IO$	$\overline{IOREQ}$
$R/\overline{W}$	$\overline{RD}$ OR $\overline{M1}$ (Further enabled when $\overline{MREQ}$ OR $\overline{IOREQ}$ is True)
$\overline{FETCH}$	$\overline{M1}$
$\overline{REFNW}$	$\overline{RFSH}$
$\overline{SLVOPREQ}$	$\overline{MREQ}$ OR $\overline{IOREQ}$ AND $\overline{M1}$ $(\overline{MREQ} + \overline{IOREQ}) \cdot \overline{M1}$
$\overline{OPREQ}$	$\overline{MREQ}$ OR $\overline{IOREQ}$ AND $\overline{M1}$

Refer to the Zilog Z80-CPU Technical Reference Manual for details on the Z80 control functions, timing, registers, and other characteristics.

For assembler operations or software details, refer to the 8002A μProcessor Lab System User's Manual and the 8002A μProcessor Lab Assembler & Emulator User's Manual that corresponds to your emulator processor.

Section 10

POWER SUPPLY

At this writing, the 8001/8002A μProcessor Lab +12 V and −12 V Power Supply module and the +5 V Power Supply module are serviced at the Tektronix Factory Service Center on an exchange basis.

See the Maintenance section (Section 11) for the proper procedure for removing the power supply modules from the mainframe.

Section 11

MAINTENANCE AND TROUBLESHOOTING

INTRODUCTION

This section describes procedures for preventing or reducing equipment malfunction, and includes techniques for troubleshooting and corrective maintenance. Preventive maintenance improves equipment reliability. Should the equipment fail to function properly, corrective measures should be taken immediately; otherwise, additional problems may develop within the equipment.

Static Sensitive Devices

1. Minimize the handling of static-sensitive parts.
2. Transport and store static-sensitive parts in their original containers, on a metal rail, or on conductive foam. Label any container having a static-sensitive assembly or device.
3. Discharge the static charge on yourself by using a wrist strap before handling these devices. It is recommended that servicing of static sensitive assemblies or devices be performed only at a static-free work station by qualified personnel.
4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.
5. Keep the leads shorted together whenever possible.
6. Pick up the part by the body, never by the leads.
7. Do not subject the part to sliding movements over any surface.
8. Avoid handling parts in areas having a floor or work surface covering that contributes to the generation of a static charge.
9. Use a soldering iron that has a connection to earth ground.
10. Use a special anti-static suction type desoldering tool, such as the Silverstat Soldapulit, or a wick type desoldering device.

REDUCTION OF SUSCEPTIBILITY TO STATIC DISCHARGE

The following safeguards have been provided within the 8001/8002A μProcessor Lab systems to minimize susceptibility to static discharge:

1. The ground (earth) wire of the primary power cable is connected to the chassis where the cable enters the unit.
2. The shields of interconnecting EIA cables are grounded to the chassis at the cable entrance or egress of each unit.
3. All interconnecting ribbon cables have a built-in ground plane which is grounded to the chassis at the cable entrance or egress of each unit.

4. Ground loops have been avoided by installing a common ground between all units. Grounding straps are utilized where necessary. Refer to the 8001/8002A μProcessor Lab Installation Guide.

CAUTION

Violation or modification of the preceding safeguards can result in ground loops and/or static discharge problems.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of cleaning, visual inspection, and performance check. The preventive maintenance schedule established for the equipment should be based on the amount of use, and on the environment in which the equipment is operated.

Cleaning

Clean the equipment often enough to prevent dust or dirt from accumulating in or on it. Dirt acts as a thermal insulating blanket and prevents efficient heat dissipation. It also provides high-resistance electrical leakage paths between conductors or components in a humid environment.

EXTERIOR

Clean the dust from the outside of the equipment by cleaning the surface with a soft cloth or brush. The brush will remove dust from around the front panel selector buttons. Hardened dirt may be removed with a cloth dampened in water that contains a mild detergent. Abrasive cleaners should not be used.

INTERIOR

Normally the interior of the equipment will not require cleaning unless it has been left uncovered for an extended period of time. Clean the interior by loosening accumulated dust with a dry soft brush, then blow the loosened dirt away with low-pressure air.

High-velocity air can damage some components. If the circuit board assemblies need cleaning, remove the circuit board and clean with a dry, soft brush. Hardened dirt or grease may be removed with a cotton-tipped applicator dampened with a solution of mild detergent and water. Do not leave detergent on critical memory components. Abrasive cleaners should not be used.

After cleaning, allow the interior to dry thoroughly before applying power to the equipment.

CAUTION

Do not allow water to get inside any enclosed assembly or components, such as switch assemblies, memory capacitors, potentiometers, etc. Instructions for removing assemblies for maintenance are provided in the Corrective Maintenance part of this section. Do not clean any plastic materials with organic cleaning solvents (such as benzene, toluene, xylene, acetone, or similar compounds); they may damage the plastic.

VISUAL INSPECTION

After cleaning, carefully check the equipment for such defects as defective connections and damaged parts. The remedy for most visible defects is obvious. If heat-damaged parts are discovered, try to determine the cause of overheating before replacing the damaged part; otherwise, the damage may be repeated.

TROUBLESHOOTING

Your Tektronix Service Support Center is best suited to perform repairs on this unit. However, the following general troubleshooting procedures may aid you in tracing a problem to its source.

Before beginning any troubleshooting work, check your warranty or service agreement. To prevent voiding the warranty, all service must be performed by Tektronix, Inc. for the first 90 days following delivery.

General

1. Check that all cabling is installed properly.
2. Verify performance of the system terminal.
3. Check that the Debug and Front Panel I/O module is in the correct slot (J9) of the motherboard.
4. After shutting off primary power to the μProcessor Lab, remove all modules from the motherboard. Clean each module's P1 edge connector with a cotton swab and isopropyl alcohol. Replace the modules.
5. If a duplicate set of modules is available, try swapping the modules, one by one, to find the defective one.
6. Check all power supply levels (usually accessible at the test points of each module).

Will Not Boot Up

1. If the system will not boot up, use another TEKDOS disc.
2. If, after boot up, the front panel indicator SYS does not come on, check the SYS indicator light and/or replace the Debug and Front Panel I/O module.

Emulation Problems

1. If the system does not function in emulation mode 1, check the clock input pins on the emulator processor to verify the presence and level of the prototype clock.
2. Check the prototype power supplies.
3. If mapped memory is being used in emulation mode 1, check that the System Communications module is plugged into the motherboard.
4. If the system fails in emulation modes 1 or 2, check that the signals that exist on the emulating microprocessor also exist at the prototype socket. If they do not, check the prototype control probe to find the problem.
5. If the MOVE, DUMP, or EXAMINE commands don't perform in prototype memory, place the emulator processor on an extender card and verify the operation of the prototype control probe data bus drivers during execution of each of these commands. Check the address and control line drivers, too.

PROM Programmer

1. If the system won't read or write PROMs, check the power level on the PROM Programmer module.

Troubleshooting Aids

DIAGRAMS

Circuit diagrams are given on foldout pages in the Diagrams section of the manual. The circuit number and electrical value of each component are shown on the diagram. (See the first tab page for definition of the reference symbology used to identify components in each circuit.) Components on circuit boards are assigned vertical and horizontal grid numbers which correspond to the location of the component on the circuit board. Refer to the Replaceable Electrical Parts List section for a complete description of each component and assembly. Those portions of the circuit that are on circuit boards are enclosed with a black border line, with the name and assembly number shown on the border.

NOTE

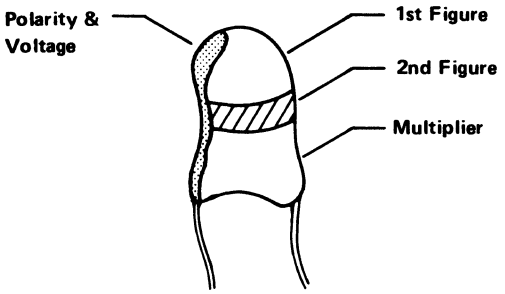
Corrections and modifications to the manual and equipment are described on inserts bound into the rear of the manual. Check this Change Information section for manual or instrument changes and corrections.

CIRCUIT BOARD ILLUSTRATIONS

Electrical components, connectors, and test points are identified on circuit board illustrations located on the inside fold of the corresponding circuit diagram or on the back of the preceding diagram. This allows cross-referencing between the diagram and the circuit board, and shows the physical location of components.

CAPACITOR MARKING

The capacitance value of common disc capacitors and some electrolytics is marked in microfarads on the side of the component body. The white ceramic capacitors are color-coded in picofarads. Tantalum capacitors are color-coded as shown in Fig. 11-1.



DIPPED TANTALUM CAPACITOR MARKING

A AND B CASE

CAPACITANCE AND VOLTAGE COLOR CODE

Rated Voltage VDC 25°C	Color	CODE FOR CAPACITANCE IN PICOFARADS		
		1st Figure	2nd Figure	Multiplier
3-4	Black	0	0	None
3-6	Brown	1	1	X10
3-10	Red	2	2	$X10^2$
3-15	Orange	3	3	$X10^3$
3-20	Yellow	4	4	$X10^4$
3-25	Green	5	5	$X10^5$
3-35	Blue	6	6	$X10^6$
3-50	Violet	7	7	$X10^7$
	Gray	8	8	
3	White	9	9	

(1733) 2312-15

Fig. 11-1. Tantalum Capacitor Color Code.

DIODE CODE

The cathode of each glass-encased diode is indicated by a stripe, a series of stripes, or a dot. Some diodes have a diode symbol printed on one side. Figure 11-2 illustrates diode types and polarity markings that are used in this equipment.

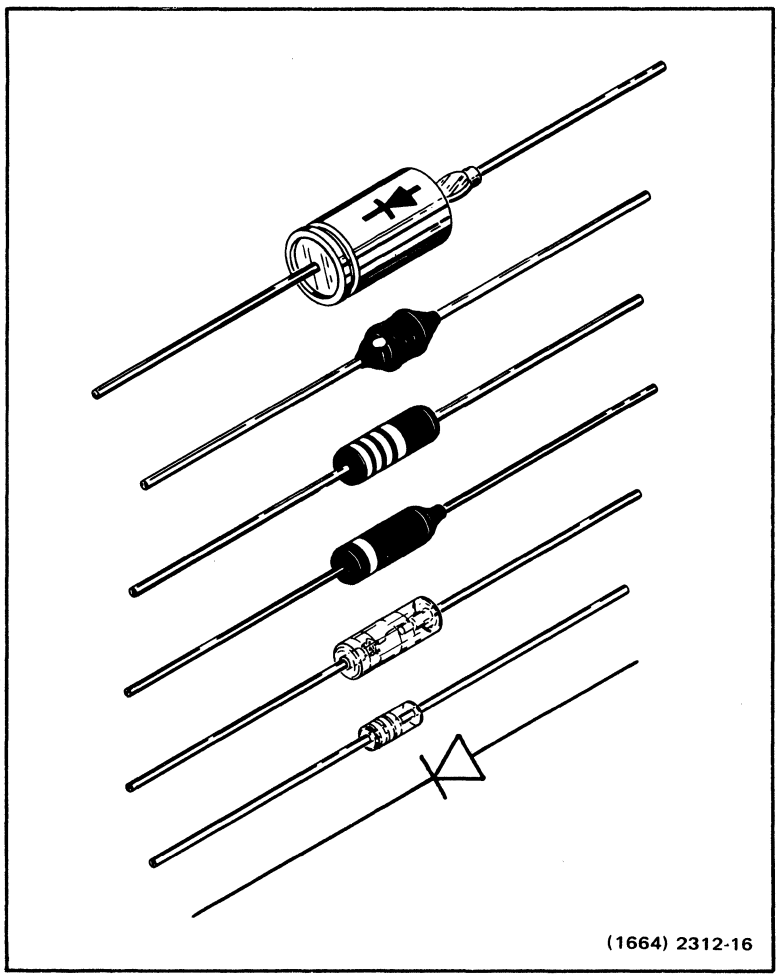


Fig. 11-2. Diode Polarity Marking.

TRANSISTOR AND INTEGRATED CIRCUIT PIN CONFIGURATION

Lead identification for the transistors is shown in Fig. 11-3. IC pin-out diagrams are shown, when necessary, on the back of the adjoining pullout schematic diagram.

DIODE CHECKS

Most diodes can be checked in the circuit by taking measurements across the diode and comparing these with voltages listed on the diagram. Forward-to-back resistance ratios can be taken by referring to the schematic and pulling appropriate transistors and pin connectors to remove low-resistance loops around the diode.

CAUTION

Do not use an ohmmeter scale with a high external current to check the diode junction.

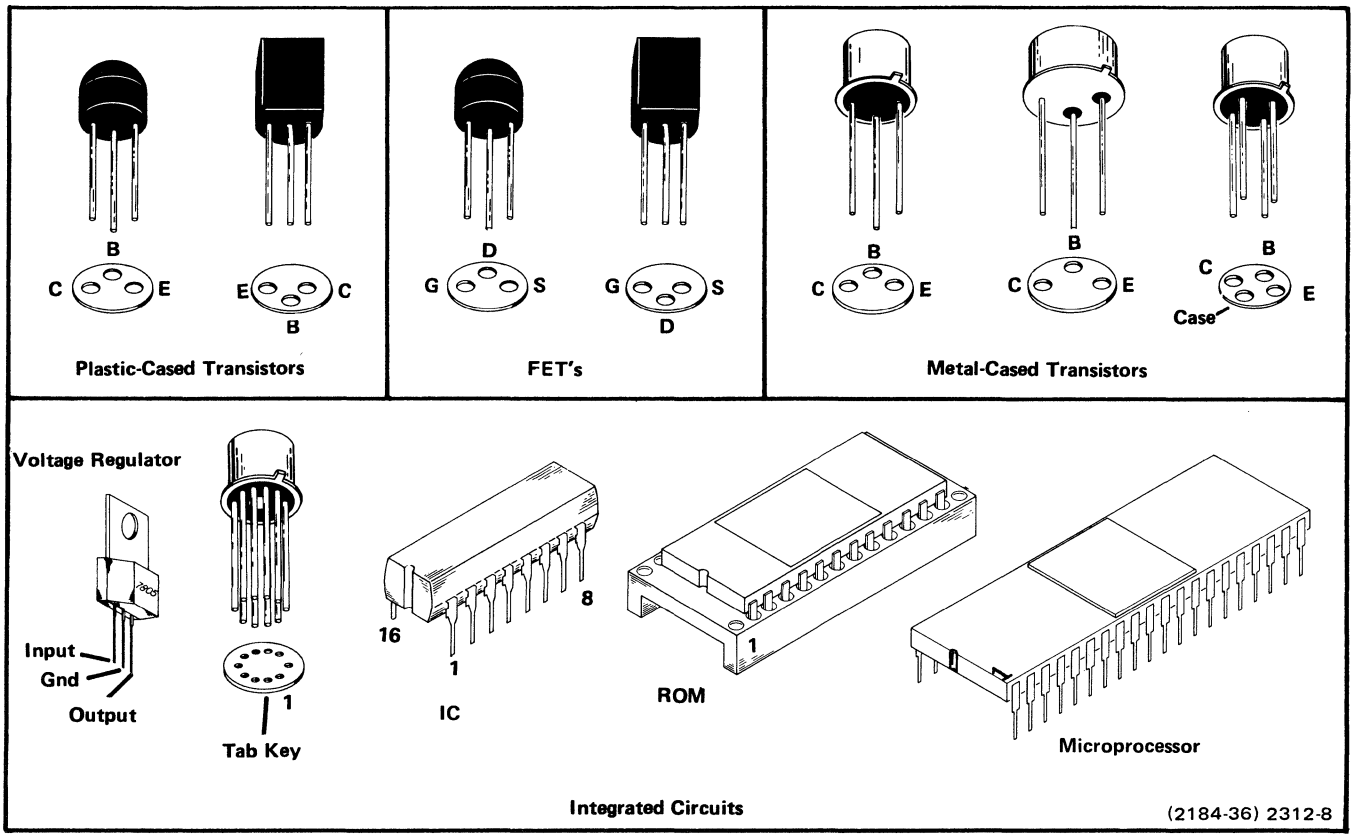


Fig. 11-3. Pin Configuration for Semiconductor Components.

11

INTEGRATED CIRCUIT (IC) CHECKS

When substitution is impossible, check input and output signal states, as described in the Circuit Description and on the diagrams. Lead configuration and data for the ICs used in this equipment are provided on the inside fold of the schematic or the back of the previous schematic.

CAUTION

To avoid possible damage from static charges, handle all ICs in accordance with the instructions at the beginning of this section.

CORRECTIVE MAINTENANCE

Corrective maintenance consists of component replacement and equipment repair. The following discussion describes special techniques and procedures required to replace components in this equipment.

Obtaining Replacement Parts

Most electrical and mechanical parts are available through your local Tektronix Field Office or representative. The Replaceable Electrical and Mechanical Parts List sections contain information on how to order these replacement parts. Many standard electronic components can be obtained locally in less time than required to order from Tektronix, Inc. It is best to duplicate the original component as closely as possible. Parts orientation and lead dress should be duplicated because orientation may affect circuit interaction.

If a component you have ordered has been replaced with a new or improved part, your local Field Office or representative will contact you concerning the change in the part number.

Parts Repair and Exchange Program

Tektronix service centers provide replacement or repair service on major assemblies, in addition to the unit itself. Contact your local service center for this service.

Soldering Technique

CAUTION

Disconnect the equipment from its power source before replacing or soldering components.

DISCRETE COMPONENT REPLACEMENT

Because it is easy to damage the plating in the board holes to which the component is soldered, it is recommended to cut the old component free and leave some lead length to solder the new component leads to. If the leads are pulled through the board, use caution when pulling them through the plated hole. Excessive heat or bent leads can damage the plating. Using a 15-watt pencil-type iron, straighten the leads on the back side of the board; then, when the solder melts, gently pull the soldered lead through the hole. A desoldering tool should be used to remove the old solder.

INTEGRATED CIRCUIT REPLACEMENT

Most of the ICs within this equipment are soldered into the module boards; therefore, extreme care must be taken to prevent damage to the module boards if the ICs are removed and replaced. The procedure used to remove ICs from the module boards is dependent upon: the cost of the IC, the competency of the technician accomplishing the repairs, and the degree of certainty that the IC is defective. One of the following procedures is recommended.

1. **Inexpensive ICs or ICs that are known to be defective.** Cut the defective IC from the board. Cut each pin close to the body of the IC, leaving as much of the pin as possible attached to the board. On the back side of the board use a 15-watt pencil-type soldering iron to melt the solder around the pins. When the solder melts, gently pull the pin out of the hole from the component side of the board. Repeat this procedure for each pin. A desoldering tool should be used to remove the old solder. Use caution when pulling the pins through the plated hole. Excessive heat or bent leads can damage the plating. When all pins have been removed and the holes are free of solder, install the new IC (ensure proper orientation of IC pin numbers). Solder each pin from the back side of the board and cut off excess pin length. Visually inspect the board for excess solder or solder bridges before testing the board's operation.

2. **Expensive ICs or ICs that *may* be defective.** On the back side of the board use a 15-watt pencil-type soldering iron to melt the solder around the pins. A desoldering tool should be used to remove the excess solder. Using needle-nose pliers, gently wiggle the pin in the hole while removing the solder. When the pin is free of solder in the hole, repeat the same procedure for each pin on the IC. When all pins are free, use an extracting tool and gently pull the IC from the board. Do not use force if the IC does not come free of the board. Use the soldering iron to remove excessive solder from the pin or pins at the same time the IC is being pulled from the board. When the IC is free of the board, carefully straighten each pin. If the IC is to be replaced or a new IC is to be installed, follow the same procedure as stated above for inexpensive ICs.

NOTE

An extracting tool to remove the ICs may be ordered from Tektronix, Inc. If an extracting tool is not available, use care to avoid damaging the pins. Pull slowly and evenly on both ends of the IC. Try to avoid having one end of the IC disengaged from the board before the other end.

Disassembly and Replacement of 8001/8002A μProcessor Lab Assemblies

The major assemblies of the 8001/8002A μProcessor Lab consist of front panel, back panel, motherboard, power supplies, and six or more module assemblies (printed circuit boards). Since the removal procedure for the power supplies requires almost a complete disassembly of the μProcessor Lab, it is the only disassembly procedure included.

NOTE

Power supply modules (+5.2 Vdc, plus and minus 12 Vdc) are listed in the Replaceable Electrical Parts list as one part number for each power supply. Component part numbers are not furnished. Complete assembly replacement is recommended.

Both power supply modules are fastened together so if either is to be serviced or replaced, both modules must be removed from the equipment. Replacement or removal requires removing all the major assemblies except the front panel and motherboard assemblies. The following describes the disassembly and replacement procedure to service or replace the power supply modules.

1. Removal of Power Supply Modules

WARNING

Before the μProcessor Lab is disassembled make sure the primary power cord has been disconnected from the back panel.

a. Remove the three screws located along each side of the top cover and lift the top cover off the mainframe.

b. Disconnect connector P2 from the System Processor module. Remove connector and ribbon cable assembly from the unit. (Interconnecting cable to the Flexible Disc Unit.)

c. Disconnect and remove all cable connectors to the Emulator Processor modules and the connectors that terminate on the back panel.

d. Place the μProcessor Lab on a flat work surface, preferably a dolly so that direct access to all sides of the unit is possible.

e. Remove all remaining connectors to the modules and remove all plug-in circuit board modules from the unit to prevent damage to the modules.

CAUTION

Depending on the 8001/8002A μProcessor Lab configuration there may be as many as nine cable assemblies with connectors that terminate at the modules and the other end terminating in either the front or back panel. When the connectors to the modules are disconnected and the modules removed, roll the cable assemblies up and secure them inside the mainframe to keep them from being damaged when the unit is turned on its side, top, or back.

f. Place the unit on its top, remove the four screws in the bottom cover then lift and place the cover aside. Set the unit back on its bottom or base.

CAUTION

Make sure the unit is placed on a flat surface to protect the bottom of the mother-board.

g. Remove Data Acquisition Interface module (if installed) from the back panel—four screws. Set the module with its attached cable aside.

h. Remove the left rear power supply cover by removing the two screws in front of the cover (through rear module positioning bracket) and the two screws through the back panel. Lift front of cover until it is clear of the module positioning bracket, then slide it forward until it clears J103 and can be removed. Replace screws in the cover to prevent their loss. (Longer screws go in front of the cover.)

i. Remove right rear power supply cover by removing the three screws in front of the cover (through rear module positioning bracket) and the three screws through the back panel. From rear of unit, move cover to the right and lift with a slight clockwise motion until the cover is clear of the module positioning bracket and connector J100. It can now be removed. Replace screws in the cover to prevent their loss. (Longer screws go in front of the cover.)

j. Remove the back panel by removing the four screws holding the back panel to the mainframe. Then tilt top of the back panel away from the mainframe to gain access to TB2 and connectors P24 and J26. (Do not pull the cables that are still attached to the back panel.)

NOTE

When reassembling, do not tighten screws in Step 1j until screws fastening covers in Steps 1h and 1i have been tightened.

k. Unsolder the chassis ground wire to TB2-3 on the back side of terminal block TB2. Remove terminal block TB2 from the back panel by removing the two machine screws and hex nuts. Pull terminal block away from back panel far enough so it can be turned and the end of the terminal block fed through the hole in the back panel.

CAUTION

The wires attached to the terminal block are long enough for removal; however, undue force should not be used when feeding the terminal block through the hole.

l. Disconnect connectors P24 and J26. The back panel is now disconnected from the mainframe. Set the back panel aside.

m. Place the unit on its right side. Remove three screws along the bottom of +5.2 Vdc power supply chassis. (Screws are through lower rear module positioning bracket.) Place the unit back on its base or bottom.

n. Disconnect connector P22 from the motherboard and connector P23 on the main power switch cable assembly. Remove interlock switch S3 mounting plate from the mainframe.

o. Disconnect all wire terminal lugs from terminal block TB1, on the motherboard.

p. Remove the three screws (one has a hex nut) that secure each end of the power supply assembly to the sides of the mainframe.

CAUTION

Before removing the screws on the right side of the mainframe, place shimming material (approximately 3/8 inch) under the power transformer of the +5.2 Vdc power supply to prevent the power supplies from dropping when the screws in Step 1p are removed.

q. The power supply assemblies or modules can now be removed from the mainframe.

CAUTION

Feed connectors (P22 and P23) and wires from terminal block under the lower rear module positioning bracket as the power supplies are removed from the mainframe.

2. Separating Power Supply Modules

If only one of the power supply modules is defective, the two modules must be separated to replace the defective module. After the power supply modules have been removed from the mainframe, remove the four screws holding the two power supply modules together. Cut cable assembly lacing (cable ties) and separate the wires for each module.

3. Replacing Defective Plus and Minus 12 Vdc Power Supply

CAUTION

The following procedure requires unsoldering and removal of existing wires on the defective power supply and re-connecting and soldering these wires to the replacement power supply. Extreme care must be taken to make sure the existing wires are not damaged and the wires are re-connected to their correct terminals.

After separating the two modules, place the defective plus and minus 12 Vdc power supply module on its top and perform the following procedure:

a. Locate primary winding termination numbers 1 thru 4 (four terminations) on the power transformer. Cut the protective tubing over the wires and transformer terminals for these four terminations. Unsolder the four terminations and remove the wires. Make sure all wires are tagged as they are removed.

NOTE

Only the primary winding terminations are disconnected on the power transformer. The secondary windings in the power transformer for the plus and minus 12 Vdc power supply are connected internally within the power supply module.

b. Unsolder and remove the three dc volt output wires that terminate into stand-off terminals. Make sure all wires are tagged.

c. The plus and minus 12 Vdc power supply module is now completely disconnected and can be removed.

d. Before re-connecting the wires to the new module transformer terminals, slip heat-shrink tubing (or similar tubing) over the wires. Re-connect and solder the wires removed in Steps 3a and 3b. Apply heat to shrink tubing over the wires and terminals after they have been soldered to the terminals. Cover as much of the transformer connecting lugs as possible before shrinking the tubing.

e. Utilize the mounting brackets from the defective power supply and reassemble both power supply modules.

f. Using cable ties or equivalent, re-bundle the cable and tie the cables that were separated during the separation procedure for the two power supplies.

4. Replacing Defective +5.2 Vdc Power Supply

CAUTION

The following procedure requires unsoldering and removal of existing wires on the defective power supply and the re-connecting and soldering of these wires to the replacement power supply. Extreme care must be taken to make sure the existing wires are not damaged and that wires are re-connected to the correct terminals.

After separating the two modules, place the defective +5.2 Vdc power supply module on its top and perform the following procedure:

a. Locate primary winding termination numbers 1 through 4 (four terminations) on the power transformer and secondary winding termination numbers 20 through 26 (seven terminations). Cut protective tubing from the wires and transformer terminals for these 11 terminations. Unsolder all 11 terminations and remove the wires. Make sure all wires are tagged as they are removed.

NOTE

Only the primary and secondary winding terminations specified in Step 4a are disconnected on the power transformer. The remaining secondary windings on the power transformer for the +5.2 Vdc power supply are connected internally within the power supply module.

b. Disconnect and remove all dc volt output wire terminal lugs (six terminal lugs) that terminate into stand-off terminals. Make sure all wires are tagged.

c. The +5.2 Vdc power supply module is now completely disconnected.

d. Before re-connecting the wires to the new module transformer terminals, slip heat-shrink tubing (or similar tubing) over the wires. Re-connect and solder the wires removed in Steps 4a and 4b. Apply heat to shrink the tubing over wires and terminals after they have been soldered to the terminals. Cover as much of the transformer connecting lugs as possible before shrinking the tubing.

e. Utilize the mounting brackets from the defective power supply and reassemble both power supply modules.

f. Using cable ties or equivalent, rebundle the cables and tie the cables that were separated during the separation procedure for the two power supplies.

5. Replacement of Power Supply Modules

To replace the power supply modules for the 8001/8002A μProcessor Lab unit, reverse the procedure for "Removal of Power Supply Modules".

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

ACTR	ACTUATOR	PLSTC	PLASTIC
ASSY	ASSEMBLY	QTZ	QUARTZ
CAP	CAPACITOR	RECP	RECEPTACLE
CER	CERAMIC	RES	RESISTOR
CKT	CIRCUIT	RF	RADIO FREQUENCY
COMP	COMPOSITION	SEL	SELECTED
CONN	CONNECTOR	SEMICOND	SEMICONDUCTOR
ELCTLT	ELECTROLYTIC	SENS	SENSITIVE
ELEC	ELECTRICAL	VAR	VARIABLE
INCAND	INCANDESCENT	WW	WIREWOUND
LED	LIGHT EMITTING DIODE	XFMR	TRANSFORMER
NONWIR	NON WIREWOUND	XTAL	CRYSTAL

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P O BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
01963	CHERRY ELECTRICAL PRODUCTS CORPORATION	3600 SUNSET AVENUE	WAUKEGAN, IL 60085
04009	ARROW-HART, INC.	103 HAWTHORNE STREET	HARTFORD, CT 06106
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
07910	TELEDYNE SEMICONDUCTOR	12515 CHADRON AVE.	HAWTHORNE, CA 90250
09023	CORNELL-DUBILIER ELECTRONIC DIVISION FEDERAL PACIFIC ELECTRIC CO.	2652 DALRYMPLE ST.	SANFORD, NC 27330
09353	C AND K COMPONENTS, INC.	103 MORSE STREET	WATERTOWN, MA 02172
11237	CTS KEENE, INC.	3230 RIVERSIDE AVE.	PASO ROBLES, CA 93446
14939	DELBAR PRODUCTS INC.	7TH AND SPRUCE	PERKASIE, PA 18944
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
24546	CORNING GLASS WORKS, ELECTRONIC COMPONENTS DIVISION	550 HIGH STREET	BRADFORD, PA 16701
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
33096	COLORADO CRYSTAL CORPORATION	2303 W 8TH STREET	LOVELAND, CO 80537
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
34430	MONSANTO COMMERCIAL PRODUCT, CO. FABRICATOR PRODUCTS DIV.	BOX 3790, 611 EAST CERRITOS AVE.	ANAHEIM, CA 92803
50522	MONSANTO CO., ELECTRONIC SPECIAL PRODUCTS	3400 HILLVIEW AVENUE	PALO ALTO, CA 94304
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.		NORTH ADAMS, MA 01247
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
82877	ROTRON, INC.	7-9 HASBROUCK LANE	WOODSTOCK, NY 12498
91418	RADIO MATERIALS COMPANY, DIV. OF P.R. MALLORY AND COMPANY, INC.	4242 W BRYN MAWR	CHICAGO, IL 60646
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
97222	FOSTER AND KLEISER DIVISION OF METROMEDIA INC.	1601 MARITIME ST.	OAKLAND, CA 94623

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-5300-01			CKT BOARD ASSY:SYSTEM PROCESSOR	80009	670-5300-01
A5	670-5299-01			CKT BOARD ASSY:DEBUG AND FRONT PANEL I/O	80009	670-5299-01
A10	670-5220-00			CKT BOARD ASSY:ASSEMBLER PROCESSOR	80009	670-5220-00
A15	670-5381-00			CKT BOARD ASSY:8001 SYSTEM MEMORY	80009	670-5381-00
A20A1	670-5298-02			CKT BOARD ASSY:16K DYNAMIC RAM	80009	670-5298-02
A20A2	670-5297-02			CKT BOARD ASSY:16K DYNAMIC RAM	80009	670-5297-02
A25A1	670-5505-03			CKT BOARD ASSY:HIGH SPEED(PROGRAM)MEMORY	80009	670-5505-03
A25A2	670-5659-01			CKT BOARD ASSY:HIGH SPEED(SYSTEM)MEMORY	80009	670-5659-01
A30	670-5219-01			CKT BOARD ASSY:SYSTEM COMMUNICATION	80009	670-5219-01
A35	670-5313-00			CKT BOARD ASSY:MOTHER	80009	670-5313-00
A40	670-5378-00			CKT BOARD ASSY:LOWER FRONT PANEL	80009	670-5378-00
A40A2	670-5225-00			CKT BOARD ASSY:PROM SOCKET	80009	670-5225-00
A45	118-0512-00			CKT BOARD ASSY:HCC15-3	80009	118-0512-00
A50	118-0513-00			CKT BOARD ASSY:F5-25	80009	118-0513-00
A1	670-5300-01			CKT BOARD ASSY:SYSTEM PROCESSOR	80009	670-5300-01
C1013	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1049	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1085	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1105	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1119	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1126	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1129	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1161	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C1162	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C1163	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C2039	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2041	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2069	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2119	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2148	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2162	283-0698-00			CAP.,FXD,MICA D:390PF,1%,500V	09023	CD15ED391F03
C3046	283-0648-00			CAP.,FXD,MICA D:10PF,5%,100V	00853	D151C100D0
C3101	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3129	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3149	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3173	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4025	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4049	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4061	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4141	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4155	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4173	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4179	283-0648-00			CAP.,FXD,MICA D:10PF,5%,100V	00853	D151C100D0
C5035	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5036	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C5066	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5125	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5172	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
CR2152	152-0233-00			SEMICOND DEVICE:SILICON,85V,100MA	80009	152-0233-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
CR2171	152-0233-00			SEMICOND DEVICE:SILICON,85V,100MA	80009	152-0233-00
R1015	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1021	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1069	307-0598-00			RES NTWK,FXD FI:7,330 OHM,2%,1.0W	91637	CSP08G01331G
R1071	307-0605-00			RES NTWK,FXD FI:7,470 OHM,2%,0.15W	91637	CSP08G01-471G
R1079	307-0598-00			RES NTWK,FXD FI:7,330 OHM,2%,1.0W	91637	CSP08G01331G
R1081	307-0605-00			RES NTWK,FXD FI:7,470 OHM,2%,0.15W	91637	CSP08G01-471G
R1092	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1093	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1094	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R1099	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R1119	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R1121	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1128	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1131	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
R1132	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
R1136	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
R1139	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1141	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
R1146	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1155	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1176	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1177	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1178	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R2085	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R2091	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R2099	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
R2133	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R2143	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R2152	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R2171	321-0247-00			RES.,FXD,FILM:3.65K OHM,1%,0.125W	91637	MFF1816G36500F
R2177	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R3036	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
R3039	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
R3055	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R3076	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
R3091	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R3155	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R3171	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R4121	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
R4129	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R4145	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R4165	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R4176	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
R5032	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R5055	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R5071	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
R5085	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R5101	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R5102	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
R5104	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
R5155	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R5165	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
R5172	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
S1141	118-0319-00			SW,CODE IND WHL:THUMBWHEEL,10POSN,1 SECT	00779	435-128-1
U1010	156-0361-00			MICROCIRCUIT,DI:UNIV A SYN RCVR XMTR	14939	AY-5-1013A
U1030	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U1040	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	80009	156-0222-00
U1050	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U1060	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U1080	156-0061-00			MICROCIRCUIT,DI:SGL,BCD TO DEC DECODER	01295	SN7442N
U1090	156-0061-00			MICROCIRCUIT,DI:SGL,BCD TO DEC DECODER	01295	SN7442N
U1100	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U1110	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U1120	156-0997-00			MICROCKT,INTFC:DUAL COMM LINE DRIVER	80009	156-0997-00
U1130	156-0995-00			MICROCKT,INTFC:DUAL COMM LINE RCVR W/HYST	80009	156-0995-00
U1150	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U1160	156-0325-00			MICROCIRCUIT,DI:DUAL 4-1 LINE,SEL/MULT	01295	SN74S153N
U2030	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U2040	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	80009	156-0222-00
U2050	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U2060	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U2070	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U2080	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U2090	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U2100	156-0035-00			MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE	80009	156-0035-00
U2110	156-0061-00			MICROCIRCUIT,DI:SGL,BCD TO DEC DECODER	01295	SN7442N
U2120	156-0061-00			MICROCIRCUIT,DI:SGL,BCD TO DEC DECODER	01295	SN7442N
U2130	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U2140	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U2150	156-0462-00			MICROCIRCUIT,DI:HEX SCHMITT TRIG,TTL	80009	156-0462-00
U2160	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U2170	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U3010	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U3020	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U3040	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U3050	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U3060	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U3070	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U3080	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U3090	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U3100	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U3110	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U3120	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U3130	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U3140	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U3150	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U3160	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U3170	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U4010	156-0986-00			MICROCIRCUIT,DI:MICROPROCESSOR,8 BIT	18324	2650
U4030	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U4040	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U4050	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U4060	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U4070	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U4080	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U4090	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U4100	156-0219-00			MICROCIRCUIT,DI:8-INPUT PRIORITY DCDR	07263	9318DC
U4110	156-0219-00			MICROCIRCUIT,DI:8-INPUT PRIORITY DCDR	07263	9318DC
U4120	156-0153-00			MICROCIRCUIT,DI:HEX INVERT,W/OPEN COIL	01295	SN7406N
U4130	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U4140	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U4150	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U4160	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U4170	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U5030	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U5040	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U5060	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U5070	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U5080	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	80009	156-0222-00
U5090	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	80009	156-0222-00
U5110	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	80009	156-0222-00
U5120	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U5130	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U5140	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U5150	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U5160	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
Y3033	158-0107-00			XTAL UNIT,QTZ:10MHZ,0.0015% SERIES	80009	158-0107-00
Y5173	158-0155-00			XTAL UNIT,QTZ:9.984MHZ,0.015%,PARALLEL	33096	PB-1167

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A5	670-5299-01			CKT BOARD ASSY:DEBUG AND FRONT PANEL I/O	80009	670-5299-01
C1015	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1075	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1098	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1114	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C1161	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2025	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2075	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2091	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2095	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2161	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3095	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3115	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3135	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3159	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4025	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4115	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4151	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5019	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5025	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5028	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C5035	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5089	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5105	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5166	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
R1085	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1095	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1115	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
R1135	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
R2015	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R2135	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R3155	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R4095	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
R5121	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R5135	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R5162	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
U1010	156-0035-00			MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE	80009	156-0035-00
U1020	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U1030	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U1040	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U1050	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U1060	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U1070	156-0690-00			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74S02N
U1080	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U1090	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U1100	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U1110	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U1120	156-0035-00			MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE	80009	156-0035-00
U1130	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U1140	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U1150	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U1160	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U2010	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U2020	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U2030	156-0989-00			MICROCIRCUIT,DI:4 X 4 RGTR FILE W/3 STATE	80009	156-0989-00
U2040	156-0990-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATE	80009	156-0990-00
U2050	156-0989-00			MICROCIRCUIT,DI:4 X 4 RGTR FILE W/3 STATE	80009	156-0989-00
U2060	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U2070	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U2080	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U2090	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	80009	156-0222-00
U2100	156-0219-00			MICROCIRCUIT,DI:8-INPUT PRIORITY DCDR	07263	9318DC
U2110	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U2120	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U2130	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U2140	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U2150	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U2160	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U3010	156-0125-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0125-00
U3020	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	80009	156-0222-00
U3030	156-0989-00			MICROCIRCUIT,DI:4 X 4 RGTR FILE W/3 STATE	80009	156-0989-00
U3040	156-0990-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATE	80009	156-0990-00
U3050	156-0989-00			MICROCIRCUIT,DI:4 X 4 RGTR FILE W/3 STATE	80009	156-0989-00
U3060	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U3070	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U3080	156-0990-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATE	80009	156-0990-00
U3090	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U3100	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U3110	156-0034-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	80009	156-0034-00
U3120	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U3130	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U3140	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U3150	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U3160	156-0034-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	80009	156-0034-00
U4010	156-0061-00			MICROCIRCUIT,DI:SGL,BCD TO DEC DECODER	01295	SN7442N
U4020	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U4030	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U4040	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U4050	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U4060	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U4070	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U4080	156-0034-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	80009	156-0034-00
U4090	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U4100	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U4110	156-0690-00			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74S02N
U4120	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U4130	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U4140	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U4150	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U4160	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U5010	156-0125-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0125-00
U5020	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U5030	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U5040	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U5050	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U5060	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U5070	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U5080	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U5090	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U5100	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U5110	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U5120	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U5130	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U5140	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U5150	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U5160	156-0034-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	80009	156-0034-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10	670-5220-00			CKT BOARD ASSY:ASSEMBLER PROCESSOR	80009	670-5220-00
C3039	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3077	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3099	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5023	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C5031	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5054	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5091	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
R3035	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R3085	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R3091	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
R4101	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R5073	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
U3030	156-0866-00			MICROCIRCUIT,DI:13 INP NAND GATES	80009	156-0866-00
U3040	156-0983-00			MICROCIRCUIT,DI:MICROPROCESSOR EIGHT BIT	80009	156-0983-00
U3060	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U3080	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U3090	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U3100	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U4030	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U4060	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U4080	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	01295	SN74LS02N
U4090	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U4100	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U5030	156-0985-00			MICROCIRCUIT,DI:DUAL 5-INPUT NOR GATE	80009	156-0985-00
U5040	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U5050	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U5060	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U5080	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U5090	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U5100	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A15	670-5381-00			CKT BOARD ASSY:8001 SYSTEM MEMORY	80009	670-5381-00
C1013	283-0128-00			CAP.,FXD,CER DI:100PF,5%,500V	72982	871-536T2H101J
C1024	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1055	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1074	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1098	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1125	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2012	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2023	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2033	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C2034	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2044	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2053	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C2054	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2074	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2088	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2092	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2109	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3025	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3044	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3064	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3074	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3084	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3094	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3104	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3112	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3114	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4011	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C5012	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C5025	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C5029	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C5035	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C5075	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C5105	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
Q1030	156-0846-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	80009	156-0846-00
R1012	321-0299-00			RES.,FXD,FILM:12.7K OHM,1%,0.125W	91637	MFF1816G12701F
R1038	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1051	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1067	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1068	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625
R2000	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R2024	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R2025	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R5032	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R5055	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625
R5065	307-0595-00			RES NTWK,FXD FI:7,5.6K OHM,2%,1.0W	32997	4308R-101-562
R5082	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R5112	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
U1010	156-0405-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	07263	9602PC
U1020	156-0386-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10N
U1040	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U1050	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U1060	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U1070	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC RAM	80009	156-0291-00
U1080	156-0291-00			MICROCIRCUIT,DI:1024 BIT X STATIC RAM	80009	156-0291-00
U1090	156-1028-00			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1028-00
U1100	156-1028-00			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1028-00
U1110	156-1028-00			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1028-00
U1120	156-1028-00			MICROCIRCUIT,DI:1024 X 4 STATIC RAM	80009	156-1028-00
U2010	156-0464-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	80009	156-0464-00
U2020	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U2030	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U2040	156-0990-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATE	80009	156-0990-00
U2050	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	01295	SN74LS02N
U2060	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U2070	156-0391-00			MICROCIRCUIT,DI:HEX LATCH WITH CLEAR	01295	SN74LS174N
U2080	156-0061-00			MICROCIRCUIT,DI:SGL,BCD TO DEC DECODER	01295	SN7442N
U2090	156-0061-00			MICROCIRCUIT,DI:SGL,BCD TO DEC DECODER	01295	SN7442N
U2100	156-0061-00			MICROCIRCUIT,DI:SGL,BCD TO DEC DECODER	01295	SN7442N
U2110	156-1084-00			MICROCIRCUIT,DI:9 INPUT PARITY GEN/CHECKER	80009	156-1084-00
U2120	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	01295	SN74LS02N
U3010	156-0061-00			MICROCIRCUIT,DI:SGL,BCD TO DEC DECODER	01295	SN7442N
U3030	160-0008-00			MICROCIRCUIT,DI:2048 X 8 E PROM,PROGRAMMED	80009	160-0008-00
U3040	160-0009-00			MICROCIRCUIT,DI:2048 X 8 E PROM,PROGRAMMED	80009	160-0009-00
U3050	160-0002-00			MICROCIRCUIT,DI:2048 X 8 E PROM,PROGRAMMED	80009	160-0002-00
U3060	160-0005-00			MICROCIRCUIT,DI:2048 X 8 E PROM,PROGRAMMED	80009	160-0005-00
U3070	160-0004-00			MICROCIRCUIT,DI:2048 X 8 E PROM,PROGRAMMED	80009	160-0004-00
U4010	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U4040	160-0007-00			MICROCIRCUIT,DI:2048 X 8 E PROM,PROGRAMMED	80009	160-0007-00
U4050	160-0006-00			MICROCIRCUIT,DI:2048 X 8 E PROM,PROGRAMMED	80009	160-0006-00
U4060	160-0003-00			MICROCIRCUIT,DI:2048 X 8 E PROM,PROGRAMMED	80009	160-0003-00
U5010	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U5020	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U5030	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U5040	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U5050	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U5060	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U5070	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U5080	156-0866-00			MICROCIRCUIT,DI:13 INP NAND GATES	80009	156-0866-00
U5090	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U5100	156-0985-00			MICROCIRCUIT,DI:DUAL 5-INPUT NOR GATE	80009	156-0985-00
U5110	156-0464-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	80009	156-0464-00
U5120	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	01295	SN74LS02N

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20A1	670-5298-02			CKT BOARD ASSY:16K DYNAMIC RAM	80009	670-5298-02
C1001	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1012	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1024	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1031	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1035	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1044	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1051	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1065	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1071	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1084	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1101	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1119	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1135	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1171	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2001	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2005	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2011	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2025	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2031	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2035	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2045	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2051	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2065	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2071	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2075	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2084	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2102	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2131	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2175	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3001	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3005	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3011	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3025	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3031	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3035	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3045	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3051	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3065	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3071	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3084	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3095	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3097	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3111	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3118	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3125	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3155	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3171	283-0676-00			CAP.,FXD,MICA D:82PF,1%,500V	00853	D105E820F0
C3173	283-0028-00			CAP.,FXD,CER DI:0.0022UF,20%,50V	56289	19C606
C4001	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4005	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4006	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
C4011	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4025	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4031	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4035	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4045	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4051	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4065	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4071	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4075	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4084	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4116	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4125	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4149	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4154	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4165	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5079	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C5169	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C6004	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C6006	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C6009	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C6029	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C6046	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
DL1140	119-0982-00			DELAY LINE,ELEC:200NS,100 OHM	97222	EP7046
R1085	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R1089	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R1091	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R1092	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R1093	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R1096	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R1141	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R2085	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R2089	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R2091	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R2096	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R2101	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R2109	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R2111	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R2135	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R2169	321-0335-00			RES.,FXD,FILM:30.1K OHM,1%,0.125W	91637	MFF1816G30101F
R3085	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R3087	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R3165	321-0335-00			RES.,FXD,FILM:30.1K OHM,1%,0.125W	91637	MFF1816G30101F
R4085	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R4097	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R4145	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R4171	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
R5085	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R5089	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R5165	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R6006	321-0291-00			RES.,FXD,FILM:10.5K OHM,1%,0.125W	91637	MFF1816G10501F
R6007	321-0303-00			RES.,FXD,FILM:14K OHM,1%,0.125W	91637	MFF1816G14001F
R6040	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R6155	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
R6159	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
R6165	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
S4163	118-0320-00			SWITCH,SLIDE:4 SPST,50M AMP,24V	11237	206-4
U1000	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1010	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1020	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1030	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1040	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1050	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1060	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1070	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1080	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1090	156-0125-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0125-00
U1100	156-0948-00			MICROCIRCUIT,DI:QUAD D FLIP-FLOP	80009	156-0948-00
U1110	156-0992-00			MICROCIRCUIT,DI:QUAD TTL-TO MOS DRIVER	80009	156-0992-00
U1120	156-0693-00			MICROCIRCUIT,DI:DECODER/DEMULTIPLEXER	01295	SN74S139N
U1130	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U1140	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U1150	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U1160	156-0180-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00N
U1170	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U2000	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2010	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2020	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2030	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2040	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2050	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2060	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2070	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2080	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2090	156-0125-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0125-00
U2100	156-0035-00			MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE	80009	156-0035-00
U2110	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U2120	156-0180-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00N
U2130	156-0125-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0125-00
U2140	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U2150	156-0118-00			MICROCIRCUIT,DI:J-K MASTER-SLAVE FLIP-FLOP	01295	SN74S112N
U2160	156-0180-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00N
U2170	156-0118-00			MICROCIRCUIT,DI:J-K MASTER-SLAVE FLIP-FLOP	01295	SN74S112N
U3000	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3010	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3020	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3030	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3040	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3050	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3060	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3070	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3080	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3090	156-0325-00			MICROCIRCUIT,DI:DUAL 4-1 LINE,SEL/MULT	01295	SN74S153N
U3100	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U3110	156-1014-00			MICROCIRCUIT,DI:9 BIT ODD/EVEN PTY GEN/CHK	80009	156-1014-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U3120	156-0035-00			MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE	80009	156-0035-00
U3130	156-0462-00			MICROCIRCUIT,DI:HEX SCHMITT TRIG,TTL	80009	156-0462-00
U3140	156-1014-00			MICROCIRCUIT,DI:9 BIT ODD/EVEN PTY GEN/CHK	80009	156-1014-00
U3150	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U3160	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U3170	156-0405-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	07263	9602PC
U4000	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4010	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4020	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4030	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4040	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4050	150-1000-00			LT EMITIING DIO:RED,650NM,40MA MAX	34430	MV-50
U4060	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4070	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4080	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4090	156-0325-00			MICROCIRCUIT,DI:DUAL 4-1 LINE,SEL/MULT	01295	SN74S153N
U4100	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U4110	156-0948-00			MICROCIRCUIT,DI:QUAD D FLIP-FLOP	80009	156-0948-00
U4120	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U4130	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U4140	156-0391-00			MICROCIRCUIT,DI:HEX LATCH WITH CLEAR	01295	SN74LS174N
U4150	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U4170	156-0043-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NOR GATE	80009	156-0043-00
U5090	156-0325-00			MICROCIRCUIT,DI:DUAL 4-1 LINE,SEL/MULT	01295	SN74S153N
U5100	156-0125-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0125-00
U5110	156-0948-00			MICROCIRCUIT,DI:QUAD D FLIP-FLOP	80009	156-0948-00
U5120	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U5130	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U5140	156-0391-00			MICROCIRCUIT,DI:HEX LATCH WITH CLEAR	01295	SN74LS174N
U5150	156-0990-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATE	80009	156-0990-00
U5160	156-0180-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00N
U5170	156-0153-00			MICROCIRCUIT,DI:HEX INVERT,W/OPEN COIL	01295	SN7406N
U6010	160-0036-01			MICROCIRCUIT,DI:PROM 8 BIT WORD PROGRAMMED	80009	160-0036-01
U6030	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U6040	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
VR6031	152-0243-00			SEMICOND DEVICE:ZENER,0.4W,15V,5%	80009	152-0243-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20A2	670-5297-02			CKT BOARD ASSY:16K DYNAMIC RAM	80009	670-5297-02
C1001	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1012	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1024	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1031	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1035	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1044	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1051	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1065	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1071	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1084	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C1101	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1119	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1135	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1171	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2001	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2005	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2011	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2025	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2031	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2035	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2045	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2051	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2065	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2071	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2075	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2084	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C2102	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2131	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2175	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3001	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3005	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3011	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3025	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3031	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3035	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3045	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3051	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3065	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3071	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3084	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3095	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C3097	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3111	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3118	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3125	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3155	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3171	283-0676-00			CAP.,FXD,MICA D:82PF,1%,500V	00853	D105E820F0
C3173	283-0028-00			CAP.,FXD,CER DI:0.0022UF,20%,50V	56289	19C606
C4001	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4005	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4006	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
C4011	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4025	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4031	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4035	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4045	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4051	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4065	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4071	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4075	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4084	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C4116	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4125	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4149	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4154	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4165	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C5079	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C5169	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C6004	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C6006	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	72982	8121-N088Z5U104M
C6009	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C6029	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C6046	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
DL1140	119-0982-00			DELAY LINE,ELEC:200NS,100 OHM	97222	EP7046
R1085	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R1089	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R1091	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R1092	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R1093	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R1096	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R1141	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R2085	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R2091	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R2096	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R2101	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R2109	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R2111	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R2135	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R2155	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R2169	321-0335-00			RES.,FXD,FILM:30.1K OHM,1%,0.125W	91637	MFF1816G30101F
R3085	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R3089	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R3165	321-0335-00			RES.,FXD,FILM:30.1K OHM,1%,0.125W	91637	MFF1816G30101F
R4085	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R4097	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R4171	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
R5085	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R5089	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R5165	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R6007	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
R6040	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R6155	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
R6159	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
R6165	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
S4163	118-0320-00			SWITCH,SLIDE:4 SPST,50M AMP,24V	11237	206-4
U1000	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1010	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1020	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1030	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1040	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1050	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1060	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1070	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1080	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U1090	156-0125-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0125-00
U1100	156-0948-00			MICROCIRCUIT,DI:QUAD D FLIP-FLOP	80009	156-0948-00
U1110	156-0992-00			MICROCIRCUIT,DI:QUAD TTL-TO MOS DRIVER	80009	156-0992-00
U1120	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U1130	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U1150	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U1160	156-0180-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00N
U1170	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U2000	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2010	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2020	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2030	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2040	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2050	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2060	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2070	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2080	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U2090	156-0125-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0125-00
U2100	156-0035-00			MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE	80009	156-0035-00
U2110	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U2120	156-0180-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00N
U2130	156-0125-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0125-00
U2140	156-0690-00			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74S02N
U2150	156-0118-00			MICROCIRCUIT,DI:J-K MASTER-SLAVE FLIP-FLOP	01295	SN74S112N
U2160	156-0180-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00N
U2170	156-0118-00			MICROCIRCUIT,DI:J-K MASTER-SLAVE FLIP-FLOP	01295	SN74S112N
U3000	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3010	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3020	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3030	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3040	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3050	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3060	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3070	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3080	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U3090	156-0325-00			MICROCIRCUIT,DI:DUAL 4-1 LINE,SEL/MULT	01295	SN74S153N
U3100	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U3110	156-1014-00			MICROCIRCUIT,DI:9 BIT ODD/EVEN PTY GEN/CHK	80009	156-1014-00
U3120	156-0035-00			MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE	80009	156-0035-00
U3130	156-0462-00			MICROCIRCUIT,DI:HEX SCHMITT TRIG,TTL	80009	156-0462-00
U3140	156-1014-00			MICROCIRCUIT,DI:9 BIT ODD/EVEN PTY GEN/CHK	80009	156-1014-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U3150	156-0690-00			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74S02N
U3160	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U3170	156-0405-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	07263	9602PC
U3090	156-0325-00			MICROCIRCUIT,DI:DUAL 4-1 LINE,SEL/MULT	01295	SN74S153N
U4000	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4010	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4020	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4030	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4040	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4050	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4060	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4070	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4080	156-1000-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM	80009	156-1000-00
U4090	156-0325-00			MICROCIRCUIT,DI:DUAL 4-1 LINE,SEL/MULT	01295	SN74S153N
U4100	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U4110	156-0948-00			MICROCIRCUIT,DI:QUAD D FLIP-FLOP	80009	156-0948-00
U4120	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U4130	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U4140	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	80009	156-0222-00
U4150	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
U4170	156-0690-00			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74S02N
U5090	156-0325-00			MICROCIRCUIT,DI:DUAL 4-1 LINE,SEL/MULT	01295	SN74S153N
U5100	156-0125-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND BFR	80009	156-0125-00
U5110	156-0948-00			MICROCIRCUIT,DI:QUAD D FLIP-FLOP	80009	156-0948-00
U5120	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U5130	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U5140	156-0222-00			MICROCIRCUIT,DI:HEX.LATCH	80009	156-0222-00
U5150	156-0990-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATE	80009	156-0990-00
U5160	156-0180-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00N
U5170	156-0153-00			MICROCIRCUIT,DI:HEX INVERT,W/OPEN COIL	01295	SN7406N
U6010	160-0036-01			MICROCIRCUIT,DI:PROM 8 BIT WORD PROGRAMMED	80009	160-0036-01
U6030	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U6040	156-0323-00			MICROCIRCUIT,DI:HEX. INVERTER	01295	SN74S04N
VR6006	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	80009	152-0195-00
VR6031	152-0278-00			SEMICOND DEVICE:ZENER,0.4W,3V,5%	07910	1N4372A

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A25A1	670-5505-03			CKT BOARD ASSY:HIGH SPEED(PROGRAM)MEMORY	80009	670-5505-03
C2025	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2031	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2035	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2041	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2051	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2055	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2061	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2071	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2075	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2081	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2091	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2095	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2101	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2132	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2162	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3011	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C3025	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3041	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3045	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3061	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3065	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3081	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3085	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3101	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3105	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3125	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3144	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3189	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4031	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4035	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4051	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4055	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4071	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4075	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4091	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4095	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4185	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5011	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C5021	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5025	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5029	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5041	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5045	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5049	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5061	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5065	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5069	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5081	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5085	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5089	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5101	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
C5105	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5109	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5131	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C6066	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C6116	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C6161	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C7011	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C7042	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C7121	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C7174	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C8148	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
DL2140	119-0982-00			DELAY LINE,ELEC:200NS,100 OHM	97222	EP7046
R2118	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R2121	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R2141	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R2145	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R3112	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
R3114	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R4112	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
R4114	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R4141	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R4147	307-0595-00			RES NTWK,FXD FI:7,5.6K OHM,2%,1.0W	32997	4308R-101-562
R5111	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R5112	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R5113	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R5114	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R5115	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R5116	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R5117	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R5118	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R6067	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R7048	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
R7147	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
S4140	260-1589-00			SWITCH,PUSH:(6)SPST,0.1A,5V	00779	435166-4
U1110	156-0381-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATES	01295	SN74LS86N
U2020	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2030	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2040	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2050	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2060	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2070	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2080	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2090	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2100	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2120	156-0321-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	80009	156-0321-00
U2130	156-0180-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00N
U2150	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U2160	156-0304-00			MICROCIRCUIT,DI:DUAL 4-INPUT,NAND GATE	18324	N74S20A
U2170	156-0180-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00N
U2180	156-0617-00			MICROCIRCUIT,DI:DUAL 4 BIT BIN COUNTER	01295	SN74393N

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U3020	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3030	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3040	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3050	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3060	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3070	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3080	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3090	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3100	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3120	156-0321-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	80009	156-0321-00
U3130	156-0693-00			MICROCIRCUIT,DI:DECODER/DEMULTIPLEXER	01295	SN74S139N
U3140	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U3150	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	01295	SN74LS02N
U3160	156-0118-00			MICROCIRCUIT,DI:J-K MASTER-SLAVE FLIP-FLOP	01295	SN74S112N
U3170	156-0118-00			MICROCIRCUIT,DI:J-K MASTER-SLAVE FLIP-FLOP	01295	SN74S112N
U3180	156-1059-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED FF	80009	156-1059-00
U4020	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4030	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4040	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4050	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4060	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4070	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4080	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4090	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4100	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4120	156-0965-00			MICROCIRCUIT,DI:ADRS MUX REFRESH CNTR	80009	156-0965-00
U4150	156-1041-00			MICROCIRCUIT,DI:4 BIT MAGNITUDE COMPARATOR	80009	156-1041-00
U4160	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U4170	156-0985-00			MICROCIRCUIT,DI:DUAL 5-INPUT NOR GATE	80009	156-0985-00
U4180	156-0804-00			MICROCIRCUIT,DI:QUADRUPLE S-R LATCH	07263	74LS279PC
U5020	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5030	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5040	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5050	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5060	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5070	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5080	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5090	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5100	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5140	156-0153-00			MICROCIRCUIT,DI:HEX INVERT,W/OPEN COIL	01295	SN7406N
U5150	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U5160	156-1059-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED FF	80009	156-1059-00
U5170	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	01295	SN74LS02N
U5180	156-0480-00			MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	80009	156-0480-00
U6020	156-1014-00			MICROCIRCUIT,DI:9 BIT ODD/EVEN PTY GEN/CHK	80009	156-1014-00
U6030	156-0948-00			MICROCIRCUIT,DI:QUAD D FLIP-FLOP	80009	156-0948-00
U6040	156-0948-00			MICROCIRCUIT,DI:QUAD D FLIP-FLOP	80009	156-0948-00
U6070	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U6080	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U6090	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U6100	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U6110	156-1014-00			MICROCIRCUIT,DI:9 BIT ODD/EVEN PTY GEN/CHK	80009	156-1014-00
U6120	156-0464-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	80009	156-0464-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U3020	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3030	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3040	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3050	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3060	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3070	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3080	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3090	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3100	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U3120	156-0321-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	80009	156-0321-00
U3130	156-0693-00			MICROCIRCUIT,DI:DECODER/DEMULTIPLEXER	01295	SN74S139N
U3140	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U3150	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	01295	SN74LS02N
U3160	156-0118-00			MICROCIRCUIT,DI:J-K MASTER-SLAVE FLIP-FLOP	01295	SN74S112N
U3170	156-0118-00			MICROCIRCUIT,DI:J-K MASTER-SLAVE FLIP-FLOP	01295	SN74S112N
U3180	156-1059-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED FF	80009	156-1059-00
U4020	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4030	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4040	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4050	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4060	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4070	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4080	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4090	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4100	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U4120	156-0965-00			MICROCIRCUIT,DI:ADRS MUX REFRESH CNTR	80009	156-0965-00
U4150	156-1041-00			MICROCIRCUIT,DI:4 BIT MAGNITUDE COMPARATOR	80009	156-1041-00
U4160	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U4170	156-0985-00			MICROCIRCUIT,DI:DUAL 5-INPUT NOR GATE	80009	156-0985-00
U4180	156-0804-00			MICROCIRCUIT,DI:QUADRUPLE S-R LATCH	07263	74LS279PC
U5020	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5030	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5040	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5050	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5060	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5070	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5080	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5090	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5100	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U5140	156-0153-00			MICROCIRCUIT,DI:HEX INVERT,W/OPEN COIL	01295	SN7406N
U5150	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U5160	156-1059-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED FF	80009	156-1059-00
U5170	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	01295	SN74LS02N
U5180	156-0480-00			MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	80009	156-0480-00
U6020	156-1014-00			MICROCIRCUIT,DI:9 BIT ODD/EVEN PTY GEN/CHK	80009	156-1014-00
U6030	156-0948-00			MICROCIRCUIT,DI:QUAD D FLIP-FLOP	80009	156-0948-00
U6040	156-0948-00			MICROCIRCUIT,DI:QUAD D FLIP-FLOP	80009	156-0948-00
U6070	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U6080	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U6090	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U6100	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U6110	156-1014-00			MICROCIRCUIT,DI:9 BIT ODD/EVEN PTY GEN/CHK	80009	156-1014-00
U6120	156-0464-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	80009	156-0464-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U6130	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U6140	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U6150	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U6160	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U6170	156-0180-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00N
U6180	156-0480-00			MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	80009	156-0480-00
U7140	156-0035-00			MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE	80009	156-0035-00
U7150	156-1059-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED FF	80009	156-1059-00
U7160	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U7170	156-0645-00			MICROCIRCUIT,DI:SCHMITT-TRIG POS NAND GATE	01295	SN74LS14N
U7180	156-0386-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10N
U8160	156-1059-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED FF	80009	156-1059-00
VR7047	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	80009	152-0195-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A25A2	670-5659-01			CKT BOARD ASSY:HIGH SPEED(SYSTEM)MEMORY	80009	670-5659-01
C2025	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2031	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2035	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2041	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2051	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2055	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2061	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2071	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2075	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2081	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2091	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2095	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2101	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2132	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C2162	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3011	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C3025	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3041	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3045	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3061	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3065	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3081	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3085	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3101	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3105	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3125	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3144	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C3189	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4031	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4035	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4051	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4055	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4071	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4075	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4091	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4095	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C4185	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5011	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C5021	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5025	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5029	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5041	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5045	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5049	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5061	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5065	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5069	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5081	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5085	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5089	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5101	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
C5105	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5109	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C5131	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C6066	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C6116	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C6161	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C7011	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C7042	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C7121	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C7174	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
C8148	283-0023-00			CAP.,FXD,CER DI:0.1UF,+80-20%,12V	91418	MX0104Z1205R5
DL2140	119-0982-00			DELAY LINE,ELEC:200NS,100 OHM	97222	EP7046
R2118	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R2121	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R2141	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R2145	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
R3112	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
R3114	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R4112	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
R4114	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R4141	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R4147	307-0595-00			RES NTWK,FXD FI:7,5.6K OHM,2%,1.0W	32997	4308R-101-562
R5111	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R5112	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R5113	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R5114	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R5115	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R5116	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R5117	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R5118	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
R6067	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R7048	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
R7147	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
S4140	260-1589-00			SWITCH,PUSH:(6)SPST,0.1A,5V	00779	435166-4
U1110	156-0381-00			MICROCIRCUIT,DI:QUAD 2-INPUT EXCL OR GATES	01295	SN74LS86N
U2020	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2030	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2040	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2050	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2060	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2070	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2080	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2090	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2100	156-1112-00			MICROCIRCUIT,DI:4096 X 1 DYNAMIC RAM,16 DIP	80009	156-1112-00
U2120	156-0321-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	80009	156-0321-00
U2130	156-0180-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00N
U2150	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U2160	156-0304-00			MICROCIRCUIT,DI:DUAL 4-INPUT,NAND GATE	18324	N74S20A
U2170	156-0180-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00N
U2180	156-0617-00			MICROCIRCUIT,DI:DUAL 4 BIT BIN COUNTER	01295	SN74393N

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U6130	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U6140	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U6150	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U6160	156-0530-00			MICROCIRCUIT,DI:QUAD 2-INP MUX,16 PIN DIP	80009	156-0530-00
U6170	156-0180-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74S00N
U6180	156-0480-00			MICROCIRCUIT,DI:QUAD 2-INPUT AND GATE	80009	156-0480-00
U7050	160-0118-00			MICROCIRCUIT,DI:512 X 8 PROM,PROGRAMMED	80009	160-0118-00
U7140	156-0035-00			MICROCIRCUIT,DI:SGL 8-INPUT POS NAND GATE	80009	156-0035-00
U7150	156-1059-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED FF	80009	156-1059-00
U7160	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U7170	156-0645-00			MICROCIRCUIT,DI:SCHMITT-TRIG POS NAND GATE	01295	SN74LS14N
U7180	156-0386-00			MICROCIRCUIT,DI:TRIPLE 3-INPUT NAND GATE	01295	SN74LS10N
U8160	156-1059-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIGGERED FF	80009	156-1059-00
VR7047	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	80009	152-0195-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A30	670-5219-01			CKT BOARD ASSY:SYSTEM COMMUNICATION	80009	670-5219-01
C1013	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C1028	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1045	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1069	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1072	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1085	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C1106	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2035	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2055	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2069	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2085	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3011	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3051	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C3081	283-0649-00			CAP.,FXD,MICA D:105PF,1%,300V	00853	D153F1050F0
C3085	283-0648-00			CAP.,FXD,MICA D:10PF,5%,100V	00853	D151C100D0
C3095	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4017	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C4021	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4028	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C4045	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4065	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4103	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4131	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
R1031	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
R1036	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R1053	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
R1054	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
R1083	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
R1084	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
R1099	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R3016	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
R3074	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R3086	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
R3089	321-0816-00			RES.,FXD,FILM:5K OHM,1%,0.125W	24546	NA55D5000F
R3094	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
R3096	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
R4099	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
R4105	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R5044	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R5045	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
R5041	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
R5051	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
U1020	156-0997-00			MICROCKT,INTFC:DUAL COMM LINE DRIVER	80009	156-0997-00
U1030	156-0995-00			MICROCKT,INTFC:DUAL COMM LINE RCVR W/HYST	80009	156-0995-00
U1040	156-0995-00			MICROCKT,INTFC:DUAL COMM LINE RCVR W/HYST	80009	156-0995-00
U1050	156-0995-00			MICROCKT,INTFC:DUAL COMM LINE RCVR W/HYST	80009	156-0995-00
U1060	156-0997-00			MICROCKT,INTFC:DUAL COMM LINE DRIVER	80009	156-0997-00
U1070	156-0995-00			MICROCKT,INTFC:DUAL COMM LINE RCVR W/HYST	80009	156-0995-00
U1080	156-0997-00			MICROCKT,INTFC:DUAL COMM LINE DRIVER	80009	156-0997-00
U1090	156-0995-00			MICROCKT,INTFC:DUAL COMM LINE RCVR W/HYST	80009	156-0995-00
U1110	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U2010	156-0984-00			MICROCIRCUIT,DI:256 X 1 RAM	80009	156-0984-00
U2020	156-0984-00			MICROCIRCUIT,DI:256 X 1 RAM	80009	156-0984-00
U2030	156-0061-00			MICROCIRCUIT,DI:SGL,BCD TO DEC DECODER	01295	SN7442N
U2040	156-0464-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	80009	156-0464-00
U2050	156-0385-00			MICROCIRCUIT,DI:HEX.INVERTER	01295	SN74LS04N
U2060	156-0383-00			MICROCIRCUIT,DI:QUAD 2-INPUT NOR GATE	01295	SN74LS02N
U2070	156-0985-00			MICROCIRCUIT,DI:DUAL 5-INPUT NOR GATE	80009	156-0985-00
U2080	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U2100	156-0658-00			MICROCIRCUIT,DI:ASYNCHRONOUS COMM INT ADPT	80009	156-0658-00
U2120	156-0658-00			MICROCIRCUIT,DI:ASYNCHRONOUS COMM INT ADPT	80009	156-0658-00
U2130	156-0658-00			MICROCIRCUIT,DI:ASYNCHRONOUS COMM INT ADPT	80009	156-0658-00
U3010	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00
U3020	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U3030	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U3040	156-0465-00			MICROCIRCUIT,DI:8-INPUT NAND GATE	27014	DM74LS304
U3050	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U3060	156-0464-00			MICROCIRCUIT,DI:DUAL 4-INPUT NAND GATE	80009	156-0464-00
U3070	156-0382-00			MICROCIRCUIT,DI:QUAD 2-INPUT NAND GATE	01295	SN74LS00N
U3080	156-0405-00			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	07263	9602PC
U3130	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U4010	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U4020	156-0089-00			MICROCIRCUIT,DI:4-BIT UP/DOWN COUNTER	80009	156-0089-00
U4030	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U4040	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U4050	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U4060	156-0996-00			MICROCIRCUIT,DI:3-STATE QUAD BUS XCVR	80009	156-0996-00
U4070	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U4080	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U4090	156-0998-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE BFR	80009	156-0998-00
U4110	156-0844-00			MICROCIRCUIT,DI:SYNC 4-BIT BIN COUNTER	34335	SN74LS161N
U4120	156-0844-00			MICROCIRCUIT,DI:SYNC 4-BIT BIN COUNTER	34335	SN74LS161N
U4130	156-0844-00			MICROCIRCUIT,DI:SYNC 4-BIT BIN COUNTER	34335	SN74LS161N

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A40	670-5378-00			CKT BOARD ASSY:LOWER FRONT PANEL	80009	670-5378-00
C2017	290-0209-00			CAP.,FXD,ELCTLT:50UF,+75-10%,25V	56289	30D688
C2096	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C2139	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
CR1017	150-1001-00			LT EMITTING DIO:RED,660NM,100MA MAX	50522	MV5024
CR1018	150-1001-00			LT EMITTING DIO:RED,660NM,100MA MAX	50522	MV5024
CR1086	150-1001-00			LT EMITTING DIO:RED,660NM,100MA MAX	50522	MV5024
CR1087	150-1001-00			LT EMITTING DIO:RED,660NM,100MA MAX	50522	MV5024
CR1096	150-1001-00			LT EMITTING DIO:RED,660NM,100MA MAX	50522	MV5024
CR1097	150-1001-00			LT EMITTING DIO:RED,660NM,100MA MAX	50522	MV5024
CR1126	150-1001-00			LT EMITTING DIO:RED,660NM,100MA MAX	50522	MV5024
CR1127	150-1001-00			LT EMITTING DIO:RED,660NM,100MA MAX	50522	MV5024
CR1146	150-1001-00			LT EMITTING DIO:RED,660NM,100MA MAX	50522	MV5024
CR1147	150-1001-00			LT EMITTING DIO:RED,660NM,100MA MAX	50522	MV5024
R1023	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
R1093	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
R1123	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
R2039	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
R2079	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
R2099	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
R2149	307-0596-00			RES NTWK,FXD FI:7,2.2K OHM,2%,1.0W	91637	CSP08G01222G
S3012	260-1915-00			SWITCH,TOGGLE:SPDT,0.4VA	09353	7101-J2V3-2
S3081	260-1912-00			SWITCH,TOGGLE:SPDT,0.4VA	09353	7109-J2V3-2
S3141	260-1912-00			SWITCH,TOGGLE:SPDT,0.4VA	09353	7109-J2V3-2
U2070	156-0030-00			MICROCIRCUIT,DI:QUAD 2-INPUT POS NAND GATE	01295	SN7400N
U2080	156-0058-00			MICROCIRCUIT,DI:HEX.INVERTER	80009	156-0058-00
U2120	156-0999-00			MICROCKT,INTFC:HIGH SPEED HEX 3-STATE INV	80009	156-0999-00
U2150	156-1015-00			MICROCIRCUIT,DI:DUAL J-K EDGE TRIG FF	80009	156-1015-00

118-0204-00 POWER SUPPLY ASSEMBLY

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A45	118-0512-00			CKT BOARD ASSY:HCC15-3	80009	118-0512-00
C1	290-0844-00			CAP.,FXD,ELCTLT:100UF,+75-10%,35 WVDC	54473	ECE-A35V100L
C2	290-0871-00			CAP.,FXD,ELCTLT:6800UF,+50-10%,35VDC		
C3	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C4	290-0844-00			CAP.,FXD,ELCTLT:100UF,+75-10%,35 WVDC	54473	ECE-A35V100L
C5	290-0871-00			CAP.,FXD,ELCTLT:6800UF,+50-10%,35 VDC		
C6	283-0003-00			CAP.,FXD,CER DI:0.01UF,+80-20%,150V	72982	855-558Z5U-103Z
C7	290-0844-00			CAP.,FXD,ELCTLT:100UF,+75-10%,35 WVDC	54473	ECE-A35V100L
CR1	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	80009	152-0066-00
CR2	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	04713	1N4721
CR3	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	04713	1N4721
CR4	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	04713	1N4721
CR5	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	04713	1N4721
CR7	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	80009	152-0066-00
CR8	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	04713	1N4721
CR9	152-0198-00			SEMICOND DEVICE:SILICON,200V,3A	04713	1N4721
CR11	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	80009	152-0066-00
CR13	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	80009	152-0066-00
Q1	151-0439-00			TRANSISTOR:SILICON,NPN	80009	151-0439-00
Q2	151-0433-01			TRANSISTOR:SILICON,NPN	04713	SJ962
Q3	151-0301-00			TRANSISTOR:SILICON,PNP	04713	2N2907A
Q4	151-0454-00			TRANSISTOR:SILICON,NPN	80009	151-0454-00
R1	301-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.50W	01121	EB3315
R4	308-0701-00			RES.,FXD,WW:0.12 OHM,5%,2W	75042	BWH-R1200J
R5	301-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.50W	01121	EB2715
R6	301-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.50W	01121	EB3625
R7	301-0362-00			RES.,FXD,CMPSN:3.6K OHM,5%,0.50W	01121	EB3625
R8	307-0051-00			RES.,FXD,CMPSN:2.7 OHM,5%,0.50W	01121	EB27G5
R9	118-0485-00			RES.,VAR,WW:1.5K OHM,20%,1.5W		
R10	323-0181-00			RES.,FXD,FILM:750 OHM,1%,0.50W	75042	CECT0-7500F
R11	323-1217-01			RES.,VAR,WW:1.80K OHM,0.5%,0.5W		
R13	301-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.50W	01121	EB3315
R14	301-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.50W	01121	EB4725
R15	301-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.50W	01121	EB3315
R16	301-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.50W	01121	EB3315
R17	301-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.50W	01121	EB4725
R18	301-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.50W	01121	EB2415
R19	307-0051-00			RES.,FXD,CMPSN:2.7 OHM,5%,0.50W	01121	EB27G5
R20	301-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.50W	01121	EB3315
R21	307-0051-00			RES.,FXD,CMPSN:2.7 OHM,5%,0.50W	01121	EB27G5
R22	118-0485-00			RES.,VAR,WW:1.5K OHM,20%,1.5W		
R23	323-0181-00			RES.,FXD,FILM:750 OHM,1%,0.50W	75042	CECT0-7500F
R24	323-1217-01			RES.,VAR,FILM:1.80K OHM,0.5%,0.5W		
R26	308-0701-00			RES.,FXD,WW:0.12 OHM,5%,2W	75042	BWH-R1200J
R27	301-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.50W	01121	EB1025
R28	301-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.50W	01121	EB1025
R29	301-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.50W	01121	EB3315
R30	301-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.50W	01121	EB1025
R31	301-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.50W	01121	EB1025
T1	118-0449-00			XFMR,PWR,SDN:		

(118-0204-00 CONTINUED)

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
U1	156-0053-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	07263	U5R7723393
U2	156-0053-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	07263	U5R7723393

(118-0204-00 CONTINUED)

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A50	118-0513-00			CKT BOARD ASSY:F5-25	80009	118-0513-00
C1	290-0838-00			CAP.,FXD,ELCTLT:2200UF,+50-10%,35V	56289	OBD
C2	290-0870-00			CAP.,FXD,ELCTLT:5400UF,+100-10%,15VDC		
C3	290-0870-00			CAP.,FXD,ELCTLT:5400UF,+100-10%,15VDC		
C4	283-0065-00			CAP.,FXD,CER DI:0.001UF,5%,100V	72982	805-518-Z5D0102J
C5	290-0869-00			CAP.,FXD,ELCTLT:1000UF,+50-10%,16VDC		
C6	290-0869-00			CAP.,FXD,ELCTLT:1000UF,+50-10%,16VDC		
C7	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	503D106G025AS
CR1	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	80009	152-0066-00
CR2	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	80009	152-0066-00
CR3	152-0729-00			SEMICOND DEVICE:RECT,SI,DUAL,30A,100V		
CR4	152-0729-00			SEMICOND DEVICE:RECT,SI,DUAL,30A,100V		
Q1	151-0454-00			TRANSISTOR:SILICON,NPN	80009	151-0454-00
Q2	151-0433-01			TRANSISTOR:SILICON,NPN	04713	SJ962
Q3	151-0433-01			TRANSISTOR:SILICON,NPN	04713	SJ962
Q4	151-0433-01			TRANSISTOR:SILICON,NPN	04713	SJ962
Q5	151-0433-01			TRANSISTOR:SILICON,NPN	04713	SJ962
R1	307-0055-00			RES.,FXD,CMPSN:3.9 OHM,5%,0.50W	01121	EB39G5
R2	301-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.50W	01121	EB2205
R3	307-0055-00			RES.,FXD,CMPSN:3.9 OHM,5%,0.50W	01121	EB39G5
R4	301-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.50W	01121	EB2205
R5	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
R6	301-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.50W	01121	EB2205
R7	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
R8	301-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.50W	01121	EB2205
R9	118-0485-00			RES.,FXD,WW:1.5K OHM,20%,1.5W		
R10	301-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.50W	01121	EB2225
R11	301-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.50W	01121	EB2225
R12	301-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.50W	01121	EB3325
R13	118-0485-00			RES.,FXD,WW:1.5K OHM,20%,1.5W		
R14	301-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.50W	01121	EB2225
R15	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
R16	307-0060-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.50W	01121	EB68G5
R17	301-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.50W	01121	EB2215
R18	301-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.50W	01121	EB4705
R19	307-0051-00			RES.,FXD,CMPSN:2.7 OHM,5%,0.50W	01121	EB27G5
R20	301-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.50W	01121	EB4705
R21	307-0055-00			RES.,FXD,CMPSN:3.9 OHM,5%,0.50W	01121	EB39G5
R22	307-0055-00			RES.,FXD,CMPSN:3.9 OHM,5%,0.50W	01121	EB39G5
SCR1	151-0533-00			SCR:SILICON		
T1	118-0514-00			XSFMR,PWR,STD:		
U1	156-0053-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	07263	U5R7723393
VR5	152-0175-00			SEMICOND DEVICE:ZENER,0.4W,5.6V,5%	80009	152-0175-00

Ckt No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				CHASSIS		
B1	119-0721-00			FAN,VENTILATING:75 CFM,7W,115VAC,50/60HZ	82877	027119
B2	119-0721-00			FAN,VENTILATING:75 CFM,7W,115VAC,50/60HZ	82877	027119
F1	159-0017-00			FUSE,CARTRIDGE:3AG,4A,250V,FAST BLOW	71400	MTH4
F2	159-0017-00			FUSE,CARTRIDGE:3AG,4A,250V,FAST BLOW	71400	MTH4
F3	159-0126-00			FUSE,CARTRIDGE:3AG,2.5A,250V,0.65 SEC	71400	AGC2-1/2
F4	159-0126-00			FUSE,CARTRIDGE:3AG,2.5A,250V,0.65 SEC	71400	AGC2-1/2
S1	260-1842-00			SWITCH,ROCKER:DPST,16A,250VAC	04009	2600-11E
S2	260-1497-00			SWITCH,PUSH:DPDT,10A,250VAC	01963	E79-30A

Section 13
DIAGRAMS

Symbols and Reference Designators

Graphic symbols for electrical and logic symbols, used on the diagrams, are based on ANSI Y32.2, 1975, and ANSI Y32.14, 1973, "American National Standards Institute." Logic symbols depict the logic function of the device in positive logic. Copies of these standards can be obtained from the Institute of Electrical and Electronics Engineers, 345 East 47th Street, New York, N.Y., 11017. Exceptions and additions are shown on this sample diagram. These conform or are based on the manufacturers data sheet and industry trends.

Resistor values are in ohms, unless noted otherwise, and the Ω symbol is omitted. Capacitor values ≤ 1 (e.g. 10) are in picofarads (pF) and values < 1 (e.g. 0.01) are in microfarads unless otherwise noted.

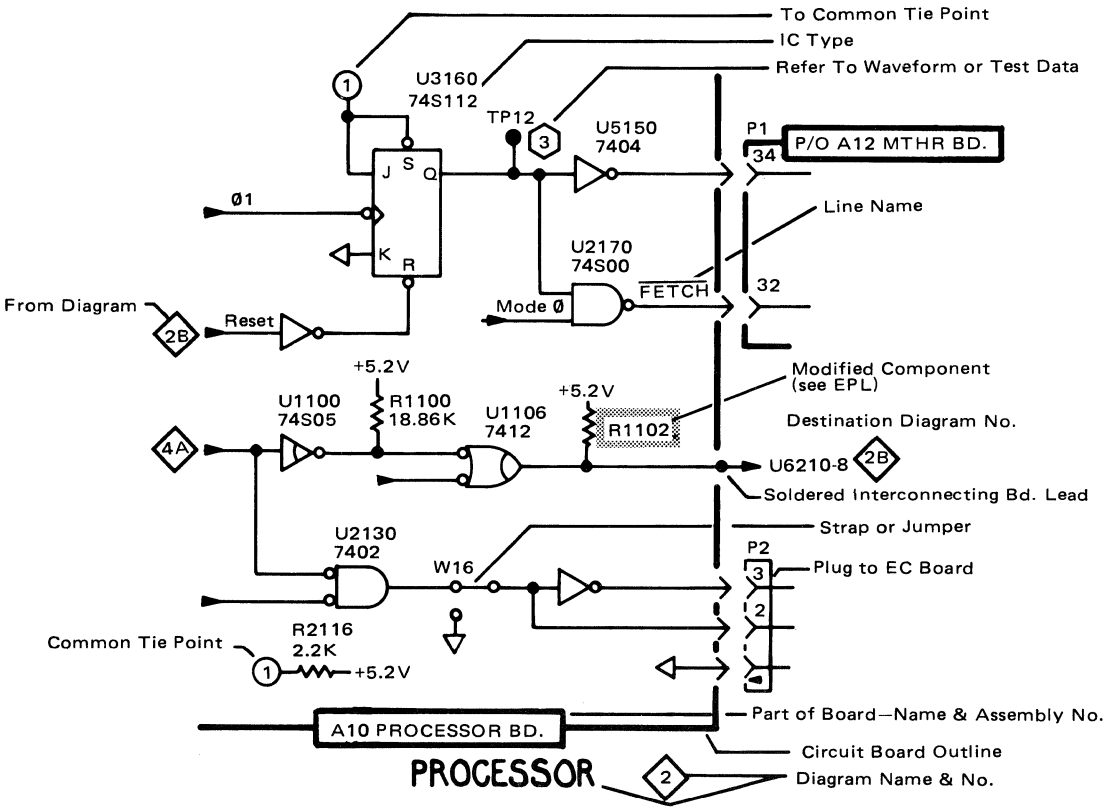
Component Circuit Numbers

Circuit numbers for the components (resistors, IC's, etc.) on the μProcessor Lab modules (boards) are assigned according to their physical location. Some circuit boards have a grid of alphanumeric notation screened or etched on the board. The letters denote row (horizontal) position, the numerals column (vertical) position. Circuit numbers for the schematics or other documentation convert the alpha notation to a number. The letter A converts to 1, B to 2, etc. All component circuit numbers can be found in the Replaceable Electrical Parts List under the assembly number. The schematic assembly number is located in the bottom center of the schematic.

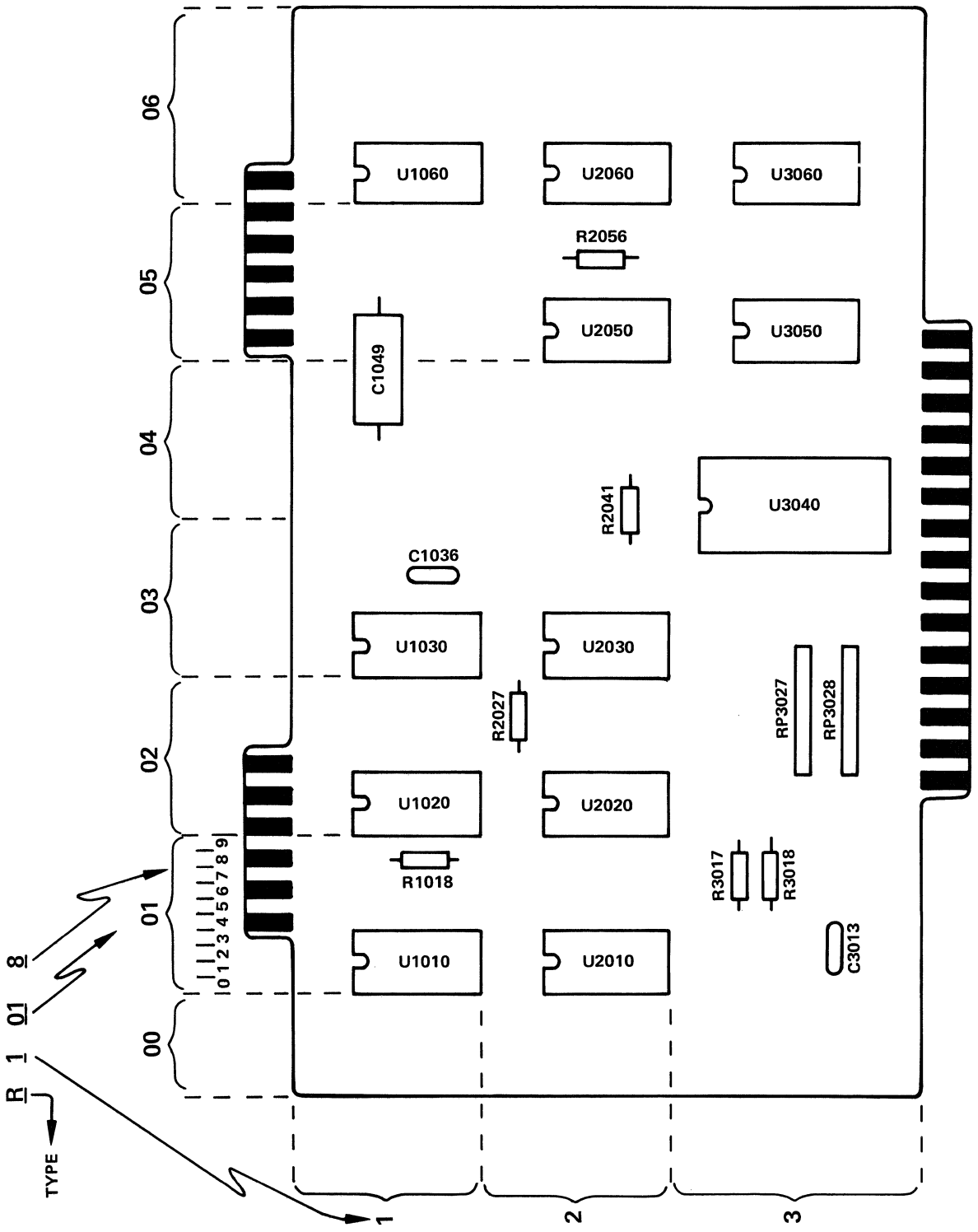
The following prefix letters are used as reference designators to identify components or assembles on the diagrams.

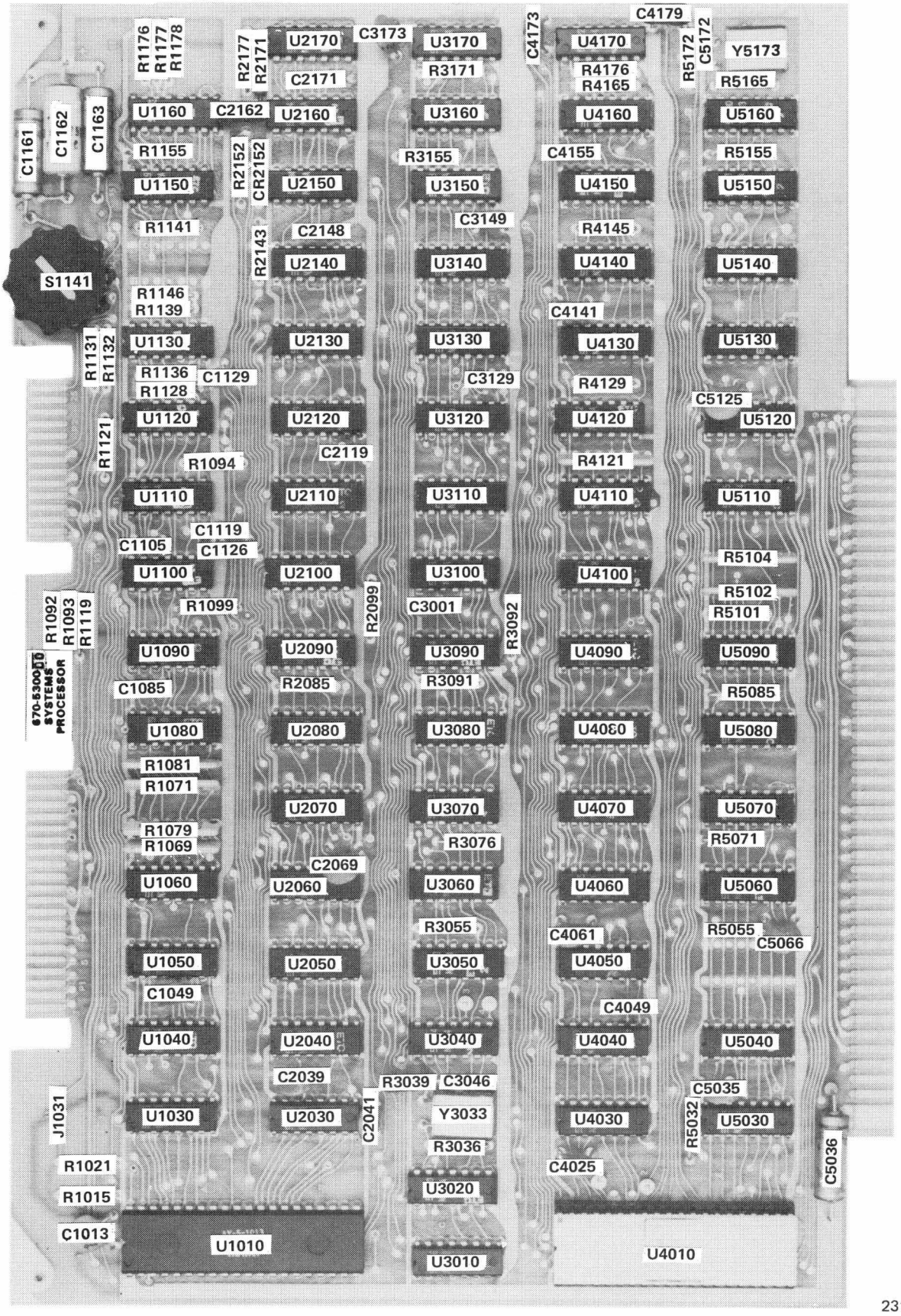
A	Assembly, separable or repairable circuit board, etc)	HY	Hybrid circuit	T	Transformer
C	Capacitor, fixed or variable	J	Connector, stationary portion	TC	Thermocouple
CR	Diode, signal or rectifier	K	Relay	TP	Test Point
DL	Delay line	L	Inductor, fixed or variable	U	Integrated circuit
DS	Indicating device (lamp)	P	Connector, movable portion	V	Electron tube
E	Spark Gap, Ferrite bead	Q	Transistor or silicon-controlled rectifier	VR	Voltage regulator (zener diode, etc.)
F	Fuse	R	Resistor, fixed or variable	W	Wirestrap or cable
FL	Filter	RT	Thermistor	Y	Crystal
H	Heat dissipating device (heat sink, heat radiator, etc.)	S	Switch or contactor	Z	Phase shifter

The following partial diagram illustrates special symbology and practices used on the diagrams with a description of the meaning.



CIRCUIT NUMBER ASSIGNMENT GUIDE



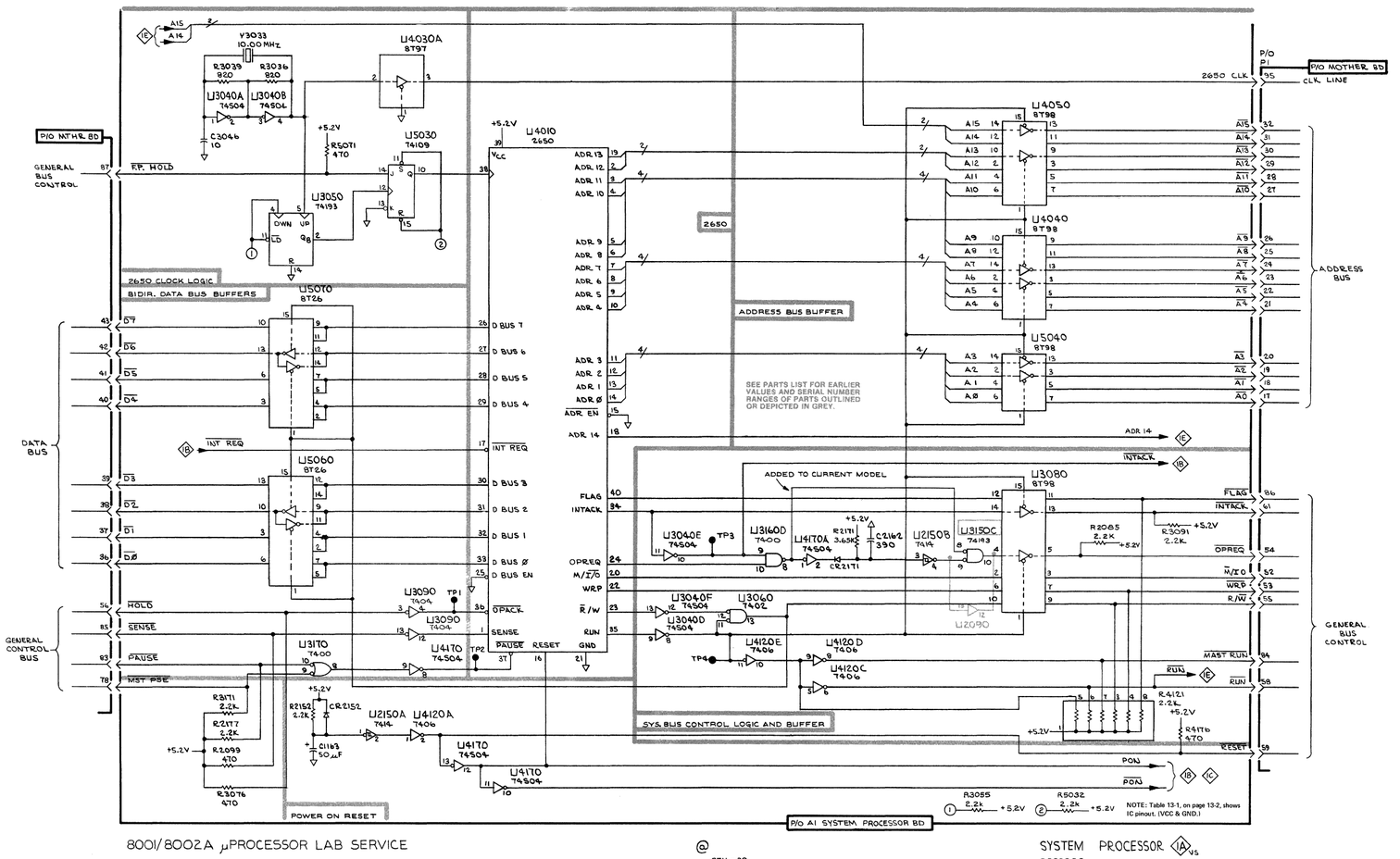


2312-9

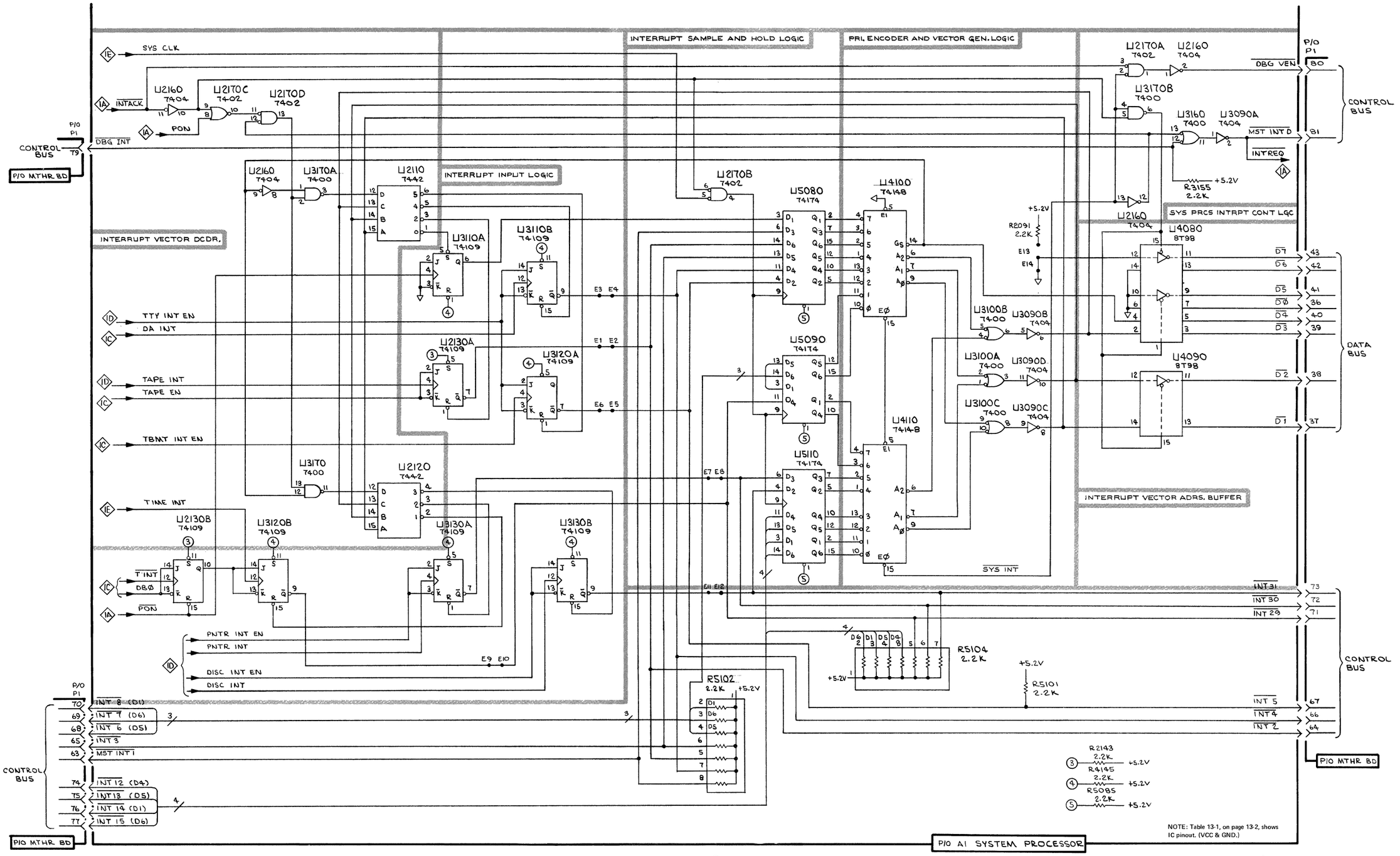
A-1 System Processor Module

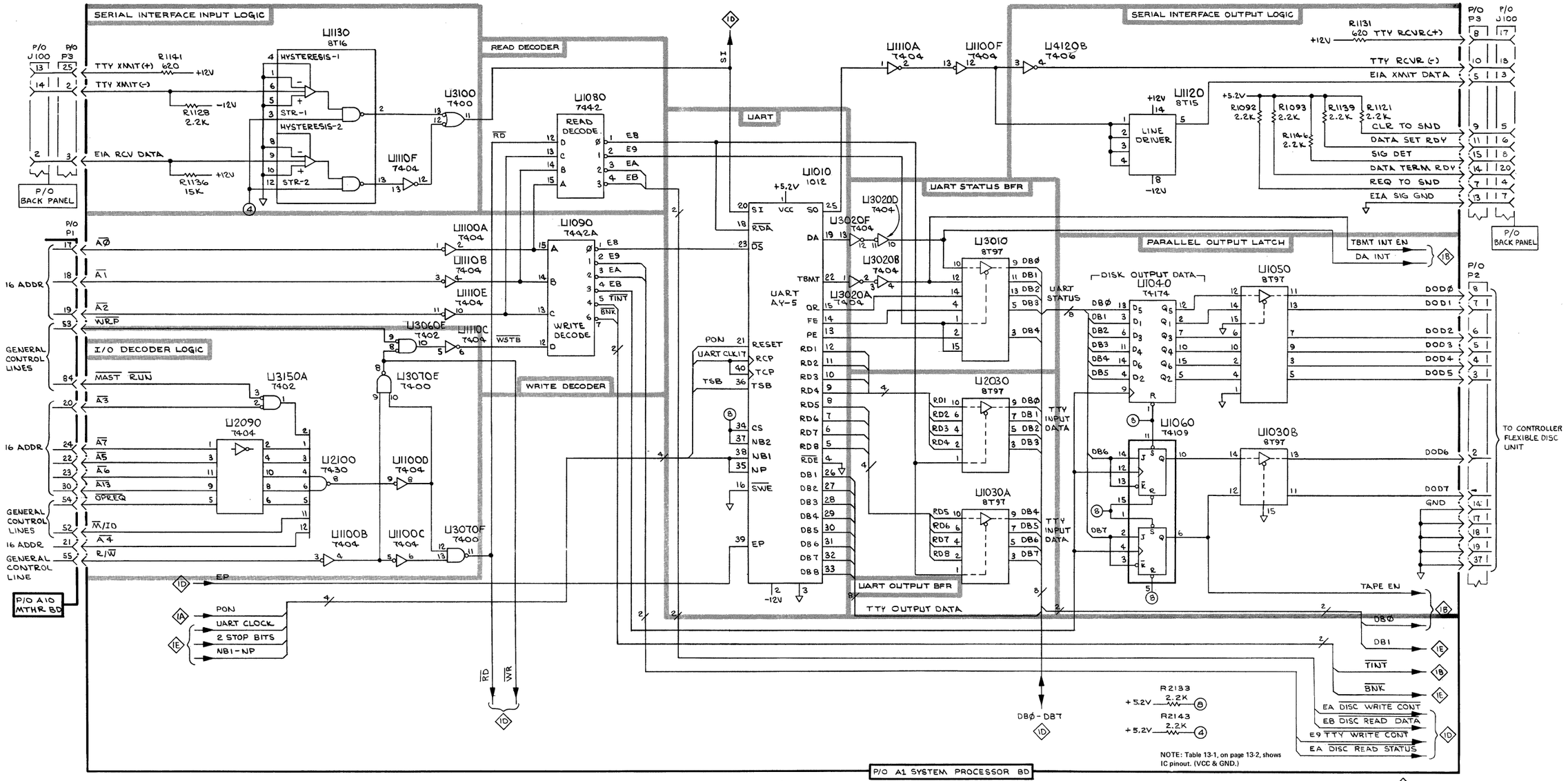
Table 13-1
VCC/GND Pinout of IC Type For 8002 Microprocessor

Type	VCC	GND
1012	7	14
1702A	12	14
2602	10	9
2650	39	21
2680	11	22
3242	28	14
3245	11	8
4027P-2	9	16
4808A	18	9
6850	12	1
7400 (S) (LS)	14	7
7402 (S) (LS)	14	7
7404 (S) (LS)	14	7
7406	14	7
74S08	14	7
74S10 (LS)	14	7
7414 (LS)	14	7
7420 (S) (LS)	14	7
7430 (LS)	14	7
7442/7442A	16	8
74LS86	14	7
74109 (LS)	16	8
74S112 (LS)	16	8
74LS133	16	8
74LS136	14	7
74S139 (LS)	16	8
74148	16	8
74157 (LS)	16	8
74LS161	16	8
74174 (LS)	16	8
74S175 (LS)	16	8
74193 (LS)	16	8
74LS260	14	7
74LS279	16	8
74S280	14	7
74393	14	7
74LS670	16	8
8T15	14	7
8T16	14	7
8T26	16	8
8T97	16	8
8T98	16	8
82S62	14	7
82S115	24	12
82S116	16	8
82S2708	24	12
9602	16	8
IM5200	24	12



8001/8002A μPROCESSOR LAB SERVICE @ 2711-39 SYSTEM PROCESSOR 1A 8032000


INTERRUPT SAMPLE AND HOLD LOGIC
PRI. ENCODER AND VECTOR GEN. LOGIC
INTERRUPT INPUT LOGIC
INTERRUPT VECTOR DCDR.
SYS PRCS INTRPT CONT LGC
INTERRUPT VECTOR ADRS. BUFFER
SYS CLK
INTACK
PON
DBG INT
TTY INT EN
DA INT
TAPE INT
TAPE EN
TBMT INT EN
TIME INT
PNTR INT EN
PNTR INT
DISC INT EN
DISC INT
T INT
DBΦ
DBG VEN
MST INT D
INTREQ
SYS INT
+5.2V
R3155 2.2K
R2091 2.2K
R5104 2.2K
R5101 2.2K
R5102 2.2K
R2143 2.2K
R4145 2.2K
R5085 2.2K
CONTROL BUS
DATA BUS
P/O P1
P/O MTHR BD
P/O A1 SYSTEM PROCESSOR
INT 8 (D1)
INT 7 (D6)
INT 6 (D5)
INT 3
MST INT 1
INT 12 (D4)
INT 13 (D5)
INT 14 (D1)
INT 15 (D6)
INT 31
INT 30
INT 29
INT 5
INT 4
INT 2
NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)



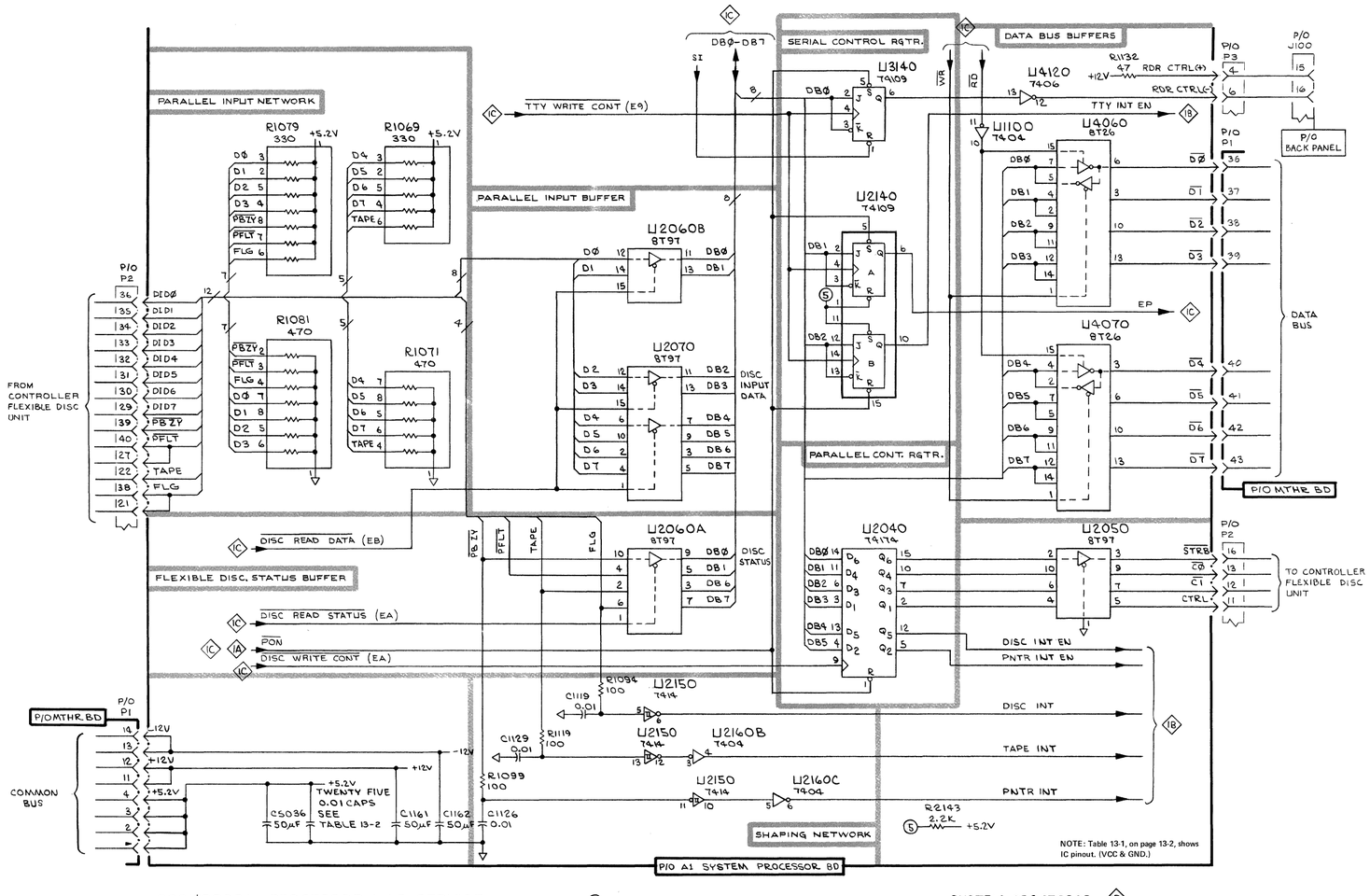
8001/8002A μPROCESSOR LAB SERVICE

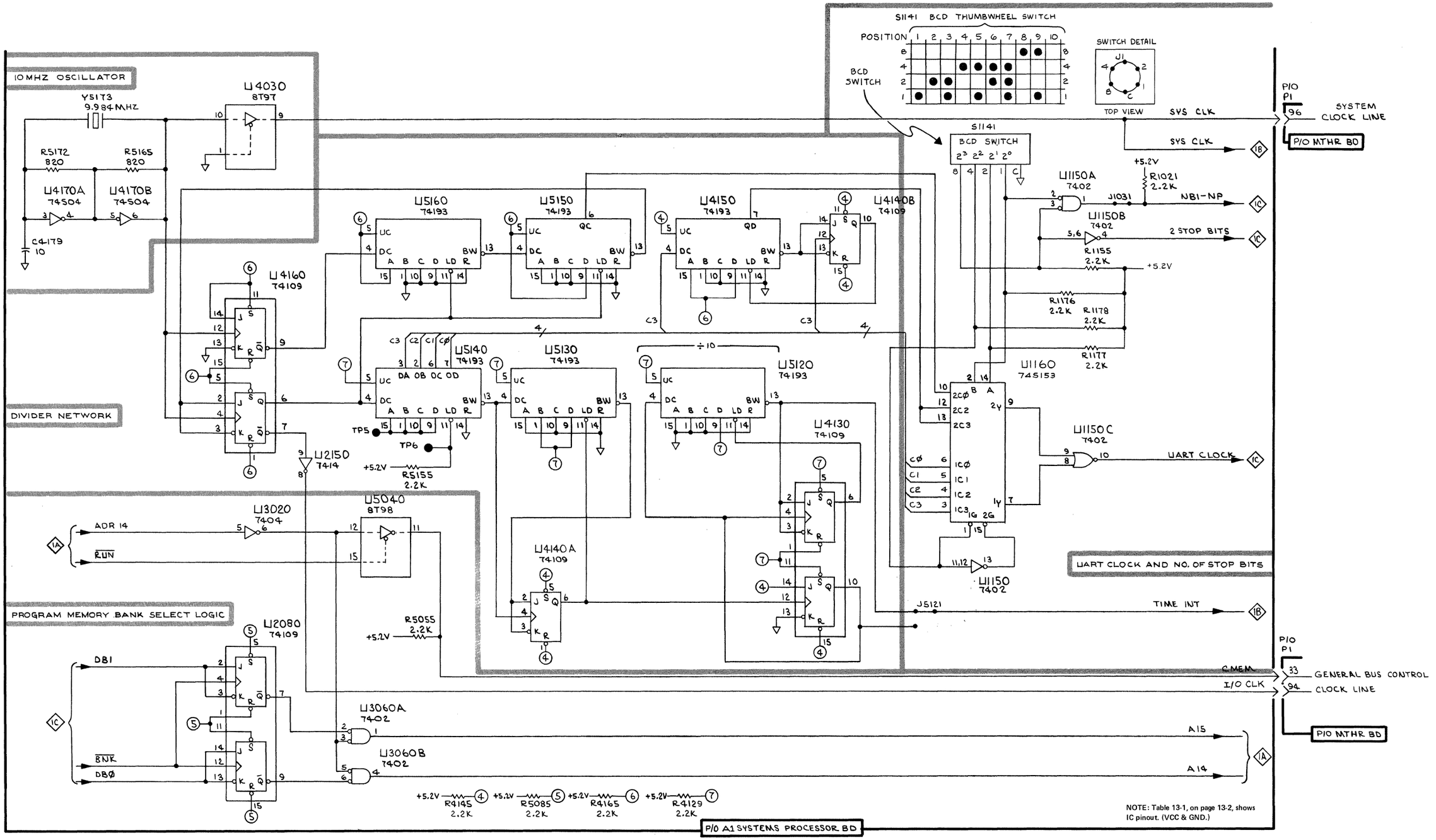
SYSTEM PROCESSOR IC VS

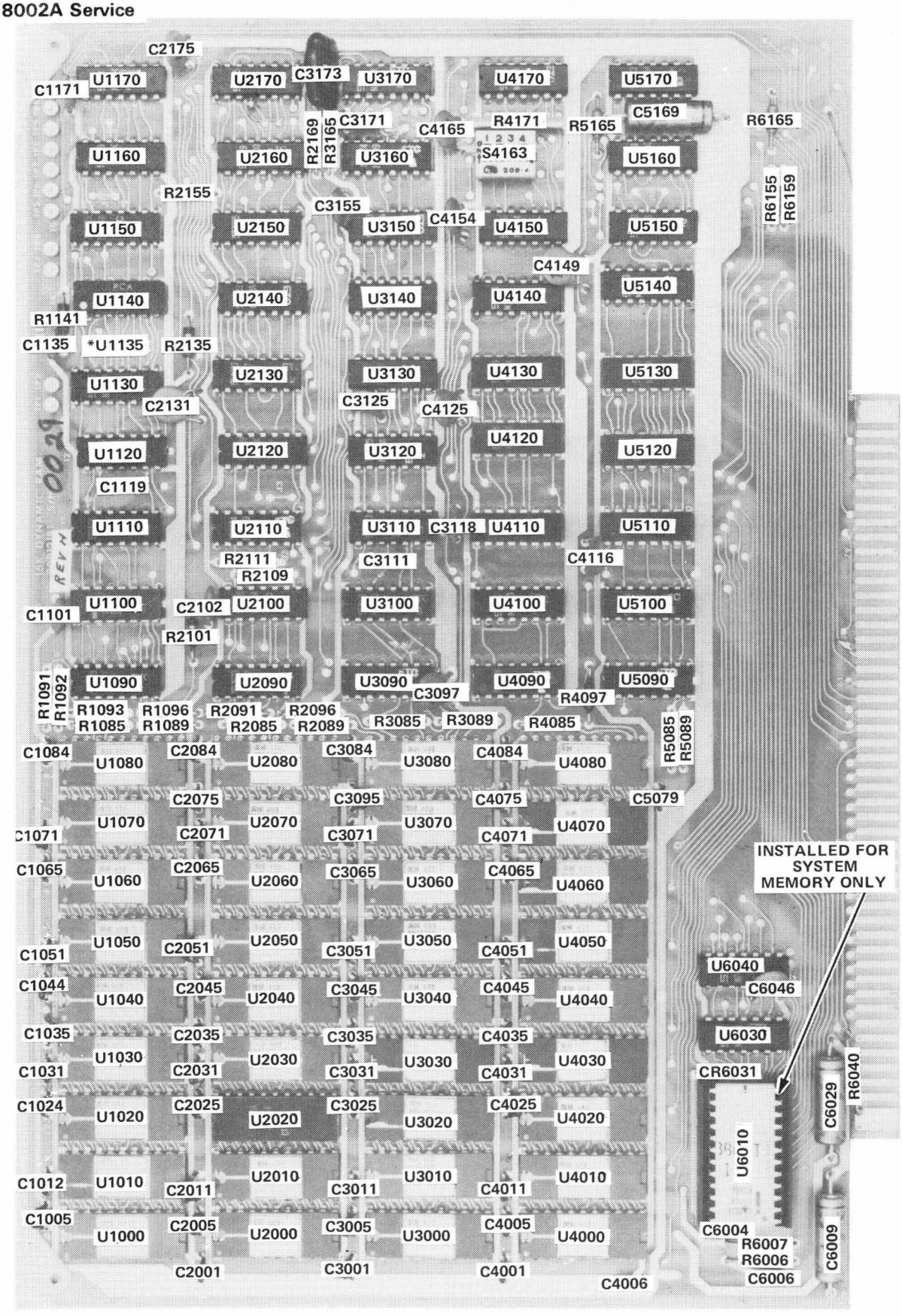
B032000

Table 13-2

C1013	C3129
C1049	C3149
C1085	C3173
C1105	C4025
C1119	C4049
C1129	C4061
C2039	C4141
C2041	C4155
C2069	C4173
C2119	C5035
C2148	C5066
C3101	C5125
	C5172




10MHZ OSCILLATOR
Y5173 9.984MHZ
U4030 8T97
R5172 820
R5165 820
U4170A 74S04
U4170B 74S04
C4179 10
DIVIDER NETWORK
U4160 74109
U5160 74193
U5150 74193
U4150 74193
U4140B 74109
U5140 74193
U5130 74193
U5120 74193
÷10
U4130 74109
U4140A 74109
U2150 74H4
TP5
TP6
+5.2V
R5155 2.2K
U5040 8T98
U3020 7404
ADR 14
RUN
PROGRAM MEMORY BANK SELECT LOGIC
U2080 74109
DBI
BNK
DBØ
U3060A 7402
U3060B 7402
R5055 2.2K
R4145 2.2K
R5085 2.2K
R4165 2.2K
R4129 2.2K
S1141 BCD THUMBWHEEL SWITCH
POSITION 1 2 3 4 5 6 7 8 9 10
BCD SWITCH
SWITCH DETAIL
TOP VIEW
S1141 BCD SWITCH
SYS CLK
P/O P1 96
SYSTEM CLOCK LINE
P/O MTHR BD
U1150A 7402
R1021 2.2K
NBI-NP
U1150B 7402
2 STOP BITS
R1155 2.2K
R1176 2.2K
R1178 2.2K
R1177 2.2K
U1160 74S153
U1150C 7402
UART CLOCK
UART CLOCK AND NO. OF STOP BITS
U1150 7402
J5121
TIME INT
C MEM
I/O CLK
P/O P1 33 GENERAL BUS CONTROL
94 CLOCK LINE
P/O MTHR BD
A15
A14
NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)
P/O A1 SYSTEMS PROCESSOR BD



*See parts list

A-20 16K Dynamic RAM Module

2312-10A

Table 13-3

C1001
C1024
C1044
C1065
C1084
C2005
C2025
C2045
C2065
C2085
C3005
C3025
C3045
C3065
C2084
C4005
C4025
C4045
C4065
C4075

Table 13-4

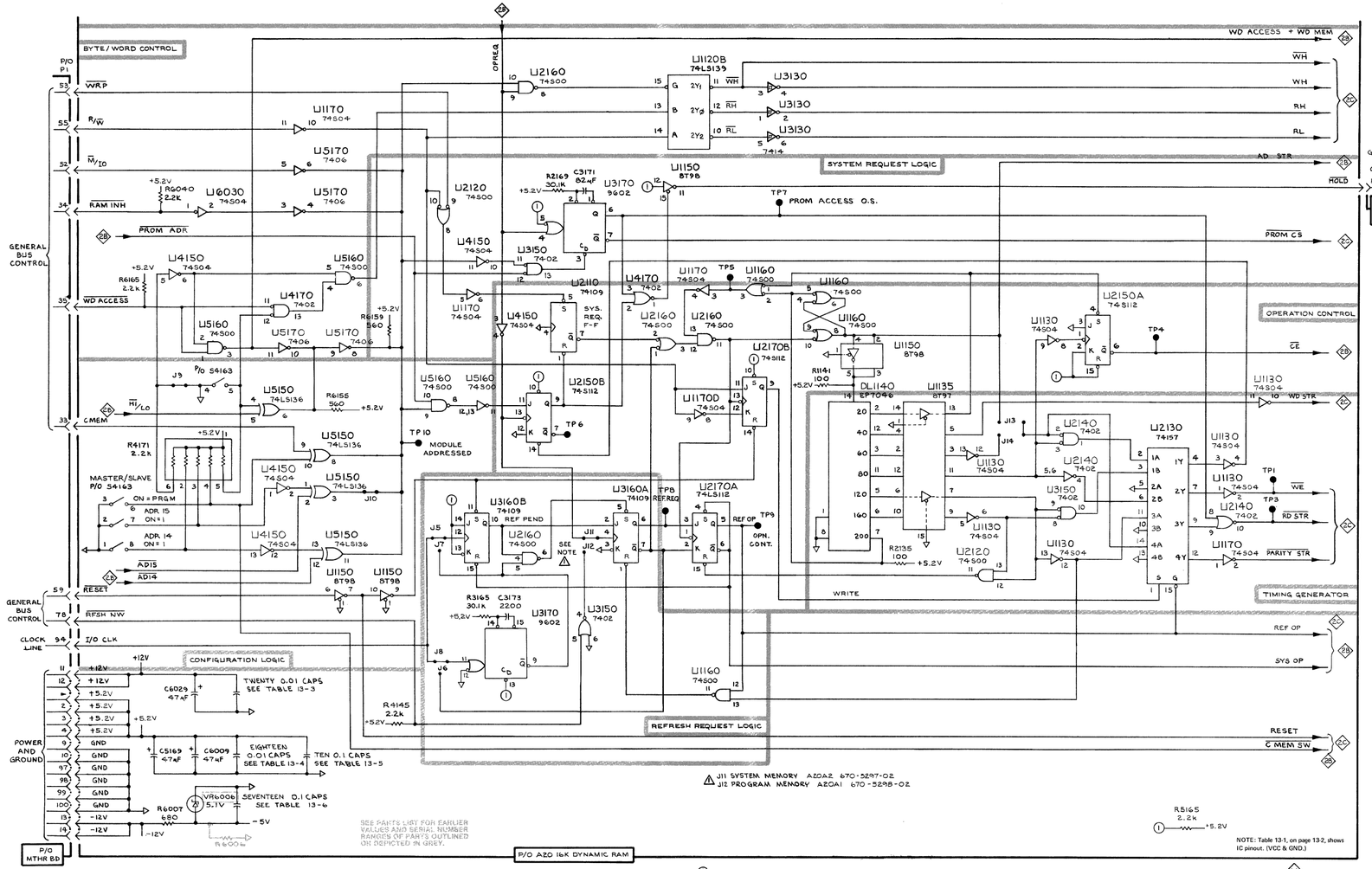
C1101
C1135
C1171
C1119
C2102
C2131
C2175
C3111
C3125
C3155
C3097
C3118
C4125
C4154
C4165
C4116
C4149
C6049

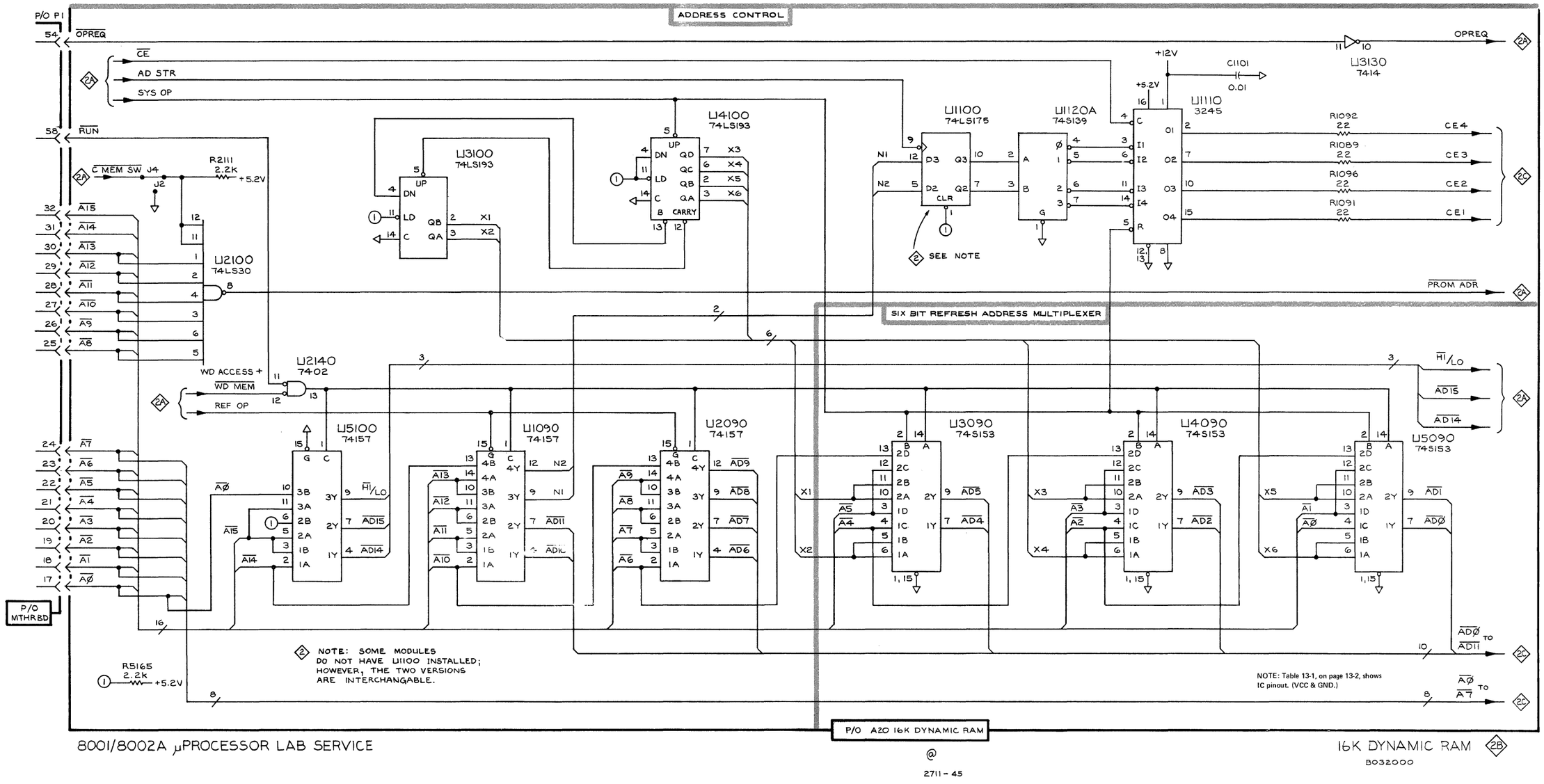
Table 13-5

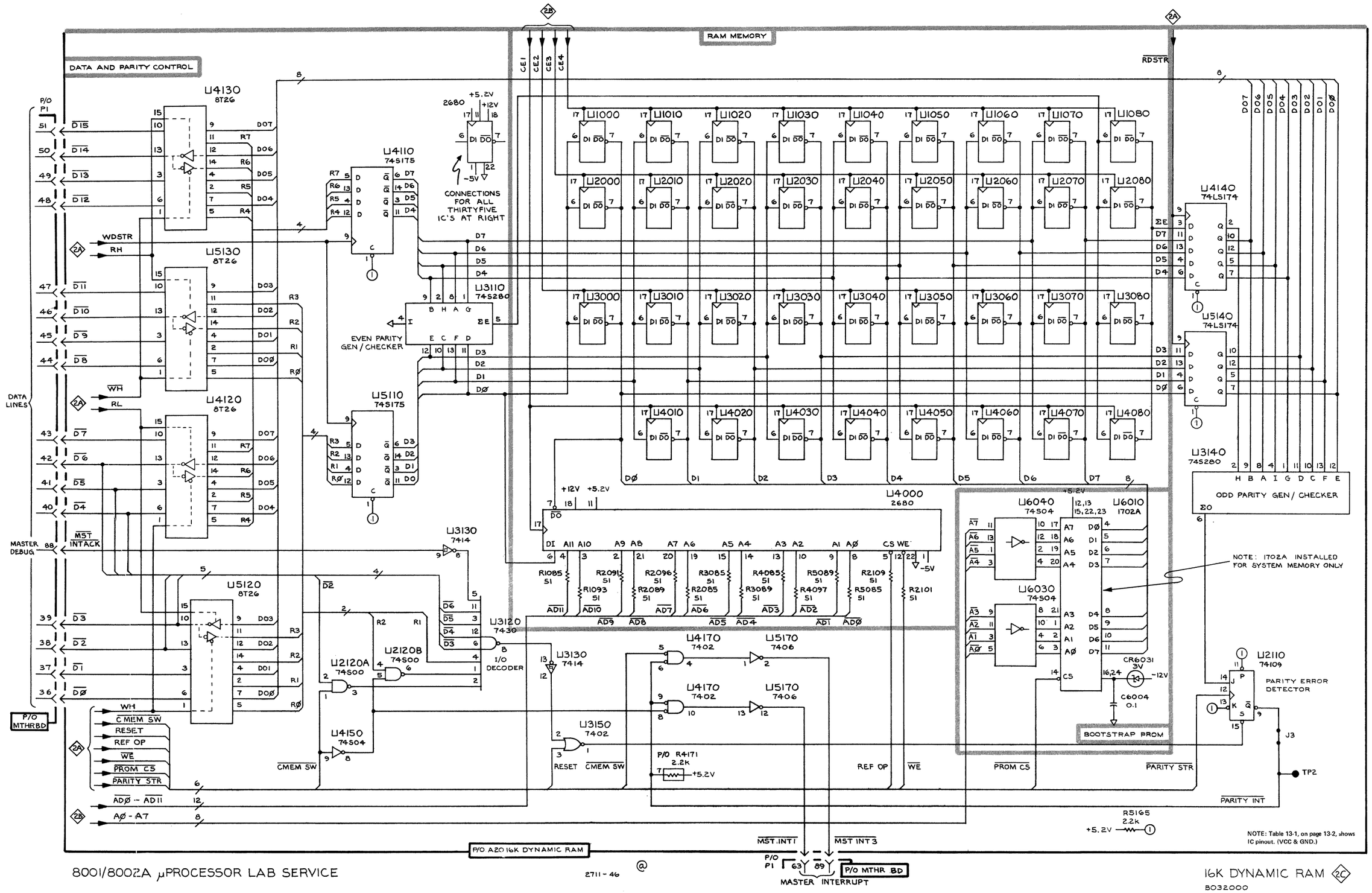
C1035
C2001
C2035
C2075
C3001
C3035
C3095
C4001
C4035
C4075

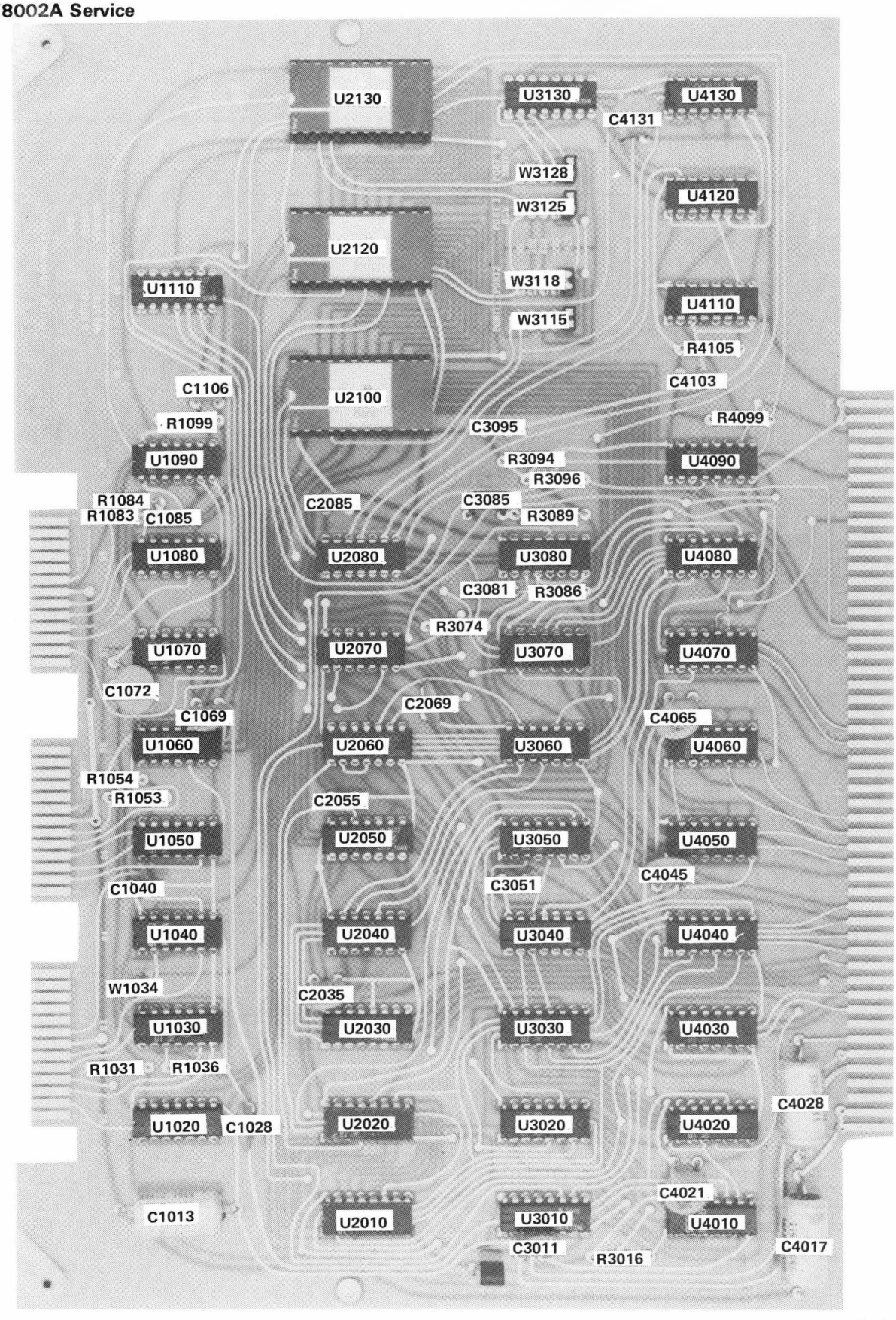
Table 13-6

C1012
C1031
C1051
C1071
C2011
C2031
C2051
C2071
C3011
C3031
C3051
C3071
C4011
C4031
C4051
C4071
C6006




P/O P1
ADDRESS CONTROL
54 OPREQ
CE
AD STR
SYS OP
58 RUN
C MEM SW J4
J2
R2111 2.2K +5.2V
U2100 74LS30
U3100 74LS193
U4100 74LS193
U1100 74-LS175
U1120A 74S139
+12V
+5.2V
C1101 0.01
U1110 3245
U3130 7414
OPREQ
R1092 2.2 CE4
R1089 2.2 CE3
R1096 22 CE2
R1091 22 CE1
SEE NOTE
PROM ADR
SIX BIT REFRESH ADDRESS MULTIPLEXER
WD ACCESS +
WD MEM
REF OP
U2140 7402
U5100 74157
U1090 74157
U2090 74157
U3090 74S153
U4090 74S153
U5090 74S153
HI/LO
AD15
AD14
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
P/O MTHRBD
R5165 2.2K +5.2V
NOTE: SOME MODULES DO NOT HAVE U1100 INSTALLED; HOWEVER, THE TWO VERSIONS ARE INTERCHANGABLE.
NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)
AD0 TO AD11
A0 TO A7
P/O A20 16K DYNAMIC RAM


DATA AND PARITY CONTROL
RAM MEMORY
U4130 8T26
U5130 8T26
U4120 8T26
U5120 8T26
U4110 74S175
U5110 74S175
U3110 74S280
EVEN PARITY GEN/CHECKER
U3130 7414
U3120 7430
I/O DECODER
U2120A 74S00
U2120B 74S00
U4150 74S04
U4170 7402
U5170 7406
U3150 7402
U4000 2680
+5.2V +12V
CONNECTIONS FOR ALL THIRTYFIVE IC'S AT RIGHT
U1000 U1010 U1020 U1030 U1040 U1050 U1060 U1070 U1080
U2000 U2010 U2020 U2030 U2040 U2050 U2060 U2070 U2080
U3000 U3010 U3020 U3030 U3040 U3050 U3060 U3070 U3080
U4010 U4020 U4030 U4040 U4050 U4060 U4070 U4080
U4140 74LS174
U5140 74LS174
U3140 74S280
ODD PARITY GEN/CHECKER
U6040 74S04
U6010 1702A
U6030 74S04
NOTE: 1702A INSTALLED FOR SYSTEM MEMORY ONLY
CR6031 3V
C6004 0.1
BOOTSTRAP PROM
U2110 74109
PARITY ERROR DETECTOR
J3
TP2
R5165 2.2k
P/O R4171 2.2K
DATA LINES
MASTER DEBUG
P/O MTHRBD
WDSTR
RH
WH
RL
MST INTACK
C MEM SW
RESET
REF OP
WE
PROM CS
PARITY STR
PARITY INT
RDSTR
ADØ -- AD11
AØ - A7
CMEM SW
MST INT1
MST INT3
MASTER INTERRUPT
P/O A20 16K DYNAMIC RAM
P/O MTHR BD
NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)



A-30 System Communications Module

2312-11

@

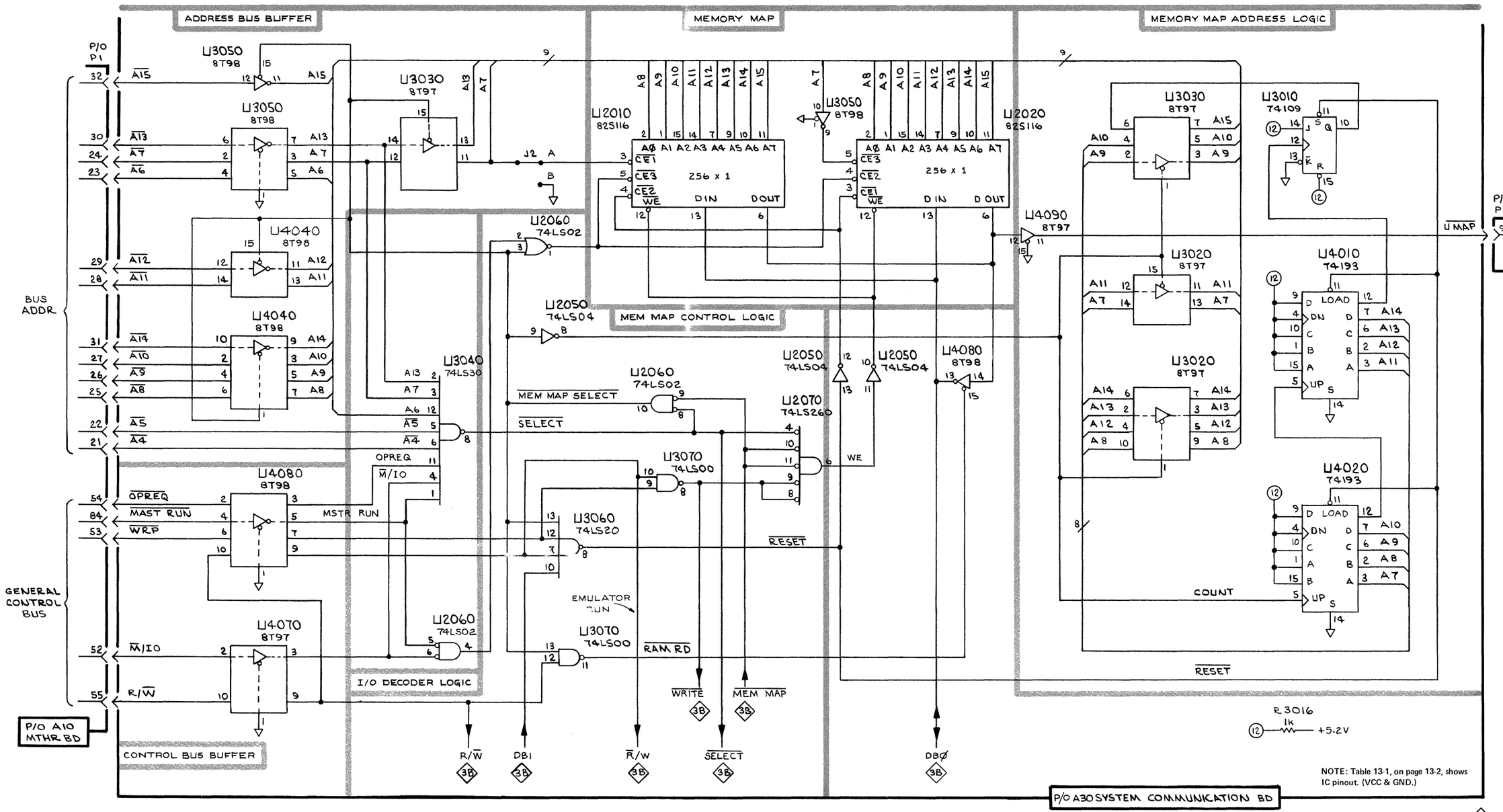
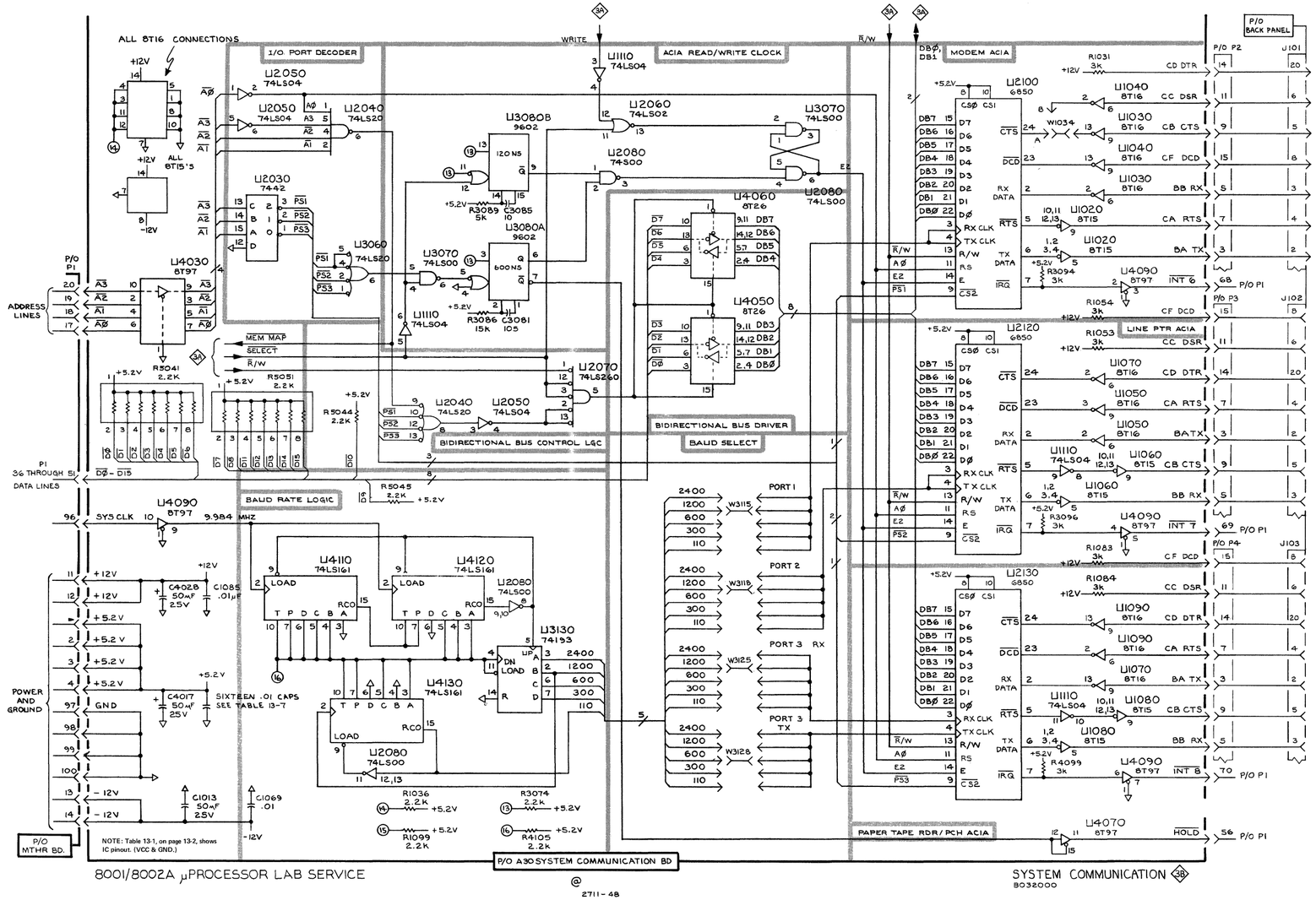
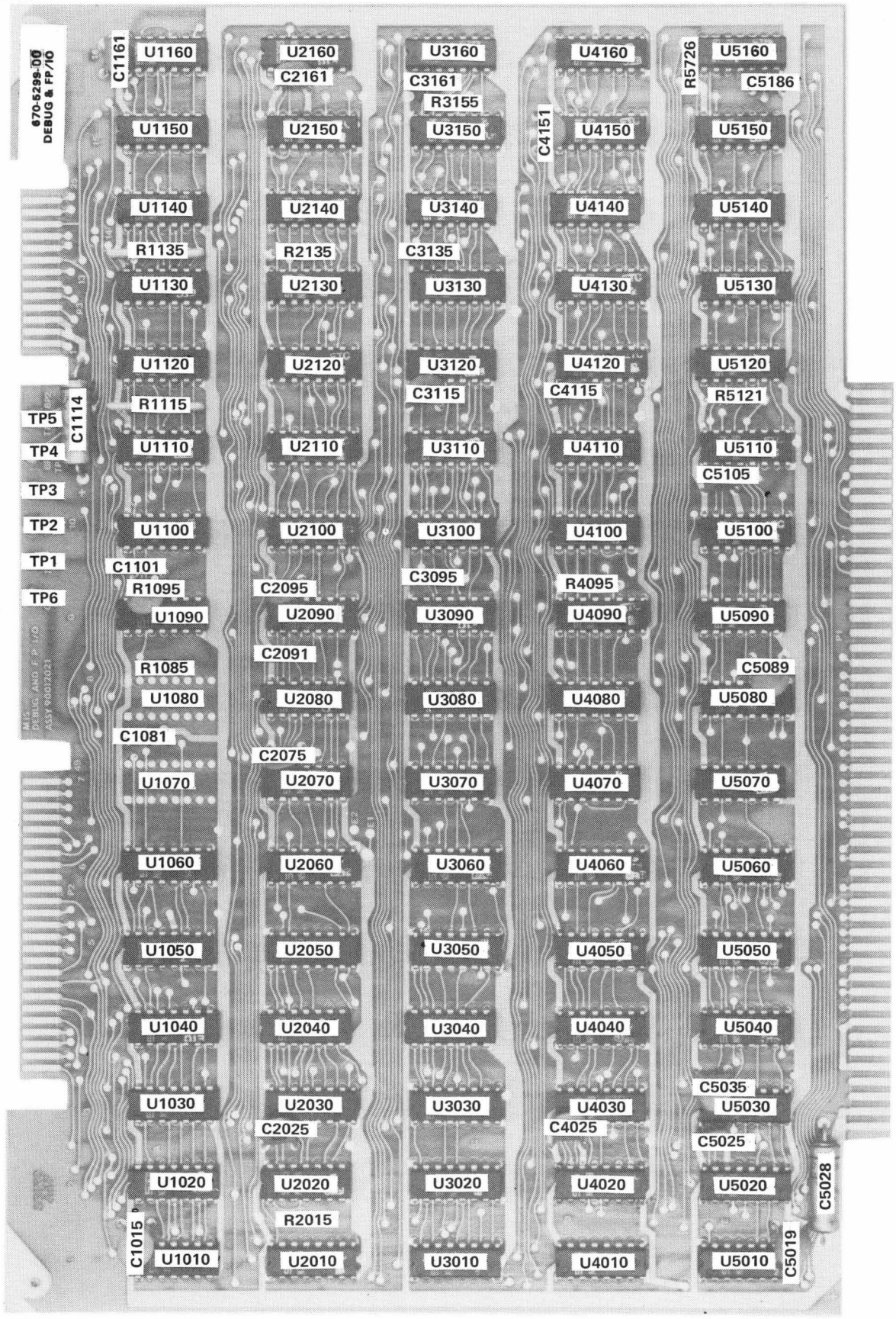

ADDRESS BUS BUFFER
MEMORY MAP
MEMORY MAP ADDRESS LOGIC
MEM MAP CONTROL LOGIC
I/O DECODER LOGIC
CONTROL BUS BUFFER
BUS ADDR
GENERAL CONTROL BUS
P/O P1
P/O A10 MTHR BD
U3050 8T98
U3030 8T97
U4040 8T98
U4080 8T98
U4070 8T97
U2010 82S116
U2020 82S116
U2060 74LS02
U2050 74LS04
U3040 74LS30
U2070 74LS260
U3070 74LS00
U3060 74LS20
U4090 8T97
U3020 8T97
U3010 74109
U4010 74193
U4020 74193
256 x 1
D IN
D OUT
LOAD
UP
MEM MAP SELECT
SELECT
OPREQ
M/IO
MAST RUN
WRP
MSTR RUN
RESET
EMULATOR RUN
RAM RD
WE
WRITE
MEM MAP
R/W
DBI
DB0
UMAP
COUNT
R3016
1k
+5.2V
P/O A10 MTHR BD
P/O A30 SYSTEM COMMUNICATION BD
NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)

Table 13-7

C1028
C1045
C1072
C1106
C2035
C2055
C2069
C2085
C3011
C3051
C3095
C4021
C4045
C4065
C4103
C4131





A-5 Debug and Front Panel I/O Module

2312-12

COMPONENT LOCATION FOR
DEBUG AND FRONT PANEL I/O

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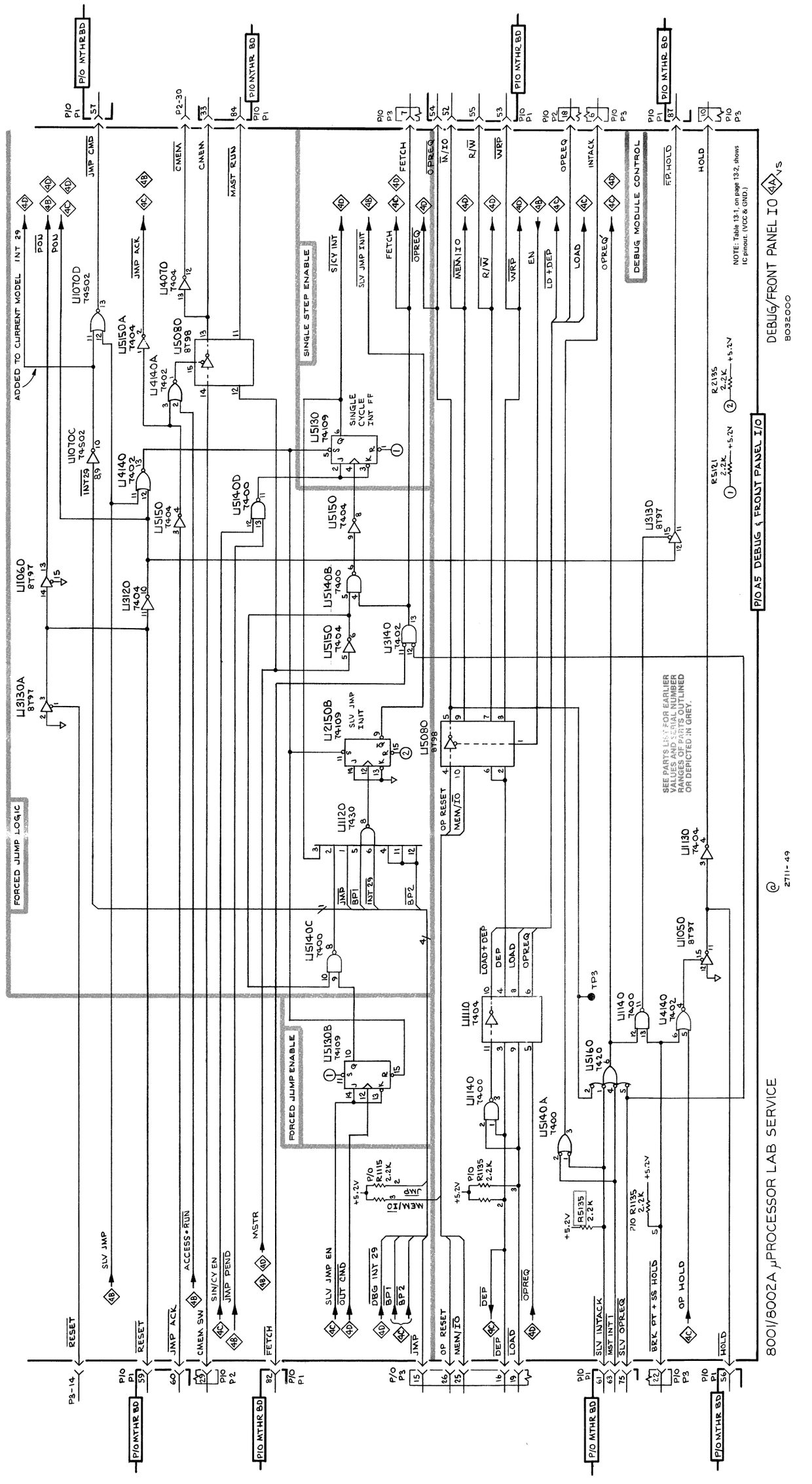
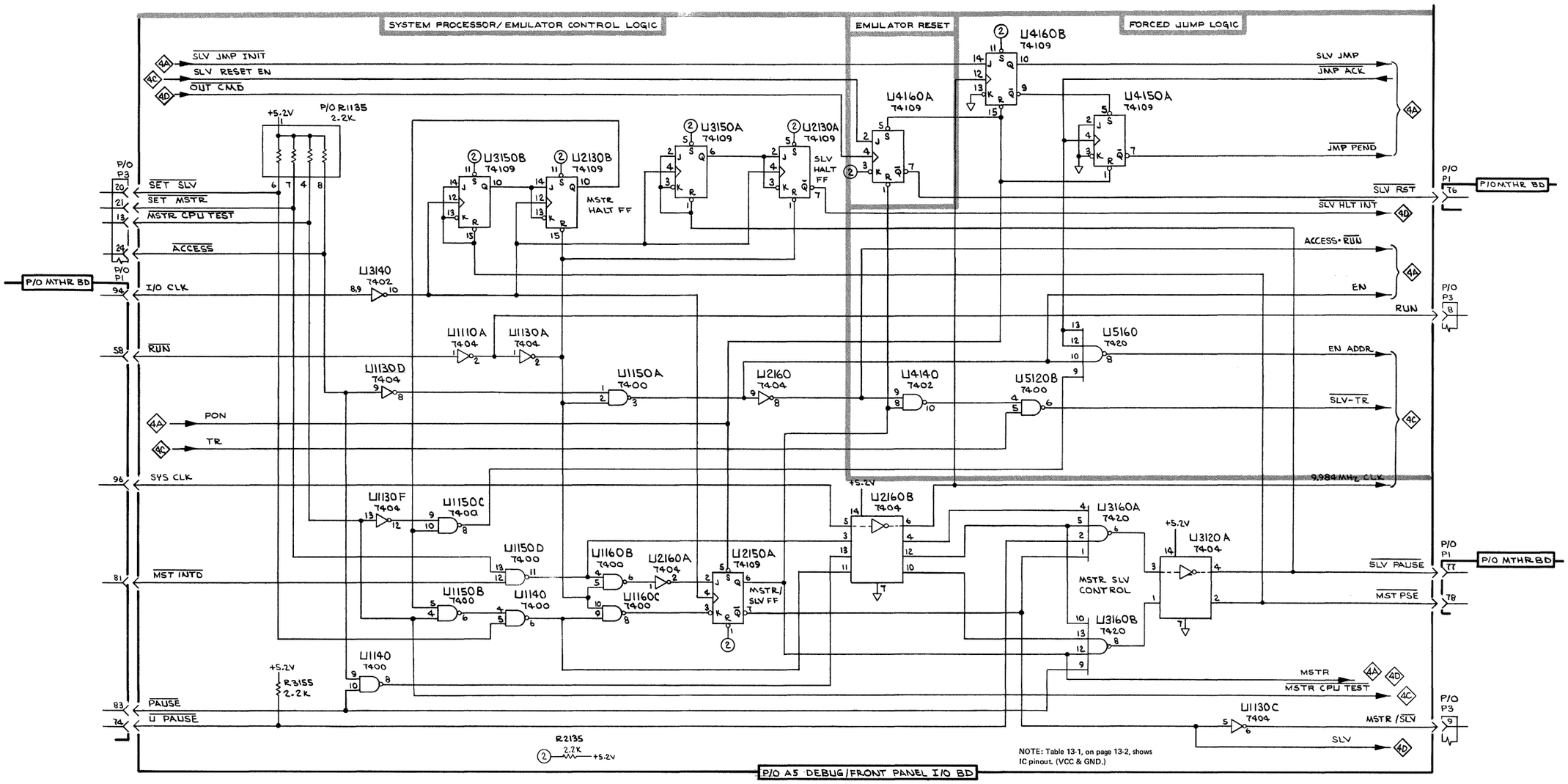

DEBUG/FRONT PANEL IO
8032000
4A-5
P10A5 DEBUG & FRONT PANEL I/O
ADDED TO CURRENT MODEL INT 29
FORCED JUMP LOGIC
SINGLE STEP ENABLE
FORCED JUMP ENABLE
DEBUG MODULE CONTROL
NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)
SEE PARTS LIST FOR EARLIER VALUES AND PART NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
8001/8002A μPROCESSOR LAB SERVICE
2711-49


SYSTEM PROCESSOR/EMULATOR CONTROL LOGIC
EMULATOR RESET
FORCED JUMP LOGIC
SLV JMP INIT
SLV RESET EN
OUT CMD
+5.2V
P/O R1135 2.2K
6 7 4 8
P/O P3
20 SET SLV
21 SET MSTR
13 MSTR CPU TEST
24 ACCESS
P/O P1
94 I/O CLK
58 RUN
4A PON
4C TR
96 SYS CLK
81 MST INTD
83 PAUSE
74 U PAUSE
P/O MTHR BD
U3140 7402
U1110A 7404
U1130A 7404
U1130D 7404
U1150A 7400
U2160 7404
U4140 7402
U5120B 7400
U5160 7420
U4160B 74109
U4160A 74109
U4150A 74109
U3150B 74109
U2130B 74109
U3150A 74109
U2130A 74109
MSTR HALT FF
SLV HALT FF
SLV JMP
JMP ACK
JMP PEND
SLV RST
SLV HLT INT
ACCESS • RUN
EN
RUN
EN ADDR
SLV-TR
9.984 MHz CLK
U1130F 7404
U1150C 7400
U1150D 7400
U1150B 7400
U1140 7400
U1160B 7400
U1160C 7400
U2160A 7404
U2150A 74109
MSTR/SLV FF
U2160B 7404
U3160A 7420
U3120A 7404
U3160B 7420
MSTR SLV CONTROL
SLV PAUSE
MST PSE
MSTR
MSTR CPU TEST
MSTR/SLV
SLV
U1130C 7404
R3155 2.2K
R2135 2.2K
P/O A5 DEBUG/FRONT PANEL I/O BD
NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)

TRACE ENABLE

DEBUG CONTROL LOGIC

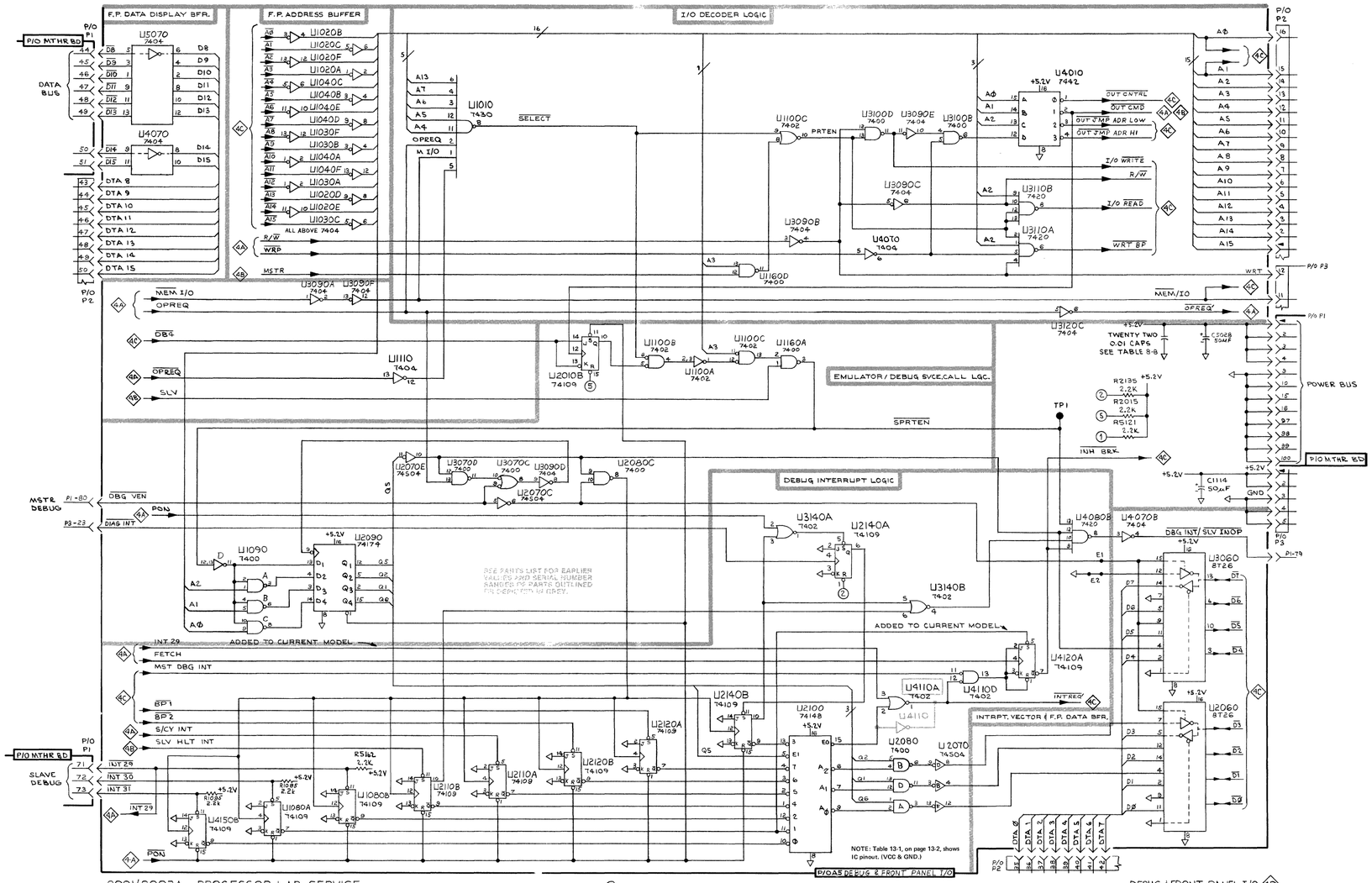
OUT JMP ADR HI
OUT JMP ADR LO
SLV TR
OPREQ'
INT REQ'
FETCH
LOAD
MSTR CPU TEST
MEM/IO
9.984 MHz CLK
PON
OUT CMD
R/W
OUT CNTRL
OP HOLD
LD SEL
P2-17
T SEQ SYNC
COMPARE
TP2
TP4
TP5
TP6
BP1
BP2
SIN/CY EN
TR
MSK DBG INT
(SLV) INT Ø
SLV JUMP EN
SLV RST EN
DB-4
EN ADDR
P/O P1
P/O MTHR BD
P/O P2
P/O P3
DATA BUS
ADDR BUS
ADD REG
ADD COMP
SEQUENCER
DEP
I/O READ
I/O WRITE
LD+DEP
WRT BP
INH BRK
JMP ACK
DEC
INC
A1
AØ
RS121 2.2K +5.2V
R2015 2.2K +5.2V
R1115 2.2K +5.2V

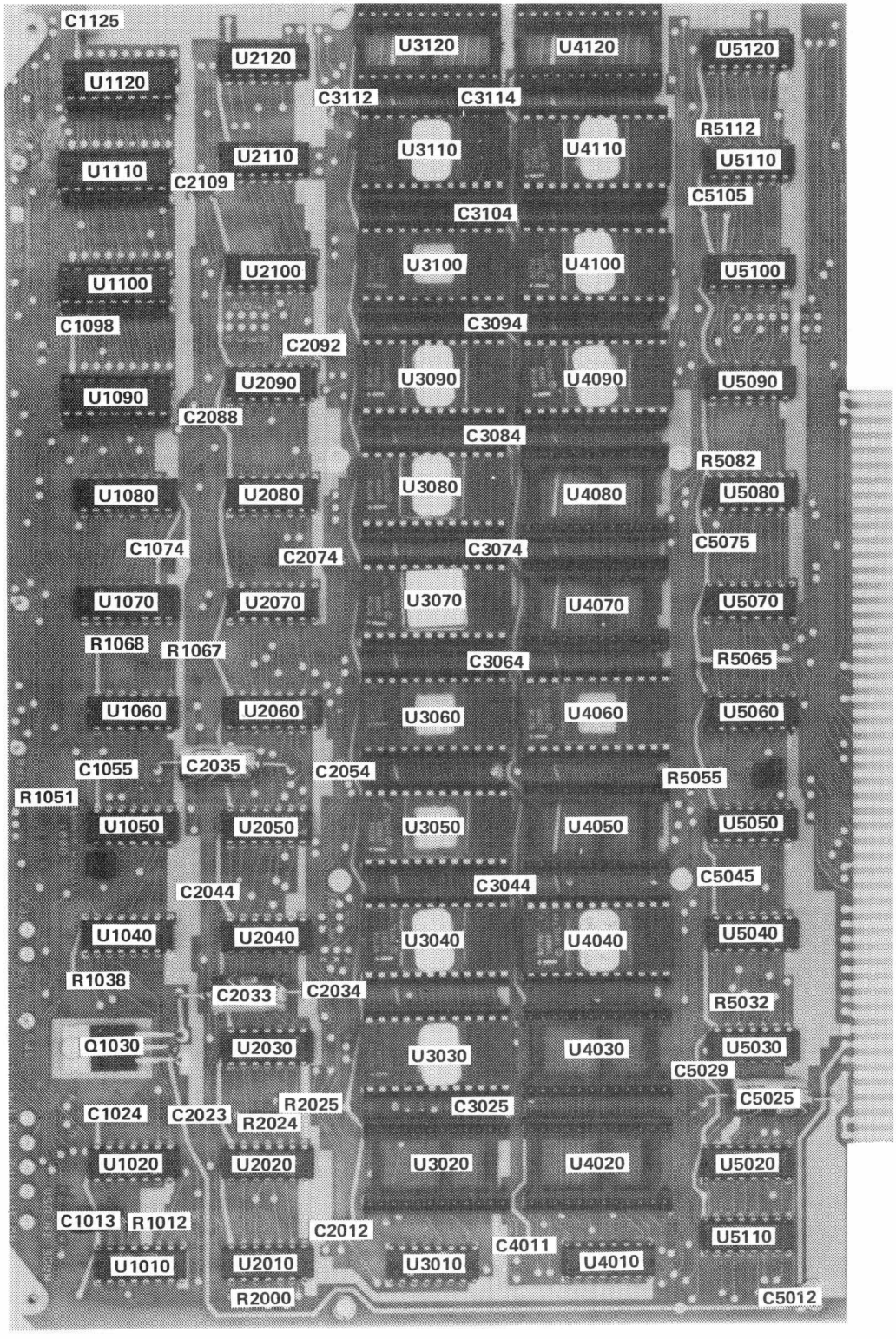
U5010 74157
U5090 7400
U3100 7400
U4130B 74109
U5120C 7400
U4120B 74109
U5120D 7400
U5120A 7400
U4130A 74109
U5090 7400
U4110B 74502
U4080 7420
U4090A 74109
U4090B 74109
U4100C 7400
U4100D 7400
U2070A 74504
U3020 74174
U3010 74157
U4100 7400
U2010A 74109
U4070A 7404
U3070A 7400
U3120 7404
U4110D 74502
U5090D 7400
U1050 BT97
U1060 BT97
U3070B 7400
U4060 BT26
U5060 BT26
U5100A 74109
U5100B 74109
U5110A 74109
U5110B 74109
U3050 LS670
U3030 LS670
U2050 LS670
U2030 LS670
U1030 7404
U2020 7404
U3040 74LS136
U2040 74LS136
U3080 74LS136
U3080 74LS136
U4020 74193
U5020 74193
U4030 74193
U5030 74193
U4050 BT26
U5050 BT26
U4040 BT26
U5040 BT26

NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)

Table 13-8

C1015	C3135
C1075	C3159
C1098	C4025
C1161	C4115
C2025	C4151
C2075	C5019
C2091	C5025
C2095	C5035
C2161	C5089
C3095	C5105
C3115	C5166





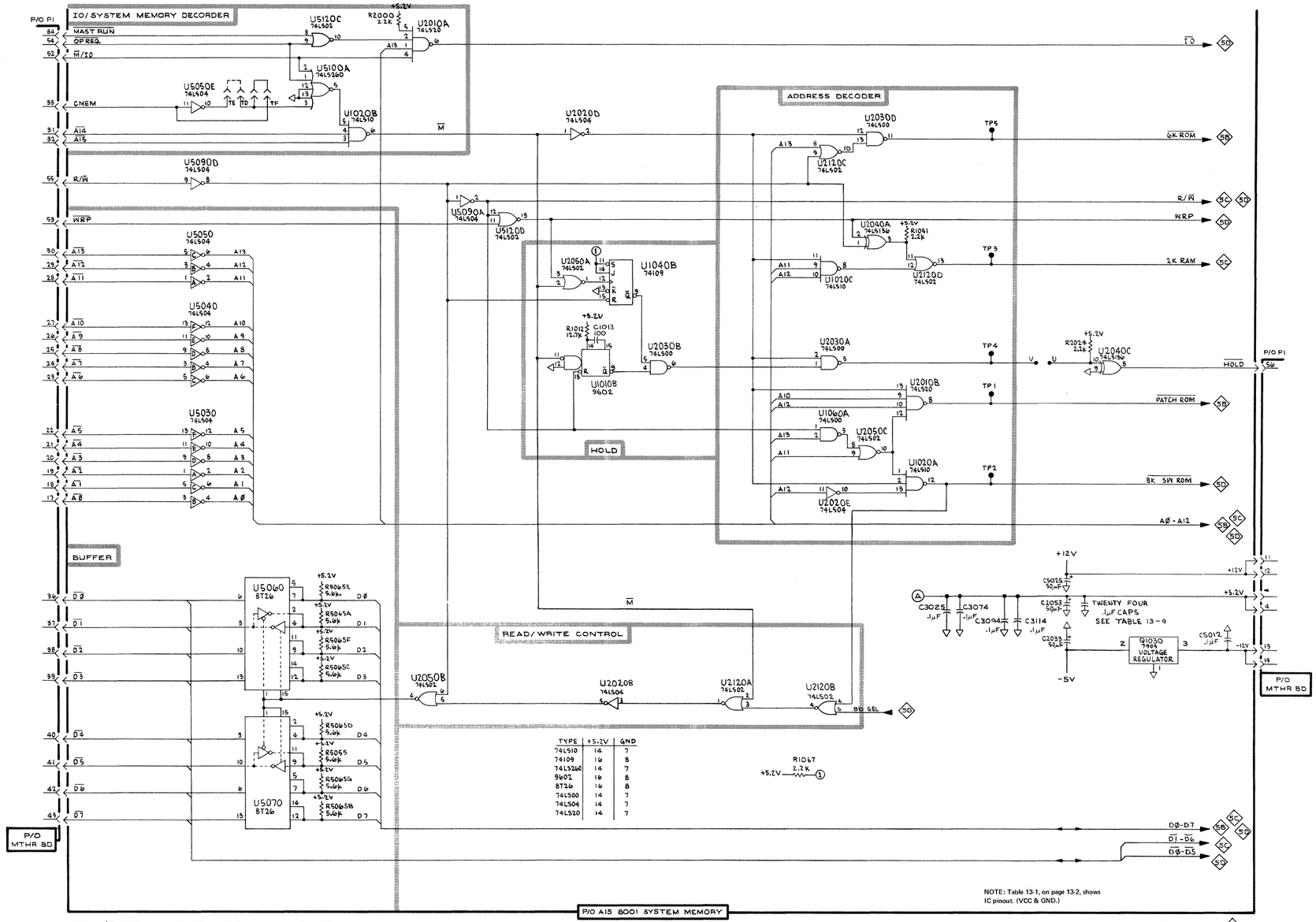
A-15 8001 System Memory Module

2312-16

COMPONENT LOCATION FOR 8001 SYSTEM MEMORY

Table 13-9

C1024	C2092
C1055	C2109
C1074	C3044
C1098	C3064
C1125	C3084
C2021	C3104
C2023	C3112
C2034	C4011
C2044	C5029
C2054	C5045
C2074	C5075
C2088	C5105



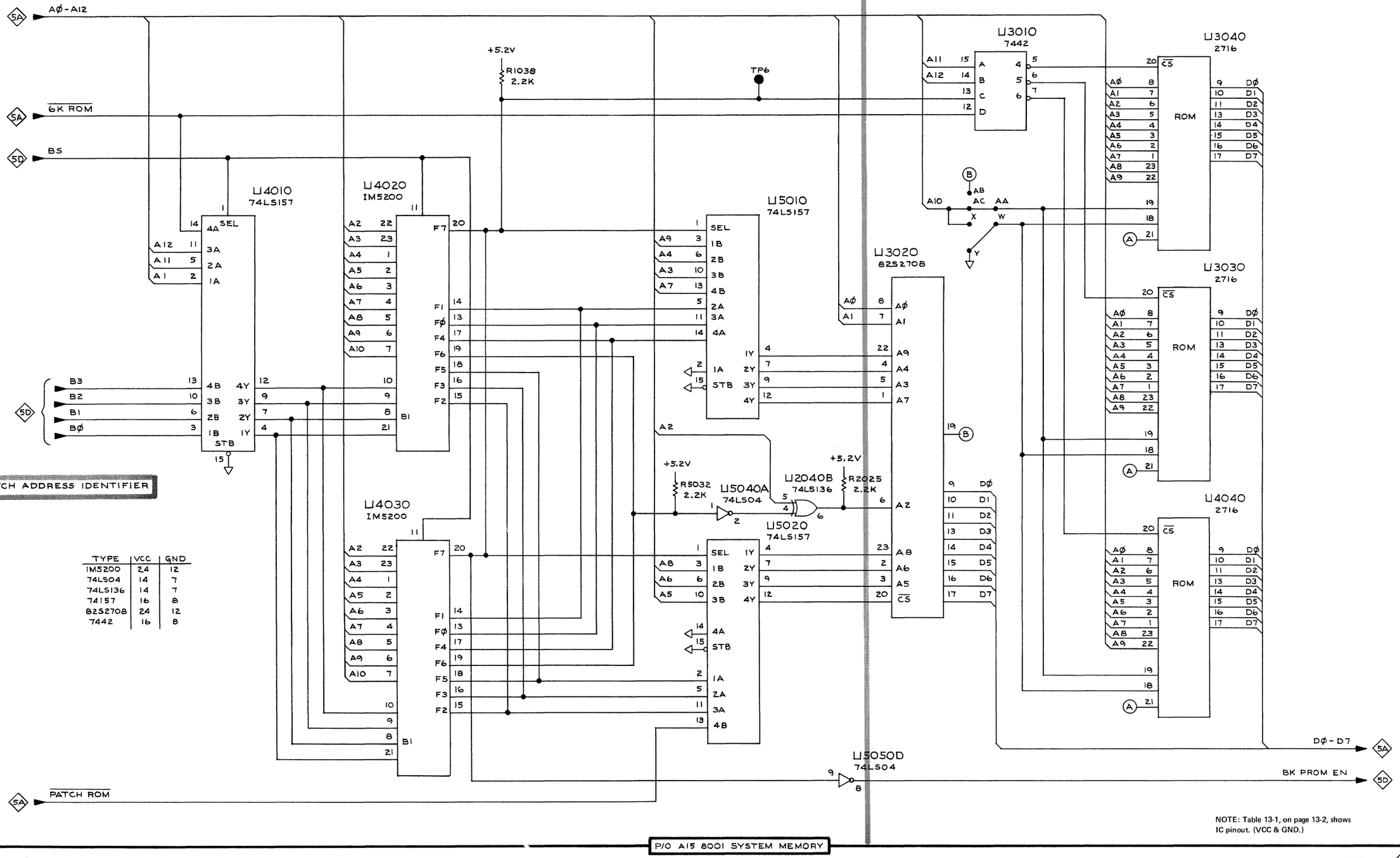
8001/8002A μPROCESSOR LAB SERVICE

@ 2711 - 53

SELECT LOGIC 5A

B032000

6K ROM AND PATCH ADDRESS LOGIC

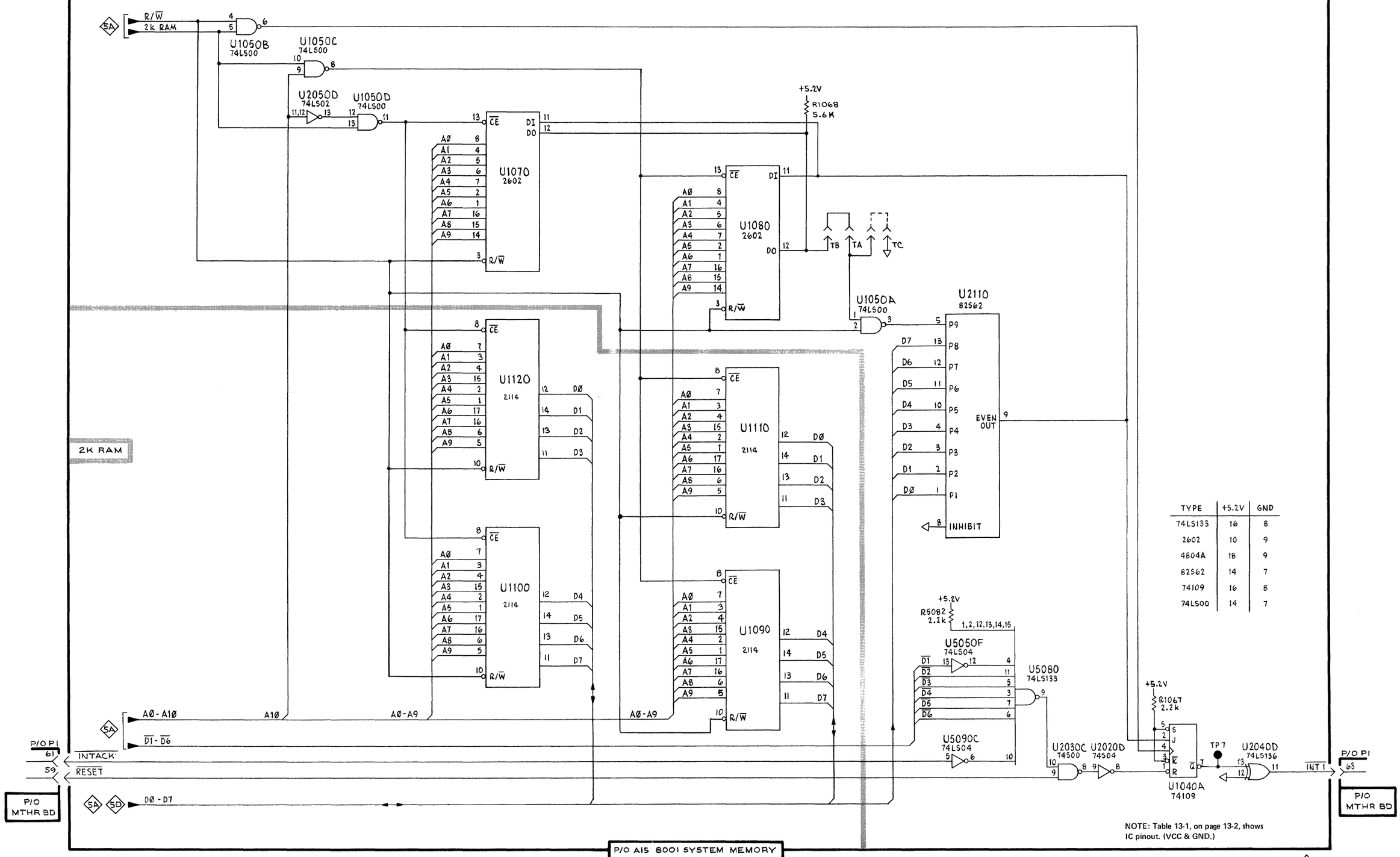


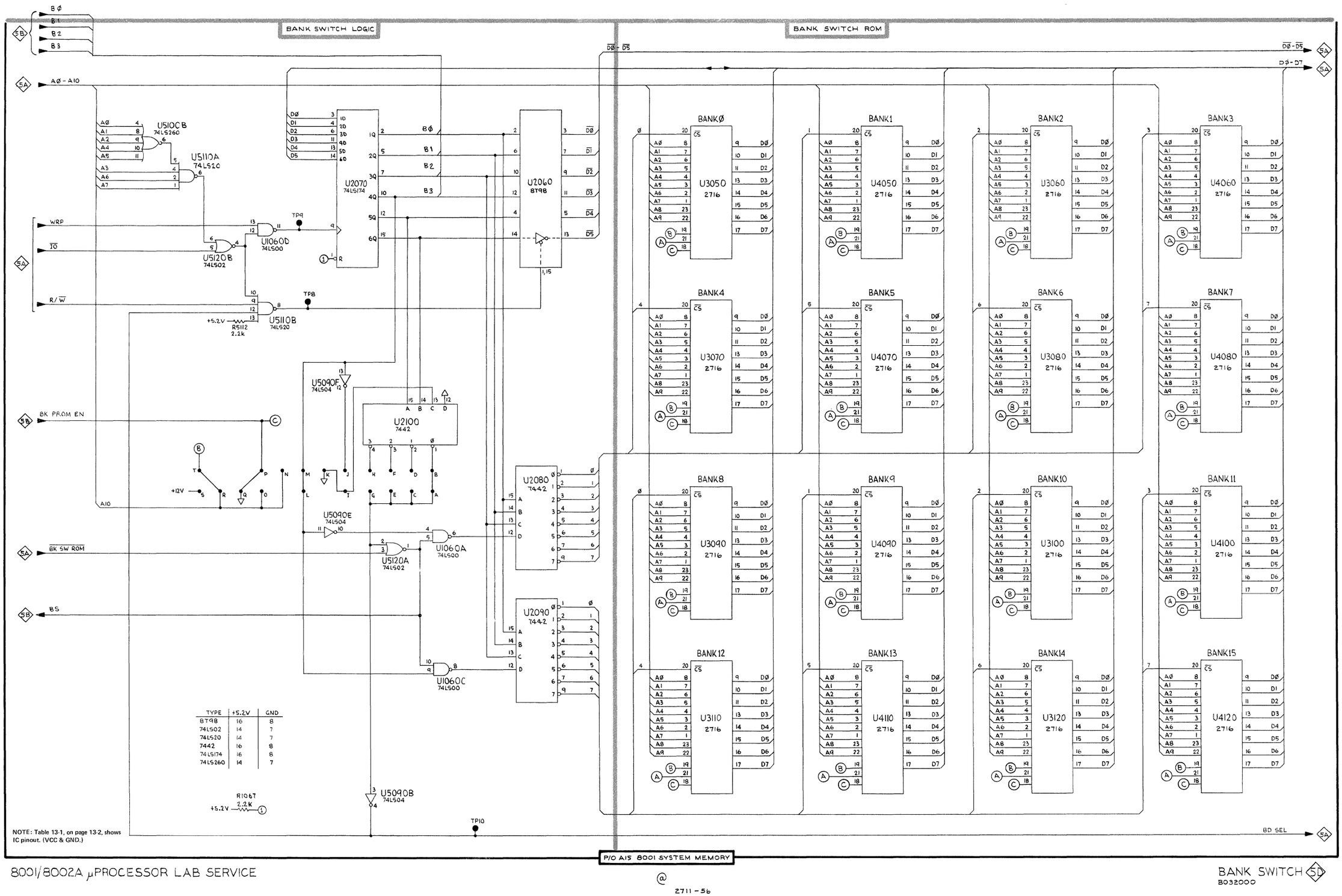
TYPE	VCC	GND
IM5200	24	12
74LS04	14	7
74LS136	14	7
74157	16	8
8252708	24	12
7442	16	8

NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)

P/O A15 8001 SYSTEM MEMORY

PARITY CONTROL LOGIC

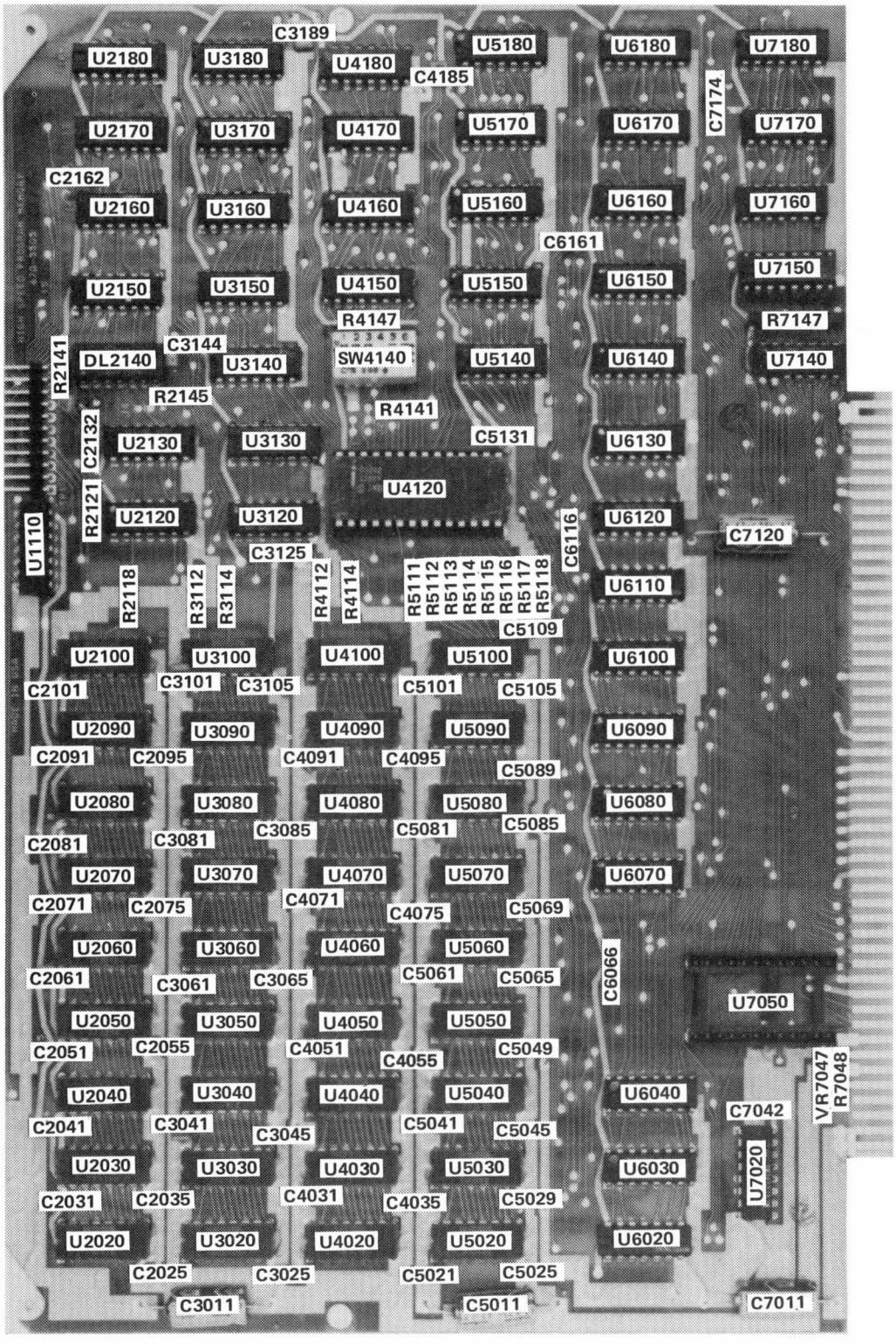




TYPE	+5.2V	GND
8T98	16	8
74LS02	14	7
74LS20	14	7
7442	16	8
74LS174	16	8
74LS260	14	7

NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)

P/O A15 8001 SYSTEM MEMORY

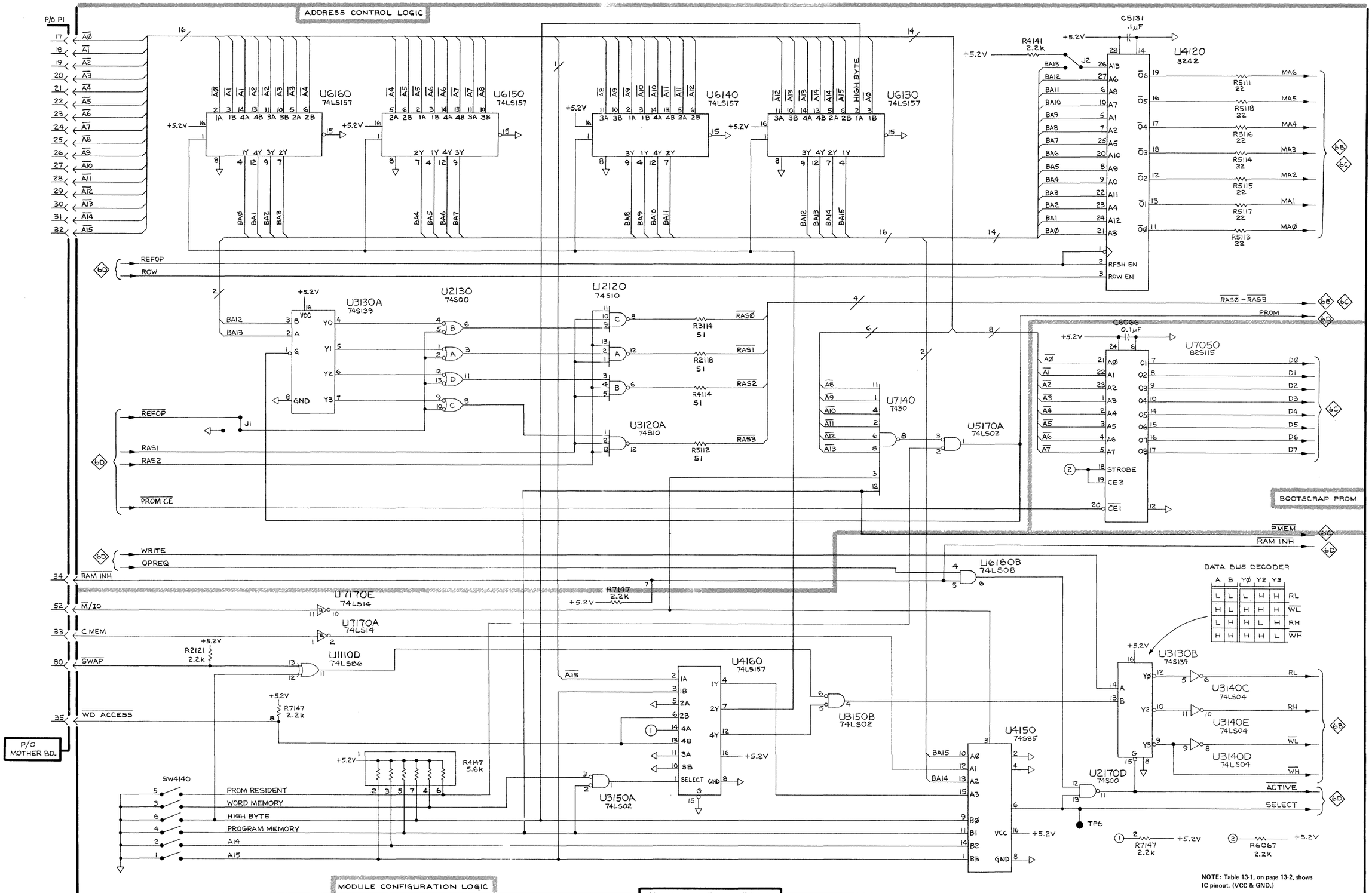


A-25 High-Speed Memory Module

2312-15

COMPONENT LOCATION FOR HIGH SPEED MEMORY

@


ADDRESS CONTROL LOGIC
P/O P1
U6160 74LS157
U6150 74LS157
U6140 74LS157
U6130 74LS157
HIGH BYTE
C5131 .1µF
R4141 2.2K
U4120 3242
RFSH EN
ROW EN
REFOP
ROW
U3130A 74S139
U2130 74S00
U2120 74S10
U3120A 74S10
U7140 7430
U5170A 74LS02
RAS0 – RAS3
PROM
C6066 0.1µF
U7050 82S115
STROBE
CE2
CE1
BOOTSCRAP PROM
REFOP
J1
RAS1
RAS2
PROM CE
WRITE
OPREQ
RAM INH
PMEM
U6180B 74LS08
DATA BUS DECODER
M/IO
C MEM
SWAP
WD ACCESS
U7170E 74LS14
U7170A 74LS14
U1110D 74LS86
R2121 2.2K
R7147 2.2K
U3130B 74S139
U3140C 74LS04
U3140E 74LS04
U3140D 74LS04
U2170D 74S00
ACTIVE
SELECT
TP6
P/O MOTHER BD.
SW4140
PROM RESIDENT
WORD MEMORY
HIGH BYTE
PROGRAM MEMORY
A14
A15
R4147 5.6K
U4160 74LS157
U3150A 74LS02
U3150B 74LS02
U4150 74S85
R6067 2.2K
MODULE CONFIGURATION LOGIC
P/O A25 HIGH SPEED MEMORY
NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)

P/O DATA AND PARITY CONTROL

RAM MEMORY

P/O P1

6A WL

6A RL

6A WH

6A RH

U6070 8T26

U6080 8T26

U6090 8T26

U6100 8T26

36	D0	LATCH 0	4	2	R0
37	D1		6	5	R1
38	D2	LATCH 1	7	14	R2
39	D3	LATCH 2	12	11	R3
		LATCH 3	9		
			15		
40	D4	LATCH 4	4	2	R4
41	D5		6	5	R5
42	D6	LATCH 5	7	14	R6
43	D7	LATCH 6	12	11	R7
		LATCH 7	9		
			15		
44	D8	LATCH 0	4	2	R0
45	D9		6	5	R1
46	D10	LATCH 1	7	14	R2
47	D11	LATCH 2	12	11	R3
		LATCH 3	9		
			15		
48	D12	LATCH 4	4	2	R4
49	D13		6	5	R5
50	D14	LATCH 5	7	14	R6
51	D15	LATCH 6	12	11	R7
		LATCH 7	9		
			15		

P/O MTHR BD

6C LATCH 0 - LATCH 7

6A MA0 - MA 6

6D WRT EN

6D CAS1, CAS2

6A RAS 0 - RAS 3

NOTE: All 4027P-2 at right have connections of sample shown below.

CAS	15	VDD	8 +12V
R	2	VCC	9 +5V
RAS	4	DIN DO	14 D_
MA 6	13	CS	
MA 5	7	A0	
MA 4	6	A1	
MA 3	5	A2	
MA 2	11	A3	
MA 1	10	A4	
MA 0	12	A5	
	3	WE	
VBB	1		-5V
VSS	16		

8

D3
D2
R0 - R7
D0 - D7
6C

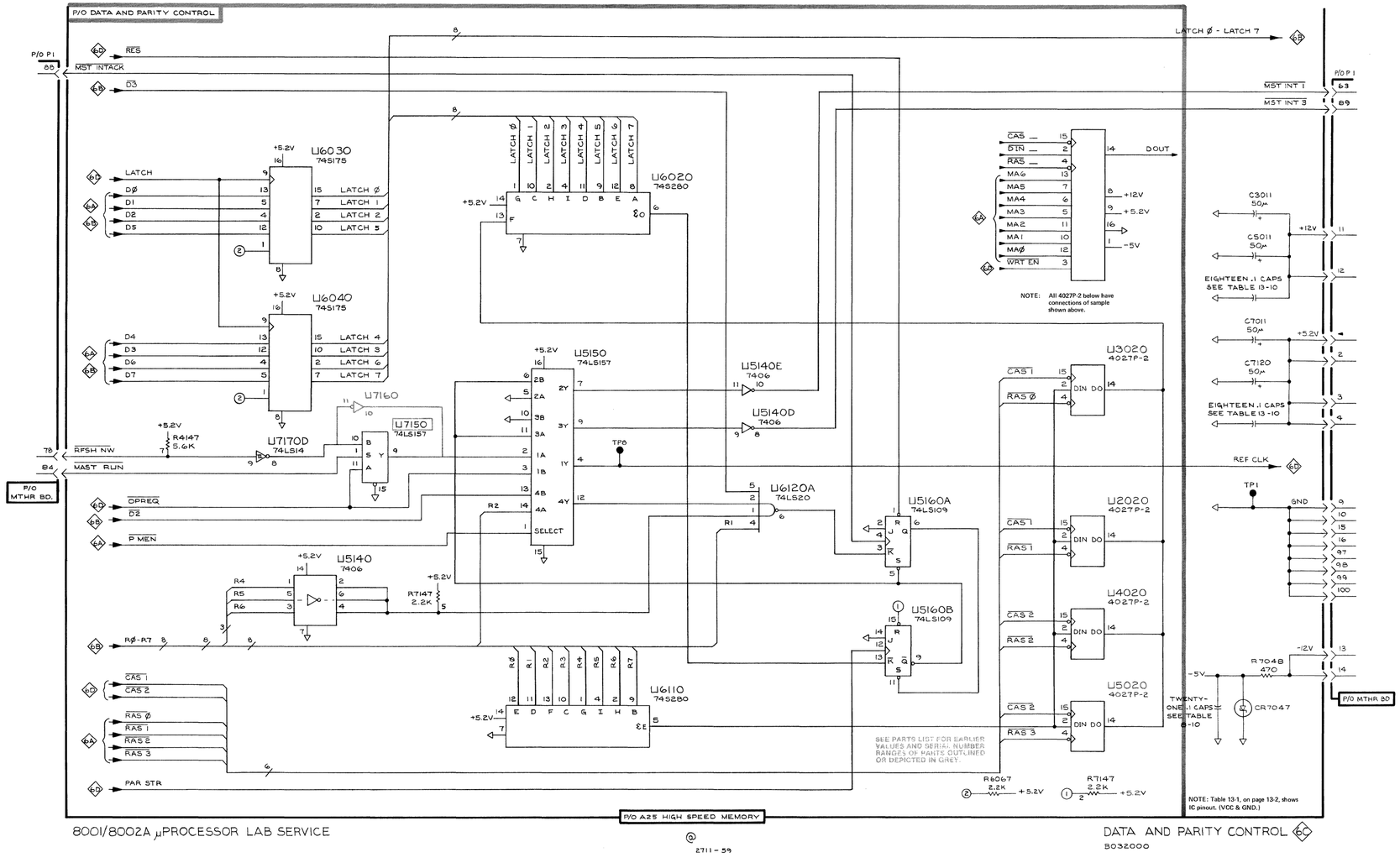
U3030	CAS1	15	U2030	CAS1	15	U4030	CAS2	15	U5030	CAS2	15
	R0	2		R0	2		R0	2		R0	2
	RAS0	4		RAS1	4		RAS2	4		RAS3	4
	DIN DO			DIN DO			DIN DO			DIN DO	
	14 D0			14 D0			14 D0			14 D0	
U3040	CAS1	15	U2040	CAS1	15	U4040	CAS2	15	U5040	CAS2	15
	R1	2		R1	2		R1	2		R1	2
	RAS0	4		RAS1	4		RAS2	4		RAS3	4
	DIN DO			DIN DO			DIN DO			DIN DO	
	14 D1			14 D1			14 D1			14 D1	
U3050	CAS1	15	U2050	CAS1	15	U4050	CAS2	15	U5050	CAS2	15
	R2	2		R2	2		R2	2		R2	2
	RAS0	4		RAS1	4		RAS2	4		RAS3	4
	DIN DO			DIN DO			DIN DO			DIN DO	
	14 D2			14 D2			14 D2			14 D2	
U3060	CAS1	15	U2060	CAS1	15	U4060	CAS2	15	U5060	CAS2	15
	R3	2		R3	2		R3	2		R3	2
	RAS0	4		RAS1	4		RAS2	4		RAS3	4
	DIN DO			DIN DO			DIN DO			DIN DO	
	14 D3			14 D3			14 D3			14 D3	
U3070	CAS1	15	U2070	CAS1	15	U4070	CAS2	15	U5070	CAS2	15
	R4	2		R4	2		R4	2		R4	2
	RAS0	4		RAS1	4		RAS2	4		RAS3	4
	DIN DO			DIN DO			DIN DO			DIN DO	
	14 D4			14 D4			14 D4			14 D4	
U3080	CAS1	15	U2080	CAS1	15	U4080	CAS2	15	U5080	CAS2	15
	R5	2		R5	2		R5	2		R5	2
	RAS0	4		RAS1	4		RAS2	4		RAS3	4
	DIN DO			DIN DO			DIN DO			DIN DO	
	14 D5			14 D5			14 D5			14 D5	
U3090	CAS1	15	U2090	CAS1	15	U4090	CAS2	15	U5090	CAS2	15
	R6	2		R6	2		R6	2		R6	2
	RAS0	4		RAS1	4		RAS2	4		RAS3	4
	DIN DO			DIN DO			DIN DO			DIN DO	
	14 D6			14 D6			14 D6			14 D6	
U3100	CAS1	15	U2100	CAS1	15	U4100	CAS2	15	U5100	CAS2	15
	R7	2		R7	2		R7	2		R7	2
	RAS0	4		RAS1	4		RAS2	4		RAS3	4
	DIN DO			DIN DO			DIN DO			DIN DO	
	14 D7			14 D7			14 D7			14 D7	

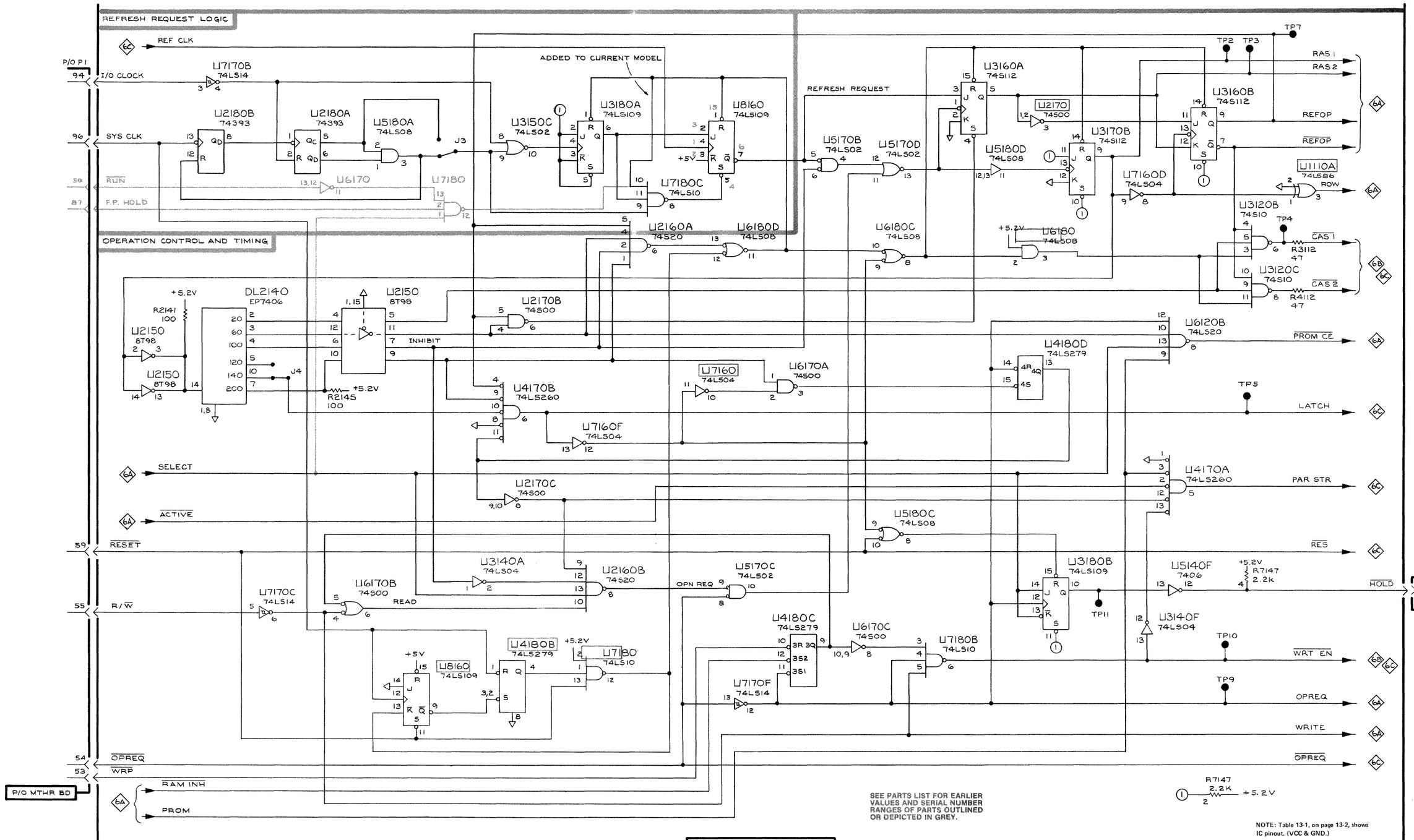
NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)

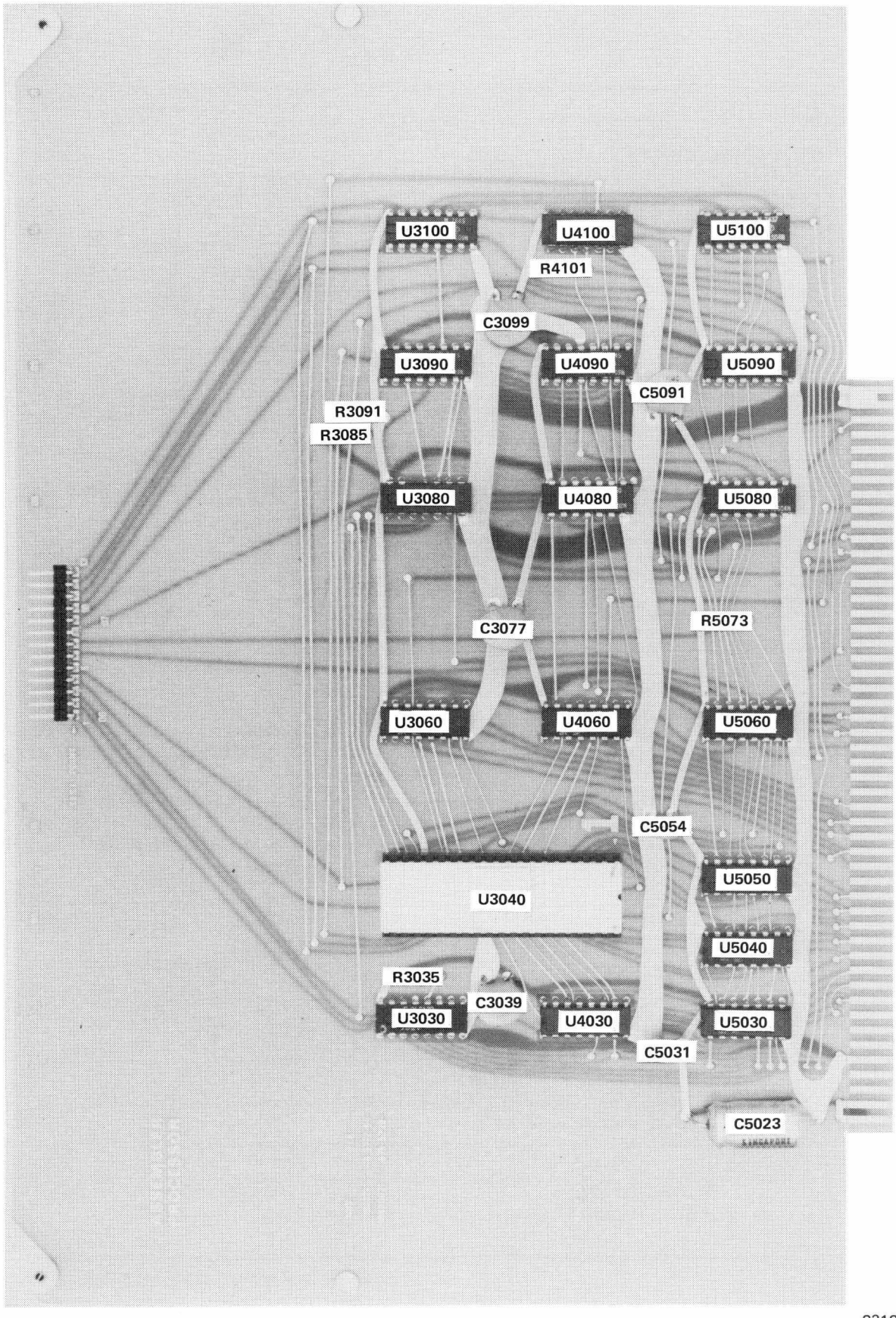
P/O A25 HIGH SPEED MEMORY

Table 13-10 CAPACITOR INFORMATION

+5.2 V	–12 V	+12 V
C2025	C2041	C2035
C2031	C2061	C2055
C2051	C2081	C2075
C2071	C2101	C2095
C2091	C2132	C3025
C3041	C2162	C3045
C3061	C3125	C3065
C3081	C3144	C3085
C3101	C3189	C3105
C4031	C4185	C4035
C4051	C5029	C4055
C4071	C5049	C4075
C4091	C5069	C4095
C5021	C5089	C5025
C5041	C5109	C5045
C5061	C5131	C5065
C5081	C6066	C5085
C5101	C6116	C5105
C6161	C6161	
	C7042	
	C7174	




REFRESH REQUEST LOGIC
OPERATION CONTROL AND TIMING
REF CLK
P/O P1
94 I/O CLOCK
96 SYS CLK
58 RUN
87 F.P. HOLD
U7170B 74LS14
U2180B 74393
U2180A 74393
U5180A 74LS08
J3
U3150C 74LS02
U3180A 74LS109
U8160 74LS109
U7180C 74LS10
U6170
U7180
ADDED TO CURRENT MODEL
REFRESH REQUEST
U3160A 74S112
U2170 74S00
U3160B 74S112
U5170B 74LS02
U5170D 74LS02
U5180D 74LS08
U3170B 74S112
U7160D 74LS04
U1110A 74LS86
ROW
U3120B 74S10
U3120C 74S10
U2160A 74S20
U6180D 74LS08
U6180C 74LS08
U6180 74LS08
+5.2V
TP7
TP2
TP3
TP4
RAS 1
RAS 2
REFOP
REFOP
CAS 1
CAS 2
R3112 47
R4112 47
DL2140 EP7406
U2150 8T98
R2141 100
R2145 100
U2170B 74S00
INHIBIT
U4170B 74LS260
U7160 74LS04
U6170A 74S00
U4180D 74LS279
U6120B 74LS20
PROM CE
TP5
LATCH
U7160F 74LS04
U2170C 74S00
U4170A 74LS260
PAR STR
SELECT
ACTIVE
59 RESET
55 R/W
U7170C 74LS14
U6170B 74S00
READ
U3140A 74LS04
U2160B 74S20
U5170C 74LS02
OPN REQ
U5180C 74LS08
U3180B 74LS109
U5140F 7406
R7147 2.2K
HOLD
P/O P1 56
P/O MTHR BD
TP11
U3140F 74LS04
TP10
WRT EN
TP9
OPREQ
WRITE
U4180C 74LS279
U6170C 74S00
U7180B 74LS10
U4180B 74LS279
U7180 74LS10
U7170F 74LS14
54 OPREQ
53 WRP
RAM INH
PROM
P/O MTHR BD
R7147 2.2K +5.2V
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.
NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)
P/O A25 HIGH SPEED MEMORY

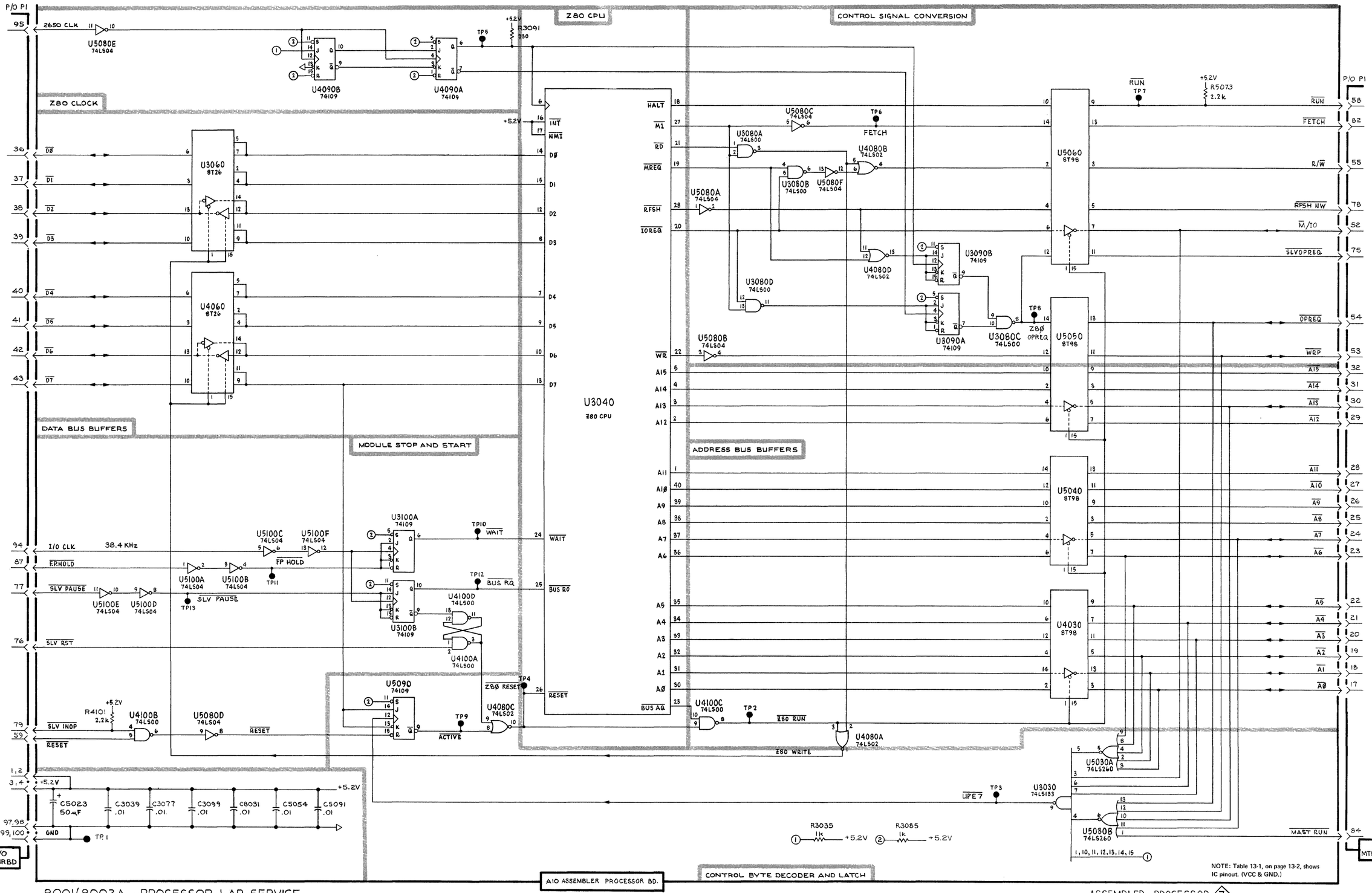


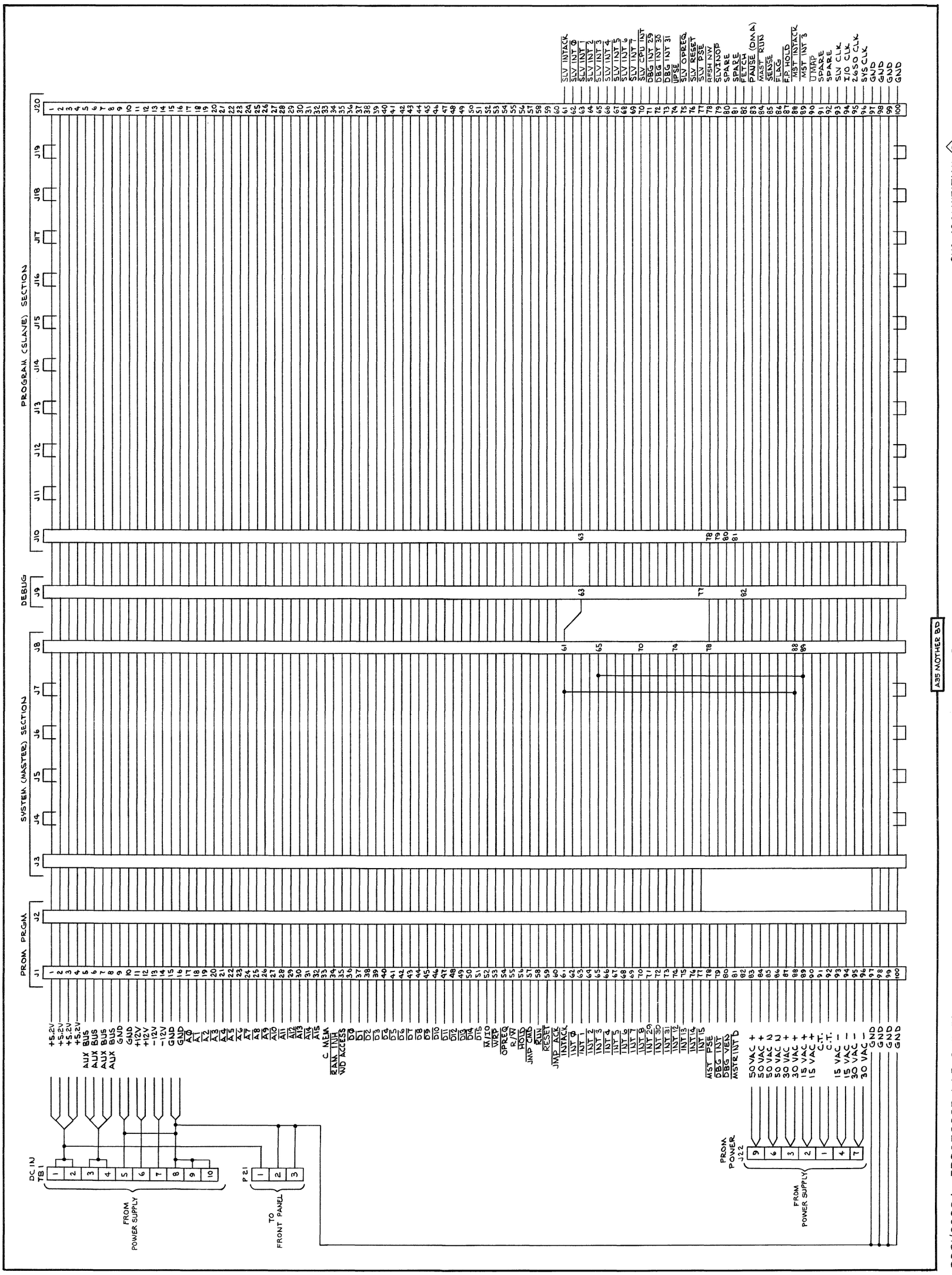
A-10 Assembler Processor Module

2312-1

COMPONENT LOCATION FOR ASSEMBLER PROCESSOR

@


P/O P1
Z80 CPU
CONTROL SIGNAL CONVERSION
Z80 CLOCK
DATA BUS BUFFERS
MODULE STOP AND START
ADDRESS BUS BUFFERS
CONTROL BYTE DECODER AND LATCH
U3040
Z80 CPU
2650 CLK
U5080E
74LS04
U4090B
74109
U4090A
74109
+5.2V
R3091
330
TP5
INT
NMI
HALT
M1
RD
MREQ
IORQ
RFSH
WR
BUS AQ
D0
D1
D2
D3
D4
D5
D6
D7
U3060
8T26
U4060
8T26
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
U5080A
74LS04
U5080B
74LS04
U5080C
74LS04
U3080A
74LS00
U3080B
74LS00
U3080C
74LS00
U3080D
74LS00
U4080B
74LS02
U4080C
74LS02
U4080D
74LS02
U5080F
74LS04
FETCH
TP6
U3090A
74109
U3090B
74109
Z80 OPREQ
TP8
RUN
TP7
+5.2V
R5073
2.2k
U5060
8T98
U5050
8T98
U5040
8T98
U4030
8T98
U5030A
74LS240
U5030B
74LS240
U3030
74LS133
TP3
UPE7
R3035
1k
R3085
1k
1,10,11,12,13,14,15
RUN
FETCH
R/W
RFSH NW
M/IO
SLVOPREQ
OPREQ
WRP
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
MAST RUN
P/O P1
P/O MTHR BD
I/O CLK
38.4 KHz
F.P.HOLD
SLV PAUSE
SLV RST
SLV INOP
RESET
GND
U5100C
74LS04
U5100F
74LS04
U5100A
74LS04
U5100B
74LS04
U5100E
74LS04
U5100D
74LS04
FP HOLD
TP11
TP13
U3100A
74109
U3100B
74109
TP10
WAIT
TP12
BUS RQ
U4100D
74LS00
U4100A
74LS00
U5090
74109
TP4
Z80 RESET
TP9
ACTIVE
R4101
2.2k
U4100B
74LS00
U5080D
74LS04
U4100C
74LS00
TP2
Z80 RUN
U4080A
74LS02
Z80 WRITE
C5023
50mF
C3039
.01
C3077
.01
C3099
.01
C8031
.01
C5054
.01
C5091
.01
TP1
P/O MTHR BD
NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)
A10 ASSEMBLER PROCESSOR BD.
@ 2711-61
8001/8002A μPROCESSOR LAB SERVICE
ASSEMBLER PROCESSOR 7
8032000
ASSEMBLER PROCESSOR
7

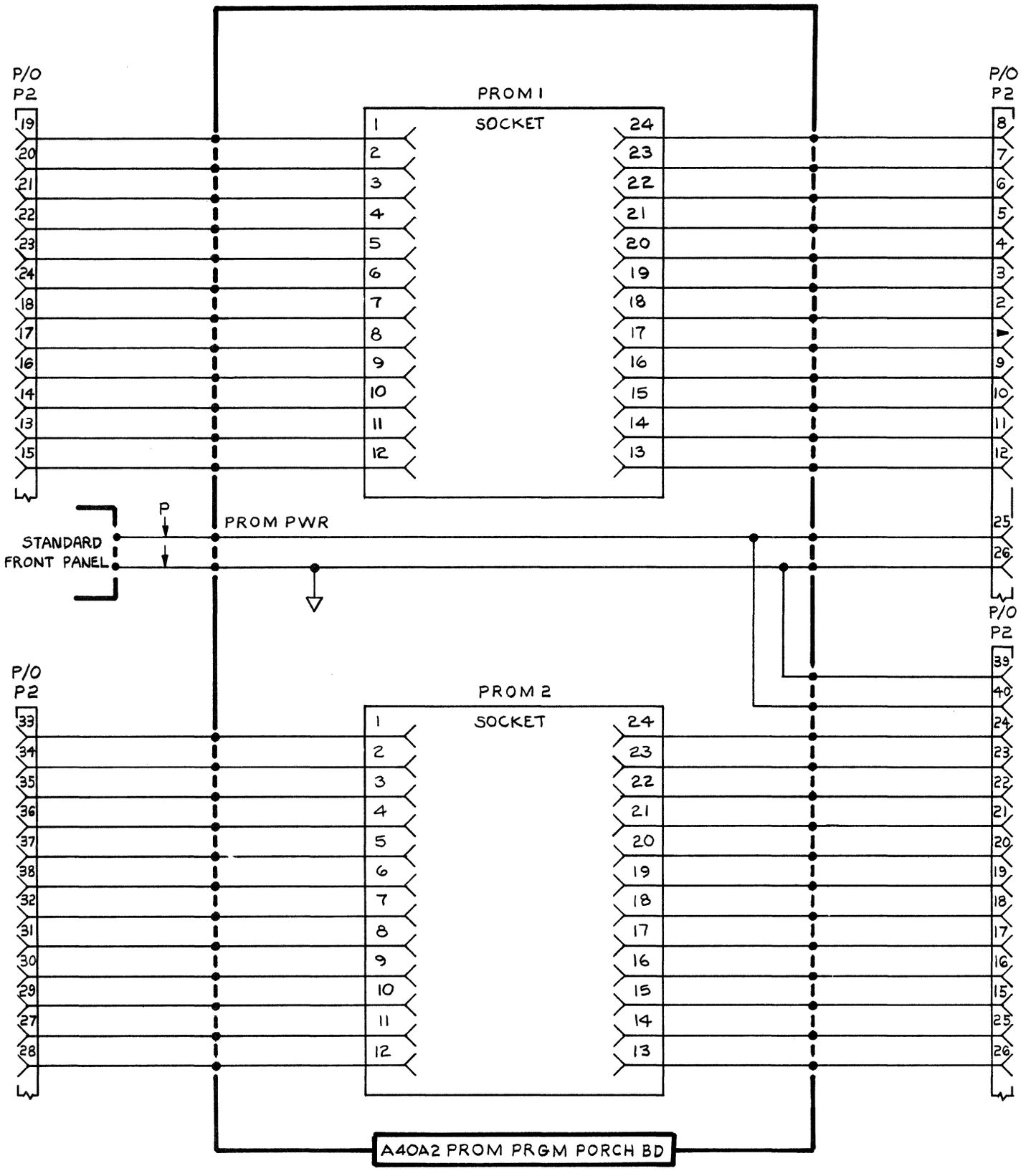


BUS ORGANIZATION 8 V5
B032000

8001/8002A μPROCESSOR LAB SERVICE

P/O DEBUG AND FRONT PANEL
P/O P3
+5.2V
P/O P2
P/O P1
P/O MTHR BD
GND
C2017 50µf
C2096 0.01
C2139 0.01
P/O DEBUG AND FRONT PANEL
MASTER
RUN
HOLD
+5.2V
P/O R1093 220
CR1086 MASTER
CR1087
CR1096 SLAVE
CR1097
P/O R1123 220
CR1126 RUN
CR1127
CR1146 POWER
CR1147
P/O R1023 220
CR1018 PROM POWER
CR1017
+5.2V
P/O R2079 2.2K
U2080A 7406
U2080 7406
U2120A 8T98
U2080 7406
U2120 8T98
PROM POWER
S3012
+5.2V
P/O R2039 2.2K
PROM COM
PROM POWER
P21
+5.2V
P/O R2079 2.2K
U2070 7400
P/O P2
P3
P/O DEBUG AND FRONT PANEL
DIAG INTRPT
S3081
DIAG INT
U2070A 7400
+5.2V
P/O R2099 2.2K
U2120 8T98
RST HOLD
RESET
+5.2V
P/O R2099 2.2K
P/O R2149 2.2K
U2150 74109
RESET
S3141
A40 STANDARD FRONT PANEL BD

NOTE: Table 13-1, on page 13-2, shows IC pinout. (VCC & GND.)



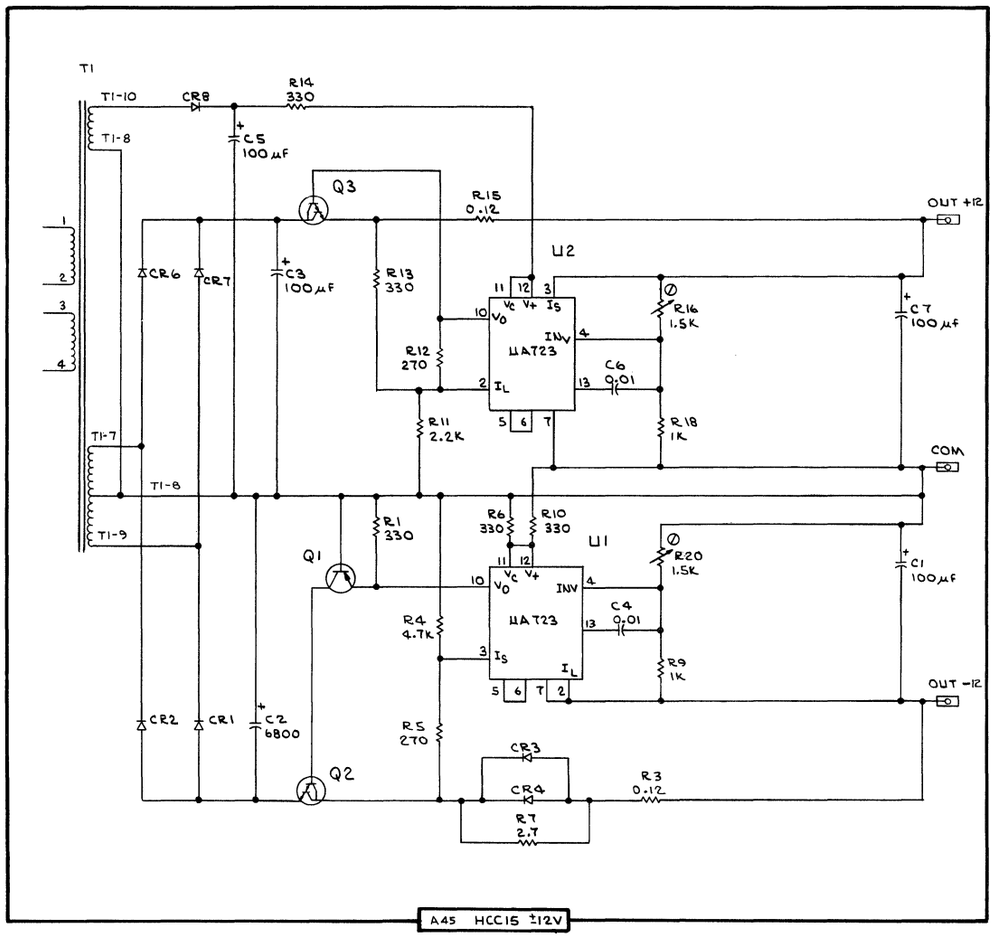
8001/8002A

µPROCESSOR LAB SERVICE @ PROM PRGM PORCH 10 BG

2711-64

B032000

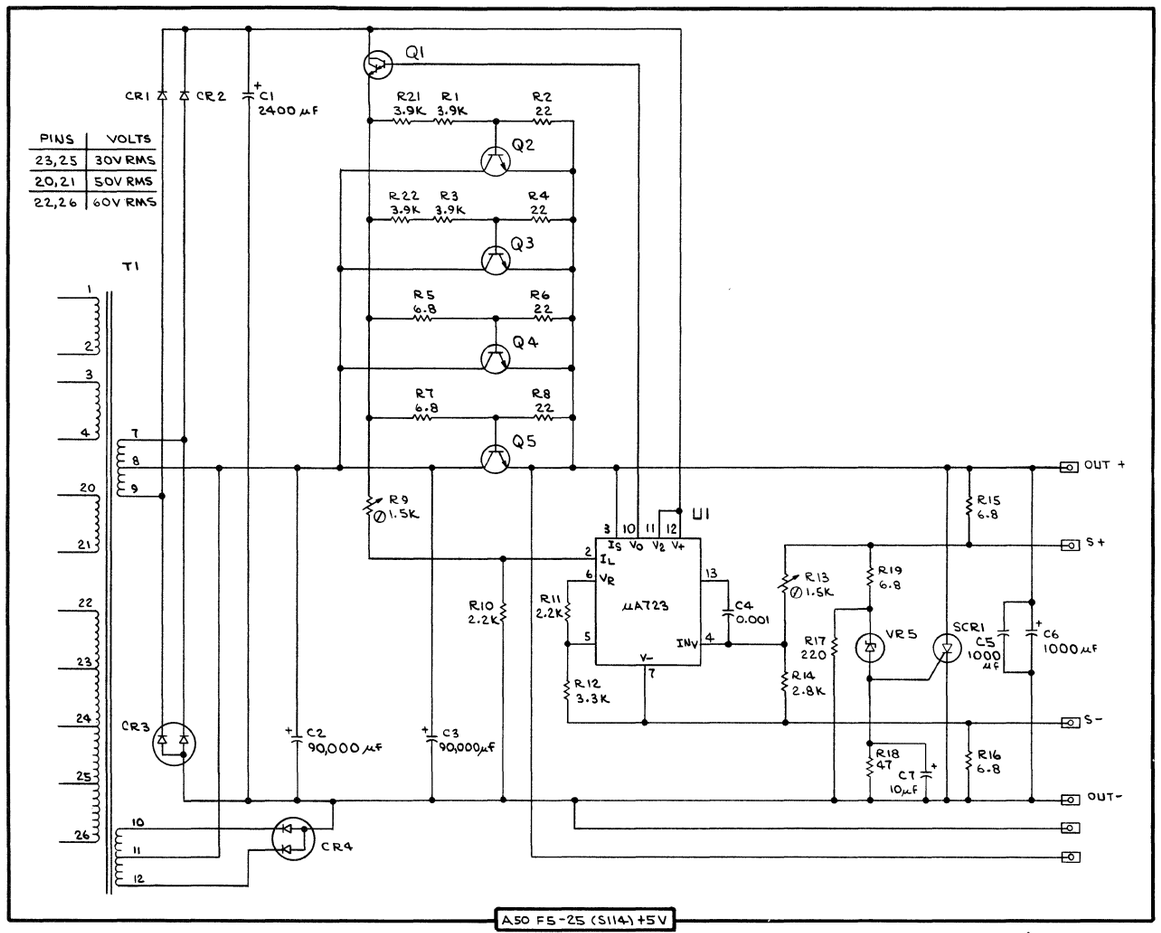
PROM PRGM PORCH 10



8001/8002A µPROCESSOR LAB SERVICE

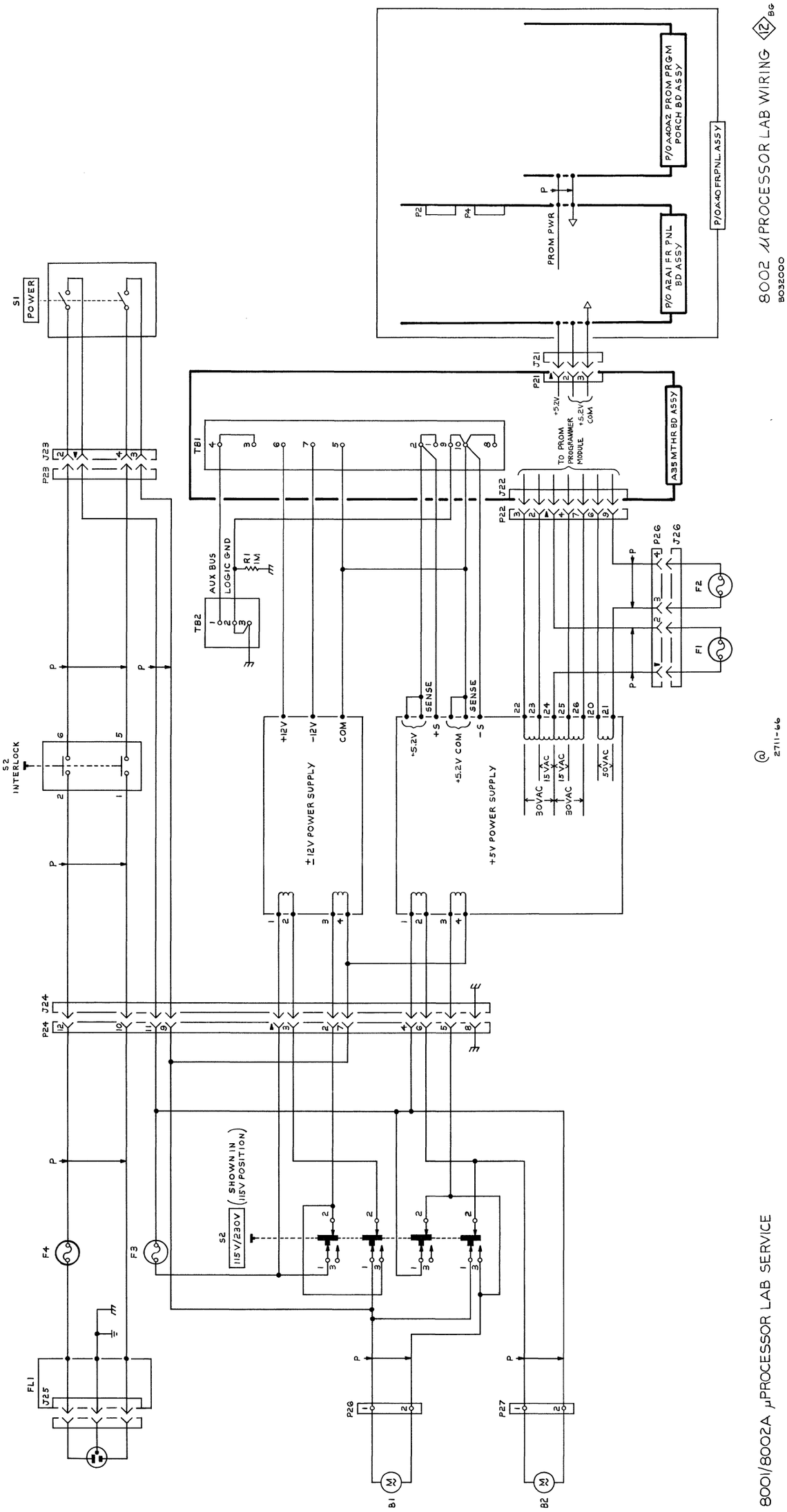
@

2711-65



POWER SUPPLY 11 VS

B032000


8002 μPROCESSOR LAB WIRING 12 BG
B032000
S1 POWER
S2 INTERLOCK
P23 J23
P
TB1
TB2
AUX BUS
LOGIC GND
R1 1M
P21 J21
P22 J22
A35 MTHR BD ASSY
TO PROM PROGRAMMER MODULE
+5.2V
COM
P/O A40A2 PROM PRGM PORCH BD ASSY
P/O A40 FR PNL ASSY
P/O A2A1 FR PNL BD ASSY
PROM PWR
P2
P4
P26 J26
F1
F2
F3
F4
S2 115V/230V (SHOWN IN 115V POSITION)
FL1 J25
P24 J24
+12V
-12V
COM
±12V POWER SUPPLY
-5.2V
+5
-5
SENSE
+5.2V COM
+5V POWER SUPPLY
22
23
24
25
26
20
21
30VAC
15VAC
P26
P27
B1
B2
8001/8002A μPROCESSOR LAB SERVICE
@ 2711-66

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W/	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000CR	MILLENNIUM INFORMATION SYSTEMS, INC.	19020 PRUNERIDGE AVENUE	CUPERTINO, CA 95014
00779	AMP, INC.	P O BOX 3608	HARRISBURG, PA 17105
01295	TEXAS INSTRUMENTS, INC., SEMICONDUCTOR GROUP	P O BOX 5012, 13500 N CENTRAL EXPRESSWAY	DALLAS, TX 75222
01963	CHERRY ELECTRICAL PRODUCTS CORPORATION	3600 SUNSET AVENUE	WAUKEGAN, IL 60085
02777	HOPKINS ENGINEERING COMPANY	12900 FOOTHILL BLVD.	SAN FERNANDO, CA 91342
04009	ARROW-HART, INC.	103 HAWTHORNE STREET	HARTFORD, CT 06106
05574	VIKING INDUSTRIES, INC.	21001 NORDHOFF STREET	CHATSWORTH, CA 91311
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
19613	TEXTOOL PRODUCTS, INC.	1410 W PIONEER DRIVE	IRVING, TX 75061
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
23880	STANFORD APPLIED ENGINEERING, INC.	340 MARTIN AVE.	SANTA CLARA, CA 95050
27264	MOLEX PRODUCTS CO.	5224 KATRINE AVE.	DOWNERS GROVE, IL 60515
71279	CAMBRIDGE THERMIONIC CORP.	445 CONCORD AVE.	CAMBRIDGE, MA 02138
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
@76381	MINNESOTA MINING AND MFG. CO.	3M CENTER	ST. PAUL, MN 55101
77969	RUBBERCRAFT CORP. OF CALIF., LTD.	1800 W. 220TH ST.	TORRANCE, CA 90507
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
82389	SWITCHCRAFT, INC.	5555 N. ELSTON AVE.	CHICAGO, IL 60630
82647	TEXAS INSTRUMENTS, INC., CONTROL PRODUCTS DIV.	34 FOREST ST.	ATTLEBORO, MA 02703
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
93907	CAMCAR SCREW AND MFG. CO.	600 18TH AVE.	ROCKFORD, IL 61101

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Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1 -1	390-0583-00			1		CAB.TOP,CONT:	80009	390-0583-00
						(ATTACHING PARTS)		
-2	212-0137-00			6		SCREW MACHINE:8-32 X 0.375 L,PNH,STEEL	83385	OBD
						- - - * - - -		
-3	334-1555-00			4		PLATE,IDENT:TRADEMARK	80009	334-1555-00
-4	426-0928-00			4		FRAME,TRIM:GRAY PLASTIC	80009	426-0928-00
						(ATTACHING PARTS FOR EACH)		
-5	213-0088-00			1		SCR,TPG,THD CTG:4-24 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-6	426-1444-00			2		FRAME SECT,CAB.:UPPER	80009	426-1444-00
						(ATTACHING PARTS FOR EACH)		
-7	210-0457-00			4		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-8	390-0582-00			1		CABINET BOTTOM:	80009	390-0582-00
						(ATTACHING PARTS)		
-9	212-0008-00			4		SCREW,MACHINE:8-32 X 0.500 INCH,PNH STL	83385	OBD
						- - - * - - -		
-10	348-0128-01			4		FOOT,CABINET:POLYURETHANE,BLACK	80009	348-0128-01
						(ATTACHING PARTS FOR EACH)		
-11	212-0008-00			2		SCREW,MACHINE:8-32 X 0.500 INCH,PNH STL	83385	OBD
						- - - * - - -		
-12	361-0871-00			2		SPACER,SLEEVE:0.2 L X 0.405ID,ALUMINUM	80009	361-0871-00
-13	426-1445-00			2		FRAME SECT,CAB.:LOWER	80009	426-1445-00
						(ATTACHING PARTS FOR EACH)		
-14	210-0457-00			4		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-15	386-3792-00			2		STIF,FRONT PNL:	000CR	14990041
						(ATTACHING PARTS FOR EACH)		
-16	210-0586-00			5		NUT,PLAIN,EXT W:4-40 X 0.25 INCH,STL	78189	211-041800-00
						- - - * - - -		
-17	260-1842-00			1		SWITCH,ROCKER:DPST,16A,250VAC	04009	2600-11E
-18	----- -----			1		CKT BOARD ASSY:LOWER FRONT PNL(SEE A40 EPL)		
						(ATTACHING PARTS)		
-19	211-0661-00			6		SCREW,MACHINE:4-40 X 0.25 INCH,PNH,STL	93907	821-01655-024
						- - - * - - -		
-20	129-0737-00			6		SPACER,POST:0.75 L,4-40 THD THRU,AL	80009	129-0737-00
-21	214-2682-00			1		IND,DIFFUSER:9.75 L X 1.25W,PLASTIC	80009	214-2682-00
-22	331-0437-00			1		MASK,LED:CONTROLLER	80009	331-0437-00
-23	407-2013-00			1		BRACKET,CKT BD:ALUMINUM	80009	407-2013-00
						(ATTACHING PARTS)		
-24	210-0457-00			4		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
						- - - * - - -		
-25	----- -----			1		CKT BOARD ASSY:PROM SOCKET(SEE A40A2 EPL)		
						(ATTACHING PARTS)		
-26	210-0586-00			4		NUT,PLAIN,EXT W:4-40 X 0.25 INCH,STL	78189	211-041800-00
-27	210-1063-00			4		WASHER,FLAT:0.147 ID X 0.1 THK,ABS,0.29 OD	80009	210-1063-00
-28	361-0950-00			4		SPACER,CKT BOARD:PLASTIC	80009	361-0950-00
						- - - * - - -		
	----- -----			-		. . CKT BOARD ASSY INCLUDES:		
-29	136-0536-00			2		. . SOCKET,PLUG-IN:24 PIN,W/LOCKING LEVER	19613	244-0331-00-0605
-30	333-2340-00			1		PANEL,FRONT:	80009	333-2340-00
-31	200-2119-00			1		COVER,CKT CARD:PROM SOCKET	80009	200-2119-00
-32	333-2344-00			1		PANEL,FRONT:	80009	333-2344-00
						(ATTACHING PARTS)		
-33	212-0137-00			4		SCREW MACHINE:8-32 X 0.375 L,PNH,STEEL	83385	OBD
						- - - * - - -		
-34	214-2685-00			1		KEY,CIRCUIT BD:	80009	214-2685-00
						(ATTACHING PARTS)		
-35	211-0510-00			2		SCREW,MACHINE:6-32 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-36	260-1497-00			1		SWITCH,PUSH:DPDT,10A,250VAC	01963	E79-30A
-37	407-2024-00			1		BRACKET,ANGLE:INTERLOCK SWITCH	80009	407-2024-00
						(ATTACHING PARTS)		
-38	210-0457-00			2		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
-39	211-0510-00			2		SCREW,MACHINE:6-32 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-40	200-2156-00			1		COVER,PWR SPLY:5V	80009	200-2156-00
						(ATTACHING PARTS)		
-41	211-0510-00			2		SCREW,MACHINE:6-32 X 0.375 INCH,PNH STL	83385	OBD
-42	211-0511-00			2		SCREW,MACHINE:6-32 X 0.50 INCH,PNH STL	83385	OBD
						- - - * - - -		
	343-0709-00			1		CLAMP,CABLE:4.38 L,ALUMINUM	80009	343-0709-00
-43	343-0722-01			5		CLAMP,CABLE:3.125 L,ALUMINUM,W/BUSHINGS	80009	343-0722-01
						(ATTACHING PARTS)		
-44	210-0949-00			14		WASHER,FLAT:0.141 ID X 0.50 INCH OD,BRS	12327	OBD
-45	210-0409-00			4		NUT,PLAIN,HEX.:8-32 X 0.312 INCH,BRS	73743	3046-402
						- - - * - - -		
-46	200-2157-00			1		COVER,PWR SPLY:12V	80009	200-2157-00
						(ATTACHING PARTS)		
-47	211-0511-00			3		SCREW,MACHINE:6-32 X 0.50 INCH,PNH STL	83385	OBD
-48	211-0510-00			3		SCREW,MACHINE:6-32 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-49	260-0987-00			1		SWITCH,SLIDE:4PDT,0.5A,125VAC	82389	47227LF
						(ATTACHING PARTS)		
-50	211-0012-00			2		SCREW,MACHINE:4-40 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-51	119-0420-00			1		FILTER,RFI:6A,250VAC,400HZ	02777	F-11935-6
						(ATTACHING PARTS)		
-52	210-0586-00			2		NUT,PLAIN,EXT W:4-40 X 0.25 INCH,STL	78189	211-041800-00
-53	211-0012-00			2		SCREW,MACHINE:4-40 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-54	118-0405-00			4		FUSEHOLDER:	80009	118-0405-00
-55	210-0457-00			2		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
-56	211-0513-00			2		SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	OBD
-57	333-2357-00			1		PANEL,REAR:BLANK	80009	333-2357-00
						(ATTACHING PARTS)		
-58	210-0586-00			4		NUT,PLAIN,EXT W:4-40 X 0.25 INCH,STL	78189	211-041800-00
						- - - * - - -		
-59	386-3808-00			1		PL,REAR PNL MTG:	80009	386-3808-00
						(ATTACHING PARTS)		
-60	211-0012-00			4		SCREW,MACHINE:4-40 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-61	200-2222-00			2		GUARD,FAN:	80009	200-2222-00
						(ATTACHING PARTS FOR EACH)		
-62	210-0457-00			4		NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
-63	211-0513-00			4		SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	OBD
						- - - * - - -		
-64	----- -----			2		FAN,VENTILATING:(SEE B1 AND B2 EPL)		
-65	252-0571-00			2		NEOPRENE EXTR:CHAN,0.234 X 0.156	77969	1353
-66	333-2342-00			1		PANEL,REAR:	80009	333-2342-00
						(ATTACHING PARTS)		
-67	212-0137-00			4		SCREW MACHINE:8-32 X 0.375 L,PNH,STEEL	83385	OBD
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1 -68	118-0204-00			1		POWER SPLY ASSY:CPU	000CR	90019061
	----- -----			-		HCC15-3		
	118-0439-00			1		. CHAS,PWR SUPPLY:ALUMINUM		
	343-0149-00			2		. CLAMP,LOOP:NYLON	80009	343-0149-00
	407-2010-00			1		. BRACKET,ANGLE:POWER SUPPLY,ALUMINUM	80009	407-2010-00
	407-2012-00			1		. BRACKET,ANGLE:POWER SUPPLY,ALUMINUM	80009	407-2012-00
	210-0458-00			2		. NUT,PLAIN,EXT W:8-32 X 0.344 INCH,STL	83385	OBD
	211-0578-00			6		. SCREW,MACHINE:6-32 X 0.438 INCH,PNH STL	83385	OBD
	212-0023-00			2		. SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
	212-0043-00			2		. SCREW,MACHINE:8-32 X 0.500 INCH,FLH STL	83385	OBD
	220-0410-00			4		. NUT,EXTENDED WA:10-32 X 0.375 INCH,STL	83385	OBD
	----- -----			-		F5-25		
	118-0440-00			1		. CHAS,PWR SUPPLY:ALUMINUM		
	255-0689-00			FT		. PLASTIC CHANNEL:0.094 W X 3.25 L		
	343-0149-00			1		. CLAMP,LOOP:NYLON	80009	343-0149-00
	343-0775-00			1		. CLIP,SPR TNSN:	76381	3484-1000
	384-0647-00			2		. POST,ELEC-MECH:0.312 X 1.344 INCH LONG,AL	80009	384-0647-00
	386-0978-00			8		. INSULATOR,PLATE:0.002 INCH MICA,FOR TO-3	80009	386-0978-00
	407-2024-00			1		. BRACKET,ANGLE:INTERLOCK SWITCH	80009	407-2024-00
	214-2952-00			4		. HEAT SINK,ELEC:POWER SUPPLY		
	118-0508-00			2		. RETAINER,CAP:		
	210-0457-00			14		. NUT,PLAIN,EXT W:6-32 X 0.312 INCH,STL	83385	OBD
	211-0559-00			4		. SCREW,MACHINE:6-32 X 0.375"100 DEG,FLH STL	83385	OBD
	211-0579-00			18		. SCREW,MACHINE:6-32 X 0.312,PNH,STL,BK OXD		
	220-0410-00			4		. NUT,EXTENDED WA:10-32 X 0.375 INCH,STL	83385	OBD

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-1	----- -----			1		CKT BOARD ASSY:SYSTEM COMM(SEE A30 EPL)		
-2	136-0578-00			3		. SOCKET,PLUG-IN:24 DIP,LOW PROFILE	01295	C952402
-3	131-0993-00			7		. LINK,TERM.CONNE:2 WIRE BLACK	00779	530153-2
-4	131-0608-00			6		. TERMINAL,PIN:0.365 L X 0.25 PH,BRZ,GOLD PL	22526	47357
-5	214-1337-00			2		. PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-6	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-7	----- -----			1		CKT BOARD ASSY:PRGM MEM(SEE A20A1 EPL)		
-8	118-0317-00			11		. TERMINAL,PIN:	80009	118-0317-00
-9	136-0578-00			1		. SOCKET,PLUG-IN:24 DIP,LOW PROFILE	01295	C952402
-10	214-1337-00			2		. PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-11	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-12	----- -----			1		CKT BOARD ASSY:SYSTEM PROCESSOR(SEE A1 EPL)		
-13	136-0623-00			1		. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	C954002
-14	118-0317-00			6		. TERMINAL,PIN:	80009	118-0317-00
-15	214-1337-00			2		. PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-16	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-17	----- -----			1		CKT BD ASSY:DEBUG AND FR PNL I/O(SEE A5 EPL)		
-18	118-0317-00			6		. TERMINAL,PIN:	80009	118-0317-00
-19	214-1337-00			2		. PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-20	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-21	----- -----			1		CKT BD ASSY:ASSEMBLER PROCESSOR(SEE A10 EPL)		
-22	136-0623-00			1		. SOCKET,PLUG-IN:40 DIP,LOW PROFILE	73803	C954002
-23	131-1425-00			13		. CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
-24	214-1337-00			2		. PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-25	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-26	----- -----			1		CKT BD ASSY:8002 SYSTEM MEM(SEE A20A2 EPL)		
-27	118-0317-00			11		. TERMINAL,PIN:	80009	118-0317-00
-28	136-0578-00			1		. SOCKET,PLUG-IN:24 DIP,LOW PROFILE	01295	C952402
-29	214-1337-00			2		. PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-30	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	80009	105-0792-00
-31	----- -----			1		CKT BOARD ASSY:MOTHER BOARD(SEE A35 EPL)		
						(ATTACHING PARTS)		
-32	211-0510-00			10		SCREW,MACHINE:6-32 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
	----- -----			-		. CKT BOARD ASSY INCLUDES:		
	131-1693-00			9		. . CONTACT,ELEC:CONN,MALE,BRSTIN PL	27264	02-09-2133
	131-1694-00			3		. . CONTACT,ELEC:CONN,FEMALE,BRS TIN PL	27264	02-09-1133
	204-0839-00			1		. CONN BODY,PLUG:3 CONT,WO/MTG EARS OR TABS	80009	204-0389-00
	204-0838-00			1		. CONN BODY,PLUG:9 CONT,W/MTG EARS	80009	204-0838-00
	124-0365-00			1		. TERMINAL BOARD:10 CONTACT PLASTIC	80009	124-0365-00
-33	131-2240-00			20		. CONN,RCPT,ELEC:CKT BD,50/100CONT	05574	3VH50/1CV5
-34	351-0575-00			40		GUIDE,CKT BD:PLASTIC	80009	351-0575-00
-35	381-0401-00			3		BAR,CKT BD GUID:ALUMINUM	80009	381-0401-00
						(ATTACHING PARTS FOR EACH)		
-36	211-0511-00			5		SCREW,MACHINE:6-32 X 0.50 INCH,PNH STL	83385	OBD
-37	211-0504-00			2		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-38	343-0776-00			60		RETAINER,GUIDE:PLASTIC	23880	3000
-39	381-0401-00			1		BAR,CKT BD GUID:ALUMINUM	80009	381-0401-00
						(ATTACHING PARTS)		
-40	211-0511-00			2		SCREW,MACHINE:6-32 X 0.50 INCH,PNH STL	83385	OBD
-41	211-0513-00			2		SCREW,MACHINE:6-32 X 0.625 INCH,PNH STL	83385	OBD
-42	211-0504-00			2		SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-43	343-0776-00			20		RETAINER,GUIDE:PLASTIC	23880	3000
-44	361-0945-00			2		SPACER,CHASSIS:0.25 SQ,0.1562 THK,AL	80009	361-0945-00
-45	343-0775-00			13		CLIP,SPR TNSN:	76381	3484-1000
-46	386-3794-00			1		PLATE,CONT:LEFT	80009	386-3794-00
						(ATTACHING PARTS)		
-47	211-0510-00			2		SCREW,MACHINE:6-32 X 0.375 INCH,PNH STL	83385	OBD
-48	212-0023-00			4		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-49	386-3795-00			1		PLATE,CONT:RIGHT	80009	386-3795-00
						(ATTACHING PARTS)		
-50	211-0510-00			2		SCREW,MACHINE:6-32 X 0.375 INCH,PNH STL	83385	OBD
-51	212-0023-00			4		SCREW,MACHINE:8-32 X 0.375 INCH,PNH STL	83385	OBD
						- - - * - - -		
-52	386-3798-00			1		STIF,CKT BD CG:	80009	386-3798-00
-53	441-1396-00			1		CHAS.CONTROLLER:MOTHER BOARD	80009	441-1396-00
-54	175-2112-02			1		CA ASSY,SP,ELEC:16,28 AWG,3.0L	80009	175-2112-02
-55	175-2116-00			1		CA ASSY,SP,ELEC:26,28 AWG,19.0 L	80009	175-2116-00
	175-2115-00			1		CA ASSY,SP,ELEC:26,28 AWG,18.0 L	80009	175-2115-00
-56	012-0764-00			1		CABLE,INTCON:22.0 L	000CR	90014011
	012-0764-01			1		CABLE,INTCON:22.0 L	000CR	90014011
	012-0764-02			1		CABLE,INTCON:22.0 L	000CR	90014011
	012-0764-03			1		CABLE,INTCON:22.0 L	000CR	90014011

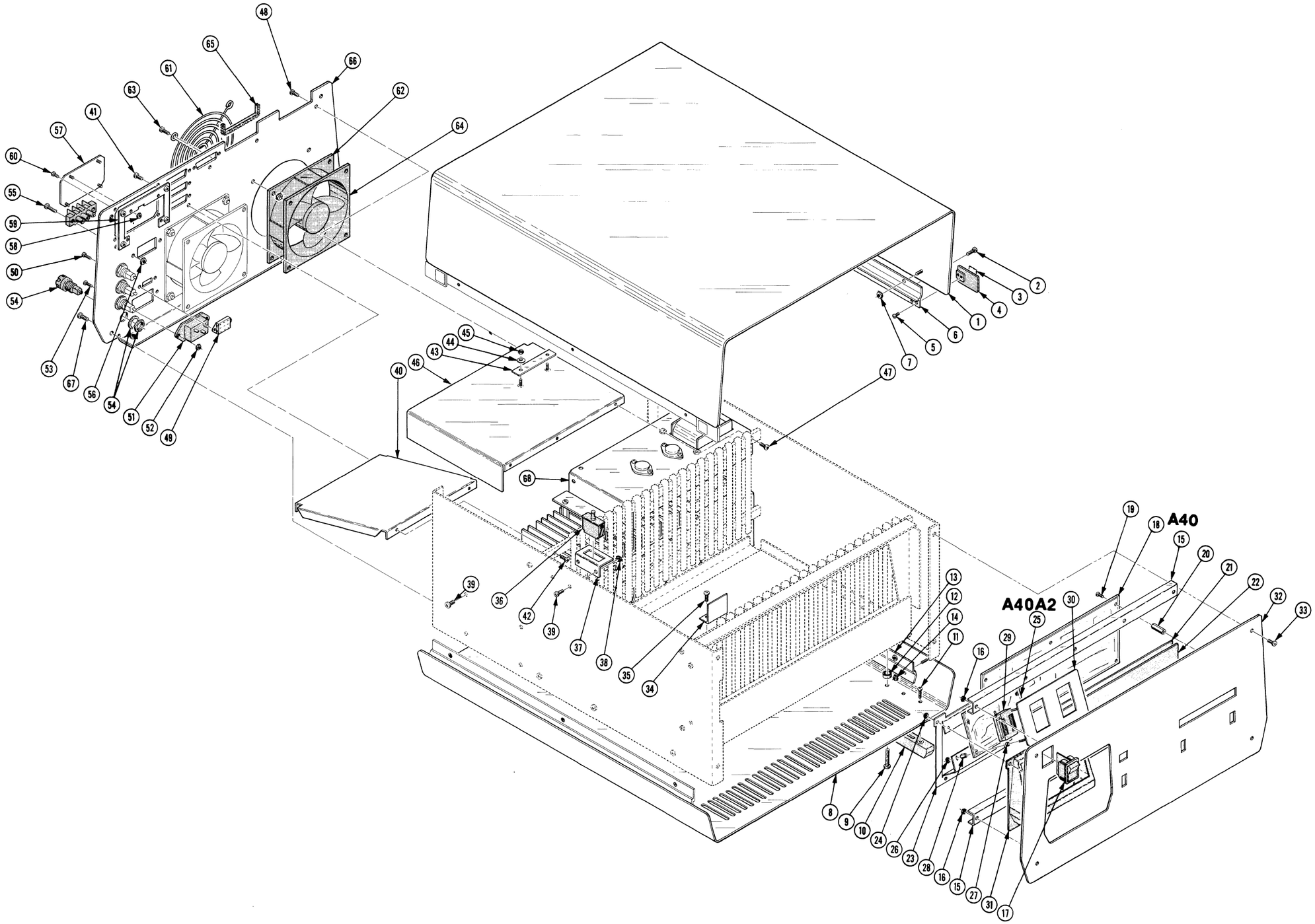
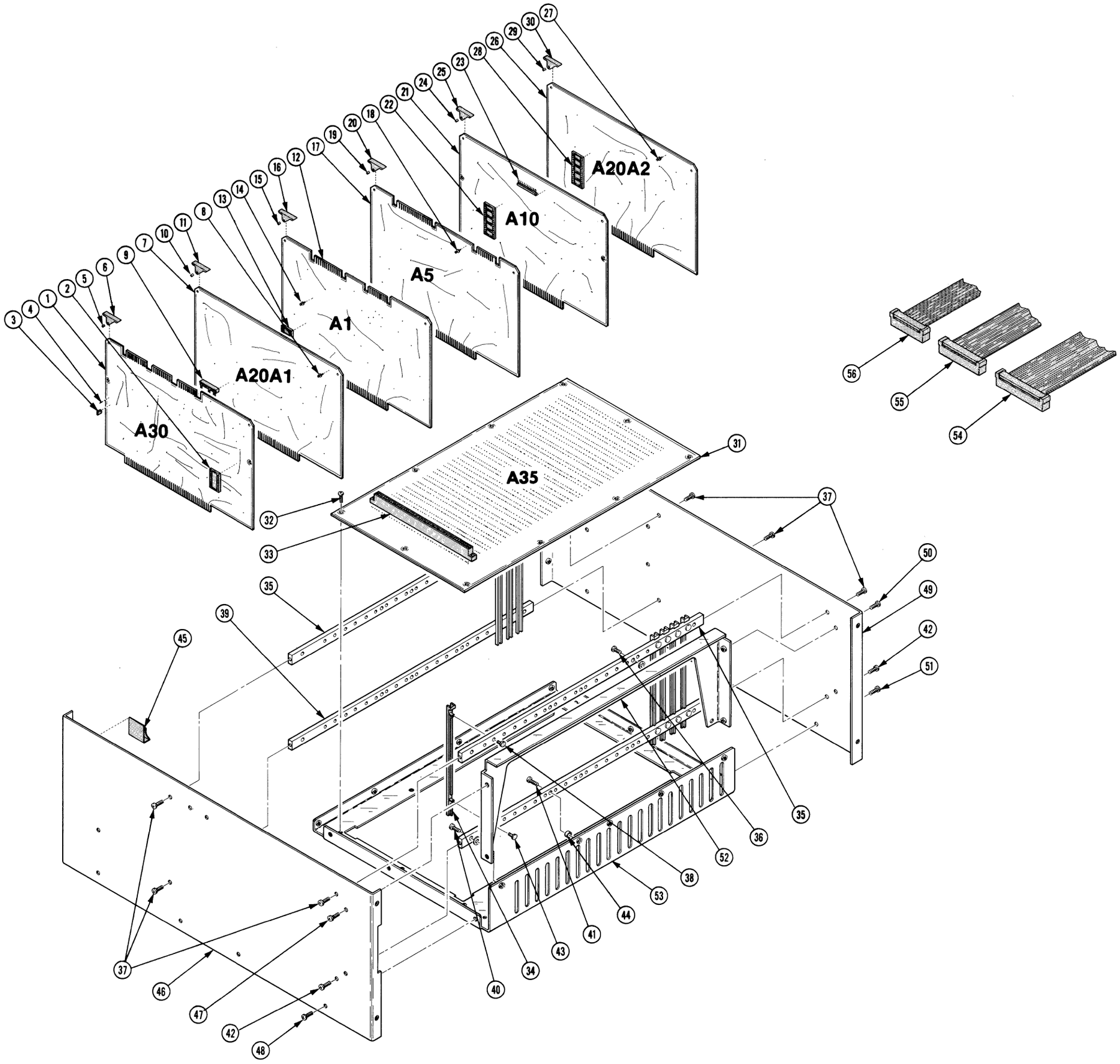
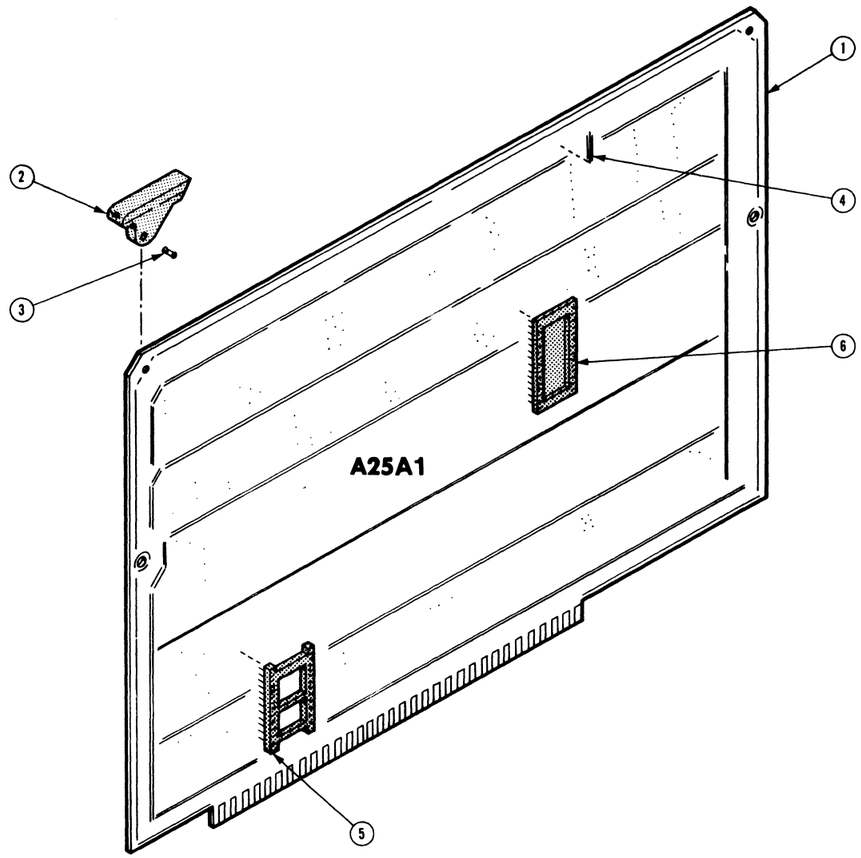

A40
A40A2

FIG. 2 CARD CARRIAGE & CIRCUIT BOARDS





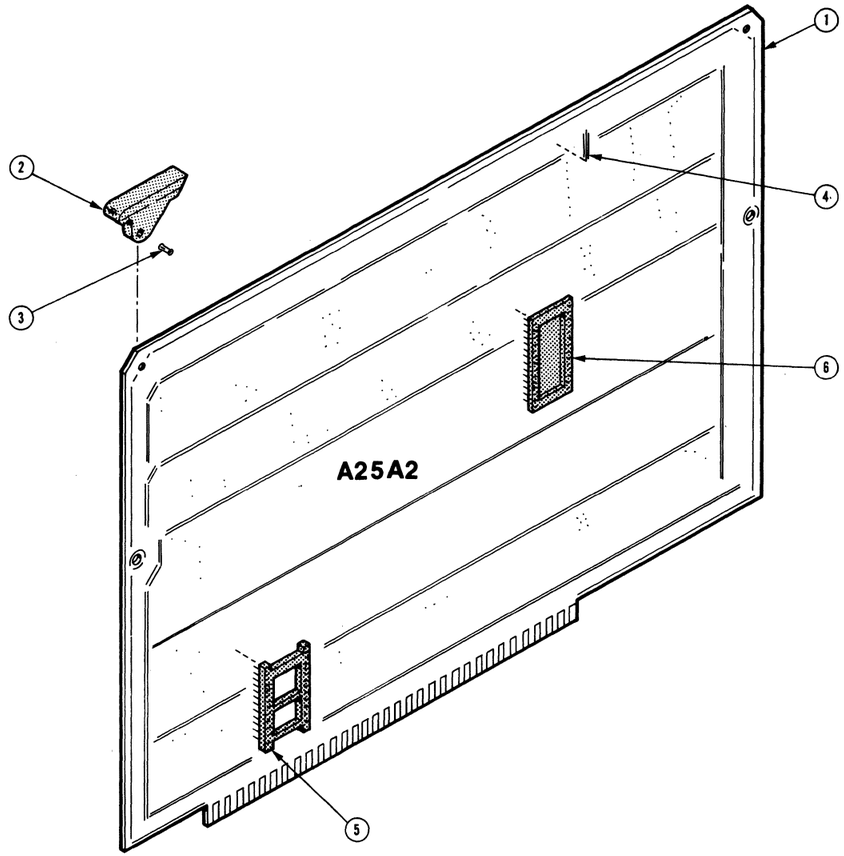
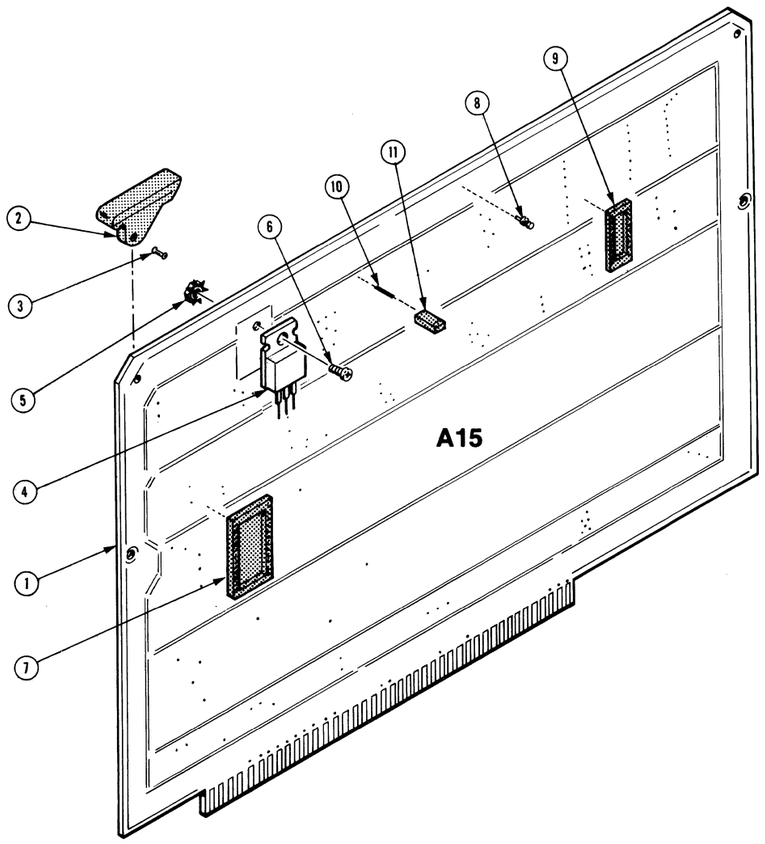


FIG. 3 HIGH SPEED SYS. & HIGH SPEED PROG. MEMORY

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-1	----- -----			1		CKT BOARD ASSY:HIGH SP PRGM MEM(SEE A25A1 EPL)		
-2	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	23880	6100
-3	214-1337-00			2		. PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-4	131-1425-00			11		. CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
-5	136-0578-00			1		. SOCKET,PLUG-IN:24 DIP,LOW PROFILE	01295	C952402
-6	136-0597-00			1		. SOCKET,PLUG-IN:28 CONTACT	71279	703-3783-01-0416

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-1	----- -----			1		CKT BOARD ASSY:HIGH SPEED SYS MEM(SEE A25A2 EPL)		
-2	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	23880	6100
-3	214-1337-00			2		. PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-4	131-1425-00			11		. CONTACT SET,ELE:R ANGLE,0.150" L,STR OF 36	22526	65521-136
-5	136-0578-00			1		. SOCKET,PLUG-IN:24 DIP,LOW PROFILE	01295	C952402
-6	136-0597-00			1		. SOCKET,PLUG-IN:28 CONTACT	71279	703-3783-01-0416

FIG. 4 SYSTEM MEMORY & ACCESSORIES



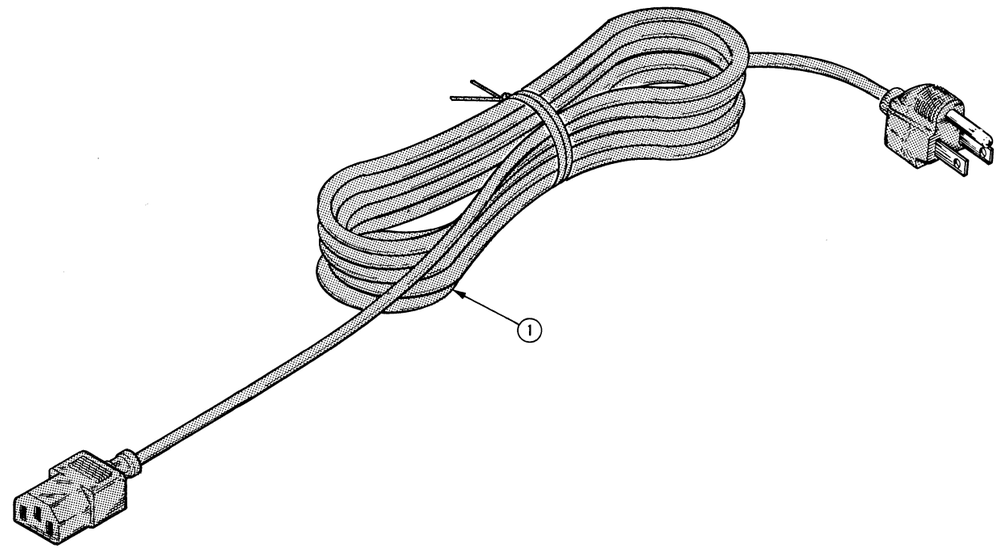


Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
4-1	----- -----			1		CKT BOARD ASSY:SYSTEM MEMORY(SEE A15 EPL)		
-2	105-0792-00			2		. EJECTOR,CKT BD:PLASTIC	23880	6100
-3	214-1337-00			2		. PIN,SPRING:0.10 OD X 0.25 INCH L,STL	80009	214-1337-00
-4	----- -----			1		. MICROCIRCUIT,LI:VOLTAGE RGTR(SEE Q1030 EPL)		
						(ATTACHING PARTS)		
-5	210-0586-00			1		. NUT,PLAIN,EXT W:4-40 X 0.25 INCH,STL	78189	211-041800-00
-6	211-0008-00			1		. SCREW,MACHINE:4-40 X 0.25 INCH,PNH STL	83385	OBD
						- - - * - - -		
-7	136-0578-00			22		. SOCKET,PLUG-IN:24 DIP,LOW PROFILE	01295	C952402
-8	118-0317-00			11		. TERMINAL PIN:	80009	118-0317-00
-9	136-0670-00			4		. SKT,PL-IN ELEK:MICROCKT,18 PIN,LOW PROFILE	82647	C951802
-10	131-1343-00			8		. TERM SET,PIN:36-0.525 L X 0.025 SQ	22526	65501-136
-11	131-0993-00			2		. LINK,TERM.CONNE:2 WIRE BLACK	00779	530153-2

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
4-						STANDARD ACCESSORIES		
1-	070-2312-01			1		MANUAL,TECH:INSTRUCTION	80009	070-2312-01
1-	161-0066-00			1		CABLE ASSY,PWR,:3 WIRE,98 INCH LONG	80009	161-0066-00

Appendix A

BUS ASSIGNMENTS

8001/8002A μProcessor Lab Motherboard Bus

Pin #	Mnemonic	Description
1—4	+5 Vdc	Primary TTL power supply.
5—8	AUX BUS	Undesignated power bus lines.
9—10	GND	Common ground with bus pins 15—16 and 97—100.
11—12	+12 Vdc	+12 volt power supply.
13—14	−12 Vdc	−12 volt power supply.
15—16	GND	Common ground with pins 9—10 and 97—100.
17	A0	Least significant bus address line.
18	A1	Bus address line.
19	A2	Bus address line.
20	A3	Bus address line.
21	A4	Bus address line.
22	A5	Bus address line.
23	A6	Bus address line.
24	A7	Bus address line.
25	A8	Bus address line.
26	A9	Bus address line.
27	A10	Bus address line.
28	A11	Bus address line.
29	A12	Bus address line.
30	A13	Bus address line.
31	A14	Bus address line.
32	A15	Most significant bus address line.
33	CMEM	Bank switch command. When high, allows System Processor to address Program Memory.
34	RAM INH	Allows any module to override a RAM address and control data bus.

8001/8002A μProcessor Lab Motherboard Bus (cont)

Pin #	Mnemonic	Description
35	WD ACCESS	Enables data on 16 bits of the data bus when used in conjunction with a 16-bit emulator.
36	D0	Least significant data bus line.
37	D1	Data bus line.
38	D2	Data bus line.
39	D3	Data bus line.
40	D4	Data bus line.
41	D5	Data bus line.
42	D6	Data bus line.
43	D7	Data bus line.
44	D8	Data bus line.
45	D9	Data bus line.
46	D10	Data bus line.
47	D11	Data bus line.
48	D12	Data bus line.
49	D13	Data bus line.
50	D14	Data bus line.
51	D15	Most significant data bus line.
52	M/IO	Indicates whether the active emulator is addressing memory (low) or I/O (high).
53	WRP	Indicates that data on the data bus is valid for a write command.
54	OPREQ	Indicates when a bus operation is in progress.
55	R/W	Read/Write control line. Signifies a Read or Write operation to memory and I/O.
56	HOLD	HOLD request to active emulator. Used by memory and I/O.
57	JMP CMD	Issued by the Debug and Front Panel I/O module to initiate a forced emulator processor jump.
58	RUN	Indicates that the active emulator processor module is in the RUN state.
59	RESET	Initializes all μProcessor Lab logic. RESET indicates both power-on reset and Front Panel reset.

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8001/8002A μProcessor Lab Motherboard Bus (cont)

Pin #	Mnemonic	Description
60	JMP ACK	A response from the emulator processor to the Debug and Front Panel I/O module to enable a jump address onto the system address bus.
61	INTACK	Issued by the System Processor in response to an interrupt request.

At this point, the μProcessor Lab bus is divided into two halves: system and program. The mnemonic for the system side is given for each pin with the mnemonic for the program side directly below in parentheses. The description of the program side will also be given in parentheses.

62	INT 0	Interrupt Level 0
	(Forced Int)	(Forced Interrupt from the Debug and Front Panel I/O module to the emulator processor.)
63	MST INT 1	Interrupt Level 1
	(Not Used)	(Not used on the program side.)
64	INT 2	Interrupt Level 2
	(Not Used)	(Not used on the program side.)
65	INT 3	Interrupt Level 3
	(Not Used)	(Not used on the program side.)
66	INT 4	Interrupt Level 4
	(Not Used)	(Not used on the program side.)
67	INT 5	Interrupt Level 5
	(Not Used)	(Not used on the program side.)
68	INT 6	Interrupt Level 6
	(Not Used)	(Not used on the program side.)

8001/8002A μProcessor Lab Motherboard Bus (cont)

Pin #	Mnemonic	Description
69	INT 7	Interrupt Level 7
	(Not Used)	(Not used on the program side.)
70	INT 8	Interrupt Level 8
	(Not Used)	(Not used on the program side.)
71	INT 29	Interrupt Level 29
	(Debug Int)	(Debug interrupt produced by the RTPA.)
72	INT 30	Interrupt Level 30
	(Debug Int)	(Debug interrupt produced by the RTPA.
73	INT 31	Interrupt Level 31
	(Debug Int)	(Not Used)
74	INT 12	Interrupt Level 12
	(UPAUSE)	(Generated by the emulator processor module.)
75	INT 13	Interrupt Level 13
	(SLV OPREQ)	(Used by the Debug and Front Panel I/O module and the RTPA.)
76	INT 14	Interrupt Level 14
	(SLV RST)	(Used by the Debug and Front Panel I/O module to reset the emulator processor.)
77	INT 15	Interrupt Level 15
	(SLV PAUSE)	(Issued by the Debug and Front Panel I/O module to the emulator processor.)

8001/8002A μProcessor Lab Motherboard Bus (cont)

Pin #	Mnemonic	Description
78	MST PSE	Indicates the System Processor is paused with its data, control, and address lines tri-stated.
	(RFSH NW)	(Issued by the emulator processor module to refresh Program Memory.)
79	DBG INT	Line from the Debug and Front Panel I/O module to the System Processor module to request an interrupt.
	(SLV INOP)	(Issued by the RTPA to reset active lines on the emulator processor.)
80	DBG VEN	Debug Vector Enable from the System Processor acknowledging the Debug interrupt and enabling the Debug interrupt vector.
	(SWAP)	(Used only by the 9900 Emulator Processor to swap addresses in Program Memory.)
81	MST INTD	Master Interrupted line from the System Processor to Debug and Front Panle I/O module. This line causes the emulator processor to be paused and the System Processor to run.
	(Spare)	(Spare line on the program side.)
82	FETCH	FETCH line from the active emulator processor, signifying an instruction fetch.
83	PAUSE	Causes all processors to go to an inactive state with control, address, and data lines tri-stated.
84	MAST RUN	Indicates that the System Processor is running.
85	SENSE	Not used in the 8001/8002A μProcessor Labs.
86	FLAG	Not used in the 8001/8002A μProcessor Labs.
87	F.P. HOLD	Front Panel Hold request to System Processor, indicating a breakpoint or single-step operation.
88	MST INTACK	Master Interrupt Acknowledge.

8001/8002A μProcessor Lab Motherboard Bus (cont)

Pin #	Mnemonic	Description
89	MST INT 3	Master Interrupt 3.
90	Spare	Spare on the system side.
	(UMAP)	(Issued by the System Communications module, indicating prototype memory mapping.)
91	Spare	
92	Spare	
93	SLV CLK	Clock output from the active emulator processor.
94	I/O CLK	38.4 kHz clock from the System Processor.
95	2650 CLK	10 MHz clock from the System Processor.
96	SYS CLK	10 MHz clock from the System Processor.
97	GND	Ground.
98	GND	Ground.
99	GND	Ground.
100	GND	Ground.

Appendix B

DECIMAL-HEXADECIMAL-BINARY EQUIVALENTS 0—255$_{10}$

Deci-mal	Hexa-deci-mal	Binary 8-bit Code	Deci-mal	Hexa-deci-mal	Binary 8-bit Code	Deci-mal	Hexa-deci-mal	Binary 8-bit Code	Deci-mal	Hexa-deci-mal	Binary 8-bit Code
0	00	0000 0000	64	40	0100 0000	128	80	1000 0000	192	C0	1100 0000
1	01	0000 0001	65	41	0100 0001	129	81	1000 0001	193	C1	1100 0001
2	02	0000 0010	66	42	0100 0010	130	82	1000 0010	194	C2	1100 0010
3	03	0000 0011	67	43	0100 0011	131	83	1000 0011	195	C3	1100 0011
4	04	0000 0100	68	44	0100 0100	132	84	1000 0100	196	C4	1100 0100
5	05	0000 0101	69	45	0100 0101	133	85	1000 0101	197	C5	1100 0101
6	06	0000 0110	70	46	0100 0110	134	86	1000 0110	198	C6	1100 0110
7	07	0000 0111	71	47	0100 0111	135	87	1000 0111	199	C7	1100 0111
8	08	0000 1000	72	48	0100 1000	136	88	1000 1000	200	C8	1100 1000
9	09	0000 1001	73	49	0100 1001	137	89	1000 1001	201	C9	1100 1001
10	0A	0000 1010	74	4A	0100 1010	138	8A	1000 1010	202	CA	1100 1010
11	0B	0000 1011	75	4B	0100 1011	139	8B	1000 1011	203	CB	1100 1011
12	0C	0000 1100	76	4C	0100 1100	140	8C	1000 1100	204	CC	1100 1100
13	0D	0000 1101	77	4D	0100 1101	141	8D	1000 1101	205	CD	1100 1101
14	0E	0000 1110	78	4E	0100 1110	142	8E	1000 1110	206	CE	1100 1110
15	0F	0000 1111	79	4F	0100 1111	143	8F	1000 1111	207	CF	1100 1111
16	10	0001 0000	80	50	0101 0000	144	90	1001 0000	208	D0	1101 0000
17	11	0001 0001	81	51	0101 0001	145	91	1001 0001	209	D1	1101 0001
18	12	0001 0010	82	52	0101 0010	146	92	1001 0010	210	D2	1101 0010
19	13	0001 0011	83	53	0101 0011	147	93	1001 0011	211	D3	1101 0011
20	14	0001 0100	84	54	0101 0100	148	94	1001 0100	212	D4	1101 0100
21	15	0001 0101	85	55	0101 0101	149	95	1001 0101	213	D5	1101 0101
22	16	0001 0110	86	56	0101 0110	150	96	1001 0110	214	D6	1101 0110
23	17	0001 0111	87	57	0101 0111	151	97	1001 0111	215	D7	1101 0111
24	18	0001 1000	88	58	0101 1000	152	98	1001 1000	216	D8	1101 1000
25	19	0001 1001	89	59	0101 1001	153	99	1001 1001	217	D9	1101 1001
26	1A	0001 1010	90	5A	0101 1010	154	9A	1001 1010	218	DA	1101 1010
27	1B	0001 1011	91	5B	0101 1011	155	9B	1001 1011	219	DB	1101 1011
28	1C	0001 1100	92	5C	0101 1100	156	9C	1001 1100	220	DC	1101 1100
29	1D	0001 1101	93	5D	0101 1101	157	9D	1001 1101	221	DD	1101 1101
30	1E	0001 1110	94	5E	0101 1110	158	9E	1001 1110	222	DE	1101 1110
31	1F	0001 1111	95	5F	0101 1111	159	9F	1001 1111	223	DF	1101 1111
32	20	0010 0000	96	60	0110 0000	160	A0	1010 0000	224	E0	1110 0000
33	21	0010 0001	97	61	0110 0001	161	A1	1010 0001	225	E1	1110 0001
34	22	0010 0010	98	62	0110 0010	162	A2	1010 0010	226	E2	1110 0010
35	23	0010 0011	99	63	0110 0011	163	A3	1010 0011	227	E3	1110 0011
36	24	0010 0100	100	64	0110 0100	164	A4	1010 0100	228	E4	1110 0100
37	25	0010 0101	101	65	0110 0101	165	A5	1010 0101	229	E5	1110 0101
38	26	0010 0110	102	66	0110 0110	166	A6	1010 0110	230	E6	1110 0110
39	27	0010 0111	103	67	0110 0111	167	A7	1010 0111	231	E7	1110 0111
40	28	0010 1000	104	68	0110 1000	168	A8	1010 1000	232	E8	1110 1000
41	29	0010 1001	105	69	0110 1001	169	A9	1010 1001	233	E9	1110 1001
42	2A	0010 1010	106	6A	0110 1010	170	AA	1010 1010	234	EA	1110 1010
43	2B	0010 1011	107	6B	0110 1011	171	AB	1010 1011	235	EB	1110 1011
44	2C	0010 1100	108	6C	0110 1100	172	AC	1010 1100	236	EC	1110 1100
45	2D	0010 1101	109	6D	0110 1101	173	AD	1010 1101	237	ED	1110 1101
46	2E	0010 1110	110	6E	0110 1110	174	AE	1010 1110	238	EE	1110 1110
47	2F	0010 1111	111	6F	0110 1111	175	AF	1010 1111	239	EF	1110 1111
48	30	0011 0000	112	70	0111 0000	176	B0	1011 0000	240	F0	1111 0000
49	31	0011 0001	113	71	0111 0001	177	B1	1011 0001	241	F1	1111 0001
50	32	0011 0010	114	72	0111 0010	178	B2	1011 0010	242	F2	1111 0010
51	33	0011 0011	115	73	0111 0011	179	B3	1011 0011	243	F3	1111 0011
52	34	0011 0100	116	74	0111 0100	180	B4	1011 0100	244	F4	1111 0100
53	35	0011 0101	117	75	0111 0101	181	B5	1011 0101	245	F5	1111 0101
54	36	0011 0110	118	76	0111 0110	182	B6	1011 0110	246	F6	1111 0110
55	37	0011 0111	119	77	0111 0111	183	B7	1011 0111	247	F7	1111 0111
56	38	0011 1000	120	78	0111 1000	184	B8	1011 1000	248	F8	1111 1000
57	39	0011 1001	121	79	0111 1001	185	B9	1011 1001	249	F9	1111 1001
58	3A	0011 1010	122	7A	0111 1010	186	BA	1011 1010	250	FA	1111 1010
59	3B	0011 1011	123	7B	0111 1011	187	BB	1011 1011	251	FB	1111 1011
60	3C	0011 1100	124	7C	0111 1100	188	BC	1011 1100	252	FC	1111 1100
61	3D	0011 1101	125	7D	0111 1101	189	BD	1011 1101	253	FD	1111 1101
62	3E	0011 1110	126	7E	0111 1110	190	BE	1011 1110	254	FE	1111 1110
63	3F	0011 1111	127	7F	0111 1111	191	BF	1011 1111	255	FF	1111 1111

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Appendix C

INTERRUPT VECTORS

Priority	Vector Address	Function
0	0000	Reset
1	0002	System Memory Parity Error
2	0004	NA
3	0006	Program Memory Parity Error
4	0008	Console In
5	000A	Console Out
6	000C	System Communications 1
7	000E	System Communications 2
8	0010	System Communications 3
9	0012	Timer
10	0014	NA
11	0016	Flexible Disc
12	0018	NA
13	001A	PROM Programmer 1
14	001C	PROM Programmer 2
15	001E	NA
16	0020	Emulator SVC 1
17	0022	Emulator SVC 2
18	0024	Emulator SVC 3
19	0026	Emulator SVC 4
20	0028	Emulator SVC 5
21	002A	Emulator SVC 6
22	002C	Emulator SVC 7
23	002E	Emulator SVC 8
24	0030	Breakpoint 1
25	0032	Breakpoint 2
26	0034	Single Cycle
27	0036	Emulator Halted
28	0038	Diagnostic Interrupt
29	003A	Real-Time Prototype Analyzer (RTPA)
30	003C	Debug Interrupt 30
31	003E	Debug Interrupt 31

NA = Not Assigned

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Appendix D

MODULE TEST POINTS

System Processor

TP1	HOLD	U3090-4
TP2	PAUSE	U4170-8
TP3	INTACK	U3040-10
TP4	RUN	U3040-8
TP5		U5140-1, 9, 10, 15
TP6	+5.2 V	U5140-11

16K Dynamic RAM

TP1	WE	U1130-2
TP2	PARITY INT	U2110-9
TP3	RD STR	U2140-10
TP4	CE	U2150-6
TP5		U1160-3
TP6	HOLD	U2150-7
TP7	PROM ACCESS	U3170-6
TP8	REF REQ	U3160-6
TP9	REF OP	U2170-5
TP10	MOD ADDR	U5150-3, 8, 11; U5170-4, 6, 8
TP11	GND	

Systems Communications Module

No test points.

Debug and Front Panel I/O

TP1	SPRTEN	U1160-3
TP2		U5100-6
TP3	OPREQ	U5080-5
TP4	BP1 (Breakpoint 1)	U4100-3
TP5	BP2 (Breakpoint 2)	U4100-6
TP6	GND	

8001 System Memory

TP1	PATCH ROM	U2010-8
TP2	BK SW ROM	U1020-12
TP3	2K RAM	U2120-13
TP4	HOLD	U2030-3
TP5	6K ROM	U2030-11
TP6		U4020-20
TP 7	INT 1	U1040-7
TP8	R/W	U5110-8
TP9	WRP	U1060-11
TP10	BD SEL	U5090-4

High-Speed Memory

TP1	GND	
TP2	RAS1	U3170-9
TP3	RAS2	U3160-5
TP4	CAS1	U3120-6
TP5	LATCH	U4170-6
TP6	SELECT	U4150-6
TP7	REF OP	U3160-9
TP8	REF CLK	U5150-4
TP9	OPREQ	U7170-12
TP10	WRT EN	U7180-6
TP11	HOLD	U3180-10

Assembler Processor

TP1	GND	
TP2	Z80 RUN	U4100-8
TP3	UPE7	U3030-9
TP4	Z80 RESET	U4080-10
TP5		U4090-6
TP6	FETCH	U5080-6
TP7	RUN	U5060-9
TP8	Z80 OPREQ	U3080-8
TP9	ACTIVE	U5090-9
TP10	WAIT	U3100-6
TP11	FP HOLD	U5100-4
TP12	BUS RQ	U3100-10
TP13	SLV PAUSE	U5100-8

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

SERVICE NOTE

Because of the universal parts procurement problem, some electrical parts in your instrument may be different from those described in the Replaceable Electrical Parts List. The parts used will in no way alter or compromise the performance or reliability of this instrument. They are installed when necessary to ensure prompt delivery to the customer. Order replacement parts from the Replaceable Electrical Parts List.

CALIBRATION TEST EQUIPMENT REPLACEMENT

Calibration Test Equipment Chart

This chart compares TM 500 product performance to that of older Tektronix equipment. Only those characteristics where significant specification differences occur, are listed. In some cases the new instrument may not be a total functional replacement. Additional support instrumentation may be needed or a change in calibration procedure may be necessary.

Comparison of Main Characteristics

DM 501 replaces 7D13		
PG 501 replaces 107	PG 501 - Risetime less than 3.5 ns into 50 Ω.	107 - Risetime less than 3.0 ns into 50 Ω.
108	PG 501 - 5 V output pulse; 3.5 ns Risetime	108 - 10 V output pulse 1 ns Risetime
PG 502 replaces 107		
108	PG 502 - 5 V output	108 - 10 V output
111	PG 502 - Risetime less than 1 ns; 10 ns Pretrigger pulse delay	111 - Risetime 0.5 ns; 30 to 250 ns Pretrigger pulse delay
PG 508 replaces 114	Performance of replacement equipment is the same or better than equipment being replaced.	
115		
2101		
PG 506 replaces 106	PG 506 - Positive-going trigger output signal at least 1 V; High Amplitude output, 60 V.	106 - Positive and Negative-going trigger output signal, 50 ns and 1 V; High Amplitude output, 100 V.
067-0502-01	PG 506 - Does not have chopped feature.	0502-01 - Comparator output can be alternately chopped to a reference voltage.
SG 503 replaces 190, 190A, 190B	SG 503 - Amplitude range 5 mV to 5.5 V p-p.	190B - Amplitude range 40 mV to 10 V p-p.
191		
067-0532-01	SG 503 - Frequency range 250 kHz to 250 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
SG 504 replaces 067-0532-01	SG 504 - Frequency range 245 MHz to 1050 MHz.	0532-01 - Frequency range 65 MHz to 500 MHz.
067-0650-00		
TG 501 replaces 180, 180A	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	180A - Trigger pulses 1, 10, 100 Hz; 1, 10, and 100 kHz. Multiple time-marks can be generated simultaneously.
181		181 - Multiple time-marks
184	TG 501 - Trigger output-slaved to market output from 5 sec through 100 ns. One time-mark can be generated at a time.	184 - Separate trigger pulses of 1 and 0.1 sec; 10, 1, and 0.1 ms; 10 and 1 μs.
2901	TG 501 - Trigger output-slaved to marker output from 5 sec through 100 ns. One time-mark can be generated at a time.	2901 - Separate trigger pulses, from 5 sec to 0.1 μs. Multiple time-marks can be generated simultaneously.

NOTE: All TM 500 generator outputs are short-proof. All TM 500 plug-in instruments require TM 500-Series Power Module.

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MANUAL CHANGE INFORMATION

Change Reference: C1/279 Date: 2-20-79

Product: 8001/8002A µPROCESSOR LAB SERVICE 070-2711-00

CHANGE	DESCRIPTION

ADD the following note to these three pages:

1. Page 4-1, at bottom of page.
2. Page 8-1, at bottom of page.
3. Page 11-3, just before the General Troubleshooting checklist.

NOTE

Reliability is reduced if 8002A µProcessor Lab Program Memory modules are reconfigured for System Memory operation, or vice-versa.

Reliability will also be reduced with the 8001 or 8002A if Program Memory is made up of both High-Speed and 16K Dynamic RAM modules.