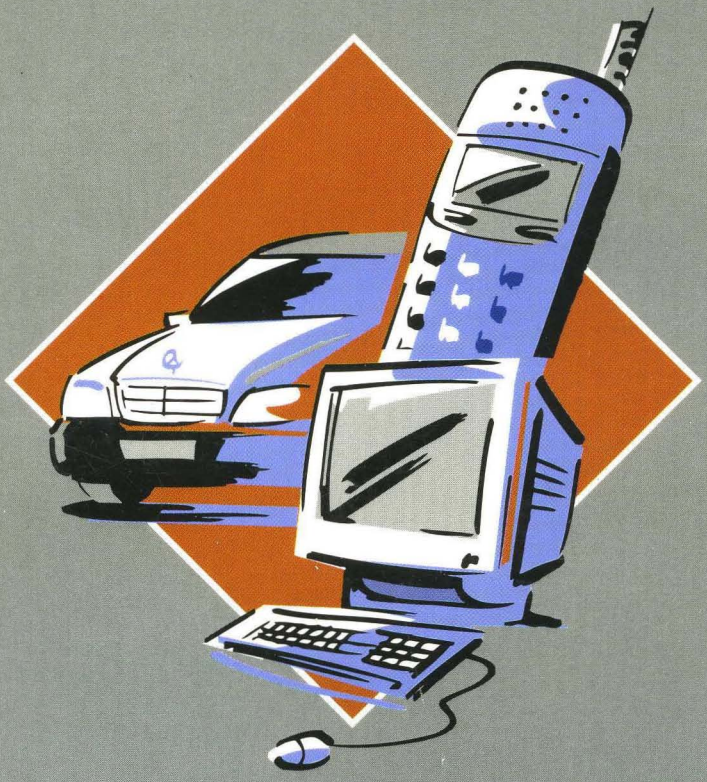
8-bit Microcontrollers

Databook - 1997



TEMIC

Semiconductors

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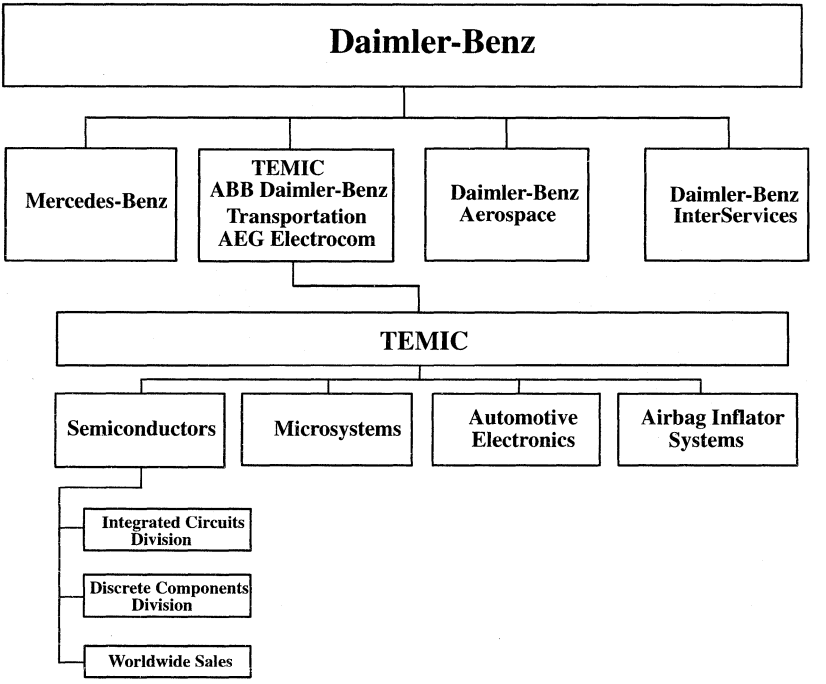
About TEMIC

TEMIC is the microelectronics enterprise of Daimler-Benz. Organized into four divisions – Semiconductors, Microsystems, Automotive Electronics, and Airbag Inflators – TEMIC offers products for the computer, communications, auto-motive, consumer, industrial as well as aerospace and defense markets. Sales are handled by the worldwide TEMIC network and by regional sales representatives and distributors.

With a technology portfolio which includes RF, bipolar, BiCMOS, GaAs, CMOS, BiC/DMOS, and DMOS processes, TEMIC Semiconductors provides a unique set of components and solutions. The company's facilities include wafer fabrication operations in Heilbronn and Itzehoe, Germany; Nantes, France; and Santa Clara, California in the United States. Assembly and test facilities are located in Vöcklabruck, Austria; Manila, Philippines; Kaohsiung, Taiwan; and Shanghai, China. The member companies of TEMIC Semiconductors are Telefunken Semiconductors, Siliconix, Matra MHS, and Dialog Semiconductor.



TEMIC Semiconductors Integrated Circuits Division

The IC Division of TEMIC Semiconductors, with its headquarters in Heilbronn, Germany, is organized into business centers that synergize the company's technical and marketing skills to provide the highest level of service to customers.

Automotive ICs

Based in Heilbronn, Germany, this business center is the European market leader for stand-alone control ICs dedicated to the harsh automotive environment. Offerings include embedded control ICs for airbag and anti-lock braking system (ABS) electronics, as well as RF and IR solutions for safety and convenience, such as keyless entry and immobilizer chip sets.

Communication ICs

Consisting of strong expert teams in the German cities of Heilbronn and Ulm, this business center is focused on high-frequency front-end solutions for handy phones and cordless phones, as well as analog and digital TV and radio receivers for worldwide markets. Current products are based on bipolar silicon high-speed technologies. Future products will also be based on a silicon germanium technology offering higher RF performance and lower power consumption, but at a cost very comparable to silicon.

Microcontrollers and Digital ICs

Located in Nantes, France, this business center's products are based on the powerful 80C51 and 80C251 cores licensed from Intel and comple-mented by a rich cell library, from E/E2PROM through a wide range of digital and mixed-signal functions and interfaces. Together, these provide a toolbox for the design of advanced embedded solutions for minimal system cost and maximum functionality. A line of high-performance SRAMs, digital ASICs and the Universal Logic Circuit (ULC) family of FPGA replacements completes this product offering. Hardened processes and fully certified quality flows enable to serve aerospace and defense applications.

Power ICs

Located in Santa Clara, California, in the heart of Silicon Valley, products from this business center combine low on-resistance power MOS transistors on a single chip with high-speed CMOS functions. The result is a range of product families such as high-frequency dc-to-dc converter ICs or highly integrated motor controller solutions which bothshare a unique combination of high power efficiency, low system cost, and small size.

Mixed-Signal ASICs

Succsessfully combining analog and digital functions on the same ASIC (Application-Specific-Integrated Circuit) is the key to true system integration. TEMIC Semiconductors' years of experience in mixed-signal ASIC technology gives our customers the ability to achieve the integrated solutions their systems need. Based in Swindon, United Kingdom, this business center supports all types of mixed-signal solutions in CMOS for a range of markets and applications, from the initial idea through to volume production.

TEMIC Semiconductors Discrete Components Division

The TEMIC Semiconductors Discrete Components Division combines TEMIC's expertise in power, IR data transmission, optoelectronic, analog signal processing, and bipolar technologies in a way that creates a clear focus on product lines and an efficient interface with target markets. With headquarters in Santa Clara, California, the Discrete Components Division includes product units focused on power MOSFETs, IrDA modules, optoelectronics, RF/bipolar transistors and diodes, and signal processing products.

Power MOS Devices

TEMIC Semiconductors is the silicon technology and packaging leader for 60-V- and -below power MOSFETs. Now in their third generation, TEMIC's TrenchFET™ power MOSFETs continue to break industry records, with the latest devices offering maximum on-resistance as low as 6 milliohms. TrenchFETs™ and advanced planar devices are available from TEMIC in through-hole and surface-mount packages, including the popular LITTLE FOOT® SO8, TSSOP8, and TSOP6.

IrDA Modules

For many years the industry leader in IR photo-module technology, TEMIC Semiconductors has quickly emerged as a top supplier of integrated transceivers and discrete components for data transmission solutions meeting the standards of the **I**nfra**r**ed **D**ata **A**ssociation (IrDA). TEMIC provides a full range of IrDA-compatible components, from transceiver modules with 115.2 kbit/s and 4 Mbit/s transmission rates to a family of discrete IREDs and photomodules that were used in the original implementations that formed the basis for the IrDA standard.

Optoelectronic Components

TEMIC Semiconductors has been a major supplier of optoelectronic devices for more than 20 years. In 1996, the company will supply upwards of 80 million IR photomodules for remote control applications. The photo pin diodes and GaA1As infrared emitting diodes at the heart of these devices are available as discrete components to provide maximum flexibility for customer designs. Visible LEDs and displays, along with a distinguished line of opto sensors, opto couplers, and opto switches, complete TEMIC's optoelectronic product offering. TEMIC Semiconductors' Optoelectronics Product Unit is located in Heilbronn, Germany.

Signal Processing

Offerings from the Signal Processing Product Unit include analog switches and multiplexers, JFETs, and DMOS FETs. A high-voltage silicon-gate process (versus the standard high-voltage metal-gate process) allows TEMIC to manufacture analog switches and multiplexers with lower analog channel leakages, higher accuracy, and faster operation than any other industry-standard products. TEMIC Semiconductors' Signal Processing Product Unit is located in Singapore.

Bipolar Transistors and Diodes

Products in this category, such as our no-roll-away MicroMELF diodes, provide the quality that customers expect plus the extra measure of ingenuity that sets TEMIC apart from its competitors. Our exclusive MOS Monolithic Circuits eliminate the need, e.g., in radio and TV tuners, for several external resistors and capacitors. Families of MOS and bipolar RF transistors, bipolar high-voltage switches, small-signal and zener diodes, as well as standard and ultra-fast rectifiers, complete the offerings of TEMIC Semiconductors' Bipolar Transistors and Diodes Business Unit located in Vöcklabruck, Austria.

TEMIC Quality Policy

Our goal is to achieve total customer satisfaction through everything we do. Therefore, the quality of our products and services is our number one priority.

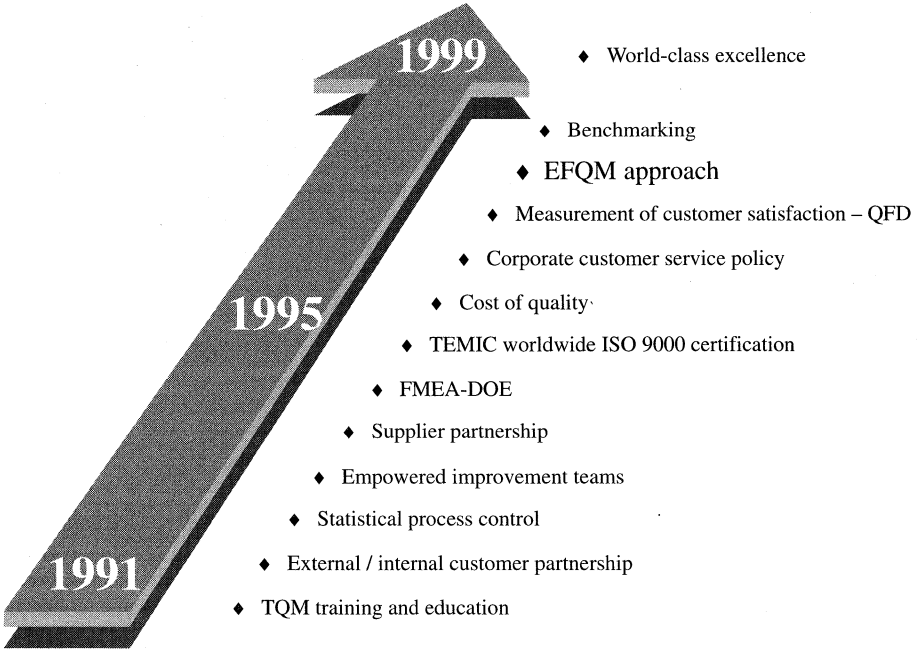
Quality comes first!

All of us at TEMIC are part of the process of continuous improvement.

Total Customer Satisfaction

Total customer satisfaction as stated in the 'TEMIC Quality Policy' means that **the customer comes first**. This applies throughout the organization, as we all strive to understand and meet the changing needs of our customers.

In this report, our methodology to achieve total customer satisfaction is shown. Furthermore, quality figures and future targets are given.



Quality System

Quality Program

At the heart of the quality process is TEMIC's worldwide quality program, **TEMIC Quality Movement (TQM)**. This program, which has been in place since the early 90's, is specifically designed to meet rapidly increasing customer quality demands now and in the future. The quality program is controlled by the TEMIC Quality Committee (TQC). The committee implements the Quality Policy and translates its requirements for use throughout the worldwide organization.

The TQC has defined a roadmap with specific targets along the way. The major target is to achieve world-class excellence throughout TEMIC Semiconductors worldwide by 1999.

TEMIC Quality Committee

The TEMIC Quality Committee (TQC) defines and implements the TEMIC quality policy at a corporate level. It acts to harmonize the quality systems of the constituent divisions and to implement Total Quality Management throughout the company worldwide.

Quality Goals and Methods

The goals are straightforward: Customer satisfaction through continuous improvement towards zero defects in every area of our operation. We are committed to meeting our customers' requirements in terms of quality and service. In order to achieve this, we build excellence into our product from concept to delivery and beyond.

- **Design-in Quality**
  Quality must be designed into products. TEMIC uses optimized design rules based on statistical information. This is refined using electrical, thermal and mechanical simulation together with techniques such as FMEA and DOE.

- **Built-in Quality**
  Quality is built into all TEMIC products by using qualified materials, suppliers and processes. Fundamental to this is the use of SPC techniques by both TEMIC and its suppliers. The use of these techniques, as well as tracking critical processes, reduces variability, optimizing the process with respect to the specification. The target is defect prevention and continuous improvement.

- **Qualification**
  All new products are qualified before release by submitting them to a series of mechanical, electrical and environmental tests. The same procedure is used for new or changed processes or packages.

- **Monitoring**
  A selection of the same or similar tests used for qualification is also used to monitor the short- and long-term reliability of the product.

- **SPC (Statistical Process Control)**
  SPC is an essential part of all TEMIC process control. It has been established for many years and is used as a tool for the continuous improvement of processes by measuring, controlling and reducing variability.

- **TEMIC's Quality System**
  All TEMIC's facilities worldwide are approved to ISO9000. In addition, some TEMIC companies hold approval to recognized international and industry standards such as MIL-STD-883, MIL-I-38535, SCC9000, AQAP1, Ford Q101, QS 9000.

The procedures used are based upon these standards and laid down in an approved and controlled Quality Manual.

Total Quality Management

Total Quality Management is a management system combining the resources of all employees, customers and suppliers in order to achieve total customer satisfaction. The fundamental elements of this system are:

- Management commitment
- EFQM assessment methodology
- Empowered Improvement Teams (EITs)
- Supplier development and partnership
- Quality tools
- Training
- Quality System

All TEMIC employees from the senior management downwards are trained in the understanding of TQM. Every employee plays its own part in the continuous improvement process which is fundamental to TQM and our corporate commitment to exceed customers' expectations in all areas including design, technology, manufacturing, human resources, marketing, and finance. Everyone is involved in fulfilling this goal. The management believes that this can only be achieved by employee empowerment.

The TEMIC corporate core values; leadership by example, employee empowerment, continuous improvement, total customer satisfaction and business excellence are the very essence of the TEMIC Quality Movement process.

- **Training**
  TEMIC maintains that it can only realize its aims if the employees are well-trained. It therefore invests heavily in courses to provide all employees with the knowledge they need to facilitate continuous improvement. A training profile has been established for all employees with emphasis being placed on Total Quality Leadership. Our long-term aim is to continuously improve our training so as to keep ahead of projected changes in business and technology.

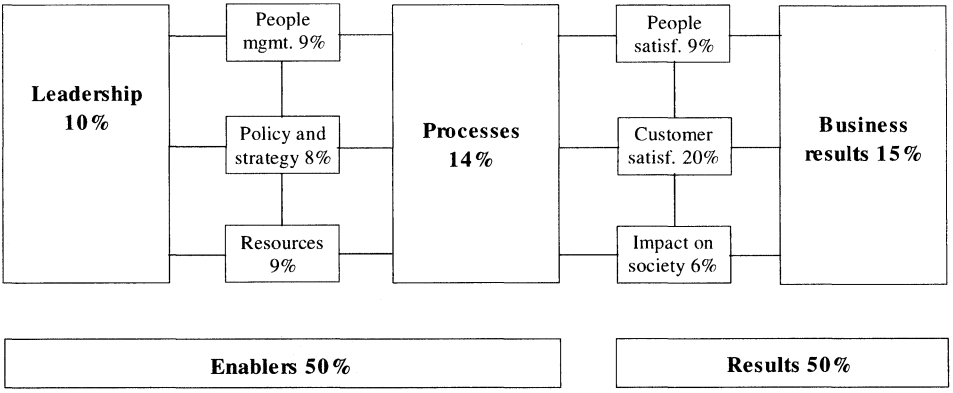
- **EFQM Assessment Methodology**
  From 1995, TEMIC has started to introduce the EFQM (European Foundation for Quality Management) methodology for structuring its Total Quality Management approach. This methodology, similar to the Malcolm Baldrige process, consists in self-assessing the various TEMIC divisions and facilities according to nine business criteria:

  - Leadership
  - People management
  - Policy and strategy
  - Resources
  - Processes
  - People satisfaction
  - Customer satisfaction
  - Impact on society
  - Business results

  The assessments are conducted on a yearly basis by 40 trained and empowered, internal TEMIC assessors. This permits the identification of key-priority improvement projects and the measurement of the progress accomplished.

  The EFQM methodology helps TEMIC to achieve world-class business excellence and will very soon bring either a Malcolm Baldrige- or an EFQM Award recognition.

- **Empowered Improvement Teams (EITs)**
  At TEMIC we believe that every person in the company has a contribution to make in meeting our target of customer satisfaction. Management therefore empowers employees to higher and higher levels of motivation, thus achieving higher levels of effectiveness and productivity. Empowered improvement teams, which are both functional and cross-functional, combine the varied talents from across the breadth of the company. By taking part in training, these teams are continually searching for ways to improve their jobs, achieving satisfaction for themselves, the company and – most important of all – the customer.



TQM Tools

As part of its search for excellence, TEMIC employs many different techniques and tools. Some of them are listed here:

- **Cost of Quality**
  Cost of Quality is used as a performance indicator. It is defined as the sum of the costs of:
  - Internal failure
  - External failure
  - Exceeding requirements
  - Lost opportunities
  - Prevention
  - Appraisal

  The goals are set as part of the company goals, initially at director level. All employees and EIT are expected to be aware of, determine, and track their associated costs.

- **Auditing**
  As well as third-party auditing employed for approval by ISO 9000 and customers, TEMIC carries out its own internal and external auditing. There is a common auditing procedure for suppliers and sub–contractors between the TEMIC entities. This procedure is also used for inter-company auditing between the facilities within TEMIC. It is based on the "Continuous Improvement" concept with heavy emphasis on the use of SPC and other statistical tools for the control and reduction of variability.Internal audits are carried out on a routine basis. They include audits of satellite facilities (i.e., sales offices, warehousing etc.). Audits are also used widely to determine attitudes and expectations both within and outside the company.

- **Failure Mode and Effect Analysis (FMEA)**
  FMEA is a technique for analyzing the possible methods of failure and their effect upon the performance/reliability of the product/process.
  Process FMEAs are performed for all processes. In addition, product FMEAs are performed on all critical or custom products.

- **Design of Experiments (DOE)**
  There is a series of tools which may be used for the statistical design of experiments. It consists of a formalized procedure for optimizing and analyzing experiments in a controlled manner. Taguchi and factorial experiment design are included in this. They provide a major advantage in determining the most important input parameters, making the experiment more efficient and promoting common understanding amongst team members of the methods and reasoning used.

- **Gauge Repeatability and Reproducibility (GR&R)**
  This technique is used to determine an equipment's suitability for purpose. It is used to make certain that all equipment is capable of functioning to the required accuracy and repeatability. All new equipment is approved before use by this technique.

- **Quality Function Deployment (QFD)**
  QFD is a method for translating customer requirements into recognizable requirements for TEMIC's marketing, design, research, manufacturing and sales (including aftersales). QFD is a process which brings together the life cycle of a product from its conception, through design, manufacture, distribution and use until it has served its expected life.

Quality Service

TEMIC believes that quality of service is equally as important as the technical ability of its products to meet their required performance and reliability. Our objectives therefore include:

- On-time delivery
- Short reaction time to customers' requests for information
- Rapid and informed technical support
- Fast handling of complaints
- A partnership with our customers

We have therefore implemented a customer service plan and charter which details our service targets. This is detailed in our brochure **The Business of Customer Service**. "The customer comes first" is a fundamental part of this charter.

- **Customer Complaints**
  Complaints fall mainly into two categories:
  - Logistical
  - Technical

TEMIC has a procedure detailing the handling of complaints. Initially complaints are forwarded to the appropriate sales office where in-depth information describing the problem is of considerable help in giving a fast and accurate response. If it is necessary to send back the product for logistical reasons, the Sales Office issues an RMA (**R**eturned **M**aterial **A**uthorization) number. On receipt of the goods in good condition, credit is automatically issued.

If there is a technical reason for complaint, a sample is sent to the Sales Office for forwarding to the Failure Analysis department of the supplying facility. The device's receipt will be acknowledged and a report issued on completion of the analysis. The cycle time for this analysis has set targets and is constantly monitored in order to improve the turnaround time. Failure analysis normally consists of electrical testing, functional testing, mechanical analysis (including X-ray), decapsulation, visual analysis and electrical probing. Other specialized techniques (i.e. LCD, thermal imaging, SEM, acoustic microscopy) may be used if necessary.

If the analysis uncovers a quality problem, a CAR (**C**orrective **A**ction **R**eport – in -8D format if required) will be issued. Any subsequent returns are handled with the RMA procedure.

- **Change Notification**
  All product and process changes are controlled and released via ECN (**E**ngineering **C**hange **N**otification). This requires the approval of the relevant departments. In the case of a major change, the change is forwarded to customers via Sales/ Marketing before implementation. Where specific agreements are in place, the change will not be implemented unless approved by the customer.

- **Ship-to-Stock/Ship-to-Line (STS/STL)**
  There are very low levels of rejects being delivered to customers. Many customers now require devices to be shipped direct to stock or to the production line by omitting any goods inwards inspection. TEMIC welcomes such agreements as part of its customer partnership program which promises an open approach in every aspect of its business.
  A product will only be supplied as STS or STL if there is a valid agreement in place between the two companies. Such an agreement details the quality level targets agreed upon between the companies and the methods to be used in case of problems.

TEMIC reserves the right to make changes in the products or specifications contained in this document in order to improve design or performance and to supply the best possible products. TEMIC also assumes no responsibility for the use of any circuits described herein, conveys no license under any patents or other rights, and makes no representations that the circuits are free from patent infringement. Applications for any integrated circuits contained in this publication are for illustration purposes only and TEMIC makes no representation or warranty that such applications will be suitable for the use specified without further testing or modification. Reproduction of any portion hereof without the prior written consent of TEMIC is prohibited.

Definition of Terms

The product datasheets contained in this document are referring to the following possible status:

Datasheet Identification	Definition
Preview	This datasheet contains the targeted specifications, all electrical parameters correspond to either targeted or simulated values. Specifications may change in any manner without notice.
Preliminary	This datasheet contains final functional specification. The electrical parameters given are based either on simulated values or on preliminary product characterization results. Specifications may change in any manner without notice.
No indication (blank)	This datasheet contains final specifications. TEMIC reserves the right to make changes at any time, according to TEMIC Quality Assurance procedures, in order to improve design and supply the best possible product.

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TEMIC 8–bit Microcontrollers: A Long Term Commitment

In the world of 8–bit microcontrollers, the 80C51 architecture has become an industry standard in embedded applications. Introduced in the early's 1980's by TEMIC/Matra MHS under Intel License, the 80C51 is still a market leader.

For over 15 years, TEMIC has been a leading provider of 80C51 microcontrollers to major embedded markets. Today, TEMIC is ranked number 3 in worldwide sales of 80C51 devices, representing over 20% market share. This unsurpassed experience is at the service of TEMIC customers in every application.

TEMIC now enlarges its product range by adding one time programmable (OTP) versions of standard products and the highly increased number of product derivatives for applications mainly targeted in the Communication, Computer and Automotive area.

Also the market is in need for a more powerful solution to meet the requirements of increasingly sophisticated embedded applications. High growth markets, including applications in communication, automotive and personal computing are driving these requirements. Therefore TEMIC has introduced in 1996 the first two products of the Intel–licensed TSC80251 8–bit extended architecture.

Our long–term commitment means you'll enjoy through C51 and C251 support for years to come.

This 8–bit Microcontroller Databook 1997 intends to provide you the latest information on the growing TEMIC offer. All available technical information of the C51 family is included while the literature for the TSC80251 family is available separately:

- TSC80251 Programmer's Guide
- TSC80251A1 Datasheet
- TSC80251G1 Design Guide

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Section I

C51 Architecture Information

Architectural Overview of the C51 Family

Summary

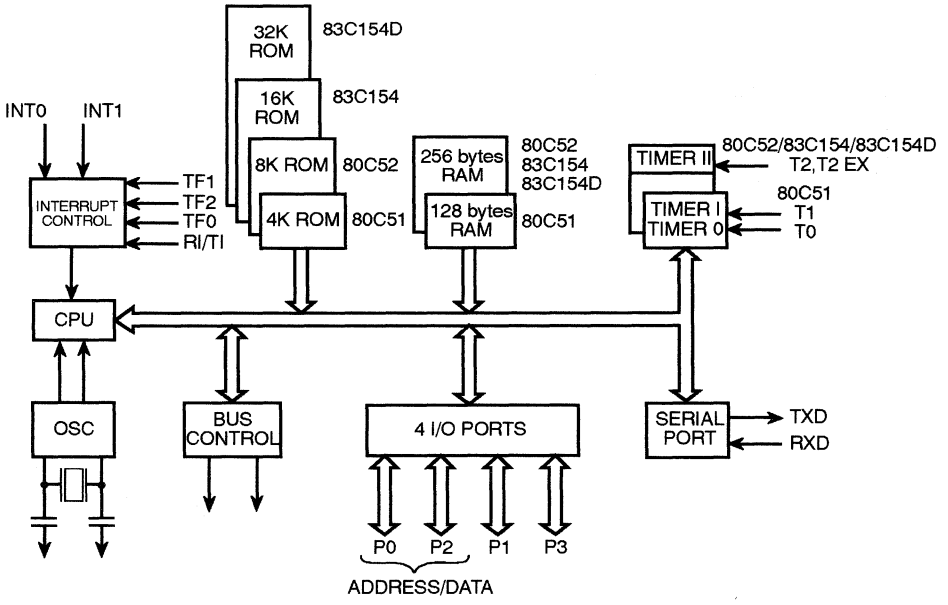
1. Introduction

The TEMIC C51 microcontroller family is based on the 80C51 core which features are :

- 8-bit CPU optimized for control applications
- Extensive boolean processing (single-bit logic) capabilities
- 64 K Program Memory address space
- 64 K Data Memory address space
- 4 K bytes of on chip Program Memory
- 128 bytes of on chip data RAM
- 32 bidirectionnal and individually addressable I/O lines
- two 16-bit timers/counters
- Full duplex UART
- 6 sources / 5-vector interrupt structure with 2 priority levels
- on chip clock oscillators

The basic architectural structure of the C51 microcontroller family is shown in figure 1.

Figure 1. Block Diagram



Each device of the C51 family is listed in Table 1.

Table 1 : C51 Family of Microcontrollers.

DEVICE NAME	ROMLESS VERSION	ROM BYTES	RAM BYTES	16-BIT TIMERS	SPEED UP TO	PROCESS
80C51, TSC80C51	80C31	4 K	128	2	44 MHz	CMOS
80C52	80C32	8 K	256	3	44 MHz	CMOS
83C154	80C154	16 K	256	3	36 MHz	CMOS
83C154D	—	32 K	256	3	36 MHz	CMOS
80C51PX	—	—	128/256	2/3	12 MHz	CMOS

1.1. TSC80C51/80C51/80C31

The 80C51 is the CMOS version of the 8051. Functionally, it is fully compatible with the 8051, but being CMOS it draws less current than its HMOS counterpart. To further exploit the power savings available in CMOS circuitry, two reduced power modes are added ;

- Software-invoked Idle Mode, during which the CPU is turned off while the RAM and other onchip peripherals continue operating. In this mode, current draw is reduced to about 15 % of the current drawn when the device is fully active.
- Software-invoked Power Down Mode, during which all on-chip activities are suspensed. The on-chip RAM continues to hold its data. In this mode the device typically draws less than 10 µA.

Although the 80C51 is functionally compatible with its HMOS counterpart, specific differences between the two types of devices must be considered in the design of an application circuit if one wishes to ensure complete interchangeability between the HMOS and CMOS devices.

The ROMless version of the 80C51 is the 80C31.

TSC80C51 is a core optimized version fully compatible with 80C51 (See product datasheets for electrical parameters).

1.2. 80C52/80C32

The 80C52 is an enhanced 80C51. It is produced with CMOS technology, and is compatible with the 80C51. Its enhancements over the 80C51 are as follows :

- 256 bytes of on-chip RAM
- Three timer/counters
- 6-source interrupt structure
- 8 K bytes of on-chip Program ROM

The ROMless version of the 80C52 is the 80C32.

1.3. 83C154/80C154

The 83C154 is an enhanced 80C52. It is produced with CMOS technology, and is compatible with the 80C51 and 80C52. Its enhancements over the 80C51 are as follows:

- 256 bytes of on-chip data RAM
- Three timer/counters (included watchdog and 32 bits timer/counters)
- 6 source interrupt structure
- Serial reception error detection
- New modes of power reduction consumption
- Programmable impedance port
- 16 K bytes of on-chip ROM
- Asynchronous Counter/Serial port mode during power-down

The ROMless version of the 83C154 is the 80C154.

1.4. 83C154D

The 83C154D is an enhanced 80C154. It is produced with CMOS technology, and is compatible with the 83C154. Its enhancements over the 80C51 are as follows :

- 256 bytes of on-chip data RAM
- Three timer/counters (included watchdog and 32 bits timer/counters)
- 6 source interrupt structure
- Serial reception error detection
- New modes of power reduction consumption
- Programmable impedance port
- 32 K bytes of on-chip ROM
- Asynchronous Counter/Serial port mode during power-down.

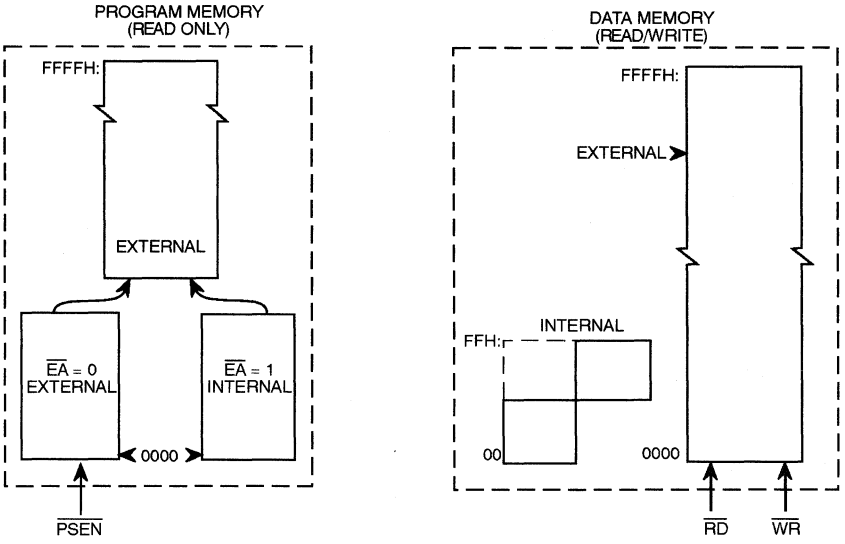
2. Memory Organization in C51 Devices

2.1. Logical Separation Of Program And Data Memory

All C51 devices have separated address spaces for program and Data Memory, as shown in figure 2. The logical separation of Program and Data Memory allows the Data Memory to be accessed by 8-bit addresses, which can be more quickly stored and manipulated by an 8-bit CPU. Nevertheless, 16-bit Data Memory addresses can also be generated through the DPTR register.

Program Memory can only be read, not written to. There can be up to 64 K bytes of program Memory. In the ROM versions of these devices the lowest 4 K, 8 K, 16 K or 32 K bytes of Program Memory are provided on-chip. Refer to Table 1 for the amount of on-chip ROM, on each device. In the ROMless versions all Program Memory is external. The read strobe for external Program Memory is the signal $\overline{PSEN}$ (Program Store Enable).

Figure 2. TEMIC C51 Memory Structure.



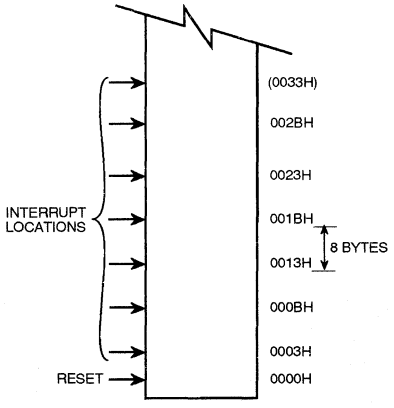
Data Memory occupies a separate address space from Program Memory. Up to 64 K bytes of external RAM can be addressed in the external Data Memory space. The CPU generates read and write signals, $\overline{RD}$ and $\overline{WR}$, as needed during external Data Memory accesses. External Program Memory and external Data Memory may be combined if desired by applying the $\overline{RD}$ and $\overline{PSEN}$ signals to the inputs of an AND gate and using the output of the gate as the read strobe to the external Program/Data memory.

2.2. Program Memory

Figure 3 shows a map of the lower part of the Program Memory. After reset, the CPU begins execution from location 0000H.

As shown in Figure 3, each interrupt is assigned a fixed location in Program Memory. The interrupt causes the CPU to jump to that location, where it commences execution of the service routine. External Interrupt 0, for example, is assigned to location 0003H. If External Interrupt 0 is going to be used, its service routine must begin at location 0003H. If the interrupt is not going to be used, its service location is available as general purpose Program Memory.

Figure 3. C51 Program Memory.



The interrupt service locations are spaced at 8-byte intervals : 0003H for External Interrupt 0, 000BH for Timer 0, 0013H for External Interrupt 1, 001BH for Timer 1, etc. If an interrupt service routine is short enough (as is often the case in control applications), it can reside entirely within that 8-byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use.

The lowest 4 K (or 8 K in the 80C52 or 16 K in the 83C154 or 32 K in the 83C154D) bytes of Program Memory can be either in the on-chip ROM or in an external ROM. This selection is made by strapping the $\overline{EA}$ (External Access) pin to either Vcc or Vss. In the 80C51 and its derivatives, if the $\overline{EA}$ pin is strapped to Vcc, then program fetches to addresses 0000H through 0FFFH are directed to the internal ROM. Program fetches to addresses 1000H through FFFFH are directed to external ROM.

In the 80C52, $\overline{EA}$ = Vcc selects addresses 0000H through 1FFFH to be internal, and addresses 2000H through FFFFH to be external.

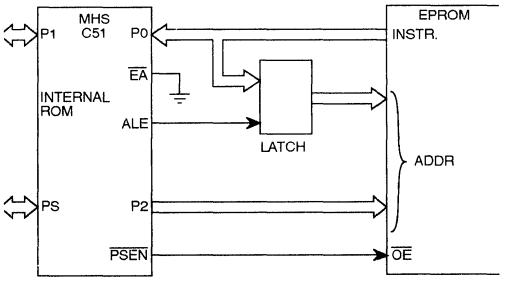
In the 83C154, $\overline{EA}$ = Vcc selects addresses 0000H through 3FFFH to be internal, and addresses 4000H to FFFFH to be external.

In the 83C154D, $\overline{EA}$ = Vcc selects addresses 0000H through 7FFFH to be internal and addresses 8000H to FFFFH to be external.

If the $\overline{EA}$ pin is strapped to Vss, then all program fetches are directed to external ROM. The ROMless parts must have this pin externally strapped to Vss to enable them to execute from external Program Memory.

The read strobe to external ROM, $\overline{PSEN}$, is used for all external program fetches. $\overline{PSEN}$ is not activated for internal program fetches.

Figure 4. Executing from External Program Memory.



The hardware configuration for external program execution is shown in figure 4. Note that 16 I/O lines (Ports 0 and 2) are dedicated to bus functions during external Program Memory fetches. Port 0 (P0 in Figure 4) serves as a multiplixed address/data bus. It emits the low byte of the Program Counter (PCL) as an address, and then goes into a float state awaiting the arrival of the code byte from the Program Memory. During the time that the low byte of the Program Counter is valid on P0, the signal ALE (Address Latch Enable) clocks this byte into an address latch. Meanwhile, Port 2 (P2 in Figure 4) emits the high byte of Program Counter (PCH). Then PSEN strobes the EPROM and the code byte is read into the microcontroller.

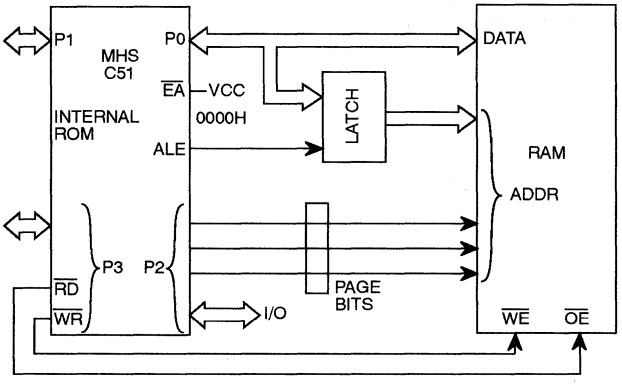
Program Memory addresses are always 16 bits wide, even though the actual amount of Program Memory used may be less than 64 K bytes. External program execution sacrifices two of the 8-bit ports, P0 and P2, to the function of addressing the Program Memory.

2.3. Data Memory

The right half of Figure 2 shows the internal and external Data Memory spaces available to the C51 user. Figure 5 shows a hardware configuration for accessing up to 2 K bytes of external RAM. The CPU in this case is executing from internal ROM. Port 0 serves as multiplexed address/data bus to the RAM, and 3 lines of Port 2 are being used to page the RAM. The CPU generates $\overline{RD}$ and $\overline{WR}$ signals as needed during external RAM accesses.

There can be up to 64 K bytes of external Data Memory. External Data Memory addresses can be either 1 or 2 bytes wide. One-byte address is often used in conjunction with one or more other I/O lines to page the RAM, as shown in Figure 5. Two-byte addresses can also be used, in which case the address byte is emitted at Port 2.

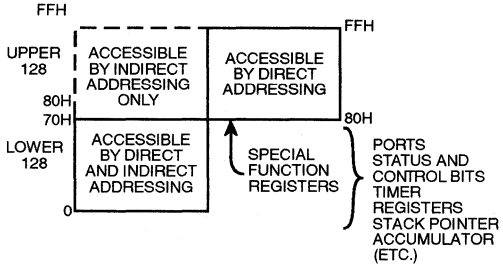
Figure 5. Accessing External Data Memory. If the Program Memory is external, the other bits of P2 are available as I/O.



Internal Data Memory is mapped in figure 6. The memory space is shown divided into three blocks, which are generally referred to as the lower 128, the Upper 128, and SFR space.

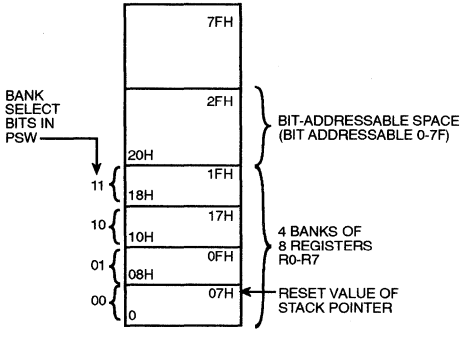
Internal Data Memory addresses are always one byte wide, which implies an address space of only 256 bytes. However, the addressing modes for internal RAM can in fact accomodate 384 bytes, using a simple trick. Direct addresses higher than 7FH access one memory space, and indirect addresses higher than 7FH access a different memory space. Thus figure 6 shows the Upper 128 and SFR space occupying the same block of addresses, 80H through FFH, although they are physically separate entities.

Figure 6. Internal Data Memory.



The Lower 128 bytes of RAM are present in all C51 devices as mapped in Figure 7. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word (PSW) select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

Figure 7. The Lower 128 Bytes of Internal RAM.



The next 16 bytes above the register banks form a block of bit-addressable memory space. The C51 instruction set includes a wide selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the Lower 128 can be accessed by either direct or indirect addressing. The Upper 128 (Figure 8) can only be accessed by indirect addressing. The Upper 128 bytes of RAM are not implemented in the 80C51 but are in the 80C52, 83C154 and 83C154D.

Figure 8. The Upper 128 Bytes of Internal RAM.

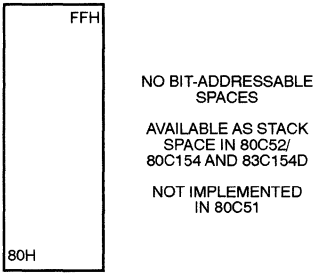
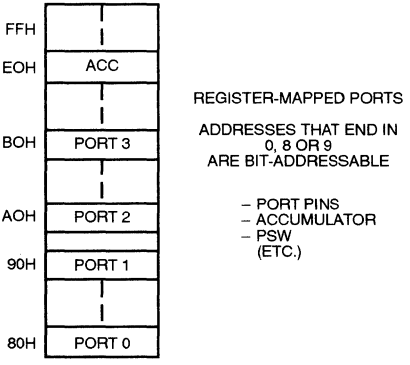


Figure 9 gives a brief look at the Special Function Register (SFR) space. SFRs include the Port latches, timers, peripheral controls, etc. These registers can only be accessed by direct addressing. In general, all C51 microcontrollers have the same SFRs as the 80C51, and at the same addresses in SFR space. However, enhancements to the 80C51 have additional SFRs that are not present in the 80C51, nor perhaps in other proliferation of the family.

Sixteen addresses in SFR space are both byte-and bit-addressable. The bit-addressable SFRs are those whose address ends in 0, 8 or 9. The bit addresses in this area are 80H through FFH.

Figure 9. SFR Space.



3. The C51 Instruction Set

All members of the C51 family execute the same instruction set. (except code A5H, skip opcode in C51/C52). The C51 instruction set is optimized for 8-bit control applications. It provides a variety of fast addressing modes for accessing the internal RAM to facilitate byte operations on small data structures. The instruction set provides extensive support for one-bit variables as a separate data type, allowing direct bit manipulation in control and logic systems that require Boolean processing.

An overview of the C51 instruction set is presented below, with a brief description of how certain instructions might be used.

3.1. Program Status Word

The Program Status Word (PSW) contains several status bits that reflect the current state of the CPU. The PSW, shown in Figure 10, resides in SFR space. It contains the Carry bit, the Auxiliary Carry (for BCD operations), the two register bank select bits, the Overflow flag, a parity bit, and two user-definable status flags.

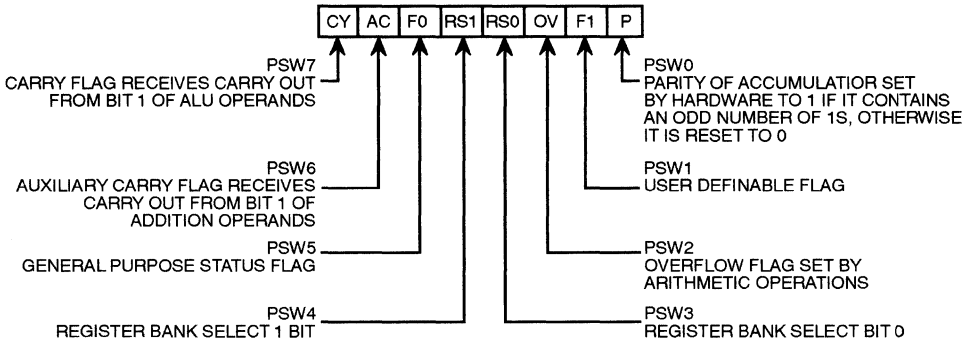
The Carry bit, other than serving the functions of a Carry bit in arithmetic operations, also serves as the "Accumulator" for a number of Boolean operations.

The bits RS0 and RS1 are used to select one of the four register banks shown in Figure 7. A number of instructions refer to these RAM locations as R0 through R7. The selection of which of the four banks is being referred to is made on the basis of the bits RS0 and RS1 at execution time.

The parity bit reflects the number of 1 s in the Accumulator : P = 1 if the Accumulator contains an odd number of 1 s, and P = 0 if the Accumulator contains an even number of 1 s. Thus the number of 1 s in the Accumulator plus P is always even.

Two bits in the PSW are uncommitted and may be used as general purpose status flags.

Figure 10. PSW (Program Status Word) Register in C51 Devices.



1

3.2. Addressing Modes

The addressing modes in the C51 instruction set are as follows :

3.2.1. Direct addressing

In direct addressing the operand is specified by an 8-bit address field in the instruction. Only 128 Lowest bytes of internal Data RAM and SFRs can be directly addressed.

3.2.2. Indirect addressing

In indirect addressing the instruction specifies a register which contains the address of the operand. Both internal and external RAM can be indirectly addressed.

The address register for 8-bit addresses can be R0 or R1 of the selected register bank, or the Stack Pointer. The address register for 16-bit addresses can only be the 16-bit "data pointer" register, DPTR.

3.2.3. Register instructions

The register banks, containing registers R0 through R7, can be accessed by certain instructions which carry a 3-bit register specification within the opcode of the instruction. Instructions that access the registers this way are code efficient, since this mode eliminates an address byte. When the instruction is executed, one of the eight registers in the selected bank is accessed. One of four banks is selected at execution time by the two bank select bits in the PSW.

3.2.4. Register-specific instructions

Some instructions are specific to a certain register. For example, some instructions always operate on the Accumulator, or Data Pointer, etc., so no address byte is needed to point to it. The opcode itself does that. Instructions that refer to the Accumulator as A assemble as accumulator-specific opcodes.

3.2.5. Immediate constants

The value of a constant can follow the opcode in Program Memory. For example,

MOV A, # 100

loads the Accumulator with the decimal number 100. The same number could be specified in hex digits as 64H.

3.2.6. Indexed addressing

Only Program Memory can be accessed with indexed addressing, and it can only be read. This addressing mode is intended for reading look-up tables in Program Memory. A 16-bit base register (either DPTR or the Program Counter) points to the base of the table, and the Accumulator is set up with the table entry number. The address of the table entry in Program Memory is formed by adding the Accumulator data to the base pointer.

Another type of indexed addressing is used in the "case jump" instruction. In this case the destination address of a jump instruction is computed as the sum of the base pointer and the Accumulator data.

3.3. Arithmetic Instructions

The menu of arithmetic instructions is listed in Table 2. The table indicates the addressing modes that can be used with each instruction to access the <byte> operand. For example, the ADD A, <byte> instruction can be written as :

```
ADD  A,   7FH      (direct addressing)
ADD  A,   @ R0     (indirect addressing)
ADD  A,   R7       (register addressing)
ADD  A,   # 127    (immediate constant)
```

Table 2 : A list of the TEMIC C51 Arithmetic Instructions.

MNEMONIC	OPERATION	ADDRESSING MODES				EXECUTION TIME (µs)
		Dir	Ind	Reg	Imm	
ADD A, <byt>e	A = A + <byte>	X	X	X	X	
ADDC A, <byte>	A = A + <byte> + C	X	X	X	X	1
SUBB A, <byte>	A = A – <byte> – C	X	X	X	X	1
INC A	A = A + 1	Accumulator only				1
INC <byte>	<byte> = <byte> + 1	X	X	X		1
INC DPTR	DPTR = DPTR + 1	Data Pointer only				2
DEC A	A = A – 1	Accumulator only				1
DEC <byte>	<byte> = <byte> – 1	X	X	X		1
MUL AB	B:A = B × A	ACC and B only				4
DIV AB	A = Int [A/B] B = Mod [A/B]	ACC and B only				4
DA A	Decimal Adjust	Accumulator only				1

The execution times listed in Table 2 assume a 12 MHz clock frequency. All of the arithmetic instructions execute in 1 µs except the INC DPTR instruction, which takes 2 µs, and the Multiply and Divide instructions, which take 4 µs.

Note that any byte in the internal Data Memory space can be incremented or decremented without going through the Accumulator.

One of the INC instructions operates on the 16-bit Data Pointer. The Data Pointer is used to generate 16-bit addresses for external memory, so being able to increment it in one 16-bit operation is a useful feature.

The MUL AB instruction multiplies the Accumulator by the data in the B register and puts the 16-bit product into the concatenated B and Accumulator registers.

The DIV AB instruction divides the Accumulator by the data in the B register and leaves the 8-bit quotient in the Accumulator, and the 8-bit remainder in the B register.

Oddly enough, DIV AB finds less use in arithmetic "divide" routines than in radix conversions and programmable shift operations. An example of the use of DIV AB in a radix conversion will be given later. In shift operations, dividing a number by 2^n shifts its n bits to the right. Using DIV AB to perform the division completes the shift in 4 µs leaves the B register holding the bits that were shifted out.

The DA A instruction is for BCD arithmetic operations. In BCD arithmetic ADD and ADDC instructions should always be followed by a DA A operation, to ensure that the result is also in BDC. Note that DAA will not convert a binary number to BCD. The DA A operation produces a meaningful result only as the second step in the addition of two BCD bytes.

3.4. Logical Instructions

Table 3 shows the list of TEMIC C51 logical instructions. The instructions that perform Boolean operations (AND, OR, Exclusive OR, NOT) on bytes perform the operation on a bit-by-bit basis. That is, if the Accumulator contains 00110101B and <byte> contains 01010011B, then

ANL A, <byte>

will leave the Accumulator holding 00010001B.
The addressing modes that can be used to access the <byte> operand are listed in Table 3. Thus, the ANL A, <byte> instruction may take any of the forms.

ANL A, 7FH	(direct addressing)
ANL A, @ R1	(indirect addressing)
ANL A, R6	(register addressing)
ANL A, # 53H	(immediate constant)

All of the logical instructions that are Accumulator specific in 1 µs (using a 12 MHz clock). The others take 2 µs.

Table 3 : A list of the TEMIC C51 Logical Instructions.

MNEMONIC	OPERATION	ADDRESSING MODES				EXECUTION TIME (µs)
		Dir	Ind	Reg	Imm	
ANL A, <byte>	A = A AND <byte>	X	X	X	X	1
ANL <byte>, A	<byte> = <byte> AND A	X				1
ANL <byte>, # data	<byte> = <byte> AND # data	X				2
ORL A, <byte>	A = A OR <byte>	X	X	X	X	1
ORL <byte>, A	<byte> = <byte> OR A	X				1
ORL <byte>, # data	<byte> = <byte> OR # data	X				2
XRL A, <byte>	A = A XOR <byte>	X	X	X	X	1
XRL <byte>, A	<byte> = <byte> XOR A	X				1
XRL <byte>, # data	<byte> = <byte> XOR # data	X				2
CLR A	A = 00H	Accumulator only				1
CLP A	A = NOT A	Accumulator only				1
RL A	Rotate ACC Left 1 bit	Accumulator only				1
RLC A	Rotate Left through Carry	Accumulator only				1
RR A	Rotate ACC Right 1 bit	Accumulator only				1
RRC A	Rotate Right through Carry	Accumulator only				1
SWAP A	Swap Nibbles in A	Accumulator only				1

Note that Boolean operations can be performed on any byte in the internal Data Memory space without going through the Accumulator. The XRL <byte>, # data instruction, for example, offers a quick and easy way to invert port bits, as in

XRL P1, #OFFH

If the operation is in response to an interrupt, not using the Accumulator saves the time and effort to stack it in the service routine.

The Rotate instructions (RLA, RLCA, etc.) shift the Accumulator 1 bit to the left or right. For a left rotation, the MSB rolls into the LSB position. For a right rotation, the LSB rolls into the MSB position.

The SWAP A instruction interchanges the high and low nibbles within the Accumulator. this is a useful operation in BCD manipulations. For example, if the Accumulator contains a binary number which is known to be less than 100, it can be quickly converted to BCD by the following code :

```
MOV     B, #10
DIV     AB
SWAP    A
ADD     A,B
```

Dividing the number by 10 leaves the tens digit in the low nibble of the Accumulator, and the ones digit in the B register. The SWAP and ADD instructions move the tens digit to the high nibble of the Accumulator, and the ones digit to the low nibble.

3.5. Data Transfers

3.5.1. Internal RAM

Table 4 shows the menu of instructions that are available for moving data around within the internal memory spaces, and the addressing modes that can be used with each one. With a 12 MHz clock, all of these instructions execute in either 1 or 2 µs.

The MOV <dest>, <src> instruction allows data to be transfered between any two internal RAM or SFR locations without going through the Accumulator. Remember the Upper 128 bytes of data RAM can be accessed only by indirect, and SFR space only by direct addressing.

Note that in all C51 devices, the stack resides in on-chip RAM, and grows upwards. The PUSH instruction first increments the Stack Pointer (SP), then copies the byte into the stack. PUSH and POP use only direct addressing to identify the byte being saved or restored, but the stack itself is accessed by indirect addressing using the SP register. This means the stack can go into the Upper 128, if they are implemented, but not into SFR space.

Table 4 : A list of the TEMIC C51 Data Transfer Instructions that Access Internal Data Memory Space.

MNEMONIC	OPERATION	ADDRESSING MODES				EXECUTION TIME (µs)
		Dir	Ind	Reg	Imm	
MOV A, <src>	A = <src>	X	X	X	X	1
MOV <dest>, A	<dest> = A	X	X	X		1
MOV <dest>, <src>	<dest> = <src>	X	X	X	X	2
MOV DPTR, # data 16	DPTR = 16-bit immediate constant				X	2
PUSH <src>	INC SP : MOV "@SP", <scr>	X				2
POP <dest>	MOV <dest>, "@SP" : DEC SP	X				2
XCH A, <byte>	ACC and <byte> Exchange Data	X	X	X		1
XCHD A, @Ri	ACC and @ Ri exchange low nibbles		X			1

The Upper 128 are not implemented in the 80C51, nor in their ROMless. With these devices, if the SP points to the Upper 128 PUSHed bytes are lost, and POPped bytes are indeterminate.

The Data Transfer instructions include a 16-bit MOV that can be used to initialize the Data Pointer (DPTR) for look-up tables in Program Memory, or for 16-bit external Data Memory accesses.

The XCH A, <byte> instruction causes the Accumulator and addressed byte to exchange data.
The XCHD A, @ Ri instruction is similar, but only the low nibbles are involved in the exchange.

The see how XCH and XCHD can be used to facilitate data manipulations, consider first the problem of shifting an 8-digit BCD number two digits to the right. Figure 11 shows how this can be done using direct MOVs, and for comparison how it can be done using XCH instructions. To aid in understanding how the code works, the contents of the registers that are holding the BCD number and the content of the Accumulator are shown alongside each instruction to indicate their status after the instruction has been executed.

After the routine has been executed, the Accumulator contains the two digits that were shifted out on the right. Doing the routine with direct MOVs uses 14 code bytes and 9 µs of execution time (assuming a 12 MHz clock). The same operation with XCHs uses less code and executes almost twice as fast.

Figure 11. Shifting a BCD Number Two Digits to the Right.

	2A	2B	2C	2D	2E	ACC
MOV A,2EH	00	12	34	56	78	78
MOV 2EH, 2DH	00	12	34	56	56	78
MOV 2DH, 2CH	00	12	34	34	56	78
MOV 2CH, 2BH	00	12	12	34	56	78
MOV 2BH, # 0	00	00	12	34	56	78

(a) Using direct MOVs : 14 bytes, 9 µs

	2A	2B	2C	2E	2E	ACC
CLR A	00	12	34	56	78	00
XCH A,2BH	00	00	34	56	78	12
XCH A,2CH	00	00	12	56	78	34
XCH A,2DH	00	00	12	34	78	56
XCH A,2EH	00	00	12	34	56	78

(b) Using XCHs : 9 bytes, 5 µs

Figure 12. Shifting a BCD Number One Digit to the Right.

	2A	2B	2C	2D	2E	ACC
MOV R1,# 2EH	00	12	34	56	78	XX
MOV R0, # 2DH	00	12	34	56	78	XX
loop for R1 = 2EH :						
LOOP : MOV A, @R1	00	12	34	56	78	78
XCHD A, @R0	00	12	34	58	78	76
SWAP A	00	12	34	58	78	67
MOV @R1, A	00	12	34	58	67	67
DEC R1	00	12	34	58	67	67
DEC R0	00	12	34	58	67	67
CJNE R1, #2AH, LOOP						
loop for R1 = 2DH :	00	12	38	45	67	45
loop for R1 = 2CH :	00	18	23	45	67	23
loop for R1 = 2BH :	08	01	23	45	67	01
CLR A	08	01	23	45	67	00
XCH A,2AH	00	01	23	45	67	08

To right-shift by an odd number of digits, a one-digit shift must be executed. Figure 12 shows a sample of code that will right-shift a BCD number one digit, using the XCHD instruction. Again, the contents of the registers holding the number and of the Accumulator are shown alongside each instruction.

First, pointers R1 and R0 are set up to point to the two bytes containing the last four BCD digits. Then a loop is executed which leaves the last byte, location 2EH, holding the last two digits of the shifted number. The pointers are decremented, and the loop is repeated for location 2DH. The CJNE instruction (Compare and Jump if Not Equal) is a loop control that will be described later.

The loop is executed from LOOP to CJNE for R1 = 2EH, 2DH, 2CH and 2BH. At that point the digit that was originally shifted out on the right has propagated to location 2AH. Since that location should be left with 0s, the lost digit is moved to the Accumulator.

3.6. External RAM

Table 5 shows a list of the Data Transfer instructions that access external Data Memory. Only indirect addressing can be used. The choice is whether to use a one-byte address, @Ri, where Ri can be either R0 or R1 of the selected register bank, or a two-byte address, @DPTR. The disadvantage to using 16-bit addresses if only a few K bytes of external RAM are involved is that 16-bit addresses use all 8 bits of Port 2 as address bus. On the other hand, 8-bit addresses allow one to address a few K bytes of RAM, as shown in Figure 5, without having to sacrifice all of Port 2.

All of these instructions execute in 2 µs, with a 12 MHz clock.

Note that in all external Data RAM accesses, the Accumulator is always either the destination or source of the data.

The read and write strobes to external RAM are activated only during the execution of a MOVX instruction. Normally these signals are inactive, and in fact if they're not going to be used at all, their pins are available as extra I/O lines. More about that later.

Table 5 : A list of the TEMIC C51 Data Transfer Instructions that Access External Data Memory Space.

ADDRESS WIDTH	MNEMONIC	OPERATION	EXECUTION TIME (µs)
8 bits	MOVX A, @Ri	Read external RAM @ Ri	2
8 bits	MOVX @ Ri, A	Write external RAM @ Ri	2
16 bits	MOVX A, @ DPTR	Read external RAM @ DPTR	2
16 bits	MOVX @ DPTR, A	Write external RAM @ DPTR	2

3.7. Lookup Tables

Table 6 shows the two instructions that are available for reading lookup tables in Program Memory. Since these instructions access only Program Memory, the lookup tables can be read, not updated. The mnemonic is MOVC for "move constant".

If the table access is to external Program Memory, then the read strobe is $\overline{PSEN}$.

The first MOVC instruction in Table 6 can accomodate a table of up to 256 entries, numbered 0 through 255. The number of the desired entry is loaded into the Accumulator, and the Data Pointer is set up to point to beginning of the table. Then

MOVC A, @A + DPTR

copies the desired table entry into the Accumulator.

The other MOVC instruction works the same way, except the Program Counter (PC) is used as the table base, and the table is accesses through a subroutine. First the number of the desired entry is loaded into the Accumulator, and the subroutine is called :

```
MOV     A, ENTRY_NUMBER
CALL    TABLE
```

The subroutine "TABLE" would look like this :

```
TABLE :  MOVC A, @A + PC
         RET
```

The table itself immediately follows the RET (return) instruction in Program Memory. This type of table can have up to 255 entries, numbered 1 through 255. Number 0 can not be used, because at the time the MOVC instruction is executed, the PC contains the address of the RET instruction. An entry numbered 0 would be the RET opcode itself.

Table 6 : The C51 Lookup Table Read Instructions.

MNEMONIC	OPERATION	EXECUTION TIME (µs)
MOVC A, @A + DPTR	Read Pgm Memory at (A + DPTR)	2
MOVC A, @A + PC	Read Pgm Memory at (A + PC)	2

3.8. Boolean Instructions

C51 devices contain a complete Boolean (single-bit) processor. The internal RAM contains 128 addressable bits, and the SFR space can support up to 128 other addressable bits. All of the port lines are bit-addressable, and each one can be treated as a separate single-bit port. The instructions that access these bits are not just conditional branches, but a complete menu of move, set, clear, complement, OR and AND instructions. These kinds of bit operations are not easily obtained in other architectures with any amount of byte-oriented software.

The instruction set for the Boolean processor is shown in Table 7. All bit accesses are by direct addressing. Bit addresses 00H through 7FH are in the Lower 128, and bit addresses 80H through FFH are in SFR space.

Table 7 : A list of the C51 Boolean Instructions.

MNEMONIC	OPERATION	EXECUTION TIME (µs)
ANL C,bit	C = C AND bit	2
ANL C,/bit	C = C AND (NOT bit)	2
ORL C,bit	C = C OR bit	2
ORL C,/bit	C = C OR (NOT bit)	2
MOV C,bit	C = bit	1
MOV bit,C	bit = C	2
CLR C	C = 0	1
CLR bit	bit = 0	1
SETB C	C = 1	1
SETB bit	bit = 1	1
CPL C	C = NOT C	1
CPL bit	bit = NOT bit	1
JC rel	Jump if C = 1	2
JNC rel	Jump if C = 0	2
JB bit,rel	Jump if bit = 1	2
JNB bit,rel	Jump if bit = 0	2
JBC bit,rel	Jump if bit = 1 ; CLR bit	2

Note how easily an internal flag can be moved to a port pin :

```
MOV     C, FLAG
MOV     P1.0, C
```

In this example, FLAG is the name of any addressable bit in the lower 128 or SFR space. An I/O line (the LSB of Port 1, in the case) is set or cleared depending on whether the flag bit is 1 or 0.

The Carry bit in the PSW is used as the single-bit Accumulator of the Boolean processor. Bit instructions that refer to the Carry bit as C assemble as Carry-specific instructions (CLR C, etc). The Carry bit also has a direct address, since it resides in the PSW register, which is bit-addressable.

Note that the Boolean instruction set includes ANL and ORL operations, but not the XRL (Exclusive OR) operation. An XRL operation is simple to implement in software. Suppose, for example, it is required to form the Exclusive OR of two bits :

C = bit1 XRL bit2

The software to do that could be as follows :

```
MOV     C, bit1
JNB     bit2, OVER
CPL     C
OVER : (continue)
```

First, bit 1 is moved to the Carry. If bit 2 = 0, then C now contains the correct result. That is, bit 1 XRL bit2 = bit1 if bit2 = 0. On the other hand, if bit2 = 1 C now contains the complement of the correct result. It need only be inverted (CPL C) to complete the operation.

This code uses the JNB instruction, one of a series of bit-test instructions which execute a jump if the addressed bit is set (JC, JB, JBC) or if the addressed bit is not set (JNC, JNB). In the above case, bit2 is being tested, and if bit2 = 0 the CPL C instruction is jumped over.

JBC executes the jump if the addresed bit is set, and also clears the bit. Thus a flag can be tested and cleared in one operation.

All the PSW bits are directly addressable, so the Parity bit, or the general purpose flags, for example, are also available to the bit-test instructions.

3.8.1. Relative offset

The destination address for these jumps is specified to the assembler by a label or by an actual address in Program Memory. However, the destination address assembles to a relative offset byte. This is a signed (two's complement) offset byte which is added to the PC in two's complement arithmetic if the jump is executed.

The range of the jump is therefore -128 to + 127 Program Memory bytes relative to the first byte following the instruction.

3.9. Jump Instructions

Table 8 shows the list of unconditional jumps.

Table 8 : Unconditional Jumps in TEMIC C51.

MNEMONIC	OPERATION	EXECUTION TIME (µs)
JMP addr	Jump to addr	2
JMP @A + DPTR	Jump to A + DPTR	2
CALL addr	Call subroutine at addr	2
RET	Return from subroutine	2
RETI	Return from interrupt	2
NOP	No operation	1

The table lists a single "JMP addr" instruction, but in fact there are three -SJMP, LJMP, AJMP -which differ in the format of the destination address. JMP is a generic mnemonic which can be used if the programmer does not care which way the jump is encoded.

The SJMP instruction encodes the destination address as relative offset, as described above. The instruction is 2 bytes long, consisting of the opcode and the relative offset byte. The jump distance is limited to range of -128 to + 127 bytes relative to the instruction following the SJMP.

The LJMP instruction encodes the destination address as a 16-bit constant. The instruction is 3 bytes long, consisting of the opcode and two address bytes. The destination address can be anywhere in the 64K Program Memory space.

The AJMP instruction encodes the destination address as an 11-bit constant. The instruction is 2 bytes long, consisting of the opcode, which itself contains 3 of the 11 address bits, followed by another byte containing the low 8 bits of the destination address. When the instruction is executed, these 11 bits are simply substituted for the low 11 bits in the PC. The high 5 bits stay the same. Hence the destination has to be within the same 2K block as the instruction following the AJMP.

In all cases the programmer specifies the destination address to the assembler in the same way : as a label or as a 16-bit constant. The assembler will put the destination address into the correct format for the given instruction. If the format required by the instruction will not support the distance to the specified destination address, a "Destination out of range" message is written, into the list file.

The JMP @ A + DPTR instruction supports case jumps. The destination address is computed at execution time as the sum of the 16-bit DPTR register and the Accumulator. Typically, DPTR is set up with the address of a jump table, and the Accumulator is given an index to the table. In a 5-way branch, for example, an integer 0 through 4 is loaded into the Accumulator.

The code to be executed might be as follows :

```
MOV     DPTR, # JUMP_TABLE
MOV     A, INDEX_NUMBER
RL      A
JMP     @ A + DPTR
```

The RLA instruction converts the index number (0 through 4) to an even number on the range 0 through 8, because each entry in the jump table is 2 bytes long :

```
JUMP_TABLE :
        AJMP CASE_0
        AJMP CASE_1
        AJMP CASE_2
        AJMP CASE_3
        AJMP CASE_4
```

Table 8 shows a single "CALLaddr" instruction, but there are two of them -LCALL and ACALL -which differ in the format in which the subroutine address is given to the CPU. CALL is a generic mnemonic which can be used if the programmer does not care which way the address is encoded.

The LCALL instruction uses the 16-bit address format, and the subroutine can be anywhere in the 64K Program Memory space. The ACALL instruction uses the 11-bit format, and the subroutine must be in the same 2K block as the instructon following the ACALL.

In any case the programmer specifies the subroutine address to the assembler in the same way : as a label or as a 16-bit constant. The assembler will put the address into the correct format for the given instructions.

Subroutines should end a RET instruction, which returns execution following the CALL.

RETI is used to return from an interrupt service routine. The only difference between RET and RETI is that RETI tells the interrupt control system that the interrupt in progress is done. If there is no interrupt in progress at the time RETI is executed, then the RETI is functionnally identical to RET.

Table 9 shows the list of conditional jumps available to the TEMIC C51 user. All of these jumps specify the destination address by the relative offset method, and so are limited to a jump distance of -128 to + 127 bytes from the instruction following the conditional jump instruction. Important to note, however, the user specifies to the assembler the actual destination address the same way as the other jumps : as a label or a 16-bit constant.

Table 9 : Conditional Jumps in TEMIC C51 Devices.

MNEMONIC	OPERATION	ADDRESSING MODES				EXECUTION TIME (µs)
		DIR	IND	REG	IMM	
JZ rel	Jump if A = 0	Accumulator only				2
JNZ rel	Jump if A ≠ 0	Accumulator only				2
DJNZ <byte>,rel	Decrement and jump if not zero	X		X		2
CJNZ A,<byte>,rel	Jump if A = <byte>	X			X	2
CJNE <byte>,#data,rel	Jump if <byte> = #data		X	X		2

There is no Zero bit in the PSW. The JZ and JNZ instructions test the Accumulator data for that condition.

The DJNZ instruction (Decrement and Jump if Not Zero) is for loop control. To execute a loop N times, load a counter byte with N and terminate the loop with DJNZ to the beginning of the loop, as shown below for N = 10 :

```
        MOV     COUNTER, # 10
LOOP :  (begin loop)
        *
        *
        *
        (end loop)
        DJNZ    COUNTER, LOOP
        (continue)
```

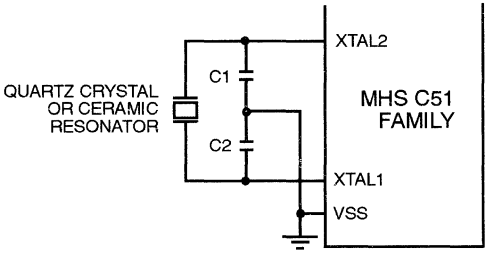
The CJNE instruction (Compare and Jump if Not Equal) can also be used for loop control as in Figure 12. Two bytes are specified in the operand field of the instruction. The jump is executed only if the two bytes are not equal. In the example of Figure 12, the two bytes were the data in R1 and the constant 2AH. The initial data in R1 was 2EH. Every time the loop was executed, R1 was decremented, and the looping was to continue until the R1 data reached 2AH.

Another application of this instruction is in "greater than, less than" comparisons. The two bytes in the operand field are taken as unsigned integers. If the first is less than the second, then the Carry bit is set (1). If the first is greater than or equal to the second, then the Carry bit is cleared.

4. CPU Timing

All C51 microcontrollers have an on-chip oscillator which can be used if desired as the clock source for the CPU. To use the on-chip oscillator, connect a crystal or ceramic resonator between the XTAL1 and XTAL2 pins of the microcontroller, and capacitors to ground as shown in Figure 13.

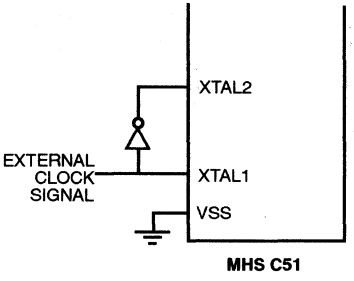
Figure 13. Using the On-Chip Oscillator.



Examples of how to drive the clock with an external oscillator are shown in Figure 14. In the TEMIC C51 devices the signal at the XTAL1 pin drives the internal clock generator. If only one pin is going to be driven with the external oscillator signal, make sure it is the right pin.

The internal clock generator defines the sequence of states that make up the TEMIC C51 machine cycle.

Figure 14. Using an External Clock.

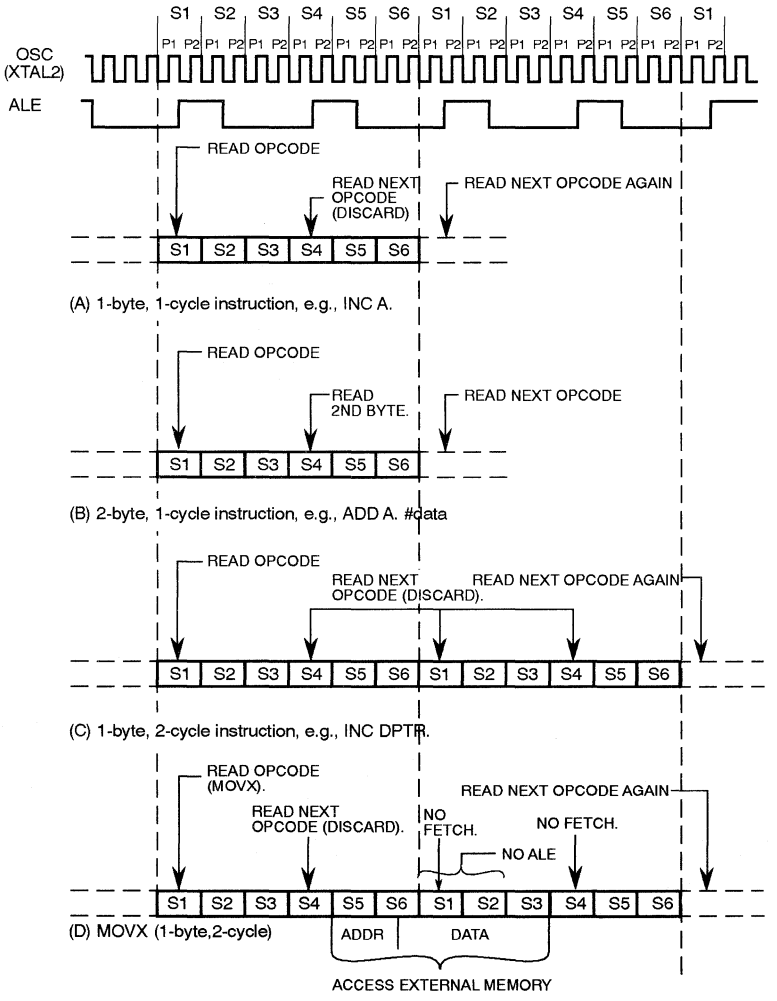


4.1. Machine Cycles

A machine cycle consists of a sequence of 6 states, numbered S1 through S6. Each state time lasts for two oscillator periods. Thus a machine cycle takes 12 oscillator periods or 1 µs if the oscillator frequency is 12 MHz.

Each state is divided into a Phase 1 half and a Phase 2 half. Figure 15 shows the fetch/execute sequences in states and phases for various kinds of instructions. Normally two program fetches are generated during each machine cycle, even if the instruction being executed doesn't require it. If the instruction being executed doesn't need more code bytes, the CPU simply ignores the extra fetch, and the Program Counter is not incremented.

Figure 15. State Sequences in TEMIC C51.



Execution of a one-cycle instruction (Figure 15A and B) begins during State 1 of the machine cycle, when the opcode is latched into the Instruction Register. A second fetch occurs during S4 of the same machine cycle. Execution is completed at the end of State 6 of this machine cycle.

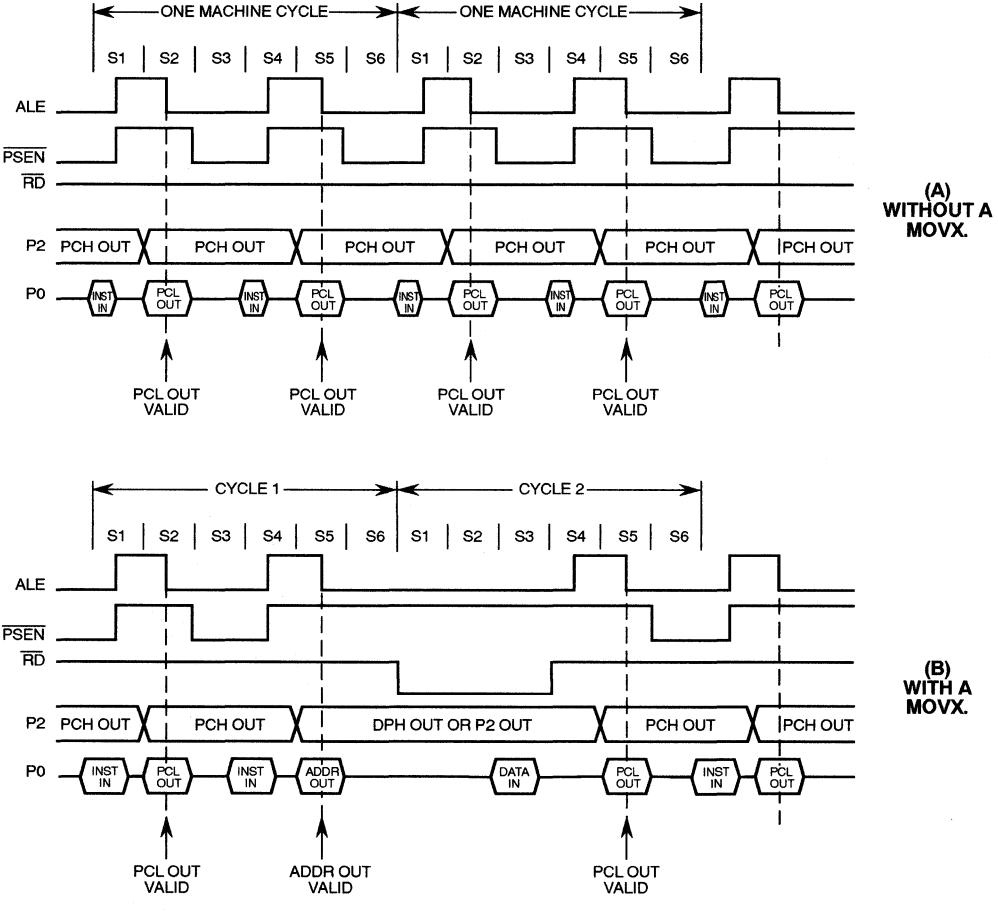
The MOVX instructions take two machine cycles to execute. No program fetch is generated during the second cycle of a MOVX instruction. This is the only time program fetches are skipped. The fetch/execute sequence for MOVX instructions is shown in Figure 15 (D).

The fetch/execute sequences are the same whether the Program Memory is internal or external to the chip. Execution times do not depend on whether the Program Memory is internal or external.

Figure 16 shows the signals and timing involved in program fetches when the Program Memory is external. If Program Memory is external, then, the Program Memory read strobe $\overline{PSEN}$ is normally activated twice per machine cycle, as shown in Figure 16 (A).

If an access to external Data Memory occurs, as shown in Figure 16 (B), two $\overline{PSEN}$s are skipped, because the address and data bus are being used for the Data Memory access.

Figure 16. Bus Cycles in TEMIC C51 Devices Executing from External Program Memory.



Note that a Data Memory bus cycle takes twice as much time as a Program Memory bus cycle. Figure 16 shows the relative timing of the addresses being emitted at ports 0 and 2, and of ALE and $\overline{PSEN}$. ALE is used to latch the low address byte from P0 into the address latch.

When the CPU is executing from internal Program Memory, PSEN is not activated, and program addresses are not emitted. However, ALE continues to be activated twice per machine cycle and so is available as a clock output signal. Note, however, that one ALE is skipped during the execution of the MOVX instruction.

4.2. Interrupt Structure

The 80C51 and his ROMless version provide 5 interrupt sources : 2 external interrupts, 2 timer interrupts, and the serial port interrupt. the 80C52, 83C154 and 83C154D and their ROMless version provide these 5 plus a sixth interrupt that is associated with the third timer/counter which is present in those devices.

What follows is an overview of the interrupt structure for these devices. More detailed information for specific members of the TEMIC C51 family is provided in the chapters of this handbook that describe the specific devices.

4.2.1. Interrupt Enables

Each of the interrupt source can be individually enabled or disabled by setting or clearing a bit in the SFR named IE (Interrupt Enable). This register also contains a global disable bit, which can be cleared to disable all interrupts at once. Figure 17 shows the IE register for the 80C51, 80C52 and 83C154 or the 83C154D.

Figure 17. IE (Interrupt Enable) Register in the 80C51, 80C52, 83C154 and 83C154D.

(MSB) (LSB)

EA	X	ET2	ES	ET1	EX1	ET0	EX0

Symbol	Position	Function
EA	IE.7	disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
–	IE.6	reserved
ET2	IE.5	enables or disables the Timer 2 overflow or capture interrupt. If ES = 0, the Timer 2 interrupt is disabled.
ES	IE.4	enables or disables the Serial Port interrupt. If ES = 0, the Serial Port interrupt is disabled.
ET1	IE.3	enables or disables the Timer 1 Overflow interrupt. If ET1 = 0, the Timer 1 interrupt is disabled.
EX1	IE.2	enables or disables External Interrupt 1. If EX1 = 0, External Interrupt 1 is disabled.
ET0	IE.1	enables or disables the Timer 0 Overflow interrupt. If ET0 = 0, the Timer 0 interrupt is disabled.
EX0	IE.0	enables or disables External Interrupt 0. If EX0 = 0, External Interrupt 0 is disabled.

4.2.2. Interrupt priorities

Each interrupt source can also be individually programmed to one of two priority level by setting or clearing a bit in the SFR named IP (Interrupt Priority). Figure 18 shows the IP register in the 80C51, 80C52, *83C154 and 83C154D.

A low-priority interrupt can be interrupted by a high-priority interrupt, but not by another low-priority interrupt.

A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Figure 18. IP (Interrupt Priority) Register in the 80C51, 80C52, 83C154 and 83C154D.

(MSB) (LSB)

PCT	X	PT2	PS	PT1	PX1	PT0	PX0

Symbol	Position	Function
PCT	IP.7	83C154/C154D only. Priority interrupt circuit control bit. The priority register contents are valid and priority assigned interrupts can be processed when this bit is "0". When the bit is "1", the priority interrupt circuit is stopped, and interrupts can only be controlled by the interrupt enable register (IE).
–	IP.6	reserved
PT2	IP.5	defines the Timer 2 interrupt priority level. PT2 = 1 programs it to the higher priority level.
PS	IP.4	defines the Serial Port interrupt priority level. PS = 1 programs it to the higher priority level.
PT1	IP.3	defines the Timer 1 interrupt priority level. PT1 = 1 programs it to the higher priority level.
PX1	IP.2	defines the External Interrupt 1 priority level. PX1 = 1 programs it to the higher priority level.
PT0	IP.1	defines the Timer 0 interrupt priority level. PT0 = 1 programs it to the higher priority level.
PX0	IP.0	defines the External Interrupt 0 priority level. PX0 = 1 programs it to the higher priority level.

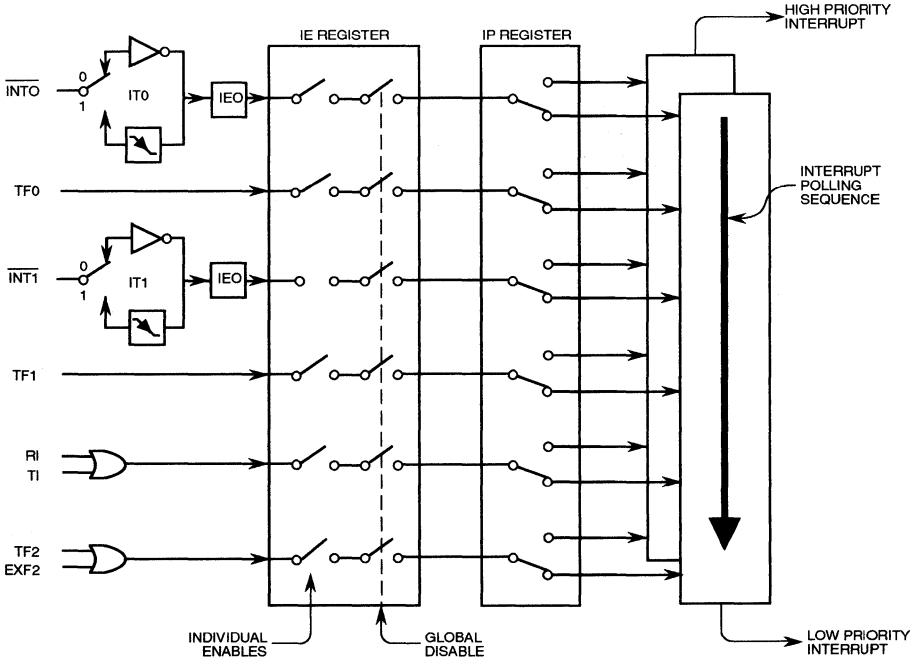
Figure 19 shows, for the 80C51, 80C52, 83C154 and 83C154D, how the IE and IP registers and the polling sequence work to determine which interrupt will be serviced.

In operation, all the interrupt flags are latched into the interrupts control system during State 5 of every machine cycle. The samples are polled during the following machine cycle. If the flag for an enabled interrupt is found to be set (1), the interrupt system generates an LCALL to the appropriate location in Program Memory, unless some other condition blocks the interrupt. Several conditions can block an interrupt, among them that an interrupt of equal or higher priority level is already in progress.

The hardware-generated LCALL causes the contents of the Program Counter to be pushed onto the stack, and reloads the PC with the beginning address of the service routine. As previously noted (Figure 3), the service routine for each interrupt begins at a fixed location.

Only the Program Counter is automatically pushed onto that stack, not the PSW or any other register. Having only the PC be automatically saved allows the programmer to decide how much time to spend saving which other registers. This enhances the interrupt response time, albeit at the expense of increasing the programmer's burden of responsability. As a result, many interrupt functions that are typical in control applications-toggling a port pin, for example, or reloading a timer, or unloading a serial buffer can often be completed in less time than it takes other architectures to commence them.

Figure 19. 80C51, 80C52, 83C154 and 83C154D Interrupt Control System.



4.2.3. Simulating a third priority level in software

Some applications require more than the two priority levels that are provided by on-chip hardware in C51 devices. In these cases, relatively simple software can be written to produce the same effect as a third priority level. First, interrupts that are to have higher priority than 1 are assigned to priority 1 in the IP (Interrupt Priority) register. The service routines for priority 1 interrupts that are supposed to be interruptible by "priority 2" interrupts are written to include the following code :

```
        PUSH    IE
        MOV     IE, # MASK
        CALL    LABEL
              **********
        (execute service routine)
              ********
        POP     IE
        RET
LABEL : RETI
```

As soon as any priority 1 interrupt is acknowledged, the IE (Interrupt Enable) register is redefined so as to disable all but "priority 2" interrupts. Then, a CALL to LABEL executes the RETI instruction, which clears the priority 1 interrupt-in-progress flip-flop. At this point any priority 1 interrupt that is enabled can be serviced, but only "priority 2" interrupts are enabled.

POPping IE restores the original enable byte. Then a normal RET (rather than another RETI) is used to terminate the service routine. The additional software adds 10 µs (at 12 MHz) to priority 1 interrupts.

Hardware Description of the C51 Family Products

Summary

1. Common Features Description

1.1. Introduction

This chapter presents a comprehensive description of the on-chip hardware features of the TEMIC C51 microcontrollers. Included in this description are :

- The port drivers and how they function both as ports and, for Ports 0 and 2, in bus operations
- The Timer/Counters
- The serial Interface
- The Interrupt System
- Reset
- The reduced Power Modes

Figure 1. C51 Architecture Block Diagram.

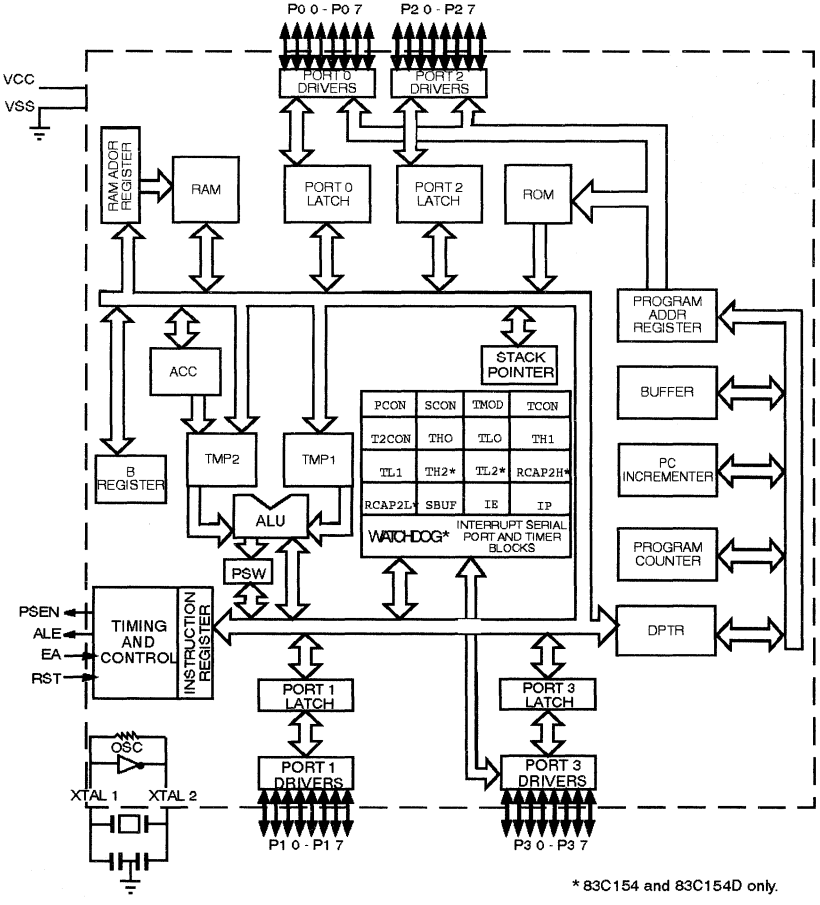


Table 1. The TEMIC C51 Family of Microcontrollers.

DEVICE NAME	ROMLESS VERSION	ROM BYTES	RAM BYTES	16-BIT TIMERS	PROCESS TYPE
80C51, TSC80C51	80C31	4K	128	2	CMOS
80C52	80C32	8K	256	3	CMOS
83C154	80C154	16K	256	3*	CMOS
83C154D		32K	256	3*	CMOS

* included watchdog and Timer 32 bits.

The devices under consideration are listed in Table 1. As it becomes unwieldy to be constantly referring to each of these devices by their individual names, we will adopt a convention of refering to them generically as 80C51s, 80C52s and 83C154s, unless a specific member of the group is being refered to, in which case it will be specifically named. The 80C51s include the TSC80C51, 80C51 and 80C31. The 80C52s are the 80C52 and 80C32. The 83C154s are the 83C154, the 80C154 and the 83C154D.

Figure 1. shows a functionnal block diagram of the 80C51s, 80C52s and 83C154s.

Special Function Registers

A map of the on-chip memory area called SFR (Special Function Register) space is shown in Figure 2. SFRs marked by parentheses are resident in the 80C52s and 83C154s but not in the 80C51s. IOCON marked by a star is only resident in the 83C154s.

Note that not all of the addresses are occupied. Unoccupied addresses are not implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have no effect.

Figure 2. SFR Map. (...) Indicates Resident in 80C52s and 83C154s, not in 80C51s.

	8 Bytes								
F8	*IOCON								FF
F0	B								F7
E8									EF
E0	ACC								E7
D8									DF
D0	PSW								D7
C8	(T2CON)		(RCAP2L)	(RCAP2H)	(TL2)	(TH2)			CF
C0									C7
B8	IP								BF
B0	P3								B7
A8	IE								AF
A0	P2								A7
98	SCON	SBUF							9F
90	P1								97
88	TCON	TMOD	TL0	TL1	TH0	TH1			8F
80	P0	SP	DPL	DPH				PCON	87

* 83C154s only.

User software should not write 1s to theses unimplemented locations, since they may be used in future TEMIC C51 products to invoke new features. In that case the reset or inactive values of the new bits will always be 0, and their active values will be 1.

The functions of the SFRs are described as below.

1.1.1. Accumulator

ACC is the Accumulator register. The mnemonics for accumulator-specific instructions, however, refer to the accumulator simply as A.

1.1.2. B Register

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

1.1.3. Program status word

The PSW register contains program status information as detailed in Figure 3.

1.1.4. Stack pointer

The Stack Pointer register is 8 bits wide. It is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the Stack Pointer is initialized to 07H after a reset. This causes the stack to begin at location 08H.

1.1.5. Data pointer

The Data Pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

1.1.6. Ports 0 to 3

P0, P1, P2 and P3 are the SFR latches of Ports 0, 1, 2 and 3, respectively.

1.1.7. Serial data buffer

The Serial Data Buffer is actually two separate registers, a transmit buffer and a receive buffer register. When data is moved to SBUF, it goes to the transmit buffer where it is held for serial transmission. (Moving a byte to SBUF is what initiates the transmission.) When data is moved from SBUF, it comes from the receive buffer.

1.1.8. Timer registers

Register pairs (TH0, TL0), (TH1, TL1), and (TH2, TL2) are the 16-bit counting registers for Timer/Counters 0, 1, and 2, respectively.

1.1.9. Capture registers

The register pair (RCAP2H, RCAP2L) are the capture register for the Timer 2 "capture mode." In this mode, in response to a transition at the 80C52's T2EX pin, TH2 and TL2 are copied into RCAP2H and RCAP2L. Timer 2 also has a 16-bit auto-reload mode, and RCAP2H and RCAP2L hold the reload value for this mode. More about Timer 2's features in Section 1.6.

1.1.10. Control registers

Special Function Registers IP, IE, TMOD, TCON, T2CON, SCON, and PCON contain control and status bits for the interrupt system, the timer/counters, and the serial port. They are described in later sections.

1.2. Oscillator and Clock Circuit

XTAL1 and XTAL2 are the input and output of a single-stage on-chip inverter, which can be configured with off-chip components as a Pierce oscillator, as shown in Figure 4. The on-chip circuitry, and selection of off-chip components to configure the oscillator are discussed in Section 1.12.

Figure 3. Crystal/Ceramic Resonator Oscillator.

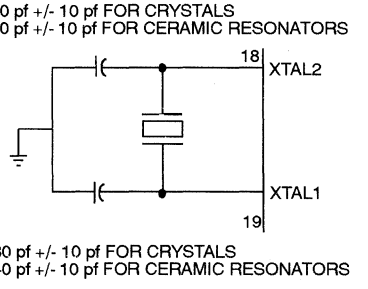


Figure 4. PSW : Program Status Work Register.

(MSB)							(LSB)
CY	AC	F0	RS1	RS0	OV	–	P

Symbol	Position	Name and Significance
CY	PSW.7	Carry flag
AC	PSW.6	Auxiliary Carry flag. (For BCD operations.)
F0	PSW.5	Flag 0 (Available to the user for general purposes.)
RS1	PSW.4	Register bank Select control bits 1 & 0. Set/cleared by software to determine working register bank (see Note).
RS0	PSW.3	
OV	PSW.2	Overflow flag.
–	PSW.1	(reserved)
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate and odd/even number of "one" bits in the accumulator, i.e., even parity.

Note : the contents of (RS1, RS0) enable the working register banks as follows
(0.0)–Bank 0 (00H-07H)
(0.1)–Bank 1 (08H-0FH)
(1.0)–Bank 2 (10H-17H)
(1.1)–Bank 3 (18H-1FH)

The oscillator, in any case, drives the internal clock generator. The clock generator provides the internal clocking signals to the chip. The internal clocking signals are at half the oscillator frequency, and define the internal phases, states, and machine cycles, which are described in the next section.

1.3. CPU Timing

A machine cycle consists of 6 states (12 oscillator periods). Each state is divided into a Phase 1 half, during which the Phase 1 clock is active, and a Phase 2 half, during which the Phase 2 clock is active. Thus, a machine cycle consists of 12 oscillator periods, numbered S1P1 (State 1, Phase 1), through S6P2 (State 6, Phase 2). Each phase lasts for one oscillator period. Each state lasts for two oscillator periods. Typically, arithmetic and logical operations take place during Phase 1 and internal register-to-register transfers take place during Phase 2.

The diagrams in Figure 5 show the fetch/execute timing referenced to the internal states and phases. Since these internal clock signals are not user accessible, the XTAL2 oscillator signal and the ALE (Address Latch Enable) signal are shown for external reference. ALE is normally activated twice during each machine cycle : once during S1P2 and S2P1, and again during S4P2 and S5P1.

Execution of one-cycle instruction begins at S1P2, when the opcode is latched into the Instruction Register. If it is a two-byte instruction, the second byte is read during S4 of the same machine cycle. If it is one-byte instruction, there is still a fetch at S4, but the byte read (which would be the next opcode), is ignored, and the Program Counter is not incremented. In any case, execution is complete at the end of S6P2. Figures 1-5A and 1-5B show the timing for a 1-byte, 1-cycle instruction and for a 2-byte, 1-cycle instruction.

Most 80C51 instructions execute in one cycle. MUL (multiply) and DIV (divide) are the only instructions that take more than two cycles to complete. They take four cycles.

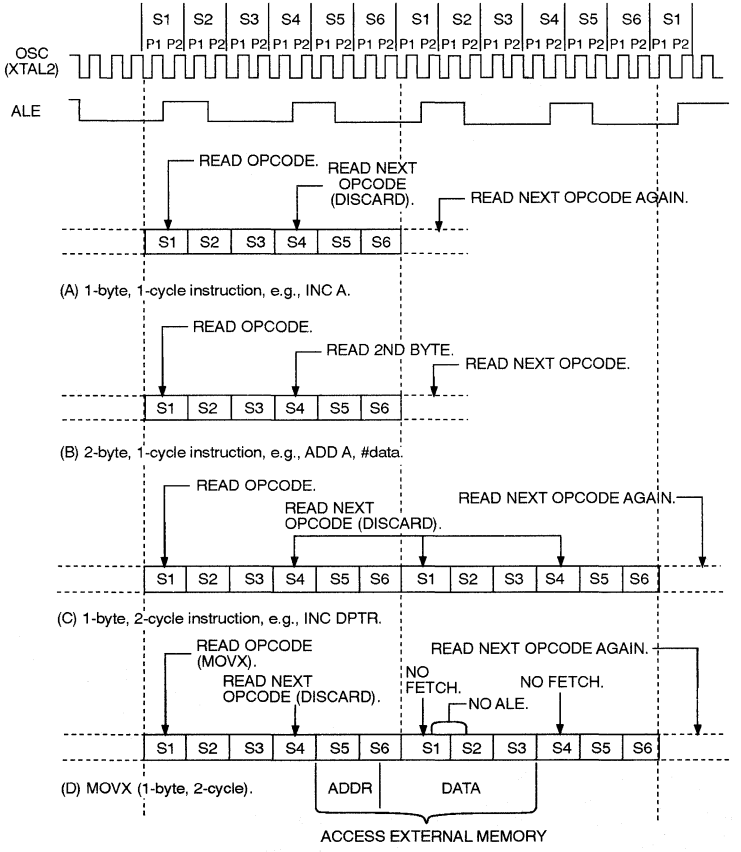
Normally, two codes bytes are fetched from Program Memory during every machine cycle. The only exception to this is when a MOVX instruction is executed. MOVX is a 1-byte 2-cycle instruction that accesses external Data Memory. During a MOVX, two fetches are skipped while the external Data Memory is being addressed and strobed. Figure 1-5C and 1-5D show the timing for a normal 1-byte, 2-cycle instruction and for a MOVX instruction.

1.4. Port Structures and Operation

All four ports in the 80C51 are bidirectional. Each consists of a latch (Special Function Register P0 through P3), an output driver, and an input buffer.

The output drivers of Ports 0 and 2, and input buffers of Port 0, are used in accesses to external memory. In this application, Port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise the Port 2 pins continue to emit the P2 SFR content.

Figure 5. 80C51 fetch/Execute Sequences.



All the Port 3 pins, and (in the 80C52) two Port 1 pins are multifunctional. They are not only port pins, but also serve the functions of various special features as listed below :

Port Pin	Alternate Function
*P1.0	T2 (Timer/Counter 2 external input)
*P1.1	T2EX (Timer/Counter 2 capture/reload trigger)
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt)
P3.3	$\overline{INT1}$ (external interrupt)
P3.4	T0 (Timer/Counter 0 external input)
P3.5	T1 (Timer/Counter 1 external input)
P3.6	$\overline{WR}$ (external Data memory write strobe)
P3.7	$\overline{RD}$ (external Data memory read strobe)

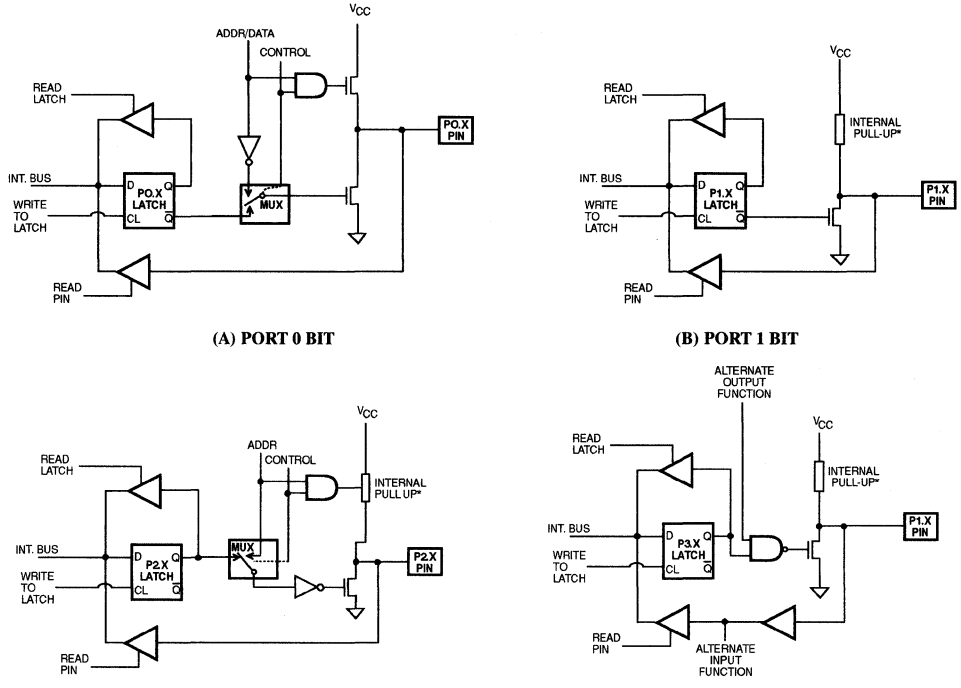
* P1.0 and P1.1 serve these alternate functions only on the 80C52, 83C154 and 83C154D.

The alternate functions can only be activated if the corresponding bit latch in the port SFR contains a 1. Otherwise the port pin is stuck at 0.

1.4.1. I/O Configurations

Figure 6. shows a functional diagram of a typical bit latch and I/O buffer in each of the four ports. The bit latch (one bit in the port's SFR) is represented as a Type D flip-flop, which will clock in a value from the internal bus in response to a "write to latch" signal from the CPU. The Q output of the flip-flop is placed on the internal bus in response to a "read latch" signal from the CPU. The level of the port pin itself is placed on the internal bus in response to a "read pin" signal from the CPU. Some instructions that read a port activate the "read latch" signal, and others activate the "read latch" signal, and others activate the "read pin" signal.

Figure 6. 80C51 Port Bit Latches and I/O Buffers.



* See Figure 7. for details of the internal pullup.

As shown in Figure 6., the output drivers of Ports 0 and 2 are switchable to an internal ADDR and ADDR/DATA bus by an internal CONTROL signal for use in external memory accesses. During external memory accesses, the P2 SFR remains unchanged, but the P0 SFR gets 1s written to it.

Also shown in Figure 6., is that if a P3 bit latch contains a 1, then the output level is controlled by the signal labeled "alternate output function." The actual P3.X pin level is always available to the pin's alternate input function, if any.

Ports 1, 2, and 3 have internal pull-ups. Ports 0 has open-drain outputs. Each I/O line can be independently used as an input or an output. (Ports 0 and 2 may not be used as general purpose I/O when being used as the ADDR/DATA BUS). To be used as an input, the port bit latch must contain a 1, which turns off the output driver FET. Then, for Ports 1, 2, and 3, the pin is pulled high by the internal pull-up, but can be pulled low by an external source.

Port 0 differs in not having internal pullups. The pullup FET in the P0 output driver (see Figure 1-6A) is used only when the Port is emitting 1s during external memory accesses. Otherwise the pullup FET is off. Consequently P0 lines that are being used as output port lines are open drain. Writing a 1 to the bit latch leaves both output FETs off, so the pin floats. In that conditions it can be used as a high-impedance input.

Because Ports 1, 2, and 3 have fixed internal pullups they are sometimes called "quasi-bidirectional" ports. When configured as inputs they pull high and will source current (IIL, in the data sheets) when externally pulled low. Port 0, on the other hand, is considered "true" bidirectional, because when configured as an input it floats.

All the port latches in the 80C51 have 1s written to them by the reset function. If a 0 is subsequently written to a port latch, it can be reconfigured as an input by writing a 1 to it.

1.4.2. Writing to a Port

In the execution of an instruction that changes the value in a port latch, the new value arrives at the latch during S6P2 of the final cycle of the instruction. However, port latches are in fact sampled by their output buffers only during Phase 1 of any clock period. (During Phase 2 the output buffer holds the value it saw during the previous Phase 1). Consequently, the new value in the port latch won't actually appear at the output pin until the next Phase 1, which be at S1P1 of the next machine cycle.

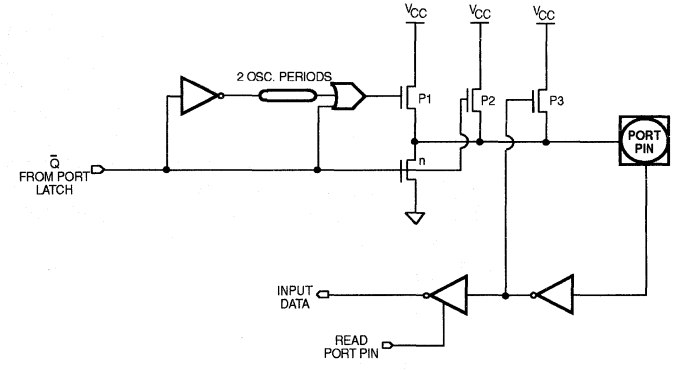
If the change requires a 0-to-1 transition in Port 1, 2, or 3, an additional pull-up is turned on during S1P1 and S1P2 of the cycle in which the transition occurs. This is done to increase the transition speed. The extra pull-up can source about 100 times the current that the normal pull-up can. It should be noted that the internal pull-ups are field-effect transistors, not linear resistors. The pull-up arrangements are shown in Figure 7.

In the CMOS versions, the pull-up consists of three pFETs. It should be noted that an n-channel FET (nFET) is turned on when a logical 1 is applied to its gate, and is turned off when a logical 0 is applied to its gate. A p-channel FET (pFET) is the opposite : it is on when its gate sees a 0, and off when its gate sees a 1.

pFET 1 in Figure 7. is the transistor that is turned on 2 oscillator periods after a 0-to-1 transition in the port latch. While it's on, it turns on pFET 3 (a weak pull-up), through the inverter. This inverter and pFET form a latch which hold the 1.

Note that if the pin is emitting a 1, a negative glitch on the pin from some external source can turn off pFET 3, causing the pin to go into a float state, pFET 2 is a very weak pull-up which is on whenever the nFET is off, in traditional CMOS style. It's only about 1/10 the strenght of pFET3. Its function is to restore a 1 to the pin in the event the pin *had* a 1 and lost it to a glitch.

Figure 7. Ports 1 and 3 CMOS Internal Pull-up Configurations.
Port 2 is similar except that it holds the strong pullup on while emitting 1s that are address bits. (See test, "Accessing External Memory".)

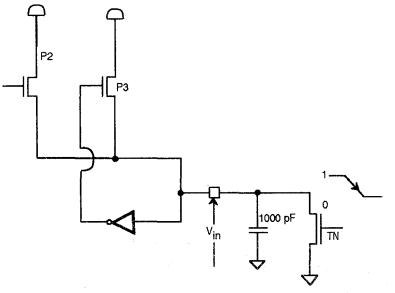


CMOS Configuration. pFET 1 is turned on for 2 osc. periods after Q makes a 1-to-0 transition. During this time, pFET 1 also turns on pFET 3 through the inverter to form a latch which holds the 1. pFET 2 is also on.

1.4.3. Port loading and interfacing

The output buffer of Ports 1, 2 and 3 can each drive 3LS TTL inputs. The pins can be driven by open-collector and open-drain outputs, but note that 0-to-1 transition will not be fast. In the CMOS device, an input 0 turns off pullup P3, leaving only the weak pullup P2 to drive the transistor. The Figure 8. shows an example where the port is driven by an open drain transistor t_N. The parasitic capacitance is equal to 100pF.

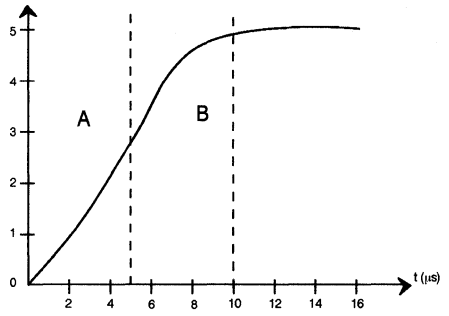
Figure 8. Port Interfacing.



The Figure 9. shows the behaviour of the port during 0-to-1 transition.

In the area A only pullup P2 sinks the capacitor and takes 5 µs to switch from 0 volt to 2 volts. In the area B, pullup P2 and P3 feed the capacitor and the time to charge the capacitor is divide roughly by ten. So this figure shows it takes some machine cycles before having a true high level during a 0-to-1 transition.

Figure 9. Port Behaviour During 0-to-1 Transition.



1.4.4. Read-Modify-Write Feature

Some instructions that read a port read the latch and others read the pin. Which ones do which ? The instructions that read the latch rather than the pin are the ones that read a value, possibly change it, and then rewrite it to the latch. These are called "read-modify-write" instructions. The instructions listed below are read-modify-write instructions. When the destination operand is a port, or a port bit, these instructions read the latch rather than the pin :

ANL	(logical AND, e.G., ANL P1,A)
ORL	(logical OR, e.g., ORL P2,A)
XRL	(logical EX-OR, e.g., XRL P3,A)
JBC	(jump if bit = 1 and clear bit, e.g., JBC P1.1, LABEL)
CPL	(complement bit, e.g., CPL P3.0)
INC	(increment, e.g., INC P2)
DEC	(decrement, e.g., DEC P2)
DJNZ	(decrement and jump if not zero, e.g., DJNZ P3, LABEL)
MOV PX.Y,C	(move carry bit to bit Y of Port X)
CLR PX.Y	(clear bit Y of Port X)
SETB PX.Y	(set bit Y of Port X)

It is not obvious that the last three instructions in this list are read-modify-write instructions, but they are. They read the port byte, all 8 bits, modify the addressed bit, then write the new byte back to the latch.

The reason that read-modify-write instructions are directed to the latch rather than the pin is to avoid a possible misinterpretation of the voltage level at the pin. For example, a port bit might be used to drive the base of a transistor. When a 1 is written to the bit, the transistor is turned on. If the CPU then reads the same port bit at the pin rather than the latch, it will read the base voltage of the transistor and interpret it as a 0. Reading the latch rather than the pin will return the correct value of 1.

Further details are given in the next chapter concerning the powerful functions of the 83C154 I/O PORTS.

1.5. Accessing External Memory

Accesses to external memory are of two types : accesses to external Program Memory and accesses to external Data Memory. Accesses to external Program Memory use signal $\overline{PSEN}$ (program store enable) as the read strobe. Accesses to external Data Memory use $\overline{RD}$ or $\overline{WR}$ (alternate function of P3.7 and P3.6) to strobe the memory.

Fetches from external Program memory always use a 16-bit address. Accesses to external Data Memory can use either a 16-bit address (MOVX @DPTR) or an 8-bit address (MOVX @Ri).

Whenever a 16-bit address is used, the high byte of the address comes out on Port 2, where it is held for the duration of the read or write cycle. Note that the Port 2 drivers use the strong pullups during the entire time that they are emitting address bits that are 1s. This is during the execution of a MOVX @DPTR instruction. During this time the Port 2 latch (the Special Function register) does not have to contain 1s, and the contents of the Port 2 SFR are not modified. If the external memory cycle is not immediately followed by another external memory cycle, the undisturbed contents of the Port 2 SFR will reappear in the next cycle.

If an 8-bit address is being used (MOVX @Ri), the contents of the Port 2 SFR remain at the Port 2 pins throughout the external memory cycle. This will facilitate paging.

In any case, the low byte of the address is time-multiplexed with the data byte on Port 0. The ADDR/DATA signal drives both FETs in the Port 0 output buffers. Thus, in this application the Port 0 pins are not open-drain outputs, and do not require external pull-ups. Signal ALE (address latch enable) should be used to capture the address byte into an external latch. The address byte is valid at the negative transitions of ALE. Then, in a write cycle, the data byte to be written appears on Port 0 just before $\overline{WR}$ is activated, and remains there until after $\overline{WR}$ is deactivated. In a read cycle, the incoming byte is accepted at Port 0 just before the read strobe is desactivated.

During any access to external memory, the CPU writes 0FFH to the Port 0 latch (the Special Function Register), thus obliterating whatever information the Port 0 SFR may have been holding.

External program Memory is accessed under two conditions :

1) Whenever signal $\overline{EA}$ is active ; or
2) Whenever the program counter (PC) contains a number that is larger than 0FFFH (1FFFH for the 80C52, 3FFFH for the 83C154 and 7FFFH for the 83C154D.

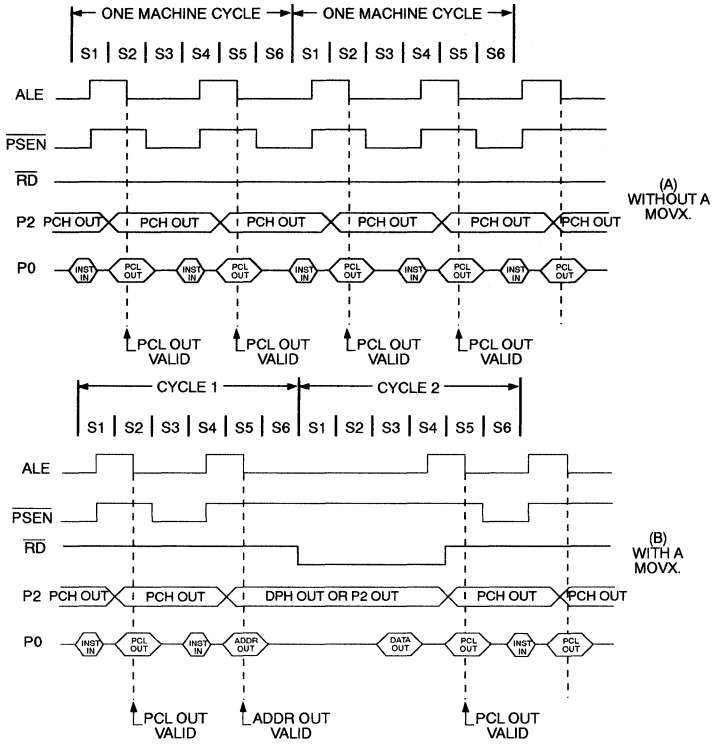
This requires that the ROMless versions have $\overline{EA}$ wired low to enable the lower 4K (8K for the 80C32, 16K for the 80C154 and 32K for the 80C154D) program bytes to be fetched from external memory.

When the CPU is executing out of external Program Memory, all 8 bits of Port 2 are dedicated to an output function and may not be used for general purpose I/O. During external program fetches they output the high byte of the PC. During this time the Port 2 drivers use the strong pullups to emit PC bits that are 1s.

$\overline{PSEN}$

The read strobe for external fetches is $\overline{PSEN}$. $\overline{PSEN}$ is not activated for internal fetches. When the CPU is accessing external Program Memory, $\overline{PSEN}$ is activated twice every cycle (except during a MOVX instruction) whether or not the byte fetched is actually needed for the current instruction. When $\overline{PSEN}$ is activated its timing is not the same as $\overline{RD}$. A complete $\overline{RD}$ cycle, including activation and deactivation of ALE and $\overline{RD}$, takes 12 oscillator periods. A complete $\overline{PSEN}$ cycle, including activation and deactivation of ALE and $\overline{PSEN}$, takes 6 oscillator periods. The execution sequence for these two types of read cycles are shown in Figure 10 for comparison.

Figure 10. External Program Memory Execution.



ALE

The main function of ALE is to provide a properly timed signal to latch the low byte of an address from P0 to an external latch during fetches from external Program Memory. For that purpose ALE is activated twice every machine cycle. This activation takes place even when the cycle involves no external fetch. The only time an ALE pulse doesn't come out is during an access to external Data Memory. The first ALE of the second cycle of a MOVX instructions is missing (see Figure 10.). Consequently, in any system that does not use external Data Memory, ALE is activated at a constant rate of 1/6 the oscillator frequency, and can be used for external clocking or timing purposes.

Overlapping External Program and Data Memory Spaces

In some applications it is desirable to execute a program from the same physical memory that is being used to store data. In the 80C51, the external Program and Data Memory spaces can be combined by ANDing $\overline{PSEN}$ and $\overline{RD}$. A positive-logic AND of these two signals produces an active-low read strobe that can be used for the combined physical memory. Since the $\overline{PSEN}$ cycle is faster than the $\overline{RD}$ cycle, the external memory needs to be fast enough to accomodate the $\overline{PSEN}$ cycle.

1.6. Timer/Counters

The 80C51 has two 16-bit timer/counter registers : Timer 0 and Timer 1. The 80C52, 83C154 and 83C154D have these two plus one more : Timer 2. All three can be configured to operate either as timers or event counters.

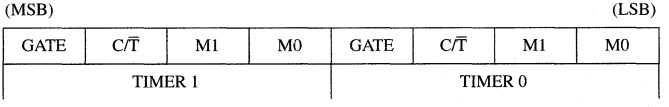
In the "timer" function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the "counter" function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0, T1 or (in the 80C52, 83C154 and 83C154D) T2. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

In addition to the "timer" or "counter" selection, Timer 0 and Timer 1 have four operating modes from which to select. Timer 2, in the 80C52, 83C154 and 83C154D has three modes of operation : "capture," "auto-reload" and "baud rate generator."

1

Figure 11. TMOD : Timer/Counter Mode Control Register.



GATE	Gating control When set. Timer/counter "x" is enabled only while "INTx" pin is high and "TRx" control pin is set. When cleared Timer "x" is enabled whenever "TRx" control bit is set.
C/T	Timer or Counter Selector Cleared for Timer operation (input from internal system clock.) Set for Counter operation (input from "Tx" input pin).

M1	M0	Operatong Mode
0	0	MCS-48 Timer "TLx" serves as five-bit prescaler.
0	1	16 bit Timer/Counter "THx" and "TLx" are cascaded ; there is no prescaler
1	0	8 bit auto-reload timer-counter "THx" holds a value which is to be reloaded into "TLx" each timer it overflows.
1	1	(Timer 0) TL0 is an eight bit timer counter-controlled by the standard Timer 0 control bits TH0 is an eight-bit timer only controlled by Timer 1 control bits.
1	1	(Timer 1) Timer-counter 1 stopped.

Timer 0 and Timer 1

These timer/counter are present in both the 80C51, the 80C52, the 83C154 and the 83C154D. The "timer" or "counter" function is selected by control bits C/$\overline{T}$ in the Special Function Register TMOD (Figure 11.). These two timer/counters have four operating modes, which are selected by bit-pairs (M1, M0) in TMOD. Modes 0, 1, and 2 are the same for both timer/counters. Modes 3 is different. The four operating modes are described below.

Mode 0

Putting either Timer into mode 0 makes it look like an 8048 Timer, which is an 8-bit counter with a divide-by-32 prescaler. Figure 12. shows the mode 0 operation as it applies to Timer 1.

In this mode, the timer register is configured as a 13-bit register. As the count rolls over from all 1s to all 0s, it sets the timer interrupt flag TF1. The counted input is enabled to the Timer when TR1 = 1 and either GATE = 0 or $\overline{INT1}$ = 1. (Setting GATE =1 allows the Timer to be controlled by external input $\overline{INT1}$, to facilitate pulse width measurements). TR1 is a control bit in the Special Function register TCON (Figure 1-10). GATE is in TMOD.

The 13-bit register consists of all 8 bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate and should be ingored. Setting the run flag (TR1) does not clear the registers.

Mode 0 operation is the same for Timer 0 as for Timer 1. Substitute TR0, TF0 and $\overline{INT0}$ for the corresponding Timer 1 signals in Figure 12. There are two different GATE bits, one for Timer 1 (TMOD.7) and one for Timer 0 (TMOD.3).

Mode 1

Mode 1 is the same as Mode 0, except that the Timer register is being run with all 16 bits.

Mode 2

Mode 2 configures the timer register as an 8-bit counter (TL1) with automatic reload, as shown in Figure 14. Overflow from TL1 not only sets TF1, which is preset by sofware. The reload leaves TH1 unchanged.

Mode 2 operation is the same for Timer/Counter 0.

Mode 3

Timer 1 in Mode 3 simply holds its count. The effect is the same as setting TR1 = 0.

Figure 12. Timer/Counter 1 Mode 0 : 13-bit Counter.

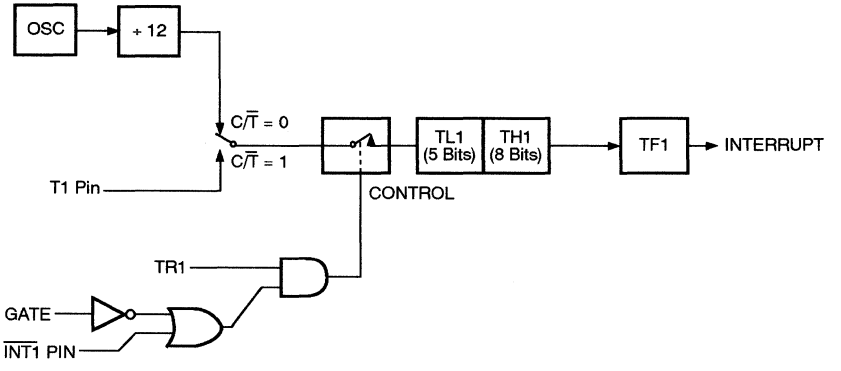


Figure 13. TCON : Timer/Counter Control Register.

(MSB) (LSB)

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Symbol	Position	Name and Significance
TF1	TCON.7	Timer 1 overflow Flag. Set by hardware on timer/counter overflow. Cleared by hardware when processor vectors to interrupt routine.
TR1	TCON.6	Timer 1 Run control bit. Set/cleared by software to turn timer/counter on/off.
TF0	TCON.5	Timer 0 overflow Flag. Set by hardware on timer/counter overflow. Cleared by hardware when processor vectors to interrupt routine.
TR0	TCON.4	Timer 0 Run control bit. Set/cleared by software to turn timer/counter on/off.

Symbol	Position	Name and Significance
IE1	TCON.3	Interrupt 1 Edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.
IT1	TCON.2	Interrupt 1 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
IE0	TCON.1	Interrupt 0 Edge flag. Set by hardware when external interrupt edge detected. Cleared when interrupt processed.
IT0	TCON.0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.

Timer 0 in Mode 3 establishes TL0 and TH0 as two separate counters. The logic for Mode 3 on Timer 0 is shown in Figure 15. TL0 uses the Timer 0 control bits : C/$\overline{T}$, GATE, TR0, $\overline{INT0}$, and TF0. TH0 is locked into a timer function (counting machine cycles) and takes over the use of TR1 and TF1 from Timer 1. Thus TH0 now controls the "Timer 1" interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer or counter. With Timer 0 in Mode 3, an 80C51 can look like it has three timer/counters, and an 80C52, an 83C154 and 83C154D, like it has four. When Timer 0 is in Mode 3, Timer 1 can be turned on and off by switching it out of and into its own Mode 3, or can still be used by the serial port as a baud rate generator, or in fact, in any application not requiring an interrupt.

Timer 2

Timer 2 is a 16-bit timer/counter which is present only in the 80C52, 83C154 and 83C154D. Like Timers 0 and 1, it can operate either as a timer or as an event counter.

Figure 14. Timer/Counter 1 Mode 2 : 8-bit Auto-reload.

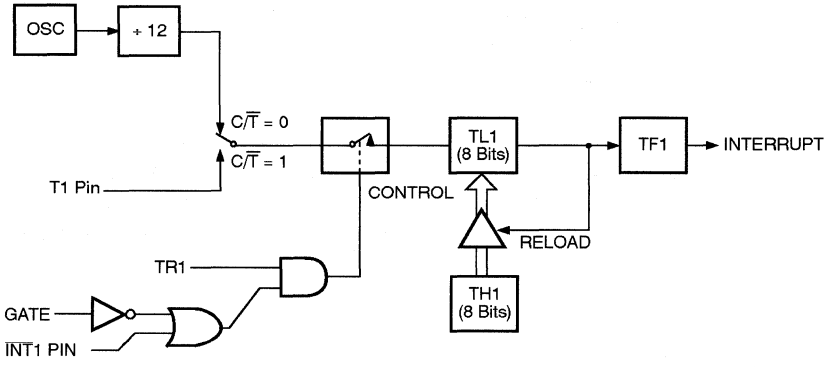


Figure 15. Timer/Counter 0 Mode 3 : Two 8-bit Counters.

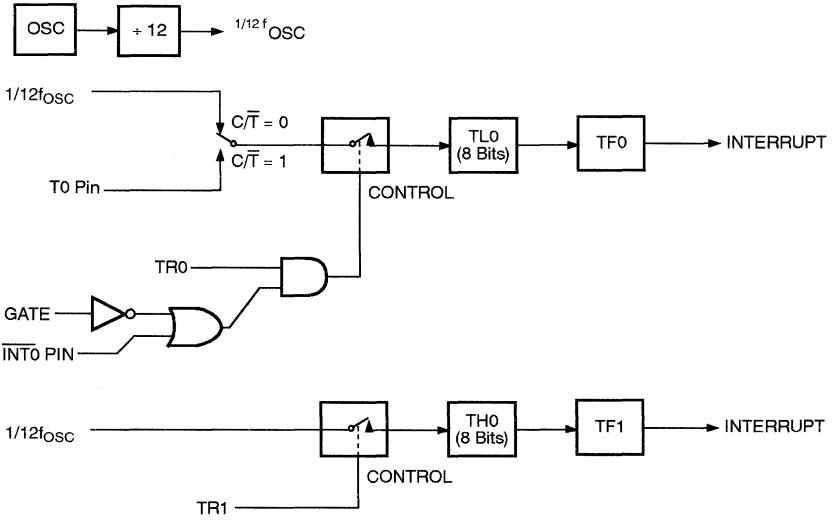


Figure 16. T2CON : Timer/Counter 2 Control Register.

(MSB)							(LSB)
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

Symbol	Position	Name and Significance
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 or TCLK = 1
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/$\overline{T2}$	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered).
CP/$\overline{RL2}$	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto–reload on Timer 2 overflow.

This is selected by bit C/$\overline{T2}$ in the Special Function Register T2CON (Figure 16). It has three operating modes : "capture," "autoload" and "baud rate generator," which are selected by bits in T2CON as shown in Table 2.

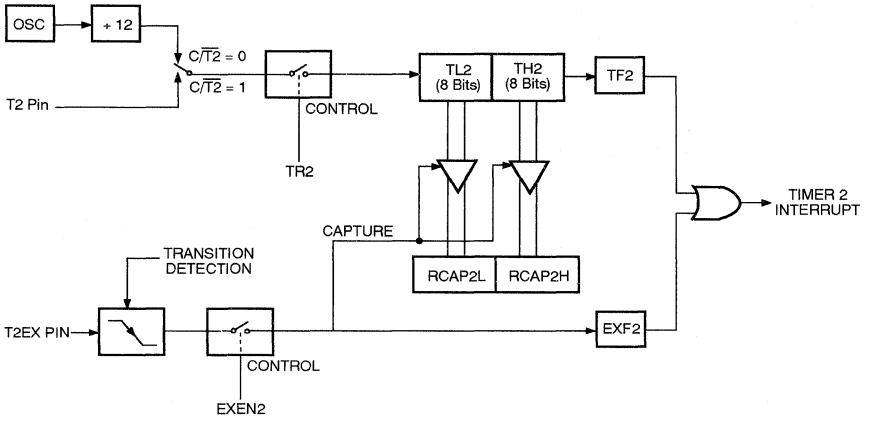
Table 2. Timer 2 Operating Modes.

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16–bit auto–reload
0	1	1	16–bit capture
1	X	1	baud rate generator
X	X	0	(off)

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16-bit timer or counter which upon overflowing sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. (RCAP2L and RCAP2H are new Special Function Registers in the 80C52, 83C154 and 83C154D. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt.

The capture mode is illustrated in Figure 17.

Figure 17. Timer 2 in Capture Mode.



In the auto-reload mode there are again two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then when Timer 2 rolls over it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16-bit reload and set EXF2.

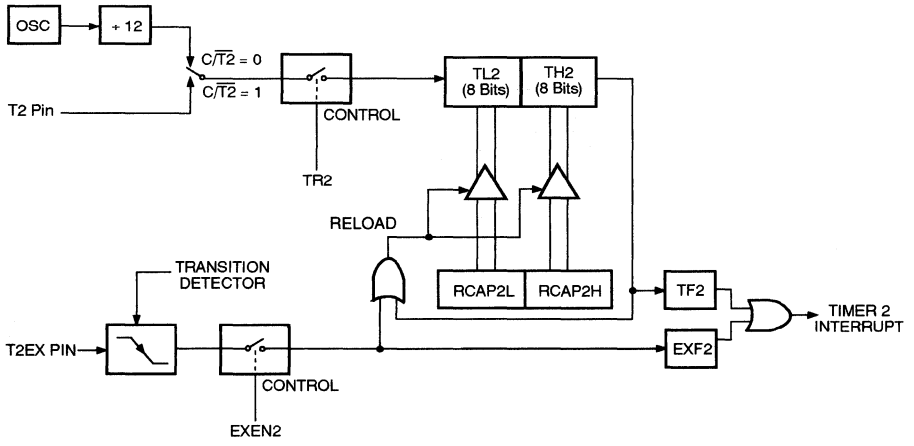
The auto-reload mode is illustrated in Figure 18.

The baud rate generator mode is selected by RCLK = 1 and/or TCLK = 1. It will be described in conjunction with the serial port.

1.7. Serial Interface (80C51 and 80C52 only)

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previoulsy received byte has been read from the receive register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost). The serial port receive and transmit registers are both accessed at Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

Figure 18. Timer 2 in Auto-Reload Mode.



The serial port can operate in 4 modes :

Mode 0 : Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted/received : 8 data bits (LSB first). The baud rate is fixed at 1/12 the oscillator frequency.

Mode 1 : 10 bits are transmitted (through TXD) or received (through RXD) : a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.

Mode 2 : 11 bits are transmitted (through TXD) or received (through RXD) : a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Function register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency.

Mode 3 : 11 bits are transmitted (through TXD) or received (through RXD) : a start bit (0), 8 data bits (LSB first), a programmable 9th data bit and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except the baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in Mde 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

1.7.1. Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor, communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = 1. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows.

When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is 1 in an address byte and 0 in a data byte. With SM2 = 1, no slave will be interrupt by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't being addressed leaved their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, and in Mode 1 can be used to check the validity of the stop bit. In a Mode 1 reception, if SM2 = 1, the receive interrupt will not be activated unless a valid stop bit is received.

Serial port Control Register

The serial port control and status register is the Special Function Register SCON, shown in Figure 19. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupts bits (TI and RI).

Figure 19. SCON : Serial Port Control Register.

(MSB)							(LSB)
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

where SM0, SM1 specify the serial port mode, as follows :

SM0	SM1	Mode	Description	Baud Rate
0	0	0	shift register	$f_{OSC}/12$
0	1	1	8 bit UART	variable
1	0	2	9 bit UART	$f_{OSC}/64$ or $f_{OSC}/32$
1	1	3	9 bit UART	variable

- SM2 enables the multiprocessor communication feature in modes 2 and 3. In mode 2 or 3, if SM2 is set to 1 then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit is not received. In mode 0, SM2 should be 0.
- REN enables serial reception. Set by software to enable reception. Clear by software to disable reception.
- TB8 is the 9th data bit that will be transmitted in modes 2 and 3. Set or clear by software as desired.
- RB8 in modes 2 and 3, is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
- TI is transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
- RI is receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

1.7.2. Baud Rates

The baud rate in Mode 0 is fixed :

$$\text{Mode 0 Baud Rate} = \frac{\text{Oscillator Frequency}}{12}$$

The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If SMOD = 0 (which is its value on reset), the baud rate is 1/64 the oscillator frequency. If SMOD = 1, the baud rate is 1/32 the oscillator frequency.

$$\text{Mode 2 Baud Rate} = \frac{2^{SMOD}}{64} \times (\text{Oscillator Frequency})$$

In the 80C51, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate. In the 80C52, 83C154 and 83C154D, these baud rates can be determined by Timer 1, or by Timer 2, or by both (one for transmit and the other for receive).

1.7.3. Using Timer 1 to Generate Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows :

$$\text{Modes 1, 3 Baud rate} = \frac{2^{SMOD}}{32} \times (\text{Timer 1 Overflow rate})$$

The Timer 1 interrupt should be disabled in this application. The Timer itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In the most typical applications, it is configured for "timer" operation, in the auto-reload mode (high nibble of TMOD = 0010B). In that case, the baud rate is given by the formula

$$\text{Modes 1, 3 Baud rate} = \frac{2^{SMOD}}{32} \times \frac{\text{Oscillator Frequency}}{12 \times [256 - (TH1)]}$$

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload.

Figure 20. lists various commonly used baud rates and how they can be obtained from Timer 1.

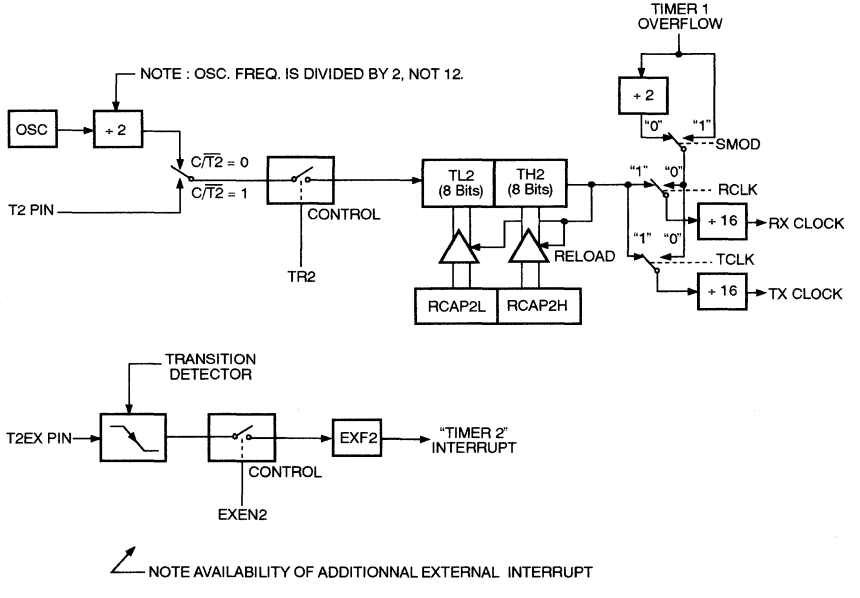
Figure 20. Timer 1 Generated Commonly Used Baud Rates.

Baud Rate	f_{OSC}	SMOD	TIMER 1		
			C/T	Mode	Reload Value
MODE 0 MAX : 1MHZ	12 MHZ	x	x	x	x
MODE 2 MAX : 375K	12 MHZ	1	x	x	x
MODES 1,3 : 62.5K	12 MHZ	1	0	2	FFH
19.2K	11.059 MHZ	1	0	2	FDH
9.6K	11.059 MHZ	0	0	2	FDH
4.8K	11.059 MHZ	0	0	2	FAH
2.4K	11.059 MHZ	0	0	2	F4H
1.2K	11.059 MHZ	0	0	2	E8H
137.5	11.986 MHZ	0	0	2	1DH
110	6 MHZ	0	0	2	72H
110	12 MHZ	0	0	1	FEEBH

1.7.4. Using Timer 2 to Generate Baud Rates

In the 80C52, 83C154 and 83C154D, Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK in T2CON (Figure 16.). Note then the baud rates for transmit and receive can be simultaneously different. Setting RCLK and/or TCLK puts Timer 2 into its baud rate generator mode, as shown in Figure 21.

Figure 21. Timer 2 in Baud Rate Generator Mode.



The baud rate generator mode is similar to the auto-reload mode, in that a rollower in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registes RCAP2H and RCAP2L, which are preset by software.

Now, the baud rates in Modes 1 and 3 are determined by Timer 2's overflow rate as follows :

$$\text{Modes 1, 3 Baud Rate} = \frac{\text{Timer 2 Overflow rate}}{16}$$

The Timer can be configured for either "timer" or "counter" operation. In the most typical applications, it is configured for "timer" operation ($C/\overline{T2} = 0$). "Timer" operation is a little different for Timer 2 when it's being used as a baud rate generator. Normally as a timer it would increment every machine cycle (thus at 1/12 the oscillator frequency). As a baud rate generator, however, it increment every state time (thus at 1/2 the oscillator frequency). In that case the baud rate is given by the formula

$$\frac{\text{Modes 1, 3}}{\text{Baud rate}} = \frac{\text{Oscillator Frequency}}{32 \times [65536-(\text{RCAP2H, RCAP2L})]}$$

where (RCAP2H, RCAP2L) is the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Timer 2 as a baud rate generator is shown in Figure 21. This Figure is valid only if RCLK + TCLK = 1 in T2CON. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Therefore, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Note too, that if EXEN2 is set, a 1-to-0 transition in T2EX will set EXF2 but will not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). Thus when Timer 2 is in use as a baud rate generator, T2EX can be used as an extra external interrupt, if desired.

It should be noted that when Timer 2 is running (TR2 = 1) in "timer" function in the baud rate generator mode, one should not try to read or write TH2 or TL2. Under these conditions the Timer is being incremented every state time, and the results of a read or write may not be accurate. The RCAP registers may be read, but shouldn't be written to, because a write might overlap a reload and cause write and/or reload errors. Turn the Timer off (clear TR2) before accessing the Timer 2 or RCAP registers, in this case.

More About Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted/received : 8 data bits (LSB first). The baud rate is fixed at 1/12 the oscillator frequency.

Figure 22. shows a simplified functional diagram of the serial port in mode 0, and associated timing.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal at S6P2 also loads a 1 into the 9th bit position of the transmit shift register and tells the TX Control block to commence a transmission. The internal timing is such that one full machine cycle will elapse between "write to SBUF", and activation of SEND.

SEND enables the output of the shift register to the alternate output function line of P3.0, and also enables SHIFT CLOCK to the alternate output function line of P3.1. SHIFT CLOCK is low during S3, S4, and S5 of every machine cycle, and high during S6, S1 and S2. At S6P2 of every machine cycle in which SEND is active, the contents of the transmit shift register are shifted to the right one position.

As data bits shift out to the right, zeros come in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position, is just to the left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control block to do one last shift and then deactivate SEND and set T1. Both of these actions occur at S1P1 of the 10th machine cycle after "write to SBUF."

Reception is initiated by the condition REN = 1 and RI = 0. At S6P2 of the next machine cycle, the RX Control unit writes the bits 11111110 to the receive shift register, and in the next clock phase activates RECEIVE.

RECEIVE enables SHIFT CLOCK to the alternate output function line of P3.1. Shift CLOCK makes transitions at S3P1 and S6P1 of every machine cycle. At S6P2 of every cycle in which RECEIVE is active, the contents of the receive shift register are shifted to the left one position. The value that comes in from the right is the value that was sampled at the P3.0 pin at S5P2 of the same machine cycle.

As data bits come in from the right, 1s shift out to the left. When the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift and load SBUF. At S1P1 of the 10th machine cycle after the write to SCON that cleared RI, RECEIVE is cleared and RI is set.

More About Mode 1

Ten bits are transmitted (through TXD), or received (through RXD) : a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in SCON. In the 80C51 the baud rate is determined by the Timer 1 overflow rate. In the 80C52, 83C154 and 83C154D it is determined either by the Timer 1 overflow rate, or the Timer 2 overflow rate, or both (one for transmit and the other for receive).

Figure 23. shows a simplified functional diagram of the serial port in Mode 1, and associated timings for transmit and receive.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads a 1 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission actually commences at S1P1 of the machine cycle following the next rollower in the divide-by-16 counter. (Thus, the bit

times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal).

The transmission begins with activation of $\overline{\text{SEND}}$, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The fisrt shift pulse occurs one bit time after that.

As data bits shift out to the right, zeros are clocked in from the left. When the MSB of the data byte is at the output position of the shift register, then the 1 that was initially loaded into the 9th position is just to the left of the MSB, and all positions to the left of that contain zeroes. This condition flags the TX Control unit to do one last shift and then deactivate $\overline{\text{SEND}}$ and set TI. This occurs at the 10th divide-by-16 rollover after "write to SBUF".

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever baud rate has been established. When a transition is detected, the divide-by-16 counter is immediately reset, and 1FFH is written into the input shift register. Resetting the divide-by-16 counter aligns its rollovers with the boundaries of the incoming bit times.

Figure 22. Serial Port Mode 0.

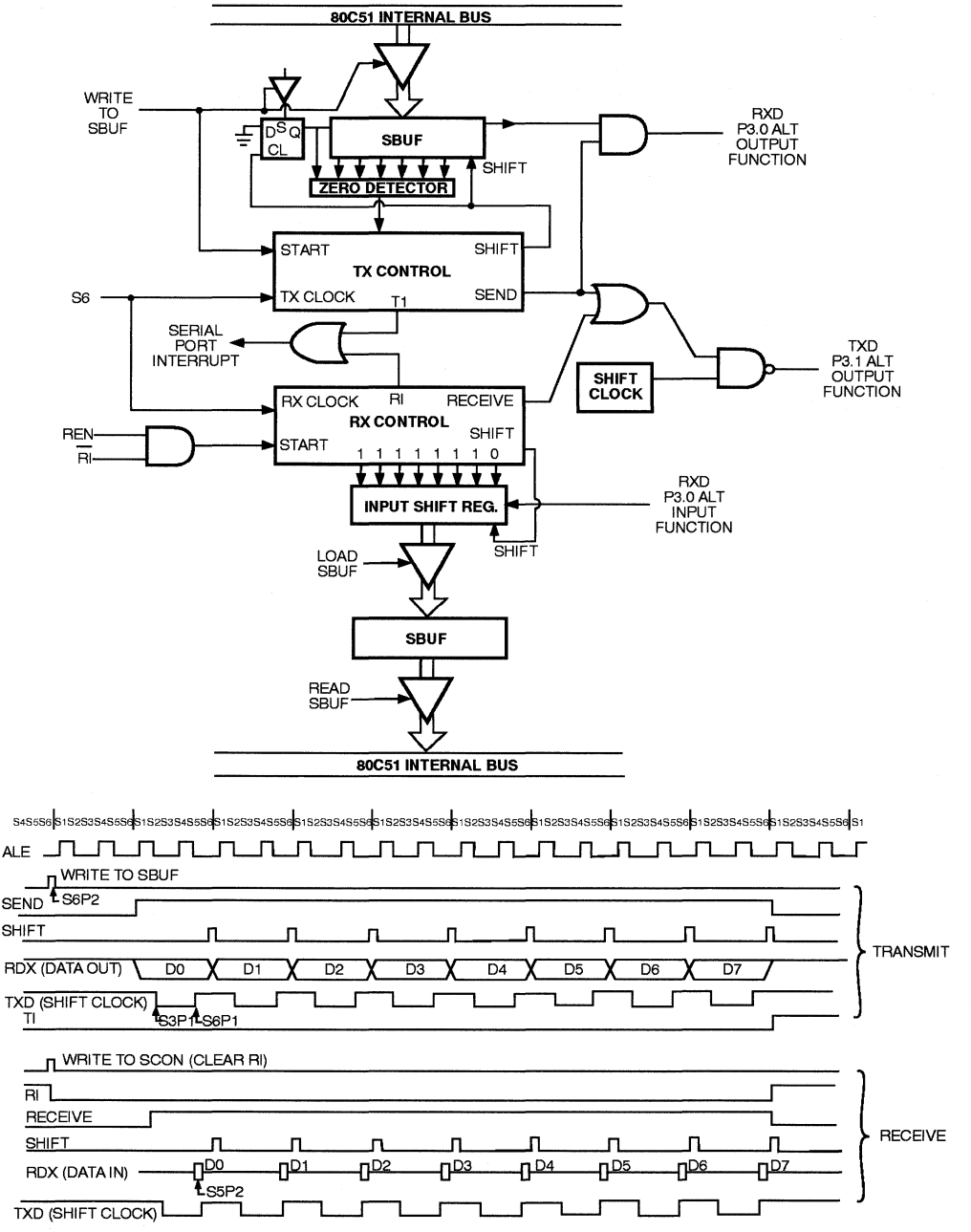
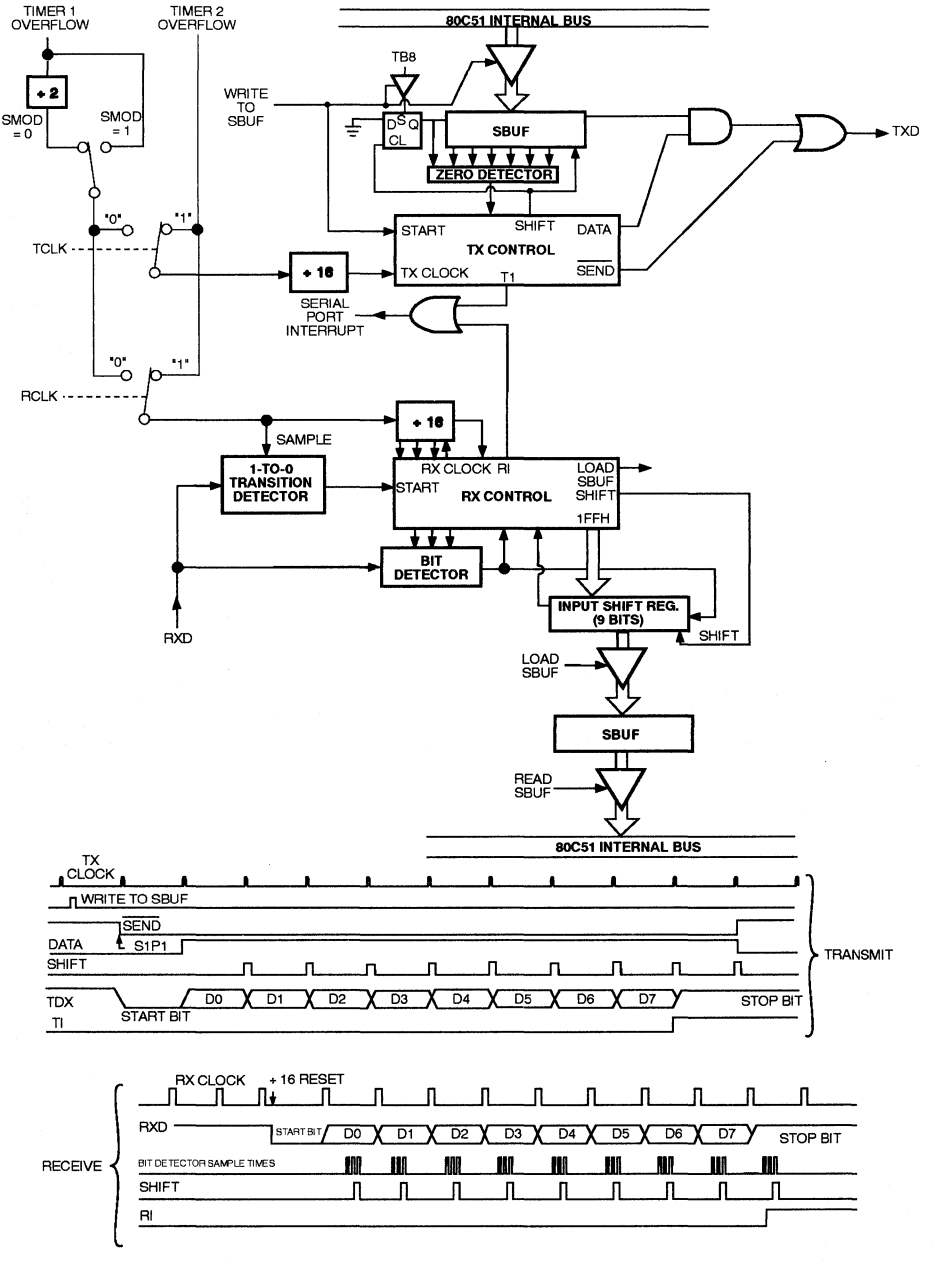


Figure 23. Serial Port Mode 1. TCLK, RCLK, and Timer 2 are present in the 80C32/80C52, 80C154/83C154 and 83C154D.



The 16 states of the counter divide each bit time into 16ths. At the 7th, 8th, and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. This is done for noise rejection. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. This is to provide rejection of false start bits. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register, (which in mode 1 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUFF and RB8, and set RI. Will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated.

1) RI = 0, and
2) Either SM2 = 0, or the received stop bit = 1

If either of these two confitions is not met, the received frame is irretrievably lost. If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. At this time, whether the above conditions are met or not, the unit goes back to looking for a 1-to-0 transition in RXD.

More About Modes 2 and 3

Eleven bits are transmitted (through TXD), or received (through RXD) : a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit goes into RB8 is SCON. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency in mode 2. Mode 3 may have a variable baud rate generated from either Timer 1 or 2 depending on the state of TCLK and RCLK.

Figures 1-24 A and B show a functional diagram of the serial port in modes 2 and 3. The receive portion is exactly the same as in mode 1. The transmit portion differs from mode 1 only in the 9th bit of the transmit shift register.

Transmission is initiated by any instruction that uses SBUF as a destination register. The "write to SBUF" signal also loads TB8 into the 9th bit position of the transmit shift register and flags the TX Control unit that a transmission is requested. Transmission commences at S1P1 of the machine cycle following the next rollover in the divide-by-16 counter. (Thus, the bit times are synchronized to the divide-by-16 counter, not to the "write to SBUF" signal.)

The transmission begins with activation of SEND, which puts the start bit at TXD. One bit time later, DATA is activated, which enables the output bit of the transmit shift register to TXD. The first shift pulse occurs one bit time after that. The first shift clocks a 1 (the stop bit) into the 9th bit position of the shift register. Thereafter, only zeroes are clocked in. Thus, as data bits shift out to the right, zeroes are clocked in from the left. When TB8 is at the output position of the shift register, then the stop bit is just to the left of TB8, and all positions to the left of that contain zeroes. This condition flags the TX Control unit to do one last shift and then deactivate $\overline{\text{SEND}}$ and set TI. This occurs at the 11th divide-by-16 rollover after "write to SBUF".

Reception is initiated by a detected 1-to-0 transition at RXD. For this purpose RXD is sampled at a rate of 16 times whatever is detected, the divide-by-16 counter is immediately reset, and 1FFH is written to the input shift register.

At the 7th, 8th and 9th counter states of each bit time, the bit detector samples the value of RXD. The value accepted is the value that was seen in at least 2 of the 3 samples. If the value accepted during the first bit time is not 0, the receive circuits are reset and the unit goes back to looking for another 1-to-0 transition. If the start bit proves valid, it is shifted into the input shift register, and reception of the rest of the frame will proceed.

As data bits come in from the right, 1s shift out to the left. When the start bit arrives at the leftmost position in the shift register (which in modes 2 and 3 is a 9-bit register), it flags the RX Control block to do one last shift, load SBUF and RB8, and set RI. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated :

1) RI = 0, and
2) Either SM2 = 0 or the received 9th data bit = 1

If either of these conditions is not met, the received frame is irretrievably lost, and RI is not set. If both conditions are met, the received 9th data bit goes into RB8, and the first 8 data bits go into SBUF. One bit time later, whether the above conditions were met or not, the unit goes back to looking for a 1-to-0 transition at the RXD input.

Note that the value of the received stop bit is irrelevant to SBUF, RB8, or RI.

Figure 24. Serial Port Mode 2.

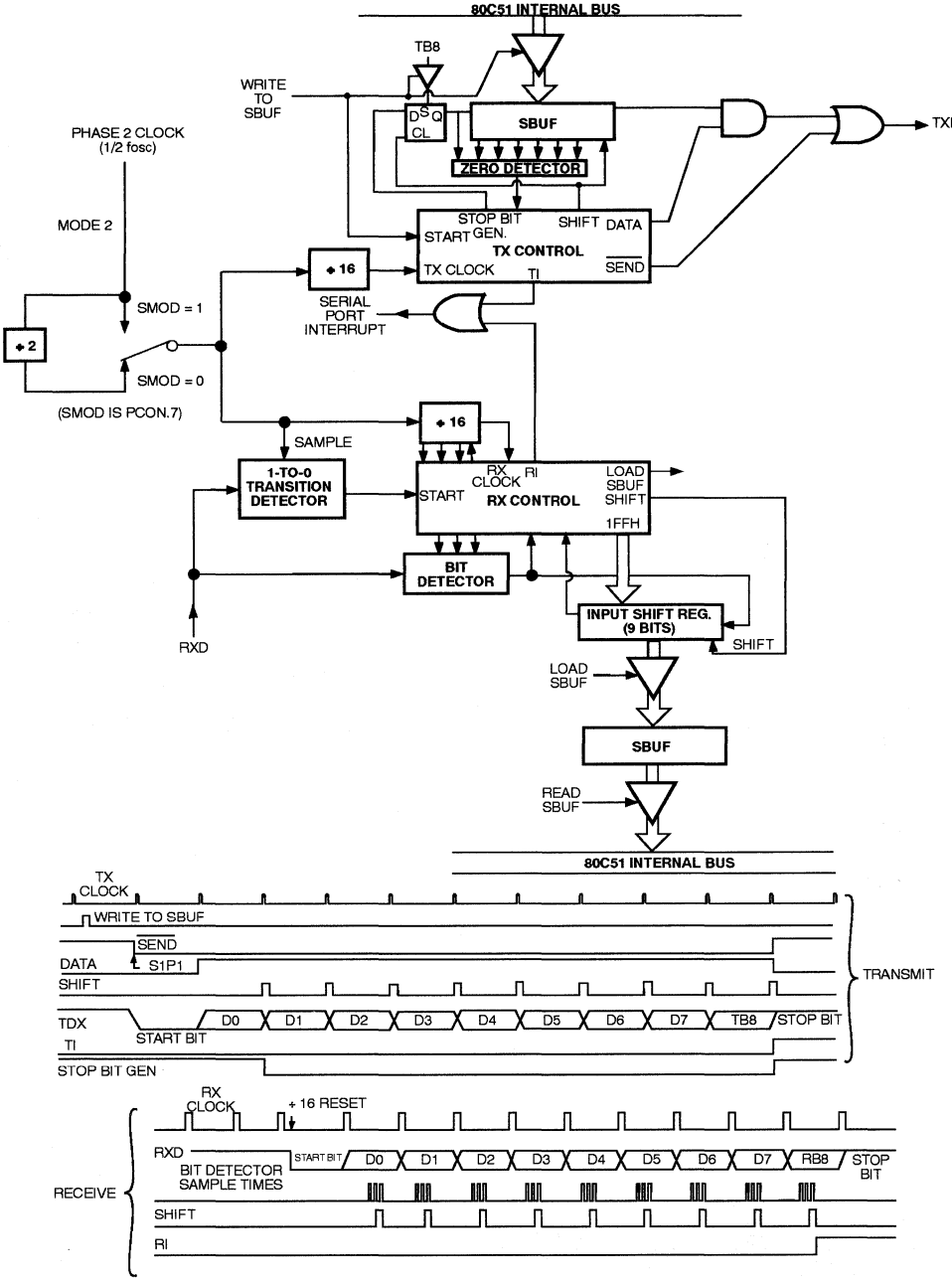
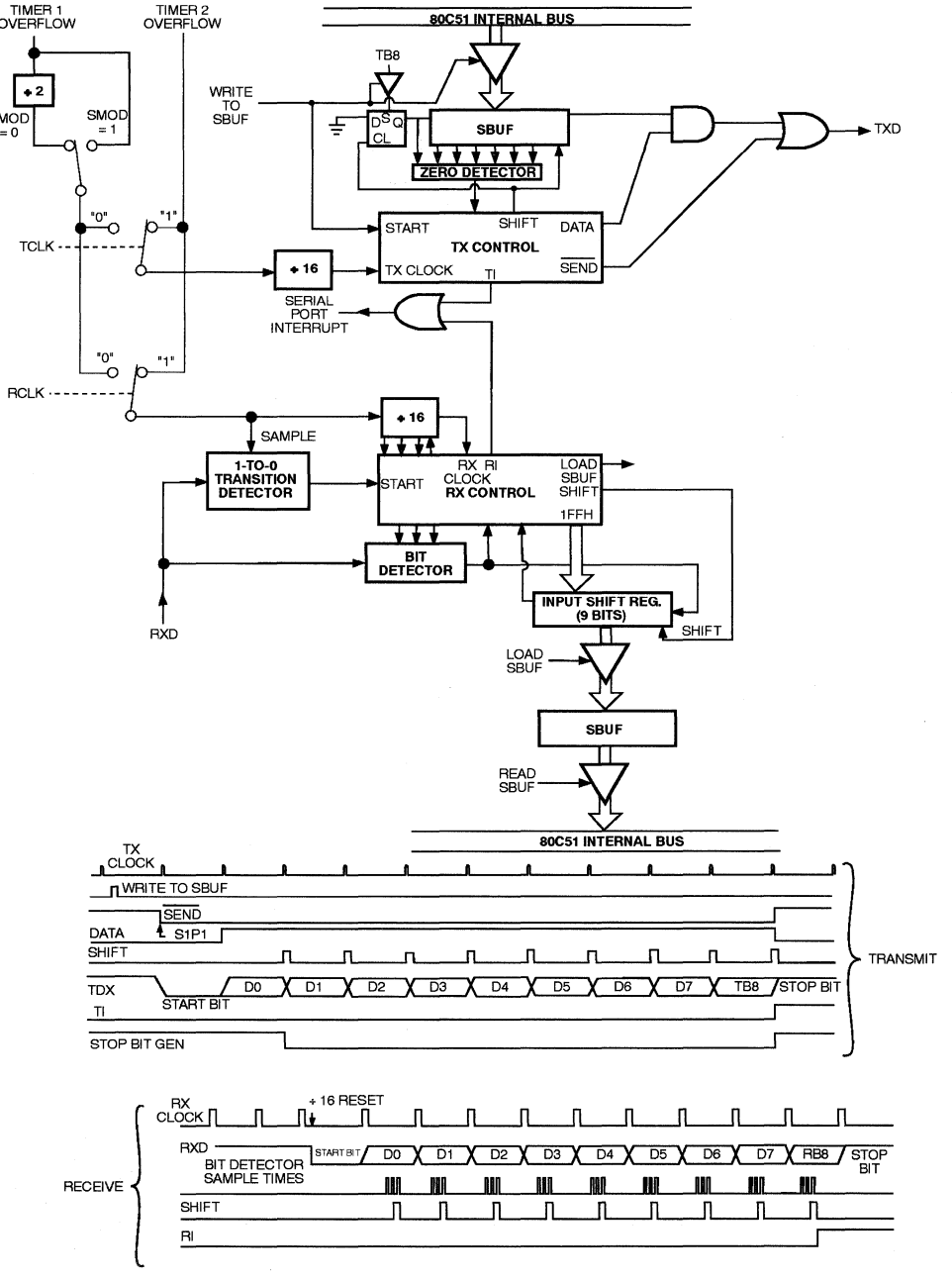


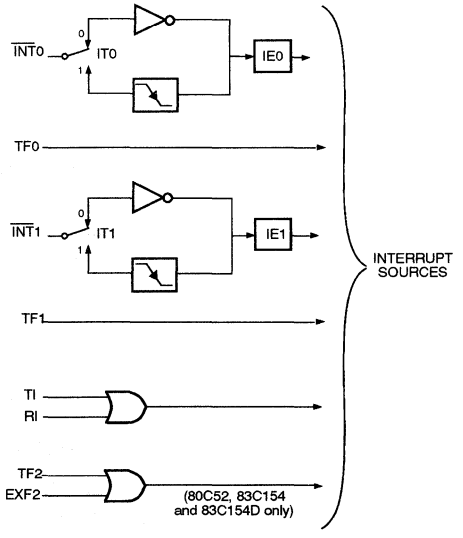
Figure 25. Serial Port Mode 3. TCLK, RCLK and Timer 2 are present in the 80C32/80C52, 80C154/83C154 and in the 83C154D.



1.8. Interrupts

The 80C51 provides 5 interrupt sources. The 80C52 83C154 and 83C154D provide 6. Theses are shown in Figure 25.

Figure 26. TEMIC C51 Interrupt Sources.



The external interrupts $\overline{INT0}$ and $\overline{INT1}$ can each be either level-activated or transition-activated, depending on bits IT0 and IT1 in Register TCON. The flags that actually generate these interrupts are bits IE0 and IE1 in TCON. When an external interrupt is generated, the flag that generated it is cleared by the hardware when the service routine is vectored to only if the interrupt was transition-activated. If the interrupt was level-activated, then the external requesting source is what controls the request flag, rather than the on-chip hardware.

The Timer 0 and Timer 1 Interrupts are generated by TF0 and TF1, which are set by a rollover in their respective timer/counter registers (except see Section 1.6 for Timer 0 in mode 3). When a timer interrupt is generated, the flag that generated it is cleared by the on-chip hardware when the service routine is vectored to.

The Serial Port Interrupt is generated by the logical OR of RI and TI. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine will normally have to determine whether it was RI or TI that generated the interrupt, and the bit will have to be cleared in software.

In the 80C52, 83C154 and 83C154D, the Timer 2 Interrupt is generated by the logical OR of TF2 and EXF2. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt, and the bit will have to be cleared in software.

All of the bits that generate interrupts can be set or cleared by sofware, with the same result as though it had been set or cleared by hardware. That is, interrupts can be generated or pending interrupts can be canceled in sofware.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE (Figure 26.). Note that IE contains also a global disable bit, EA, which disables all interrupts at once.

Figure 27. IE : Interrupt Enable Register.

(MSB) (LSB)

EA	X	ET2	ES	ET1	EX1	ET0	EX0

Symbol	Position	Function
EA	IE.7	disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enables bit.
–	IE.6	reserved.
ET2	IE.5	enables or disables the Timer 2 overflow or capture interrupt. If ET2 = 0, the Timer 2 interrupt is disabled.
ES	IE.4	enables or disables the Serial Port interrupt is disabled.
ET1	IE.3	enables or disables the Timer 1 Overflow interrupt. If ET1 = 0, the Timer 1 interrupt is disabled.
EX1	IE.2	enables or disables External Interrupt 1. If EX1 = 0, External interrupt 1 is disabled.
ET0	IE.1	enables or disables the Timer 0 Overflow interrupt. If ET0 = 0, the Timer 0 interrupt is disabled.
EX0	IE.0	enables or disables External Interrupt 0. If EX0 = 0, External Interrupt 0 is disabled.

Priority Level Structure

Each interrupt source can also be individually programmed to one of two priority levels by setting or clearing a bit in Special Function Register IP (Figure 27.). A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

Figure 28. IP : Interrupt Priority Register.

(MSB) (LSB)

X	X	PT2	PS	PT1	PX1	PT0	PX0

Symbol	Position	Function
–	IP.7	reserved
–	IP.6	reserved
PT2	IP.5	defines the Timer 2 interrupt priority level. PT2 = 1 programs it do the higher priority level.
PS	IP.4	defines the Serial Port Interrupt priority level. PS = 1 programs it to the higher priority level.
PT1	IP.3	defines the Timer 1 interrupt priority level. PT1 = 1 programs it to the higher priority level.
PX1	IP.2	defines the external interrupt 1 priority level. PX1 = 1 programs it to the higher priority level.
PT0	IP.1	defines the Timer 0 interrupt priority level. PT0 = 1 programs it to the higher priority level.
PX0	IP.0	defines the External Interrupt 0 priority level. PX0 = 1 programs it to the higher priority level.

If two requests of different priority levels are received simultaneoulsy, the request of higher priority level is serviced. If requests of the same priority level are received simultaneously, an internal polling sequence determine which request is serviced. Thus within each priority level is a second priority structure determined by the polling sequence, as follows :

	SOURCE	PRIORITY WITHIN LEVEL
1.	IE0	(highest)
2.	TF0	
3.	IE1	
4.	TF1	
5.	RI + TI	
6.	TF2 + EXF2	(lowest)

Note that the "priority within level" structure is only used to resolve *simultaneous requests of the same priority level.*

How Interrupts Are Handled

The interrupt flags are sampled at S5P2 of every machine cycle. The samples are polled during the following machine cycle. If one of the flags was in a set condition at S5P2 of the preceding cycle, the polling cycle will find it and the interrupt system will generate an LCALL to the appropriate service routine, provided this hardware-generated LCALL is not clocked by any of the following conditions :

1. An interrupt of equal or higher priority level is already in progress.

2. The current (polling) cycle is not the final cycle in the execution of the instruction in progress.

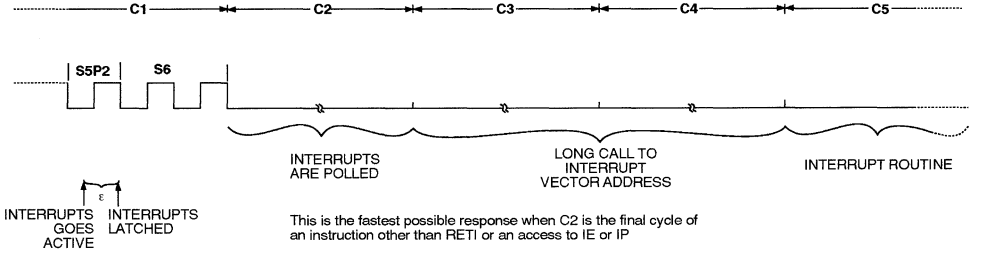
3. The instruction in progress is RETI or any access to the IE or IP registers.

The polling cycle is repeated with each machine cycle, and the values polled are the values that were present at S5P2 of the previous machine cycle. Note then that if an interrupt flag is active but not being responded to for one of the above conditions, if the flag is not *still* active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the facts that the interrupt flag was once active but not serviced is not remembered. Every polling cycle is new.

The polling cycle/LCALL sequence is illustrated in Figure 28.

Note that if an interrupt of higher priority level goes active prior to S5P2 of the machine cycle labeled C3 in Figure 28., then in accordance with the above rules it will be vectored to during C5 and C6, without any instruction of the lower priority routine having been executed.

Figure 29. Interrupt response Timing Diagram.



Thus the processor acknowledges an interrupt request by executing a hardware-generated LCALL to the appropriate servicing routine. In some cases it also clears the flag that generated the interrupt, and in other cases it doesn't. It never clears the Serial Port or Timers 2 flags. This has to be done in the user's software. It clears an external interrupt flag (IE0 or IE1) only if it was transition-activated. The hardware-generated LCALL pushes the contents of the Program Counter onto the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to, as shown below.

SOURCE	VECTOR ADDRESS
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI + TI	0023H
TF2 + EXF2	002BH

Execution proceeds from that location until the RETI instruction is encountered. The RETI instruction informs the processor that this interrupt routine is no longer in progress, then pops the top two bytes from the stack and reloads the Program Counter. Execution of the interrupted program continues from where it left off.

Note that a simple RET instruction would also have returned execution to the interrupted program, but it would have left the interrupt control system thinking an interrupt was still in progress.

External Interrupts

The external sources can be programmed to be level-activated or transition-activated by setting or clearing bit IT1 or IT0 in Register TCON. If ITx = 0, external interrupt x is triggered by a detected low at the $\overline{\text{INTx}}$ pin. If ITx = 1, external interrupt x is edge-triggered. In this mode if successive samples of the $\overline{\text{INTx}}$ pin show a high in one cycle and a low in the next cycle, interrupt request flag IEx in TCON is set. Flag bit IEx then requests the interrupt.

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 12 oscillator periods to ensure sampling. If the external interrupt is transition-activated, the external source has to hold the request pin high for at least one cycle, and then hold it low for at least one cycle to ensure that the transition is seen so that interrupt request flag IEx will be set. IEx will be automatically cleared by the CPU when the service routine is called.

If the external interrupt is level-activated, the external source has to hold the request active until the requested interrupt is actually generated. Then it has to deactivate the request before the interrupt service routine is completed, or else another interrupt will be generated.

Response Time

The $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ levels are inverted and latched into IE0 and IE1 and S5P2 of every machine cycle. The values are not actually polled by the circuitry until the next machine cycle. If a request is active and conditions are right for it to be acknowledged, a hardware subroutine call to the requested service routine will be the next instruction to be executed. The call itself takes two cycles. Thus, a minimum of three complete machine cycles elapse between activation of an external interrupt request and the beginning of execution of the service routine. Figure 28. shows interrupt response timings.

A longer response time would result if the request is blocked by one of the 3 previously listed conditions. If an interrupt of equal or higher priority level is already in progress, the additional wait time obviously depends on the nature of the other interrupt's service routine. If the instruction in progress is not in its final cycle, the additional wait time cannot be more than 3 cycles, since the longest instructions (MUL and DIV) are only 4 cycles long, and if the instruction in progress is RETI or an access to IE or IP, the additional wait time cannot be more than 5 cycles (a maximum of one more cycle to complete the instruction in progress, plus 4 cycles to complete the next instruction if the instruction is MUL or DIV).

Thus, in a single-interrupt system, the response time is always more than 3 cycles and less than 8 cycles.

1.9. Single Step Operation

The 80C51 interrupt structure allows single-step execution with very little software overhead. As previously noted, an interrupt request will not be responded to while an interrupt of equal priority level is still in progress, nor will it be responded to after RETI until at least one other instruction has been executed. Thus, once an interrupt routine has been entered, it cannot be re-entered until at least once instruction of the interrupted program is executed. One way to use this feature for single-step operation is to program one of the external interrupts (say, $\overline{INT0}$) to be level-activated. The service routine for the interrupt will terminate with the following code :

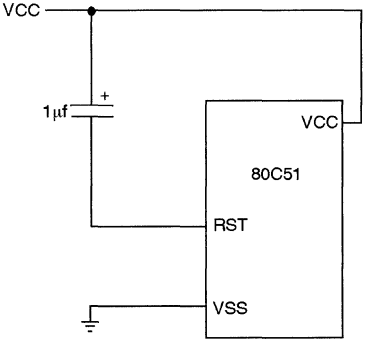
```
JNB     P3.2,$    WAIT HERE TILL INTO
                  GOES HIGH
JB      P3.2,$    NOW WAIT HERE TILL
                  IT GOES LOW
RETI              GO BACK AND EXECUTE
                  ONE INSTRUCTION
```

Now, if the $\overline{INT0}$ pin, which is also the P3.2 pin, is hold normally low, the CPU will go right into the External interrupt 0 routine and stay there until $\overline{INT0}$ is pulsed (from low to high to low). Then it will execute RETI, go back to the task program, execute one instruction, and immediately re-enter the External Interrupt 0 routine to await the next pulsing of P3.2. One step of the task program is executed each time P3.2 is pulsed.

1.10. Reset

The reset input is the RST pin, which is the input to a Schmitt Trigger.

Figure 30. Power on Reset Circuit.



A reset accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), *while the oscillator is running*. The CPU responds by executing an internal reset. It also configures the ALE and $\overline{PSEN}$ pins as inputs. (They are quasi-bidirectional). The internal reset is executed during the second cycle in which RST is high and is repeated every cycle until RST goes low. It leaves the internal registers as follows :

REGISTER	CONTENT
PC	0000H
ACC	00H
B	00H
PSW	00H
SP	07H
DPTR	0000H
P0-P3	0FFH
IP (80C51)	XXX00000B
IP (80C52, 83C154 and 83C154D)	XX000000B
IE (80C51)	0XX00000B
IE (80C52, 83C154 and 83C154D)	0X000000B
TMOD	00H
TCON	00H
T2CON (80C52, 83C154 and 83C154D)	00H
TH0	00H
TL0	00H
TH1	00H
TL1	00H
TH2	00H
TL2	00H
RCAP2H (80C52 83C154 and 83C154D)	00H
RCAP2L (80C52, 83C154 and 83C154D)	00H
SCON	00H
SBUF	Indeterminate
IOCON	00H
PCON (80C51 and 80C52)	0XXX0000B
PCON (83C154 and 83C154D)	000X0000B

The internal RAM is not affected by reset. When VCC is turned on, the RAM content is indeterminate unless the part is returning from a reduced power mode of operation.

Power-on reset

An automatic reset can be obtained when VCC is turned on by connecting the RST pin to VCC through a 1 µf capacitor providing the VCC risetime does not exceed a millisecond and the oscillator start-up time does not exceed 10 milli-seconds. This power-on reset circuit is shown in Figure 1-29. When power comes on, the current drawn by RST commences to charge the capacitor. The voltage at RST is the difference between VCC and the capacitor voltage, and decreases from VCC as the cap charges. The larger the capacitor, the more slowly VRST decreases. VRST must remain above the lower threshold of the Schmitt Trigger long enough to effect a complete reset. The time required is the oscillator start-up time, plus 2 machine cycles.

1.11. Power-Saving Modes of Operation

For applications where power consumption is a critical factor, the TEMIC C51 parts provide two power mode : power-down and idle mode. The first one reduces the consumption up to few microamperes and the second one divides the consumption roughly by 25 %. Both of the modes are controlled by software via the PCON register. In Power-Down mode (PD = 1, PCON = 87H => XXXX XX1X) the oscillator is frozen. In idle mode (IDL = 1, PCON = 87H => XXXX XX01). The oscillator continues to run and the interrupt, serial port, and timer blocks continue to be clocked but the clock signal is gated off the CPU. The activities of the CPU no longer exists unless waiting for an interrupt request. Both Power-Down and Idle mode are explained below. Further function concerning the TEMIC C154 parts will be explain in the next chapter.

Idle Mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and $\overline{PSEN}$ hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give and indication if an interrupt occured during normal operation or during and Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The over way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

Figure 31. PCON : Power Control Register.

(MSB) (LSB)

SMOD	–	–	–	GF1	GF0	PD	IDL

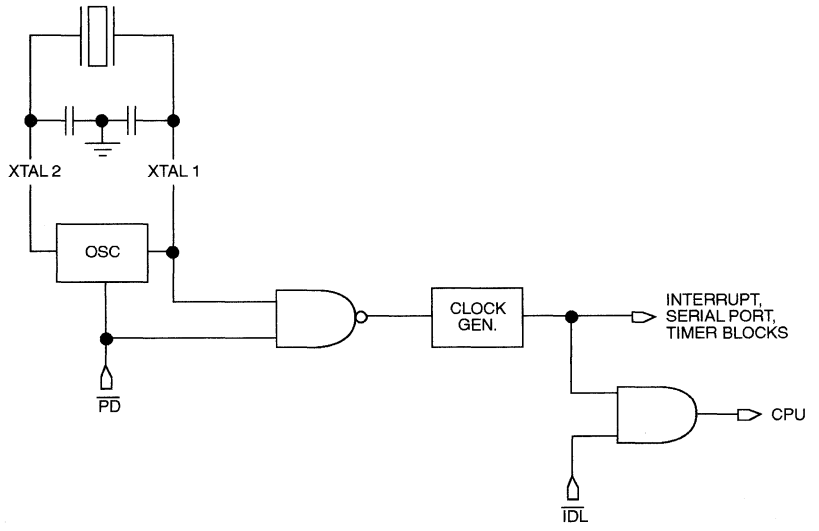
Symbol	Position	Name and Function
SMOD	PCON.7	Double Baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2 or 3.
–	PCON.6	(Reserved)
–	PCON.5	(Reserved)
–	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.

If 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XXX0000).

Power Down Mode

An instruction that sets PCON.1 causes that to be the last instruction executed before going into the Power Down mode. In the Power Down mode, the on-chip oscillator is stopped. With the clock frozen, all functions are stopped, but the on-chip RAM and Special Function Registers are held. The port pins output the values held by their respective SFRs. ALE and $\overline{PSEN}$ output lows.

Figure 32. Idle and Power Down Hardware.



The only exit from Power Down is a hardware reset. Reset redefines all the SFRs, but does not change the on-chip RAM.

In the Power down mode of operation, VCC can be reduced to minimize power consumption. Care must be taken, however, to ensure that VCC is not reduced before the Power Down mode is invoken, and that VCC is restored to its normal operating level, before the Power Down mode is terminated. The reset that terminates Power Down also frees the oscillator. The reset should not be activated before VCC is restored to its normal operating level, and must be held active long enough to allow the oscillator to restart and stabilize (normally less than 10 msec).

This table shows the state of ports during idle and power-down modes.

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

1.12. More about the On-chip Oscillator

The on-chip oscillator circuitry for 80C51's family, shown in Figure 32., consists of a single stage linear inventer for use as a crystal-controlled, positive reactance oscillator.

The on-chip oscillator is able to run with a crystal or with ceramic resonnator. The Figure 33. shows the schematic to work which a crystal and a ceramic resonnator working on a fundamental mode.

Figure 33. On-chip oscillator Circuit.

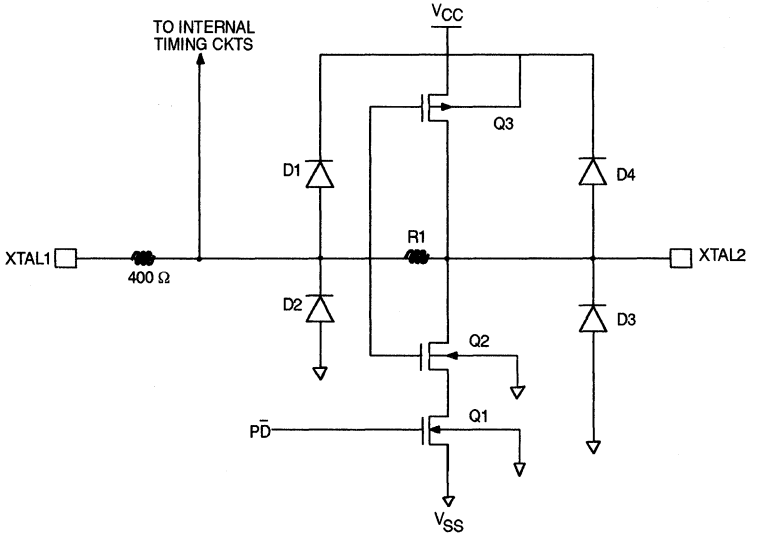
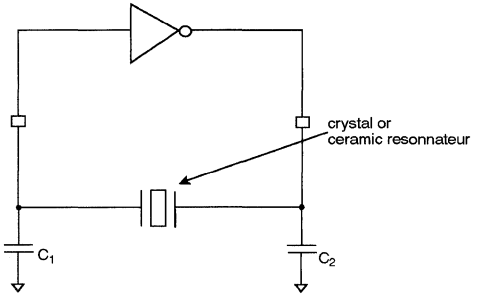


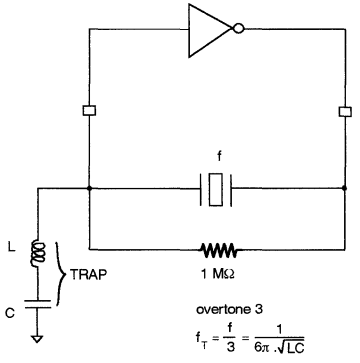
Figure 34. Fundamental Resonance.



The Figure 34. shows the use of a crystal working on an overtone 3 resonance.

An overtone 3 crystal doesn't work on its fundamental resonance but on its third overtone. So it's necessary to catch in its fundamental frequency. The trap consists of the inductor L and the capacitance C. The trap frequency is the running frequency of the crystal divides by 3. An external resistor of 1 MΩ is connected on the both side of the crystal to decrease the gain on the amplifier. Cause the equivalent inductor for a overtone 3 crystal is more larger than a fundamental crystal, the oscillator needs less energy. Without external resistor the level on pin XTAL1 isn't enough to control the internal clock circuitry.

Figure 35. Overtone 3 Resonance.

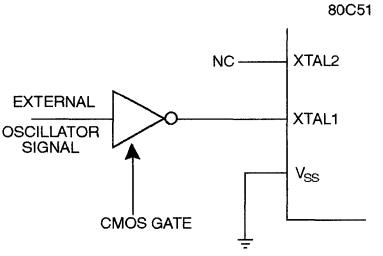


The TEMIC-51 parts can by controlled by an external clock. In this case the external clock signal is connected directly on XTAL1 input and XTAL2 in left floating (Figure 35.).

1.13. Internal Timing

Figure 36. through Figure 39. show when the various strobe and port signals are clocked internally. The figures do not show rise and fall times of the signals, nor do they show propagation delays between the XTAL2 signal and events at other pins.

Figure 36. Driving the C51 parts with an external clock source.



Rise and gall times are dependent on the external loading that each pin must drive. They are often taken to be something in the neighborhood of 10 nsec, measured between 0.8 V and 2.0 V.

Propagation delays are different for different pins. For a given pin they vary with pin loading, temperature, VCC, and manufacturing lot. If the XTAL2 waveform is taken as the timing reference, prop delays may vary from 25 to 125 nsec.

The AC Timings section of the data sheets do not reference any timing to the XTAL2 waveform. Rather, they relate the critical edges of control and input signals to each other. The timing published in the data sheets include the effects of propagation delays under the specified test conditions.

1.14. C51 Pin Description

VCC : Supply voltage.

VSS : Circuit ground potential.

Port 0 : Port 0 is an 8-bit open drain bidirectional I/O Port. As an open drain output port it can sink 8 LS TTL loads. Port 0 pins that have 1s written to them float, and in that state will functions as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external memory. In this application it uses strong internal pullups when emitting 1s. Port 0 also emits code bytes during program verification. In that application, external pullups are required.

Port 1 : Port 1 is an 8-bit bidirectional I/O port with internal pullups. The port 1 output buffers can sink/source 4 LS TTL loads. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.

In the 80C52, 83C154 and 83C154D pins P1.0 and P1.1 also serve the alternate functions of T2 and T2EX. T2 is the Timer 2 external input. T2EX is the input through which a Timer 2 "capture" is triggered.

Port 2 : Port 2 is an 8-bit bidirectional I/O port with internal pullups. The port 2 output buffers can sink/source 4 LS TTL loads. Port 2 emits the high-order addres byte during accesses to external memory that use 16-bit addresses. In this application it uses the strong internal pullups when emitting 1s.

Port 3 : Port 3 is an 8-bit bidirectional I/O port with internal pullups. It also serves the functions of various special features of the TEMIC-C51 Family, as listed below :

PORT PIN	ALTERNATE FUNCTION
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

The Port 3 output buffers can source/sink 4 LS TTL loads.

RST : reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE : Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. ALE is emitted at a constant rate of 1/6 of the oscillator frequency, for external timing or clicking purposes, even when there are no accesses to external memory. (However, one ALE pulse is skipped during each access to external Data Memory).

$\overline{\text{PSEN}}$: Program Store Enable is the read strobe to external Program Memory. When the device is executing out of external Program Memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle (except that two $\overline{\text{PSEN}}$ activations are skipped during accesses to external Data Memory). $\overline{\text{PSEN}}$ is not activated when the deviced is executing out of internal Program Memory.

$\overline{\text{EA}}$: When $\overline{\text{EA}}$ is held high, the CPU executes out of internal Program Memory (unless the Program Counter exceeds 0FFFH in the 80C51, or 1FFFH in the 80C52, or 3 FFFH in the 83C154 or 7FFFH in the 83C154D). Holding $\overline{\text{EA}}$ low forces the CPU to execute out of external memory regardless of the Program Counter value. In the 80C31, 80C32 and 80C154. $\overline{\text{EA}}$ must be externally wired low.

XTAL1 : Input to the inverting oscillator amplifier.

XTAL2 : Output from the inverting oscillator amplifier.

Figure 37. External Program Memory Fetches.

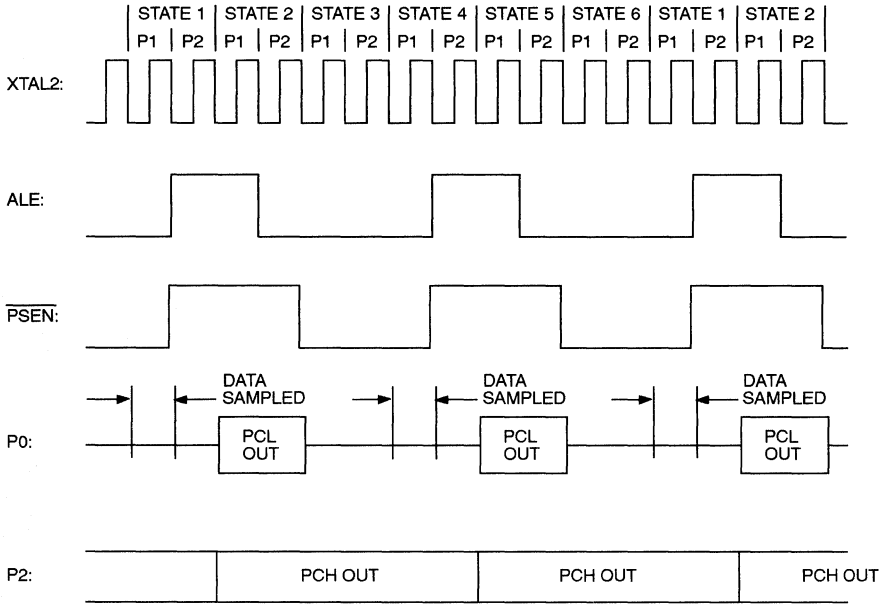


Figure 38. External Data Memory Read Cycle.

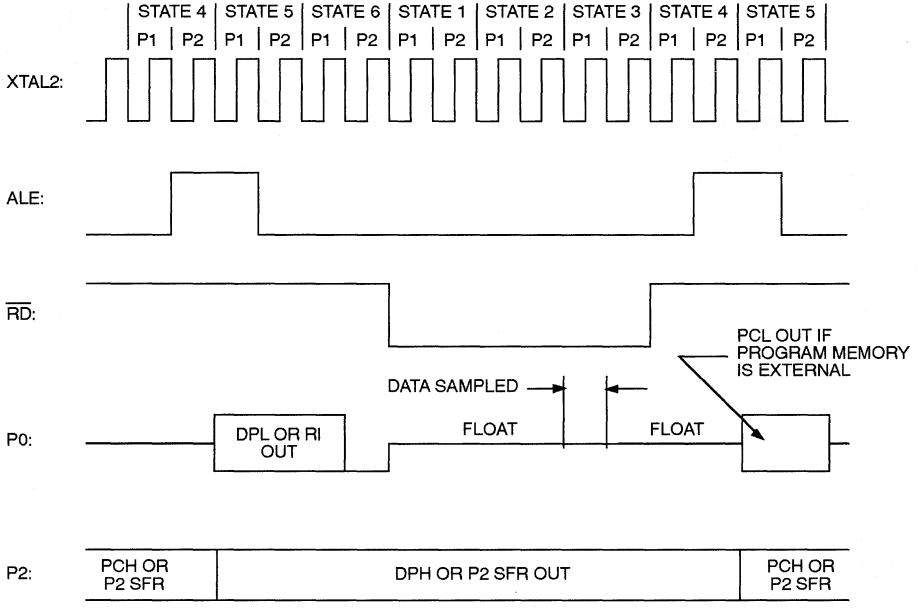


Figure 39. External Data Memory Write Cycle.

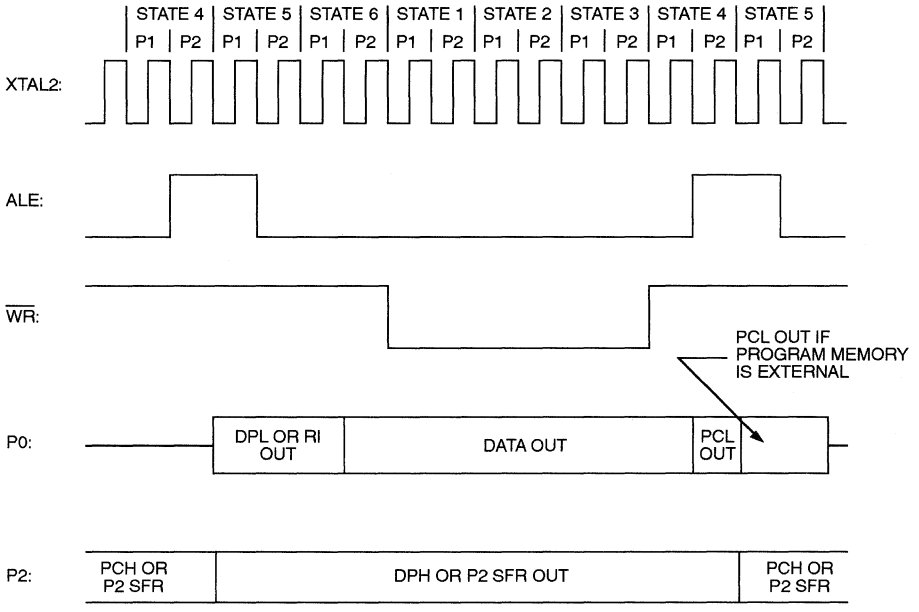
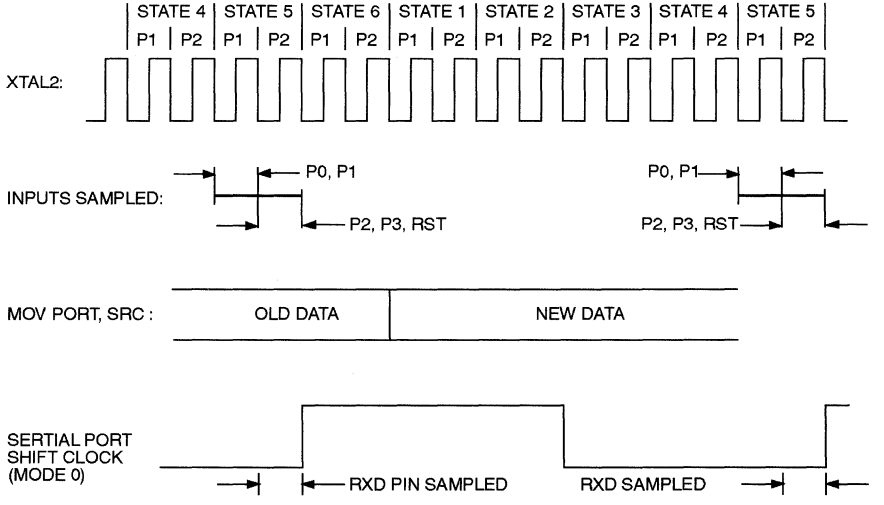


Figure 40. Port Operation.



2. More Features for C154 Parts

This chapter explains, in details, the new features of the 83C154 and 83C154D. The only one difference between 83C154 and 83C154D is the internal ROM size (respectively 16 K bytes and 32 K bytes long).

The major new features of TEMICC154 is listed below :

- I/O part impedance selection
- Watchdog and 32-Bit TIMER/Counter Mode
- Power-down mode
  - Software control
  - Hardware control
- Frame and Overrun error serial link detection.

All these new features are controlled via the IOCON register (new one) and the PCON register.

2.1. I/O Port Impedance

The structure and behaviour of the 83C154s'ports P1, P2 and P3 are indentical to those of the 80C52. Only the control block for the different pullups and pulldowns has been changed. The pullup resistance value can be programmed by means of the IOCON register.

There are three possible values :
- three states (P1, P2, P3 and N are OFF),
- high impedance (100 kΩ, P2 = ON),
- low impedance (10 kΩ, P3 = ON).

Figure 41. is a functional diagram of the PORT.

Figure 42. shows the configuration of the IOCON register which is used to set the right value of the impedance port.

Figure 41. I/O Port Block Diagram.

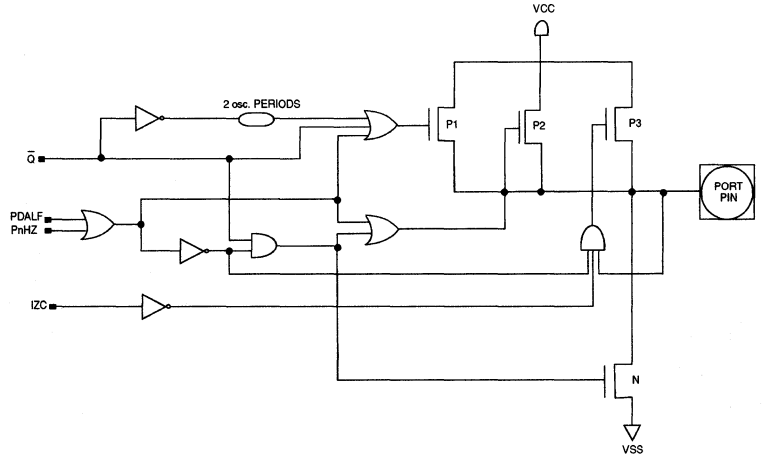


Figure 42. IOCON Register Configuration.

(MSB) (LSB)

WDT	T32	SERR	IZC	P3HZ	P2HZ	P1HZ	ALF

Symbol	Position	Function
ALF	IOCON.0	– Set to 1 and in Power mode PORTS 1, 2 and 3 are floating.
P1HZ	IOCON.1	– If P1HZ = 0 and IZC = 0, PORT P1 is at low impedance. – If P1HZ = 0 and IZC = 0, PORT P1 is at high impedance. – If P1HZ = 1, PORT P1 is floating.
P2HZ	IOCON.2	– If P2HZ = 0 and IZC = 0, PORT P2 is at low impedance. – If P2HZ = 0 and IZC = 0, PORT P2 is at high impedance. – If p2HZ = 1, PORT P2 is floating.
P3HZ	IOCON.3	– If P3HZ = 0 and IZC = 0, PORT P3 is at low impedance. – If P3HZ = 0 and IZC = 0, PORT P3 is at high impedance. – If P3HZ = 1, PORT P3 is floating.
IZC	IOCON.4	– In conjunction with PnHZ selects the output pullup value.

Low impedance

This mode is the default mode upon a reset and it is compatible with C51 parts. The configuration of IOCON is explained by the Figure 42. Whenever PnHZ and IZC are equal to zero, P1, P2 and P3 are in this mode. In this case 3 LS TTL loads can be interfaced.

High impedance

This mode is invoked by setting PnHZ = 0 and IZC = 1. Only the transistor PZ of the Figure 41. is on and one LS TTL load can be interfaced.

Three states mode

Two different modes can be used. The first one allows to set each of the 3 ports in three states during a normal operation. The second one allows to set all the 3 parts in three states by entering in the Power-Down mode.

Whenever PnHZ is set to 1, the part is in three states mode. If ALF is set to 1, at each time the Power-Down mode is called all the three parts are in the three states. When the C154 part exist from the Power-Down mode, the part impedance is the impedance just before entering in this mode (the part switches as soon as the interrupt request is generated, not after the oscillator start-up). The three states mode switch-off all the transistor.

2.2 Watchdog and 32-bit Timer/Counter Mode

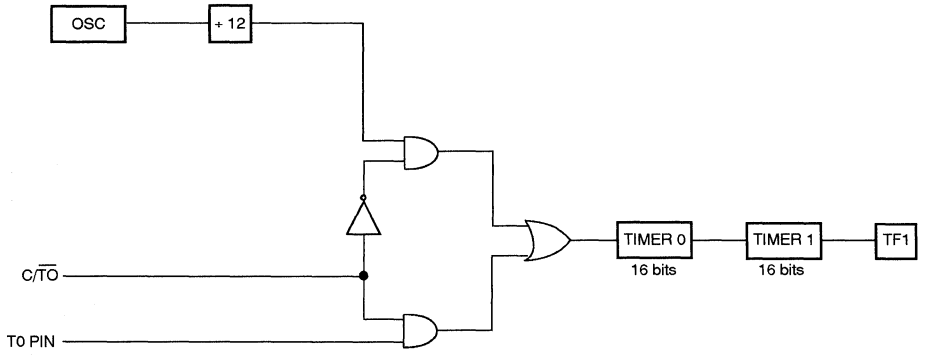
TIMER/COUNTER of C51 family can be configured in four modes. With C154 parts, two new modes can be used. Both of them use TIMER0 and/or TIMER 1. The first one is used like a 32-Bit Timer/Counter and the second one is used like a 8/13/16/32-Bit Watch-Dog. Both of this two modes is programmed by software by using the IOCON register. The 32-Bit mode is on by setting the Bit T32. The Watchdog mode is on by setting the bit WDT. The Figure 43. shows the configuration of the register IOCON.

Figure 43. 32 Bit/Watchdog Mode.

(MSB)							(LSB)
WDT	T32	SERR	IZC	P3HZ	P2HZ	P1HZ	ALF

Symbol	Position	Function
T32	IOCON.6	– If T32 = 1 and if C/T0 = 0, T1 and T0 are programmed as a 32 bit TIMER. – If T32 = 1 and if C/T0 = 1, T1 and T0 are programmed as a 32 bit COUNTER.
WDT	IOCON.7	– If WDT = 1 and according to the mode selected by TMOD, and 8 bit or 32 bit WATCHDOG is configured from TIMERS 0 and 1.

Figure 44. 32 Bit Mode.



32 Bit Mode

T32 = 1 enables access to this mode. As shown in Figure 44. this 32 bit mode consists in cascading TIMER 0 for the LSBs and TIMER 1 for the MSBs.

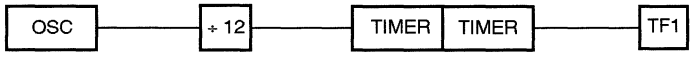
T32 = 1 starts the timer/counter and T32 = 0 stops it.

It should be noted that as soon as T32 = 0, TIMERs 0 and 1 assume the configuration specified by register TMOD. Moreover, if TR0 = 1 or if TR1 = 1, the content of the TIMERs evolves. Consequently, in 32 bit mode, if the TIMER/COUNTER must be stopped (T32 = 0). TR0 and TR1 must be set to 0.

32 Bit Timer

Figure 45 illustrates the 32 Bit TIMER mode.

Figure 45.



In this mode, T32 = 1 and C/T0 = 0, the 32 bit timer is incremented on each S3P1 state of each machine cycle. An overflow of TIMER 0 (TF0 has not been set to 1) increments TIMER 1 and the overflow of the 32 bit TIMER is signalled by setting TF1 (S5P1) to 1.

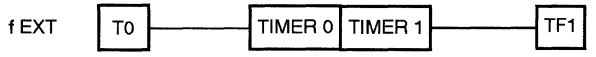
The following formula should be used to calculate the required frequency :

$$f = \frac{OSC}{12 \times (65536-(T0,\ T1))}$$

32 Bit Counter

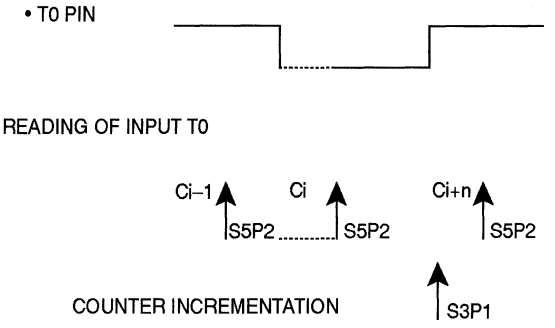
Figure 46. illustrates the 32 BIT COUNTER mode.

Figure 46. 32 Bit Counter Configuration.



In this mode, T32 = 0 and C/$\overline{T0}$ = 1. Before it can make an increment, the 83C154 must detect two transitions on its T0 input. As shown in Figure 47. input T0 is sampled on each S5P2 state of every machine cycle or, in other words, every OSC ÷ 12.

Figure 47. Counter Incrementation Condition.



The counter will only evolve if a level 1 is detected during state S5P2 of cycle Ci and if a level 0 is detected during state S5P2 of cycle Ci + n.

Consequently, the minimal period of signal fEXT admissible by the counter must be greater than or equal to two machine cycles. The following formula should be used to calculate the operating frequency.

$$f = \frac{fEXT}{(65536-(T0,\ T1))}$$

$$fEXT \leq \frac{OSC}{24}$$

watchdog Mode

WDT = 1 enables access to this mode. As shown in Figure 48. all the modes of TIMERs 0 and 1, of which the overflows act on TF1 (TF1 = 1), activate the watchdog Mode.

If C/$\overline{T}$ = 0, the watchdog is a TIMER that is incremented every machine cycle. If C/$\overline{T}$ = 1, the watchdog is a counter that is incremented by an external signal of which the frequency cannot exceed OSC ÷ 24.

The overflow of the TIMER/COUNTER is signalled by raising flag TF1 to 1. The reset of the 83C154/83C154D is executed during the next machine cycle and lasts for the next 5 machine cycles. The results of this reset are identical to those of a hardware reset. The internal RAM is not affected and the special register assume the values shown in Table 2.

Table 3. Content of the SFRs after a reset triggered by the WATCHDOG.

REGISTER	CONTENT
PC	0000H
ACC	00H
B	00H
PSW	00H
SP	00H
DPTR	0000H
P0–P3	0FFH
IP	00H
IE	0X000000B
TMOD	00H
TCON	00H
T2CON	00H
TH0	00H
TL0	00H
TH1	00H
TL1	00H
TH2	00H
TL2	00H
RCAP2H	00H
RCAP2L	00H
SCON	00H
SBUF	Indeterminate
IOCON	00H

As there are no precautions for protecting bit WDT from spurious writing in the IOCON register, special care must be taken when writing the program. In particular, the user should use the IOCON register bit handing instructions :

– SETB and CLR x

in preference to the byte handling instructions :

– MOV IOCON, # XXH, ORL IOCON, # XXH,

– ANL IOCON, # XXH,

External Counting in Power-down Mode (PD = PCON.1 = 1)

In the power-down mode, the oscillator is turned off and the 83C154s'activity is frozen. However, if an external clock is connected to one of the two inputs, T1/T0, TIMER/COUNTERS 0 and 1 can continue to operate. In this case, counting becomes asynchronous and the maximum, admissible frequency of the signal is OSC : 24.

The overflow of either counter TF0 or TF1 causes an interrupt to be serviced or forces a reset if the counter is in the watchdog MODE (T32 = ICON.7 = 1).

2.3 Power-Reducing Mode

Basically the Power-Reducing Mode of the TEMIC C154 parts are 100 % compatible with the 80C51 and 80C52 parts. However both Idle and Power-Down mode are improved with some new powerful features.

Idle mode is improved by giving the software possibility to execute or not the software interrupt routine when an interrupt request occurs (Recover Power Mode).

Power-Down mode is now more powerful because an interrupt request can avake the TEMIC C154 parts. In addition an external hardware signal can control entirely the mode (Hardware Power Mode).

Details on these new features are given below.

Idle Mode

This mode is basically compatible with the TEMIC C51 parts (refer to the chapter 1.11). The new feature concerns the way to exit from this mode. Now with the Recover Power Mode, the software interrupt routine is or not executed when the interrupt routine occurs. This mode is activated by setting the bit RPD in PCON register. In this case the next instruction executed is the next following the IDLE instruction (MOV PLON, # 01).

Power-Down Mode

Software control

This mode is basically compatible with the C51 parts (refer to the chapter 1.11). The new features concern the way to exit from this mode.

With the C51 parts the only way to complete this mode is to apply an hardware reset. The newest thing is the possibility to exist from this mode by an interrupt request coming from the both external interrupts and the both counter 0 and 1 if an external clock is connected on pin T1 or T0.

Likewise IDLE mode, it is possible to execute or not the software interrupt routine. By setting the RPD bit the next instruction executed, after the interrupt request has been processed, will be the instruction following the POWER-DOWN intruction. If the RPD bit is not set, the program will continue by executing the software interrupt routine. The Figure 48. shows the behaviour of the Recover Power Mode.

Figure 48. Example in Recover Power Mode.

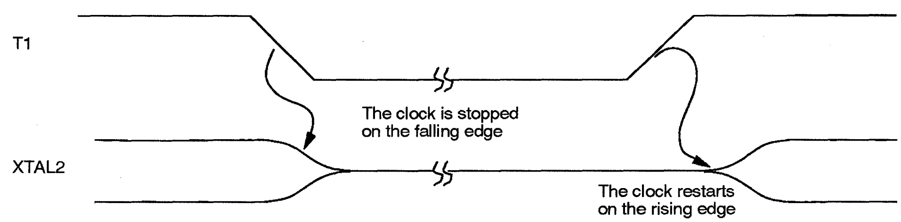
```
ex :
                                 ; The Recover Mode is enable
                                 ; The Power-Down is enable
      Adr n  MOV  PCON, #001XXX10...
                                 ; The CPU waits for an asynchronous
                                 ; event

                                 ; An interrupt request occurs and
                                 ; the instruction located at the
                                 ; address Adr n + 1 is executed
      Adr n + 1
```

Hardware control

This mode is new and controls the Power-Down by an external hardware signal connected on pin T1 (P3.5). This mode is called by setting HPD bit in the PCON register. The 83C154 will be in Power-Down as soon as T1 input will be drive by a falling edge and will remain in this state until T1 input will be drive by a rising edge. The Figure 49. shows the behaviour of the Hardware Power Mode.

Figure 49. Behaviour of the Hardware Power Mode (HPD = 1).



The time takes by the oscillator to restart depends of the crystal and the capacitors connected on both side of the crystal (typically 10 ms).

Software and hardware control

This two modes can be mixed to control the Power-Down Mode. Entry to the mode can be made either by setting PD bit to 1 or by setting HPD bit to 1 and presenting a falling edge on T1 input. Exit from this mode can be made if the software and hardware conditions are met : a rising edge on T1 input and an interrupt request. If these two conditions are not satisfied, only an hardware reset can complete the mode.

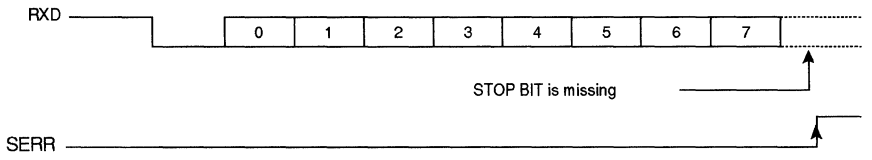
2.4 Frame and Overrun Error Serial Link Detection

This feature is new and allows to the user to detect a serial link error. Two kinds of error can be detected during a reception : OVERRUN ERROR and FRAME ERROR. Both of them set the SERR bit in the IOCON register at the half of the stop bit. This must be cleared by software.

Frame error

This error occurs when the format of the received Data is wrong. The Figure 50. shows an example of a Frame error.

Figure 50. FRAME ERROR example, STOP BIT is missing.

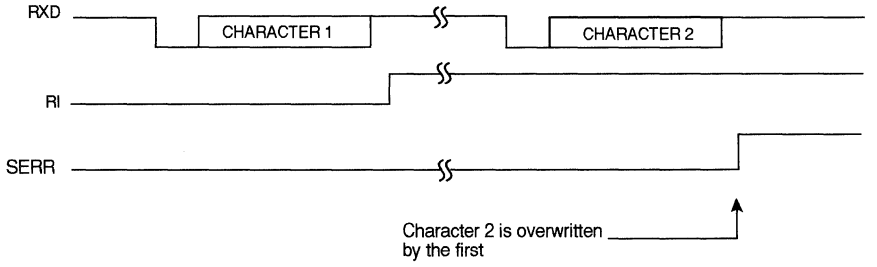


In this example the receiver waits for a STOP BIT to complete the frame reception. Unfortunately the stop bit isn't there and the receiver indicates the frame error by setting to 1 the SERR bit in the IOCON register.

Overrun Error

This error occurs, when a character received and not read by the C.P.U, is overwritten by a new one. The Figure 51. shows an example of OVERRUN ERROR.

Figure 51. OVERRUN ERROR example.



In this example the character 1 is received and the RI bit is set to 1. A second character is sent before the CPU reads the first one. The character 1 is overwritten and SERR bit is set to 1 to indicate the loss of the first character.

Note
With the C154 parts the RI bit isn't set on the same time than the C51 parts. With the C51 parts the RI bit is set on the last data bit. With the C154 the RI bit is set on the stop bit.

C51 Family Programmer's Guide and Instruction Set

Summary

1. Memory Organization

1.1. Program Memory

The TEMIC C51 Microcontroller Family has separate address spaces for program Memory and Data Memory. The program memory can be up to 64 K bytes long. The lower 4 K for the 80C51 (8 K for the 80C52, 16 K for the 83 C154 and 32 K for the 83C154D) may reside on chip. Figure 1 to 4 show a map of 80C51, 80C52, 83C154 and 83C154D program memory.

Figure 1. The 80C51 Program Memory.

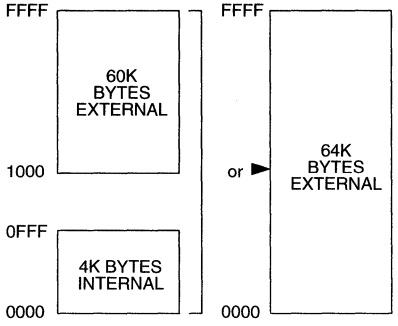


Figure 2. The 80C52 Program Memory.

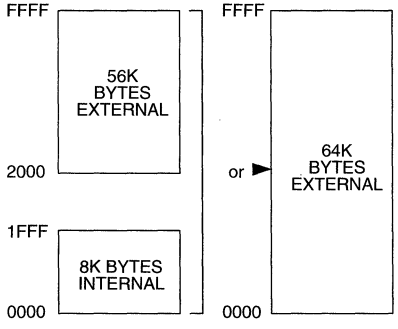


Figure 3. The 83C154 Program Memory.

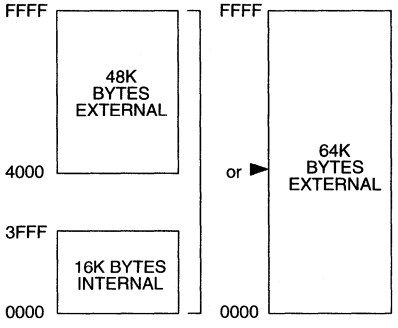
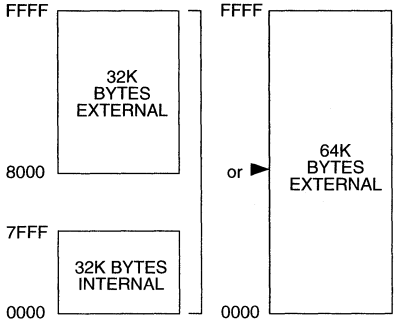


Figure 4. The 83C154D Program Memory.



1.2. Data Memory

The C51 Microcontroller Family can address up to 64 K bytes of Data Memory to the chip. The "MOVX" instruction is used to access the external data memory (refer to the C51 instruction set, in this chapter, for detailed description of instructions).

The 80C51 has 128 bytes of on-chip-RAM (256 bytes in the 80C52, 83C154 and 83C154D) plus a number of Special Function Registers (SFR). The lower 128 bytes of RAM can be accessed either by direct addressing (MOV data addr). or by indirect addressing (MOV @Ri). Figure 5 and 6 show the 80C51, 80C52, 83C154 and 83C154D Data Memory organization.

Figure 5. The 80C51 Data Memory Organisation.

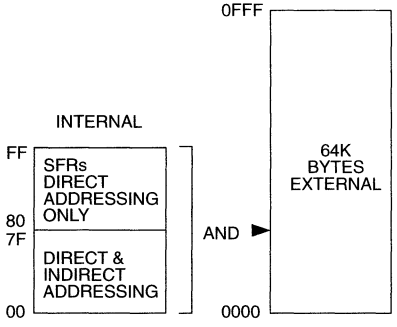
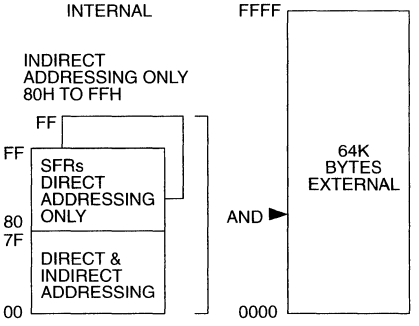


Figure 6. The 80C52, 83C154 and 83C154D Data Memory Organisation.



1.3. Indirect Address Area

Note that in Figure 6 - the SFRs and the indirect address RAM have the same addresses (80H-OFFH). Nevertheless, they are two separate areas and are accessed in two different ways. For example the instruction

MOV 80H, #0AAH

writes 0AAH to Port 0 which is one of the SFRs and the instruction

MOV R0, # 80H
MOV @ R0, # 0BBH

writes 0BBH in location 80H of the data RAM. Thus, after execution of both of the above instructions Port 0 will contain 0AAH and location 80 of the RAM will contain 0BBH.

Note that the stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space in those devices which implement 256 bytes of internal RAM.

1.4. Direct And Indirect Address Area

The 128 bytes of RAM which can be accessed by both direct and indirect addressing can be divided into 3 segments as listed below and shown in figure 7.

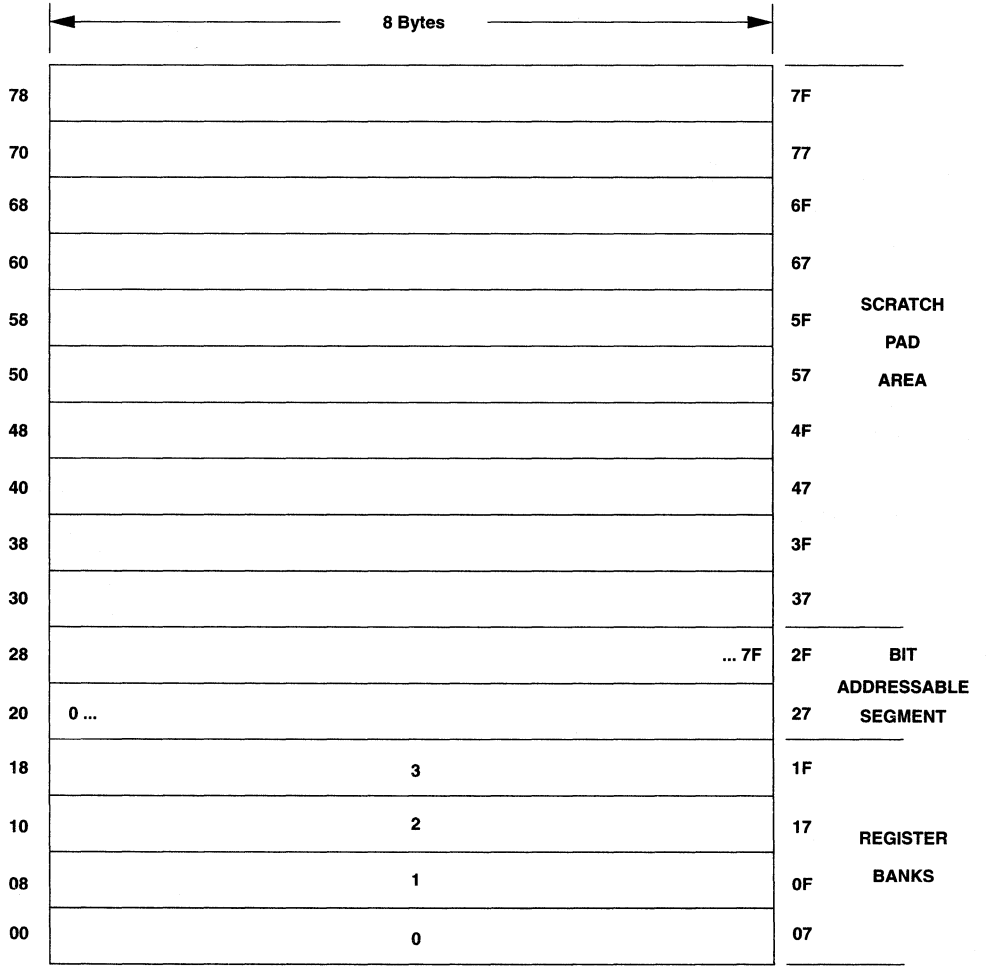
1. Register Banks 0.3 : Locations 0 through 1FH (32 bytes). ASM-51 and the device after reset default to register bank 0. To use the other register banks the user must select them in the software. Each register bank contains 8 one-byte registers, 0 through 7.
Reset initializes the Stack Pointer to location 07H and it is incremented once to start from location 08H which is the first register (R0) of the second register bank. Thus, in order to use more than one register bank, the SP should be initialized to a different location of the RAM where it is not used for data storage (ie, higher part of the RAM).

2. Bit Addressable Area : 16 bytes have been assigned for this segment, 20H-2FH. Each one of the 128 bits of this segment can be directly addressed (0-7FH).
The bits can be referred to in two ways both of which are

acceptable by the ASM-51. One way is to refer to their addresses, ie, 0 to 7FH. The other way is with reference to bytes 20H to 2FH. Thus, bits 0-7 can also be referred to as bits 20.0-20.7, and bits 8-FH are the same as 21.0-21.7 and so on.
Each of the 16 bytes in this segment can also be addresses as a byte.

3. Scratch Pad Area : Bytes 30H through 7FH are available to user as data RAM. However, if the stack pointer has been initialized to this area, enough number of bytes should be left aside to prevent SP data destruction.

Figure 7. 128 Bytes of RAM Direct and Indirect Addressable.



1.5. Special Function Registers

Table 1 contains a list of all the SFRs and their addresses. Comparing table 1 and figure 8 shows that all of the SFRs that are byte and bit addressable are located on the first column of the diagram in figure 8.

Table 1.

SYMBOL	NAME	ADDRESS
*ACC	Accumulator	0E0H
*B	B Register	0F0H
*PSW	Program Status Word	0D0H
SP	Stack Pointer	81H
DPTR	Data Pointer 2 Bytes	
DPL	Low Byte	82H
DPH	High Byte	83H
*P0	Port 0	80H
*P1	Port 1	90H
*P2	Port 2	0A0H
*P3	Port 3	0B0H
*IP	Interrupt Priority Control	0B8H
*IE	Interrupt Enable Control	0A8H
TMOD	Timer/Counter Mode Control	89H
*TCON	Timer/Counter Control	88H
*+T2CON	Timer/Counter 2 Control	0C8H
TH0	Timer/Counter 0 High Byte	8CH
TL0	Timer/Counter 0 Low Byte	8AH
TH1	Timer/Counter 1 High Byte	8DH
TL1	Timer/Counter 1 Low Byte	8BH
+TH2	Timer/Counter 1 High Byte	0CDH
+TL2	Timer/Counter 2 Low Byte	0CCH
+RCAP2H	T/C 2 Capture Reg. High Byte	0CBH
+RCAP2L	T/C 2 Capture Reg. Low Byte	0CAH
*SCON	Serial Control	98H
SBUF	Serial Data Buffer	99H
PCON	Power Control	87H
*IOCON (1)	IO Control	F8H

+ 80C52, 83C154 and 83C154D only * bit addressable
(1) 83C154 and 83C154D only

2. SFR Memory Map

Figure 8.

	8 Bytes								
F8	IOCON								FF
F0	B								F7
E8									EF
E0	ACC								E7
D8									DF
D0	PSW								D7
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2			CF
C0									C7
B8	IP								BF
B0	P3								B7
A8	IE								AF
A0	P2								A7
98	SCON	SBUF							9F
90	P1								97
88	TCON	TMOD	TL0	TL1	TH0	TH1			8F
80	P0	SP	DPL	DPH				PCON	87

↑ bit addressable

2.1. What do the SFRs Contain just after Power-on or a Reset ?

Table 2 lists the contents of each SFR after a power-on reset or a hardware reset.

Table 2. Contents of the SRFs after reset.

REGISTER	VALUE IN BINARY
*ACC	0000 0000
*B	0000 0000
*PSW	0000 0000
SP	0000 0111
DPTR	0000 0000
*P0	1111 1111
*P1	1111 1111
*P2	1111 1111
*P3	1111 1111
*IP	XXX0 0000 80C51 XXX0 0000 80C52 0X00 0000 83C154/C154D
*IE	0XX0 0000 80C51 0X000 0000 83C154/C154D and 80C52
TMOD	0000 0000

* : bit addressable.
\+ : 80C52, 83C154 and 83C154D only.
– : 83C154 and 83C154D only.
X : Undefined.

These SFRs that have their bits assigned for various functions are listed in this section. A brief description of each bit is provided for quick reference. For more detailed information refer to the Architecture chapter of this book.

REGISTER	VALUE IN BINARY
*TCON	0000 0000
+*T2CON	0000 0000
TH0	0000 0000
TL0	0000 0000
TH1	0000 0000
TL1	0000 0000
+ TH2	0000 0000
+ TL2	0000 0000
+ RCAP2L	0000 0000
+ RCAP2H	0000 0000
*SCON	0000 0000
SBUF	Indeterminate
PCON	0XXX 0000 80C51 and 80C52 000X 0000 83C154 and 83C154D
–*IOCON	0000 0000

PSW : Program Status Word (Bit Addressable)

CY	AC	F0	RS1	RS0	OV	F1	P

CY	PSW.7	Carry Flag.
AC	PSW.6	Auxiliary Carry Flag.
F0	PSW.5	Flag 0 available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1 (SEE NOTE).
RS0	PSW.3	Register Bank selector bit 0 (SEE NOTE).
OV	PSW.2	Overflow Flag.
F1	PSW.1	Flag F1 available to the user for general purpose.
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of "1" bits in the accumulator.

Note :

The value presented by RS0 and RS1 selects the corresponding register bank.

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00H–07H
0	1	1	08H–0FH
1	0	2	10H–17H
1	1	3	18H–1FH

* User software should not write 1s to reserved bits. These bits may be used in future TEMIC C51 products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1.

PCON : Power Control Register (Not Bit Addressable)

SMOD	HPD	RPD	-	GF1	GF0	PD	IDL

SMOD	PCON.7	Double baud rate bit. If SMOD = 1, the baud rate is doubled when the serial part is used in mode 1, 2 and 3.
HPD	PCON.6	Hard Power Down. (83C154 and 83C154D only). The falling/rising edge of a signal connected on pin P3.5 Starts/Stops the Power-Down mode. A reset can also stop this mode.
RPD	PCON.5	Recover Power Down bit. (83C154 and 83C154D only). It's used to cancel a Power-Down/IDLE mode. If it's set, an interrupt (enable or disable) can cancel this mode. A reset can also stop this mode (see Note 1).
-	PCON.4	Not implemented, reserved for futur used*
GF1	PCON.3	General purpose bit.
GF0	PCON.2	General purpose bit.
PD	PCON.1	Power Down bit. If set, the oscillator is stopped. A reset or an interrupt (83C154 and 83C154D only) can cancel this mode (Note 1).
IDL	PCON.0	IDLE bit. If set the activity CPU is stopped. A reset or an interrupt can cancel this mode (See Note 1).

* User software should not write 1s to reserved bits. These bits may be used in future TEMIC C51 products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1.

Note 1 (83C154 and 83C154D only) :

– if RPD = 0 and if an interrupt cancels the mode Power-Down/IDLE, the next instruction to execute is a LCALL at the interrupt routine.

– RPD = 1 – if interrupt request is enable the next instruction to execute is a LCALL at the interrupt routine.
– if interrupt request is disable, the program continue with the instruction immediately after the Power-Down/Idle instruction.

2.2. Interrupts

In order to use any of the interrupts in the C51, the following three steps must be taken.
1. Set the EA (enable all) bit in the IE register to 1.
2. Set the corresponding individual interrupt enable bit in the IE register to 1.
3. Begin the Interrupt service routine at the corresponding Vector Address of that interrupt. See Table below.

INTERRUPT SOURCE	VECTOR ADDRESS
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI & TI	0023H
TF2 & EXF2	002BH

In addition, for external interrupts, pins $\overline{INT0}$ and $\overline{INT1}$ (P3.2 and P3.3) must be set to 1, and depending on whether the interrupt is to be level or transition activated, bits IT0 or IT1 in the TCON register may need to be set to 1.

ITX = 0 level activated
ITX = 1 transition activated

IE : Interrupt Enable Register (Bit Addressable)

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	-	ET2	ES	ET1	EX1	ET0	EX0

EA	IE.7	Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, interrupt source is individually enable or disabled by setting or clearing its enable bit.
-	IE.6	Not implemented, reserved for future use*.
ET2	IE.5	Enable or disable the Timer 2 overflow or capture interrupt (80C52, 83C154 and 83C154D only).
ES	IE.4	Enable or disable the Serial port interrupt.
ET1	IE.3	Enable or disable the Timer 1 overflow interrupt.
EX1	IE.2	Enable or disable External interrupt 1.
ET0	IE.1	Enable or disable the Timer 0 overflow interrupt.
EX0	IE.0	Enable or disable External Interrupt 0.

* User software should not write 1s to reserved bits. These bits may be used in future TEMIC C51 products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1.

2.3. Assigning Higher Priority to one More Interrupts

In order to assign higher priority to an interrupt the corresponding bit in the IP register must be set to 1. Remember that while an interrupt service is in progress, it cannot be interrupted by a lower or same level interrupt.

2.4. Priority Within Level

Priority within level is only to resolve simultaneous requests of the same priority level. From high to low, interrupt sources are listed below :

IE0
TF0
IE1
TF1
RI or TI
TF2 or EXF2

IP : Interrupt Priority Register (Bit Addressable)

If the bit is 0, the corresponding interrupt has a lower priority and if the bit is the corresponding interrupt has a higher priority.

PCT	-	PT2	PS	PT1	PX1	PT0	PX0

PCT	IP.7	Defines the same priority level for all the source interrupt (83C154 and 83C154D only).
-	IP.6	Not implemented, reserved for future use*.
PT2	IP.5	Defines the Timer 2 interrupt priority level (80C52, 83C154 and 83C154D only).
PS	IP.4	Defines the Serial Port interrupt priority level.
PT1	IP.3	Defines the Timer 1 Interrupt priority level.
PX1	IP.2	Defines External Interrupt priority level.
PT0	IP.1	Defines the Timer 0 interrupt priority level.
PX0	IP.0	Defines the External Interrupt 0 priority level.

* User software should not write 1s to reserved bits. These bits may be used in future TEMIC C51 products to invoke new features. In that case, the reset or inactive value of the now bit will be 0, and its active value will be 1.

IOCON : Input/Output Control Register (83C154 and 83C154D only)

WDT	T32	SERR	IZC	P3HZ	P2HZ	P1HZ	ALF

WDT IOCON.7 Watch Dog Timer bit. Set when Timer 1 is overflow (TF = 1). The CPU is reset and the program is executed from address 0.

T32 IOCON.6 Timer 32 bits. The Timer 1 and Timer 0 are connected together to form a 32 bits Timer/Counter. If C/TO = 0, it's a Timer. If C/TO = 1, it's a counter.

SERR IOCON.5 Serial Port Reception Error flag. Set when an overrun on frame error is received.

IZC IOCON.4 Set/Cleared by software to select 100/10 K pull up resistance for Port 1, 2 and 3.

P3HZ IOCON.3 When Set, Port 3 becomes a tri-state input. When cleared, the pull-up resistance value is selected by IZC.

P2HZ IOCON.2 When Set, Port 2 becomes a tri-state input. When cleared, the pull-up resistance value is selected by IZC.

P1HZ IOCON.1 When Set, Port 1 becomes a tri-state input. When cleared, the pull-up resistance value is selected by IZC.

ALF IOCON.0 All Port tri-state. When Set and CPU in Power-Down mode, port 1, 2 and 3 are tri-state.

TCON : Timer/Counter Control Register (Bit Addressable)

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TF1 TCON.7 Timer 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as processor vectors to the interrupt service routine.

TR1 TCON.6 Timer 1 run control bit. Set/cleared by software to turn Timer/Counter ON/OFF.

TF0 TCON.5 Timer 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as processor vectors to the service routine.

TR0 TCON.4 Timer 0 run control bit. Set/cleared by software to turn Timer/Counter 0 ON/OFF.

IE1 TCON.3 External Interrupt 1 edge flag. Set by hardware when External interrupt edge is detected. Cleared by hardware when interrupt is processed.

IT1 TCON.2 Interrupt 1 type control bit. Set/cleared by software to specify falling edge/flow level triggered External Interrupt.

IE0 TCON.1 External Interrupt 0 edge flag. Set by hardware when External Interrupt edge detected. Cleared by hardware when interrupt is processed.

IT0 TCON.0 Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered External Interrupt.

TMOD : Timer/Counter Mode Control Register (Not Bit Addressable)

GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TIMER 1				TIMER 0			

GATE When TRx (in TCON) is set and GATE = 1, TIMER/COUNTERx will run only while INTx pin is high (hardware control). When GATE = 0, TIMER/COUNTERx will run only while TRx = 1 (software control).

C/$\overline{T}$ Timer or Counter selector. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from Tx input pin).

M1 Mode selector bit (NOTE 1).

M0 Mode selector bit (NOTE 1).

Note 1 :

M1	M0	OPERATING MODE	
0	0	0	13–bit Timer
0	1	1	16–bit Timer/Counter
1	0	2	8–bit Auto–Reload Timer/Counter
1	1	3	(Timer 0) TL0 is an 8–bit Timer/Counter controlled by the standard Timer 0 control bits, TH0 is an 8–bit Timer and is controlled by Timer 1 control bits.
1	1	3	(Timer 1) Timer/Counter 1 stopped.

2.5. Timer Set-up

Tables 3 through 6 give some values for TMOD which can be used to set up Timer 0 in different modes.

It is assumed that only one timer is being used at a time. It is desired to run Timers 0 and 1 simultaneously, in any mode, the value that in TMOD for Timer 0 must be ORed with the value shown for Timer 1 (Tables 5 and 6).

For example, if it is desired to run Timer 0 in mode 1 GATE (external control) and Timer 1 in mode 2 COUNTER, then the value must be loaded into TMOD is 69H (09H from Table 3 ORed with 60H from Table 6).

Moreover, it is assumed that the user, at this point, is not ready to turn the timers on and will do that a different point in the program by setting bit TRx (in TCON) to 1.

2.6. Timer/Counter 0

Table 3. As a Timer

MODE	TIMER 0 FUNCTION	TMOD	
		INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
0	13–bit Timer	00H	08H
1	16–bit Timer	01H	09H
2	8–bit Auto–Reload	02H	0AH
3	Two 8–bit Timers	03H	0BH

Table 4. As a Counter

MODE	TIMER 0 FUNCTION	TMOD	
		INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
0	13–bit Timer	04H	0CH
1	16–bit Timer	05H	0DH
2	8–bit Auto–Reload	06H	0EH
3	one 8–bit Timers	07H	0FH

Notes : 1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on $\overline{INT0}$ (P3.2) when TR0 = 1 (hardware control).

2.7. Timer/Counter 1

Table 5. As a Timer

MODE	TIMER 0 FUNCTION	TMOD	
		INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
0	13–bit Timer	00H	80H
1	16–bit Timer	10H	90H
2	8–bit Auto–Reload	20H	A0H
3	does not run	30H	B0H

Table 6. As a Counter

MODE	TIMER 0 FUNCTION	TMOD	
		INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
0	13–bit Timer	40H	C0H
1	16–bit Timer	50H	D0H
2	8–bit Auto–Reload	60H	E0H
3	not available	–	–

Notes : 1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1 to 0 transition on $\overline{INT1}$ (P3.2) when TR1 = 1 (hardware control).

T2CON : Timer/Counter 2 Control register (Bit Addressable) (80C52, 83C154 and 83C154D only)

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

TF2 T2CON.7 Timer 2 overflow flag set by hardware and cleared by software. TF2 cannot be set when either RCLK = 1 or CLK = 1

EXF2 T2CON.6 Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX, and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.

RCLK T2CON.5 Receive clock flag. When set, causes the Serial Port to use Timer 2 overflow pulses for its receive clock in modes 1 & 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.

TCLK T2CON.4 Transmit clock flag. When set, causes the Serial Port use Timer 2 overflow pulses for its transmit clock in modes 1 & 3, TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.

EXEN2 T2CON.3 Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of negative transition on T2EX if Timer 2 is not being used to clock the Serial Port. EXEN2 = 0 causes Timer 2 to ignore events as T2EX.

TR2 T2CON.2 Software START/STOP control for Timer 2. A logic 1 starts the Timer.

C/$\overline{T2}$ T2CON.1 Timer or Counter select.

CP/$\overline{RL2}$ T2CON.0 Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, Auto-Reloads will occur either with Timer2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the Timer is forced to Auto-Reload on Timer 2 overflow.

2.8. Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the Timer on.

Table 7. As a Timer

MODE	T2CON	
	INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
16–bit Auto–Reload	00H	08H
16–bit Capture	01H	09H
BAUD rate generator receive & transmit same baud rate	34H	36H
receive only	24H	26H
transmit only	14H	16H

Table 8. As a Counter

MODE	T2CON	
	INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
16–bit Auto–Reload	02H	0AH
16–bit Capture	03H	0BH

Notes : 1. Capture/Reload occurs only Timer/Counter overflow.
2. Capture/Reload occurs on Timer/Counter overflow and a 1 to 0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generating mode.

SCON : Serial Port Control Register (Bit Addressable)

SM0	SM1	SM2	REN	TN8	RB8	TI	RI

SM0 SCON.7 Serial Port mode specifier (NOTE 1).

SM1 SCON.6 Serial Port mode specifier (NOTE 1).

SM2 SCON.5 Enables the multiprocessor communication feature in mode 2 & 3. In mode 2 or 3, if SM2 is set to 1 then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In mode 0, SM2 should be 0 (See table 9).

REN SCON.4 Set/Cleared by software to Enable/Disable reception.

TB8 SCON.3 The 9th bit that will be transmitted in modes 2 & 3. Set/Cleared by software.

RB8 SCON.2 In modes 2 & 3, is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.

TI SCON.1 Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes. Must be cleared by software.

RI SCON.0 Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or half way through the stop bit time in the other modes (except see SM2). Must be cleared by software.

Note 1 :

SM0	SM1	MODE	DESCRIPTION	BAUD RATE
0	0	0	SHIFT REGISTER	Fosc./12
0	1	1	8 bit UART	Variable
1	0	2	8 bit UART	Fosc./64 OR Fosc./32
1	1	3	8 bit UART	Variable

2.9. Serial Port Set-Up

Table 9.

MODE	SCON	SM2 VARIATION
0	10H	
1	50H	Single Processor
2	90H	Environment
3	D0H	(SM2 = 0)
0	NA	
1	70H	Multiprocessor
2	B0H	Environment
3	F0H	(SM2 = 1)

2.10. Generating Baud Rates

Serial Port in Mode 0 :
Mode 0 has a fixed baud rate which is 1/12 of oscillator frequency. To run serial port in this mode none of the Timer/Counters need to be set up. Only the SCON register needs to be defined.

$$\text{Baud Rate} = \frac{\text{Osc Freq}}{12}$$

Serial Port in Mode 1 :
Mode 1 has a variable baud rate. The baud rate can be generated by either Timer 1 or Timer 2 (80C52, 83C154 and 83C154D only).

2.11. Using Timer/Counter 1 to Generate Baud Rates

For this purpose, Timer 1 is used in mode 2 (Auto-Reload). Refer to Timer Setup section of this chapter.

$$\text{Baud Rate} = \frac{K \times \text{Oscillator freq.}}{32 \times 12 \times [256-(TH1)]}$$

if SMOD = 0, then K = 1.

If SMOD = 1, then K = 2. (SMOD is the PCON register). Most of the time the user knows the baud rate and needs to know the reload value for TH1. Therefore, the equation to calculate TH1 can be written as :

$$TH1 = 256 - \frac{K \times \text{Oscillator freq.}}{384 \times \text{baud rate}}$$

TH1 must be integer value. Rounding off TH1 to the nearest integer may not produce the desired baud rate. In this case, the user may have to choose another crystal frequency.

Since the PCON register is not bit addressable, one way to set the bit is logical ORing the PCON register (ie, ORL PCON, #80H). The address of PCON is 87H.

2.12. Using Timer/Counter 2 to Generate Baud Rates

For this purpose, Timer 2 must be used in the baud rate generating mode. Refer to Timer 2 Setup Table in this chapter. If Timer 2 is being clocked through pin T2 (P1.0) the baud rate is :

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

And if it being clocked internally the baud rate is :

$$\text{Baud Rate} = \frac{\text{Osc. Freq}}{32 \times [65536 - (RCAP2H,\ RCAP2L)]}$$

To obtain the reload value for RCAP2H and RCAP2L the above equation can be written as :

$$RCAP2H,\ RCAP2L = 65536 - \frac{\text{Osc. Freq}}{32 \times \text{Baud rate}}$$

2.13. Serial Port in Mode 2

The baud rate is fixed in this mode and 1/32 or 1/64 of the oscillator frequency depending on the value of the SMOD bit in the PCON register.

In this mode none of the Timers are used and the clock comes from the internal phase 2 clock.

SMOD = 1, Baud Rate = 1/32 Osc Freq.

SMOD = 0, Baud Rate = 1/64 Osc Freq.

To set the SMOD bit : ORL PCON, #80H. The address of PCON is 87H.

2.14. Serial Port in Mode 3

The baud rate in mode 3 is variable and sets up exactly the same as in mode 1.

Table 10. TEMIC C51 Instruction Set

Interrupt Response time : Refer to Hardware Description Chapter.

Instructions that Affect Flag Settings (1)

INSTRUC.	FLAG			INSTRUC.	FLAG		
	C	OV	AC		C	OV	AC
ADD	X	X	X	CLRC	O		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	0	X		ANL C,/ bit	X		
DIV	0	X		ORL C, bit		X	
DA	X			ORL C, bit		X	
RRC	X			MOV C, bit		X	
RLC	X			CJNE	X		
SETB C	1						

(1) note that operations on SFR byte address 208 or bit addresses 209–215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

Note on instruction set and addressing modes :

Rn	– Register R7–R0 of the currently selected Register Bank
direct	– 8-bit internal data location's address. This could be an Internal Data RAM location (0–127) or a SFR (i.e., I/O port, control register, status register, etc. (128–255)).
@Ri	– 8-bit internal data RAM location (0-255) addresses indirectly through register R1 or R0.
# data	– 8-bit constant included in instruction.
# data 16	– 16-bit constant included in instruction.
addr 16	– 16-bit destination address. Used by LCALL & LJMP. Abranch can be anywhere within the 64K-byte Program memory address space
addr 11	– 11-bit destination address. Used by ACALL & AJMP. The branch will be within the same 2K–byte page of program memory as the first byte of the following instruction
rel	– Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditionnal jumps. Range is –128 to + 127 bytes relative to first byte of the following instruction.
bit	– Direct Addressed bit in internal Data RAM or special Function Register.

MNEMONIC	DESCRIPTION	BYTE	OSCIL. PERIOD
ARITHMETIC OPERATIONS			
ADD A, Rn	Add register to Accumulator	1	12
ADD A, direct	Add direct byte to Accumulator	2	12
ADD A, @Ri	Add indirect RAM to Accumulator	1	12
ADD A, #data	Add immediate data to Accumulator	2	12
ADDCA, Rn	Add register to Accumulator with Carry	1	12
ADDCA, direct	Add direct byte to Accumulator with Carry	2	12
ADDCA, @Ri	Add indirect RAM to Accumulator with Carry	1	12
ADDCA, #data	Add immediate data to Acc with Carry	2	12
SUBB A, Rn	Subtract Register from Acc with borrow	1	12
SUBB A, direct	Subtract direct byte from Acc with borrow	2	12
SUBB A, @Ri	Subtract indirect RAM from ACC with borrow	1	12
SUBB A, #data	Subtract immediate data from Acc with borrow	2	12
INC A	Increment Accumulator	1	12
INC Rn	Increment register	1	12
INC direct	Increment direct byte	2	12
INC @Ri	Increment direct RAM	1	12
DEC A	Decrement Accumulator	1	12
DEC Rn	Decrement Register	1	12
DEC direct	Decrement direct byte	2	12
DEC @Ri	Decrement indirect RAM	1	12
INC DPTR	Increment Data Pointer	1	24
MUL AB	Multiply A & B	1	48
DIV AB	Divide A by B	1	48
DA A	Decimal Adjust Accumulator	1	12

MNEMONIC	DESCRIPTION	BYTE	OSCIL. PERIOD
LOGICAL OPERATIONS			
ANL A, Rn	AND Register to Accumulator	1	12
ANL A, direct	AND direct byte to Accumulator	2	12
ANL A, @Ri	AND indirect RAM to Accumulator	1	12
ANL A, #data	AND immediate data to Accumulator	2	12
ANL direct, A	AND Accumulator to direct byte	2	12
ANL direct, #data	AND immediate data to direct byte	3	24
ORL A, Rn	OR register to Accumulator	1	12
ORL A, direct	OR direct byte to Accumulator	2	12
ORL A, @Ri	OR indirect RAM to Accumulator	1	12
ORL A, #data	OR immediate data to Accumulator	2	12
ORL direct, A	OR Accumulator to direct byte	2	12
ORL direct, #data	OR immediate data to direct byte	3	24
XRL A, Rn	Exclusive-OR register to Accumulator	1	12
XRL A, direct	Exclusive-OR direct byte to accumulator	2	12
XRL A, @Ri	Exclusive-OR indirect RAM to Accumulator	1	12
XRL A, #data	Exclusive–OR immediate data to Accumulator	2	12
XRL direct, A	Exclusive–OR Accumulator to direct byte	2	12
XRL direct, #data	Exclusive–OR immediate data to direct byte	3	24
CLR A	Clear Accumulator	1	12
CPL A	Complement Accumulator	1	12
RL A	Rotate Accumulator Left	1	12
RLC A	Rotate Accumulator Left through the Carry	1	12
RR A	Rotate Accumulator Right	1	12
RRC A	Rotate Accumulator Right through the Carry	1	12
SWAP A	Swap nibbles within the Accumulator	1	12

MNEMONIC	DESCRIPTION	BYTE	OSCIL. PERIOD
DATA TRANSFERT			
MOV A, Rn	Move Register to Accumulator	1	12
MOV A, direct	Move direct byte to Accumulator	2	12
MOV A, @Ri	Move indirect RAM to Accumulator	1	12
MOV A, #data	Move immediate data to Accumulator	2	12
MOV Rn, A	Move Accumulator to register	1	12
MOV Rn, direct	Move direct byte to register	2	24
MOV Rn, #data	Move immediate data to register	2	12
MOV direct, A	Move Accumulator to direct byte	2	12
MOV direct, Rn	Move register to direct byte	2	24
MOV direct, direct	Move direct byte to direct	3	24
MOV direct, @Ri	Move indirect RAM to direct byte	2	24
MOV direct, #data	Move immediate data to direct byte	3	24
MOV @Ri, A	Move Accumulator to indirect RAM	1	12
MOV @Ri, direct	Move direct by to indirect RAM	2	24
MOV @Ri, #data	Move immediate data to indirect RAM	2	12
MOV DPTR, #data16	Load Data Pointer with a 16–bit constant	3	24
MOVCA @A+DPTR	Move Code byte relative to DPTR to Acc	1	24
MOVCA @A+PC	Move Code byte relative to PC to Acc	1	24
MOVXA, @Ri	Move External RAM (8-bit addr) to Acc	1	24
MOVXA, @DPTR	Move External RAM (16-bit addr) to Acc	1	24
MOVX@Ri, A	Move Acc to External RAM (8-bit addr)	1	24
MOVX@DPTR, A	Move Acc to External RAM (16-bit addr)	1	24
PUSH direct	Push direct byte only stack	2	24
POP direct	Pop direct byte from stack	2	24

MNEMONIC	DESCRIPTION	BYTE	OSCIL. PERIOD
DATA TRANSFERT (continued)			
XCH A, Rn	Exchange register with Accumulator	1	12
XCH A, direct	Exchange direct byte with Accumulator	2	12
XCH A, @Ri	Exchange indirect RAM with Accumulator	1	12
XCHD A, @Ri	Exchange loworder Digit indirect RAM with Acc	1	12
BOOLEAN VARIABLE MANIPULATION			
CLR C	Clear Carry	1	12
CLR bit	Clear direct bit	2	12
SETB C	Set Carry	1	12
SETB bit	Set direct bit	2	12
CPL C	Complement Carry	1	12
CPL bit	Complement direct bit	2	12
ANL C, bit	AND direct bit to Carry	2	24
ANL C, /bit	AND complement of direct bit to Carry	2	24
ORL C, bit	OR direct bit to Carry	2	24
ORL C, /bit	OR complement of direct bit to Carry	2	24
MOV C, bit	Move direct bit to Carry	2	12
MOV bit, C	Move Carry to direct bit	2	24
JC rel	Jump if Carry is set	2	24
JNC rel	Jump if Carry not set	2	24
JB bit, rel	Jump if direct Bit is set	3	24
JNB bit, rel	Jump if direct Bit is Not set	3	24
JBC bit, rel	Jump if direct Bit is set & clear bit	3	24

MNEMONIC	DESCRIPTION	BYTE	OSCIL. PERIOD
PROGRAM BRANCHING			
ACALLK addr11	Absolute Subroutine Call	2	24
LCALL addr16	Long Subroutine Call	3	24
RET	Return from Subroutine	1	24
RETI	Return from interrupt	1	24
AJMPaddr11	Absolute Jump	2	24
LJMPaddr16	Long Jump	3	24
SJMP rel	Short Jump (relative addr)	2	24
JMP @A+DPTR	Jump direct relative to the DPTR	1	24
JZ rel	Jump if Accumulator is zero	2	24
JNZ rel	Jump if Accumulator is not Zero	2	24
CNJE A, direct, rel	Compare direct byte to Acc and Jump if Not Equal	3	24
CJNE A, #data, rel	Compare immediate to Acc and Jump if Not Equal	3	24
CJNE Rn, #data, rel	Compare immediate to register and Jump if Not Equal	3	24
CJNE @Ri, #data, rel	Compare immediate to indirect and Jump if Not Equal	3	24
DJNZ Rn, rel	Decrement register and Jump if Not Zero	2	24
DJNZ direct, rel	Decrement direct byte and Jump if Not Zero	3	24
NOP	No Operation	1	12

3. Instruction Definitions

ACALL addr 11

Function : Absolute Call

Description : ACALL unconditionally calls a subroutine located at the indicated address. The instruction increments the PC twice to obtain the address of the following instruction, then pushes the 16-bit result onto the stack (low-order byte first) and increments the Stack Pointer twice. The destination address is obtained by successively concatenating the five high-order bits of the incremented PC, opcode bits 7-5, and the second byte of the instruction. The subroutine called must therefore start within the same 2 K block of the program memory as the first byte of the instruction following ACALL. No flags are affected.

Example : Initially SP equals 07H. The labs " SUBRTN " is at program memory location 0345 H. After executing the instruction,

ACALL SUBRTN

at location 0123H, SP will contain 09H, internal RAM locations 08H and 09H will contain 25H and 01H, respectively, and the PC will contain 0345H.

Bytes : 2

Cycles : 2

Encoding :

a10	a9	a8	1	0	0	0	1	a7	a6	a5	a4	a3	a2	a1	a0

Operation :

ACALL
(PC) ← (PC) + 2
(SP) ← (SP) + 1
[(SP)] ← (PC_{7-0})
(SP) ← (SP) + 1
[(SP)] ← (PC_{15-8})
(PC_{10-0}) ← page address

ADD a, <src-byte>

Function : Add

Description : ADD adds the byte variable indicated to the Accumulator, leaving the result in the Accumulator. The carry and auxiliary-carry flags are set, respectively, if there is a carry-out from bit 7 or bit 3, and cleared otherwise. When adding unsigned integers, the carry flag indicates an overflow occured.

OV is set there is a carry-out of bit 6 but not out of bit 7, or a carry-out of bit 7 but not bit 6 ; otherwise OV is cleared. When adding signed integers, OV indicates a negative number produced as the sum of two positive operands, or a positive sum from two negative operands.

Four source operand addressing modes are allowed : register, direct, register-indirect, or immediate.

Example : The Accumulator holds 0C3H (11000011B) and register 0 holds 0AAH (10101010B). The instruction,

ADD A, R0

will leave 6DH (01101101B) in the Accumulator with the AC flag cleared and both the carry flag and OV set to 1.

ADD A, Rn

Byte : 1

Cycle : 1

Encoding :

0	0	1	0	1	r	r	r

Operation : ADD
(A) ← (A) + (Rn)

ADD A, direct

Bytes : 2

Cycle : 1

Encoding :

0	0	1	0	0	1	0	1	direct address

Operation : ADD
(A) ← (A) + (direct)

ADD A, @RI

Byte : 1

Cycle : 1

Encoding :

0	0	1	0	1	1	1	i

Operation : ADD
(A) ← (A) + ((RI))

ADD A, # data

Bytes : 2

Cycle : 1

Encoding :

0	0	1	0	0	1	0	0	Immediate data

Operation : ADD
(A) ← (A) + # data

ADDC A, <src-byte>

Function : Add with Carry

Description : ADDC simultaneously adds the byte variable indicated, the carry flag and the Accumulator contents, leaving the result in the Accumulator. The carry and auxiliary-carry or bit flags are set, respectively, if there is a carry-out from bit 7 or bit 3, and cleared otherwise. When adding unsigned integers, the carry flag indicates an overflow occured.

OV is set if there is a carry-out of bit 6 but not out of bit 7, or a carry-out of bit 7 but not out of bit 6 ; otherwise OV is cleared. When adding signed intergers, OV indicates a negative number produced as the sum of two positive operands or a positive sum from two negative operands.

Four source operand addressing mode are allowed ; register, direct, register-indirect, or immediate.

Example : The Accumulator holds 0C3H (11000011B) and register 0 holds 0AAH (10101010B) with the carry flag set. The instruction,

ADDC A, R0

will leave 6EH (01101110B) in the Accumulator with AC cleared and both the Carry flag and OV set to 1.

ADDC A, RN

Byte : 1

Cycle : 1

Encoding :

0	0	1	1	1	r	r	r

Operation : ADDC
$(A) \leftarrow (A) + (C) + (R_n)$

ADDC A, direct

Bytes : 2

Cycle : 1

Encoding :

0	0	1	1	0	1	0	1	direct address

Operation : ADDC
$(A) \leftarrow (A) + (C) + (direct)$

ADDC A, @ RI

Byte : 1

Cycle : 1

Encoding :

0	0	1	1	0	1	1	i

Operation : ADDC
$(A) \leftarrow (A) + (C) + ((R_i))$

ADDC A, #data

Bytes : 2

Cycle : 1

Encoding :

0	0	1	1	0	1	0	0	immediate data

Operation : ADDC
$(A) \leftarrow (A) + (C) + \#\ data$

AJMP addr11

Function : Absolute Jump

Description : AJMP transfers program execution to the indicated address, which is formed at run-time by concatenating the high-order five bits of the PC (*after* incrementing the PC twice), opcode bits 7-5, and the second byte of the instruction. The destination must therefore be within the same 2 K block of program memory as the first byte of the instruction following AJMP.

Example : The label " JMPADR " is at program memory location 0123H. The instruction,
AJMP JMPADR
is a location 0345H and will load the PC with 0123H.

ADD A, direct

Bytes : 2
Cycles : 2

Encoding :

a10	a9	a8	0	0	0	0	1	a7	a6	a5	a4	a3	a2	a1	a0

Operation : AJMP
(PC) ← (PC) + 2
($PC_{10\text{-}0}$) ← page address

ANL <dest-byte>, <src-byte>

Function : Logical-AND for byte variables

Description : ANL performs the bitwise logical-AND operation between the variables indicated and stores the results in the destination variable. No flags are affected. The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing ; when the destination is a direct address, the source can be the Accumulator or immediate data. *Note* : When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example : If the Accumulator holds 0C3H (11000011B) and register 0 holds 55H (01010101B) then the instruction,
ANL A, R0
will leave 41H (01000001B) in the Accumulator.
When the destination is a directly addressed byte, this instruction will clear combinations of bits in any RAM location or hardware register. The mask byte determining the pattern of bits to be cleared would either be a constant contained in the instruction or a value computed in the Accumulator at run-time. The instruction,
ANL P1, #01110011B
will clear bits 7, 3, and 2 of output port 1.

ANL A, Rn

Bytes : 1
Cycles : 1

Encoding :

0	1	0	1	1	r	r	r

Operation : ANL
(A) ← (A) ∧ (Rn)

ANL A, direct

Bytes : 2
Cycles : 1

Encoding :

0	1	0	1	0	1	0	1	direct address

Operation : ANL
(A) ← (A) ∧ (direct)

ANL A, @ RI

Byte : 1

Cycle : 1

Encoding :

0	1	0	1	0	1	1	i

Opération : ANL
(A) ← (A) ∧ ((Ri))

ANL A, #DATA

Bytes : 2

Cycle : 1

Encoding :

0	1	0	1	0	1	0	0	immediate data

Operation : ANL
(A) ← (A) ∧ # data

ANL direct, A

Bytes : 2

Cycle : 1

Encoding :

0	1	0	1	0	0	1	0	direct address

Operation : ANL
(direct) ← (direct) ∧ (A)

ANL direct, # data

Bytes : 3

Cycles : 2

Encoding :

0	1	0	1	0	0	1	1	direct address	immediate data

Operation : ANL
(direct) ← (direct) ∧ # data

ANL C, <src-bit>

Function : Logical-AND for bit variables

Description : If the Boolean value of the source bit is logical 0 then clear the carry flag ; otherwise leave the carry flag in its current state. A slash (" / ") preceding the operand in the assembly language indicates that the logical complement of the addressed bit is used as the source value, *but the source bit itself is not affected.* No other flags are affected.

Only direct addressing is allowed for the source operand.

Example : Set the carry flag if, P1.0 = 1, ACC.7 = 1, and OV = 0 :

```
MOV C, P1.0          ; LOAD CARRY WITH INPUT PIN STATE
ANL C, ACC.7           ; AND CARRY WITH ACCUM. BIT 7
ANL C,/OV              ; AND WITH INVERSE OF OVERFLOW FLAG
```

ANL C, bit

Bytes : 2

Cycles : 2

Encoding :

1 0 0 0 0 0 1 0	bit address

Operation :

ANL
(C) ← (C) ∧ (bit)

ANL C, /bit

Bytes : 2

Cycles : 2

Encoding :

1 0 1 1 0 0 0 0	bit address

Operation :

ANL
(C) ← (C) ∧ $\overline{(bit)}$

CJNE<dest-byte>, <src-byte>, rel

Function : Compare and Jump if Not Equal

Description : CJNE compares the magnitudes of the first two operands, and branches if their values are not equal. The branch destination is computed by adding the signed relative-displacement in the last instruction byte to the PC, after incrementing the PC to the start of the next instruction. The carry flag is set if the unsigned integer value of <dest-byte> is less than the unsigned integer value of <src-byte> ; otherwise, the carry is cleared. Neither operand is affected.

The first two operands allow four addressing mode combinations : the Accumulator may be compared with any directly addressed byte or immediate data, and any indirect RAM location or working register can be compared with an immediate constant.

Example : The Accumulator contains 34H, register 7 contains 56H. The first instruction in the sequence,

```
                CJNE    R7, #60H, NOT_EQ
;               ...     ...             ; R7 = 60H
NOT_EQ :        JC      REQ_LOW         ; IF R7 < 60H
;               ...     ...             ; R7 > 60H
```

sets the carry flag and branches to the instruction at label NOT-EQ. By testing the carry flag, this instruction determines whether R7 is greater or less than 60H.

If the data being presented to Port 1 is also 34H, then the instruction,

WAIT : CJNE A, P1, WAIT

clears the carry flag and continues with the next instruction in sequence, since the Accumulator does equal the data read from P1. (If some other value was being input on P1, the program will loop at this point until the P1 data changes to 34H).

CJNE A, direct, rel

Bytes : 3
Cycles : 2

Encoding :

1 0 1 1 0 1 0 1	direct address	rel. address

Operation :

(PC) ← (PC) + 3
IF (A) <> (direct)
THEN
    (PC) ← (PC) + *relative offset*
IF (A) < (direct)
THEN
    (C) ← 1
ELSE
    (C) ← 0

CJNE A, # data, rel

Bytes : 3
Cycles : 2

Encoding :

1 0 1 1 0 1 0 0	immediate data	rel. address

Operation :

(PC) ← (PC) + 3
IF (A) <> *(data)*
THEN
    (PC) ← (PC) + *relative offset*
IF (A) < data
THEN
    (C) ← 1
ELSE
    (C) ← 0

CJNE Rn, # data, rel

Bytes : 3
Cycles : 2

Encoding :

1 0 1 1 1 r r r	immediate data	rel. address

Operation :

(PC) ← (PC) + 3
IF (Rn) <> *data*
THEN
    (PC) ← (PC) + *relative offset*
IF (Rn) < *data*
THEN
    (C) ← 1
ELSE
    (C) ← 0

CJNE @Ri, # data, rel

Bytes : 3
Cycles : 2

Encoding :

1 0 1 1 0 1 1 i	immediate data	rel. address

Operation :

(PC) ← (PC) + 3
IF (Ri) <> *data*
THEN
    (PC) ← (PC) + *relative offset*
IF ((Ri)) < *data*
THEN
    (C) ← 1
ELSE
    (C) ← 0

CLR A

Function : Clear Accumulator

Description : The Accumulator is cleared (all bits set on zero). No flags are affected.

Example : The Accumulator contains 5CH (01011100B). The instruction,
CLRA
Will leave the Accumulator set to 00H (00000000B).

Bytes : 1

Cycles : 1

Encoding :

1	1	1	1	0	1	0	0

Operation : CLR
(A) ← 0

CLR bit

Function : Clear bit

Description : The indicated bit is cleared (reset to zero). No other flags are affected. CLR can operate on the carry flag or any directly addressable bit.

Example : Port 1 has previously been written with 5DH (01011101B). The instruction,
CLR P1.2
will leave the port set to 59H (01011001B).

CLR C

Bytes : 1

Cycles : 1

Encoding :

1	1	0	0	0	0	1	1

Operation : CLR
(C) ← 0

CLR bit

Bytes : 2

Cycles : 1

Encoding :

1	1	0	0	0	0	1	0	bit address

Operation : CLR
(bit) ← 0

CPLA

Function : Complement Accumulator

Descritpion : Each bit of the Accumulator is logically complemented (one's complement). Bits which previously contained a one are changed to a zero and vice-versa. No flags are affected.

Example : The accumulator contains 5CH (01011100B). The instruction,
CPLA
will leave the Accumulator set to 0A3H (10100011B).

Bytes : 1

Cycles : 1

Encoding :

1	1	1	1	0	1	0	0

Operation : CPL
(A) ← $\overline{(A)}$

CPL bit

Function : Complement bit

Description : The bit variable specified is complemented. A bit which had been a one is changed to zero and vice-versa. No other flags are affected. CLR can operate on the carry or any directly addressable bit.
Note : When this instruction is used to modify an output pin, the value used as the original data will be read from the output data latch, not the input pin.

Example : Port 1 has previously been written with 5BH (01011101B). The instruction sequence.
CPL P1.1
CPL P1.2
will leave the port set to 5BH (01011011B).

CPL C

Bytes : 1

Cycles : 1

Encoding :

1	0	1	1	0	0	1	1

Operation :
CPL
$(C) \leftarrow \overline{(C)}$

CPL bit

Bytes : 2

Cycles : 1

Encoding :

1	0	1	1	0	0	1	0	bit address

Operation :
CPL
$(bit) \leftarrow \overline{(bit)}$

DA A

Function : Decimal-adjust Accumulator for Addition

Description : DA A adjusts the eight-bit value in the Accumulator resulting from the earlier addition of two variables (each in packed-BCD format), producing two four-bit digits, Any ADD or ADDC instruction may have been used to perform the addition.

If Accumulator bits 3-0 are greater than nine (xxxx1010-xxxx1111), or if the AC flag is one, six is added to the Accumulator producing the proper BCD digit in the low-order nibble. This internal addition would set the carry flag if a carry-out of the low-order four-bit field propagated through all high-order bits, but it would not clear the carry flag otherwise.

If the carry flag is now set, or if the four high-order bits now exceed nine (1010xxxx -111xxxx), these high-order bits are incremented by six, producing the proper BCD digit in the high-order nibble. Again, this would set the carry flag if there was a carry-out of the high-order bits, but wouldn't clear the carry. The carry flag thus indicates if the sum of the original two BCD variables is greater than 100, allowing multiple precision decimal. OV is not affected.

All of this occurs during the one instruction cycle. Essentially, this instruction performs the decimal conversion by adding 00H, 06H, 60H, or 66H to the Accumulator, depending on initial Accumulator and PSW conditions.

Note : DA A *cannot* simply convert a hexadecimal number in the Accumulator to BCD notation, nor does DA A apply to decimal substraction.

Example : The Accumulator holds the value 56H (01010110B) representing the packed BCD digits of the decimal number 56. Register 3 contains the value 67H (01100111B) representing the packed BCD digits of the decimal number 67. The carry flag is set. The instruction sequence.

```
ADDCA, R3
DA     A
```

will first perform a standard twos-complement binary addition, resulting in the value 0BEH (10111110), in the Accumulator. The carry and auxillary carry flags will be cleared.

The decimal Adjust instruction will then after the Accumulator to the value 24H (00100100B) indicating the packed BCD digits of the decimal number 24, the low-order two digits of the decimal sum of 56,67, and the carry-in. The carry flag will set by the Decimal Adjust instruction, indicating that a decimal overflow occured. The true sum 56,67, and 1 is 124. BCD variables can be incremented or decremented by adding 01H or 99H. If the Accumulator initially holds 30H (representing the digits of 30 decimal), then the instruction sequence,

```
ADD  A, #99H
DA   A
```

will leave the carry set and 29H in the Accumulator, since 30 + 99 = 129. The low-order byte of the sum can be interpreted to mean 30 -1 = 29.

Bytes : 1

Cycles : 1

Encoding :

1	1	0	1	0	1	0	0

Operation :

```
DA
– contents of Accumulator are BCD
IF [[(A3 – 0) > 9] V [(AC) = 1]]
      THEN (A3 – 0) ← (A3 – 0) + 6
            AND
IF [[(A7 – 4) > 9] V [(C) = 1]]
      THEN (A7 – 4) ← (A7 – 4) + 6
```

DEC byte

Function : Decrement

Description : The variable indicated is decremented by 1. An original value of 00H will underflow to 0FFH. No flags are affected. Four operand addressing modes are allowed : accumulator, register, direct, or register-indirect.

Note : When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example : Register 0 contains 7FH (01111111B). Internal RAM locations 7 EH and 7FH contain 00H and 40H, respectively. The instruction sequence.

DEC @ R0

DEC R0

DEC @ R0

will leave register 0 set to 7EH internal RAM locations 7EH and 7FH to 0FFH and 3FH.

DEC A

Bytes : 1

Cycles : 1

Encoding :

0	0	0	1	0	1	0	0

Operation : DEC
(A) ← (A) - 1

DEC Rn

Bytes : 1

Cycles : 1

Encoding :

0	0	0	1	1	r	r	r

Operation : DEC
(Rn) ← (Rn) - 1

DEC direct

Bytes : 2

Cycles : 1

Encoding :

0	0	0	1	0	1	0	1	direct address

Operation : DEC
(direct) ← (direct) - 1

DEC @ RI

Bytes : 1

Cycles : 1

Encoding :

0	0	0	1	0	1	1	i

Operation : DEC
((Ri)) ← ((Ri)) - 1

DIV AB

Function : Divide

Description : DIV AB divides the unsigned eight-bit integer in the Accumulator by the unsigned eight-bit integer in register B. The Accumulator receives the integer part of the quotient ; register B receives the integer remainder. The carry and OV flags will be cleared. *Exception* : If B had originally contained 00H ; the values returned in the Accumulator and B-register will be undefined and the overflow flag will be set. The carry flag is cleared in any case.

Example : The Accumulator contains 251 (0FBH or 11111011B) and B contains 18 (12H or 00010010B). The instruction,

DIV AB

will leave 13 in the Accumulator (0DH or 00001101B) and the value 17 (11H or 00010001B) in B, since 251 = (13 × 18) + 17. Carry and OV will both be cleared.

Bytes : 1

Cycles : 4

Encoding :

1	0	0	0	0	1	0	0

Operation : DIV

$(A)_{15-8} \leftarrow (A)/(B)$

$(B)_{7-0}$

DJNZ <byte>, <rel-addr>

Function : Decrement and Jump if Not Zero

Description : DJNZ decrements the location indicated by 1, and branches to the address indicated by the second operand if the resulting value is not zero. An original value of 00H will underflow to 0FFH. No flags are affected. The branch destination would be computed by adding the signed relative-displacement value in the last instruction byte to the PC, after incrementing the PC to the first byte of the following instruction.

The location decremented may be a register or directly addressed byte.

Note : When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example : Internal RAM locations 40H, 50H, and 60H contain the values 01H, 70H, and 15H, respectively. the instruction sequence,

DJNZ 40H, LABEL_1

DJNZ 50H, LABEL_2

DJNZ 60H, LABEL_3

will cause a jump to the instruction at label LABEL2 with the values 00H, 6FH, and 15H in the three RAM locations. The first jump was *not* taken because the result was zero.

This instruction provides a simple way of executing a program loop a given number of times, or for adding a moderate time delay (from 2 to 512 machine cycles) with a single instruction. The instruction sequence,

```
        MOV  R2, #8
TOGGLE: CPL  P1.7
        DJNZ R2, TOGGLE
```

will toggle P1.7 eight times, causing four output pulses to appear at bit 7 of output Port 1. Each pulse will last three machine cycles ; two for DJNZ and one to after the pin.

DJNZ Rn, rel

Bytes : 2

Cycles : 2

Encoding :

1	1	0	1	1	r	r	r	rel. address

Operation :
DJNZ
(PC) ← (PC) + 2
(Rn) ← (Rn) - 1
IF (RN) > 0 or (Rn) < 0
THEN
(PC) ← (PC) + rel

DJNZ direct, rel

Bytes : 3

Cycles : 2

Encoding :

1	1	0	1	0	1	0	1	direct address	rel. address

Operation :
DJNZ
(PC) ← (PC) + 2
(direct) ← (direct) - 1
IF (direct) > 0 or (direct) < 0
THEN
(PC) ← (PC) + rel

INC <byte>

Function : Increment

Description : INC increments the indicated variable by 1. An original value of 0FFH will overflow to 00H. No flags are affected. There addressing modes are allowed : register, direct, or register-indirect.

Note : When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example : Register 0 contains 7EH (01111110B). Internal locations 7EH and 7FH contain 0FFH and 40H, respectively. The instruction sequence,

INC @R0

INC R0

INC @R0

will leave register 0 set to 7FH and internal RAM locations 7EH and 7FH holding (respectively) 00H and 41H.

INC A

Bytes : 1

Cycles : 1

Encoding :

0	0	0	0	0	1	0	0

Operation :
INC
(A) ← (A) + 1

INC Rn

Bytes : 1

Cycles : 1

Encoding :

0	0	0	0	1	r	r	r

Operation :
INC
(Rn) ← (Rn) + 1

INC direct

Bytes : 2

Cycles : 1

Encoding :

0	0	0	0	0	1	0	1	direct address

Operation : INC
(direct) ← (direct) + 1

INC @ RI

Bytes : 1

Cycles : 1

Encoding :

0	0	0	0	0	1	1	i

Operation : INC
((Ri)) ← ((Ri)) + 1

INC DPTR

Function : Increment Data Pointer

Description : Increment the 16-bit data pointer by 1.A 16-bit increment (modulo 2^{16}) is performed ; an overflow of the low-order byte of the data pointer (DPL) from 0FFH to 00H will increment the high-order byte (DPH). No flags are affected.

This is the only 16-bit register which can be incremented.

Example : Registers DPH and DPL contain 12H and 0FEH, respectively. The instruction sequence,

INC DPTR

INC DPTR

INC DPTR

will change DPH and DPL to 13H and 01H.

Bytes : 1

Cycles : 2

Encoding :

1	0	1	0	0	0	1	1

Operation : INC
(DPTR) ← (DPTR) + 1

JB bit, rel

Function : Jump if Bit set

Descritpion : If the indicated bit is a one, jump to the address indicated ; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. *The bit tested is not modified.* No flags are affected.

Note : When this instruction is used to test an output pin, the value used as the original data will be read from the output data latch, *not* the input pin.

Example : The data present at input port 1 is 11001010B. The Accumulator holds 56 (01010110B). The instruction sequence.

JB P1.2, LABEL 1 JB ACC.2, LABEL 2

will cause program execution to branch to the instruction at label LABEL 2.

Bytes : 3
Cycles : 2

Encoding :

0	0	1	0	0	0	0	0	bit address							
rel. address															

Operation :
JB
(PC) ← (PC) + 3
IF (bit) = 1
THEN
(PC) ← (PC) + rel

JBC bit, rel

Function : Jump if Bit is set and Clear bit

Description : If the indicated bit is a one, branch to the address indicated ; otherwise proceed with the next instruction. *The bit will not be cleared if it is already a zero.* The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. No flags are affected.

Note : When this instruction is used to test an output pin, the value used as the original data will be read from the output data latch, *not* the input pin.

Example : The Accumulator holds 56H (01010110B). The instruction sequence,

JBC ACC.3, LABEL 1
JBC ACC.2, LABEL 2

will cause program execution to continue at the instruction identified by the label LABEL2, with the Accumulator modified to 52H (01010010B).

Bytes : 3
Cycles : 2

Encoding :

0	0	0	1	0	0	0	0	bit address							
rel. address															

Operation :
JBC
(PC) ← (PC) + 3
IF (bit) = 1
THEN
(bit) ← 0
(PC) ← (PC) + rel

JC rel

Function : Jump if Carry is set

Description : If the carry flag is set, branch to the address indicated ; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. No flags are affected.

Example : The carry flag is cleared. The instruction sequence,

```
JC    LABEL 1
CPL   C
JC    LABEL 2
```

will set the carry and cause program execution to continue at the instruction identified by the label LABEL2.

Bytes : 2
Cycles : 2

Encoding :

0	1	0	0	0	0	0	0	rel. address							

Operation :
JC
(PC) ← (PC) + 2
IF (C) = 1
THEN
(PC) ← (PC) + rel

JMP @A + DPTR

Function : Jump indirect

Description : Add the eight-bit unsigned contents of the Accumulator with the sixteen-bit data pointer, and load the resulting sum to the program counter. This will be the address for subsequent instruction fetches. Sixteen-bit addition is performed (modulo 2^{16}) : a carry-out from the low-order eight bits propagates through the higher-order bits. Neither the Accumulator nor the Data Pointer is altered. No flags are affected.

Example : An even number from 0 to 6 is in the Accumulator. The following sequence of instructions will branch to one of four AJMP instructions in a jump table starting at JMP-TBL :

```
                MOV     DPTR, #JMP_TBL
                JMP     @ A + DPTR
JMP_TBL :       AJMP    LABEL0
                AJMP    LABEL1
                AJMP    LABEL2
                AJMP    LABEL3
```

If the Accumulator equals 04H when starting this sequence, execution will jump to label LABEL2. Remembers that AJMP is a two-byte instruction, so the jump instructions start at every other address.

Bytes : 1

Cycles : 2

Encoding :

0	1	1	1	0	0	1	1

Operation :

JMP
(PC) ← (A) + (DPTR)

JNB bit, rel

Function : Jump if Bit not set

Description : If the indicated bit is a zero, branch to the indicated address ; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. *The bit tested is not modified.* No flags are affected.

Example : The data present at input port 1 is 11001010B. The Accumulator holds 56H (01010110B). The instruction sequence,

```
JNB P1.3, LABEL1
JNB ACC3, LABEL2
```

will cause program execution to continue at the instruction at label LABEL2.

Bytes : 3

Cycles : 2

Encoding :

0	0	1	1	0	0	0	0	bit address	rel. address

Operation :

JNB
(PC) ← (PC) + 3
IF (bit) = 0
THEN (PC) ← (PC) + rel

JNC rel

Function : Jump if Carry not set

Description : If the carry flag is a zero, branch to the address indicated ; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice to point to the next instruction. The carry flag is not modified.

Example : The carry flag is set. The instruction sequence,

```
JNC LABEL1
CPLC
JNC LABEL2
```

will clear the carry and cause program execution to continue at the instruction identified by the label LABEL2.

Bytes : 2

Cycles : 2

Encoding :

0	1	0	1	0	0	0	0	rel. address

Operation :

```
JNC
(PC) ← (PC) + 2
IF (C) = 0
        THEN (PC) ← (PC) + rel
```

JNZ rel

Function : Jump if Accumulator Not Zero

Description : If any bit of the Accumulator is a one, branch to the indicated address ; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. The Accumulator is not modified. No flags are affected.

Example : The Accumulator originally holds 00H. The instruction sequence,

```
JNZ LABEL1
INC A
JNZ LABEL2
```

will set the Accumulator to 01H and continue at label LABEL2.

Bytes : 2

Cycles : 2

Encoding :

0	1	1	1	0	0	0	0	rel. address

Operation :

```
JNZ
(PC) ← (PC) + 2
IF (A) ≠ 0
        THEN (PC) ← (PC) + rel
```

JZ rel

Function : Jump if Accumulator Zero

Description : If all bits of the Accumulator are zero, branch to the address indicated ; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. The Accumulator is not modified. No flags are affected.

Example : The Accumulator originally contains 01H. The instruction sequence.

```
JZ      LABEL1
DEC     A
JZ      LABEL2
```

will change the Accumulator to 00H and cause program execution at the instruction identified by the label LABEL2.

Bytes : 2

Cycles : 2

Encoding :

Operation :

JZ
(PC) ← (PC) + 2
IF (A) = 0
THEN (PC) ← (PC) + rel

LCALL addr16

Function : Long call

Description : LCALL calls a subroutine located at the indicated address. The instruction adds three to the program counter to generate the address of the next instruction and then pushes the 16-bit result onto the stack (low byte first), incrementing the Stack Pointer by two. The high-order and low-order bytes of the PC are then loaded, respectively, with the second and third bytes of the LCALL instruction. Program execution continues with the instruction at this address. The subroutine may therefore begin anywhere in the full 64K-byte program memory address space. No flags are affected.

Example : Initially the Stack Pointer equals 07H. The label " SUBRTN " is assigned to program memory location 1234H. After executing the instruction,

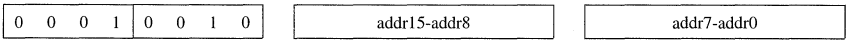
LCALL SUBRTN

at location 0123H, the Stack Pointer will contain 09H, internal RAM locations 08H and 09H will contain 26H and 01H, and the PC will contain 1235H.

Bytes : 3

Cycles : 2

Encoding :



Operation :

LCALL
(PC) ← (PC) + 3
(SP) ← (SP) + 1
((SP)) ← (PC_{7-0})
(SP) ← (SP) + 1
((SP)) ← (SP_{15-8})
(PC) ← $addr_{15-0}$

LJMP addr16

Function : Long Jump

Description : LJMP causes an unconditional branch to the indicated address, by loading the high-order and low-order bytes of the PC (respectively) with the second and third instruction bytes. The destination may therefore be anywhere in the full 64K program memory address space. No flags are affected.

Example : The label " JMPADR " is assigned to the instruction at program memory location 1234H. The instruction,

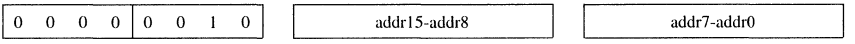
LJMP JMPADR

at location 0123H will load the program counter with 1234H.

Bytes : 3

Cycles : 2

Encoding :



Operation : LJMP
(PC) ← $addr_{15-0}$

MOV <dest-byte>, <src-byte>

Function : Move byte variable

Description : The byte variable indicated the second operand is copied into the location specified by the first operand. The source byte is not affected. No other register or flag is affected.

This is by far the most flexible operation. Fifteen combinaisons of source and destination addressing modes are allowed.

Example : Internal RAM location 30H holds 40H. The value of RAM location 40H is 10H. The data present at input port 1 is 11001010B (0CAH).

```
MOV     R0, #30H        ; R0 <= 30h
MOV     A, @ R0         ; A <= 40H
MOV     R1, A           ; R1 <= 40h
MOV     R, @ R1         ; B <= 10h
MOV     @ R1, P1        ; RAM (40H) <= OCAH
MOV     P2, P1          ; P2 # 0CAH
```

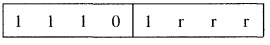
leaves the value 30H in register 0,40H in both the Accumulator and register 1,10H in register B, and 0CAH (11001010B) both in RAM location 40H and output on port 2.

MOV A, Rn

Bytes : 1

Cycles : 1

Encoding :



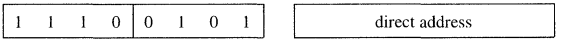
Operation : MOV
(A) ← (Rn)

*MOV A,direct

Bytes : 2

Cycles : 1

Encoding :



Operation : MOV
(A) ← (direct)

*MOV A, ACC is not valid instruction.

MOV A,@ RI

Bytes : 1

Cycles : 1

Encoding :

1	1	1	0	0	1	1	i

Operation : MOV
(A) ← (Ri)

MOV A, # data

Bytes : 2

Cycles : 1

Encoding :

0	1	1	1	0	1	0	0	immediate data

Operation : MOV
(A) ← # data

MOV Rn, A

Bytes : 1

Cycles : 1

Encoding :

1	1	1	1	1	r	r	r

Operation : MOV
(Rn) ← (A)

MOV Rn, direct

Bytes : 2

Cycles : 2

Encoding :

1	0	1	0	1	r	r	r	direct addr.

Operation : MOV
(Rn) ← (direct)

MOV Rn, # data

Bytes : 2

Cycles : 1

Encoding :

0	1	1	1	1	r	r	r	immediate data

Operation : MOV
(Rn) ← # data

MOV direct, A

Bytes : 2

Cycles : 1

Encoding :

1	1	1	1	0	1	0	1	direct address

Operation : MOV
(direct) ← (A)

MOV direct, Rn

Bytes : 2

Cycles : 2

Encoding :

1	0	0	0	1	r	r	r	direct address

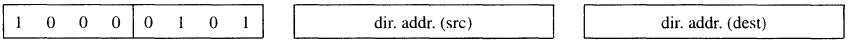
Operation : MOV
(direct) ← (Rn)

MOV direct, direct

Bytes : 3

Cycles : 2

Encoding :



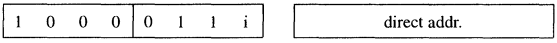
Operation : MOV
(direct) ← (direct)

MOV direct, @ Ri

Bytes : 2

Cycles : 2

Encoding :



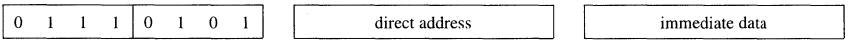
Operation : MOV
(direct) ← (Ri)

MOV direct, # data

Bytes : 3

Cycles : 2

Encoding :



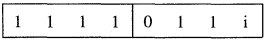
Operation : MOV
(direct) ← # data

MOV @ Ri, A

Bytes : 1

Cycles : 1

Encoding :



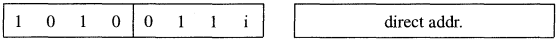
Operation : MOV
((Ri)) ← (A)

MOV @ Ri, direct

Bytes : 2

Cycles : 2

Encoding :



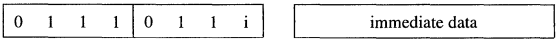
Operation : MOV
((Ri)) ← (direct)

MOV @ Ri*, data

Bytes : 2

Cycles : 1

Encoding :



Operation : MOV
((Ri)) ← # data

MOV <dest-bit>, <src-bit>

Function : More bit data

Description : The Boolean variable indicated by the second operand is copied into the location specified by the first operand. One of the operands must be the carry flag ; the other may be any directly addressable bit. No other register or flag is affected.

Example : The carry flag is originally set. The data present at input Port 3 is 11000101B. The data previously written to output Port 1 is 35H (00110101B).

```
MOV     P1.3, C
MOV     C, P3.3
MOV     P1.2, C
```

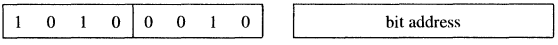
will leave the carry cleared and change Port 1 to 39H (00111001B).

MOV C, bit

Bytes : 2

Cycles : 1

Encoding :



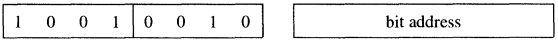
Operation :
MOV
(C) ← (bit)

MOV bit, C

Bytes : 2

Cycles : 2

Encoding :



Operation :
MOV
(bit) ← (C)

MOV DPTR, # data 16

Function : Load Data Pointer with a 16-bit constant

Description : The Data Pointer is loaded with the 16-bit constant indicated. the 16-bit constant is loaded into the second and third bytes of the instruction. The second byte (DPH) is the high-order byte, while the third byte (DPL) holds the low-order byte. No flags are affected.

This is the only instruction which moves 16-bits of data at once.

Example : The instruction,

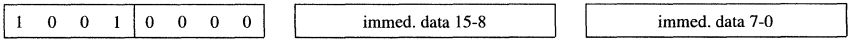
MOV DPTR, 1234H

will load the value 1234H into the Data Pointer : DPH will hold 12H and DPL will hold 34H.

Bytes : 3

Cycles : 2

Encoding :



Operation :
MOV
(DPTR) ← # $data_{15-0}$
DPH DPL ← # $data_{15-8}$ # $data_{7-0}$

MOVC A, @ A + <base-reg>

Function : Move Code byte

Description : The MOVC instructions load the Accumulator with a code byte, or constant from program memory. The address of the byte fetched is the sum of the original unsigned eight-bit. Accumulator contents and the contents of a sixteen-bit base register, which may be either the Data Pointer or the PC. In the latter case, PC is incremented to the address of the following instruction before being added with the Accumulator ; otherwise the base register is not altered. Sixteen-bit addition is performed so a carry-out from the low-order eight bits may propagate through higher-order bits. No flags are affected.

Example : A value between 0 and 3 is in the Accumulator. The following instructions will translate the value in the Accumulator to one of four values defined by the DB (define byte) directive.

```
REL PC :  INC     A
          MOVC    A, @ A + PC
          RET
          DB      66H
          CB      77H
          CB      88H
          DB      99H
```

If the subroutine is called with the Accumulator equal to 01H, it will return with 77H in the Accumulator. The INC A before the MOVC instruction is needed to " get around " the RET instruction above the table. If several bytes of code separated the MOVC from the table, the corresponding number would be added to the Accumulator instead.

MOVC A, @ A + DPTR

Bytes : 1

Cycles : 2

Encoding :

1	0	0	1	0	0	1	1

Operation : MOVC
(A) ← ((A) + (DPTR))

MOVC A, @ A + PC

Bytes : 1

Cycles : 2

Encoding :

1	0	0	0	0	0	1	1

Operation : MOVC
(PC) ← (PC) + 1
(A) ← ((A) + (PC))

MOVX <dest-byte>, <src-byte>

Function : Move External

Description : The MOVX instructions transfer data between the Accumulator and a byte of external data memory, hence the "X" appended to MOV. There are two types of instructions, differing in whether they provide an eight-bit or sixteen-bit indirect address to the external data RAM.
In the first type, the contents of R0 or R1 in the current register bank provide an eight-bit address multiplexed with data on P0. Eight bits are sufficient for external I/O expansion decoding or for a relatively small RAM array. For somewhat larger arrays, any output port pins can be used to output higher-order address bits. These pins would be controlled by an output instruction preceding the MOVX.
In the second type of MOVX instruction, the Data Pointer generates a sixteen-bit address. P2 outputs the high-order eight address bits (the contents of DPH) while P0 multiplexes the low-order eight bits (DPL) with data. The P2 Special Function Register retains its previous contents while the P2 output buffers are emitting the contents of DPH. This form is faster and more efficient when accessing very large data arrays (up to 64K bytes), since no additional instructions are needed to set up the output ports.
It is possible in some situation to mix the two MOVX types. A large RAM array with its high-order address lines driven by P2 can be addressed via the Data Pointer, or with code to output high-order address bits to P2 followed by a MOVX instruction using R0 or R1.

Example : An external 256 byte RAM using multiplexed address/data lines is connected to the 80C51 Port 0. Port 3 provides control lines for the external RAM. Ports 0 and 2 are used for normal I/O. Registers 0 and 1 contain 12H and 34H. Location 34H of the external RAM holds the value 56H. The instruction sequence

```
MOVX    A, @ R1
MOVX    @ R0, A
```

copies the value 56H into both the Accumulator and external RAM location 12H.

MOVX A, @ Ri

Bytes : 1
Cycles : 2

Encoding :

1	1	1	0	0	0	1	i

Operation :
MOVX
(A) ← ((Ri))

MOVX @ Ri, A

Bytes : 1
Cycles : 2

Encoding :

1	1	1	1	0	0	1	i

Operation :
MOVX
((Ri)) ← (A)

MOVX A, @ DPTR

Bytes : 1
Cycles : 2

Encoding :

1	1	1	0	0	0	0	0

Operation :
MOVX
(A) ← ((DPTR))

MOVX @ DPTR, A

Bytes : 1
Cycles : 2

Encoding :

1	1	1	1	0	0	0	0

Operation :
MOVX
(DPTR) ← (A)

MUL AB

Function : Multiply

Description : MUL AB multiplies the unsigned eight-bit integers in the Accumulator and register B. The low-order byte of the sixteen-bit product is left in the Accumulator, and the high-order byte in B. If the product is greater than 255 (OFFH) the overflow flag is set ; otherwise it is cleared. The carry flag is always cleared.

Example : Originally the Accumulator holds the value 80 (50H). Register B holds the value 160 (OAOH). The instruction,

MUL AB

will give the product 12,800 (3200H), so B is changed to 32H (00110010B) and the Accumulator is cleared. The overflow flag is set, carry is cleared.

Bytes : 1

Cycles : 4

Encoding :

1	0	1	0	0	1	0	0

Operation : MUL

$(A)_{7-0} \leftarrow (A) \times (B)$

$(B)_{15-8}$

NOP

Function : No Operation

Description : Execution continue at the following instruction. Other than the PC, no registers or flags are effected.

Example : It is desired to produce a low-going output pulse on bit 7 of Port 2 lasting exactly 5 cycles. A simple SETB/CLR sequence would generate a one-cycle pulse, so four additional cycles must be inserted. This may be done (assuming no interrupts are enable) with the instruction sequence.

```
CLR     P2.7
NOP
NOP
NOP
NOP
SETP    P2.7
```

Bytes : 1

Cycles : 1

Encoding :

0	0	0	0	0	0	0	0

Operation : NOP

$(PC) \leftarrow (PC) + 1$

ORL <dest-byte> <src-byte>

Function : Logical-OR for byte variables

Description : ORL performs the bitwise logical-OR operation between the indicated variables, storing the results in the destination byte, No flags are affected. The two operands allow six addressing mode combinaisons. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing ; when the destination is a direct address, the source can be the Accumulator or immediate data. *Note :* When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, not the input pins.

Example : If the Accumulator holds 0C3H (11000011B) and R0 holds 55H (01010101B) then the instruction,
ORL A, R0
will leave the Accumulator holding the value 0D7H (11010111B).
When the destination is a directly addressed byte, the instruction can set combinations of bits in any RAM location or hardware register. The pattern of bits to be set is determined by a mask byte, which may be either a constant data value in the instruction or a variable computed in the Accumulator at run-time. The instruction.,
ORL P1, # 00110010b
will set bits 5, 4, and 1 of output Port 1.

ORL A, Rn

Bytes : 1
Cycles : 1

Encoding :

0	1	0	0	1	r	r	r

Operation ORL
(A) ← (A) V (Rn)

ORL A, direct

Bytes : 2
Cycles : 1

Encoding :

0	1	0	0	0	1	0	1	direct address

Operation : ORL
(A) ← (A) V (direct)

ORL A, @ Ri

Bytes : 1
Cycles : 1

Encoding :

0	1	0	0	0	1	1	i

Operation : ORL
(A) ← (A) V ((Ri))

ORL A, # data

Bytes : 2
Cycles : 1

Encoding :

0	1	0	0	0	1	0	0	immediate data

Operation : ORL
(A) ← (A) V # data

ORL direct, A

Bytes : 2
Cycles : 1

Encoding :

0	1	0	0	0	0	1	0	direct address

Operation : ORL
(direct) ← (direct) V (A)

ORL direct, # data

Bytes : 3

Cycles : 2

Encoding :

0	1	0	0	0	0	1	1	direct address	immediate data

Operation : ORL
(direct) ← (direct) V # data

ORL C, <src-bit>

Function : Logical-OR for bit variable

Description : Set the carry flag if the Boolean value is a logical 1 ; leave the carry in its current state otherwise. A slash (" / ") preceding the operand in the assembly language indicates that the logical complement of the addressed bit is used as the source value, but the source bit it self is not affected. No other flags are affected.

Example : Set the carry flag if and only if P1.0 = 1, ACC. 7 = 1, or OV = 0 :

```
MOV     C, P1.0       ; LOAD CARRY WITH INPUT PIN P10
ORL     C, ACC.7      ; OR CARRY WITH THE ACC. BIT7
ORL     C,/OV         ; OR CARRY WITH THE INVERSE OF OV
```

ORL C, bit

Bytes : 2

Cycles : 2

Encoding :

0	1	1	1	0	0	1	0	bit address

Operation : ORL
(C) ← (C) V (bit)

ORL C, /bit

Bytes : 2

Cycles : 2

Encoding :

1	0	1	0	0	0	0	0	bit address

Operation : ORL
(C) ← (C) V $\overline{(bit)}$

POP direct

Function : Pop from stack.

Description : The contents of internal RAM location addressed by the Stack Pointer is read, and the Stack Pointer is decremented by one. The value read is then transferred to the directly addressed byte indicated. No flags are affected.

Example : The Stack Pointer originally contains the value 32H, and internal RAM locations 30H through 32H contain the values 20H, 23H, and 01H, respectively. The instruction sequence,

```
POP DPH
POP DPL
```

will leave the Stack Pointer equal to the value 30H and the Data Pointer set to 0123H. At this point the instruction, POP SP
will leave the Stack Pointer set to 20H. Note that in this special case the Stack Pointer was decremented to 2FH before being loaded with the value popped (20H)

Bytes : 2

Cycles : 2

Encoding :

1	1	0	1	0	0	0	0	direct address

Operation : POP
(direct) ← ((SP))
(SP) ← (SP) – 1

PUSH direct

Function : push onto stack.

Description : The Stack Pointer is incremented by one. The contents fo the indicated variable is then copied into the internal RAM location addressed by the Stack Pointer. Otherwise no flags are affected.

Example : On entering interrupt routine the Stack Pointer contains 09H. The Data Pointer holds the value 0123H. The instruction sequence,

PUSH DPL
PUSH DPH

will leave the Stack Pointer set to 0BH and store 23H and 01H in internal RAM location 0AH and 0BH, respectively.

Bytes : 2

Cycles : 2

Encoding :

1	1	0	0	0	0	0	0	direct address

Operation :
PUSH
(SP) ← (SP) + 1
((SP)) ← (direct)

RET

Function : Return from subroutine

Description : RET pops the high-and low-order bytes of the PC successively from the stack, decrementing the Stack Pointer by two. Program execution continues at the resulting address, generally the instruction immediately following en ACALL or LCALL. No flags are affected.

Example : The Stack Pointer originally contains the value 0BH. Internal RAM locations 0AH and 0BH contain the values 23H, and 01H, respectively. The instruction,
RET
will leave the Stack Pointer equal to the value 09H. Program execution will continue at location 0123H.

Bytes : 1

Cycles : 2

Encoding :

0	0	1	0	0	0	1	0

Operation :
RET
(PC_{15-8}) ← ((SP))
(SP) ← (SP) – 1
(PC7-0) ← ((SP))
(SP) ← (SP) – 1

RETI

Function : Return from interrupt

Description : RETI pops the high-and low-order bytes of the PC successively from the stack, and restores the interrupt logic to accept additional interrupts at the same priority level as the one just processed. The Stack Pointer is left decremented by two. No other registers are affected ;the PSW is *not* automatically restored to its pre-interrupt status. Program execution continues at the resulting address, which is generally the instruction immediately after the point at which the interrupt request was detected. If a lower-or-same-level interrupt had been pending when the RETI instruction is executed, that one instruction will be executed before the pending interrupt is processed.

Example : The Stack Pointer originally contains the value 0BH. An interrupt was detected during the instruction ending at location 0122H. Internal RAM locations 0AH and 0BH contain the values 23H and 01H, respectively. The instruction,
RETI
will leave the Stack Pointer equal to 09H and return program execution to location 0123H.

Bytes : 1
Cycles : 2

Encoding :

0	0	1	1	0	0	1	0

Operation : RETI
$(PC_{15-8}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$
$(PC_{7-0}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$

RL A

Function : Rotate Accumulator Left

Description : The eight bits in the Accumulator are rotated one bit to the left. Bit 7 rotated into the bit 0 position. No flags are affected.

Example : The Accumulator holds the value 0C5H (11000101B). The instruction,
RL A
leaves the Accumulator holding the value 8BH (100001011B) with the carry unaffected.

Bytes : 1
Cycles : 1

Encoding :

0	0	1	0	0	0	1	1

Operation : RL
$(An + 1) \leftarrow (An)$ n = 0 – 6
$(A0) \leftarrow (A7)$

RLC A

Function : Rotate Accumulator Left through the Carry flag

Description : The eight bits in the Accumulator and the carry flag are together rotated one bit to the left. Bit 7 moves into the carry flag ; the original state of the carry flag moves into the bit 0 position. No other flags are affected.

Example : The Accumulator holds the value 0C5H (11000101B), and the carry is zero. The instruction,
RCL A
leaves the Accumulator holding the value 8BH (10001010B) with the carry set.

Bytes : 1
Cycles : 1

Encoding :

0	0	1	1	0	0	1	1

Operation : RLC
$(An + 1) \leftarrow (An)$ n = 0 – 6
$(A0) \leftarrow (C)$
$(C) \leftarrow (A7)$

RR A

Function : Rotate Accumulator Right

Description : The eight bits in the Accumulator are rotated one bit to the right. Bit 0 is rotated into the bit 7 position. No flags are affected.

Example : The Accumulator holds the value 0C5H (11000101B). The instruction,

RR A

leaves the Accumulator holding the value 0E2H (11100010B) with the carry unaffected.

Bytes : 1

Cycles : 1

Encoding :

0	0	0	0	0	0	1	1

Operation :

RR
(An) ← (An + 1) n = 0 - 6
(A7) ← (A0)

RRC A

Function : Rotate Accumulator Right through Carry flag

Description : The eight bits in the Accumulator and the carry flag are together rotated one bit to the right. Bit 0 moves into the carry flag ; the original value of the carry flag moves into the bit 7 position. No other flags are affected.

Example : The Accumulator holds the value 0C5H (11000101B), and the carry is zero. The instruction,

RRC A

leaves the Accumulator holding the value 62 (01100010B) with the carry set.

Bytes : 1

Cycles : 1

Encoding :

0	0	0	1	0	0	1	1

Operation :

RRC
(An) ← (A_n + 1)n = 0 - 6
(A7) ← (C)
(C) ← (A0)

SETB <bit>

Function : Set bit

Description : SETB sets the indicated bit to one. SETB can operate on the carry flag or any direct addressable bit. No other flags are affected.

Example : The carry flag is cleared. Output Port 1 has been written with the value 34H (00110100B). The instructions,

```
SETB   C
SETB   P1.0
```

will leave the carry flag set to 1 and change the data output on Port 1 to 35H (00110101B).

SETB C

Bytes : 1

Cycles : 1

Encoding :

1	1	0	1	0	0	1	1

Operation :
SETB
(C) ← 1

SETB bit

Bytes : 2

Cycles : 1

Encoding :

1	1	0	1	0	0	1	0	bit address

Operation :
SETB
(bit) ← 1

SJMP rel

Function : Short Jump

Description : Program control branches unconditionally to the address indicated. The branch destination is computed by adding the signed displacement in the second instruction byte to the PC, after incrementing the PC twice. Therefore, the range of destinations allowed is from 128 bytes preceding this instruction to 127 bytes following it.

Example : The label "RELADR" is assigned to an instruction at program memory location 0123H. The instruction,

```
SJMP RELADR
```

will assemble into location 0100H. After the instruction is executed, the PC will contain the value 0123H.

(*Note* : Under the above conditions the instruction following SJMP will be at 102H. therefore, the displacement byte of the instruction will be the relative offset (0123H - 0102H) = 21H. Put another way, an SJMP with a displacement of 0FEH would be an one-instruction infinite loop).

Bytes : 2

Cycles : 2

Encoding :

1	0	0	0	0	0	0	0	rel. address

Operation :
SJMP
(PC) ← (PC) + 2
(PC) ← (PC) + rel

SETB <bit>

Function : Subtract with borrow

Description : SUBB subtracts the indicated variable and the carry flag together from the Accumulator, leaving the result in the Accumulator. SUBB sets the carry (borrow) flag if a borrow is needed for bit 7, and clears C otherwise. (If C was set before executing a SUBB instruction, this indicates that a borrow was needed for the previous step in a multiple precision substraction so the carry is subtracted from the Accumulator along with the source operand). AC is set if a borrow is needed for bit 3, and cleared otherwise. OV is set if a borrow is needed into bit 6, but not into bit 7, or into bit 7, but not bit 6. When subtracting signed integers OV indicates a negative number produced when a negative value is subtracted from a positive value, or a positive result when a positive number is subtracted from a negative number. The source operand allows four addressing modes : register, direct, register-indirect, or immediate.

Example : The Accumulator holds 0C9H (11001001B), register 2 holds 54H (01010100B), and the carry flag is set. the instruction,

SUBB A, R2

will leave the value 74H (01110100B) in the accumulator, with the carry flag and AC cleared but OV set.

Notice that 0C9H minus 54H is 75H. The difference between this and the above result is due to the carry (borrow) flag being set before the operation. If the state of the carry is not known before starting a single or multiple-precision substraction, it should not be explicity cleared by a CLRC instruction.

SUBB A, Rn

Bytes : 1

Cycles : 1

Encoding :

1	0	0	1	1	r	r	r

Operation : SUBB
(A) ← (A) – (C) – (Rn)

SUBB A, direct

Bytes : 2

Cycles : 1

Encoding :

1	0	0	1	0	1	0	1	direct address

Operation : SUBB
(A) ← (A) – (C) – (direct)

SUBB A, @ Ri

Bytes : 1

Cycles : 1

Encoding :

1	0	0	1	0	1	1	i

Operation : SUBB
(A) ← (A) – (C) – (Ri)

SUBB A, # data

Bytes : 2

Cycles : 1

Encoding :

1	0	0	1	0	1	0	0	immediate data

Operation : SUBB
(A) ← (A) – (C) – # data

SWAP A

Function : Swap nibbles within the Accumulator

Description : SWAP A interchanges the low-and high-order nibbles (four-bit fields) of the Accumulator (bits 3 - 0 and bits 7 - 4). The operation can also be thought of a four-bit rotate instruction. No flag are affected.

Example : The Accumulator holds the value 0C5H (11000101B). The instruction,

SWAP A

leave the Accumulator holding the value 5CH (01011100B).

Bytes : 1

Cycles : 1

Encoding :

1	1	0	0	0	1	0	0

Operation : SWAP

$(A_{3-0}) \rightleftarrows (A_{7-4})$

XCH A, <byte>

Function : Exchange Accumulator with byte variable

Description : XCH loads the Accumulator with the contents of the indicated variable, at the same time writing the original Accumulator contents to the indicated variable. The source/destination operand can use register, direct, or register-indirect addressing.

Example : R0 contains the addres 20H. The Accumulator holds the value 3FH (00111111B). Internal RAM location 20H holds the value 75H (01110101B). The instruction,

XCH A, @R0

will leave RAM location 20H holding the values 3FH (00111111B) and 75H (01110101B) in the Accumulator.

XCH A, Rn

Bytes : 1

Cycles : 1

Encoding :

1	1	0	0	1	r	r	r

Operation : XCH

(A) $\rightleftarrows$ (Rn)

XCH A, direct

Bytes : 2

Cycles : 1

Encoding :

1	1	0	0	0	1	0	1	direct address

Operation : XCH

(A) $\rightleftarrows$ (direct)

XCH A, @Ri

Bytes : 1

Cycles : 1

Section II

Product Information

Product Selection

Products by Application Domain

Communication	Automotive
General Purpose C51 Microcontrollers: • TSC80C31 / TSC80C51 • TSC80CL31 / TSC80CL51 • 80C32 / 80C52 • 80C154 / 83C154 • 83C154D Extended 8–bit TSC80251 Microcontrollers: • TSC80251G1 • TSC80251G2 (2)	General Purpose C51 Microcontrollers: • TSC80C31 / TSC80C51 • TSC80CL31 / TSC80CL51 • 80C32 / 80C52 • 80C154 / 83C154 • 83C154D Dedicated C51 Microcontrollers: • TSC8051A11 / TSC8751A11 (1) • TSC8051A30 / TSC8751A30 (1) • TSC8051A1 / TSC8751A1 (1) • TSC8051A2 / TSC8751A2 (1) Extended 8–bit TSC80251 Microcontrollers: • TSC80251A1 • TSC80251A2 (2) • TSC80251A11 (2)
Computer	**Aerospace & Defense**
General Purpose C51 Microcontrollers: • TSC80C31 / TSC80C51 • TSC80CL31 / TSC80CL51 • 80C32 / 80C52 • 80C154 / 83C154 • 83C154D Dedicated Microcontrollers: • TSC8051C1 • TSC8051C2 (1) Extended 8–bit TSC80251 Microcontrollers: • TSC80251G1 • TSC80251G2 (2)	General Purpose C51 Microcontrollers: • TSC80C31 / TSC80C51 • TSC80CL31 / TSC80CL51 • 80C32 / 80C52 • 80C154 / 83C154 • 83C154D
Industrial	**Broadcast Media**
General Purpose C51 Microcontrollers: • TSC80C31 / TSC80C51 • TSC80CL31 / TSC80CL51 • 80C32 / 80C52 • 80C154 / 83C154 • 83C154D Dedicated C51 Microcontrollers: • TSC8051A11 / TSC8751A11 (1) • TSC8051A1 / TSC8751A1 (1) Extended 8–bit TSC80251 Microcontrollers: • TSC80251G1 • TSC80251G2 (2)	General Purpose C51Microcontrollers: • TSC80C31 / TSC80C51 • TSC80CL31 / TSC80CL51 • 80C32 / 80C52 • 80C154 / 83C154 • 83C154D

(1) Available during 1997. Please check with your TEMIC sales office.

(2) Planned.

C51 8–bit Microcontrollers Selection Table

Device	Status	ROM (byte)	RAM (byte)	Max Speed (MHz)	I/0	Serial Interfaces	16–bit Timers	WD	8–bit ADC	Other Features
General Purpose Microcontrollers – 5 Volt										
TSC80C31	now	–	128	44	32	UART	2			SR, ST
TSC80C51	now	4 K	128	44	32	UART	2			SR, ST
TSC87C51	Q3–96	4 K OTP	128	44	32	UART	2			SR, ST
80C32	now	–	256	44	32	UART	3			SR, ST
80C52	now	8 K	256	36	32	UART	3			SR, ST
87C52	Q3–96	8 K OTP	256	36	32	UART	3			SR, ST
80C154	now	–	256	36	32	UART	3	•		SR, ST
83C154	now	16 K	256	36	32	UART	3	•		SR, ST
83C154D	now	32 K	256	36	32	UART	3	•		SR, ST
General Purpose – Low Voltage: 3 Volt, up to 20 MHz !										
TSC80C31–L	now	–	128	20	32	UART	2			SR, ST
TSC80C51.–L	now	4 K	128	20	32	UART	2			SR, ST
80C32–L	now	–	256	16	32	UART	3			SR, ST
80C52...–L	now	8 K	256	16	32	UART	3			SR, ST
80C154–L	now	–	256	16	32	UART	3 (WD)	•		SR, ST
83C154...–L	now	16 K	256	16	32	UART	3 (WD)	•		SR, ST
83C154D...–L	now	32 K	256	16	32	UART	3 (WD)	•		SR, ST
General Purpose – Very Low Voltage: 1.8 Volt –NEW–										
TSC80CL31	now	–	128	4	32	UART	2			SR, ST
TSC80CL51	now	4 K	128	4	32	UART	2			SR, ST
Application Specific Microcontrollers										
TSC8051C1	now	8 K	256	16	32	UART, I^2C	2	•		12x 8–bit PWM
TSC8751C1	Q2–97	8 K OTP	256	16	32	UART, I^2C	2	•		12x 8–bit PWM
TSC8051C2	Q1–97	4 K	256	16	32	UART	2	•		12x 8–bit PWM
TSC8751C2	Q2–97	4 K OTP	256	16	32	UART	2	•		12x 8–bit PWM
TSC8051A11	98	24 K	512	20	48	UART, SPI, µWire	2+CCU	•	•	CAN 2.0B controller

Device	Status	ROM (byte)	RAM (byte)	Max Speed (MHz)	I/0	Serial Interfaces	16–bit Timers	WD	8–bit ADC	Other Features
Application Specific Microcontrollers (continued)										
TSC8751A11	Q3–97	24 K OTP	512	20	48	UART, SPI, µWire	2+CCU	•	•	CAN 2.0B controller
TSC8051A30	98	16 K	256	20	32	UART, SPI, µWire	2+CCU	•	•	VAN controller
TSC8751A30	Q4–97	16 K OTP	256	20	32	UART, SPI, µWire	2+CCU	•	•	VAN controller
TSC8051A1	98	24 K	512	20	48	UART, SPI, µWire	2+CCU	•	•	
TSC8751A1	Q3–97	24 K OTP	512	20	48	UART, SPI, µWire	2+CCU	•	•	
TSC8051A2	98	16 K	256	20	32	UART, SPI, µWire	2+CCU	•	•	
TSC8751A2	Q4–97	16 K OTP	256	20	32	UART, SPI, µWire	2+CCU	•	•	

2

Abbreviations

SPI: Serial Peripheral Interface
PWM: Pulse Width Modulation
I^2C: Inter–Integrated Circuit Communication Bus
WD: Watchdog Timer
ADC: Analog–to–Digital Converter
PMU: Pulse Measurement Unit
CCU: 8 channels input Capture, output Compare timing Unit
VAN: Vehicle Area Network
CAN: Controller Area Network

SR: Secret ROM
encrypted ROM option to secure the ROM against piracy.
ST: Secret Tag
a 64–Bit identifier can be customized in order to serialize each microcontroller with a unique number.

TSC80251 Extended 8–bit Microcontrollers Selection Table

Device	Status	ROM (byte)	RAM (byte)	Max Speed (MHz)	I/0	Serial Interfaces	16–bit Timers	WD	8–bit ADC	Other Features
TSC80251G1	now	–	1 K	16	32	UART, I^2C, SPI, µWire	3	1		EWC
TSC83251G1	now	16 K	1 K	16	32	UART, I^2C, SPI, µWire	3	1		EWC
TSC87251G1	now	16 K OTP	1 K	16	32	UART, I^2C, SPI, µWire	3	1		EWC
TSC80251G2	Planned	–	1 K	16	32	UART, I^2C, SPI, µWire	3	1		EWC
TSC83251G2	Planned	32 K	1 K	16	32	UART, I^2C, SPI, µWire	3	1		EWC
TSC87251G2	Planned	32 K OTP	1 K	16	32	UART, I^2C, SPI, µWire	3	1		EWC
TSC80251A1	now	–	1 K	16	32	UART	2	1	1	PMU, EWC
TSC83251A1	now	24 K	1 K	16	32	UART	2	1	1	PMU, EWC
TSC87251A1	now	24 K OTP	1 K	16	32	UART	2	1	1	PMU, EWC
TSC80251A2	Planned	–	1 K	16	48	UART, I^2C, SPI, µWire	2	1	1	PWM, EWC
TSC83251A2	Planned	32 K	1 K	16	48	UART, I^2C, SPI, µWire	2	1	1	PWM, EWC
TSC87251A2	Planned	32 K OTP	1 K	16	48	UART, I^2CI, SPI, µWire	2	1	1	PWM, EWC
TSC80251A11	Planned	–	4 K	16	48	UART	3+CCU	1	1	PWM, CAN 2.0B controller
TSC83251A11	Planned	64 K	4 K	16	48	UART	3+CCU	1	1	PWM, CAN 2.0B controller
TSC87251A11	Planned	64 K OTP	4 K	16	48	UART	3+CCU	1	1	PWM, CAN 2.0B controller

Abbreviations

SPI: Serial Peripheral Interface
PWM: Pulse Width Modulation
I^2C: Inter–Integrated Circuit Communication Bus
WD: Watchdog Timer
ADC: Analog–to–Digital Converter
PMU: Pulse Measurement Unit
CCU: 8 channels input Capture, output Compare timing Unit
EWC: Event and Waveform Controller
VAN: Vehicle Area Network
CAN: Car Area Network

Military and Space Products

The main characteristics of the TEMIC 8–bit microcontrollers available in military and space grades can be found on the product datasheets.

More details on military and space compliant flows are described inn the Quality Flow Section.

Standard Military Drawings (SMD)

The following products are registred by the DESC under SMD numbers.

They are manufactured by TEMIC in military temperature range according to Mil 883 compliant quality flows.

TEMIC Part–Number	SMD Number	Device	Speed	Package
MD80C31–12/883	5962–8506401MQA	80C31	12 MHz	CDIL40 (.6)
MR80C31–12/883	5962–8506401MXC	80C31	12 MHz	LCC44
MD80C51xxx–12/883	5962–8506402MQA	80C51	12 MHz	CDIL40 (.6)
MR80C51xxx–12/883	5962–8506402MXC	80C51	12 MHz	LCC44
MD80C31–16/883	5962–8506403MQA	80C31	16 MHz	CDIL40 (.6)
MD80C31–16/883	5962–8506403MXC	80C31	16 MHz	LCC44
MD80C51xxx–16/883	5962–8506404MQA	80C51	16 MHz	CDIL40 (.6)
MR80C51xxx–16/883	5962–8506404MXC	80C51	16 MHz	LCC44

Space Qualified Parts

The following product are available in space grade, processed on Radiation Tolerant technology. The SCC numbers indicates the qualification by ESA's Componants groups of the device/package.

TEMIC Part–Number	SCC Number	Device	Speed	Package
MJ–80C32E–20		80C32	20 MHz	JLCC44
MJ–80C32E–25		80C32	25 MHz	JLCC44
MJ–80C32E–30	SCC952100202	80C32	30 MHz	JLCC44
MR–80C32E–20		80C32	20 MHz	LCC44
MR–80C32E–25		80C32	25 MHz	LCC44
MR–80C32E–30	SCC952100203	80C32	30 MHz	LCC44
MC–80C32E–20		80C32	20 MHz	SB40 (.6)
MC–80C32E–25		80C32	25 MHz	SB40 (.6)
MC–80C32E–30	SCC952100201	80C32	30 MHz	SB40 (.6)

C51 General Purpose Products

CMOS 0 to 44 MHz Single-Chip 8 Bit Microcontroller

Description

The TSC80C31/80C51 is high performance SCMOS versions of the 8051 NMOS single chip 8 bit µC.

The fully static design of the TSC80C31/80C51 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The TSC80C31/80C51 retains all the features of the 8051 : 4 K bytes of ROM ; 128 bytes of RAM ; 32 I/O lines ; two 16 bit timers ; a 5-source, 2-level interrupt structure ; a full duplex serial port ; and on-chip oscillator and clock circuits.

In addition, the TSC80C31/80C51 has two software-selectable modes of reduced activity for further reduction in power consumption. In the Idle Mode the CPU is frozen while the RAM, the timers, the serial port, and the interrupt system continue to function. In the Power Down Mode the RAM is saved and all other functions are inoperative.

The TSC80C31/80C51 is manufactured using SCMOS process which allows them to run from 0 up to 44 MHz with VCC = 5 V. The TSC80C31/80C51 is also available at 20 MHz with 2.7 V < Vcc < 5.5 V.

- TSC80C31/80C51-L16 : Low power version
  Vcc : 2.7–5.5 V Freq : 0–16 MHz
- TSC80C31/80C51-L20 : Low power version
  Vcc : 2.7–5.5 V Freq : 0–20 MHz
- TSC80C31/80C51-12 : 0 to 12 MHz
- TSC80C31/80C51-20 : 0 to 20 MHz
- TSC80C31/80C51-25 : 0 to 25 MHz
- TSC80C31/80C51-30 : 0 to 30 MHz
- TSC80C31/80C51-36 : 0 to 36 MHz
- TSC80C31/80C51-40 : 0 to 40 MHz
- TSC80C31/80C51-44 : 0 to 44 MHz*

* Commercial and Industrial temperature range only. For other speed and range please consult your sale office.

Features

- Power control modes
- 128 bytes of RAM
- 4 K bytes of ROM (TSC80C31/80C51)
- 32 programmable I/O lines
- Two 16 bit timer/counter
- 64 K program memory space
- 64 K data memory space
- Fully static design
- 0.8 µm CMOS process
- Boolean processor
- 5 interrupt sources
- Programmable serial port
- Temperature range : commercial, industrial, automotive and military

Optional

- Secret ROM : Encryption
- Secret TAG : Identification number

Interface

Figure 1. Block Diagram

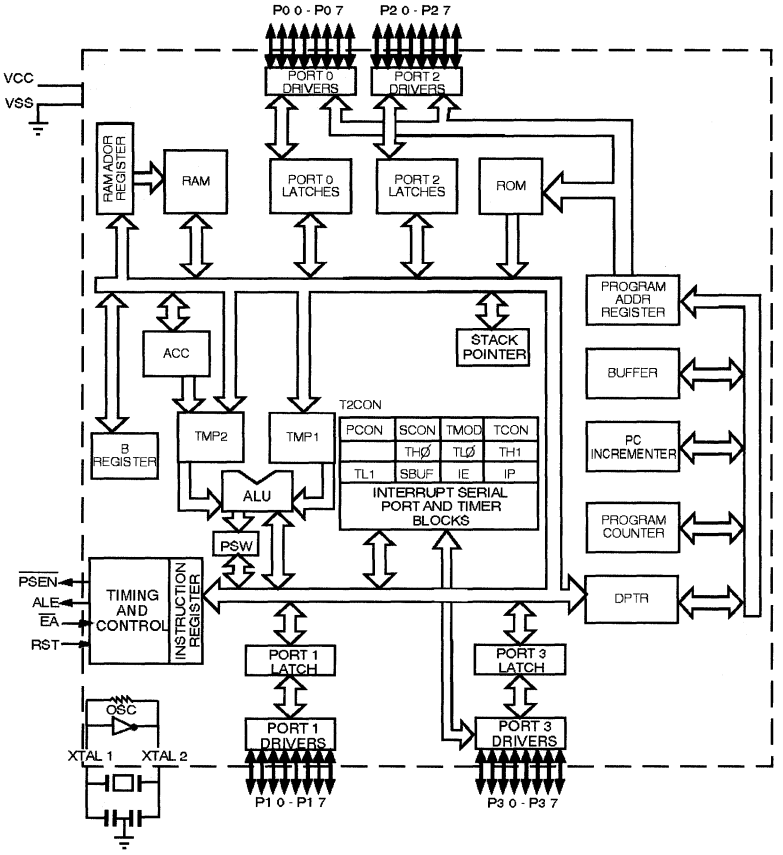
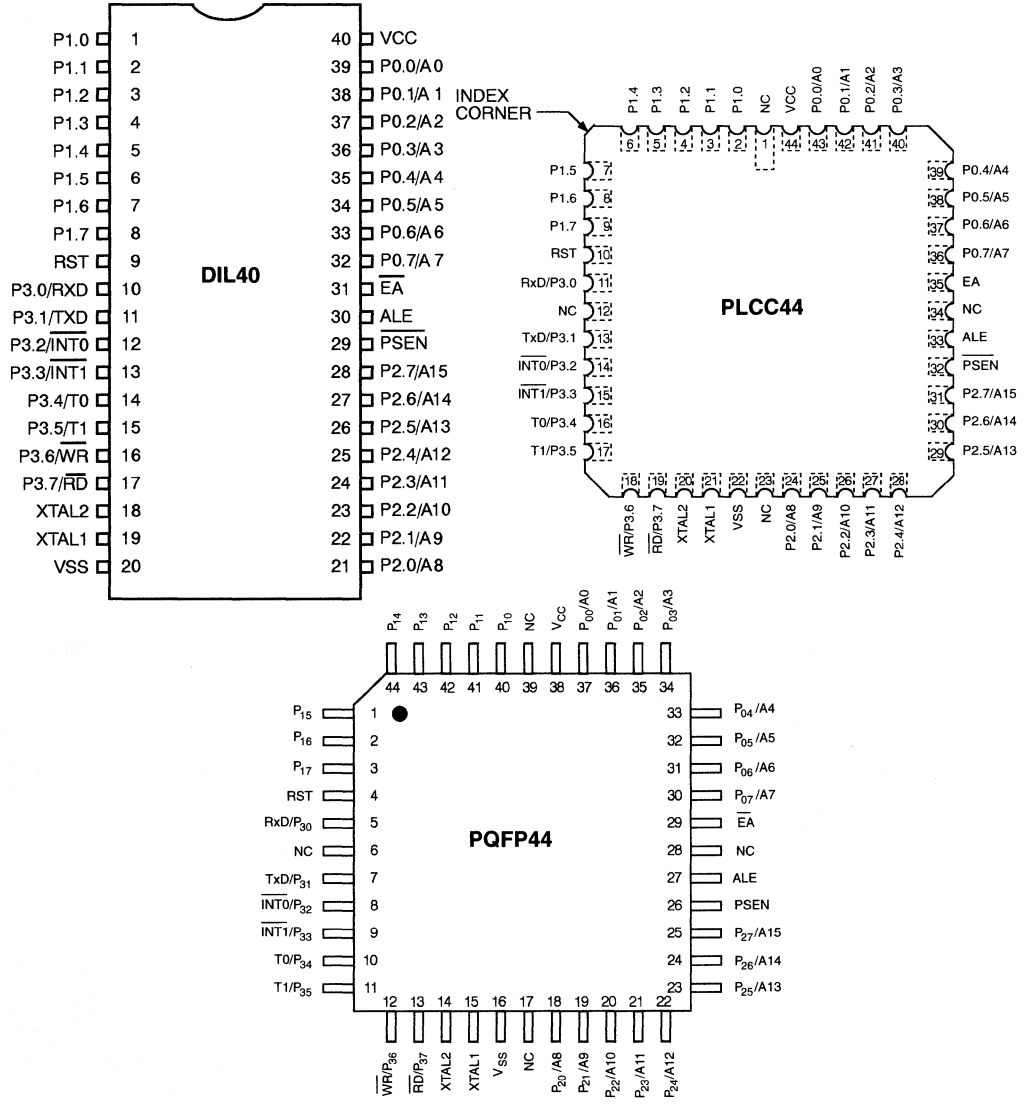


Figure 2. Pin Configuration



Diagrams are for reference only. Packages sizes are not to scale.

Pin Description

VSS

Circuit ground potential.

VCC

Supply voltage during normal, Idle, and Power Down operation.

Port 0

Port 0 is an 8 bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's. Port 0 also outputs the code bytes during program verification in the TSC80C31/80C51. External pullups are required during program verification. Port 0 can sink eight LS TTL inputs.

Port 1

Port 1 is an 8 bit bi-directional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address byte during program verification. In the TSC80C31/80C51, Port 1 can sink or source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Port 2

Port 2 is an 8 bit bi-directional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (ILL, on the data sheet) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16 bit addresses (MOVX @DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8 bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

It also receives the high-order address bits and control signals during program verification in the TSC80C31/80C51. Port 2 can sink or source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Port 3

Port 3 is an 8 bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (ILL, on the data sheet) because of the pullups. It also serves the functions of various special features of the TEMIC C51 Family, as listed below.

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	TD (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external Data Memory write strobe)
P3.7	RD (external Data Memory read strobe)

Port 3 can sink or source three LS TTL inputs. It can drive CMOS inputs without external pullups.

RST

A high level on this for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to V_{CC}. As soon as the Reset is applied (Vin), PORT 1, 2 and 3 are tied to one. This operation is achieved asynchronously even if the oscillator does not start-up.

ALE

Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.
If desired, ALE operation can be disabled by setting bit 0 of SFR location AFh (MSCON). With the bit set, ALE is active only during MOVX instruction and external fetches. Otherwise the pin is pulled low. MSCON SFR is set to XXXXXXX0 by reset.

$\overline{PSEN}$

Program Store Enable output is the read strobe to external Program Memory. PSEN is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory, two activations of PSEN are skipped during each access to external Data Memory). PSEN is not activated during fetches from internal Program Memory. PSEN can sink or source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{EA}$

When EA is held high, the CPU executes out of internal Program Memory (unless the Program Counter exceeds 3 FFFH). When EA is held low, the CPU executes only out of external Program Memory. EA must not be floated.

XTAL1

Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

XTAL2

Output of the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.

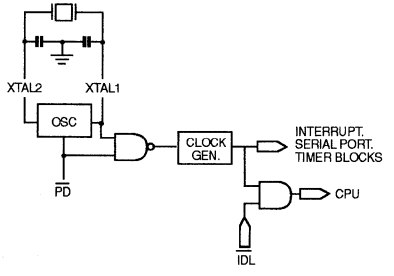
2

Idle And Power Down Operation

Figure 3. shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. Idle mode operation allows the interrupt, serial port, and timer blocks to continue to function, while the clock to the CPU is gated off.

These special modes are activated by software via the Special Function Register, PCON. Its hardware address is 87H. PCON is not bit addressable.

Figure 3. Idle and Power Down Hardware.



PCON : Power Control Register

(MSB) (LSB)

SMOD	–	–	–	GF1	GF0	PD	IDL

Symbol	Position	Name and Function
SMOD	PCON.7	Double Baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2 or 3.
–	PCON.6	(Reserved)
–	PCON.5	(Reserved)
–	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.

If 1's are written to PD and IDL at the same time. PD takes, precedence. The reset value of PCON is (000X0000).

Idle Mode

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety : the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during idle. Table 1 describes the status of the external pins during Idle mode.

There are three ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

Power Down Mode

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register is saved during power down mode. The hardware reset initiates the Special Fucntion Register. In the Power Down mode, VCC may be lowered to mi-nimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the power down mode is entered, and that the voltage is restored before the hardware reset is applied which freezes the oscillator. Reset should not be released until the oscillator has restarted and stabilized. A hardware reset is the only way of exiting the power down mode.

Table 1 describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a 1, the port pin is held high during the power down mode by the strong pullup, T1, shown in Figure 4.

Table 1. Status of the external pins during idle and power down modes.

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

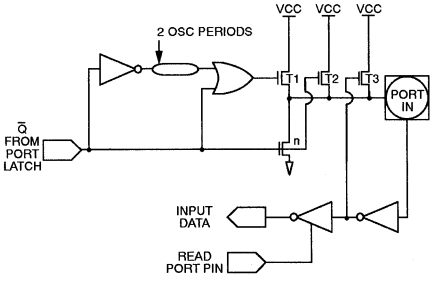
Stop Clock Mode

Due to static design, the TSC80C31/80C51 clock speed can be reduced until 0 MHz without any data loss in memory or registers. This mode allows step by step utilization, and permits to reduce system power consumption by bringing the clock frequency down to any value. At 0 MHz, the power consumption is the same as in the Power Down Mode.

I/O Ports

The I/O buffers for Ports 1, 2 and 3 are implemented as shown in Figure 4.

Figure 4. I/O Buffers in the TSC80C31/80C51 (Ports 1, 2, 3).



When the port latch contains a 0, all pFETS in Figure 4. are off while the nFET is turned on. When the port latch makes a 0-to-1 transition, the nFET turns off. The strong pFET, T1, turns on for two oscillator periods, pulling the output high very rapidly. As the output line is drawn high, pFET T3 turns on through the inverter to supply the IOH source current. This inverter and T form a latch which holds the 1 and is supported by T2.

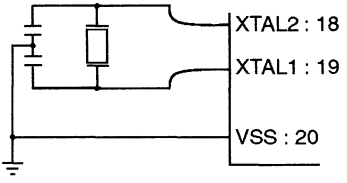
When Port 2 is used as an address port, for access to external program of data memory, any address bit that contains a 1 will have his strong pullup turned on for the entire duration of the external memory access.

When an I/O pin son Ports 1, 2, or 3 is used as an input, the user should be aware that the external circuit must sink current during the logical 1-to-0 transition. The maximum sink current is specified as ITL under the D.C. Specifications. When the input goes below approximately 2 V, T3 turns off to save ICC current. Note, when returning to a logical 1, T2 is the only internal pullup that is on. This will result in a slow rise time if the user's circuit does not force the input line high.

Oscillator Characteristics

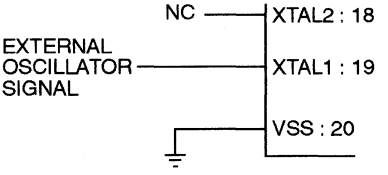
XTAL1 and XTAL2 are the input and output respectively, of an inverting amplifier which is configured for use as an on-chip oscillator, as shown in Figure 5. Either a quartz crystal or ceramic resonator may be used.

Figure 5. Crystal Oscillator.



To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in Figure 6. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

Figure 6. External Drive Configuration.



TSC80C51 with Secret ROM

TEMIC offers TSC80C31/80C51 with the encrypted secret ROM option to secure the ROM code contained in the TSC80C31/80C51 microcontrollers.

The clear reading of the program contained in the ROM is made impossible due to an encryption through several random keys implemented during the manufacturing process.

The keys used to do such encryption are selected randomwise and are definitely different from one microcontroller to another.

This encryption is activated during the following phases :

- Everytime a byte is addressed during a verify of the ROM content, a byte of the encryption array is selected.
- MOVC instructions executed from external program memory are disabled when fetching code bytes from internal memory.
- EA is sampled and latched on reset, thus all state modification are disabled.

For further information please refer to the application note (ANM053) available upon request.

TSC80C31/80C51 with Secret TAG

TEMIC offers special 64-bit identifier called "SECRET TAG" on the microcontroller chip.

The Secret Tag option is available on both ROMless and masked microcontrollers.

The Secret Tag feature allows serialization of each microcontroller for identification of a specific equipment. A unique number per device is implemented in the chip during manufacturing process. The serial number is a 64-bit binary value which is contained and addressable in the Special Function Registers (SFR) area.

This Secret Tag option can be read-out by a software routine and thus enables the user to do an individual identity check per device. This routine is implemented inside the microcontroller ROM memory in case of masked version which can be kept secret (and then the value of the Secret Tag also) by using a ROM Encryption.

For further information, please refer to the application note (ANM031) available upon request.

Electrical Characteristics

Absolute Maximum Ratings*

Ambiant Temperature Under Bias :
C = commercial ..... 0°C to 70°C
I = industrial ..... –40°C to 85°C
Storage Temperature ..... –65°C to + 150°C
Voltage on VCC to VSS ..... –0.5 V to + 7 V
Voltage on Any Pin to VSS ..... –0.5 V to V_{CC} + 0.5 V
Power Dissipation ..... 1 W**
** This value is based on the maximum allowable die temperature and the thermal resistance of the package

* Notice

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Parameters

TA = 0°C to 70°C ; VSS = 0 V ; VCC = 5 V ± 10 % ; F = 0 to 44 MHz
TA = –40°C + 85°C ; VSS = 0 V ; VCC = 5 V ± 10 % ; F = 0 to 44 MHz

Symbol	Parameter	Min	Typ (3)	Max	Unit	Test Conditions
VIL	Input Low Voltage	– 0.5		0.2 Vcc – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 0.9		Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc		Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3) (4)			0.3 0.45 1.0	V V V	IOL = 100 µA IOL = 1.6 mA (2) IOL = 3.5 mA
VOL1	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$) (4)			0.3 0.45 1.0	V V V	IOL = 200 µA IOL = 3.2 mA (2) IOL = 7.0 mA
VOH	Output High Voltage Port 1, 2, 3	Vcc – 0.3			V	IOH = – 10 µA
		Vcc – 0.7			V	IOH = – 30 µA
		Vcc – 1.5			V	IOH = – 60 µA VCC = 5 V ± 10 %
VOH1	Output High Voltage (Port 0, ALE, $\overline{PSEN}$)	Vcc – 0.3			V	IOH = – 200 µA
		Vcc – 0.7			V	IOH = – 3.2 mA
		Vcc – 1.5			V	IOH = – 7.0 mA VCC = 5 V ± 10 %
IIL	Logical 0 Input Current (Ports 1, 2 and 3)			– 50	µA	Vin = 0.45 V
ILI	Input leakage Current			± 10	µA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)			– 650	µA	Vin = 2.0 V
IPD	Power Down Current		5	30	µA	Vcc = 2.0 V to 5.5 V (1)
RRST	RST Pulldown Resistor	50	90	200	KΩ	
CIO	Capacitance of I/O Buffer			10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current Freq = 1 MHz Icc op Icc idle Freq = 6 MHz Icc op Icc idle Freq ≥ 12 MHz Icc op max = 0.9 Freq (MHz) + 5 Icc idle max = 0.3 Freq (MHz) + 1.7 Freq ≤ 20 MHz Icc op typ = 0.7 Freq (MHz) Freq ≥ 20 MHz Icc op typ = 0.5 Freq (MHz) + 4 Freq ≤ 20 MHz Icc idle typ = 0.16 Freq (MHz) + 0.4 Freq ≥ 20 MHz Icc idle typ = 0.12 Freq (MHz) + 1.2		 0.7 0.5 4.2 1.4	 1.8 1 9 3.5	 mA mA mA mA mA mA mA mA mA mA	Vcc = 5.5 V

Absolute Maximum Ratings*

Ambient Temperature Under Bias :
A = Automotive ..... –40°C to +125°C
Storage Temperature ..... –65°C to + 150°C
Voltage on VCC to VSS ..... –0.5 V to + 7 V
Voltage on Any Pin to VSS ..... –0.5 V to VCC + 0.5 V
Power Dissipation ..... 1 W**

** This value is based on the maximum allowable die temperature and the thermal resistance of the package

* Notice

Stresses above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Parameters

TA = –40°C + 125°C ; VSS = 0 V ; VCC = 5 V ± 10 % ; F = 0 to 40 MHz

Symbol	Parameter	Min	Typ (3)	Max	Unit	Test Conditions
VIL	Input Low Voltage	– 0.5		0.2 Vcc – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 0.9		Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc		Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3) (4)			0.3 0.45 1.0	V V V	IOL = 100 µA IOL = 1.6 mA (2) IOL = 3.5 mA
VOL1	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$) (4)			0.3 0.45 1.0	V V V	IOL = 200 µA IOL = 3.2 mA (2) IOL = 7.0 mA
VOH	Output High Voltage Port 1, 2 and 3	Vcc – 0.3			V	IOH = – 10 µA
		Vcc – 0.7			V	IOH = – 30 µA
		Vcc – 1.5			V	IOH = – 60 µA VCC = 5 V ± 10 %
VOH1	Output High Voltage (Port 0, ALE, $\overline{PSEN}$)	Vcc – 0.3			V	IOH = – 200 µA
		Vcc – 0.7			V	IOH = – 3.2 mA
		Vcc – 1.5			V	IOH = – 7.0 mA VCC = 5 V ± 10 %
IIL	Logical 0 Input Current (Ports 1, 2 and 3)			– 75	µA	Vin = 0.45 V
ILI	Input leakage Current			±10	µA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)			– 750	µA	Vin = 2.0 V
IPD	Power Down Current		5	75	µA	Vcc = 2.0 V to 5.5 V (1)
RRST	RST Pulldown Resistor	50	90	200	KΩ	
CIO	Capacitance of I/O Buffer			10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current Freq = 1 MHz Icc op Icc idle Freq = 6 MHz Icc op Icc idle Freq ≥ 12 MHz Icc op max = 0.9 Freq (MHz) + 5 Icc idle max = 0.3 Freq (MHz) + 1.7 Freq ≤ 20 MHz Icc op typ = 0.7 Freq (MHz) Freq ≥ 20 MHz Icc op typ = 0.5 Freq (MHz) + 4 Freq ≤ 20 MHz Icc idle typ = 0.16 Freq (MHz) + 0.4 Freq ≥ 20 MHz Icc idle typ = 0.12 Freq (MHz) + 1.2		 0.7 0.5 4.2 1.4	 1.8 1 9 3.5	 mA mA mA mA mA mA mA mA mA mA	Vcc = 5.5 V

Absolute Maximum Ratings*

Ambient Temperature Under Bias :
M = Military ..... –55°C to +125°C
Storage Temperature ..... –65°C to + 150°C
Voltage on VCC to VSS ..... –0.5 V to + 7 V
Voltage on Any Pin to VSS ..... –0.5 V to VCC + 0.5 V
Power Dissipation ..... 1 W**

** This value is based on the maximum allowable die temperature and the thermal resistance of the package

* Notice

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Parameters

TA = –55°C + 125°C ; Vss = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 40 MHz

Symbol	Parameter	Min	Typ (3)	Max	Unit	Test Conditions
VIL	Input Low Voltage	– 0.5		0.2 Vcc – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 0.9		Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc		Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3) (4)			0.45	V	IOL = 1.6 mA (2)
VOL1	Output Low Voltage (Port 0, ALE, PSEN) (4)			0.45	V	IOL = 3.2 mA (2)
VOH	Output High Voltage (Port 1, 2 and 3)	2.4			V	IOH = – 60 µA Vcc = 5 V ± 10 %
		0.75 Vcc			V	IOH = – 25 µA
		0.9 Vcc			V	IOH = – 10 µA
VOH1	Output High Voltage (Port 0 in External Bus Mode, ALE, PEN)	2.4			V	IOH = – 400 µA Vcc = 5 V ± 10 %
		0.75 Vcc			V	IOH = – 150 µA
		0.9 Vcc			V	IOH = – 40 µA
IIL	Logical 0 Input Current (Ports 1, 2 and 3)			– 75	µA	Vin = 0.45 V
ILI	Input leakage Current			+/– 10	µA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)			– 750	µA	Vin = 2.0 V
IPD	Power Down Current		5	75	µA	Vcc = 2.0 V to 5.5 V (1)
RRST	RST Pulldown Resistor	50	90	200	KΩ	
CIO	Capacitance of I/O Buffer			10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current					Vcc = 5.5 V
	Freq = 1 MHz Icc op		0.7	1.8	mA	
	Icc idle		0.5	1	mA	
	Freq = 6 MHz Icc op		4.2	9	mA	
	Icc idle		1.4	3.5	mA	
	Freq ≥ 12 MHz Icc op max = 0.9 Freq (MHz) + 5				mA	
	Icc idle max = 0.3 Freq (MHz) + 1.7				mA	
	Freq ≤ 20 MHz Icc op typ = 0.7 Freq (MHz)				mA	
	Freq ≥ 20 MHz Icc op typ = 0.5 Freq (MHz) + 4				mA	
	Freq ≤ 20 MHz Icc idle typ = 0.16 Freq (MHz) + 0.4				mA	
	Freq ≥ 20 MHz Icc idle typ = 0.12 Freq (MHz) + 1.2				mA	

Absolute Maximum Ratings*

Ambient Temperature Under Bias :
C = Commercial ..... 0°C to 70°C
I = Industrial ..... –40°C to 85°C
Storage Temperature ..... –65°C to + 150°C
Voltage on VCC to VSS ..... –0.5 V to + 7 V
Voltage on Any Pin to VSS ..... –0.5 V to VCC + 0.5 V
Power Dissipation ..... 1 W**
** This value is based on the maximum allowable die temperature and the thermal resistance of the package

* Notice

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Characteristics : Low Power Version

TA = 0°C to 70°C ; Vcc = 2.7 V to 5.5 V ; Vss = 0 V ; F = 0 to 20 MHz
TA = –40°C to 85°C ; Vcc = 2.7 V to 5.5 V ; F = 0 to 20 MHz

Symbol	Parameter	Min	Typ (3)	Max	Unit	Test Conditions
VIL	Input Low Voltage	– 0.5		0.2 V_{CC} – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
VIH2	Input High Voltage to RST for Reset	0.7 V_{CC}		V_{CC} + 0.5	V	
VIH1	Input High Voltage to XTAL1	0.7 V_{CC}		V_{CC} + 0.5	V	
VPD	Power Down Voltage to Vcc in PD Mode	2.0		5.5	V	
VOL	Output Low Voltage (Ports 1, 2, 3) (4)			0.45	V	IOL = 0.8 mA (2)
VOL1	Output Low Voltage Port 0, ALE, $\overline{PSEN}$ (4)			0.45	V	IOL = 1.6 mA (2)
VOH	Output High Voltage (Port 1, 2 and 3)	0.9 Vcc			V	IOH = – 10 µA
VOH1	Output High Voltage (Port 0 in External Bus Mode), ALE, $\overline{PSEN}$	0.9 Vcc			V	IOH = – 40 µA
IIL	Logical 0 Input Current Ports 1, 2, 3			– 50	µA	Vin = 0.45 V
ILI	Input Leakage Current			± 10	µA	0.45 < Vin < V_{CC}
ITL	Logical 1 to 0 Transition Current (Ports 1, 2, 3)			– 650	µA	Vin = 2.0 V
IPD	Power Down Current		5	30	µA	V_{CC} = 2.0 V to 5.5 V (1)
RRST	RST Pulldown Resistor	50	90	200	kΩ	
CIO	Capacitance of I/O Buffer			10	pF	fc = 1 MHz, T_A = 25°C

Icc (mA)

	Operating (1)						Idle (1)					
Frequency/Vcc	2.7 V		3 V		3.3 V		2.7 V		3 V		3.3 V	
	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ
1 MHz	0.8	0.37	1	0.42	1.1	0.46	0.4	0.22	0.5	0.24	0.6	0.27
6 MHz	4	2.2	5	2.5	6	2.7	1.5	1.2	1.7	1.4	2	1.6
12 MHz	8	4	10	4.7	12	5.3	2.5	1.7	3	2.2	3.5	2.6
16 MHz	10	5	12	5.8	14	6.6	3	1.9	3.8	2.5	4.5	3
Freq > 12MHz (Vcc = 5.5 V)	Icc op max (mA) = 0.9 × Freq (MHz) + 5 Icc Idle max (mA) = 0.3 × Freq (MHz) + 1.7											

Idle ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + 0.5 V, VIH = VCC – 0.5 V ; XTAL2 N.C ; Port 0 = VCC ; EA = RST = VSS.

Power Down ICC is measured with all output pins disconnected ; EA = PORT 0 = VCC ; XTAL2 N.C. ; RST = VSS.

Note 2 : Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLS of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operations. In the worst cases (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45 V with maxi VOL peak 0.6 V. A Schmitt Trigger use is not necessary.

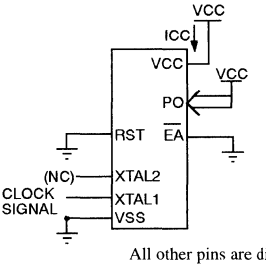
Note 3 : Typicals are based on a limited number of samples and are not guaranteed. the values listed are at room temperature and 5V.

Note 4 : Under steady state (non–transient)) conditions, IOL must be externally limited as follows :

Maximum IOL per port pin :	10 mA
Maximum IOL per 8–bit port :	
Port 0 :	26 mA
Ports 1, 2 and 3 :	15 mA
Maximum total IOL for all output pins :	71 mA

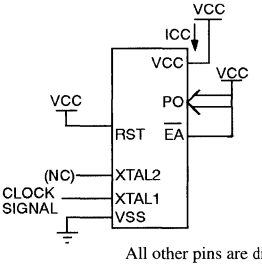
If IOL exceed the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

Figure 7. ICC Test Condition, Idle Mode.



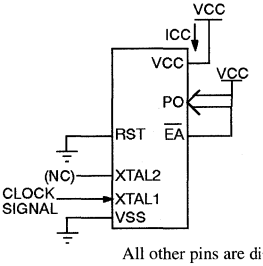
All other pins are disconnected.

Figure 8. ICC Test Condition, Active Mode.



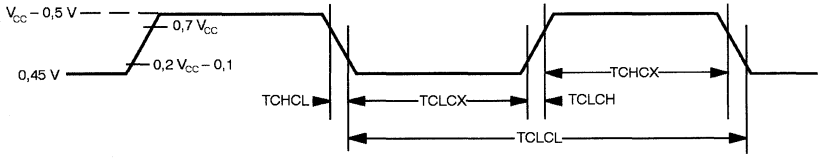
All other pins are disconnected.

Figure 9. ICC Test Condition, Power Down Mode.



All other pins are disconnected.

Figure 10. Clock Signal Waveform for ICC Tests in Active and Idle Modes.



TCLCH = TCHCL = 5 ns.

Explanation of the AC Symbol

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example :

TAVLL = Time for Address Valid to ALE low.

TLLPL = Time for ALE low to $\overline{\text{PSEN}}$ low.

A : Address.
C : Clock.
D : Input data.
H : Logic level HIGH
I : Instruction (program memory contents).
L : Logic level LOW, or ALE.
P : PSEN.
Q : Output data.
R : READ signal.
T : Time.
V : Valid.
W : WRITE signal.
X : No longer a valid logic level.
Z : Float.

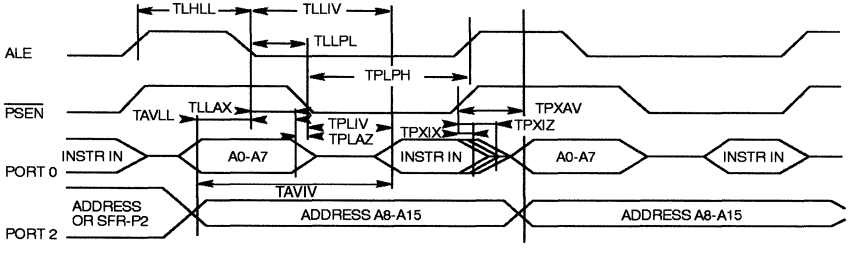
AC Parameters

TA= 0 to + 70°C ; Vss= 0 V ; Vcc= 5 V ± 10 % ; F= 0 to 44 MHz
TA= 0 to +70°C ; Vss= 0 V ; 2.7 V <Vcc < 5.5 V ; F= 0 to 16 MHz
TA=–40° to +85°C; Vss= 0 V; 2.7 V<Vcc <5.5 V ; F= 0 to 16 MHz
TA= –55° + 125°C; Vss= 0 V; Vcc= 5 V ± 10 % ; F= 0 to 40 MHz
(Load Capacitance for PORT 0, ALE and PSEN = 100 pF ; Load Capacitance for all other outputs = 80 pF)

External Program Memory Characteristics (values in ns)

		16 MHz		20 MHz		25 MHz		30 MHz		36 MHz		40 MHz		44 MHz	
SYMBOL	PARAMETER	min	max	min	max	min	max	min	max	min	max	min	max	min	max
TLHLL	ALE Pulse Width	110		90		70		60		50		40		30	
TAVLL	Address valid to ALE	40		30		20		15		10		9		7	
TLLAX	Address Hold After ALE	35		35		35		35		35		30		20	
TLLIV	ALE to valid instr in		185		170		130		100		80		70		65
TLLPL	ALE to PSEN	45		40		30		25		20		15		12	
TPLPH	PSEN pulse Width	165		130		100		80		75		65		54	
TPLIV	PSEN to valid instr in		125		110		85		65		50		45		35
TPXIX	Input instr Hold After PSEN	0		0		0		0		0		0		0	
TPXIZ	Input instr Float After PSEN		50		45		35		30		25		20		10
TPXAV	PSEN to Address Valid	55		50		40		35		30		25		15	
TAVIV	Address to Valid instr in		230		210		170		130		90		80		70
TPLAZ	PSEN low to Address Float		10		10		8		6		5		5		5

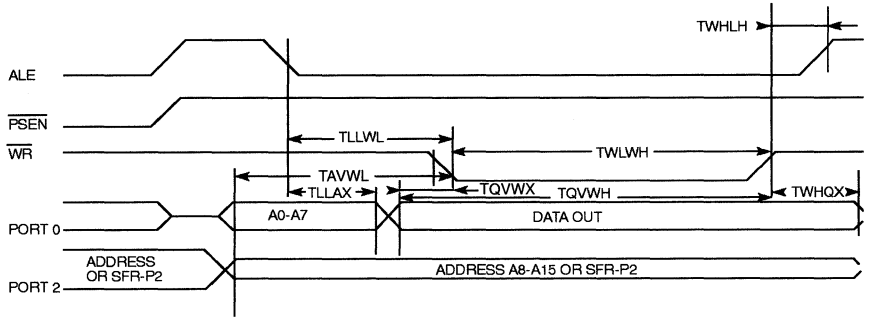
External Program Memory Read Cycle



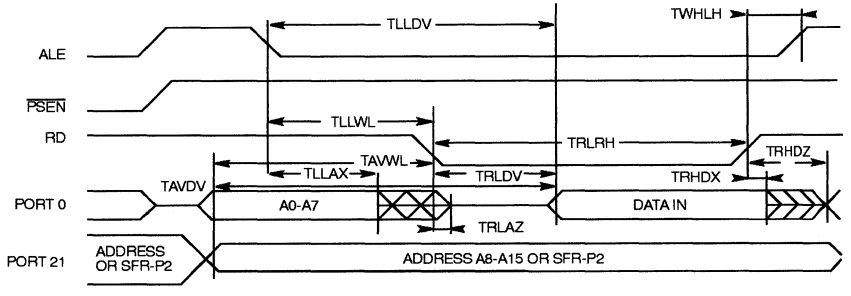
External Data Memory Characteristics (values in ns)

		16 MHz		20 MHz		25 MHz		30 MHz		36 MHz		40 MHz		44 MHz	
SYMBOL	PARAMETER	min	max	min	max	min	max	min	max	min	max	min	max	min	max
TRLRH	RD pulse Width	340		270		210		180		120		100		80	
TWLWH	WR pulse Width	340		270		210		180		120		100		80	
TLLAX	Address Hold After ALE	85		85		70		55		35		30		25	
TRLDV	RD to Valid data in		240		210		175		135		110		90		70
TRHDX	Data hold after RD	0		0		0		0		0		0		0	
TRHDZ	Data float after RD		90		90		80		70		50		45		35
TLLDV	ALE to Valid Data In		435		370		350		235		170		150		130
TAVDV	Address to Valid Data IN		480		400		300		260		190		180		170
TLLWL	ALE to WR or RD	150	250	135	170	120	130	90	115	70	100	60	95	50	85
TAVWL	Address to WR or RD	180		180		140		115		75		65		55	
TQVWX	Data valid to WR transition	35		35		30		20		15		10		6	
TQVWH	Data Setup to WR transition	380		325		250		215		170		160		140	
TWHQX	Data Hold after WR	40		35		30		20		15		10		6	
TRLAZ	RD low to Address Float		0		0		0		0		0		0		0
TWHLH	RD or WR high to ALE high	35	90	35	60	25	45	20	40	20	40	15	35	13	33

External Data Memory Write Cycle



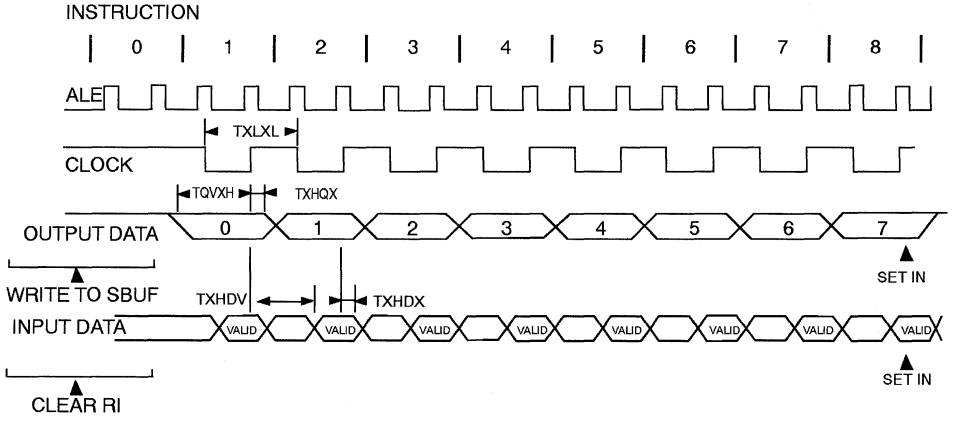
External Data Memory Read Cycle



Serial Port Timing – Shift Register Mode (values in ns)

		16 MHz		20 MHz		25 MHz		30 MHz		36 MHz		40 MHz		44 MHz	
SYMBOL	PARAMETER	min	max	min	max	min	max	min	max	min	max	min	max	min	max
TXLXL	Serial Port Clock Cycle Time	750		600		480		400		330		250		227	
TQVXH	Output Data Setup to Clock Rising Edge	563		480		380		300		220		170		140	
TXHQX	Output Data Hold after Clock Rising Edge	90		90		65		50		45		35		25	
TXHDX	Input Data Hold after Clock Rising Edge	0		0		0		0		0		0		0	
TXHDV	Clock Rising Edge to Input Data Valid		563		450		350		300		250		200		160

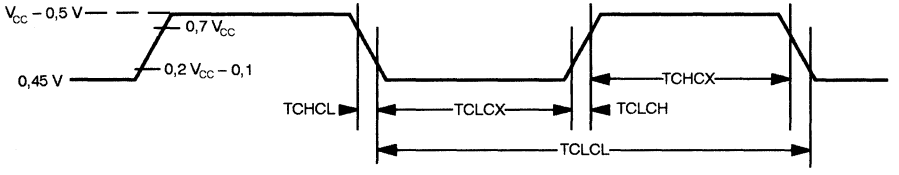
Shift Register Timing Waveforms



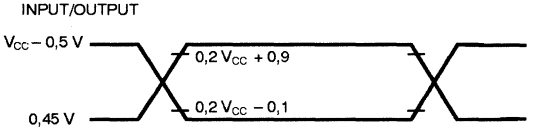
External Clock Drive Characteristics (XTAL1)

SYMBOL	PARAMETER	MIN	MAX	UNIT
FCLCL	Oscillator Frequency		44	MHz
TCLCL	Oscillator period	22.7		ns
TCHCX	High Time	5		ns
TCLCX	Low Time	5		ns
TCLCH	Rise Time		5	ns
TCHCL	Fall Time		5	ns

External Clock Drive Waveforms

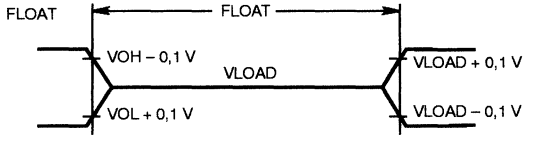


AC Testing Input/Output Waveforms



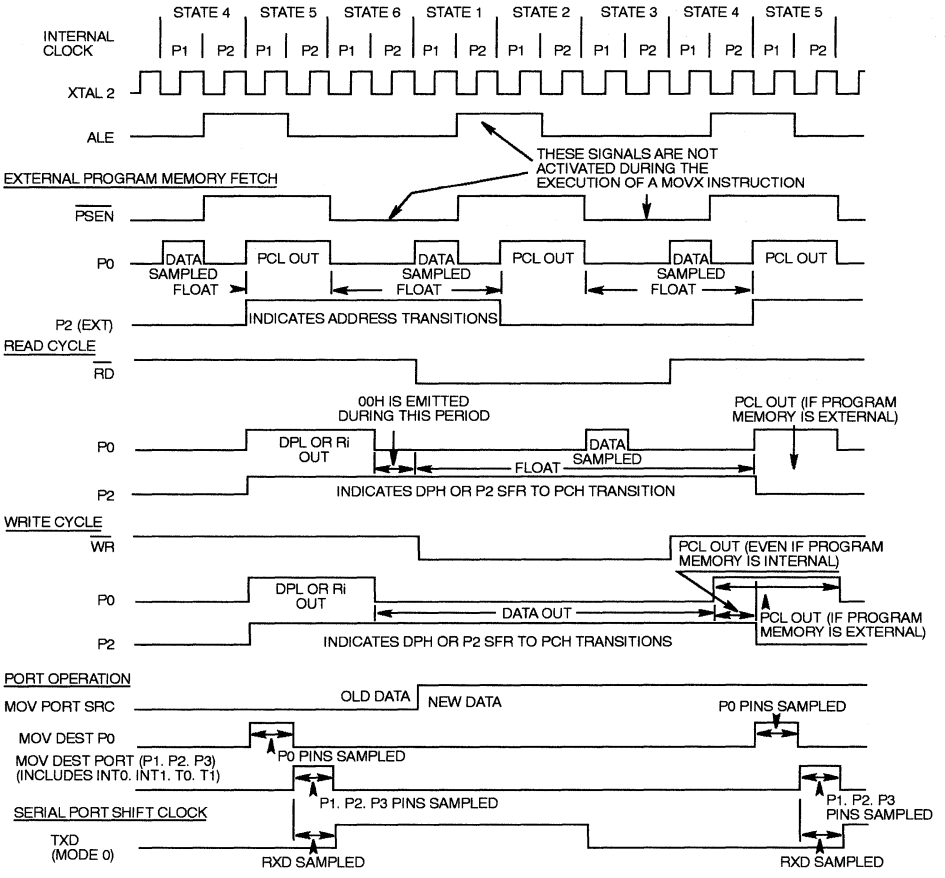
AC inputs during testing are driven at Vcc – 0.5 for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at VIH min for a logic "1" and VIL max for a logic "0".

Float Waveforms



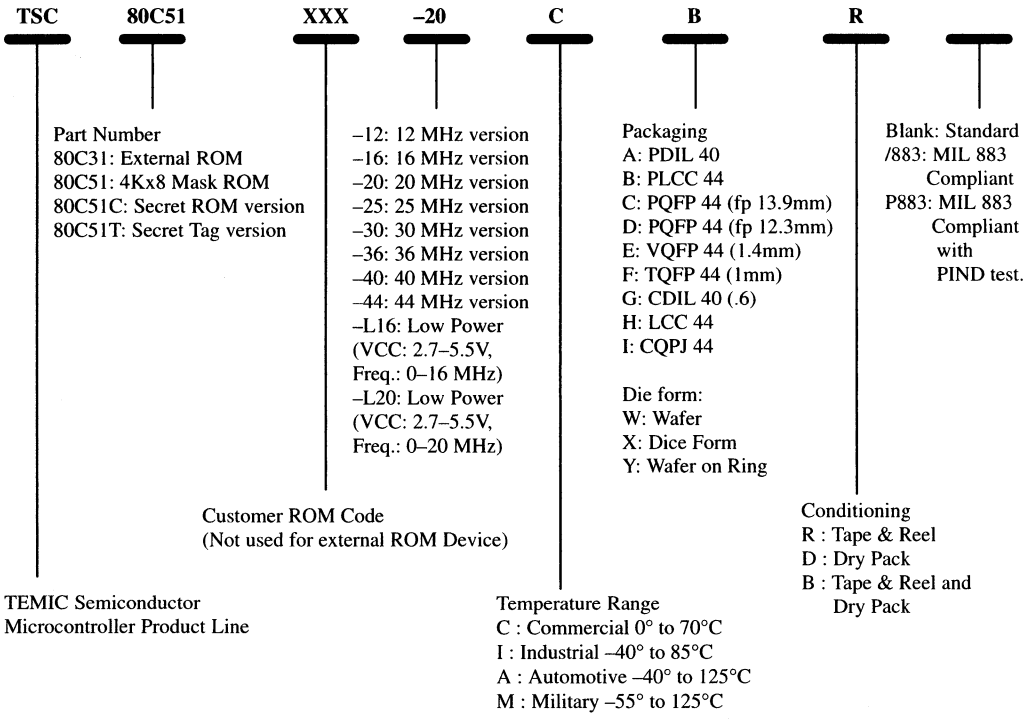
For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded VOH/VOL level occurs. Iol/IoH ≥ ± 20 mA.

Clock Waveforms



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A = 25°C fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

Ordering Information



Examples :
Mask ROM version XXX, PDIL 40, 20 MHz version, Commercial Temperature Range . TSC80C31/80C51XXX–20CA

(1) Ceramic of multi–layer packages: contact TEMIC Sales office

Product Marking :
For PDIL 40, PLCC 44 & QFP 44 Packages

TEMIC
Customer P/N
Temic P/N
© Intel 80, 82
YYWW Lot Number

TSC80CL31/TSC80CL51

CMOS 1.8 Volt Single-Chip 8 Bit Microcontroller

Description

TEMIC's 80C31 and 80C51 are high performance SCMOS versions of the 8051 NMOS single chip 8 bit µC.

The fully static design of the TEMIC TSC80CL31/TSC80CL51 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The TSC80CL51 retains all the features of the 8051 : 4 K bytes of ROM ; 128 bytes of RAM ; 32 I/O lines ; two 16 bit timers ; a 5-source, 2-level interrupt structure ; a full duplex serial port ; and on-chip oscillator and clock circuits.

The TSC80CL51 is a general purpose microcontroller especially suited for battery–powered applications. This very low voltage version fits in all applications using two battery cells.

In addition, the TSC80CL51 has two software-selectable modes of reduced activity for further reduction in power consumption. In the Idle Mode the CPU is frozen while the RAM, the timers, the serial port, and the interrupt system continue to function. In the Power Down Mode the RAM is saved and all other functions are inoperative.

The TSC80CL31 is identical to the TSC80CL51 except that it has no on–chip ROM.

TEMIC's TSC80CL31/TSC80CL51 are manufactured using SCMOS process which allows them to run from 0 up to 4 MHz with VCC = 1.8 V.

Available Products

- Very Low Voltage version
  Vcc : 1.8-5.5 V Freq : 0-4 MHz
- TSC80CL31–V4: ROMless version
- TSC80CL51–V4: 4K x 8 Mask ROM version

Features

- Power control modes
- 128 bytes of RAM
- 4 K bytes of ROM (TSC80CL51)
- 32 programmable I/O lines
- Two 16 bit timer/counter
- 64 K program memory space
- 64 K data memory space
- Fully static design
- 0.8 µm CMOS process
- Boolean processor
- 5 interrupt sources
- Programmable serial port
- Temperature range : commercial

Optional

- Secret ROM : Encryption
- Secret TAG : Identification number

Interface

Figure 1. Block Diagram

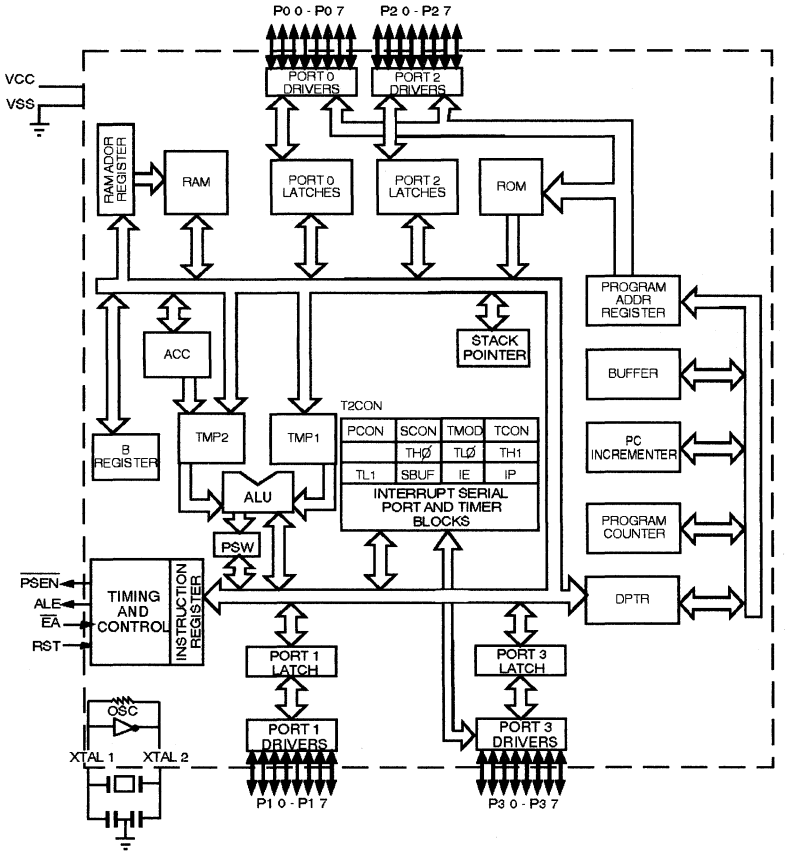
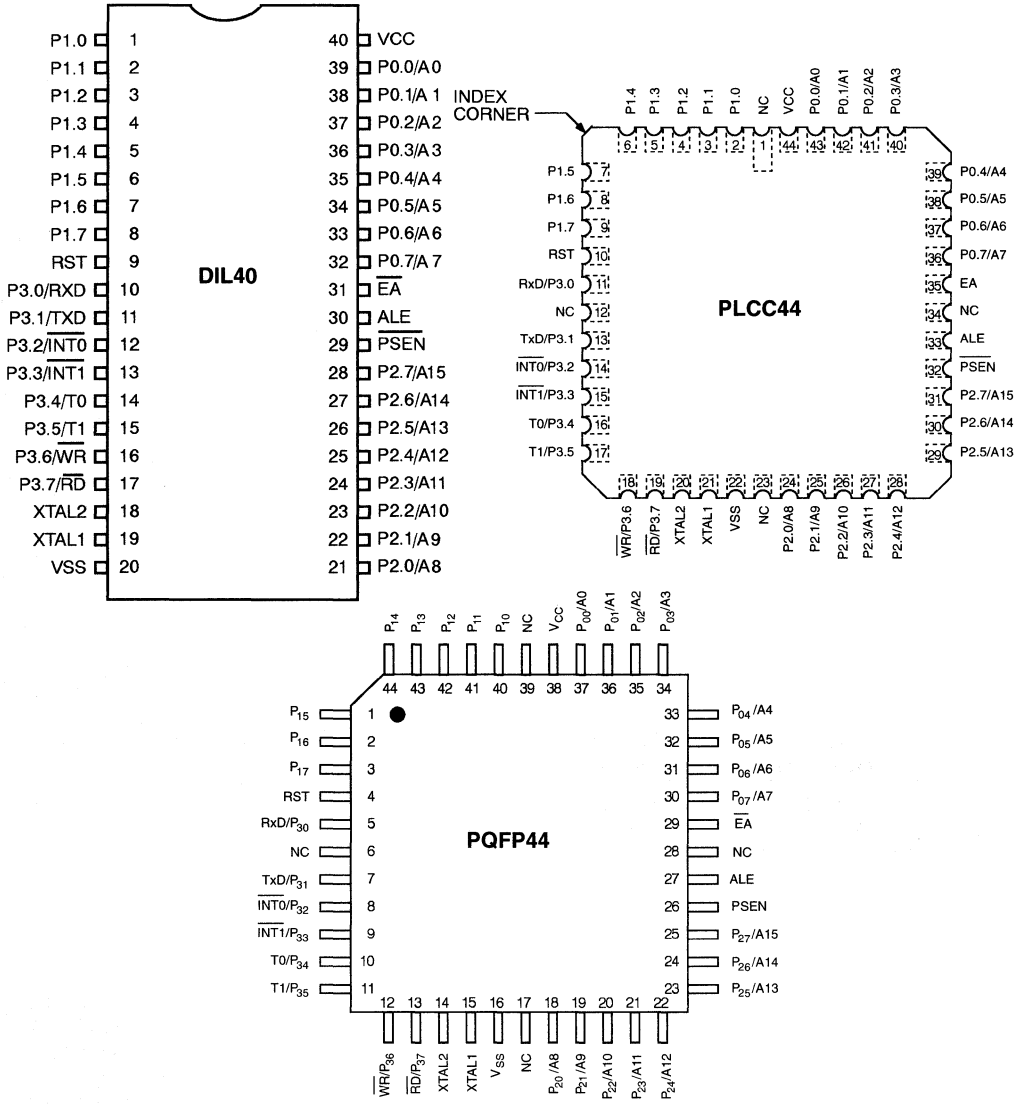


Figure 2. Pin Configuration



Diagrams are for reference only. Packages sizes are not to scale.

Pin Description

VSS

Circuit ground potential.

VCC

Supply voltage during normal, Idle, and Power Down operation.

Port 0

Port 0 is an 8 bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's. Port 0 also outputs the code bytes during program verification in the TSC80CL51. External pullups are required during program verification. Port 0 can sink eight LS TTL inputs.

Port 1

Port 1 is an 8 bit bi-directional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address byte during program verification. In the TSC80CL51, Port 1 can sink or source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Port 2

Port 2 is an 8 bit bi-directional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (ILL, on the data sheet) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16 bit addresses (MOVX @DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8 bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

It also receives the high-order address bits and control signals during program verification in the TSC80CL51. Port 2 can sink or source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Port 3

Port 3 is an 8 bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (ILL, on the data sheet) because of the pullups. It also serves the functions of various special features of the TEMIC 51 Family, as listed below.

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	TD (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external Data Memory write strobe)
P3.7	RD (external Data Memory read strobe)

Port 3 can sink or source three LS TTL inputs. It can drive CMOS inputs without external pullups.

RST

A high level on this for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to V_{CC}. As soon as the Reset is applied (Vin), PORT 1, 2 and 3 are tied to one. This operation is achieved asynchronously even if the oscillator does not start-up.

ALE

Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.
If desired, ALE operation can be disabled by setting bit 0 of SFR location AFh (MSCON). With the bit set, ALE is active only during MOVX instruction and external fetches. Otherwise the pin is pulled low. MSCON SFR is set to XXXXXXX0 by reset.

$\overline{PSEN}$

Program Store Enable output is the read strobe to external Program Memory. PSEN is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory, two activations of PSEN are skipped during each access to external Data Memory). PSEN is not activated during fetches from internal Program Memory. PSEN can sink or source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{EA}$

When EA is held high, the CPU executes out of internal Program Memory (unless the Program Counter exceeds 3 FFFH). When EA is held low, the CPU executes only out of external Program Memory. EA must not be floated.

XTAL1

Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

XTAL2

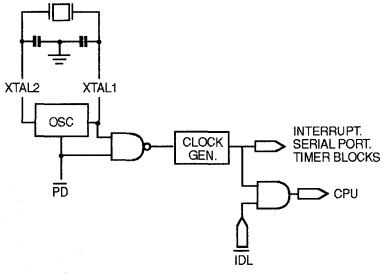
Output of the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.

Idle And Power Down Operation

Figure 3. shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. Idle mode operation allows the interrupt, serial port, and timer blocks to continue to function, while the clock to the CPU is gated off.

These special modes are activated by software via the Special Function Register, PCON. Its hardware address is 87H. PCON is not bit addressable.

Figure 3. Idle and Power Down Hardware.



PCON : Power Control Register

(MSB)							(LSB)
SMOD	–	–	–	GF1	GF0	PD	IDL

Symbol	Position	Name and Function
SMOD	PCON.7	Double Baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2 or 3.
–	PCON.6	(Reserved)
–	PCON.5	(Reserved)
–	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.

If 1's are written to PD and IDL at the same time. PD takes, precedence. The reset value of PCON is (000X0000).

Idle Mode

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety : the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during idle. Table 1 describes the status of the external pins during Idle mode.

There are three ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

Power Down Mode

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register is saved during power down mode. The hardware reset initiates the Special Fucntion Register. In the Power Down mode, VCC may be lowered to mi-nimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the power down mode is entered, and that the voltage is restored before the hardware reset is applied which freezes the oscillator. Reset should not be released until the oscillator has restarted and stabilized. A hardware reset is the only way of exiting the power down mode.

The second way of terminating the Idle mode is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

Table 1 describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a 1, the port pin is held high during the power down mode by the strong pullup, T1, shown in Figure 4.

Table 10 : Status of the external pins during idle and power down modes.

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

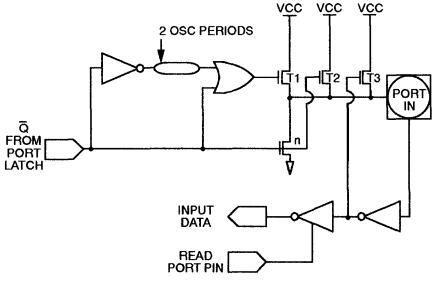
Stop Clock Mode

Due to static design, the TEMIC TSC80CL31/C51 clock speed can be reduced until 0 MHz without any data loss in memory or registers. This mode allows step by step utilization, and permits to reduce system power consumption by bringing the clock frequency down to any value. At 0 MHz, the power consumption is the same as in the Power Down Mode.

I/O Ports

The I/O buffers for Ports 1, 2 and 3 are implemented as shown in Figure 4.

Figure 4. I/O Buffers in the TSC80CL51 (Ports 1, 2, 3).



When the port latch contains a 0, all pFETS in Figure 4. are off while the nFET is turned on. When the port latch makes a 0-to-1 transition, the nFET turns off. The strong pFET, T1, turns on for two oscillator periods, pulling the output high very rapidly. As the output line is drawn high, pFET T3 turns on through the inverter to supply the IOH source current. This inverter and T form a latch which holds the 1 and is supported by T2.

When Port 2 is used as an address port, for access to external program of data memory, any address bit that contains a 1 will have his strong pullup turned on for the entire duration of the external memory access.

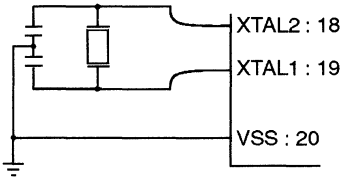
When an I/O pin son Ports 1, 2, or 3 is used as an input, the user should be aware that the external circuit must sink current during the logical 1-to-0 transition. The maximum sink current is specified as ITL under the D.C. Specifications. When the input goes below approximately 2 V, T3 turns off to save ICC current. Note, when returning to a logical 1, T2 is the only internal pullup that is on. This will result in a slow rise time if the user's circuit does not force the input line high.

2

Oscillator Characteristics

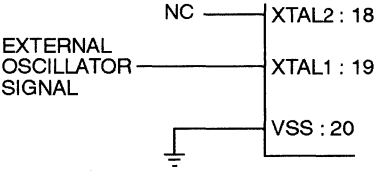
XTAL1 and XTAL2 are the input and output respectively, of an inverting amplifier which is configured for use as an on-chip oscillator, as shown in Figure 5. Either a quartz crystal or ceramic resonator may be used.

Figure 5. Crystal Oscillator.



To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in Figure 6. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

Figure 6. External Drive Configuration.



TSC80CL51 with Secret ROM

TEMIC offers TSC80CL51 with the encrypted secret ROM option to secure the ROM code contained in the TSC80CL51 microcontrollers.

The clear reading of the program contained in the ROM is made impossible due to an encryption through several random keys implemented during the manufacturing process.

The keys used to do such encryption are selected randomwise and are definitely different from one microcontroller to another.

This encryption is activated during the following phases :

- Everytime a byte is addressed during a verify of the ROM content, a byte of the encryption array is selected.
- MOVC instructions executed from external program memory are disabled when fetching code bytes from internal memory.
- EA is sampled and latched on reset, thus all state modification are disabled.

For further information please refer to the application note (ANM053) available upon request.

TSC80CL51 with Secret TAG

TEMIC offers special 64-bit identifier called "SECRET TAG" on the microcontroller chip.

The Secret Tag option is available on both ROMless and masked microcontrollers.

The Secret Tag feature allows serialization of each microcontroller for identification of a specific equipment. A unique number per device is implemented in the chip during manufacturing process. The serial number is a 64-bit binary value which is contained and addressable in the Special Function Registers (SFR) area.

This Secret Tag option can be read-out by a software routine and thus enables the user to do an individual identity check per device. This routine is implemented inside the microcontroller ROM memory in case of masked version which can be kept secret (and then the value of the Secret Tag also) by using a ROM Encryption.

For further information, please refer to the application note (ANM031) available upon request.

Electrical Characteristics

Absolute Maximum Ratings*

Ambient Temperature Under Bias :
C = Commercial ..... 0°C to 70°C
Storage Temperature ..... –65°C to + 150°C
Voltage on VCC to VSS ..... –0.5 V to + 7 V
Voltage on Any Pin to VSS ..... –0.5 V to VCC + 0.5 V
Power Dissipation ..... 1 W**
** This value is based on the maximum allowable die temperature and the thermal resistance of the package

* Notice

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2

DC Characteristics : Very Low Voltage Version

TA = 0°C to 70°C ; Vcc = 1.8 V to 5.5 V ; Vss = 0 V ; F = 0 to 4 MHz

Symbol	Parameter	Min	Max	Unit	Test Conditions
VIL	Input Low Voltage	– 0.5	0.2 V_{CC} – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 V_{CC} + 1.4	V_{CC} + 0.5	V	
VIH2	Input High Voltage to RST for Reset	0.7 V_{CC}	V_{CC} + 0.5	V	
VIH1	Input High Voltage to XTAL1	0.7 V_{CC}	V_{CC} + 0.5	V	
VPD	Power Down Voltage to Vcc in PD Mode	1.8	5.5	V	
VOL	Output Low Voltage (Ports 1, 2, 3)		0.45	V	IOL = 0.8 mA (2)
VOL1	Output Low Voltage Port 0, ALE, $\overline{PSEN}$		0.45	V	IOL = 1.6 mA (2)
VOH	Output High Voltage (Port 1, 2 and 3)	0.9 Vcc		V	IOH = – 10 µA
VOH1	Output High Voltage (Port 0 in External Bus Mode), ALE, $\overline{PSEN}$	0.9 Vcc		V	IOH = – 40 µA
IIL	Logical 0 Input Current Ports 1, 2, 3		– 50	µA	Vin = 0.45 V
ILI	Input Leakage Current		± 10	µA	0.45 < Vin < V_{CC}
ITL	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		– 650	µA	Vin = 2.0 V
IPD	Power Down Current		10 50	µA µA	V_{CC} = 1.8 V to 2.2 V (1) V_{CC} = 2.2 V to 5.5 V (1)
RRST	RST Pulldown Resistor	50	200	kΩ	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, T_A = 25°C

Maximum Icc (mA)

	Operating (1)				Idle (1)			
Frequency/Vcc	1.8 V	2.2 V	3.3 V	5.5 V	1.8 V	2.2 V	3.3 V	5.5 V
32 KHz	60 µA	80 µA	200 µA	400 µA	25 µA	30 µA		
455 KHz	200 µA	250 µA	350 µA	1 mA	50 µA	75 µA	150 µA	400 µA
3.58 MHz	1.5 mA	2 mA	3 mA	6 mA	300 µA	500 µA	1 mA	2.5 mA
4 MHz	2 mA	2.5 mA	3.5 mA	7 mA	400 µA	600 µA	1.2 mA	3 mA

Note 1 : ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + 0.5 V, VIH = VCC – 0.5 V ; XTAL2 N.C. ; EA = RST = Port 0 = VCC. ICC would be slighty higher if a crystal oscillator used.

Idle ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + 0.5 V, VIH = VCC – 0.5 V ; XTAL2 N.C ; Port 0 = VCC ; EA = RST = VSS.

Power Down ICC is measured with all output pins disconnected ; EA = PORT 0 = VCC ; XTAL2 N.C. ; RST = VSS.

Note 2 : Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLS of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operations. In the worst cases (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45 V with maxi VOL peak 0.6 V. A Schmitt Trigger use is not necessary.

Figure 7. ICC Test Condition, Idle Mode. All other pins are disconnected.

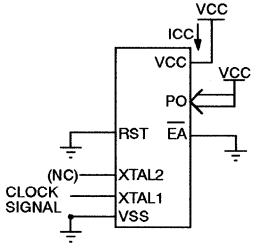


Figure 8. ICC Test Condition, Active Mode. All other pins are disconnected.

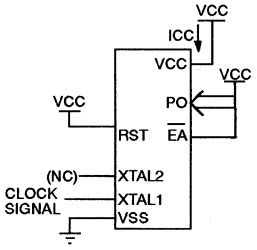


Figure 9. ICC Test Condition, Power Down Mode. All other pins are disconnected.

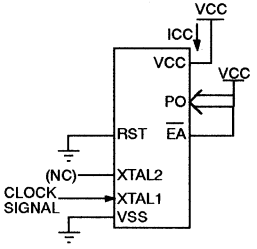
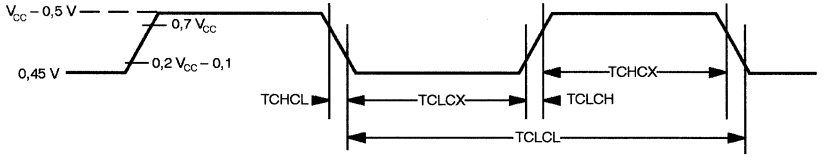


Figure 10. Clock Signal Waveform for ICC Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.



Explanation of the AC Symbol

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example :

TAVLL = Time for Address Valid to ALE low.

TLLPL = Time for ALE low to $\overline{PSEN}$ low.

A : Address.	Q : Output data.
C : Clock.	R : READ signal.
D : Input data.	T : Time.
H : Logic level HIGH	V : Valid.
I : Instruction (program memory contents).	W : WRITE signal.
L : Logic level LOW, or ALE.	X : No longer a valid logic level.
P : PSEN.	Z : Float.

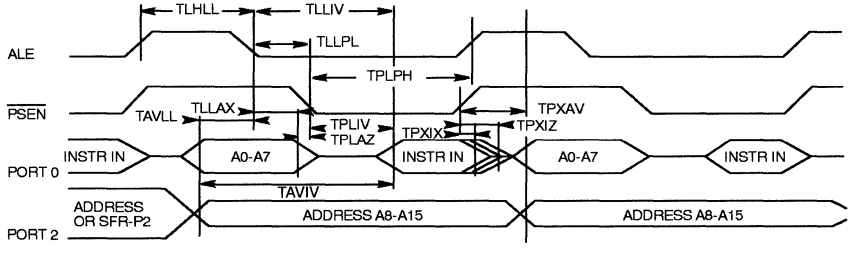
AC Parameters

TA = 0 to +70°C ; Vss = 0 V ; 1.8 V < Vcc < 5.5 V ; F = 0 to 4 MHz
(Load Capacitance for PORT 0, ALE and PSEN = 100 pF ; Load Capacitance for all other outputs = 80 pF)

External Program Memory Characteristics (values in ns)

		4 MHz	
SYMBOL	**PARAMETER**	**min**	**max**
TLHLL	ALE Pulse Width	460	
TAVLL	Address valid to ALE	210	
TLLAX	Address Hold After ALE	220	
TLLIV	ALE to valid instr in		900
TLLPL	ALE to PSEN	220	
TPLPH	PSEN pulse Width	705	
TPLIV	PSEN to valid instr in		650
TPXIX	Input instr Hold After PSEN	0	
TPXIZ	Input instr Float After PSEN		225
TPXAV	PSEN to Address Valid	250	
TAVIV	Address to Valid instr in		1100
TPLAZ	PSEN low to Address Float		10

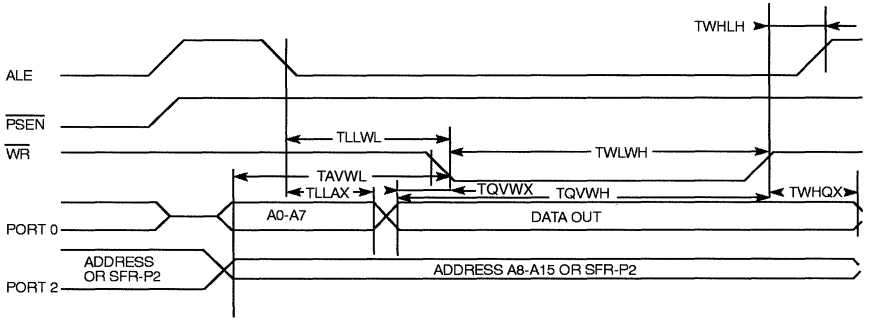
External Program Memory Read Cycle



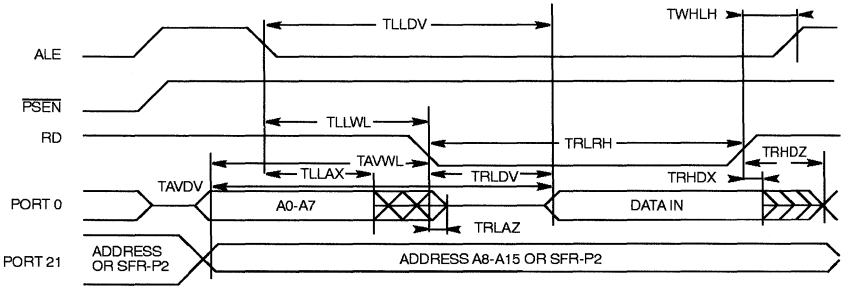
External Data Memory Characteristics (values in ns)

		4 MHz	
SYMBOL	**PARAMETER**	**min**	**max**
TRLRH	RD pulse Width	1400	
TWLWH	WR pulse Width	1400	
TLLAX	Address Hold After ALE	220	
TRLDV	RD to Valid data in		1100
TRHDX	Data hold after RD	0	
TRHDZ	Data float after RD		460
TLLDV	ALE to Valid Data In		1850
TAVDV	Address to Valid Data IN		2100
TLLWL	ALE to WR or RD	700	800
TAVWL	Address to WR or RD	870	
TQVWX	Data valid to WR transition	200	
TQVWH	Data Setup to WR transition	1600	
TWHQX	Data Hold after WR	200	
TRLAZ	RD low to Address Float		0
TWHLH	RD or WR high to ALE high	210	290

External Data Memory Write Cycle



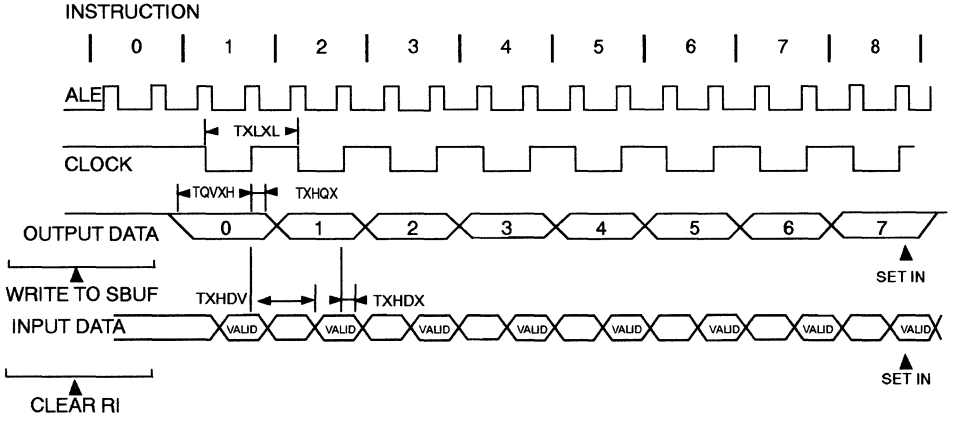
External Data Memory Read Cycle



Serial Port Timing – Shift Register Mode (values in ns)

		4 MHz	
SYMBOL	PARAMETER	min	max
TXLXL	Serial Port Clock Cycle Time	12 Clk	
TQVXH	Output Data Setup to Clock Rising Edge	2370	
TXHQX	Output Data Hold after Clock Rising Edge	390	
TXHDX	Input Data Hold after Clock Rising Edge	0	
TXHDV	Clock Rising Edge to Input Data Valid		2370

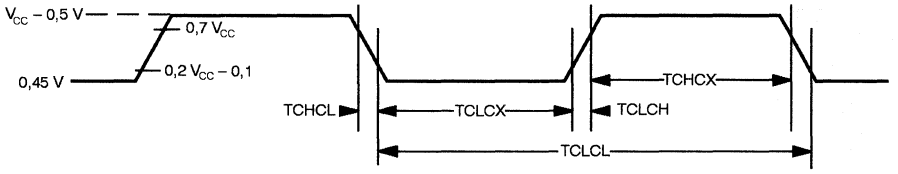
Shift Register Timing Waveforms



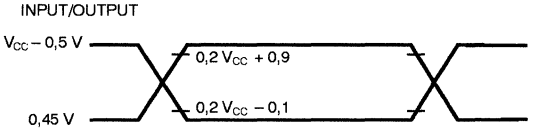
External Clock Drive Characteristics (XTAL1)

SYMBOL	PARAMETER	MIN	MAX	UNIT
FCLCL	Oscillator Frequency		42	MHz
TCLCL	Oscillator period	23.8		ns
TCHCX	High Time	5		ns
TCLCX	Low Time	5		ns
TCLCH	Rise Time		5	ns
TCHCL	Fall Time		5	ns

External Clock Drive Waveforms

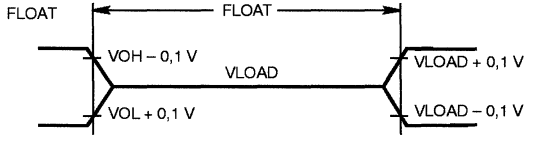


AC Testing Input/Output Waveforms



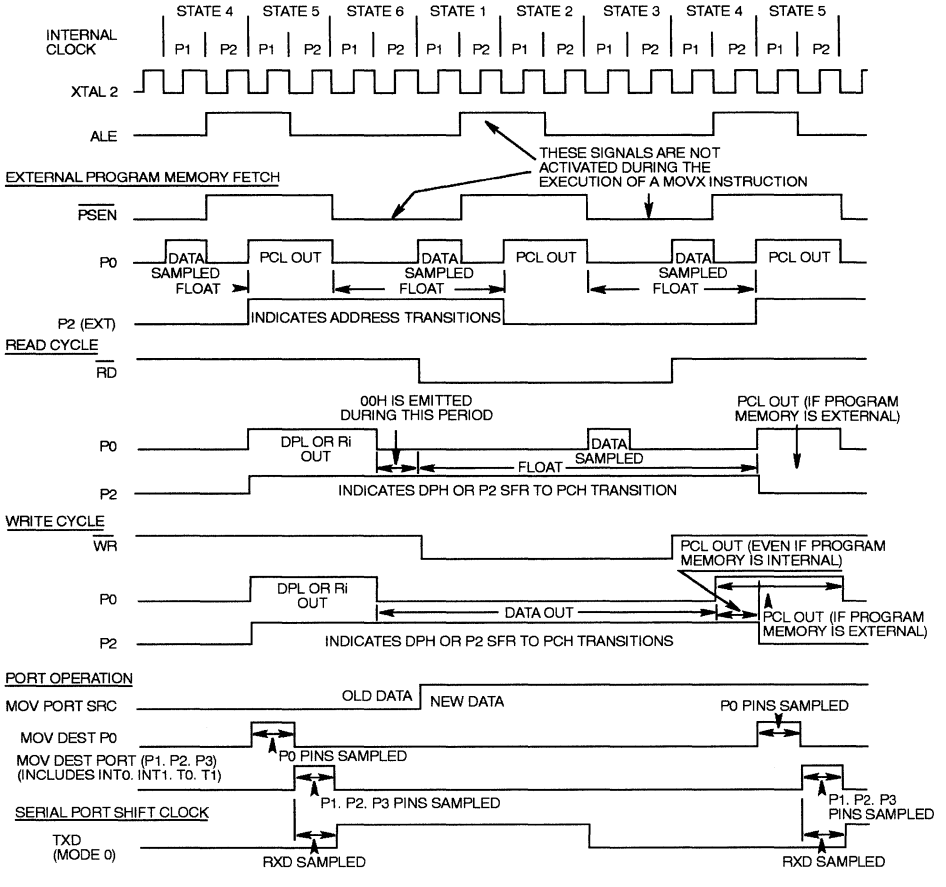
AC inputs during testing are driven at Vcc – 0.5 for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at VIH min for a logic "1" and VIL max for a logic "0".

Float Waveforms



For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded VOH/VOL level occurs. Iol/IoH ≥ ± 20 mA.

Clock Waveforms



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A = 25°C fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

Ordering Information

Commercial Temperature Range

Part Number	Type	Frequency	Package		
			Type	Footprint	Thickness
TSC80CL31–V4CA	ROMless version	4 MHz	PDIL 40	15.50 mm	5 mm
TSC80CL31–V4CB	ROMless version	4 MHz	PLCC 44	17.50 mm	4.40 mm
TSC80CL31–V4CC	ROMless version	4 MHz	PQFP 44	13.90 mm	2 mm
TSC80CL31–V4CD	ROMless version	4 MHz	PQFP 44	12.30 mm	2 mm
TSC80CL31–V4CE	ROMless version	4 MHz	VQFP 44	12 mm	1.40 mm
TSC80CL31–V4CF	ROMless version	4 MHz	TQFP 44	12 mm	1 mm
TSC80CL51xxx–V4CA	MASKROM version	4 MHz	PDIL 40	15.50 mm	5 mm
TSC80CL51xxx–V4CB	MASKROM version	4 MHz	PLCC 44	17.50 mm	4.40 mm
TSC80CL51xxx–V4CC	MASKROM version	4 MHz	PQFP 44	13.90 mm	2 mm
TSC80CL51xxx–V4CD	MASKROM version	4 MHz	PQFP 44	12.30 mm	2 mm
TSC80CL51xxx–V4CE	MASKROM version	4 MHz	VQFP 44	12 mm	1.40 mm
TSC80CL51xxx–V4CF	MASKROM version	4 MHz	TQFP 44	12 mm	1 mm

Options: Tape and Reel & Dry Pack, Secret ROM, Secret Tag and Die offering.
Please consult your sales office.

Product Marking :
For PDIL 40, PLCC 44 & QFP 44 Packages

TEMIC
Customer P/N
Temic P/N
© Intel 80, 82
YYWW Lot Number

CMOS 0 to 44 MHz Single Chip 8–bit Microntroller

Description

TEMIC's 80C52 and 80C32 are high performance CMOS versions of the 8052/8032 NMOS single chip 8 bit µC.

The fully static design of the TEMIC 80C52/80C32 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The 80C52 retains all the features of the 8052 : 8 K bytes of ROM ; 256 bytes of RAM ; 32 I/O lines ; three 16 bit timers ; a 6-source, 2-level interrupt structure ; a full duplex serial port ; and on-chip oscillator and clock circuits. In addition, the 80C52 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the RAM, the timers, the serial port and the interrupt system continue to function. In the power down mode the RAM is saved and all other functions are inoperative.

The 80C32 is identical to the 80C52 except that it has no on-chip ROM. TEMIC's 80C52/80C32 are manufactured using SCMOS process which allows them to run from 0 up to 44 MHz with Vcc = 5 V.

TEMIC's 80C52 and 80C32 are also available at 16 MHz with 2.7 V < V_{CC} < 5.5 V.

- 80C32 : Romless version of the 80C52
- 80C32/80C52-L16 : Low power version
  Vcc : 2.7 – 5.5 V Freq : 0-16 MHz
- 80C32/80C52-12 : 0 to 12 MHz
- 80C32/80C52-16 : 0 to 16 MHz
- 80C32/80C52-20 : 0 to 20 MHz
- 80C32/80C52-25 : 0 to 25 MHz
- 80C32/80C52-30 : 0 to 30 MHz
- 80C32/80C52-36 : 0 to 36 MHz
- 80C32-40 : 0 to 40 MHz*
- 80C32-42 : 0 to 42 MHz*
- 80C32-44 : 0 to 44 MHz*

* 0 to 70°C temperature range.
For other speed and temperature range availability please consult your sales office.

Features

- Power control modes
- 256 bytes of RAM
- 8 Kbytes of ROM (80C52)
- 32 programmable I/O lines
- Three 16 bit timer/counters
- 64 K program memory space
- 64 K data memory space
- Fully static design
- 0.8µ CMOS process
- Boolean processor
- 6 interrupt sources
- Programmable serial port
- Temperature range : commercial, industrial, automotive, military

Optional

- Secret ROM : Encryption
- Secret TAG : Identification number

Interface

Figure 1. Block Diagram

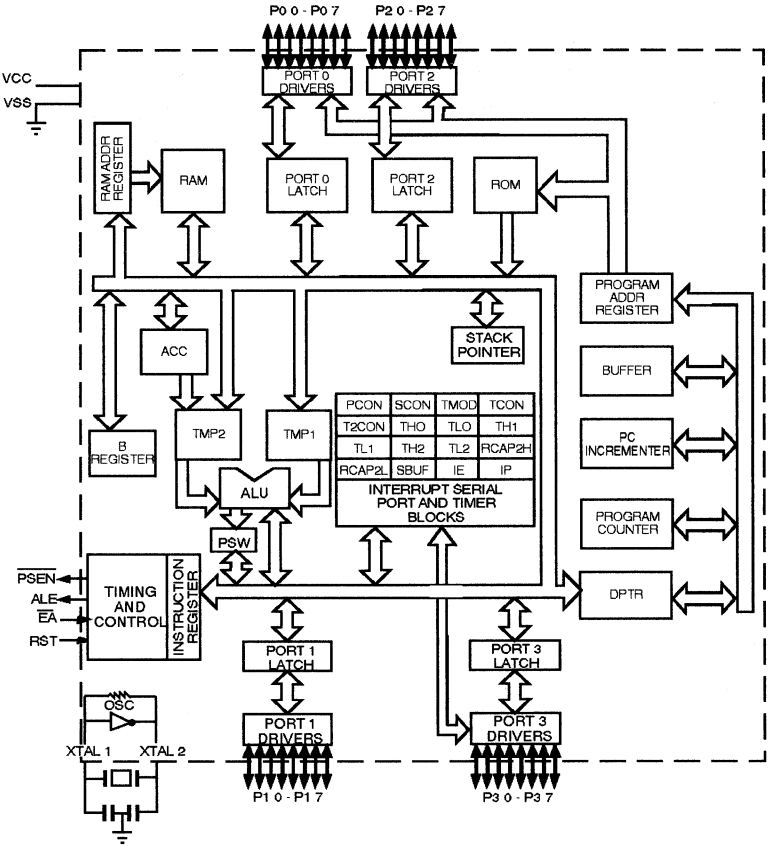
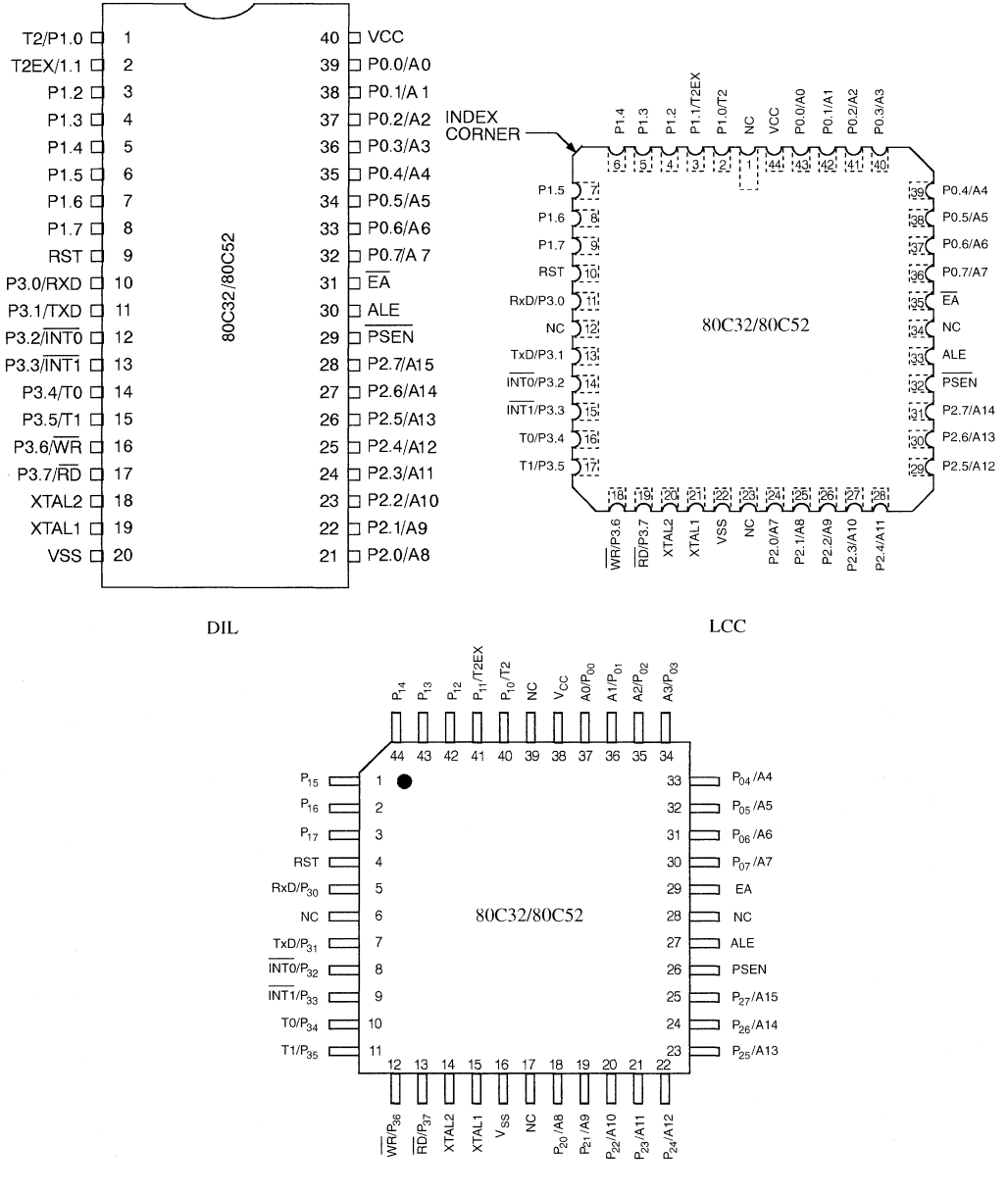


Figure 2. Pin Configuration



Diagrams are for reference only. Package sizes are not to scale.

Pin Description

VSS

Circuit ground potential.

VCC

Supply voltage during normal, Idle, and Power Down operation.

Port 0

Port 0 is an 8 bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's. Port 0 also outputs the code bytes during program verification in the 80C52. External pullups are required during program verification. Port 0 can sink eight LS TTL inputs.

Port 1

Port 1 is an 8 bit bi-directional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address byte during program verification. In the 80C52, Port 1 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

2 inputs of PORT 1 are also used for timer/counter 2 :

P1.0 [T2] : External clock input for timer/counter 2. P1.1 [T2EX] : A trigger input for timer/counter 2, to be reloaded or captured causing the timer/counter 2 interrupt.

Port 2

Port 2 is an 8 bit bi-directional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (ILL, on the data sheet) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16 bit addresses (MOVX @DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8 bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

It also receives the high-order address bits and control signals during program verification in the 80C52. Port 2 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Port 3

Port 3 is an 8 bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (ILL, on the data sheet) because of the pullups. It also serves the functions of various special features of the TEMIC 51 Family, as listed below.

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	TD (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external Data Memory write strobe)
P3.7	RD (external Data Memory read strobe)

Port 3 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

RST

A high level on this for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to V_{CC}. As soon as the Reset is applied (Vin), PORT 1, 2 and 3 are tied to one. This operation is achieved asynchronously even if the oscillator does not start-up.

ALE

Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{\text{PSEN}}$

Program Store Enable output is the read strobe to external Program Memory. PSEN is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory, two activations of PSEN are skipped during each access to external Data Memory). PSEN is not activated during fetches from internal Program Memory. PSEN can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{\text{EA}}$

When EA is held high, the CPU executes out of internal Program Memory (unless the Program Counter exceeds 1 FFFH). When EA is held low, the CPU executes only out of external Program Memory. EA must not be floated.

XTAL1

Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

XTAL2

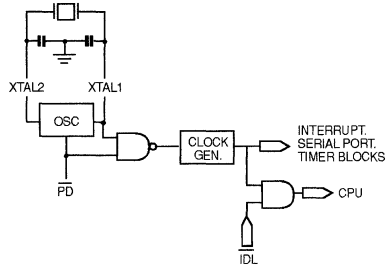
Output of the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.

Idle And Power Down Operation

Figure 3 shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. Idle mode operation allows the interrupt, serial port, and timer blocks to continue to function, while the clock to the CPU is gated off.

These special modes are activated by software via the Special Function Register, PCON. Its hardware address is 87H. PCON is not bit addressable.

Figure 3.Idle and Power Down Hardware.



PCON : Power Control Register

(MSB) (LSB)

SMOD	–	–	–	GF1	GF0	PD	IDL

Symbol	Position	Name and Function
SMOD	PCON.7	Double Baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2 or 3.
–	PCON.6	(Reserved)
–	PCON.5	(Reserved)
–	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.

If 1's are written to PD and IDL at the same time. PD takes, precedence. The reset value of PCON is (000X0000).

Idle Mode

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety : the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during idle. *Table 1* describes the status of the external pins during Idle mode.

There are three ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

Power Down Mode

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register is saved during power down mode. The hardware reset initiates the Special Fucntion Register. In the Power Down mode, VCC may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the power down mode is entered, and that the voltage is restored before the hardware reset is applied which freezes the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

Table 1 describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a 1, the port pin is held high during the power down mode by the strong pullup, T1, shown in *Figure 4.*

Table 1. Status of the external pins during idle and power down modes.

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

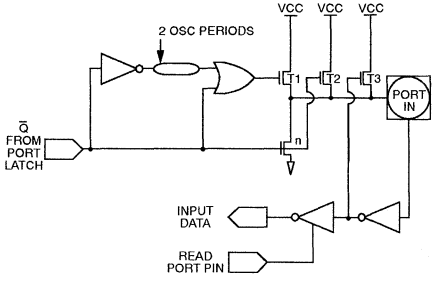
Stop Clock Mode

Due to static design, the TEMIC 80C32/C52 clock speed can be reduced until 0 MHz without any data loss in memory or registers. This mode allows step by step utilization, and permits to reduce system power consumption by bringing the clock frequency down to any value. At 0 MHz, the power consumption is the same as in the Power Down Mode.

I/O Ports

The I/O buffers for Ports 1, 2 and 3 are implemented as shown in *figure 4.*

Figure 4.I/O Buffers in the 80C52 (Ports 1, 2, 3).



When the port latch contains a 0, all pFETS in figure 4 are off while the nFET is turned on. When the port latch makes a 0-to-1 transition, the nFET turns off. The strong pFET, T1, turns on for two oscillator periods, pulling the output high very rapidly. As the output line is drawn high, pFET T3 turns on through the inverter to supply the IOH source current. This inverter and T form a latch which holds the 1 and is supported by T2.

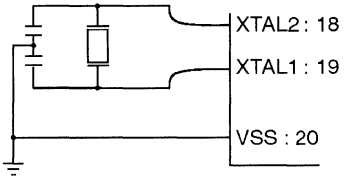
When Port 2 is used as an address port, for access to external program of data memory, any address bit that contains a 1 will have his strong pullup turned on for the entire duration of the external memory access.

When an I/O pin on Ports 1, 2, or 3 is used as an input, the user should be aware that the external circuit must sink current during the logical 1-to-0 transition. The maximum sink current is specified as ITL under the D.C. Specifications. When the input goes below approximately 2 V, T3 turns off to save ICC current. Note, when returning to a logical 1, T2 is the only internal pullup that is on. This will result in a slow rise time if the user's circuit does not force the input line high.

Oscillator Characteristics

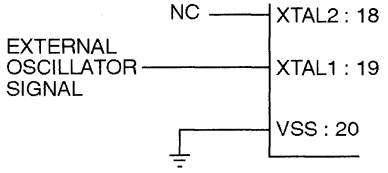
XTAL1 and XTAL2 are the input and output respectively, of an inverting amplifier which is configured for use as an on-chip oscillator, as shown in figure 5. Either a quartz crystal or ceramic resonator may be used.

Figure 5. Crystal Oscillator.



To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in *figure 6*. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

Figure 6. External Drive Configuration.



Hardware Description

Same as for the 80C51, plus a third timer/counter :

Timer/Event Counter 2

Timer 2 is a 16 bit timer/counter like Timers 0 and 1, it can operate either as a timer or as an event counter. This is selected by bit C/$\overline{T2}$ in the Special Function Register T2CON (Figure 1). It has three operating modes : "capture", "autoload" and "baud rate generator", which are selected by bits in T2CON as shown in *Table 2*.

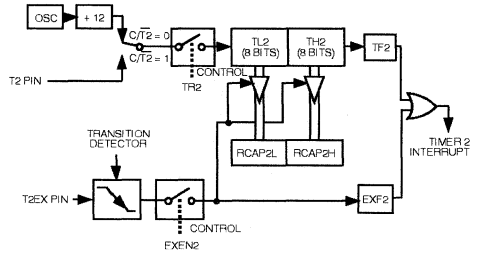
In the capture mode there are two options which are selected by bit EXEN2 in T2CON; If EXEN2 = 0, then Timer 2 is a 16 bit timer or counter which upon overflowing sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively, (RCAP2L and RCAP2H are new Special Function Register in the 80C52). In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt.

Table 2. Timer 2 Operating Modes.

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16 bit auto-reload
0	1	1	16 bit capture
1	X	1	baud rate generator
X	X	0	(off)

The capture mode is illustrated in *Figure 7.*

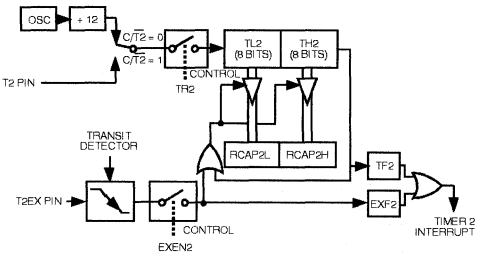
Figure 7. Timer 2 in Capture Mode.



In the auto-reload mode there are again two options, which are selected by bit EXEN2 in T2CON.If EXEN2 = 0, then when Timer 2 rolls over it does not only set TF2 but also causes the Timer 2 register to be reloaded with the 16 bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16 bit reload and set EXF2.

The auto-reload mode is illustrated in *Figure 8.*

Figure 8. Timer in Auto-Reload Mode.



(MSB) (LSB)

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

The baud rate generator mode is selected by : RCLK = 1 and/or TCLK = 1.

Symbol	Position	Name and Significance
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 OR TCLK = 1.
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/$\overline{T2}$	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered).
CP/$\overline{RL2}$	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN 2 = 1. When cleared, auto reloads will occur either with Timer 2 overflows or negative transition at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

80C52 with Secret ROM

TEMIC offers 80C52 with the encrypted secret ROM option to secure the ROM code contained in the 80C52 microcontrollers.

The clear reading of the program contained in the ROM is made impossible due to an encryption through several random keys implemented during the manufacturing process.

The keys used to do such encryption are selected randomwise and are definitely different from one microcontroller to another.

This encryption is activated during the following phases :

- Everytime a byte is addressed during a verify of the ROM content, a byte of the encryption array is selected.
- MOVC instructions executed from external program memory are disabled when fetching code bytes from internal memory.
- EA is sampled and latched on reset, thus all state modification are disabled.

For further information please refer to the application note (ANM053) available upon request.

80C52 with Secret TAG

TEMIC offers special 64-bit identifier called "SECRET TAG" on the microcontroller chip.

The Secret Tag option is available on both ROMless and masked microcontrollers.

The Secret Tag feature allows serialization of each microcontroller for identification of a specific equipment. A unique number per device is implemented in the chip during manufacturing process. The serial number is a 64-bit binary value which is contained and addressable in the Special Function Registers (SFR) area.

This Secret Tag option can be read-out by a software routine and thus enables the user to do an individual identity check per device. This routine is implemented inside the microcontroller ROM memory in case of masked version which can be kept secret (and then the value of the Secret Tag also) by using a ROM Encryption.

For further information, please refer to the application note (ANM031) available upon request.

Electrical Characteristics

Absolute Maximum Ratings*

Ambiant Temperature Under Bias :
C = commercial ..... 0°C to 70°C
I = industrial ..... –40°C to 85°C
Storage Temperature ..... –65°C to + 150°C
Voltage on VCC to VSS ..... –0.5 V to + 7 V
Voltage on Any Pin to VSS ..... –0.5 V to V_{CC} + 0.5 V
Power Dissipation ..... 1 W
* This value is based on the maximum allowable die temperature and the thermal resistance of the package

**** Notice***

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Parameters

TA = 0°C to 70°C ; VSS = 0 V ; VCC = 5 V ± 10 % ; F = 0 to 44 MHz
TA = –40°C + 85°C ; VSS = 0 V ; VCC = 5 V ± 10 % ; F = 0 to 36 MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 Vcc – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 1.4	Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc	Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3)		0.3 0.45 1.0	V V V	IOL = 100 µA IOL = 1.6 mA (note 2) IOL = 3.5 mA
VOL1	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)		0.3 0.45 1.0	V V V	IOL = 200 µA IOL = 3.2 mA (note 2) IOL = 7.0 mA
VOH	Output High Voltage Port 1, 2, 3	Vcc – 0.3		V	IOH = – 10 µA
		Vcc – 0.7		V	IOH = – 30 µA
		Vcc – 1.5		V	IOH = – 60 µA VCC = 5 V ± 10 %
VOH1	Output High Voltage (Port 0, ALE, $\overline{PSEN}$)	Vcc – 0.3		V	IOH = – 200 µA
		Vcc – 0.7		V	IOH = – 3.2 mA
		Vcc – 1.5		V	IOH = – 7.0 mA VCC = 5 V ± 10 %
IIL	Logical 0 Input Current (Ports 1, 2 and 3)		– 50	µA	Vin = 0.45 V
ILI	Input leakage Current		± 10	µA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		– 650	µA	Vin = 2.0 V
IPD	Power Down Current		50	µA	Vcc = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	200	KOhm	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current Freq = 1 MHz Icc op Icc idle Freq = 6 MHz Icc op Icc idle Freq ≥ 12 MHz Icc op = 1.25 Freq (MHz) + 5 mA Icc idle = 0.36 Freq (MHz) + 2.7 mA		 1.8 1 10 4	 mA mA mA mA	Vcc = 5.5 V

Absolute Maximum Ratings*

Ambient Temperature Under Bias :
A = Automotive ..... –40°C to +125°C
Storage Temperature ..... –65°C to + 150°C
Voltage on VCC to VSS ..... –0.5 V to + 7 V
Voltage on Any Pin to VSS ..... –0.5 V to VCC + 0.5 V
Power Dissipation ..... 1 W
* This value is based on the maximum allowable die temperature and the thermal resistance of the package

**** Notice***

Stresses above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Parameters

TA = –40°C + 125°C ; VSS = 0 V ; VCC = 5 V ± 10 % ; F = 0 to 36 MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 Vcc – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 1.4	Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc	Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3)		0.3 0.45 1.0	V V V	IOL = 100 µA IOL = 1.6 mA (note 2) IOL = 3.5 mA
VOL1	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)		0.3 0.45 1.0	V V V	IOL = 200 µA IOL = 3.2 mA (note 2) IOL = 7.0 mA
VOH	Output High Voltage Port 1, 2 and 3	Vcc – 0.3		V	IOH = – 10 µA
		Vcc – 0.7		V	IOH = – 30 µA
		Vcc – 1.5		V	IOH = – 60 µA VCC = 5 V ± 10 %
VOH1	Output High Voltage (Port 0, ALE, $\overline{PSEN}$)	Vcc – 0.3		V	IOH = – 200 µA
		Vcc – 0.7		V	IOH = – 3.2 mA
		Vcc – 1.5		V	IOH = – 7.0 mA VCC = 5 V ± 10 %
IIL	Logical 0 Input Current (Ports 1, 2 and 3)		– 75	µA	Vin = 0.45 V
ILI	Input leakage Current		±10	µA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		– 750	µA	Vin = 2.0 V
IPD	Power Down Current		75	µA	Vcc = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	200	KOhm	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current Freq = 1 MHz Icc op Icc idle Freq = 6 MHz Icc op Icc idle Freq ≥ 12 MHz Icc op = 1.25 Freq (MHz) + 5 mA Icc idle = 0.36 Freq (MHz) + 2.7 mA		 1.8 1 10 4	 mA mA mA mA	Vcc = 5.5 V

Absolute Maximum Ratings*

Ambient Temperature Under Bias :
M = Military ..... –55°C to +125°C
Storage Temperature ..... –65°C to + 150°C
Voltage on VCC to VSS ..... –0.5 V to + 7 V
Voltage on Any Pin to VSS ..... –0.5 V to VCC + 0.5 V
Power Dissipation ..... 1 W
* This value is based on the maximum allowable die temperature and the thermal resistance of the package

**** Notice***

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Parameters

TA = –55°C + 125°C ; Vss = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 36 MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 Vcc – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 1.4	Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc	Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3)		0.45	V	IOL = 1.6 mA (note 2)
VOL1	Output Low Voltage (Port 0, ALE, PSEN)		0.45	V	IOL = 3.2 mA (note 2)
VOH	Output High Voltage (Port 1, 2 and 3)	2.4		V	IOH = – 60 µA Vcc = 5 V ± 10 %
		0.75 Vcc		V	IOH = – 25 µA
		0.9 Vcc		V	IOH = – 10 µA
VOH1	Output High Voltage (Port 0 in External Bus Mode, ALE, PEN)	2.4		V	IOH = – 400 µA Vcc = 5 V ± 10 %
		0.75 Vcc		V	IOH = – 150 µA
		0.9 Vcc		V	IOH = – 40 µA
IIL	Logical 0 Input Current (Ports 1, 2 and 3)		– 75	µA	Vin = 0.45 V
ILI	Input leakage Current		+/– 10	µA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		– 750	µA	Vin = 2.0 V
IPD	Power Down Current		75	µA	Vcc = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	200	KΩ	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current Freq = 1 MHz Icc op Icc idle Freq = 6 MHz Icc op Icc idle Freq ≥ 12 MHz Icc op = 1.25 Freq (MHz) + 5 mA Icc idle = 0.36 Freq (MHz) + 2.7 mA		 1.8 1 10 4	 mA mA mA mA	Vcc = 5.5 V

Absolute Maximum Ratings*

Ambient Temperature Under Bias :
C = Commercial ..... 0°C to 70°C
I = Industrial ..... −40 to 85°C
Storage Temperature ..... −65°C to + 150°C
Voltage on VCC to VSS ..... −0.5 V to + 7 V
Voltage on Any Pin to VSS ..... −0.5 V to VCC + 0.5 V
Power Dissipation ..... 1 W**
** This value is based on the maximum allowable die temperature and the thermal resistance of the package

** Notice*

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2

DC Characteristics

TA = 0°C to 70°C ; Vcc = 2.7 V to 5.5 V ; Vss = 0 V ; F = 0 to 16 MHz
TA = –40°C to 85°C ; Vcc = 2.7 V to 5.5 V

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 V_{CC} – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 V_{CC} + 1.4	V_{CC} + 0.5	V	
VIH2	Input High Voltage to RST for Reset	0.7 V_{CC}	V_{CC} + 0.5	V	
VIH1	Input High Voltage to XTAL1	0.7 V_{CC}	V_{CC} + 0.5	V	
VPD	Power Down Voltage to Vcc in PD Mode	2.0	5.5	V	
VOL	Output Low Voltage (Ports 1, 2, 3)		0.45	V	IOL = 0.8 mA (note 2)
VOL1	Output Low Voltage Port 0, ALE, $\overline{PSEN}$		0.45	V	IOL = 1.6 mA (note 2)
VOH	Output High Voltage Ports 1, 2, 3	0.9 Vcc		V	IOH = – 10 µA
VOH1	Output High Voltage (Port 0 in External Bus Mode), ALE, $\overline{PSEN}$	0.9 Vcc		V	IOH = – 40 µA
IIL	Logical 0 Input Current Ports 1, 2, 3		– 50	µA	Vin = 0.45 V
ILI	Input Leakage Current		± 10	µA	0.45 < Vin < V_{CC}
ITL	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		– 650	µA	Vin = 2.0 V
IPD	Power Down Current		50	µA	V_{CC} = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	200	kΩ	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, T_A = 25°C

Maximum Icc (mA)

	OPERATING (NOTE 1)				IDLE (NOTE 1)			
FREQUENCY/Vcc	2.7 V	3 V	3.3 V	5.5 V	2.7 V	3 V	3.3 V	5.5 V
1 MHz	0.8 mA	1 mA	1.1 mA	1.8 mA	400 µA	500 µA	600 µA	1 mA
6 MHz	4 mA	5 mA	6 mA	10 mA	1.5 mA	1.7 mA	2 mA	4 mA
12 MHz	8 mA	10 mA	12 mA		2.5 mA	3 mA	3.5 mA	
16 MHz	10 mA	12 mA	14 mA		3 mA	3.8 mA	4.5 mA	
Freq > 12 MHz (Vcc = 5.5 V)	Icc (mA) = 1.25 × Freq (MHz) + 5 Icc Idle (mA) = 0.36 × Freq (MHz) + 2.7							

Note 1 : ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + .5 V, VIH = VCC –.5 V ; XTAL2 N.C. ; EA = RST = Port 0 = VCC. ICC would be slighty higher if a crystal oscillator used.

Idle ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + 5 V, VIH = VCC –.5 V ; XTAL2 N.C ; Port 0 = VCC ; EA = RST = VSS.

Power Down ICC is measured with all output pins disconnected ; EA = PORT 0 = VCC ; XTAL2 N.C. ; RST = VSS.

Note 2 : Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLS of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operations. In the worst cases (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45 V may exceed 0,45 V with maxi VOL peak 0.6 V. A Schmitt Trigger use is not necessary.

Figure 9. ICC Test Condition, Idle Mode. All other pins are disconnected.

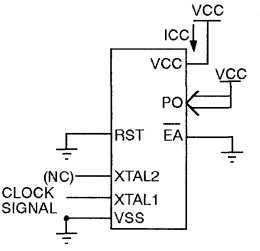


Figure 10. ICC Test Condition, Active Mode. All other pins are disconnected.

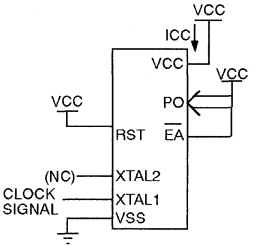


Figure 11. ICC Test Condition, Power Down Mode. All other pins are disconnected.

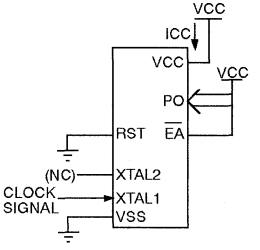
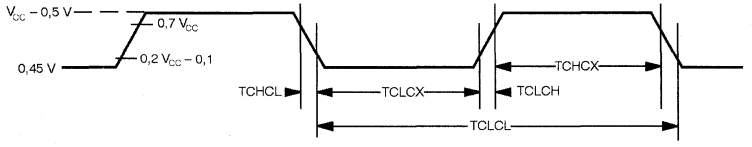


Figure 12. Clock Signal Waveform for ICC Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.



Explanation of the AC Symbol

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example :

TAVLL = Time for Address Valid to ALE low.

TLLPL = Time for ALE low to $\overline{\text{PSEN}}$ low.

A : Address.
C : Clock.
D : Input data.
H : Logic level HIGH
I : Instruction (program memory contents).
L : Logic level LOW, or ALE.
P : PSEN.
Q : Output data.
R : READ signal.
T : Time.
V : Valid.
W : WRITE signal.
X : No longer a valid logic level.
Z : Float.

2

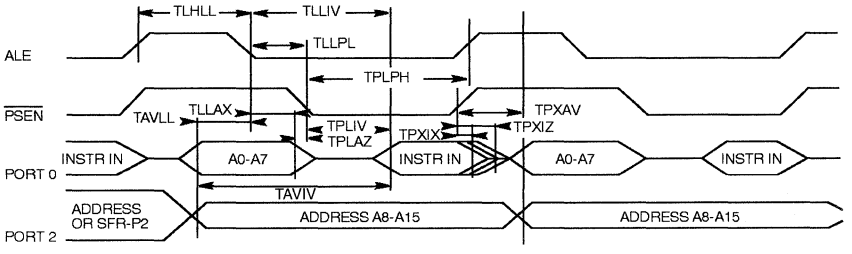
AC Parameters

TA = 0 to + 70°C ; Vss = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 44 MHz
TA = 0 to +70°C ; Vss = 0 V ; 2.7 V < Vcc < 5.5 V ; F = 0 to 16 MHz
TA = –40° to + 85°C ; Vss = 0 V ; 2.7 V < Vcc < 5.5 V ; F = 0 to 16 MHz
TA = –55° + 125°C ; Vss = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 36 MHz
(Load Capacitance for PORT 0, ALE and PSEN = 100 pF ; Load Capacitance for all other outputs = 80 pF)

External Program Memory Characteristics (values in ns)

		16 MHz		20 MHz		25 MHz		30 MHz		36 MHz		40 MHz		42 MHz		44 MHz	
SYM-BOL	PARAMETER	min	max	min	max	min	max	min	max	min	max	min	max	min	max	min	max
TLHLL	ALE Pulse Width	110		90		70		60		50		40		35		30	
TAVLL	Address valid to ALE	40		30		20		15		10		9		8		7	
TLLAX	Address Hold After ALE	35		35		35		35		35		30		25		17	
TLLIV	ALE to valid instr in		185		170		130		100		80		70		65		65
TLLPL	ALE to PSEN	45		40		30		25		20		15		13		12	
TPLPH	PSEN pulse Width	165		130		100		80		75		65		60		54	
TPLIV	PSEN to valid instr in		125		110		85		65		50		45		40		35
TPXIX	Input instr Hold After PSEN	0		0		0		0		0		0		0		0	
TPXIZ	Input instr Float After PSEN		50		45		35		30		25		20		15		10
TPXAV	PSEN to Address Valid	55		50		40		35		30		25		20		15	
TAVIV	Address to Valid instr in		230		210		170		130		90		80		75		70
TPLAZ	PSEN low to Address Float		10		10		8		6		5		5		5		5

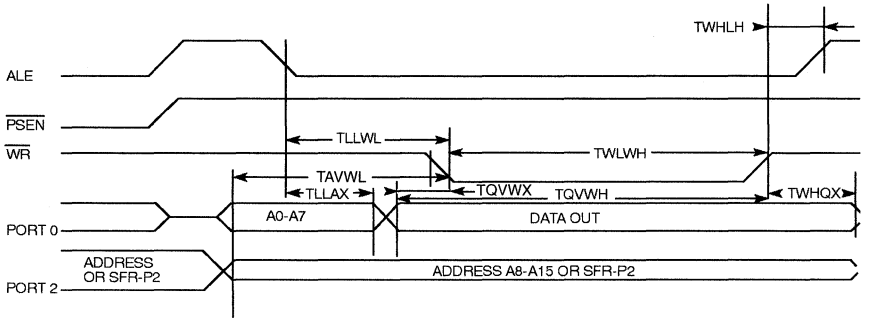
External Program Memory Read Cycle



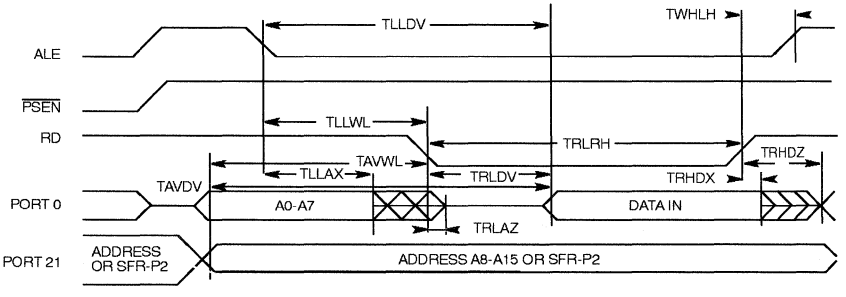
External Data Memory Characteristics (values in ns)

		16 MHz		20 MHz		25 MHz		30 MHz		36 MHz		40 MHz		42 MHz		44 MHz	
SYM-BOL	PARAMETER	min	max	min	max	min	max	min	max	min	max	min	max	min	max	min	max
TRLRH	RD pulse Width	340		270		210		180		120		100		90		80	
TWLWH	WR pulse Width	340		270		210		180		120		100		90		80	
TLLAX	Address Hold After ALE	85		85		70		55		35		30		25		25	
TRLDV	RD to Valid Data in		240		210		175		135		110		90		80		70
TRHDX	Data hold after RD	0		0		0		0		0		0		0		0	
TRHDZ	Data float after RD		90		90		80		70		50		45		40		35
TLLDV	ALE to Valid Data In		435		370		290		235		170		150		140		130
TAVDV	Address to Valid Data IN		480		400		320		260		190		180		175		170
TLLWL	ALE to WR or RD	150	250	135	170	120	130	90	115	70	100	60	95	55	90	50	85
TAVWL	Address to WR or RD	180		180		140		115		75		65		60		55	
TQVWX	Data valid to WR transition	35		35		30		20		15		10		8		6	
TQVWH	Data Setup to WR transition	380		325		250		215		170		160		150		140	
TWHQX	Data Hold after WR	40		35		30		20		15		10		8		6	
TRLAZ	RD low to Address Float		0		0		0		0		0		0		0		0
TWHLH	RD or WR high to ALE high	35	90	35	60	25	45	20	40	20	40	15	35	13	33	13	33

External Data Memory Write Cycle



External Data Memory Read Cycle

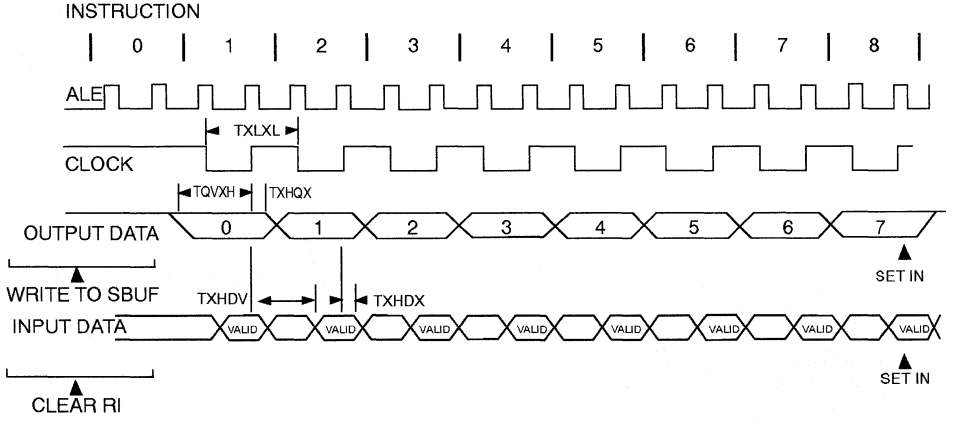


Serial Port Timing – Shift Register Mode (values in ns)

		16 MHz		20 MHz		25 MHz		30 MHz		36 MHz		40 MHz		42 MHz		44 MHz	
SYM-BOL	PARAMETER	min	max	min	max	min	max	min	max	min	max	min	max	min	max	min	max
TXLXL	Serial Port Clock Cycle Time	750		600		480		400		330		250		230		227	
TQVXH	Output Data Setup to Clock Rising Edge	563		480		380		300		220		170		150		140	
TXHQX	Output Data Hold after Clock Rising Edge	63		90		65		50		45		35		30		25	
TXHDX	Input Data Hold after Clock Rising Edge	0		0		0		0		0		0		0		0	
TXHDV	Clock Rising Edge to Input Data Valid		563		450		350		300		250		200		180		160

2

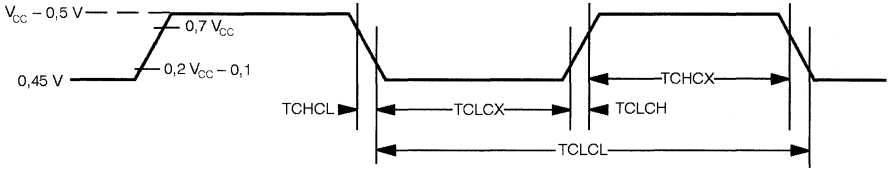
Shift Register Timing Waveforms



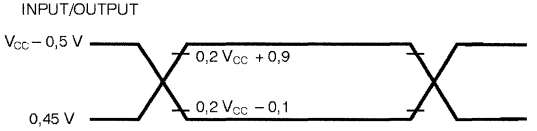
External Clock Drive Characteristics (XTAL1)

SYMBOL	PARAMETER	MIN	MAX	UNIT
FCLCL	Oscillator Frequency		44	MHz
TCLCL	Oscillator period	22.7		ns
TCHCX	High Time	5		ns
TCLCX	Low Time	5		ns
TCLCH	Rise Time		5	ns
TCHCL	Fall Time		5	ns

External Clock Drive Waveforms

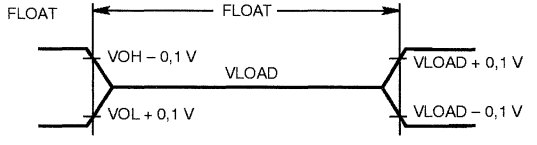


AC Testing Input/Output Waveforms



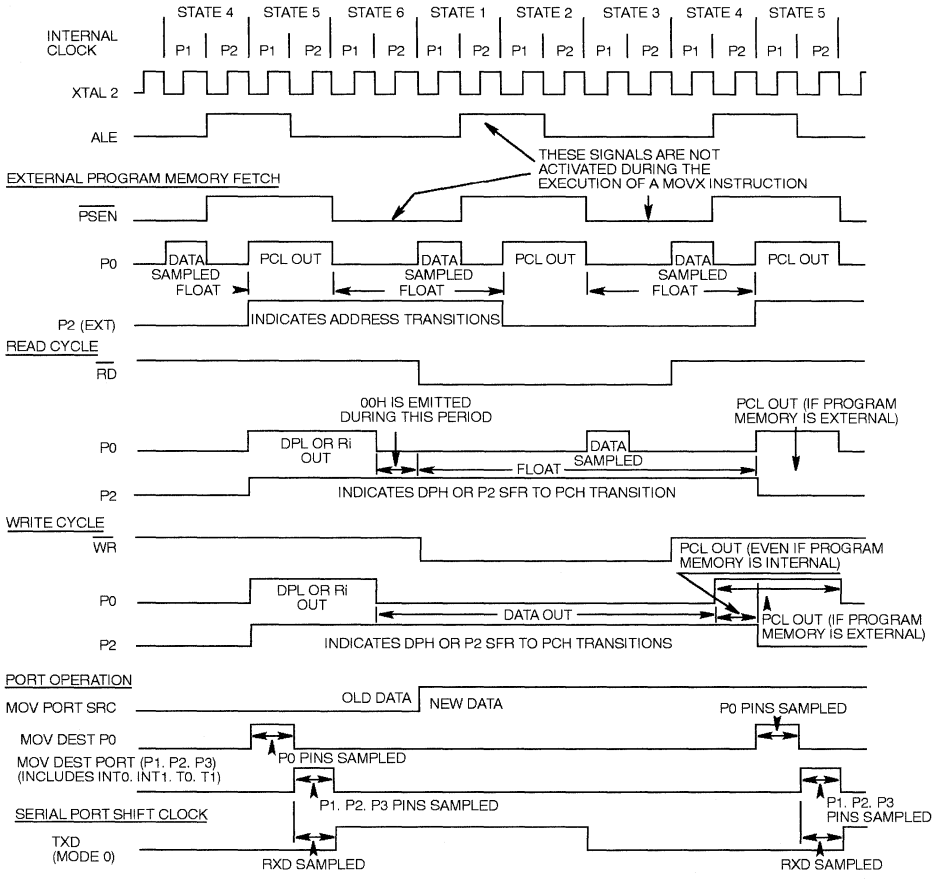
AC inputs during testing are driven at Vcc – 0.5 for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at VIH min for a logic "1" and VIL max for a logic "0".

Float Waveforms



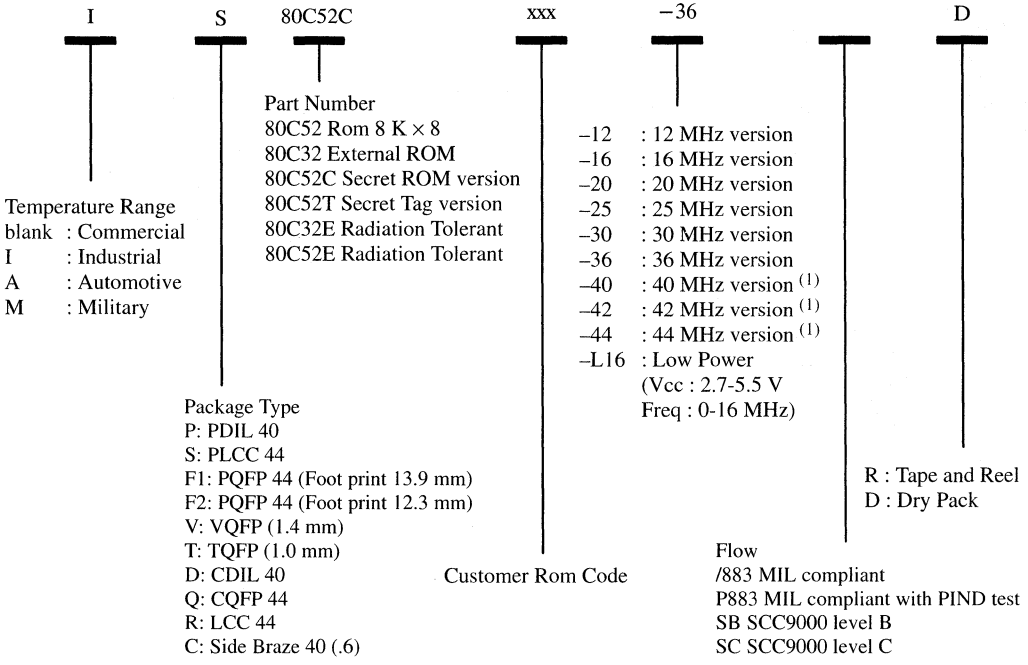
For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded VOH/VOL level occurs. Iol/IoH ≥ ± 20 mA.

Clock Waveforms



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A = 25°C fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

Ordering Information



(1) Only for 80C31 at commercial range.

80C154/83C154

CMOS 0 to 36 MHz Single Chip 8–bit Microcontroller

Description

TEMIC's 80C154 and 83C154 are high performance CMOS single chip µC. The 83C154 retains all the features of the 80C52 with extended ROM capacity (16 K bytes), 256 bytes of RAM, 32 I/O lines, a 6-source 2-level interrupts, a full duplex serial port, an on-chip oscillator and clock circuits, three 16 bit timers with extra features : 32 bit timer and watchdog functions. Timer 0 and 1 can be configured by program to implement a 32 bit timer. The watchdog function can be activated either with timer 0 or timer 1 or both together (32 bit timer).

In addition, the 83C154 has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the RAM is saved, and the timers, the serial port and the interrupt system continue to function. In the power down mode the RAM is saved and the timers, serial port and interrupt continue to function when driven by external clocks. In addition as for the TEMIC 80C51/80C52, the stop clock mode is also available.

The 80C154 is identical to the 83C154 except that it has no on-chip ROM. TEMIC's 80C154 and 83C154 are manufactured using SCMOS process which allows them to run from 0 up to 36 MHz with Vcc = 5 V.

- 80C154 : ROMless version of the 83C154µ
- 80C154/83C154-12 : 0 to 12 MHz
- 80C154/83C154-16 : 0 to 16 MHz
- 80C154/83C154-20 : 0 to 20 MHz
- 80C154/83C154-25 : 0 to 25 MHz
- 80C154/83C154-30 : 0 to 30 MHz
- 80C154/83C154-36 : 0 to 36 MHz
- 80C154/83C154-L16 : Low power version
  VCC : 2.7-5.5 V Freq : 0-16 MHz

For other speed and temperature range availability please consult your sales office.

Features

- Power control modes
- 256 bytes of RAM
- 16 Kbytes of ROM (83C154)
- 32 Programmable I/O lines (programmable impedance)
- Three 16 bit timer/counters (including watchdog and 32 bit timer)
- 64 K program memory space
- 64 K data memory space
- Fully static design
- 0.8µ CMOS process
- Boolean processor
- 6 interrupt sources
- Programmable serial port
- Temperature range : commercial, industrial, automotive, military

Optional

- Secret ROM : Encryption
- Secret TAG : Identification number

Interface

Figure 1. Block Diagram

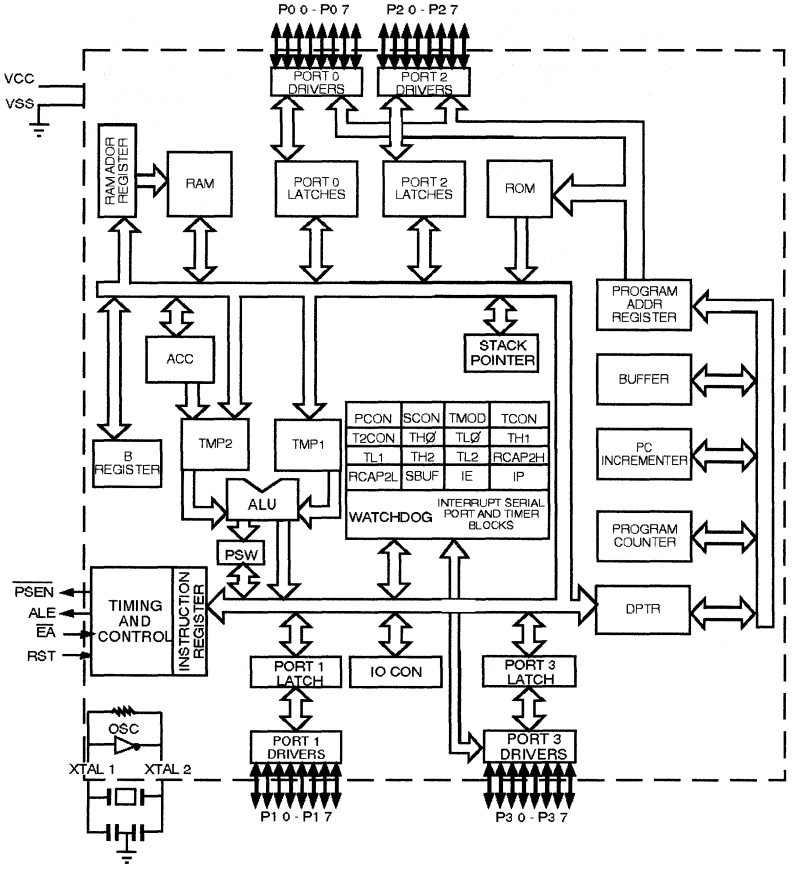
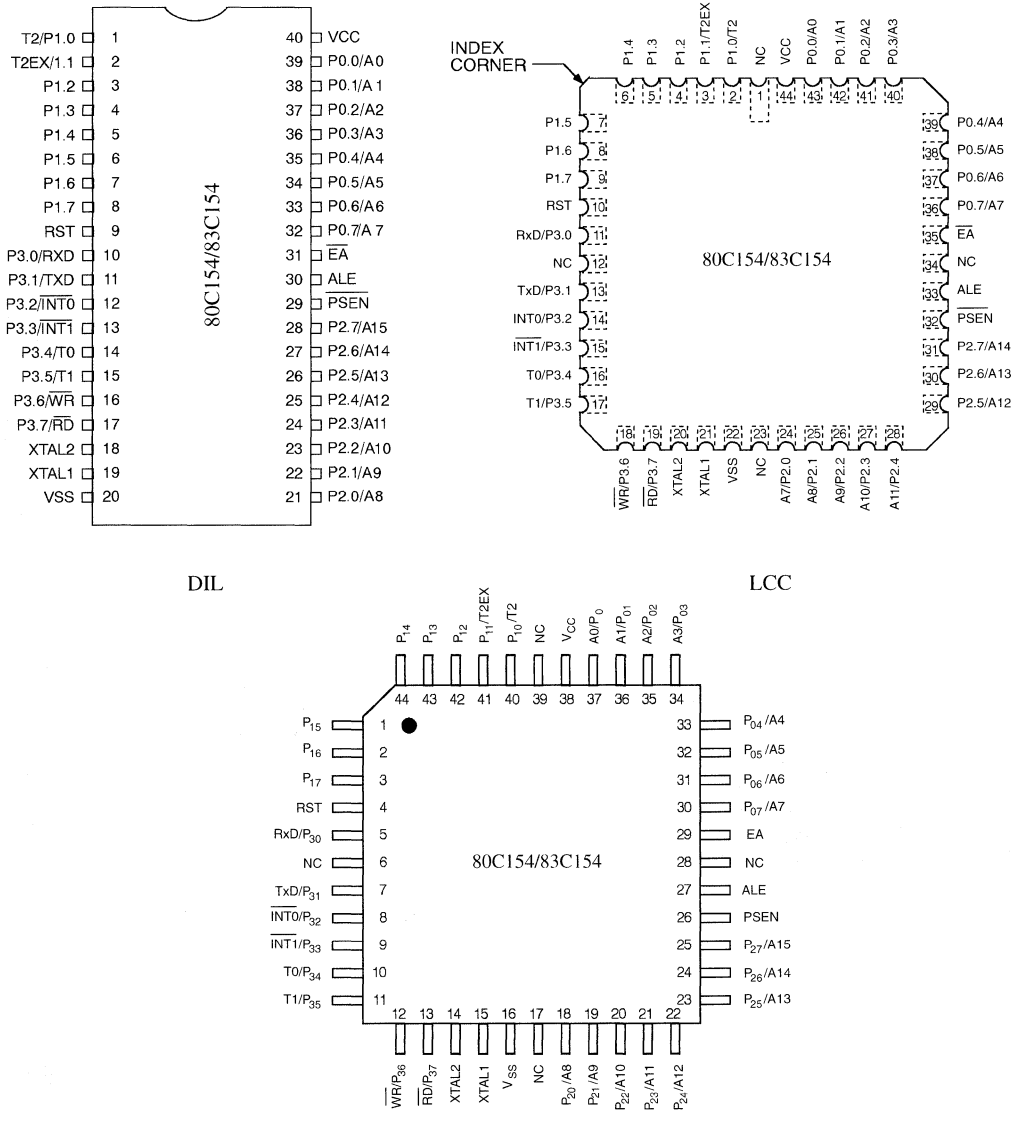


Figure 2. Pin Configuration



Diagrams are for reference only. Package sizes are not to scale

Pin Description

Vss

Circuit Ground Potential.

VCC

Supply voltage during normal, Idle, and Power Down operation.

Port 0

Port 0 is an 8 bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's. Port 0 also outputs the code bytes during program verification in the 83C154. External pullups are required during program verification. Port 0 can sink eight LS TTL inputs.

Port 1

Port 1 is an 8 bit bi-directional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address byte during program verification. In the 83C154, Port 1 can sink or source three LS TTL inputs. It can drive CMOS inputs without external pullups.

2 inputs of PORT 1 are also used for timer/counter 2 :

P1.0 [T2] : External clock input for timer/counter 2. P1.1 [T2EX] : A trigger input for timer/counter 2, to be reloaded or captured causing the timer/counter 2 interrupt.

Port 2

Port 2 is an 8 bit bi-directional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (ILL, on the data sheet) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16 bit addresses (MOVX @DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8 bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

It also receives the high-order address bits and control signals during program verification in the 83C154. Port 2 can sink or source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Port 3

Port 3 is an 8 bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (ILL, on the data sheet) because of the pullups. It also serves the functions of various special features of the TEMIC 51 Family, as listed below.

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	TD (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external Data Memory write strobe)
P3.7	RD (external Data Memory read strobe)

Port 3 can sink or source three LS TTL inputs. It can drive CMOS inputs without external pullups.

RST

A high level on this for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to VCC. As soon as the result is applied (Vin), PORT 1, 2 and 3 are tied to 1. This operation is achieved asynchronously even if the oscillator is not start up.

ALE

Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink or source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{\text{PSEN}}$

Program Store Enable output is the read strobe to external Program Memory. PSEN is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory, two activations of PSEN are skipped during each access to external Data Memory). PSEN is not activated during fetches from internal Program Memory. PSEN can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{\text{EA}}$

When EA is held high, the CPU executed out of internal Program Memory (unless the Program Counter exceeds 3FFFH). When EA is held low, the CPU executes only out of external Program Memory. EA must not be floated.

XTAL1

Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

XTAL2

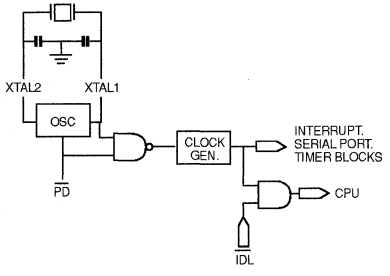
Output of the inverting amplifier that forms the oscillator, and input to the internal clock generator. This pin should be floated when an external oscillator is used.

2

Idle and Power Down Operation

Figure 3 shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. The interrupt, serial port, and timer blocks continue to function only with external clock (INT0, INT1, T0, T1).

Figure 3. Idle and Power Down Hardware.



Idle Mode operation allows the interrupt, serial port, and timer blocks to continue to function with internal or external clocks, while the clock to CPU is gated off. The special modes are activated by software via the Special Function Register, PCON. Its hardware address is 87H. PCON is not bit addressable.

PCON : Power Control Register

(MSB) (LSB)

SMOD	HPD	RPD	–	GF1	GF0	PD	IDL

Symbol	Position	Name and Function
SMOD	PCON.7	Double Baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2 or 3.
HPD	PCON.6	Hard power Down bit. Setting this bit allows CPU to enter in Power Down state on an external event (1 to 0 transition) on bit T1 (p. 3.5) the CPU quit the Hard Power Down mode when bit T1 p. 3.5) goes high or when reset is activated.
RPD	PCON.5	Recover from Idle or Power Down bit. When 0 RPD has no effetc. When 1, RPD permits to exit from idle or Power Down with any non enabled interrupt source (except time 2). In this case the program start at the next address. When interrupt is enabled, the appropriate interrupt routine is serviced.
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.

If 1's are written to PD and IDL at the same time. PD takes, precedence. The reset value of PCON is (000X0000).

Idle Mode

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety : the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during idle. In the idle mode, the internal clock signal is gated off to the CPU, but interrupt, timer and serial port functions are maintained. Table 1 describes the status of the external pins during Idle mode. There are three ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

The third way to terminate the Idle mode is the activation of any disabled interrupt when recover is programmed (RPD = 1). This will cause PCON.0 to be cleared. No interrupt is serviced. The next instruction is executed. If interrupt are disabled and RPD = 0, only a reset can cancel the Idle mode.

Power Down Mode

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register is saved during power down mode. The three ways to terminate the Power Down mode are the same than the Idle mode. But since the onchip oscillator is stopped, the external interrupts, timers and serial port must be sourced by external clocks only, via INT0, INT1, T0, T1.

In the Power Down mode, VCC may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the power down mode is entered, and that the voltage is restored before the hardware reset is applied which frees the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

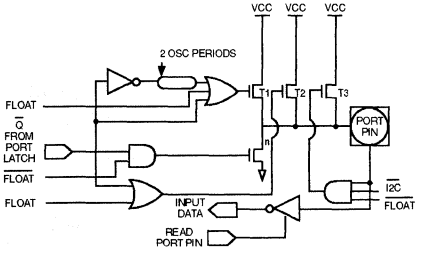
When using voltage reduction : interrupt, timers and serial port functions are guaranteed in the VCC specification limits.

Table 1 describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the port switches from 0 to 1, the port pin is held high during the power down mode by the strong pullup, T1, shown in figure 4.

Table 1. Status of the external pins during idle and power down modes.

MODE	PROGRAM MEMORY	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Figure 4. I/O Buffers in the 83C154 (Ports 1, 2, 3).



Stop Clock Mode

Due to static design, the TEMIC 83C154 clock speed can be reduced until 0 MHz without any data loss in memory or registers. This mode allows step by step utilization, and permits to reduce system power consumption by bringing the clock frequency down to any value. At 0 MHz, the power consumption is the same as in the Power Down Mode.

I/O Ports

The I/O drives for P1, P2, P3 of the 83C154 are impedance programmable. The I/O buffers for Ports 1, 2 and 3 are implemented as shown in *figure 4*.

When the port latch contains 0, all pFETS in figure 4 are off while the nFET is turned on. When the port latch makes a 0-to-1 transition, the nFET turns off. The strong pullup pFET, T1, turns on for two oscillator periods, pulling the output high very rapidly. As the output line is drawn high, pFET T3 turns on through the inverter to supply the IOH source current. This inverter and T3 form a latch which holds the 1 and is supported by T2. When Port 2 is used as an address port, for access to external program of data memory, any address bit that contains a 1 will have his strong pullup turned on for the entire duration of the external memory access.

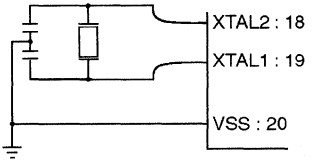
When an I/O pin on Ports 1, 2, or 3 is used as an input, the user should be aware that the external circuit must sink current during the logical 1-to-0 transition. The maximum sink current is specified as ITL under the D.C. Specifications. When the input goes below approximately 2 V, T3 turns off to save ICC current. Note, when returning to a logical 1, T2 is the only internal pullup that is on. This will result in a slow rise time if the user's circuit does not force the input line high.

The input impedance of Port 1, 2, 2 are programmable through the register IOCON. The ALF bit (IOCON0) set all of the Port 1, 2, 3 floating when a Power Down mode occurs. The P1HZ, P2HZ, P3HZ bits (IOCON1, IOCON2, IOCON3) set respectively the Ports P1, P2, P3 in floating state. The IZC (IOCON4) allows to choose input impedance of all ports (P1, P2, P3). When IZC = 0, T2 and T3 pullup of I/O ports are active ; the internal input impedance is approximately 10 K. When IZC = 1 only T2 pull-up is active. The T3 pull-up is turned off by IZC. The internal impedance is approximately 100 K.

Oscillator Characteristics

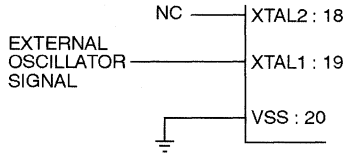
XTAL1 and XTAL2 are the input and output respectively, of an inverting amplifier which is configured for use as an on-chip oscillator, as shown in figure 5. Either a quartz crystal or ceramic resonator may be used.

Figure 5. Crystal Oscillator.



To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in *figure 6*. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

Figure 6. External Drive Configuration.



Hardware Description

Same as for the 80C51, plus a third timer/counter :

Timer/Event Counter 2

Timer 2 is a 16 bit timer/counter like Timers 0 and 1, it can operate either as a timer or as an event counter. This is selected by bit C/$\overline{T2}$ in the Special Function Register T2CON (Figure 1). It has three operating modes : "capture", "autoload" and "baud rate generator", which are selected by bits in T2CON as shown in *Table 2*.

Table 2.Timer 2 Operating Modes.

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16 bit auto-reload
0	1	1	16 bit capture
1	X	1	baud rate generator
X	X	0	(off)

In the capture mode there are two options which are selected by bit EXEN2 in T2CON; If EXEN2 = 0, then Timer 2 is a 16 bit timer or counter which upon overflowing sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt.

The capture mode is illustrated in *Figure 7*.

In the auto-reload mode there are again two options, which are selected by bit EXEN2 in T2CON.If EXEN2 = 0, then when Timer 2 rolls over it does not only set TF2 but also causes the Timer 2 register to be reloaded with the 16 bit value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16 bit reload and set EXF2.

The auto-reload mode is illustrated in *Figure 8*.

Figure 7. Timer 2 in Capture Mode.

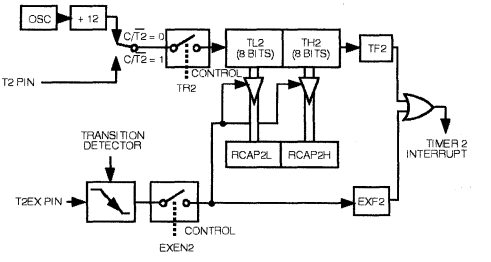
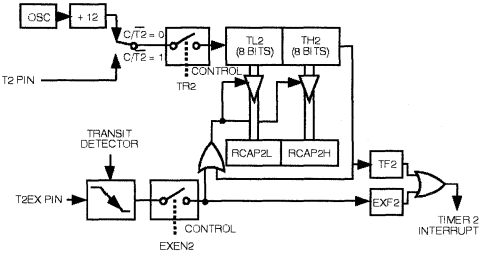


Figure 8. Timer 2 in Auto-Reload Mode.



(MSB) (LSB)

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

The baud rate generator mode is selected by : RCLK = 1 and/or TCLK = 1.

Symbol	Position	Name and Significance
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 OR TCLK = 1.
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/$\overline{T2}$	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered).
CP/$\overline{RL2}$	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN 2 = 1. When cleared, auto reloads will occur either with Timer 2 overflows or negative transition at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Timer Functions

In fact, timer 0 & 1 can be connected by a software instruction to implement a 32 bit timer function. Timer 0 (mode 3) or timer 1 (mode 0, 1, 2) or a 32 bit timer consisting of timer 0 + timer 1 can be employed in the watchdog mode, in which case a CPU reset is generated upon a TF1 flag.

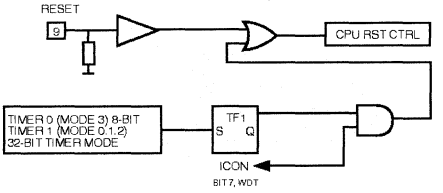
The internal pull-up resistances at ports 1~3 can be set to a ten times increased value simply by software.

32 Bit Mode and Watching Mode

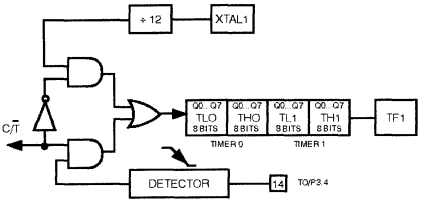
The 83C154 has two supplementary modes. They are accessed by bits WDT and T32 of register IOCON. Figure 10 showns how IOCON must be programmed in order to have access to these functions

Figure 9.

Watchdog timer



32 bit timer [IOCON bit 6 (T32) = 1]



(MSB) (LSB)

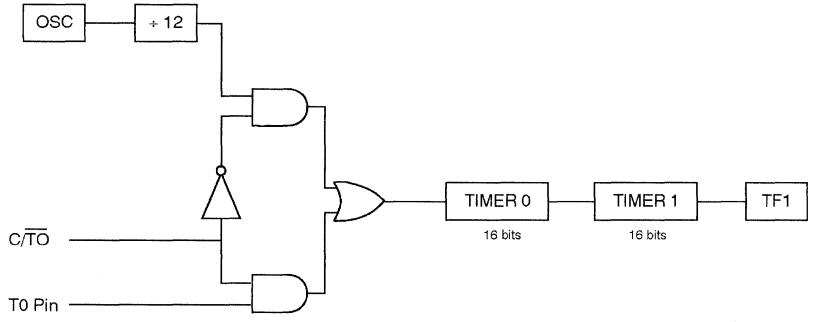
WDT	T32	SERR	IZC	P3HZ	P2HZ	P1HZ	ALF

Symbol	Position	Name and Significance
T32	IOCON.6	– If T32 = 1 and if C/$\overline{T0}$ = 0, T1 and T0 are programmed as a 32 bit TIMER. – If T32 = 1 and if C/$\overline{T0}$ = 1, T1 and T0 are programmed as a 32 bit COUNTER.
WDT	IOCON.7	– If WDT = 1 and according to the mode selected by TMOD, an 8 bit or 32 bit WATCHDOG is configured from TIMERS 0 and 1.

32 Bit Mode

- T32 = 1 enables access to this mode. As shown in figure 11, this 32 bit mode consists in cascading TIMER 0 for the LSBs and TIMER 1 for the MSBs

Figure 10.32 Bit Timer/counter.



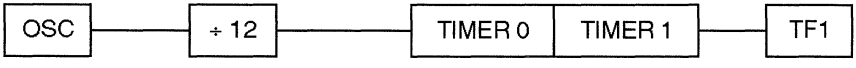
T32 = 1 starts the timer/counter and T32 = 0 stops it.

It should be noted that as soon as T32 = 0. TIMERs 0 and 1 assume the configuration specified by register TMOD. Moreover, if TR0 = 1 or if TR1 = 1, the content of the TIMERs evolves. Consequently, in 32 bit mode, if the TIMER/COUNTER muste be stopped (T32 = 0), TR0 and TR1 must be set to 0.

32 Bit Timer

- Figure 12 illustrates the 32 bit TIMER mode.

Figure 11. 32 Bit Timer Configuration.



- In this mode, T32 = 1 and C/$\overline{T0}$ = 0, the 32 bit timer is incremented on each S3P1 state of each machine cycle. An overflow of TIMER 0 (TF0 has not been set to 1) increments TIMER 1 and the overflow of the 32 bit TIMER is signalled by setting TF1 (S5P1) to 1.
- The following formula should be used to calculate the required frequency :

$$f = \frac{OSC}{12 \times (65536 - (T0, T1))}$$

32 Bit Counter

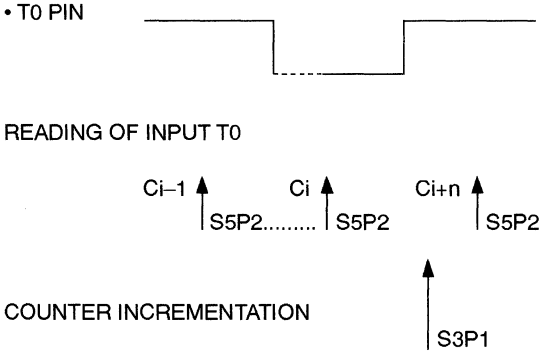
Figure 13 illustrates the 32 bit COUNTER mode.

Figure 12. 32 Bit Counter Configuration.

- In this mode, T32 = 0 and C/$\overline{T0}$ = 1. Before it can make an increment, the 83C154µ must detect two transitions on its T0 input. As shown in figure 14, input T0 is sampled on each S5P2 state of every machine cycle or, in other words, every OSC ÷ 12.

2

Figure 13. Counter Incrementation Condition.



- The counter will only evolve if a level 1 is detected during state S5P2 of cycle Ci and if a level 0 is detected during state S5P2 of cycle Ci + n.
- Consequently, the minimal period of signal fEXT admissible by the counter must be greater than or equal to two machine cycles. The following formula should be used to calculate the operating frequency.

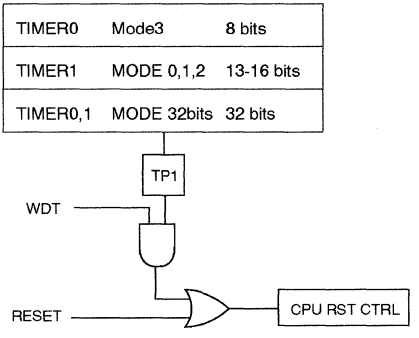
$$f = \frac{fEXT}{65536-(T0,\ T1)}$$

$$fEXT < \frac{OSC}{24}$$

Watchdog Mode

- WDT = 1 enables access to this mode. As shown in figure 15, all the modes of TIMERS 0 and 1, of which the overflows act on TF1 (TF1 = 1), activate the WATCHDOG Mode.

Figure 14. The Different Watchdog Configurations.



- If C/$\overline{T}$ = 0, the WATCHDOG is a TIMER that is incremented every machine cycle. If C/$\overline{T}$ = 1, the WATCHDOG is a counter that is incremented by an external signal of which the frequency cannot exceed OSC ÷ 24.
- The overflow of the TIMER/COUNTER is signalled by raising flag TF1 to 1. The reset of the 83C154 is executed during the next machine cycle and lasts for the next 5 machine cycles. The results of this reset are identical to those of a hardware reset. The internal RAM is not affected and the special register assume the values shown in Table 3.

Table 3. Content of the SFRS after a reset triggered by the watchdog.

REGISTER	CONTENT
PC	000H
ACC	00H
B	00H
PSW	00H
SP	07H
DPTR	0000H
P0-P3	0FFH
IP	0X000000B
IE	0X000000B
TMOD	00H
TCON	00H
T2CON	00H
TH0	00H
TL0	00H
TH1	00H
TL1	00H
TH2	00H
TL2	00H
RCAP2H	00H
RCAP2L	00H
SCON	00H
SBUF	Indeterminate
IOCON	00H
PCON	000X0000B

- As there are no precautions for protecting bit WDT from spurious writing in the IOCON register, special care must be taken when writing the program. In particular, the user should use the IOCON register bit handling instructions :
  - SETB and CLR x
    in preference to the byte handling instructions :
  - MOV IOCON, # XXH, ORL IOCON, #XXH,
  - ANL IOCON, #XXH

External Counting in Power-down Mode (PD = PCON.1 = 1)

- In the power-down mode, the oscillator is turned off and the 83C154's activity is frozen. However, if an external clock is connected to one of the two inputs, T1/T0, TIMER/COUNTERS 0 and 1 can continue to operate.
  In this case, counting becomes asychronous and the maximum, admissible frequency of the signal is OSC : 24.
- The overflow of either counter TF0 or TF1 causes an interrupt to be serviced or forces a reset if the counter is in the WATCHDOG MODE (T32 = ICON.7 = 1).

83C154 with Secret ROM

TEMIC offers 83C154 with the encrypted secret ROM option to secure the ROM code contained in the 83C154 microcontrollers.

The clear reading of the program contained in the ROM is made impossible due to an encryption through several random keys implemented during the manufacturing process.

The keys used to do such encryption are selected randomwise and are definitely different from one microcontroller to another.

This encryption is activated during the following phases :

- Everytime a byte is addressed during a verify of the ROM content, a byte of the encryption array is selected.
- MOVC instructions executed from external program memory are disabled when fetching code bytes from internal memory.
- EA is sampled and latched on reset, thus all state modification are disabled.

For further information please refer to the application note (ANM053) available upon request.

83C154 with Secret TAG

TEMIC offers special 64-bit identifier called "SECRET TAG" on the microcontroller chip.

The Secret Tag option is available on both ROMless and masked microcontrollers.

The Secret Tag feature allows serialization of each microcontroller for identification of a specific equipment. A unique number per device is implemented in the chip during manufacturing process. The serial number is a 64-bit binary value which is contained and addressable in the Special Function Registers (SFR) area.

This Secret Tag option can be read-out by a software routine and thus enables the user to do an individual identity check per device. This routine is implemented inside the microcontroller ROM memory in case of masked version which can be kept secret (and then the value of the Secret Tag also) by using a ROM Encryption.

For further information, please refer to the application note (ANM031) available upon request.

Electrical Characteristics

Absolute Maximum Ratings*

Ambiant Temperature Under Bias :
C = commercial ..... 0°C to +70°C
I = industrial ..... –40°C to +85°C
Storage Temperature ..... –65°C to + 150°C
Voltage on VCC to VSS ..... –0.5 V to + 7 V
Voltage on Any Pin to VSS ..... –0.5 V to VCC + 0.5 V
Power Dissipation ..... 1 W**
** This value is based on the maximum allowable die temperature and the thermal resistance of the package

**** Notice***

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Parameters

TA = 0°C to 70°C ; Vcc = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 36 MHz
TA = –40°C + 85°C ; Vcc = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 36 MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 Vcc – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 1.4	Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc	Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3)		0.3 0.45 1.0	V V V	IOL = 100 µA IOL = 1.6 mA (note 2) IOL = 3.5 mA
VOL1	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)		0.3 0.45 1.0	V V V	IOL = 200 µA IOL = 3.2 mA (note 2) IOL = 7.0 mA
VOH	Output High Voltage Port 1, 2 and 3	Vcc – 0.3		V	IOH = – 10 µA
		Vcc – 0.7		V	IOH = – 30 µA
		Vcc – 1.5		V	IOH = – 60 µA VCC = 5 V ± 10 %
VOH1	Output High Voltage (Port 0, ALE, $\overline{PSEN}$)	Vcc – 0.3		V	IOH = – 200 µA
		Vcc – 0.7		V	IOH = – 3.2 mA
		Vcc – 1.5		V	IOH = – 7.0 mA VCC = 5 V ± 10 %
IIL	Logical 0 Input Current (Ports 1, 2 and 3)		– 50	µA	Vin = 0.45 V
ILI	Input leakage Current		+/– 10	µA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		– 650	µA	Vin = 2.0 V
IPD	Power Down Current		50	µA	Vcc = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	200	KOhm	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current Freq = 1 MHz Icc op Icc idle Freq = 6 MHz Icc op Icc idle Freq ≥ 12 MHz Icc op = 1.3 Freq (MHz) + 4.5 mA Icc idle = 0.36 Freq (MHz) + 2.7 mA		 1.8 1 10 4	 mA mA mA mA	Vcc = 5.5 V

Absolute Maximum Ratings*

Ambient Temperature Under Bias :
A = Automotive ..... –40°C to +125°C
Storage Temperature ..... –65°C to + 150°C
Voltage on VCC to VSS ..... –0.5 V to + 7 V
Voltage on Any Pin to VSS ..... –0.5 V to VCC + 0.5 V
Power Dissipation ..... 1 W
** This value is based on the maximum allowable die temperature and the thermal resistance of the package

* *Notice*

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2

DC Parameters

TA = –40°C + 125°C ; Vss = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 36 MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 Vcc – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 1.4	Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc	Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3)		0.3 0.45 1.0	V	IOL = 100 µA IOL = 1.6 mA (note 2) IOL = 3.5 mA
VOL1	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)		0.3 0.45 1.0	V	IOL = 200 µA IOL = 3.2 mA (note 2) IOL = 7.0 mA
VOH	Output High Voltage Port 1, 2 and 3	Vcc – 0.3		V	IOH = – 10 µA
		Vcc – 0.7		V	IOH = – 30 µA
		Vcc – 1.5		V	IOH = – 60 µA VCC = 5 V ± 10 %
VOH1	Output High Voltage (Port 0, ALE, $\overline{PSEN}$)	Vcc – 0.3		V	IOH = – 200 µA
		Vcc – 0.7		V	IOH = – 3.2 mA
		Vcc – 1.5		V	IOH = – 7.0 mA VCC = 5 V ± 10 %
IIL	Logical 0 Input Current (Ports 1, 2 and 3)		– 50	µA	Vin = 0.45 V
ILI	Input leakage Current		±10	µA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		– 750	µA	Vin = 2.0 V
IPD	Power Down Current		75	µA	Vcc = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	200	KOhm	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current Freq = 1 MHz Icc op Icc idle Freq = 6 MHz Icc op Icc idle Freq ≥ 12 MHz Icc op = 1.3 Freq (MHz) + 4.5 mA Icc idle = 0.36 Freq (MHz) + 2.7 mA		 1.8 1 10 4	 mA mA mA mA	Vcc = 5.5 V

Absolute Maximum Ratings*

Ambient Temperature Under Bias :

M = Military ..... –55°C to +125°C

Storage Temperature ..... –65°C to + 150°C

Voltage on VCC to VSS ..... –0.5 V to + 7 V

Voltage on Any Pin to VSS ..... –0.5 V to VCC + 0.5 V

Power Dissipation ..... 1 W

** This value is based on the maximum allowable die temperature and the thermal resistance of the package

Notice

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Parameters

TA = –55°C + 125°C ; Vss = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 36 MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 Vcc – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 1.4	Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc	Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3)		0.45	V	IOL = 1.6 mA (note 2)
VOL1	Output Low Voltage (Port 0, ALE, PSEN)		0.45	V	IOL = 3.2 mA (note 2)
VOH	Output High Voltage (Port 1, 2, 3)	2.4		V	IOH = – 60 µA Vcc = 5 V ± 10 %
		0.75 Vcc		V	IOH = – 25 µA
		0.9 Vcc		V	IOH = – 10 µA
VOH1	Output High Voltage (Port 0 in External Bus Mode, ALE, PEN)	2.4		V	IOH = – 400 µA Vcc = 5 V ± 10 %
		0.75 Vcc		V	IOH = – 150 µA
		0.9 Vcc		V	IOH = – 40 µA
IIL	Logical 0 Input Current (Ports 1, 2 and 3)		– 75	µA	Vin = 0.45 V
ILI	Input leakage Current		±10	µA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		– 750	µA	Vin = 2.0 V
IPD	Power Down Current		75	µA	Vcc = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	200	KOhm	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current Freq = 1 MHz Icc op Icc idle Freq = 6 MHz Icc op Icc idle Freq ≥ 12 MHz Icc op = 1.3 Freq (MHz) + 4.5 mA Icc idle = 0.36 Freq (MHz) + 2.7 mA		 1.8 1 10 4	 mA mA mA mA	Vcc = 5.5 V

Absolute Maximum Ratings*

Ambient Temperature Under Bias :
C = Commercial ..... 0°C to +70°C
I = Industrial ..... –40°C to 85°C
Storage Temperature ..... –65°C to + 150°C
Voltage on VCC to VSS ..... –0.5 V to + 7 V
Voltage on Any Pin to VSS ..... –0.5 V to VCC + 0.5 V
Power Dissipation ..... 1 W
** This value is based on the maximum allowable die temperature and the thermal resistance of the package

** Notice*

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2

DC Parameters

TA = 0°C to 70°C ; Vcc = 2.7 V to 5.5 V ; Vss = 0 V ; F = 0 to 16 MHz
TA = –40°C to 85°C ; Vcc = 2.7 V to 5.5 V

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 VCC – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 VCC + 1.4 V	VCC + 0.5	V	
VIH1	Input High Voltage to XTAL1	0.7 VCC	VCC + 0.5	V	
VIH2	Input High Voltage to RST for Reset	0.7 VCC	VCC + 0.5	V	
VPD	Power Down Voltage to Vcc in PD Mode	2.0	6.0	V	
VOL	Output Low Voltage (Ports 1, 2, 3)		0.45	V	IOL = 0.8 mA (note 2)
VOL1	Output Low Voltage Port 0, ALE, $\overline{PSEN}$		0.45	V	IOL = 1.6 mA (note 2)
VOH	Output High Voltage Ports 1, 2, 3	0.9 Vcc		V	IOH = – 10 µA
VOH1	Output High Voltage (Port 0 in External Bus Mode), ALE, $\overline{PSEN}$	0.9 Vcc		V	IOH = – 40 µA
IIL	Logical 0 Input Current Ports 1, 2, 3		– 50	µA	Vin = 0.45 V
ILI	Input Leakage Current		± 10	µA	0.45 < Vin < VCC
ITL	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		– 650	µA	Vin = 2.0 V
IPD	Power Down Current		50	µA	VCC = 2 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	200	kΩ	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, T_A = 25°C

Maximum Icc (mA)

	OPERATING (NOTE 1)				IDLE (NOTE 1)			
FREQUENCY/Vcc	2.7 V	3 V	3.3 V	5.5 V	2.7 V	3 V	3.3 V	5.5 V
1 MHz	0.8 mA	1 mA	1.1 mA	1.8 mA	400 µA	500 µA	600 µA	1 mA
6 MHz	4 mA	5 mA	6 mA	10 mA	1.5 mA	1.7 mA	2 mA	4 mA
12 MHz	8 mA	10 mA	12 mA		2.5 mA	3 mA	3.5 mA	
16 MHz	10 mA	12 mA	14 mA		3 mA	3.8 mA	4.5 mA	
Freq > 12 MHz (Vcc = 5.5 V)	Icc (mA) = 1.3 × Freq (MHz) + 4.5 Icc Idle (mA) = 0.36 × Freq (MHz) + 2.7							

Note 1 : ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + .5 V, VIH = VCC –.5 V ; XTAL2 N.C. ; EA = RST = Port 0 = VCC. ICC would be slighty higher if a crystal oscillator used.

Idle ICC is measured with all otput pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + 5 V, VIH = VCC -.5 V ; XTAL2 N.C ; Port 0 = VCC ; EA = RST = VSS.

Power Down ICC is measured with all output pins disconnected ; EA = PORT 0 = VCC ; XTAL2 N.C. ; RST = VSS.

Note 2 : Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLS of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operations. In the worst cases (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45 V may exceed 0,45 V with maxi VOL peak 0.6 V A Schmitt Trigger use is not necessary.

Figure 15. ICC Test Condition, Idle Mode. All other pins are disconnected.

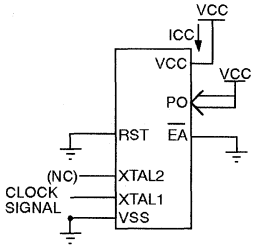


Figure 16. ICC Test Condition, Active Mode. All other pins are disconnected.

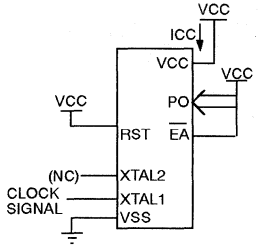


Figure 17. ICC Test Condition, Power Down Mode. All other pins are disconnected.

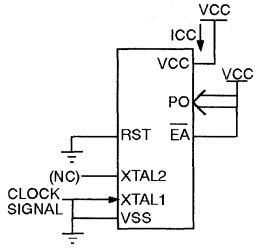
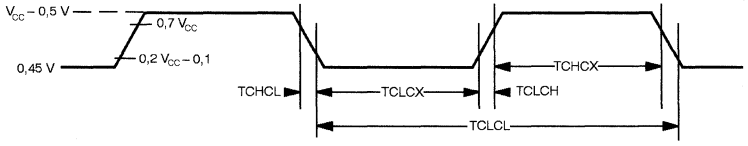


Figure 18. Clock Signal Waveform for ICC Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.



Explanation of the AC Symbol

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example :

TAVLL = Time for Address Valid to ALE low.

TLLPL = Time for ALE low to $\overline{\text{PSEN}}$ low.

A : Address.
C : Clock.
D : Input data.
H : Logic level HIGH
I : Instruction (program memory contents).
L : Logic level LOW, or ALE.
P : PSEN.
Q : Output data.
R : READ signal.
T : Time.
V : Valid.
W : WRITE signal.
X : No longer a valid logic level.
Z : Float.

2

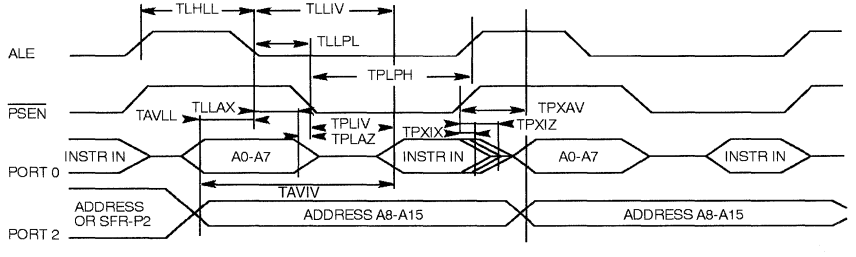
AC Parameters

TA = 0 to + 70°C ; Vss = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 36 MHz
TA = –55° + 125°C ; Vss = 0 V ; 2.7 V < Vcc < 5.5 V ; F = 0 to 16 MHz
TA = –55° + 125°C ; Vss = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 36 MHz
(Load Capacitance for PORT 0, ALE and PSEN = 100 pF ; Load Capacitance for all other outputs = 80 pF)

External Program Memory Characteristics

		16 MHz		20 MHz		25 MHz		30 MHz		36 MHz	
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**
TLHLL	ALE Pulse Width	110		90		70		60		50	
TAVLL	Address valid to ALE	40		30		20		15		10	
TLLAX	Address Hold After ALE	35		35		35		35		35	
TLLIV	ALE to valid instr in		185		170		130		100		80
TLLPL	ALE to PSEN	45		40		30		25		20	
TPLPH	PSEN pulse Width	165		130		100		80		75	
TPLIV	PSEN to valid instr in		125		110		85		65		50
TPXIX	Input instr Hold After PSEN	0		0		0		0		0	
TPXIZ	Input instr Float After PSEN		50		45		35		30		25
TPXAV	PSEN to Address Valid	55		50		40		35		30	
TAVIV	Address to Valid instr in		230		210		170		130		90
TPLAZ	PSEN low to Address Float		10		10		8		6		5

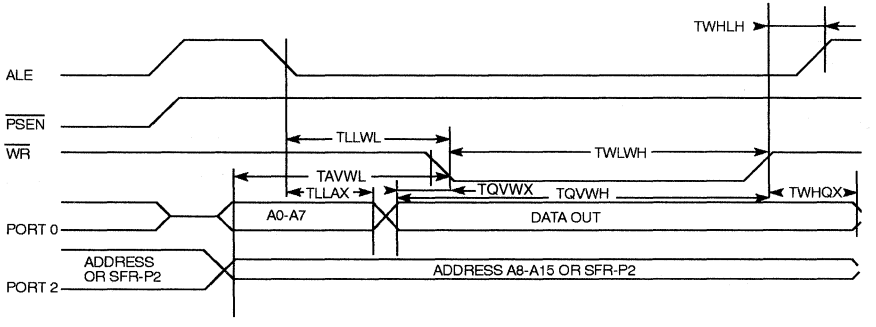
External Program Memory Read Cycle



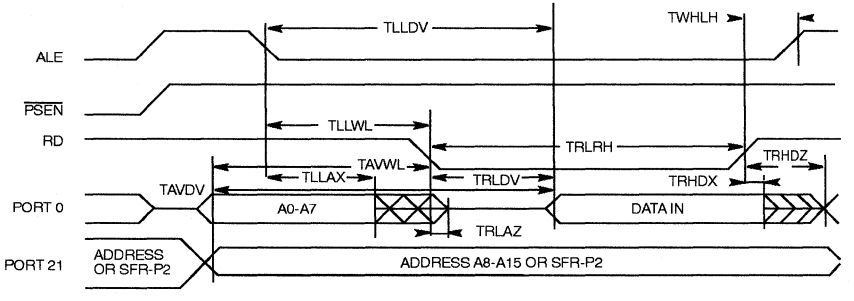
External Data Memory Characteristics

		16 MHz		20 MHz		25 MHz		30 MHz		36 MHz	
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
TRLRH	RD pulse Width	340		270		210		180		120	
TWLWH	WR pulse Width	340		270		210		180		120	
TLLAX	Address Hold After ALE	85		85		70		55		35	
TRLDV	RD to Valid in		240		210		175		135		110
TRHDX	Data hold after RD	0		0		0		0		0	
TRHDZ	Data float after RD		90		90		80		70		50
TLLDV	ALE to Valid Data In		435		370		350		235		170
TAVDV	Address to Valid Data IN		480		400		300		260		190
TLLWL	ALE to WR or RD	150	250	135	170	120	130	90	115	70	100
TAVWL	Address to WR or RD	180		180		140		115		75	
TQVWX	Data valid to WR transition	35		35		30		20		15	
TQVWH	Data Setup to WR transition	380		325		250		215		170	
TWHQX	Data Hold after WR	40		35		30		20		15	
TRLAZ	RD low to Address Float		0		0		0		0		0
TWHLH	RD or WR high to ALE high	35	90	35	60	25	45	20	40	20	40

External Data Memory Write Cycle



External Data Memory Read Cycle

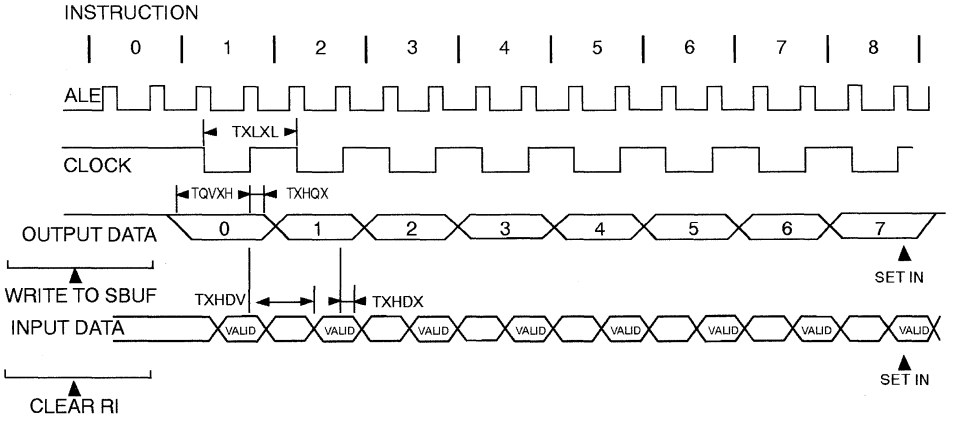


Serial Port Timing – Shift Register Mode

		16 MHz		20 MHz		25 MHz		30 MHz		36 MHz	
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
TXLXL	Serial Port Clock Cycle Time	750		600		480		400		330	
TQVXH	Output Data Setup to Clock Rising Edge	563		480		380		300		220	
TXHQX	Output Data Hold after Clock Rising Edge	63		90		65		50		45	
TXHDX	Input Data Hold after Clock Rising Edge	0		0		0		0		0	
TXHDV	Clock Rising Edge to Input Data Valid		563		450		350		300		250

2

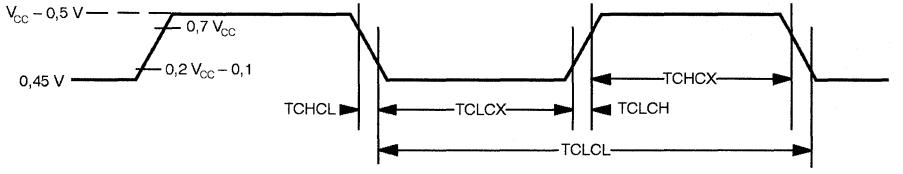
Shift Register Timing Waveforms



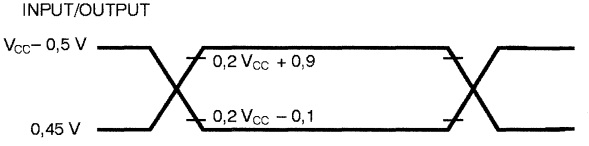
External Clock Drive Characteristics (XTAL1)

SYMBOL	PARAMETER	MIN	MAX	UNIT
FCLCL	Oscillator Frequency		36	MHz
TCLCL	Oscillator period	27.8		ns
TCHCX	High Time	5		ns
TCLCX	Low Time	5		ns
TCLCH	Rise Time		5	ns
TCHCL	Fall Time		5	ns

External Clock Drive Waveforms

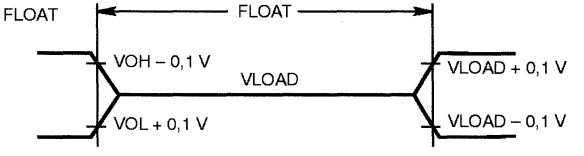


AC Testing Input/Output Waveforms



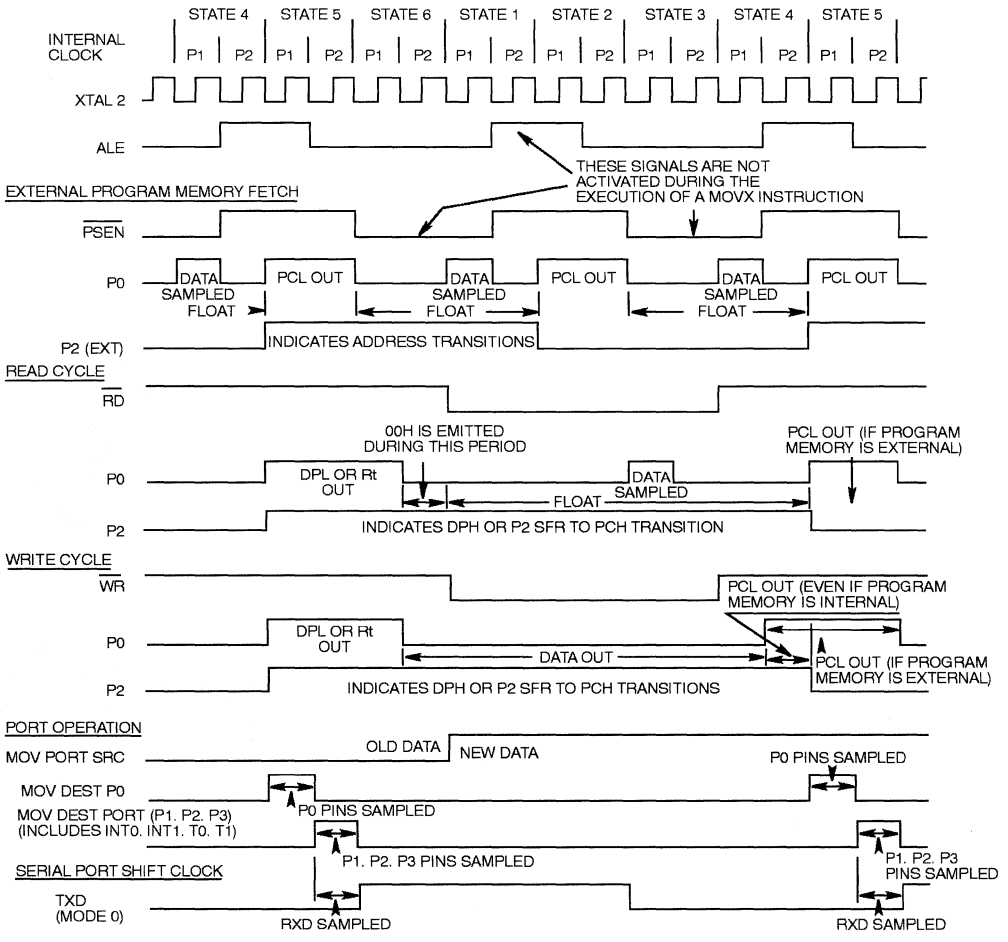
AC inputs during testing are driven at Vcc – 0.5 for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at VIH min for a logic "1" and VIL max for a logic "0".

Float Waveforms



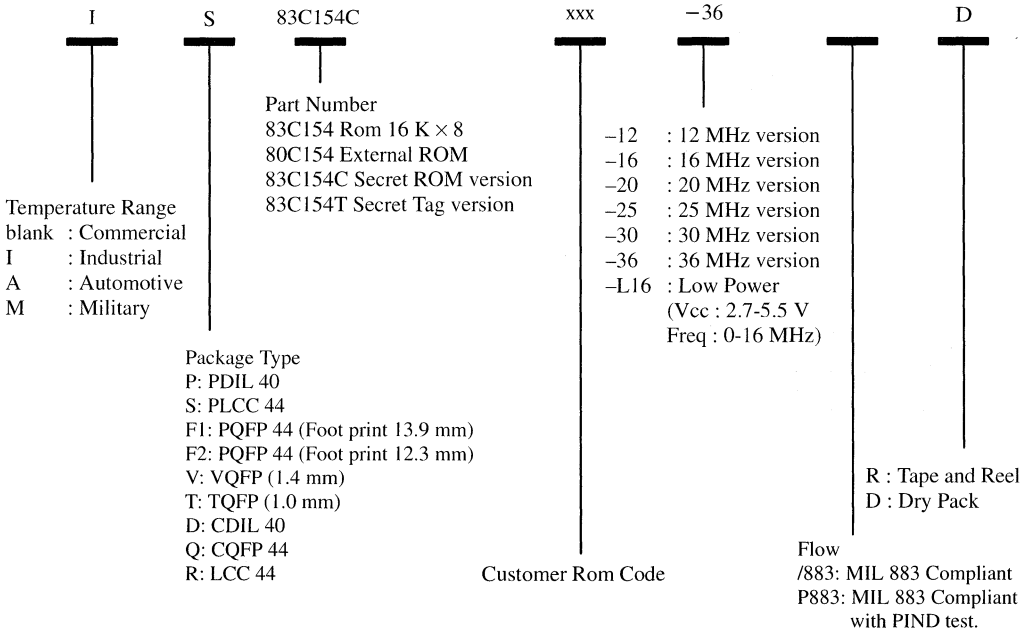
For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded VOH/VOL level occurs. Iol/IoH ≥ ± 20 mA.

Clock Waveforms



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A = 25°C fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

Ordering Information



CMOS 0 to 30 MHz Single Chip 8–bit Microcontroller

Description

The TEMIC 83C154D retains all the features of the TEMIC 80C52 with extended ROM capacity (32 K bytes), 256 bytes of RAM, 32 I/O lines, a 6-source 2-level interrupts, a full duplex serial port, an on-chip oscillator and clock circuits, three 16 bit timers with extra features : 32 bit timer and watch dog functions. Timer 0 and 1 can be configured by program to implement a 32 bit timer. The watchdog function can be activated either with timer 0, or timer 1 or both together (32 bit timer).

In addition, the 83C154D has two software selectable modes of reduced activity for further reduction of power consumption. In the Idle Mode, the CPU is frozen while the RAM is saved, ant the timers, the serial port, and the interrupt system continue to function. In the Power Down Mode, the RAM is saved and the timers, serial port and interrupts continue to function when driven by external clocks. In addition as for the TEMIC 80C51/C52, the stop clock mode is also available.

- 83C154D-12 : 0 to 12 MHz
- 83C154D-16 : 0 to 16 MHz
- 83C154D-20 : 0 to 20 MHz
- 83C154D-25 : 0 to 25 MHz
- 83C154D-30 : 0 to 30 MHz (commercial and industrial only)
- 83C154D-L16 : 0 to 16 MHz with 2,7 V < V_{CC} < 5,5 V (commercial only)

Features

- Power Control Mode
- 256 bytes RAM
- 32 K bytes of ROM
- 32 programmable I/O lines (programmable impedance)
- Three 16 bit timer/counters (including watch dog and 32 bit timer)
- 64 K program memory space
- Fully static design
- 0.8 µ CMOS process
- Boolean processor
- 6 interrupt sources
- Programmable serial port
- 64 K data memory space
- Temperature range : commercial, industrial, automotive, military

Optional

- Secret ROM : Encryption
- Secret TAG : Identification number

Interface

Figure 1. Block Diagram

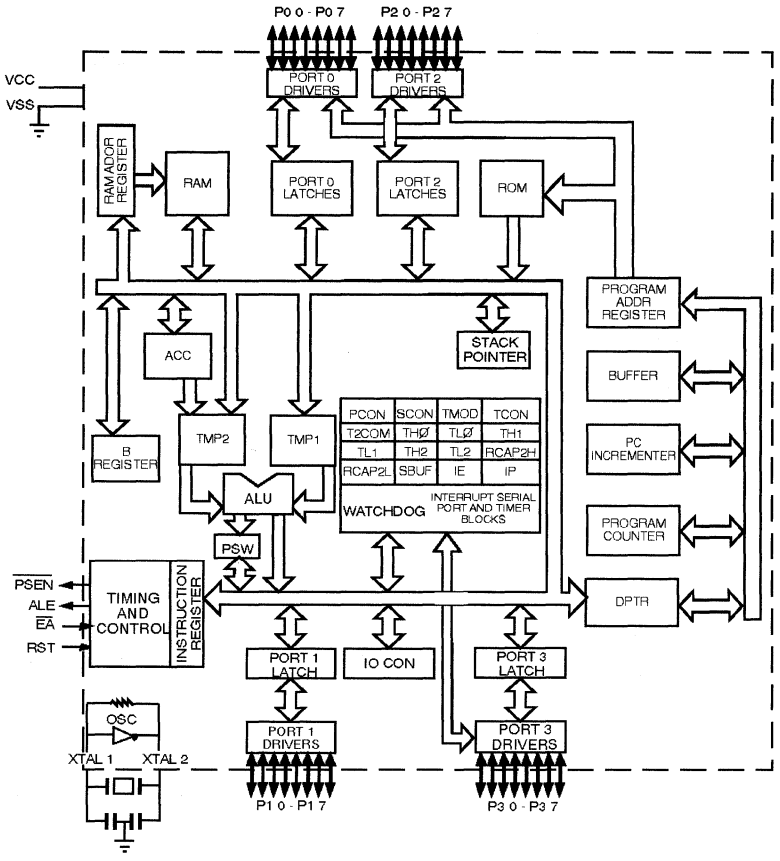
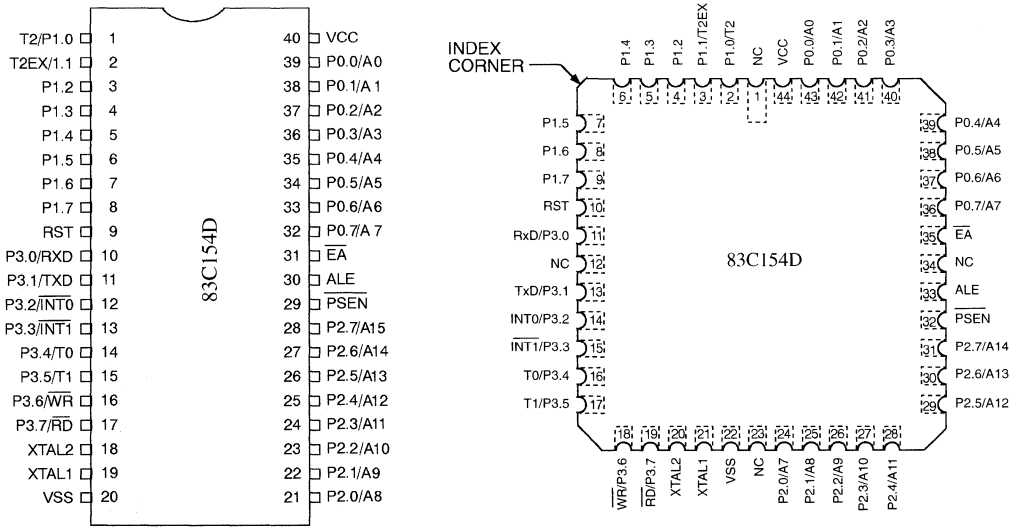
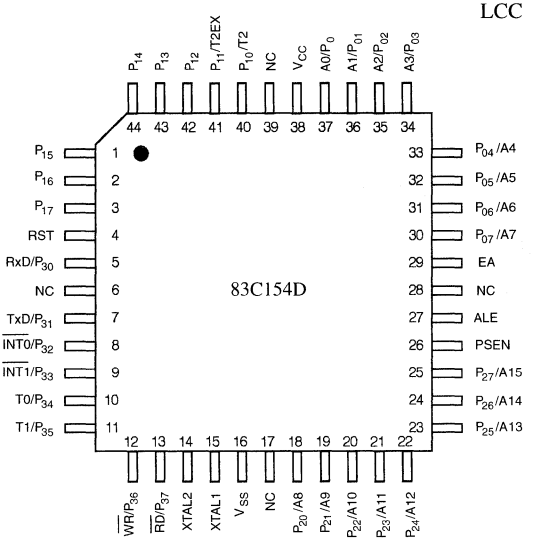


Figure 2. Pin Configuration



DIL LCC



Flat Pack

Diagrams are for reference only. Package sizes are not to scale

Pin Description

Vss

Circuit Ground Potential.

VCC

Supply voltage during normal, Idle, and Power Down operation.

Port 0

Port 0 is an 8 bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's. Port 0 also outputs the code bytes during program verification in the 83C154D. External pullups are required during program verification. Port 0 can sink eight LS TTL inputs.

Port 1

Port 1 is an 8 bit bi-directional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address byte during program verification. In the 83C154D, Port 1 can sink or source three LS TTL inputs. It can drive CMOS inputs without external pullups.

2 inputs of PORT 1 are also used for timer/counter 2 :

P1.0 [T2] : External clock input for timer/counter 2. P1.1 [T2EX] : A trigger input for timer/counter 2, to be reloaded or captured causing the timer/counter 2 interrupt.

Port 2

Port 2 is an 8 bit bi-directional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (ILL, on the data sheet) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16 bit addresses (MOVX @DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that use 8 bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

It also receives the high-order address bits and control signals during program verification in the 83C154. Port 2 can sink or source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Port 3

Port 3 is an 8 bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (ILL, on the data sheet) because of the pullups. It also serves the functions of various special features of the TEMIC 51 Family, as listed below.

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	TD (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external Data Memory write strobe)
P3.7	RD (external Data Memory read strobe)

Port 3 can sink or source three LS TTL inputs. It can drive CMOS inputs without external pullups.

RST

A high level on this for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to VCC. As soon as the reset is applied (Vin), PORT 1, 2 and 3 are tied to 1. This operation is achieved asynchronously even if the oscillator is not start up.

ALE

Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time on ALE pulse is skipped. ALE can sink or source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{\text{PSEN}}$

Program Store Enable output is the read strobe to external Program Memory. PSEN is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory, two activations of PSEN are skipped during each access to external Data Memory). PSEN is not activated during fetches from internal Program Memory. PSEN can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{\text{EA}}$

When EA is held high, the CPU executes out of internal Program Memory (unless the Program Counter exceeds 7 FFFH). When EA is held low, the CPU executes only out of external Program Memory. EA must not be floated.

XTAL1

Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

XTAL2

Output of the inverting amplifier that forms the oscillator. This pin should be floated when an external oscillator is used.

2

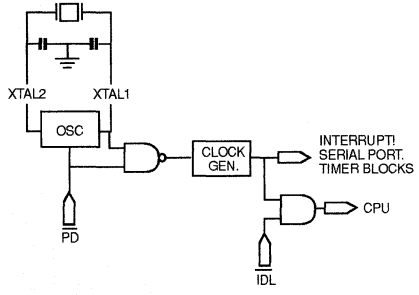
Idle And Power Down Operation

Figure 3 shows the internal Idle and Power Down clock configuration.

As illustrated, Power Down operation stops the oscillator. The interrupt, serial port, and timer blocks continue to function only with external clock (INT0, INT1, T0, T1).

Idle Mode operation allows the interrupt, serial port, and timer blocks to continue to function with internal or external clocks, while the clock to CPU is gated off. The special modes are activated by software via the Special Function Register, PCON. Its hardware address is 87H. PCON is not bit addressable.

Figure 3. Idle and Power Down Hardware.



PCON : Power Control Register

(MSB) (LSB)

SMOD	HPD	RPD	–	GF1	GF0	PD	IDL

Symbol	Position	Name and Function
SMOD	PCON.7	Double Baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2 or 3.
HPD	PCON.6	Hard power Down bit. Setting this bit allows CPU to enter in Power Down state on an external event (1 to 0 transition) on bit T1 (p. 3.5) the CPU quit the Hard Power Down mode when bit T1 (p. 3.5) goes high or when reset is activated.
RPD	PCON.5	Recover from Idle or Power Down bit. When 0 RPD has no effect. When 1, RPD permits to exit from idle or Power Down with any non enabled interrupt source (except timer 2). In this case the program start at the next address. When interrupt is enabled, the appropriate interrupt routine is serviced.
–	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Idle mode bit. Setting this bit activates power down operation.

If 1's are written to PD and IDL at the same time. PD takes, precedence. The reset value of PCON is (000X0000).

Idle Mode

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety : the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during idle. In the idle mode, the internal clock signal is gated off to the CPU, but interrupt, timer and serial port functions are maintained. Table 1 describes the status of the external pins during Idle mode.

There are three ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

The third way to terminate the Idle mode is the activation of any disabled interrupt when recover is programmed (RPD = 1). This will cause PCON.0 to be cleared. No interrupt is serviced. The next instruction is executed. If interrupt are disabled and RPD = 0, only a reset can cancel the Idle mode.

Power Down Mode

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register is saved during power down mode. The three ways to terminate the Power Down mode are the same than the Idle Mode. But since the onchip oscillator is stopped, the external interrupts, timers and serial port must be sourced by external clocks only, via INT0, INT1, T0, T1.

In the Power Down mode, V_{CC} may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the power down mode is entered, and that the voltage is restored before the hardware reset is applied which frees the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

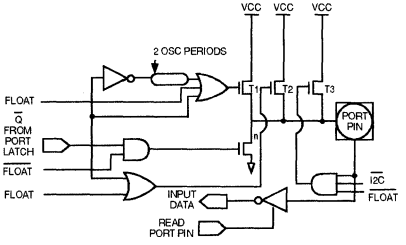
When using voltage reduction : interrupt, timers and serial port functions are guaranteed in the V_{CC} specification limits.

Table 1 describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the port switches from 0 to 1, the port pin is held high during the power down mode by the strong pullup, T1, shown in figure 4.

Table 1.Status of the external pins during idle and power down modes.

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Figure 4.I/O Buffers in the 83C154D (Ports 1, 2, 3).



Stop Clock Mode

Due to static design, the TEMIC 83C154D clock speed can be reduced until 0 MHz without any data loss in memory or registers. This mode allows step by step utilization, and permits to reduce system power consumption by bringing the clock frequency down to any value. At 0 MHz, the power consumption is the same as in the Power Down Mode.

I/O Ports

The I/O drives for P1, P2, P3 of the 83C154D are impedance programmable. The I/O buffers for Ports 1, 2 and 3 are implemented as shown in *figure 4*.

When the port latch contains 0, all pFETS in figure 4 are off while the nFET is turned on. When the port latch makes a 0-to-1 transition, the nFET turns off. The strong pullup pFET, T1, turns on for two oscillator periods, pulling the output high very rapidly. As the output line is drawn high, pFET T3 turns on through the inverter to supply the I_{OH} source current. This inverter and T3 form a latch which holds the 1 and is supported by T2. When Port 2 is used as an address port, for access to external program of data memory, any address bit that contains a 1 will have his strong pullup turned on for the entire duration of the external memory access.

When an I/O pin on Ports 1, 2, or 3 is used as an input, the user should be aware that the external circuit must sink current during the logical 1-to-0 transition. The maximum sink current is specified as ITL under the D.C. Specifications. When the input goes below approximately 2 V, T3 turns off to save ICC current. Note, when returning to a logical 1, T2 is the only internal pullup that is on. This will result in a slow rise time if the user's circuit does not force the input line high.

The input impedance of Port 1, 2, 3 are programmable through the register IOCON. The ALF bit (IOCON0) set all of the Port 1, 2, 3 floating when a Power Down mode occurs. The P1HZ, P2HZ, P3HZ bits (IOCON1, IOCON2, IOCON3) set respectively the Ports P1, P2, P3 in floating state. The IZC (IOCON4) allows to choose input impedance of all ports (P1, P2, P3). When IZC = 0, T2 and T3 pullup of I/O ports are active ; the internal input impedance is approximately 10 K. When IZC = 1 only T2 pull-up is active. The T3 pull-up is turned off by IZC. The internal impedance is approximately 100 K.

Oscillator Characteristics

XTAL1 and XTAL2 are the input and output respectively, of an inverting amplifier which is configured for use as an on-chip oscillator, as shown in *figure 5*. Either a quartz crystal or ceramic resonator may be used.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in *figure 6*. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

Figure 5. Crystal Oscillator.

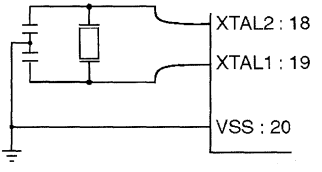
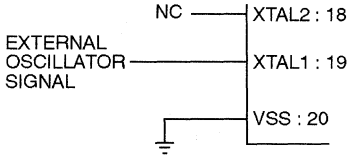


Figure 6. External Drive Configuration.



Hardware Description

Same as for the 80C51 except for the following :

Timer/Event Counter 2

Timer 2 is a 16 bit timer/counter like Timers 0 and 1, it can operate either as a timer or as an event counter. This is selected by bit C/$\overline{T2}$ in the Special Function Register T2CON (Figure 1). It has three operating modes : "capture", "autoload", and "baud rate generator", which are selected by bits in T2CON as shown in *Table 2*.

Table 2. Timer 2 Operating Modes.

RCLK + TCLK	CP/$\overline{RL2}$	TR2	MODE
0	0	1	16 bit auto-reload
0	1	1	16 bit capture
1	X	1	baud capture generator
X	X	0	(off)

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then Timer 2 is a 16 bit timer or counter which upon overflowing sets bit TF2, the Timer 2 overflow bit, which can be used to generate an interrupt. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 ans TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt.
The capture mode is illustrated in *Figure 7*.

In the auto-reload mode there are again two options, which are selected by bit EXEN2 in T2CON. If EXEN2 = 0, then when Timer 2 rolls over it not only sets TF2 but also causes the Timer 2 registers to be reloaded with the 16 bit-value in registers RCAP2L and RCAP2H, which are preset by software. If EXEN2 = 1, then Timer 2 still does the above, but with the added feature that a 1-to-0 transition at external input T2EX will also trigger the 16 bit reload and set EXF2.
The auto-reload mode is illustrated in *Figure 8*.

Figure 7. Timer 2 in Capture Mode.

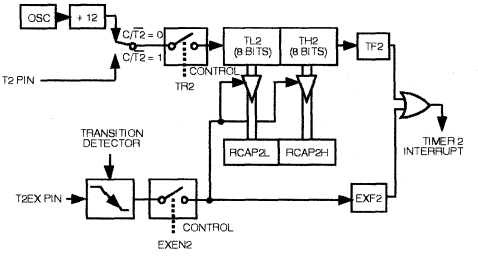
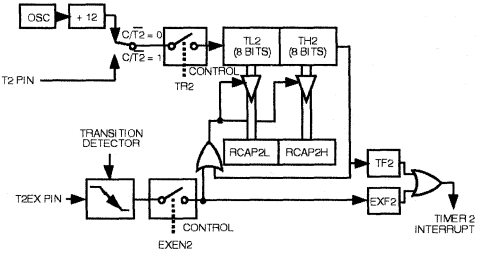


Figure 8. Timer in Auto-Reload Mode.



(MSB) (LSB)

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

The baud rate generator mode is selected by : RCLK = 1 and/or TCLK = 1.

Symbol	Position	Name and Significance
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK = 1 OR TCLK = 1.
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
C/$\overline{T2}$	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered).
CP/$\overline{RL2}$	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN 2 = 1. When cleared, auto reloads will occur either with Timer 2 overflows or negative transition at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

Timers Functions

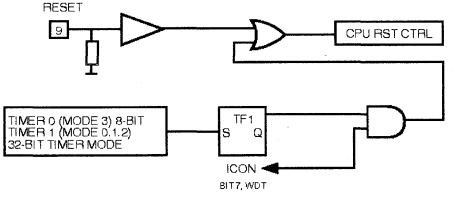
In fact, timer 0 α 1 can be connected by a software instruction to implement a 32 bit timer function. Timer 0 (mode 3) or timer 1 (mode 0, 1, 2) or a 32 bit timer consisting of timer 0 + timer 1 can be employed in the watchdog mode, in which case a CPU reset is generated upon a TF1 flag.

The internal pull-up resistances at ports 1_3 can be set to a ten times increased value simply by software.

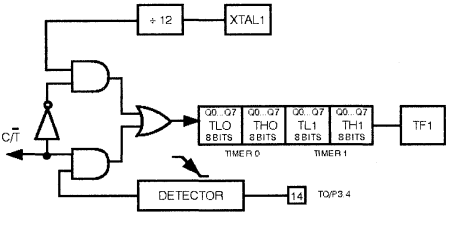
32 Bit Mode and Watching Mode

- The 83C154D has two supplementary modes. They are accessed by bits WDT and T32 of register IOCON. Figure 9 showns how IOCON must be programmed in order to have access to these functions.

Watchdog timer



32 bit timer [IOCON bit 6 (T32) = 1]



(MSB) (LSB)

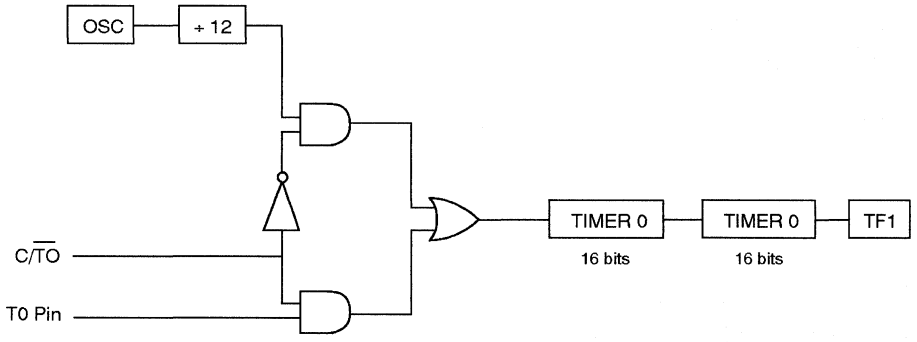
WDT	T32	SERR	IZC	P3HZ	P2HZ	P1HZ	ALF

Symbol	Position	Function
T32	IOCON.6	– If T32 = 1 and if C/T0 = 0, T1 and T0 are programmed as a 32 bit TIMER. – If T32 = 1 and if C/T0 = 1, T1 and T0 are programmed as a 32 bit COUNTER.
WDT	IOCON.7	– If WDT = 1 and according to the mode selected by TMOD, an 8 bit or 32 bit WATCHDOG is configured from TIMERS 0 and 1.

32 Bit Mode

- T32 = 1 enables access to this mode. As shown in figure 10, this 32 bit mode consists in cascading TIMER 0 for the LSBs and TIMER 1 for the MSBs

Figure 9. 32 Bit Timer/Counter.



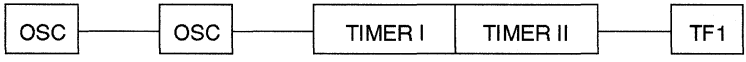
T32 = 1 starts the timer/counter and T32 = 0 stops it.

It should be noted that as soon as T32 = 0. TIMERs 0 and 1 assume the configuration specified by register TMOD. Moreover, if TR0 = 1 or if TR1 = 1, the content of the TIMERs evolves. Consequently, in 32 bit mode, if the TIMER/COUNTER must be stopped (T32 = 0), TR0 and TR1 must be set to 0.

32 Bit Timer

- Figure 11 illustrates the 32 bit TIMER mode.

Figure 10. 32 Bit Timer Configuration.



- In this mode, T32 = 1 and C/$\overline{T0}$ = 0, the 32 bit timer is incremented on each S3P1 state of each machine cycle. An overflow of TIMER 0 (TF0 has not been set to 1) increments TIMER 1 and the overflow of the 32-bit TIMER is signalled by setting TF1 (S5P1) to 1.
- The following formula should be used to calculate the required frequency :

$$f = \frac{OSC}{12 \times (65536 - (T0,\ T1))}$$

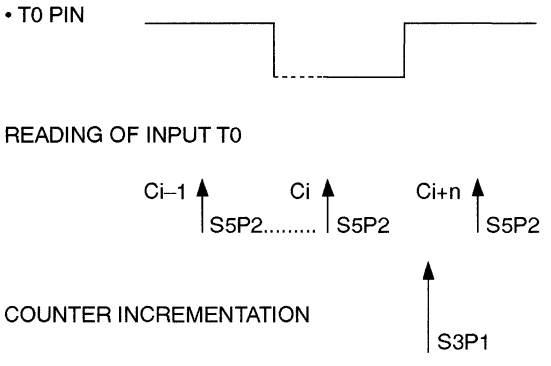
32 Bit Counter

Figure 13 illustrates the 32 bit COUNTER mode.

Figure 11. 32 Bit Counter Configuration.

- In this mode, T32 = 0 and C/$\overline{T0}$ = 1. Before it can make an increment, the 83C154D must detect two transitions on its T0 input. As shown in figure 13, input T0 is sampled on each S5P2 state of every machine cycle or, in other words, every OSC ÷ 12.

Figure 12. Counter Incrementation Condition.



- The counter will only evolve if a level 1 is detected during state S5P2 of cycle Ci and if a level 0 is detected during state S5P2 of cycle Ci + n.
- Consequently, the minimal period of signal fEXT admissible by the counter must be greater than or equal to two machine cycles. The following formula should be used to calculate the operating frequency.

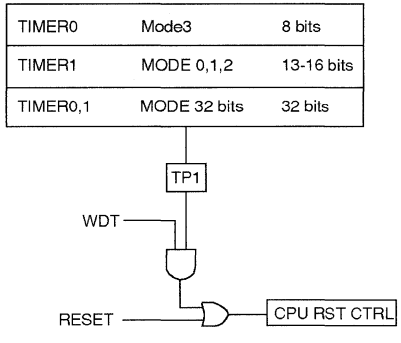
$$f = \frac{fEXT}{65536 - (T0,\ T1)}$$

$$fEXT < \frac{OSC}{24}$$

Watchdog Mode

- WDT = 1 enables access to this mode. As shown in figure 14, all the modes of TIMERs 0 and 1, of which the overflows act on TF1 (TF1 = 1), activate the WATCHDOG Mode.

Figure 13. The Different Watchdog Configurations.



- If C/$\overline{T}$ = 0, the WATCHDOG is a TIMER that is incremented every machine cycle. If C/$\overline{T}$ = 1, the WATCHDOG is a counter that is incremented by an external signal of which the frequency cannot exceed OSC ÷ 24.
- The overflow of the TIMER/COUNTER is signalled by raising flag TF1 to 1. The reset of the 83C154D is executed during the next machine cycle and lasts for the next 5 machine cycles. The results of this reset are identical to those of a hardware reset. The internal RAM is not affected and the special register assume the values shown in Table 3.

Table 3. Content of the SFRS after a reset triggered by the watchdog.

REGISTER	CONTENT
PC	0000H
ACC	00H
B	00H
PSW	00H
SP	00H
DPTR	0000H
P0-P3	0FFH
IP	00H
IE	0X000000B
TMOD	00H
TCON	00H
T2CON	00H
TH0	00H
TL0	00H
TH1	00H
TL1	00H
TH2	00H
TL2	00H
RCAP2H	00H
RCAP2L	00H
SCON	00H
SBUF	Indeterminate
IOCON	00H

- As there are no precautions for protecting bit WDT from spurious writing in the IOCON register, special care must be taken when writing the program. In particular, the user should use the IOCON register bit handling instructions :
  - SETB and CLR x
    in preference to the byte handling instructions :
  - MOV IOCON, # XXH, ORL IOCON, #XXH,
  - ANL IOCON, #XXH, ...

External Counting in Power-down Mode (PD = PCON.1 = 1)

- In the power-down mode, the oscillator is turned off and the 83C154D activity is frozen. However, if an external clock is connected to one of the two inputs, T1/T0, TIMER/COUNTERS 0 and 1 can continue to operate.
  In this case, counting becomes asynchronous and the maximum, admissible frequency of the signal is OSC : 24.
- The overflow of either counter TF0 or TF1 causes an interrupt to be serviced or forces a reset if the counter is in the WATCHDOG MODE (T32 = ICON.7 = 1).

83C154D with Secret ROM

TEMIC offers 83C154D with the encrypted secret ROM option to secure the ROM code contained in the 83C154D microcontrollers.

The clear reading of the program contained in the ROM is made impossible due to an encryption through several random keys implemented during the manufacturing process.

The keys used to do such encryption are selected randomwise and are definitely different from one microcontroller to another.

This encryption is activated during the following phases :

- Everytime a byte is addressed during a verify of the ROM content, a byte of the encryption array is selected.
- MOVC instructions executed from external program memory are disabled when fetching code bytes from internal memory.
- EA is sampled and latched on reset, thus all state modification are disabled.

For further information please refer to the application note (ANM053) available upon request.

83C154D with Secret TAG

TEMIC offers special 64-bit identifier called "SECRET TAG" on the microcontroller chip.

The Secret Tag option is available on both ROMless and masked microcontrollers.

The Secret Tag feature allows serialization of each microcontroller for identification of a specific equipment. A unique number per device is implemented in the chip during manufacturing process. The serial number is a 64-bit binary value which is contained and addressable in the Special Function Registers (SFR) area.

This Secret Tag option can be read-out by a software routine and thus enables the user to do an individual identity check per device. This routine is implemented inside the microcontroller ROM memory in case of masked version which can be kept secret (and then the value of the Secret Tag also) by using a ROM Encryption.

For further information, please refer to the application note (ANM031) available upon request.

Electrical Characteristics

Absolute Maximum Ratings*

Ambiant Temperature Under Bias :
C = commercial ..... 0°C to 70°C
I = industrial ..... –40°C to +85°C
Storage Temperature ..... –65°C to + 150°C
Voltage on V_{CC} to V_{SS} ..... –0.5 V to + 7 V
Voltage on Any Pin to V_{SS} ..... –0.5 V to V_{CC} + 0.5 V
Power Dissipation ..... 1 W**
** This value is based on the maximum allowable die temperature and the thermal resistance of the package.

**** Notice***

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Characteristics

Ta = 0°C to 70°C ; V_{CC} = 5V ± 10 % ; V_{SS} = 0V ; F = 0 to 30 MHz
Ta = –40°C to 85°C ; V_{CC} = 5V ± 10 % ; V_{SS} = 0V ; F = 0 to 30 MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 VCC – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 VCC + 0.9	VCC + 0.5	V	
VIH1	Input High Voltage (RST and XTAL1)	0.7 VCC	VCC + 0.5	V	
VOL	Output Low Voltage (Ports 1, 2, 3)		0.3 0.45 1.0	V V V	IOL = 100 µA IOL = 1.6 mA (note 2) IOL = 3.5 mA
VOL1	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)		0.3 0.45 1.0	V V V	IOL = 200 µA IOL = 3.2 mA (note 2) IOL = 7.0 mA
VOH	Output High Voltage Ports 1, 2, 3	VCC – 0.3		V	IOH = – 10 µA
		VCC – 0.7		V	IOH = – 30 µA
		VCC – 1.5		V	IOH = – 60 µA
VOH1	Output High Voltage (Port 0, ALE, $\overline{PSEN}$)	VCC – 0.3		V	IOH = – 200 µA
		VCC – 0.7		V	IOH = – 3.2 mA
		VCC – 1.5		V	IOH = – 7.0 mA
IIL	Logical 0 Input Current Ports 1, 2, 3		C –50 I –60	µA	Vin = 0.45 V
ILI	Input Leakage Current (Port 0, EA)		± 10	µA	0.45 < Vin < VCC
ITL	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		– 650	µA	Vin = 2.0 V
IPD	Power Down Current		50	µA	V_{CC} = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	150	kΩ	
CIO	Capacitance of I/O Buffer		10	pF	f_c = 1 MHz, T_A = 25°C
ICC	Power Supply Current Freq = 1 MHz Icc op Icc idle Freq = 6 MHz Icc op Icc idle Freq ≥ 12 MHz Icc op = 1.14 × Freq (MHz) + 12.2 mA Icc idle = 0.36 Freq (MHz) + 2.7 mA		 1.8 1 10 4	 mA mA mA mA	Vcc = 5.5 V

Absolute Maximum Ratings*

Ambient Temperature Under Bias :
A = Automotive ..... –40°C to +125°C
Storage Temperature ..... –65°C to + 150°C
Voltage on VCC to VSS ..... –0.5 V to + 7 V
Voltage on Any Pin to VSS ..... –0.5 V to VCC + 0.5 V
Power Dissipation ..... 1 W
** This value is based on the maximum allowable die temperature and the thermal resistance of the package

** Notice*

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Parameters

TA = –40°C + 125°C ; Vss = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 25 MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 Vcc – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 1.4	Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc	Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3)		0.3 0.45 1.0	V	IOL = 100 µA IOL = 1.6 mA (note 2) IOL = 3.5 mA
VOL1	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)		0.3 0.45 1.0	V	IOL = 200 µA IOL = 3.2 mA (note 2) IOL = 7.0 mA
VOH	Output High Voltage Port 1, 2 and 3	Vcc – 0.3		V	IOH = – 10 µA
		Vcc – 0.7		V	IOH = – 30 µA
		Vcc – 1.5		V	IOH = – 60 µA VCC = 5 V ± 10 %
VOH1	Output High Voltage (Port 0, ALE, $\overline{PSEN}$)	Vcc – 0.3		V	IOH = – 200 µA
		Vcc – 0.7		V	IOH = – 3.2 mA
		Vcc – 1.5		V	IOH = – 7.0 mA VCC = 5 V ± 10 %
IIL	Logical 0 Input Current (Ports 1, 2 and 3)		– 50	µA	Vin = 0.45 V
ILI	Input leakage Current		±10	µA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		– 750	µA	Vin = 2.0 V
IPD	Power Down Current		75	µA	Vcc = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	200	KOhm	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current Freq = 1 MHz Icc op Icc idle Freq = 6 MHz Icc op Icc idle Freq ≥ 12 MHz Icc op = 1.14 Freq (MHz) + 12.2 mA Icc idle = 0.36 Freq (MHz) + 2.7 mA		 1.8 1 10 4	 mA mA mA mA	Vcc = 5.5 V

Absolute Maximum Ratings*

Ambient Temperature Under Bias :
M = Military ..... –55°C to +125°C
Storage Temperature ..... –65°C to + 150°C
Voltage on VCC to VSS ..... –0.5 V to + 7 V
Voltage on Any Pin to VSS ..... –0.5 V to VCC + 0.5 V
Power Dissipation ..... 1 W
** This value is based on the maximum allowable die temperature and the thermal resistance of the package

** Notice*

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Parameters

TA = –55°C + 125°C ; Vss = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 25 MHz

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 Vcc – 0.1	V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 Vcc + 1.4	Vcc + 0.5	V	
VIH1	Input High Voltage (for XTAL and RST)	0.7 Vcc	Vcc + 0.5	V	
VOL	Output Low Voltage (Port 1, 2 and 3)		0.45	V	IOL = 1.6 mA (note 2)
VOL1	Output Low Voltage (Port 0, ALE, PSEN)		0.45	V	IOL = 3.2 mA (note 2)
VOH	Output High Voltage (Port 1, 2, 3)	2.4		V	IOH = – 60 µA Vcc = 5 V ± 10 %
		0.75 Vcc		V	IOH = – 25 µA
		0.9 Vcc		V	IOH = – 10 µA
VOH1	Output High Voltage (Port 0 in External Bus Mode, ALE, PEN)	2.4		V	IOH = – 400 µA Vcc = 5 V ± 10 %
		0.75 Vcc		V	IOH = – 150 µA
		0.9 Vcc		V	IOH = – 40 µA
IIL	Logical 0 Input Current (Ports 1, 2 and 3)		– 75	µA	Vin = 0.45 V
ILI	Input leakage Current		±10	µA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current (Ports 1, 2 and 3)		– 750	µA	Vin = 2.0 V
IPD	Power Down Current		75	µA	Vcc = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	200	KOhm	
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz, Ta = 25°C
ICC	Power Supply Current Freq = 1 MHz Icc op Icc idle Freq = 6 MHz Icc op Icc idle Freq ≥ 12 MHz Icc op = 1.14 Freq (MHz) + 12.2 mA Icc idle = 0.36 Freq (MHz) + 2.7 mA		 1.8 1 10 4	 mA mA mA mA	Vcc = 5.5 V

Absolute Maximum Ratings*

Ambiant Temperature Under Bias :
C = commercial ..... 0°C to 70°C
I = industrial ..... –40°C to +85°C
Storage Temperature ..... –65°C to + 150°C
Voltage on V_{CC} to V_{SS} ..... –0.5 V to + 7 V
Voltage on Any Pin to V_{SS} ..... –0.5 V to V_{CC} + 0.5 V
Power Dissipation ..... 1 W**
** This value is based on the maximum allowable die temperature and the thermal resistance of the package.

** Notice*

Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC Characteristics

T_A = 0°C to 70°C ; V_{CC} = 2.7 V to 5.5 V ; V_{SS} = 0V ; F = 0 to 16 MHz
T_A = –40°C to 85°C ; V_{CC} = 2.7 V to 5.5 V ; V_{SS} = 0V ; F = 0 to 16 MHz

SYMBOL	PARAMETER	MIN	MAX		UNIT	TEST CONDITIONS
VIL	Input Low Voltage	– 0.5	0.2 V_{CC} – 0.1		V	
VIH	Input High Voltage (Except XTAL and RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5		V	
VIH1	Input High Voltage to RST for Reset	0.7 V_{CC}	V_{CC} + 0.5		V	
VIH2	Input High Voltage to XTAL1	0.7 V_{CC}	V_{CC} + 0.5		V	
VPD	Power Down Voltage to Vcc in PD Mode	2.0	6.0		V	
VOL	Output Low Voltage (Ports 1, 2, 3)		0.45		V	IOL = 0.8 mA (note 2)
VOL1	Output Low Voltage Port 0, ALE, $\overline{PSEN}$		0.45		V	IOL = 1.6 mA (note 2)
VOH	Output High Voltage Ports 1, 2, 3	0.9 V_{CC}			V	IOH = – 10 µA
VOH1	Output High Voltage (Port 0 in External Bus Mode), ALE, $\overline{PSEN}$	0.9 V_{CC}			V	IOH = – 40 µA
IIL	Logical 0 Input Current Ports 1, 2, 3		C	– 50	µA	Vin = 0.45 V
			I	– 60		
ILI	Input Leakage Current		± 10		µA	0.45 < Vin < V_{CC}
ITL	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		– 650		µA	Vin = 2.0 V
IPD	Power Down Current		50		µA	V_{CC} = 2.0 V to 5.5 V (note 1)
RRST	RST Pulldown Resistor	50	150		kΩ	
CIO	Capacitance of I/O Buffer		10		pF	f_c = 1 MHz, T_A = 25°C

Maximum I_{CC} (mA)

	OPERATING (NOTE 1)				IDLE (NOTE 1)			
FREQUENCY/Vcc	2.7 V	3 V	3.3 V	5.5 V	2.7 V	3 V	3.3 V	5.5 V
1 MHz	0.8 mA	1 mA	1.1 mA	1.8 mA	400 µA	500 µA	600 µA	1 mA
6 MHz	4 mA	5 mA	6 mA	10 mA	1.5 mA	1.7 mA	2 mA	4 mA
12 MHz	8 mA	10 mA	12 mA		2.5 mA	3 mA	3.5 mA	
16 MHz	10 mA	12 mA	14 mA		3 mA	3.8 mA	4.5 mA	
Freq > 12 MHz (Vcc = 5.5 V)	Icc (mA) = 1.14 × Freq (MHz) + 12.2 Icc Idle (mA) = 0.36 × Freq (MHz) + 2.7							

Note 1 :
ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + .5 V, VIH = VCC –.5 V ; XTAL2 N.C. ; EA = RST = Port 0 = VCC. ICC would be slightly higher if a crystal oscillator used. Idle ICC is measured with all output pins disconnected ; XTAL1 driven with TCLCH, TCHCL = 5 ns, VIL = VSS + .5 V, VIH = VCC –.5 V ; XTAL2 N.C ; Port 0 = VCC ; EA = RST = VSS.
Power Down ICC is measured with all output pins disconnected ; EA = PORT 0 = VCC ; XTAL2 N.C. ; RST = VSS.

Note 2 :
Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OLS} of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operations. In the worst (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45 V with maxi VOL peak 0.6 V. A. Schmitt Trigger use is not necessary.

Figure 14. ICC Test Condition, Idle Mode. All Other Pins Are Disconnected.

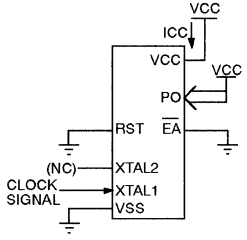


Figure 15. ICC Test Condition, Active Mode. All Other Pins Are Disconnected.

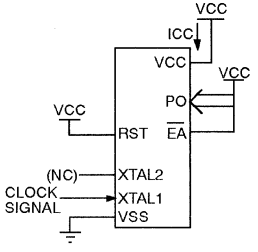


Figure 16. ICC Test Condition, Power Down Mode. All Other Pins Are Disconnected.

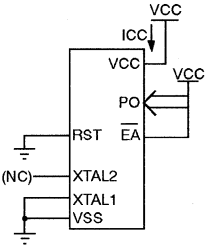
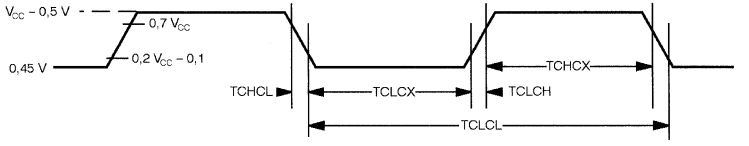


Figure 17. Clock Signal Waveform for ICC Tests in Active And Idle Modes. TCLCH = TCHCL = 5 ns.



Explanation of the AC Symbol

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example :

TAVLL = Time for Address Valid to ALE low.

TLLPL = Time for ALE low to $\overline{\text{PSEN}}$ low.

A : Address.	Q : Output data.
C : Clock.	R : READ signal.
D : Input data.	T : Time.
H : Logic level HIGH	V : Valid.
I : Instruction (program memory contents).	W : WRITE signal.
L : Logic level LOW, or ALE.	X : No longer a valid logic level.
P : PSEN.	Z : Float.

2

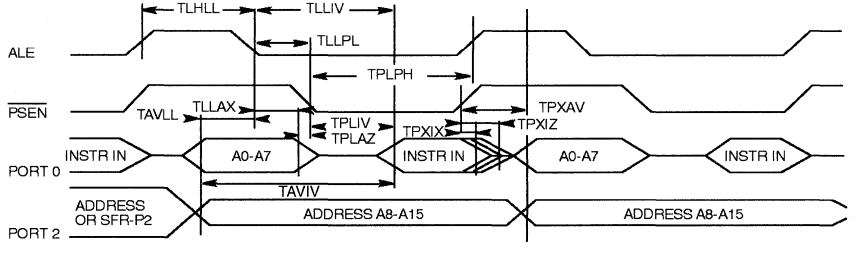
AC Parameters

TA = 0 to + 70°C ; Vss = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 30 MHz
TA = 0° + 70°C ; Vss = 0 V ; 2.7 V < Vcc < 5.5 V ; F = 0 to 16 MHz
TA = –55° + 125°C ; Vss = 0 V ; Vcc = 5 V ± 10 % ; F = 0 to 25 MHz
(Load Capacitance for PORT 0, ALE and PSEN = 100 pF ; Load Capacitance for all other outputs = 80 pF)

External Program Memory Characteristics

		16 MHz		20 MHz		25 MHz		30 MHz	
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
TLHLL	ALE Pulse Width	110		90		70		60	
TAVLL	Address valid to ALE	40		30		20		15	
TLLAX	Address Hold After ALE	35		35		35		35	
TLLIV	ALE to valid instr in		185		170		130		100
TLLPL	ALE to PSEN	45		40		30		25	
TPLPH	PSEN pulse Width	165		130		100		80	
TPLIV	PSEN to valid instr in		125		110		85		65
TPXIX	Input instr Hold After PSEN	0		0		0		0	
TPXIZ	Input instr Float After PSEN		50		45		35		30
TPXAV	PSEN to Address Valid	55		50		40		35	
TAVIV	Address to Valid instr in		230		210		170		130
TPLAZ	PSEN low to Address Float		10		10		8		6

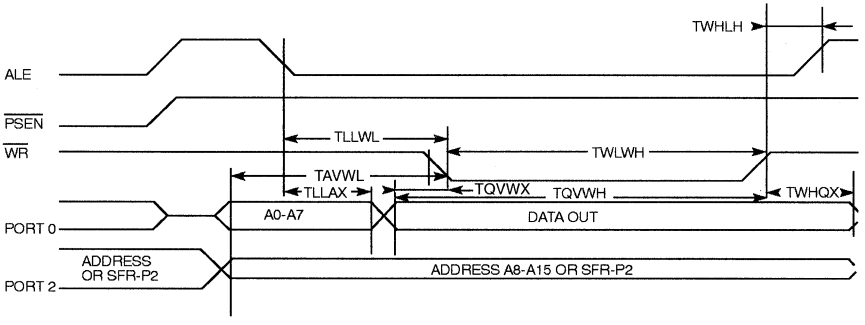
External Program Memory Read Cycle



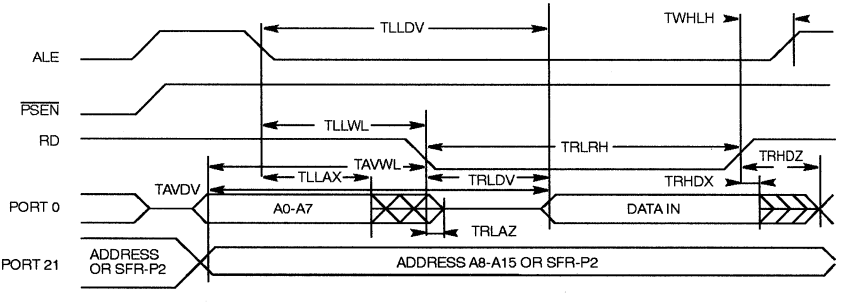
External Data Memory Characteristics

		16 MHz		20 MHz		25 MHz		30 MHz	
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
TRLRH	RD pulse Width	340		270		210		180	
TWLWH	WR pulse Width	340		270		210		180	
TLLAX	Address Hold After ALE	85		85		70		55	
TRLDV	RD to Valid in		240		210		175		135
TRHDX	Data hold after RD	0		0		0		0	
TRHDZ	Data float after RD		90		90		80		70
TLLDV	ALE to Valid Data In		435		370		350		235
TAVDV	Address to Valid Data IN		480		400		300		260
TLLWL	ALE to WR or RD	150	250	135	170	120	130	90	115
TAVWL	Address to WR or RD	180		180		140		115	
TQVWX	Data valid to WR transition	35		35		30		20	
TQVWH	Data Setup to WR transition	380		325		250		215	
TWHQX	Data Hold after WR	40		35		30		20	
TRLAZ	RD low to Address Float		0		0		0		0
TWHLH	RD or WR high to ALE high	35	90	35	60	25	45	20	40

External Data Memory Write Cycle



External Data Memory Read Cycle

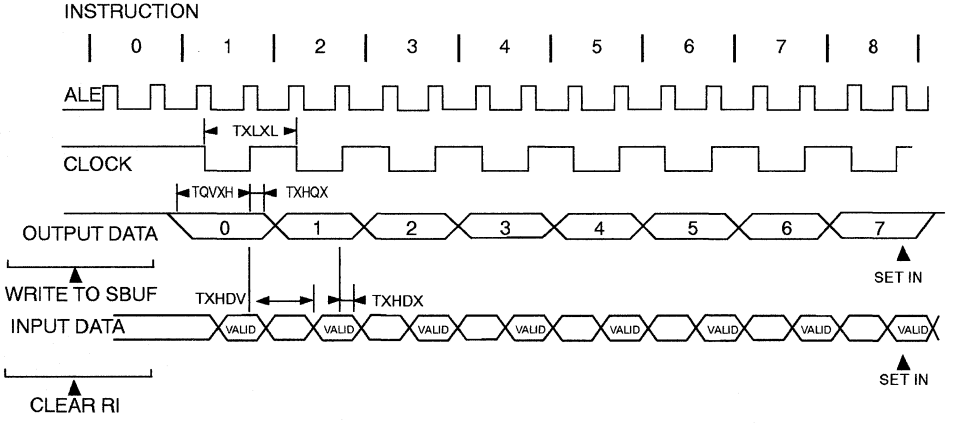


Serial Port Timing – Shift Register Mode

		16 MHz		20 MHz		25 MHz		30 MHz	
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
TXLXL	Serial Port Clock Cycle Time	750		600		480		400	
TQVXH	Output Data Setup to Clock Rising Edge	563		480		380		300	
TXHQX	Output Data Hold after Clock Rising Edge	63		90		65		50	
TXHDX	Input Data Hold after Clock Rising Edge	0		0		0		0	
TXHDV	Clock Rising Edge to Input Data Valid		563		450		350		300

2

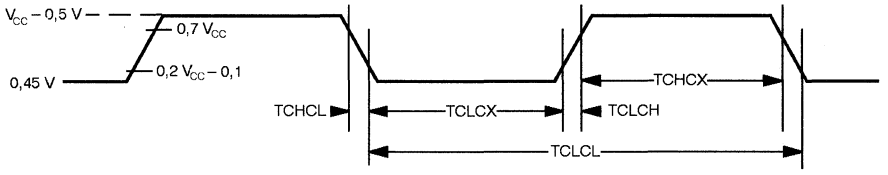
Shift Register Timing Waveforms



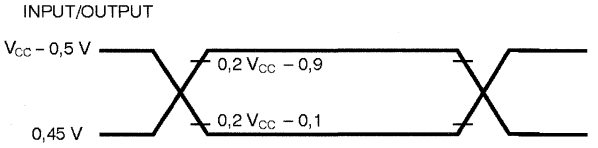
External Clock Drive Characteristics (XTAL1)

SYMBOL	PARAMETER	MIN	MAX	UNIT
FCLCL	Oscillator Frequency		30	MHz
TCLCL	Oscillator period	33.3		ns
TCHCX	High Time	5		ns
TCLCX	Low Time	5		ns
TCLCH	Rise Time		5	ns
TCHCL	Fall Time		5	ns

External Clock Drive Waveforms

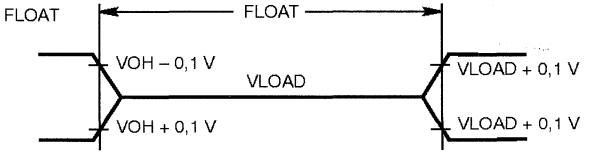


AC Testing Input/Output, Float Waveforms



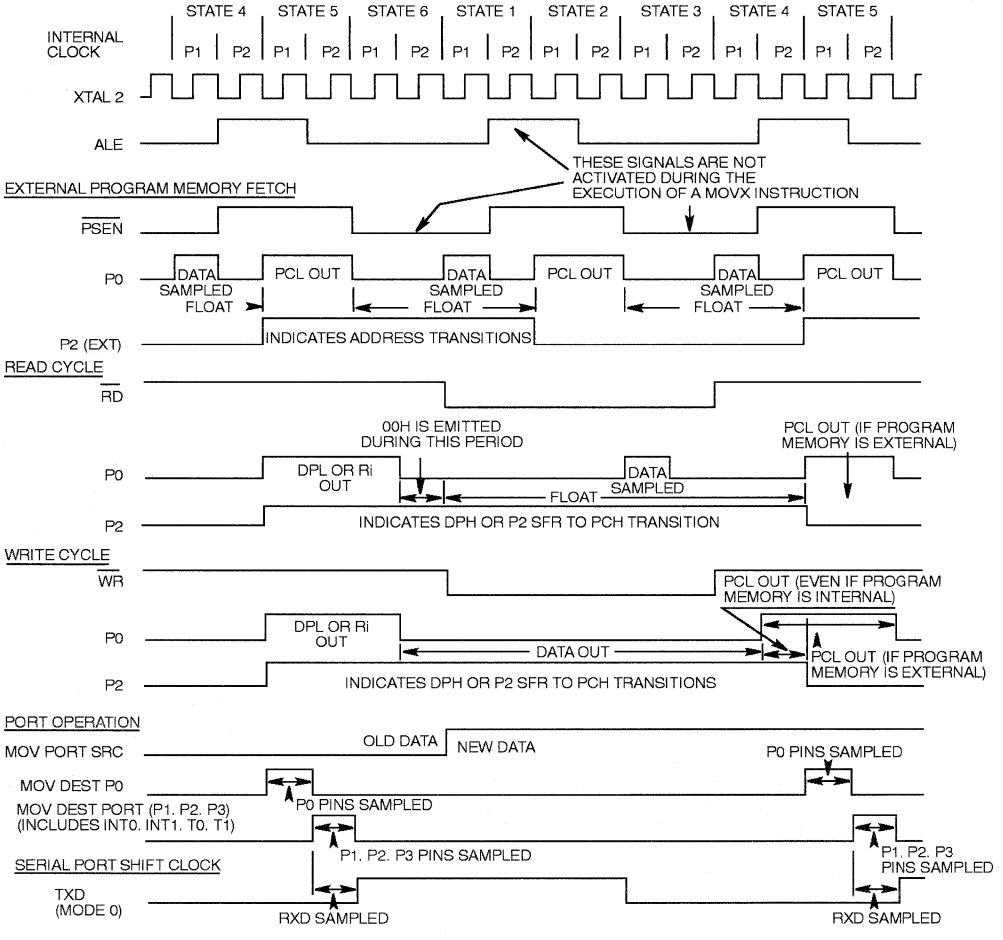
AC inputs during testing are driven at V_{CC} – 0.5 for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at VIH min for a logic "1" and VIL max for a logic "0".

Float Waveforms



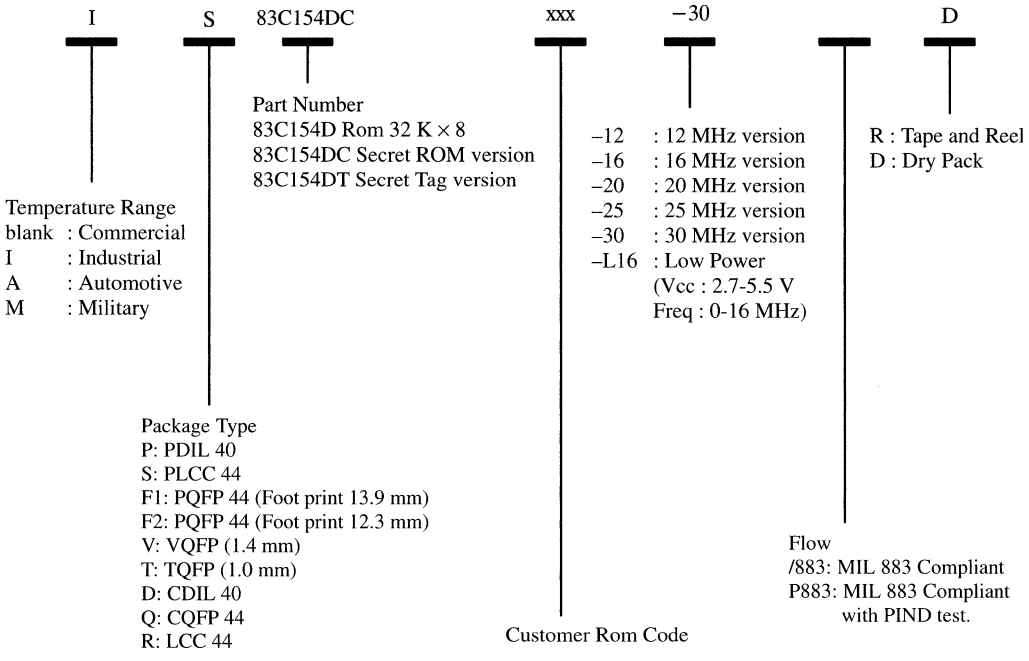
For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded VOH/VOL level occurs. Iol/IoH > ± 20 mA.

Clock Waveforms



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A = 25°C fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

Ordering Information



C51 Computer/Communication Products

TSC8051C1

8-Bit Microcontroller for Digital Computer Monitors

1. Introduction

The TSC8051C1 is a stand–alone high performance CMOS 8–bit embedded microcontroller and is designed for use in CRT monitors. It is also suitable for automotive and industrial applications.

The TSC8051C1 includes the fully static 8–bit "80C51" CPU core with 256 bytes of RAM; 8 Kbytes of ROM; two 16–bit timers; 12 PWM Channels; a 6 sources and 2–level interrupt controller; a full duplex serial port; a full I^2C™* interface; a watchdog timer and on–chip oscillator.

In addition, the TSC8051C1 has 2 software selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the RAM, the timers, the serial ports, and the interrupt system continue to function. In the power down mode the RAM is saved and all other functions are inoperative.

The TSC8051C1 enables the users reducing a lot of external discrete components while bringing the maximum of flexibility.

2. Features

- Boolean processor
- Fully static design
- 8K bytes of ROM
- 256 bytes of RAM
- 2 x 16–bit timer/counter
- Programmable serial port
- Programmable Multimaster I^2C controller
- 6 interrupt sources:
  - External interrupts (2)
  - Timers interrupt (2)
  - Serial port interrupt
  - I^2C interrupt
- Watchdog reset
- On chip oscillator for crystal or ceramic resonator
- 2 power saving control modes:
  - Idle mode
  - Power–down mode
- Controlled HSYNC & VSYNC outputs
- Up to 12 programmable PWM channels with 8–bit resolution
- Up to 32 programmable I/O lines depending on the package
- 40 pins DIP, 44 pins PQFP, 44 and 52 pins PLCC packages
- Commercial and industrial temperature ranges
- Operating Frequency: 12 MHz to 16 MHz

* I2C is a trademark of PHILIPS Corporation

3. Block Diagram

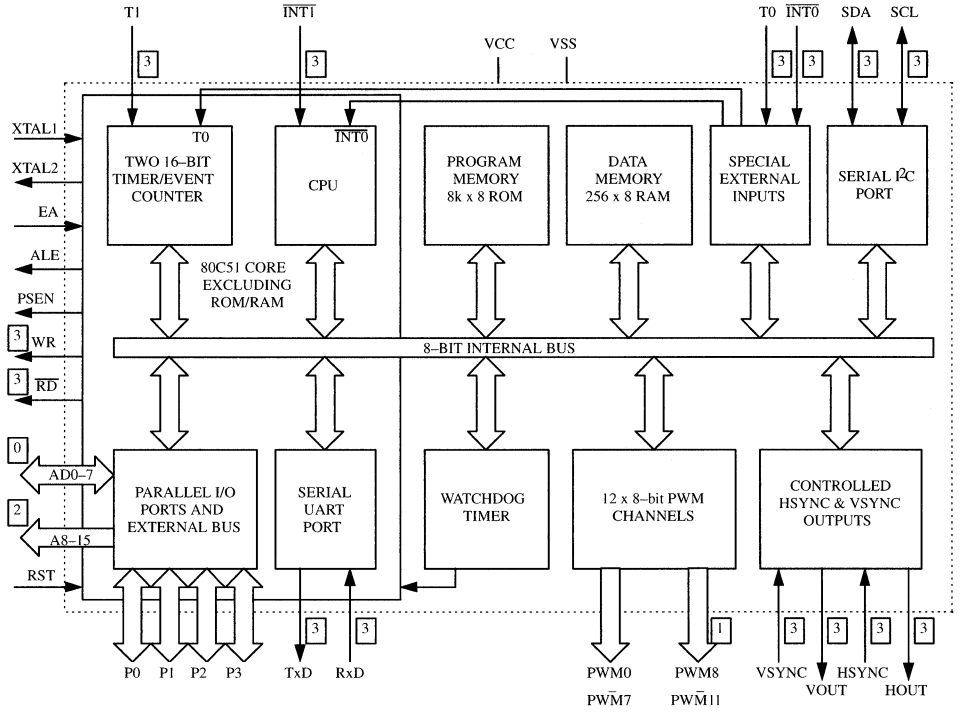
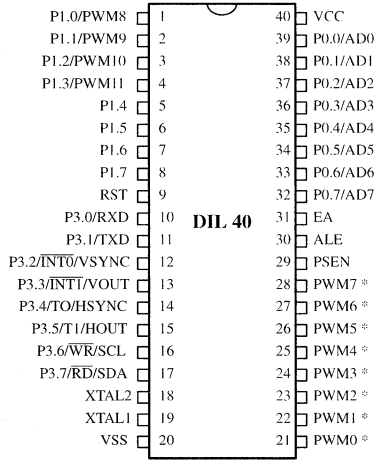
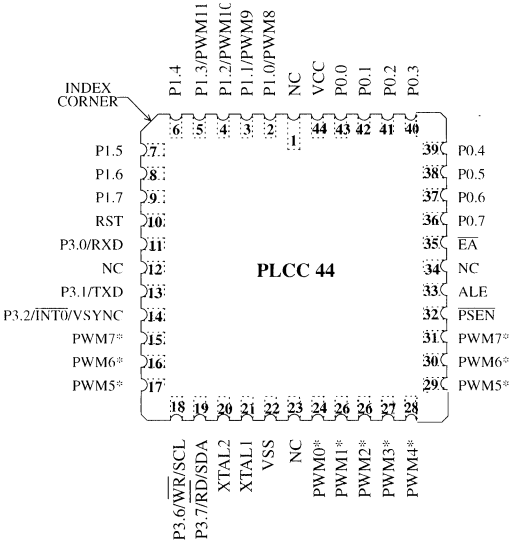


Figure 1. TSC8051C1 block diagram.

4. Pin Configurations





*PWMx or P2.x depending on option (see ordering information)

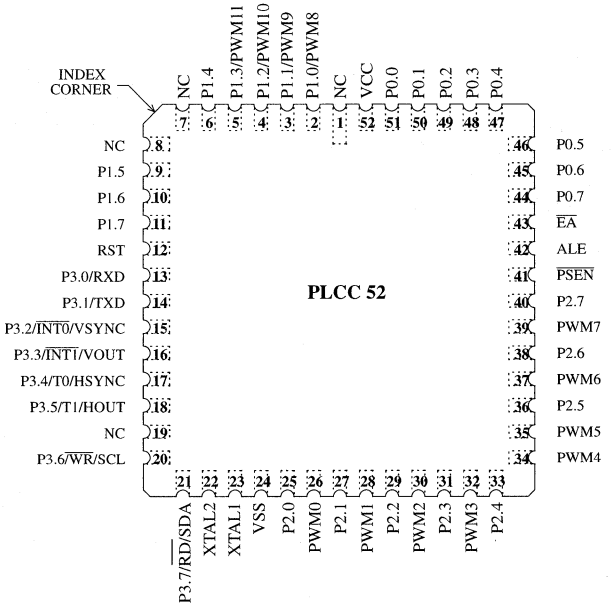


Figure 2. TSC8051C1 pin configurations.

5. Pin Description

VSS

Circuit ground.

VCC

Power supply voltage.

RST

A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pulldown resistor permits power–on reset using only a capacitor connected to VCC.

PORT 0 (P0.0–P0.7)

Port 0 is an 8–bit open–drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high–impedance inputs.

Port 0 is also the multiplexed low–order address and data bus during access to external Program and Data memory. In this application it uses strong internal pull–up when emitting 1's.

Port 0 can sink and source 8 LS TTL loads.

PORT 1 (P1.0–P1.7)

Port 1 is an 8–bit bidirectional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL on the data–sheet) because of the internal pullups.

Port 1 also serves 4 programmable PWM open drain outputs, as listed below:

Port Pin	Alternate Function
P1.0	PWM8: Pulse Width Modulation output 8.
P1.1	PWM9: Pulse Width Modulation output 9.
P1.2	PWM10: Pulse Width Modulation output 10.
P1.3	PWM11: Pulse Width Modulation output 11.

Port 1 can sink and source 3 LS TTL loads.

PORT 2 (P2.0–P2.7)

Port 2 is an 8–bit bidirectional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL on the data–sheet) because of the internal pullups.

Port 2 emits the high–order 8–bit address during fetches from external Program Memory and during accesses to external Data Memory that use 16–bit addresses. In this application it uses strong internal pull–up when emitting 1's.

Port 2 can sink and source 3 LS TTL loads.

PORT 3 (P3.0–P3.7)

Port 3 is an 8–bit bidirectional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL on the data–sheet) because of the internal pullups.

Each line on this port has 2 or 3 functions either a general I/O or special control signal, as listed below:

Port Pin	Alternate Function
P3.0	RXD: serial input port.
P3.1	TXD: serial output port.
P3.2	$\overline{INT0}$: external interrupt 0. VSYNC: vertical synchro input.
P3.3	$\overline{INT1}$: external interrupt 1. VOUT: buffered V-SYNC output.
P3.4	T0: Timer 0 external input. HSYNC: horizontal synchro input.
P3.5	T1: Timer 1 external input. HOUT: buffered H–SYNC output.
P3.6	$\overline{WR}$: external data memory write strobe. SCL: serial port clock line I^2C bus.
P3.7	$\overline{RD}$: external data memory read strobe. SDA: serial port data line I^2C bus.

Port 3 can sink and source 3 LS TTL loads.

PWM0–7

These eight Pulse Width Modulation outputs are true open drain outputs and are floating after reset.

ALE

The Address Latch Enable output signal occurs twice each machine cycle except during external data memory access. The negative edge of ALE strobes the address into external data memory or program memory. ALE can sink and source 8 LS TTL loads.

If desired, ALE operation can be disabled by setting bit 0 of SFR location AFh (MSCON). With the bit set, ALE is active only during MOVX instruction and external fetches. Otherwise the pin is pulled low.

$\overline{EA}$

When the External Access input is held high, the CPU executes out of internal program memory (unless the Program Counter exceeds 1FFFh). When $\overline{EA}$ is held low the CPU executes only out of external program memory. must not be left floating.

$\overline{PSEN}$

The Program Store Enable output signal remains high during internal program memory. An active low output occurs during an external program memory fetch. $\overline{PSEN}$ can sink and source 8 LS TTL loads.

XTAL1

Input to the inverting oscillator amplifier and input to the external clock generator circuits.

XTAL2

Output from the inverting oscillator amplifier. This pin should be non–connected when external clock is used.

6. Basic Functional Description

6.1. Idle And Power Down Operation

Figure 3 shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. Idle mode operation allows the interrupt, serial port, and timer blocks to continue to operate while the clock to the CPU is gated off.

These special modes are activated by software via the Special Function Register, its hardware address is 87h. PCON is not bit addressable.

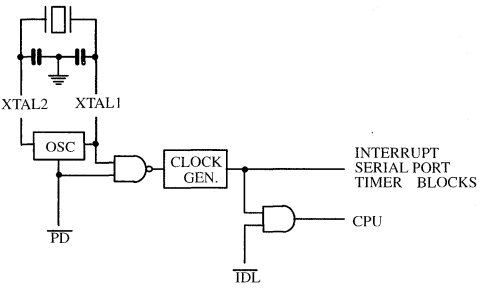


Figure 3. Idle and Power Down Hardware.

PCON: Power Control Register

MSB			SFR 87h				LSB
SMOD	–	–	–	GF1	GF0	PD	IDL

Symbol	Position	Name and Function
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
GF0	PCON.2	General–purpose flag bit.
GF1	PCON.3	General–purpose flag bit.
–	PCON.4	(Reserved).
–	PCON.5	(Reserved).
–	PCON.6	(Reserved).
SMOD	PCON.7	Double Baud rate bit. Setting this bit causes the baud rate to double when the serial port is being used in either modes 1, 2 or 3.

If 1's are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is 0XXX0000b.

6.1.1. Idle Mode

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM, and all other register maintain their data during Idle Table 1 describes the status of the external pins during Idle mode.

There are two ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

6.1.2. Power Down Mode

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register are saved during power down mode. A hardware reset is the only way of exiting the power down mode. The hardware reset initiates the Special Function Register. In the Power Down mode, VCC may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the power down mode is entered, and that the voltage is restored before the hardware reset is applied which frees the oscillator. Reset should not be released until the oscillator has restarted and stabilized. Table 1 describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a 1, the port pin is held high during the power down mode by the strong pullup transistor.

Table 1. Status of the external pins during Idle and Power Down modes.

Mode	Program Memory	ALE	PSEN	Port 0	Port 1	Port 2	Port 3	PWMx
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data	Floating
Idle	External	1	1	Floating	Port Data	Address	Port Data	Floating
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data	Floating
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data	Floating

6.2. Stop Clock Mode

Due to static design, the TSC8051C1 clock speed can be reduced down to 0 MHz without any data loss in memory or register. This mode allows step by step code execution, and permits to reduce system power consumption by bringing the clock frequency down to any value. When the clock is stopped, the power consumption is the same as in the Power Down Mode.

6.3. I/O Ports Structure

The TSC8051C1 has four 8–bit ports. Each port consist of a latch (special function register P0 to P3), an input buffer and an output driver. These ports are the same as in 80C51, with the exception of the additional functions of port 1 and port 3 (see Pin Description section).

6.4. I/O Configurations

Figure 4. shows a functional diagram of the generic bit latch and I/O buffer in each of the four ports. The bit latch, (one bit in the port SFR) is represented as a D type flip–flop. A 'write to latch' signal from the CPU latches a bit from the internal bus and a 'read latch' signal from the CPU places the Q output of the flip–flop on the internal bus. A 'read pin' signal from the CPU places the actual pin logical level on the internal bus.
Some instructions that read a port read the actual pin, and other instructions read the latch (SFR).

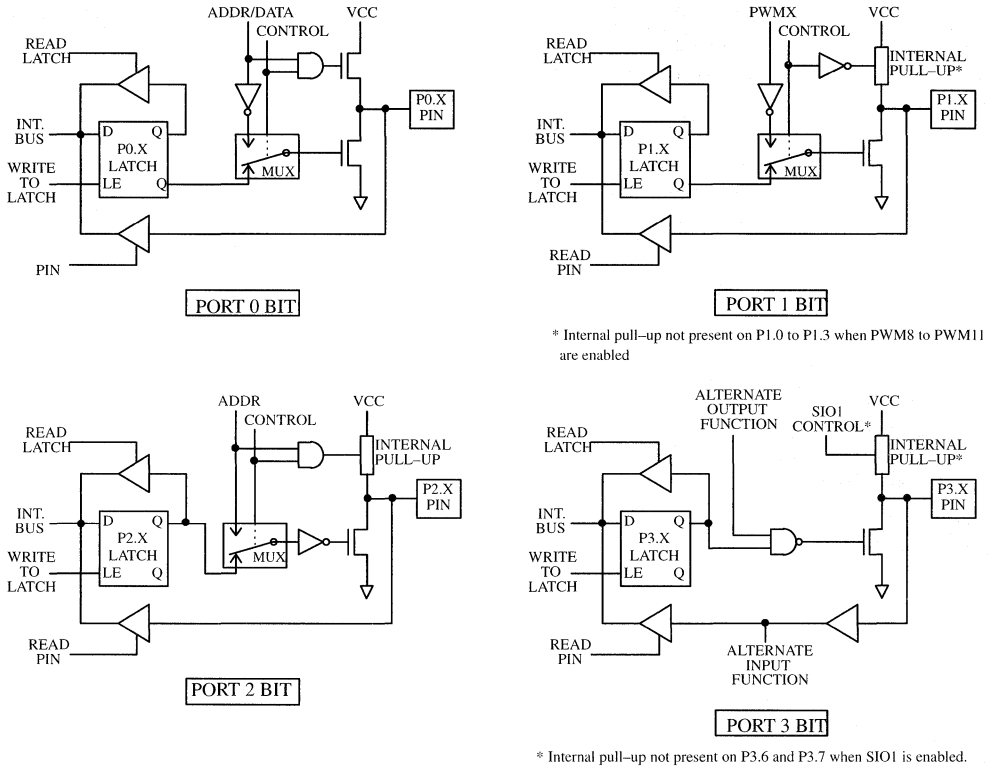


Figure 4. Port Bit Latches and I/O buffers

6.5. Reset Circuitry

The reset circuitry for the TSC8051C1 is connected to the reset pin RST. A Schmitt trigger is used at the input for noise rejection (see Figure 5.).

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by executing an internal reset. It also configures the ALE and PSEN pins as inputs (they are quasi–bidirectional). A Watchdog timer underflow if enabled, will force a reset condition to the TSC8051C1 by an internal connection.

The internal reset is executed during the second cycle in which reset is high and is repeated every cycle until RST goes low. It leaves the internal registers as follows:

Register	Content
ACC	00h
B	00h
DPTR	0000h
EICON	00h
HWDR	00h
IE	0X000000b
IP	XX000000b
MSCON	XXXXXXX0b
MXCR0–1	00h
P0–P3	FFh

Register	Content
PC	0000h
PCON	0XXX0000b
PSW	00h
PWM0–11	00h
PWMCON	XXXXXXX0b
S1CON	00h
S1DAT	00h
S1STA	F8h
SBUF	00h
SCON	00h
SOCR	00h
SP	07h
TCON	00h
TH0, TH1	00h
TL0, TL1	00h
TMOD	00h

The internal RAM is not affected by reset. At power–on reset, the RAM content is indeterminate.

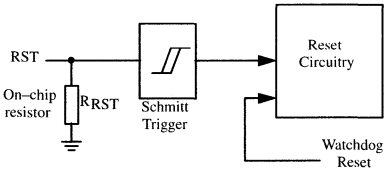


Figure 5. On–Chip Reset Configuration.

An automatic reset can be obtained when VCC is turned on by connecting the RST pin to VCC through a 1µF capacitor providing the VCC setting time does not exceed 1ms and the oscillator start–up time does not exceed 10ms. This power–on reset circuit is shown in Figure 6. When power comes on, the current drawn by RST starts to charge the capacitor. The voltage at RST is the difference between VCC and the capacitor voltage, and decreases from VCC as the capacitor charges. VRST must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start–up time, plus 2 machine cycles.

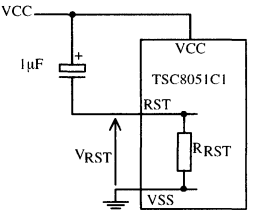


Figure 6. Power–on Reset Circuit

6.6. Oscillator Characteristics

XTAL1 and XTAL2 are respectively the input and output of an inverting amplifier which is configured for use as an on–chip oscillator. As shown in Figure 7. , either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in Figure 8.

There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide–by–two flip–flop. The minimum high and low times specified on the data sheet must be observed however.

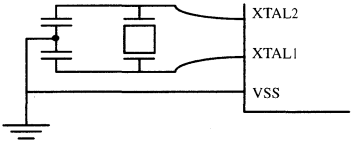


Figure 7. Crystal Oscillator

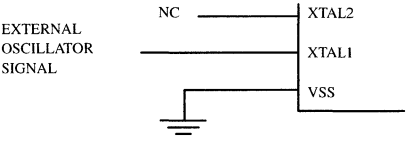


Figure 8. External Drive Configuration

6.7. Memory organization

The memory organisation of the TSC8051C1 is the same as in the 80C51, with the exception that the TSC8051C1 has 8k bytes ROM, 256 bytes RAM, and additional SFRs. Details of the differences are given in the following paragraphs.

In the TSC8051C1, the lowest 8k of the 64k program memory address space is filled by internal ROM. Depending on the package used, external access is available or not. By tying the $\overline{EA}$ pin high, the processor fetches instructions from internal program ROM. Bus expansion for accessing program memory from 8k upward is automatic since external instruction fetches occur automatically when the program counter exceeds 1FFFh. If the $\overline{EA}$ pin is tied low, all program memory fetches are from external memory. The execution speed is the same regardless of whether fetches are from external or internal program memory. If all storage is on–chip, then byte location 1FFFh should be left vacant to prevent an undesired pre–fetch from external program memory address 2000h.

Certain locations in program memory are reserved for specific purposes. Locations 0000h to 0002h are reserved for the initialisation program. Following reset, the CPU always begins execution at location 0000h. Locations 0003h to 0032h are reserved for the six interrupt request service routines.

The internal data memory space is divided into a 256–bytes internal RAM address space and a 128 bytes special function register address space.

The internal data RAM address space is 0 to FFh. Four 8–bit register banks occupy locations 0 to 1Fh. 128 bit locations of the internal data RAM are accessible through direct addressing. These bits reside in 16 bytes of internal RAM at location 20h to 2Fh. The stack can be located anywhere in the internal data RAM address space by loading the 8–bit stack pointer (SP SFR).

The SFR address space is 100h to 1FFh. All registers except the program counter and the four 8–bit register banks reside in this address space. Memory mapping of the SFRs allows them to be accessed as easily as internal RAM, and as such, they can be operated on by most instructions.The mapping in the SFR address space of the 43 SFRs is shown in Table 2. The SFR names in italic are TSC8051C1 new SFRs and are described in Peripherals Functional Description section. The SFR names in bold are bit addressable.

Table 2. Mapping of Special Function Register

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
F8					*PWM8*	*PWM9*	*PWM10*	*PWM11*
F0	B				*PWM4*	*PWM5*	*PWM6*	*PWM7*
E8					*PWM0*	*PWM1*	*PWM2*	*PWM3*
E0	ACC				*EICON*	*SOCR*	*HWDR*	*MXCR0*
D8	*S1CON*	*S1STA*	*S1DAT*					*PWMCON*
D0	PSW							*MXCR1*
C8								
C0								
B8	IP							
B0	P3							
A8	IE							MSCON
A0	P2							
98	SCON	SBUF						
90	P1							
88	TCON	TMOD	TL0	TL1	TH0	TH1		
80	P0	SP	DPL	DPH				PCON

6.8. Interrupts

The TSC8051C1 has six interrupt sources, each of which can be assigned one of two priority levels. The five interrupt sources common to the 80C51 are the external interrupts (INT0 and INT1), the timer 0 and timer 1 interrupts (IT0 and IT1), and the serial I/O interrupt (RI or TI). In the TSC8051C1, the standard serial I/O is called SIO0.

The SIO1 (I^2C) interrupt is generated by the SI flag in the control register (S1CON SFR). This flag is set when the status register (S1STA SFR) is loaded with a valid status code.

6.8.1. Interrupt Enable Register:

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable register (IE SFR). All interrupts sources can also be globally enabled or disabled by setting or clearing the EA bit in IE register.

IE: Interrupt Enable Register

MSB			SFR A8h				LSB
EA	–	ES1	ES0	ET1	EX1	ET0	EX0

Symbol	Position	Name and Function
EX0	IE.0	Enable external interrupt 0.
ET0	IE.1	Enable timer 0 interrupt.
EX1	IE.2	Enable external interrupt 1.
ET1	IE.3	Enable timer 1 interrupt.
ES0	IE.4	Enable SIO0 (UART) interrupt.
ES1	IE.5	Enable SIO1 (I^2C) interrupt.
–	IE.6	(Reserved).
EA	IE.7	Enable all interrupts.

6.8.2. Interrupt Priority Structure:

Each interrupt source can be assigned one of two priority levels. Interrupt priority levels are defined by the interrupt priority register (IP SFR). Setting a bit in the interrupt priority register selects a high priority interrupt, clearing it selects a low priority interrupt.

IP: Interrupt Priority Register

MSB			SFR B8h				LSB
–	–	PS1	PS0	PT1	PX1	PT0	PX0

Symbol	Position	Name and Function
PX0	IP.0	External interrupt 0 priority level.
PT0	IP.1	Timer 0 interrupt priority level.
PX1	IP.2	External interrupt 1 priority level.
PT1	IP.3	Timer 1 interrupt priority level.
PS0	IP.4	SIO0 (UART) interrupt priority level.
PS1	IP.5	SIO1 (I^2C) interrupt priority level.
–	IP.6	(Reserved).
–	IP.7	(Unused).

A low priority interrupt service routine may be interrupted by a high priority interrupt. A high priority interrupt service routine cannot be interrupted by any other interrupt source.

If two requests of different priority levels occur simultaneously, the high priority level request is serviced. If requests of same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus, within each priority level, there is a second priority structure determined by the polling sequence, as follows:

Order	Source	Priority Within Level
1	INT0	(highest)
2	Timer 0	↑
3	INT1	
4	Timer 1	
5	SIO0	↓
6	SIO1	(lowest)

6.8.3. Interrupt Handling:

The interrupt flags are sampled at S5P2 of every machine cycle. The samples are polled during the following machine cycle. If one of the flags was in a set condition at S5P2 of the previous machine cycle, the polling cycle will find it and the interrupt system will generate a LCALL to the appropriate service routine, provided this hardware–generated LCALL is not blocked by any of the following conditions:

1. An interrupt of higher or equal priority is already in progress.

2. The current (polling) cycle is not the final cycle in the execution of the instruction in progress.

3. The instruction in progress is RETI or any access to the IE or IP SFR.

Any of these three conditions will block the generation of the LCALL to the interrupt service routine. Note that if an interrupt is active but not being responded to for one of the above conditions, if the flag is not still active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the facts that the interrupt flag was once active but not serviced is not memorized. Every polling cycle is new.

The processor acknowledges an interrupt request by executing a hardware–generated LCALL to the appropriate service routine. In some cases it also clears the flag that generated the interrupt, and in other case it does not. It clears the timer 0, timer 1, and external interrupt flags. An external interrupt flag (IE0 or IE1) is cleared only if it was transition–activated. All other interrupt flags are not cleared by hardware and must be cleared by the software. The LCALL pushes the contents of the program counter onto the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to, as listed below:

Source	Vector Address
IE0	0003h
TF0	000Bh
IE1	0013h
TF1	001Bh
RI + TI	0023h
SI	002Bh

Execution proceeds from the vector address until the RETI instruction is encountered. The RETI instruction clears the 'priority level active' flip–flop that was set when this interrupt was acknowledged. It then pops two bytes from the the top of the stack and reloads the program counter with them. Execution of the interrupted program continues from where it was interrupted.

7. Peripherals Functional Description

For detailed functionnal description of standard 80C51 peripherals, please refer to C51 Family, Hardware Description and Programmer's Guides.

7.1. Watchdog Timer

The watchdog timer consists of a 4–bit timer with a 17–bit prescaler as shown in Figure 9. The prescaler is fed with a signal whose frequency is 1/12 the oscillator frequency (1MHz with a 12MHz oscillator).

The 4–bit timer is decremented every 't' seconds, where: t = 12 x 131072 x 1/fosc. (131.072ms at fosc = 12MHz). Thus, the interval may vary from 131.072ms to 2097.152ms in 16 possible steps (see Table 3.).

The watchdog timer has to be reloaded (write to HWDR SFR) within periods that are shorter than the programmed watchdog interval, otherwise the watchdog timer will underflow and a system reset will be generated which will reset the TSC8051C1.

HWDR: Hardware WatchDog Register

MSB			SFR E6h				LSB
WTE	–	–	–	WT3	WT2	WT1	WT0

Symbol	Position	Name and Function
WT0	HWDR.0	Watchdog Timer Interval bit 0.
WT1	HWDR.1	Watchdog Timer Interval bit 1.
WT2	HWDR.2	Watchdog Timer Interval bit 2.
WT3	HWDR.3	Watchdog Timer Interval bit 3.
–	HWDR.4	Reserved for test purpose, must remain to 0 for normal operation.
–	HWDR.5	(Reserved).
–	HWDR.6	(Reserved).
WTE	HWDR.7	Watchdog Timer Enable bit. Setting this bit activates watchdog operation.

Table 3. Watchdog timer interval value format.

WT3	WT2	WT1	WT0	Interval
0	0	0	0	t x 16
0	0	0	1	t x 1
0	0	1	0	t x 2
:	:	:	:	:
:	:	:	:	:
1	1	1	1	t x 15

Once the watchdog timer enabled setting WTE bit, it cannot be disabled anymore, except by a system reset.

The watchdog timer is frozen during idle or power down mode.

HWDR is a write only register. Its value after reset is 00h which disables the watchdog operation.

HWDR is using TSC8051C1 Special Function Register address, E6h.

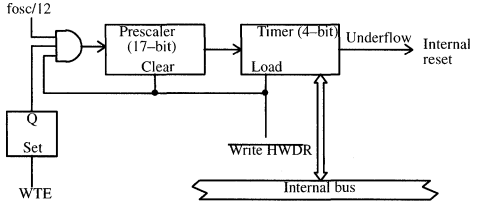


Figure 9. Watchdog timer block diagram

7.2. Pulse Width Modulated Outputs

The TSC8051C1 contains twelve pulse width modulated output channels (see Figure 10.). These channels generate pulses of programmable duty cycle with an 8–bit resolution.

The 8–bit counter counts modulo 256 by default i.e., from 0 to 255 inclusive but can count modulo 254 i.e., from 0 to 253 inclusive by programming the bit 0 of the PWMCON register. The counter clock is supplied by the oscillator frequency. Thus, the repetition frequency fpwm is constant and equals to the oscillator frequency divided by 256 or 254 (fpwm=46.875KHz or 47.244KHz with a 12MHz oscillator). The 8–bit counter is common to all PWM channels, its value is compared to the contents of the twelve registers: PWM0 to PWM11. Provided the content of each of these registers is greater than the counter value, the corresponding output is set low. If the contents of these registers are equal to, or less than the counter value the output will be high.

The pulse–width ratio is therefore defined by the contents of these registers, and is in the range of 0 (all '0' written to PWM register) to 255/256 or 1 (all '1' written to PWM register) and may be programmed in increments of 1/256 or 1/254. When the 8–bit counter counts modulo 254, it can never reach the value of the PWM registers when they are loaded with FEh or FFh.

PWMx: Pulse Width Modulator x Register

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

When a compare register (PWM0 to PWM11) is loaded with a new value, the associated output is updated immediately. It does not have to wait until the end of the current counter period. All the PWM outputs are open–drain outputs with standard current drive and standard maximum voltage capability. When they are disabled, eight of them (PWM0 to PWM7) are in high impedance while the other four (PWM8 to PWM11) are standard Port outputs with internal pullups.

PWM0 to PWM11 are write only registers. Their value after reset is 00h.

PWM0 to PWM11 are using TSC8051C1 Special Function Registers addresses as detailed in Table 4.

Table 4. PWM SFR register addresses

Channel	SFR address
PWM0	ECh
PWM1	EDh
PWM2	EEh
PWM3	EFh
PWM4	F4h
PWM5	F5h
PWM6	F6h
PWM7	F7h
PWM8	FCh
PWM9	FDh
PWM10	FEh
PWM11	FFh

Two 8–bit control registers: MXCR0 and MXCR1 are used to enable or disable PWM outputs.

MXCR0 is used for PWM0 to PWM7. MXCR1 is used for PWM8 to PWM11, these PWMs are multiplexed with PORT 1 (see Table 5.)

MXCR0: PWM Multiplexed Control Register 0

MSB			SFR E7h				LSB
PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0

Symbol	Position	Name and Function
PEx	MXCR0.x	PWM_X Enable bit. Setting this bit enables PWMx output. Clearing this bit disables PWMx output.

MXCR1: PWM Multiplexed Control Register 1

MSB			SFR D7h				LSB
–	–	–	–	PE11	PE10	PE9	PE8

Symbol	Position	Name and Function
PEx	MXCR1.x	PWM_{X+8} Enable bit. Setting this bit enables PWMx output. Clearing this bit disables PWMx output and activates the I/O pin (see Table 5).

MXCR0 and MXCR1 are read/write registers. Their value after reset is 00h which corresponds to all PWM disabled.

PWM will not operate in idle and power down modes (frozen counter). When idle or power down mode is entered, the PWM0 to PWM7 output pins are floating and PWM8 to PWM11 pins are set to general purpose P1 port with the value of P1 SFR.

MXCR0 and MXCR1 are using TSC8051C1 Special Function Register addresses, E7h and D7h respectively.

Table 5. PWM alternate pin.

Channel	Pin assignment
PWM8	P1.0
PWM9	P1.1
PWM10	P1.2
PWM11	P1.3

PWMCON is used to control the PWM counter.

PWMCON: PWM Control Register

MSB			SFR DFh				LSB
–	–	–	–	–	–	–	CMOD

Symbol	Position	Name and Function
CMOD	PWMCON.0	Counter modulo. Setting this bit sets the modulo to 254. Clearing this bit sets the modulo to 256.

PWMCON is a write only register. Its value after reset is 00h which sets the PWM counter modulo to 256.

PWMCON is using TSC8051C1 Special Function Register address, DFh.

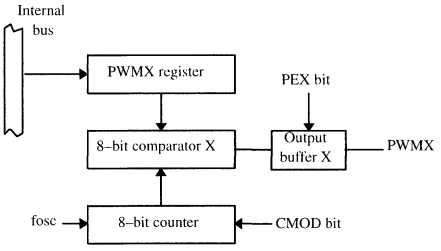


Figure 10. Pulse width modulated outputs block diagram

Figure 11. shows a PWM programming example with PWM register content 55h and counter modulo 256.

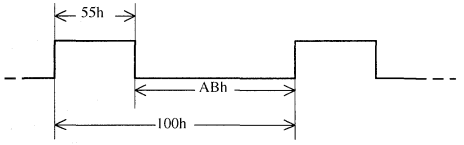


Figure 11. PWM programming example.

SOCR: Synchronisation Output Control Register.

MSB		SFR E5h					LSB
–	–	VOS	HOS	VOP	VOE	HOP	HOE

Symbol	Position	Name and Function
HOE	SOCR.0	HSYNC Output Enable bit. Setting this bit enables the HSYNC signal.
HOP	SOCR.1	HSYNC Output Polarity bit. Setting this bit inverts the HSYNC output.
VOE	SOCR.2	VSYNC Output Enable bit. Setting this bit enables the VSYNC signal.
VOP	SOCR.3	VSYNC Output Polarity bit. Setting this bit inverts the VSYNC output.
HOS	SOCR.4	HSYNC Output Selection bit. Setting this bit selects the VSYNC output, clearing it selects P3.5 SFR bit.
VOS	SOCR.5	VSYNC Output Selection bit. Setting this bit selects the VSYNC output, clearing it selects P3.3 SFR bit.

SOCR is a write only register. Its value after reset is 00h which enables P3.3 and P3.5 general purpose I/O pins.

SOCR is using TSC8051C1 Special Function Register address, E5h.

Note: when packaging P2.X is selected, PWM0 to PWM7 are not available. Please refer to ordering information.

7.3. Controlled HSYNC and VSYNC Outputs

SOCR is used to configure P3.3 and P3.5 pins as buffered HSYNC and VSYNC outputs or as general purpose I/Os. When either HSYNC or VSYNC is selected, the output level can be respectively programmed as P3.4 or P3.2 input level (inverted or not), or as a low level if not enabled. Figure 12. shows the programmable HSYNC and VSYNC output block diagram.

2

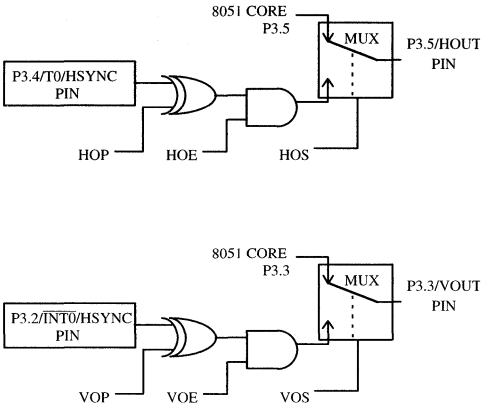


Figure 12. Buffered HSYNC and VSYNC block diagram

7.4. HSYNC and VSYNC Inputs

EICON is used to control $\overline{INT0}$VSYNC input. Thus, an interrupt on either falling or rising edge and on either high or low level can be requested. Figure 13. shows the programmable $\overline{INT0}$/VSYNC input block diagram.

EICON is also used to control T0/HSYNC input as short pulses input capture to be able to count them with timer 0. Pulse duration shorter than 1 clock period is rejected; depending on the position of the sampling point in the pulse, pulse duration longer than 1 clock period and shorter than 1.5 clock period may be rejected or accepted; and pulse duration longer than 1.5 clock period is accepted. Moreover selection of negative or positive pulses can be programmed.

Accepted pulse is lengthened up to 1 cycle period to be sampled by the 8051 core (one time per machine cycle: 12 clock periods), this implies that the maximum pulse frequency is unchanged and equal to $f_{OSC}/24$. Figure 14. shows the programmable T0/HSYNC input block diagram. The Digital Timer Delay samples T0/HSYNC pulses and rejects or lengthens them.

EICON: External Input Control Register

MSB			SFR E4h				LSB
–	–	–	–	–	T0L	T0S	I0L

Symbol	Position	Name and Function
I0L	EICON.0	$\overline{INT0}$/VSYNC input Level bit. Setting this bit inverts $\overline{INT0}$/VSYNC input signal. Clearing it allows standard use of $\overline{INT0}$/VSYNC input.
T0S	EICON.1	T0/HSYNC input Selection bit. Setting this bit allows short pulse capture. Clearing it allows standard use of T0/HSYNC input.
T0L	EICON.2	T0/HSYNC input Level bit. Setting this bit allows positive pulse capture. Clearing it allows negative pulse capture.

EICON is a write only register. Its value after reset is 00h which allows standard $\overline{INT0}$ and T0 inputs feature.

EICON is using TSC8051C1 Special Function Register address, E4h.

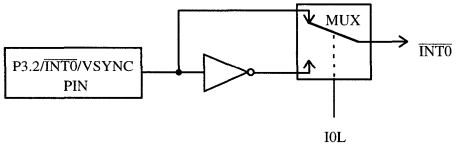


Figure 13. $\overline{INT0}$/VSYNC input block diagram

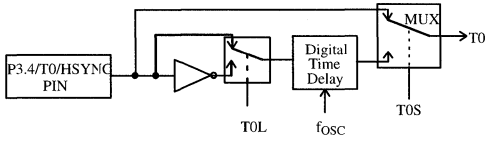


Figure 14. T0/HSYNC input block diagram

7.5. SIO1, I²C Serial I/O

SIO1 provides a serial interface that meets the I²C bus specification and supports the master transfer modes with multimaster capability from and to the I²C bus. The SIO1 logic handles bytes transfer autonomously. It also keeps track of serial transfers and a status register reflects the status of SIO1 and the I²C bus.

Figure 15. shows a typical use of I²C bus with SIO1, and
Figure 16. shows a complete data transfer with SIO1.

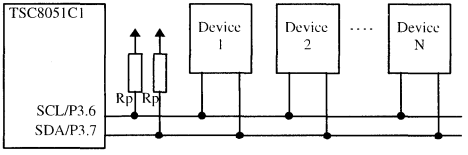


Figure 15. Typical I²C bus configuration

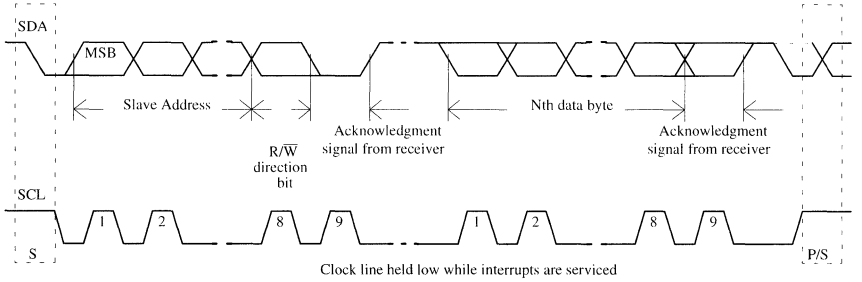


Figure 16. Complete data transfer on I²C bus

Three 8–bit special function registers are used to control SIO1: the control register (S1CON SFR), the status register (S1STA SFR) and the data register (S1DAT SFR).

S1CON is used to enable SIO1, to program the bit rate (see Table 6.), to acknowledge or not a received data, to send a start or a stop condition on the I²C bus, and to acknowledge a serial interrupt.

S1CON: Synchronous Serial Control Register

MSB			SFR D8h				LSB
CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Symbol	Position	Name and Function
CR0	S1CON.0	Control Rate bit 0. See Table 6.
CR1	S1CON.1	Control Rate bit 1. See Table 6.
AA	S1CON.2	Assert Acknowledge flag. In receiver mode, setting this bit forces an acknowledge (low level on SDA). In receiver mode, clearing this bit forces a not acknowledge (high level on SDA). When in transmitter mode, this bit has no effect.
SI	S1CON.3	Synchronous Serial Interrupt flag. This bit is set by hardware when a serial interrupt is requested. This bit must be reset by software to acknowledge interrupt.
ST0	S1CON.4	Stop flag. Setting this bit causes a stop condition to be sent on bus.
STA	S1CON.5	Start flag. Setting this bit causes a start condition to be sent on bus.
ENS1	S1CON.6	Synchronous Serial Enable bit. Setting this bit enables the SIO1 controller.
CR2	S1CON.7	Control Rate bit 2. See Table 6.

S1CON is a read/write. Its value after reset is 00h which disables the I²C controller.

S1CON is using TSC8051C1 Special Function Register address, D8h.

Table 6. Serial Clock Rates

			Bit frequency (kHz)		
CR2	**CR1**	**CR0**	**6MHz**	**12MHz**	**fosc divided by**
0	0	0	23.5	47	256
0	0	1	27	53.5	224
0	1	0	31.25	62.5	192
0	1	1	37.5	75	160
1	0	0	6.25	12.5	960
1	0	1	50	100	120
1	1	0	100	–	60
1	1	1	0.25<62.5	0.5<62.5	Timer 1 overflow 96 x (256 – reload value) value: 0–254 in mode 2

S1STA contains a status code which reflects the status of SIO1 and the I^2C bus. The three least significant bits are always zero. The five most significant bits contains the status code. There are 12 possible status code. When S1STA contains F8h, no relevant state information is available and no serial interrupt is requested. A valid status code is available in S1STA one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software. Table 7. to Table 9. give the status for the operating modes and miscellaneous states.

S1STA: Synchronous Serial Status Register

MSB			**SFR D9h**				**LSB**
SC4	SC3	SC2	SC1	SC0	0	0	0

Symbol	**Position**	**Name and Function**
SC0	S1STA.3	Status Code bit 0.
SC1	S1STA.4	Status Code bit 1.
SC2	S1STA.5	Status Code bit 2.
SC3	S1STA.6	Status Code bit 3.
SC4	S1STA.7	Status Code bit 4.

S1STA is a read only register. Its value after reset is F8h.

S1STA is using TSC8051C1 Special Function Register address, D9h.

Table 7. Status for master transmitter mode.

Status code	Status of I^2C bus and SIO1 hardware
08h	A START condition has been transmitted.
10h	A repeated START condition has been transmitted
18h	SLA+W has been transmitted; ACK has been received.
20h	SLA+W has been transmitted; NOT ACK has been received.
28h	Data byte has been transmitted; ACK has been received.
30h	Data byte has been transmitted; NOT ACK has been received.
38h	Arbitration lost in SLA+R/W or data bytes.

Table 8. Status for master receiver mode

Status code	Status of I^2C bus and SIO1 hardware
08h	A START condition has been transmitted.
10h	A repeated START condition has been transmitted.
38h	Arbitration lost in NOT ACK bit
40h	SLA+R has been transmitted; ACK has been received.
48h	SLA+R has been transmitted; NOT ACK has been received.
50h	Data byte has been received; ACK has been received.
58h	Data byte has been received; NOT ACK has been received.

Table 9. Status for miscellaneous states

Status code	Status of I^2C bus and SIO1 hardware
00h	Bus error.
F8h	No relevant state information available.

S1DAT contains a byte of serial data to be transmitted or a byte which has just been received. It is addressable while it is not in process of shifting a byte. This occurs when SIO1 is in a defined state and the serial interrupt flag is set. Data in S1DAT remains stable as long as SI is set. While data is being shifted out, data on the bus is simultaneously shifted in; S1DAT always contains the last byte present on the bus.

2

S1DAT: Synchronous Serial Data Register

MSB			SFR DAh				LSB
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0

Symbol	Position	Name and Function
SD0	S1DAT.0	Address bit 0 (R/$\overline{W}$) or Data bit 0.
SDX	S1DAT.X	Address bit X or Data bit X.

S1DAT is a read/write register. Its value after reset is 00h.

S1DAT is using TSC8051C1 Special Function Register address, DAh.

When SIO1 is enabled, P3.6 and P3.7 must be set to 1 to avoid low level asserting on SCL or SDA lines.

When SIO1 is used, external data memory access is not available.

8. Electrical Characteristics

Absolute Maximum Ratings(1)

Operating Temperature:
Commercial ..... 0°C to 70°C
Industrial ..... –40°C to +85°C

Storage Temperature ..... –65°C to +150°C

Voltage on VCC to VSS ..... –0.5V to +7V

Voltage on Any Pin to VSS .... –0.5V to VCC + 0.5V

Power Dissipation ..... 1W(2)

Notice:

1. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. *This value is based on the maximum allowable die temperate and the thermal resistance of the package.*

8.1. DC Characteristics

T_A = 0°C to +70°C; VSS = 0V; VCC = 5V ± 10%; F = 0 to 16MHz.

T_A = –40°C to +85°C; VSS = 0V; VCC = 5V ± 10%; F = 0 to 16MHz.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Inputs						
VIL	Input Low Voltage, except SCL, SDA	–0.5		0.2 Vcc – 0.1	V	
VIL1	Input Low Voltage, SCL, SDA(5)	–0.5		0.3 Vcc	V	
VIH	Input High Voltage except XTAL1, RST, SCL, SDA	0.2 Vcc + 0.9		Vcc + 0.5	V	
VIH1	Input High Voltage, XTAL1, RST	0.7 Vcc		Vcc + 0.5	V	
VIH2	Input High Voltage, SCL, SDA(5)	0.7 Vcc		Vcc + 0.5	V	
IIL	Logical 0 Input Current ports 1, 2 and 3			–50	µA	Vin = 0.45V
ILI	Input Leakage Current			±10	µA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current, ports 1, 2, 3			–650	µA	Vin = 2.0V
Outputs						
VOL	Output Low Voltage, ports 1, 2, 3, SCL, SDA, PWM0–7 (7)			0.3 0.45 1.0	V V V	IOL = 100µA(4) IOL = 1.6mA(4) IOL = 3.5mA(4)
VOL1	Output Low Voltage, port 0, ALE, $\overline{PSEN}$ (7)			0.3 0.45 1.0	V V V	IOL = 200µA(4) IOL = 3.2mA(4) IOL = 7.0mA(4)
VOH	Output High Voltage, ports 1, 2, 3, SCL, SDA	Vcc – 0.3 Vcc – 0.7 Vcc – 1.5			V V V	IOH = –10µA IOH = –30µA IOH = –60µA Vcc = 5V ± 10%
VOH1	Output High Voltage, port 0, ALE, $\overline{PSEN}$	Vcc – 0.3 Vcc – 0.7 Vcc – 1.5			V V V	IOH =–200µA IOH = –3.2mA IOH = –7.0mA Vcc = 5V ± 10%
RRST	RST Pulldown Resistor	50	90 (6)	200	kΩ	

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
CIO	Capacitance of I/O Buffer			10	pF	fc = 1MHz, TA = 25°C
ICC	Power Supply Current (8) Active Mode 12MHz Idle Mode 12MHz		 8.5 (6) 2.6 (6)	 17 8	 mA mA	 Vcc = 5.5V(1) Vcc = 5.5V(2)
IPD	Power Down Current		5 (6)	30	µA	Vcc = 2.0V to 5.5V(3)

Notes for DC Electrical Characteristics

1. ICC is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5 ns (see Figure 20.), VIL = VSS + 0.5V, VIH = VCC – 0.5V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = VCC. ICC would be slightly higher if a crystal oscillator used (see Figure 17.).
2. Idle ICC is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5ns, VIL = VSS + 0.5V, VIH = VCC–0.5V; XTAL2 N.C; Port 0 = VCC; $\overline{EA}$ = RST = VSS (see Figure 19.).
3. Power Down ICC is measured with all output pins disconnected; $\overline{EA}$ = PORT 0 = VCC; XTAL2 NC.; RST = VSS (see Figure 19.).
4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLs of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi VOL peak 0.6V. A Schmitt Trigger use is not necessary.
5. The input threshold voltage of SCL and SDA (SIO1) meets the I^2C specification, so an input voltage below 0.3·VCC will be recognised as a logic 0 while an input voltage above 0.7·VCC will be recognised as a logic 1.
6. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
7. Under steady state (non–transient) conditions, IOL must be externally limited as follows:
   Maximum IOL per port pin: 10 mA
   Maximum IOL per 8–bit port:
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total IOL for all output pins: 71 mA
   If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
8. For other values, please contact your sales office.

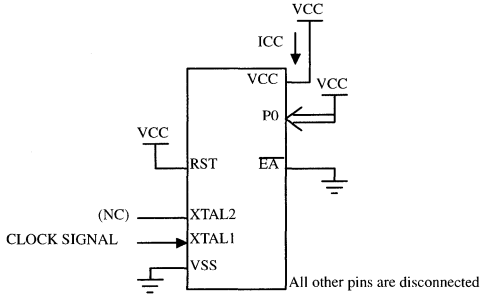


Figure 17. ICC Test Condition, Active Mode.

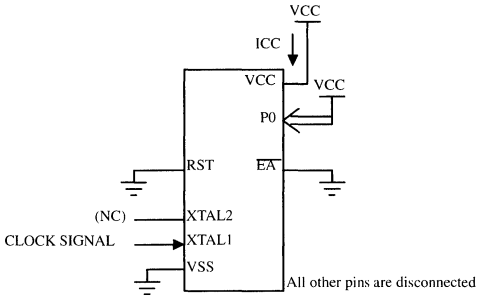


Figure 18. ICC Test Condition, Idle Mode.

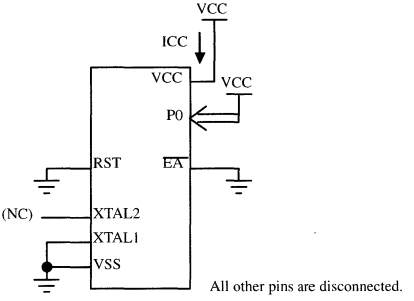


Figure 19. ICC Test Condition, Power Down Mode.

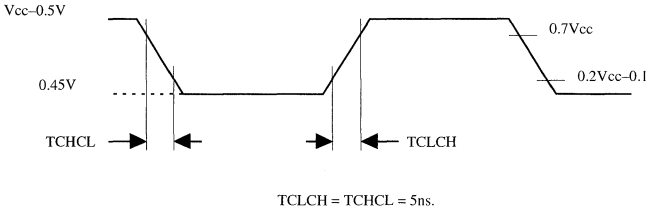


Figure 20. Clock Signal Waveform for ICC Tests in Active and Idle Modes.

8.2. Explanation Of The AC Symbol

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:

TAVLL = Time for Address Valid to ALE low.

TLLPL = Time for ALE low to PSEN low.

A: Address.	Q: Output data.
C: Clock.	R: READ signal.
D: Input data.	T: Time.
H: Logic level HIGH.	V: Valid.
I: Instruction (Program memory contents).	W: WRITE signal.
L: Logic level LOW, or ALE.	X: No longer a valid logic level.
P: PSEN.	Z: Float.

8.3. AC Parameters

T_A = 0 to +70°C; VSS = 0V VCC = 5V±10%; 0 to 12MHz

T_A = –40°C to +85°C; VSS = 0V; VCC = 5V ± 10%; F = 0 to 12MHz.

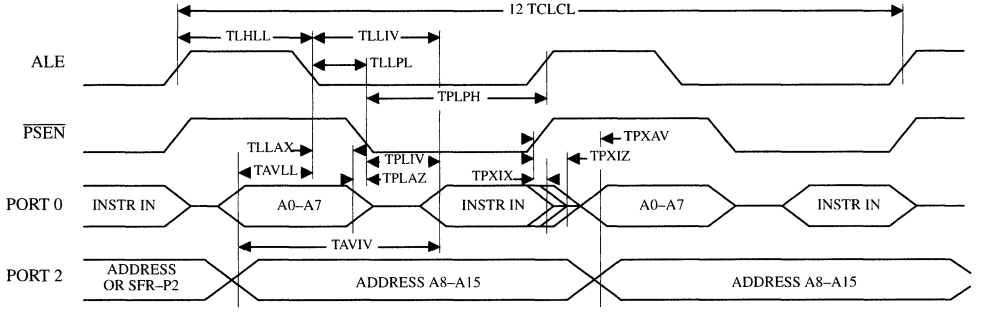
(Load Capacitance for PORT 0, ALE and PSEN = 100pf; Load Capacitance for all other outputs = 80 pF.)

8.4. External Program Memory Characteristics

Symbol	Parameter	0 to 12MHz		Units
		Min	Max	
TLHLL	ALE pulse width	2TCLCL – 40		ns
TAVLL	Address Valid to ALE	TCLCL – 40		ns
TLLAX	Address Hold After ALE	TCLCL – 30		ns
TLLIV	ALE to Valid Instruction In		4TCLCL – 100	ns
TLLPL	ALE to PSEN	TCLCL – 30		ns
TPLPH	PSEN Pulse Width	3TCLCL – 45		ns
TPLIV	PSEN to Valid Instruction In		3TCLCL – 105	ns
TPXIX	Input Instruction Hold After PSEN	0		ns

Symbol	Parameter	0 to 12MHz		Units
		Min	Max	
TPXIZ	Input Instruction Float After PSEN		TCLCL – 25	ns
TPXAV	PSEN to Address Valid	TCLCL – 8		ns
TAVIV	Address to Valid Instruction In		5TCLCL – 105	ns
TPLAZ	PSEN Low to Address Float		10	ns

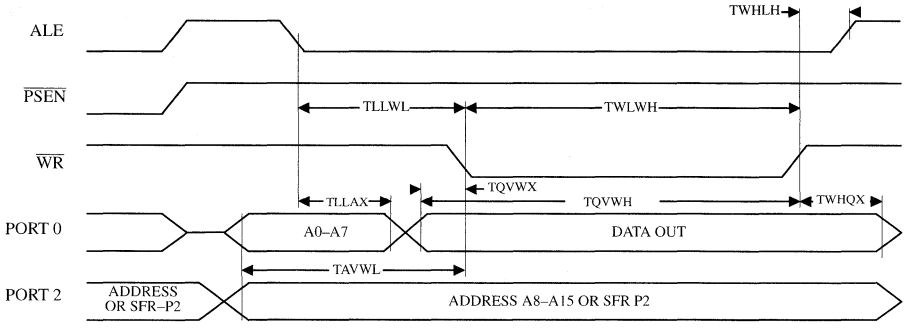
8.5. External Program Memory Read Cycle



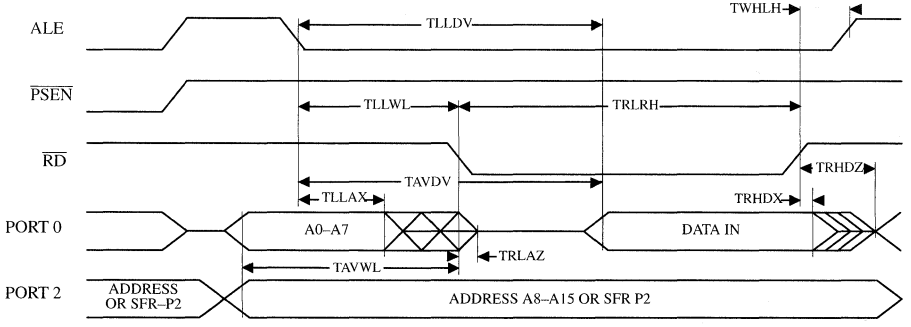
8.6. External Data Memory Characteristics

Symbol	Parameter	0 to 12MHz		Units
		Min	Max	
TRLRH	RD Pulse Width	6TCLCL–100		ns
TWLWH	WR Pulse Width	6TCLCL–100		ns
TRLDV	RD to Valid Data In		5TCLCL–165	ns
TRHDX	Data Hold After RD	0		ns
TRHDZ	Data Float After RD		2TCLCL–60	ns
TLLDV	ALE to Valid Data In		8TCLCL–150	ns
TAVDV	Address to Valid Data In		9TCLCL–165	ns
TLLWL	ALE to WR or RD	3TCLCL–50	3TCLCL+50	ns
TAVWL	Address to WR or RD	4TCLCL–130		ns
TQVWX	Data Valid to WR Transition	TCLCL–50		ns
TQVWH	Data set–up to WR High	7TCLCL–150		ns
TWHQX	Data Hold After WR	TCLCL–50		ns
TRLAZ	RD Low to Address Float		0	ns
TWHLH	RD or WR High to ALE high	TCLCL–40	TCLCL+40	ns

8.7. External Data Memory Write Cycle



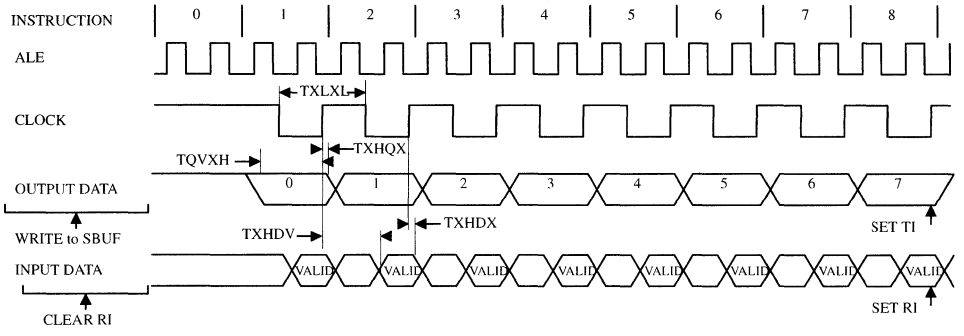
8.8. External Data Memory Read Cycle



8.9. Serial Port Timing–Shift Register Mode

Symbol	Parameter	0 to 12MHz		Units
		Min	Max	
TXLXL	Serial port clock cycle time	12TCLCL		ns
TQVHX	Output data set–up to clock rising edge	10TCLCL–133		ns
TXHQX	Output data hold after clock rising edge	2TCLCL–117		ns
TXHDX	Input data hold after clock rising edge	0		ns
TXHDV	Clock rising edge to input data valid		10TCLCL–133	ns

8.10. Shift Register Timing Waveforms

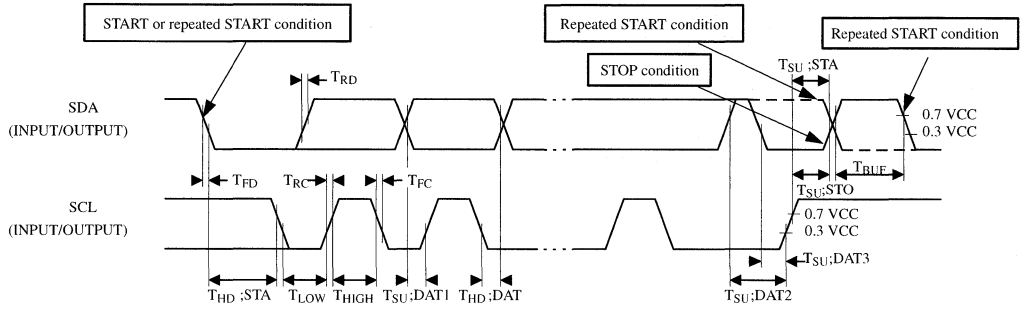


8.11. SIO1 (I^2C) Interface Timing

Symbol	Parameter	Input	Output
THD; STA	Start condition hold time	≥ 14 TCLCL	> 4.0µs (1)
TLOW	SCL low time	≥ 16 TCLCL	> 4.7µs (1)
THIGH	SCL high time	≥ 14 TCLCL	> 4.0µs (1)
TRC	SCL rise time	≤ 1µs	– (2)
TFC	SCL fall time	≤ 0.3µs	< 0.3µs (3)
TSU; DAT1	Data set–up time	≥ 250ns	> 20 TCLCL - TRD
TSU; DAT2	SDA set–up time (before repeated START condition)	≥ 250ns	> 1µs (1)
TSU; DAT3	SDA set–up time (before STOP condition)	≥ 250ns	> 8 TCLCL
THD; DAT	Data hold time	≥ 0ns	> 8 TCLCL - TFC
TSU; STA	Repeated START set–up time	≥ 14 TCLCL	> 4.7µs (1)
TSU; STO	STOP condition set–up time	≥ 14 TCLCL	> 4.0µs (1)
TBUF	Bus free time	≥ 14 TCLCL	> 4.7µs (1)
TRD	SDA rise time	≤ 1µs	– (2)
TFD	SDA fall time	≤ 0.3µs	< 0.3µs (3)

Notes:
1. At 100 kbit/s. At other bit–rates this value is inversely proportional to the bit–rate of 100 kbit/s.
2. Determined by the external bus–line capacitance and the external bus–line pull–up resistor, this must be < 1µs.
3. Spikes on the SDA and SCL lines with a duration of less than 3 TCLCL will be filtered out. Maximum capacitance on bus–lines SDA and SCL = 400pF.

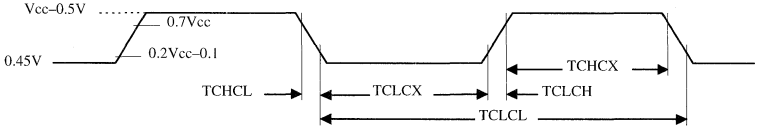
8.12. SIO1 (I^2C) Timing Waveforms



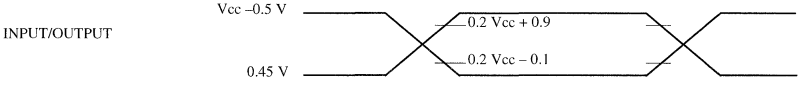
8.13. External Clock Drive Characteristics (XTAL1)

Symbol	Parameter	Min	Max	Units
TCLCL	Oscillator Period	83.3		ns
TCHCX	High Time	5		ns
TCLCX	Low Time	5		ns
TCLCH	Rise Time		5	ns
TCHCL	Fall Time		5	ns

8.14. External Clock Drive Waveforms

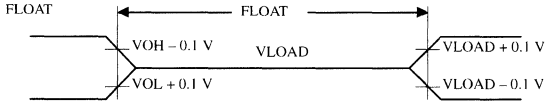


8.15. AC Testing Input/Output Waveforms



AC inputs during testing are driven at Vcc – 0.5 for a logic "1" and 0.45V for a logic "0". Timing measurement are made at VIH min for a logic "1" and VIL max for a logic "0".

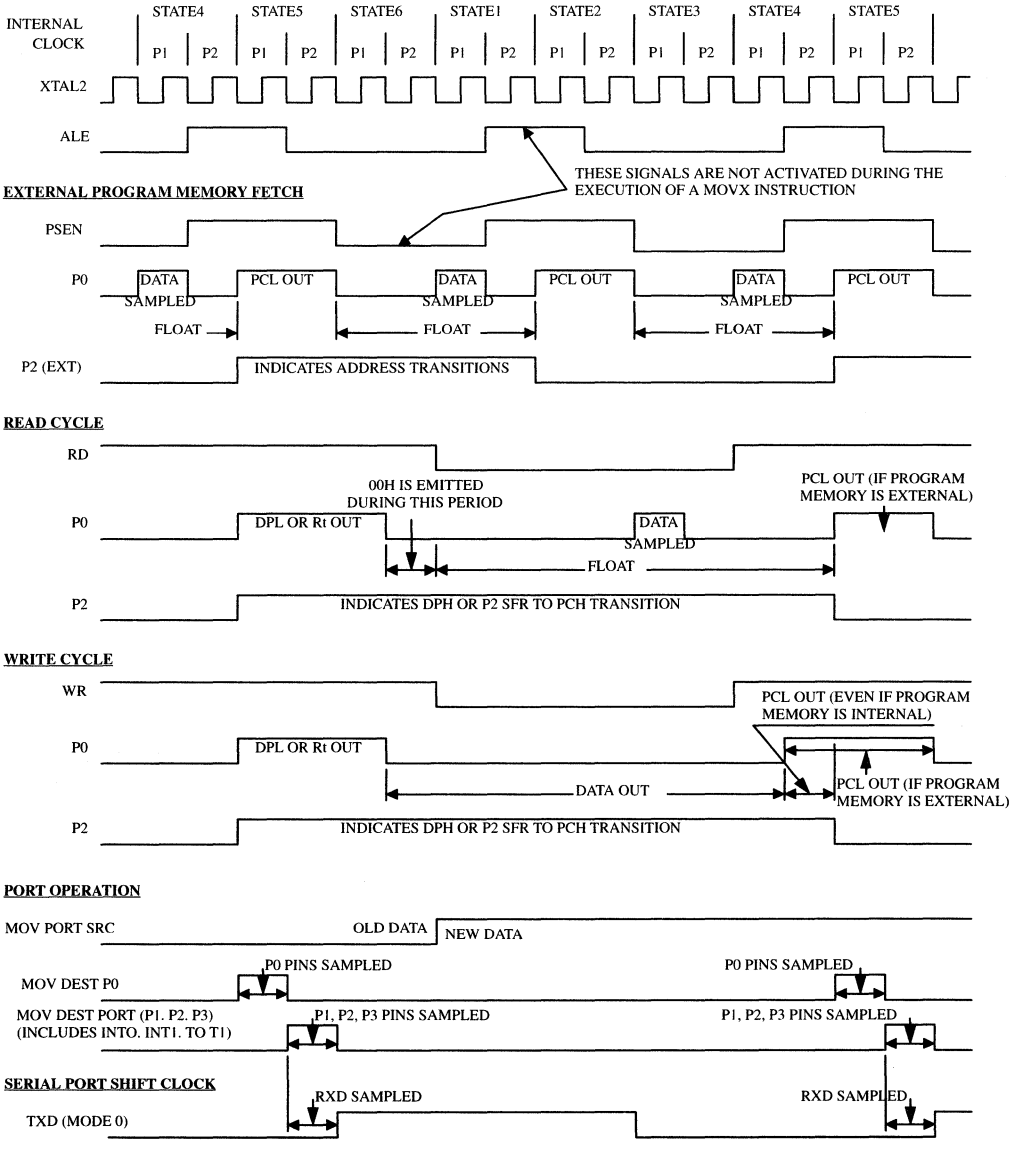
8.16. Float Waveforms



For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded VOH/VOL level occurs. IOL/IOH ≥ ± 20mA.

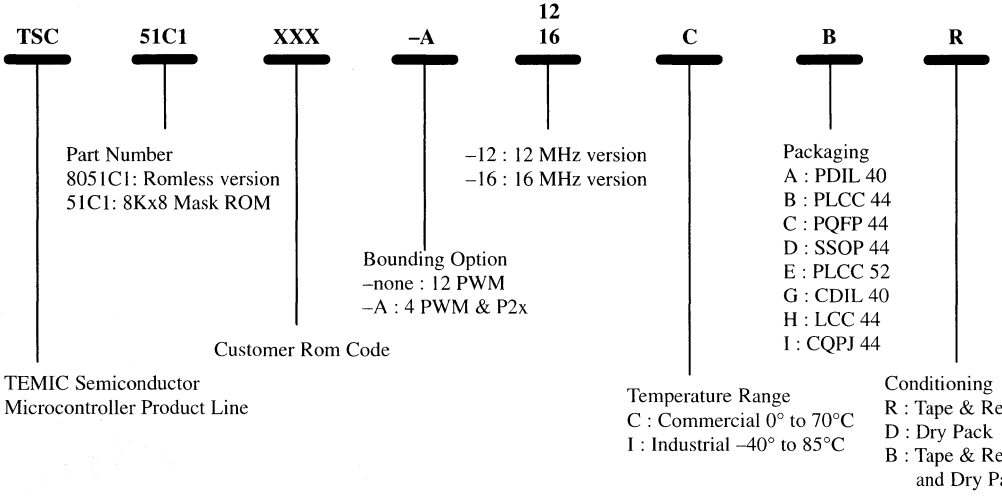
2

8.17. Clock Waveform



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A=25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50ns. The other signals are typically 85ns. Propagation delays are incorporated in the AC specifications.

9. Ordering Information



Examples

Part Number	Description
TSC51C1XXX–12CA	Mask ROM XXX, 12 MHz, PDIL 40, 0 to 70°C
TSC8051C1–16CER	ROMless, 16 MHz, PLCC 52, 0 to 70°C, Tape and Reel

Development Tools

Reference	Description
ANM059	Application Note: "How to recognize video mode and generate free running synchronization signals using TSC8051C1/C2 Microcontroller"
IM–80C51–RB–400–40	Emulator Base
PC–TSC8051C1–RB–16	Probe card for TSC8051C1. These products are released by Metalink. Please consult the local tools distributor or your sales office.

Product Marking :

TEMIC
Customer P/N
Temic P/N
© Intel 80, 82
YYWW Lot Number

TSC8051C2

8-Bit Microcontroller for Digital Computer Monitors

1. Introduction

The TSC8051C2 is a stand–alone high performance CMOS 8–bit embedded microcontroller and is designed for use in CRT monitors. It is also suitable for automotive and industrial applications.

The TSC8051C2 includes the fully static 8–bit "80C51" CPU core with 256 bytes of RAM; 4 Kbytes of ROM; two 16–bit timers; 12 PWM Channels; a 5 sources and 2–level interrupt controller; a full duplex serial port; a watchdog timer; power voltage monitor and on–chip oscillator.

In addition, the TSC8051C2 has 2 software selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the RAM, the timers, the serial ports, and the interrupt system continue to function. In the power down mode the RAM is saved and all other functions are inoperative.

The TSC8051C2 enables the users reducing a lot of external discrete components while bringing the maximum of flexibility.

2. Features

- Boolean processor
- Fully static design
- 4K bytes of ROM
- 256 bytes of RAM
- 2 x 16–bit timer/counter
- Programmable serial port
- 5 interrupt sources:
  - External interrupts (2)
  - Timers interrupt (2)
  - Serial port interrupt
- Watchdog reset
- Power Fail reset
- On chip oscillator for crystal or ceramic resonator
- 2 power saving control modes:
  - Idle mode
  - Power–down mode
- SYNC Processor
  - Controlled HSYNC & VSYNC outputs
  - Controlled HSYNC & VSYNC inputs
  - Clamp pulse output
- Up to 12 programmable PWM channels with 8–bit resolution
- Up to 32 programmable I/O lines depending on the package
- 40 pins DIP, 44 pins PQFP, 44 and 52 pins PLCC packages
- Commercial and industrial temperature ranges
- Operating Frequency: 12 MHz to 16 MHz

Preview

3. Block Diagram

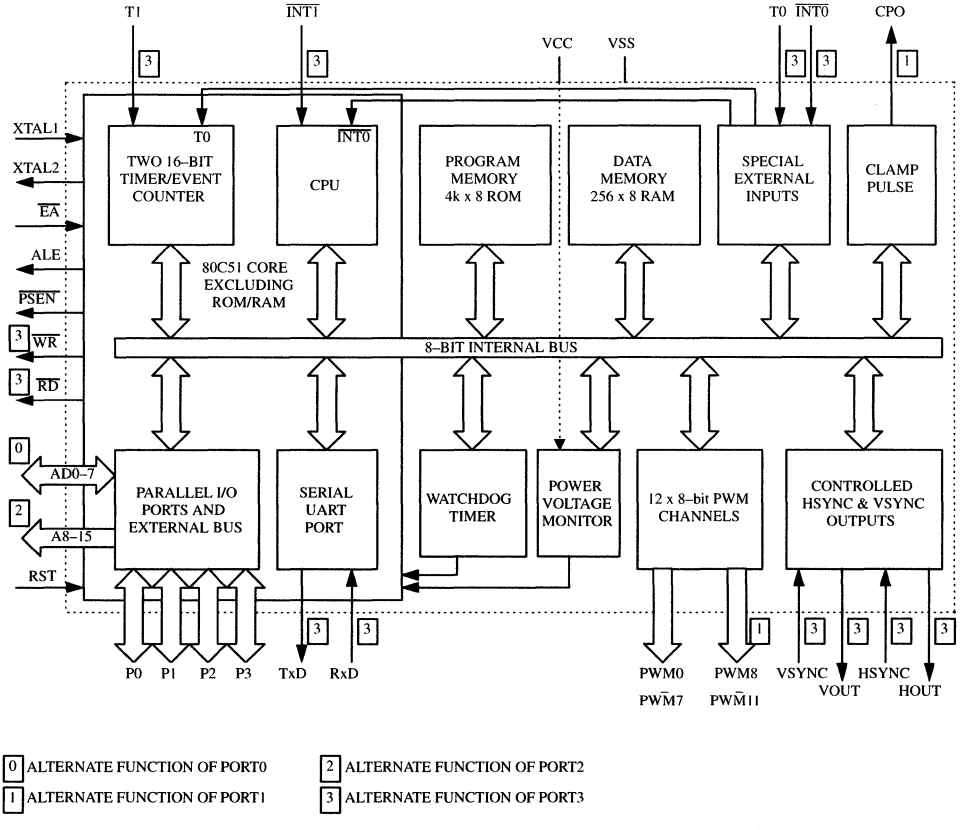
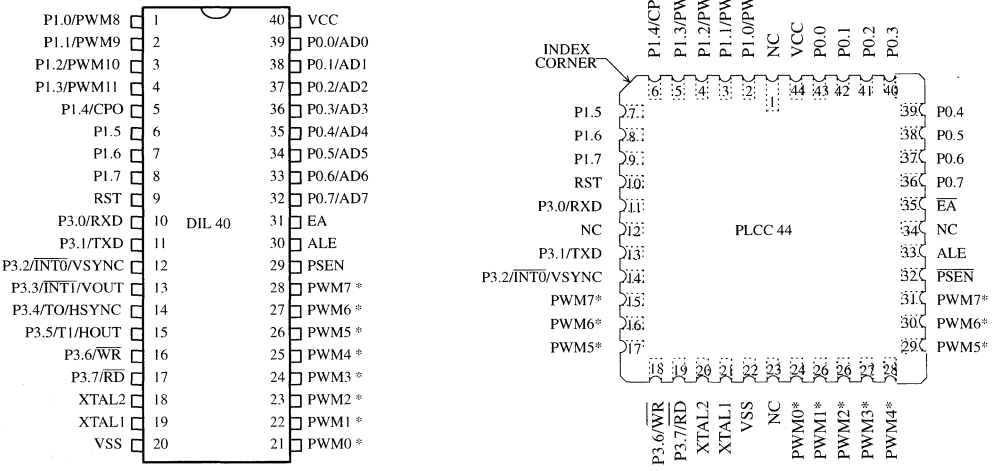


Figure 1. TSC8051C2 block diagram.

4. Pin Configurations



*PWMx or P2.x depending on option (see ordering information)

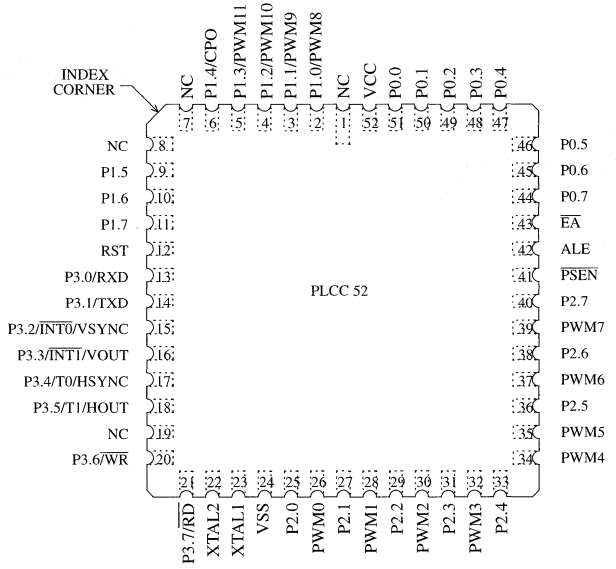


Figure 2. TSC8051C2 pin configurations.

5. Pin Description

VSS

Circuit ground.

VCC

Power supply voltage.

RST

A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal pulldown resistor permits power–on reset using only a capacitor connected to VCC.

PORT 0 (P0.0–P0.7)

Port 0 is an 8–bit open–drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high–impedance inputs.

Port 0 is also the multiplexed low–order address and data bus during access to external Program and Data memory. In this application it uses strong internal pull–up when emitting 1's.

Port 0 can sink and source 8 LS TTL loads.

PORT 1 (P1.0–P1.7)

Port 1 is an 8–bit bidirectional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL on the data–sheet) because of the internal pullups.

Port 1 also serves 4 programmable PWM open drain outputs and programmable open drain CPO, as listed below:

Port Pin	Alternate Function
P1.0	PWM8: Pulse Width Modulation output 8.
P1.1	PWM9: Pulse Width Modulation output 9.
P1.2	PWM10: Pulse Width Modulation output 10.
P1.3	PWM11: Pulse Width Modulation output 11.
P1.4	CPO: Clamp Pulse Output.

Port 1 can sink and source 3 LS TTL loads.

PORT 2 (P2.0–P2.7)

Port 2 is an 8–bit bidirectional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL on the data–sheet) because of the internal pullups.

Port 2 emits the high–order 8–bit address during fetches from external Program Memory and during accesses to external Data Memory that use 16–bit addresses. In this application it uses strong internal pull–up when emitting 1's.

Port 2 can sink and source 3 LS TTL loads.

PORT 3 (P3.0–P3.7)

Port 3 is an 8–bit bidirectional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL on the data–sheet) because of the internal pullups.

Each line on this port has 2 or 3 functions either a general I/O or special control signal, as listed below:

Port Pin	Alternate Function
P3.0	RXD: serial input port.
P3.1	TXD: serial output port.
P3.2	$\overline{INT0}$: external interrupt 0. VSYNC: vertical synchro input.
P3.3	$\overline{INT1}$: external interrupt 1. VOUT: buffered V-SYNC output.
P3.4	T0: Timer 0 external input. HSYNC: horizontal synchro input.
P3.5	T1: Timer 1 external input. HOUT: buffered H–SYNC output.
P3.6	$\overline{WR}$: external data memory write strobe.
P3.7	$\overline{RD}$: external data memory read strobe.

Port 3 can sink and source 3 LS TTL loads.

PWM0–7

These eight Pulse Width Modulation outputs are true open drain outputs and are floating after reset.

ALE

The Address Latch Enable output signal occurs twice each machine cycle except during external data memory access. The negative edge of ALE strobes the address into external data memory or program memory. ALE can sink and source 8 LS TTL loads.

If desired, ALE operation can be disabled by setting bit 0 of SFR location AFh (MSCON). With the bit set, ALE is active only during MOVX instruction and external fetches. Otherwise the pin is pulled low.

$\overline{EA}$

When the External Access input is held high, the CPU executes out of internal program memory (unless the Program Counter exceeds 1FFFh). When $\overline{EA}$ is held low the CPU executes only out of external program memory. must not be left floating.

$\overline{PSEN}$

The Program Store Enable output signal remains high during internal program memory. An active low output occurs during an external program memory fetch. $\overline{PSEN}$ can sink and source 8 LS TTL loads.

XTAL1

Input to the inverting oscillator amplifier and input to the external clock generator circuits.

XTAL2

Output from the inverting oscillator amplifier. This pin should be non–connected when external clock is used.

6. Basic Functional Description

6.1. Idle And Power Down Operation

Figure 3 shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. Idle mode operation allows the interrupt, serial port, and timer blocks to continue to operate while the clock to the CPU is gated off.

These special modes are activated by software via the Special Function Register, its hardware address is 87h. PCON is not bit addressable.

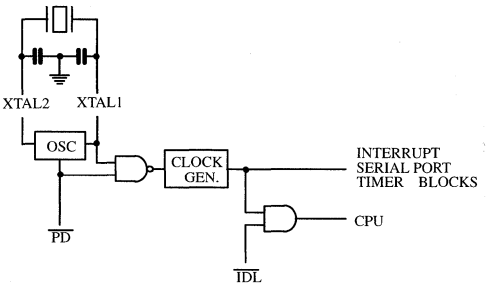


Figure 3. Idle and Power Down Hardware.

PCON: Power Control Register

MSB			SFR 87h				LSB
SMOD	–	–	PFRE	GF1	GF0	PD	IDL

Symbol	Position	Name and Function
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
GF0	PCON.2	General–purpose flag bit.
GF1	PCON.3	General–purpose flag bit.
PFRE	PCON.4	Power Fail Reset Enable bit. Setting this bit enables the power voltage monitor. The only way to clear this bit is to apply an external reset.
–	PCON.5	(Reserved).
–	PCON.6	(Reserved).
SMOD	PCON.7	Double Baud rate bit. Setting this bit causes the baud rate to double when the serial port is being used in either modes 1, 2 or 3.

If 1's are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is 0XX0 0000b.

6.1.1. Idle Mode

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM, and all other register maintain their data during Idle Table 1 describes the status of the external pins during Idle mode.

There are two ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

6.1.2. Power Down Mode

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register are saved during power down mode. A hardware reset is the only way of exiting the power down mode. The hardware reset initiates the Special Function Register. In the Power Down mode, VCC may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the power down mode is entered, and that the voltage is restored before the hardware reset is applied which frees the oscillator. Reset should not be released until the oscillator has restarted and stabilized. Table 1 describes the status of the external pins while in the power down mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a 1, the port pin is held high during the power down mode by the strong pullup transistor.

Table 1. Status of the external pins during Idle and Power Down modes.

Mode	Program Memory	ALE	PSEN	Port 0	Port 1	Port 2	Port 3	PWMx
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data	Floating
Idle	External	1	1	Floating	Port Data	Address	Port Data	Floating
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data	Floating
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data	Floating

6.2. Stop Clock Mode

Due to static design, the TSC8051C2 clock speed can be reduced down to 0 MHz without any data loss in memory or register. This mode allows step by step code execution, and permits to reduce system power consumption by bringing the clock frequency down to any value. When the clock is stopped, the power consumption is the same as in the Power Down Mode.

6.3. I/O Ports Structure

The TSC8051C2 has four 8–bit ports. Each port consist of a latch (special function register P0 to P3), an input buffer and an output driver. These ports are the same as in 80C51, with the exception of the additional functions of port 1 and port 3 (see Pin Description section).

6.4. I/O Configurations

Figure 4. shows a functional diagram of the generic bit latch and I/O buffer in each of the four ports. The bit latch, (one bit in the port SFR) is represented as a D type flip–flop. A 'write to latch' signal from the CPU latches a bit from the internal bus and a 'read latch' signal from the CPU places the Q output of the flip–flop on the internal bus. A 'read pin' signal from the CPU places the actual pin logical level on the internal bus.
Some instructions that read a port read the actual pin, and other instructions read the latch (SFR).

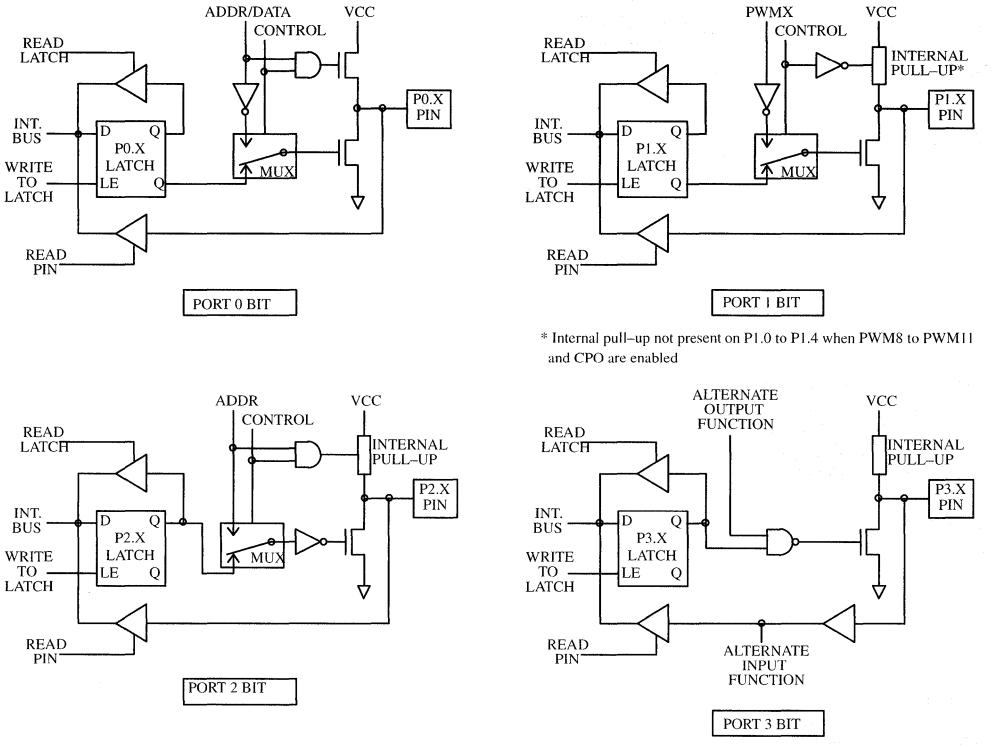


Figure 4. Port Bit Latches and I/O buffers

6.5. Reset Circuitry

The reset circuitry for the TSC8051C2 is connected to the reset pin RST. A Schmitt trigger is used at the input for noise rejection (see Figure 5.).

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods) while the oscillator is running. The CPU responds by executing an internal reset. It also configures the ALE and PSEN pins as inputs (they are quasi–bidirectional). A Watchdog timer underflow or a power Fail condition if enabled, will force a reset condition to the TSC8051C2 by an internal connection.
The internal reset is executed during the second cycle in which reset is high and is repeated every cycle until RST goes low. It leaves the internal registers as follows:

Register	Content
ACC	00h
B	00h
DPTR	0000h
EICON	00h
HWDR	00h
IE	0XX0 0000b
IP	XXX0 0000b
MSCON	XXXX XXX0b
MXCR0–1	00h
P0–P3	FFh
PC	0000h
PCON	0XX0 0000b
PSW	00h
PWM0–11	00h
PWMCON	XXXX XXX0b
SBUF	00h

Register	Content
SCON	00h
SOCR	00h
SP	07h
TCON	00h
TH0, TH1	00h
TL0, TL1	00h
TMOD	00h

The internal RAM is not affected by reset. At power–on reset, the RAM content is indeterminate.

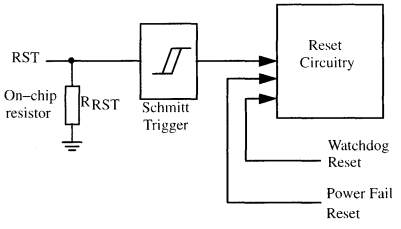


Figure 5. On–Chip Reset Configuration.

An automatic reset can be obtained when VCC is turned on by connecting the RST pin to VCC through a 1µF capacitor providing the VCC setting time does not exceed 1ms and the oscillator start–up time does not exceed 10ms. This power–on reset circuit is shown in Figure 6. When power comes on, the current drawn by RST starts to charge the capacitor. The voltage at RST is the difference between VCC and the capacitor voltage, and decreases from VCC as the capacitor charges. VRST must remain above the lower threshold of the Schmitt trigger long enough to effect a complete reset. The time required is the oscillator start–up time, plus 2 machine cycles.

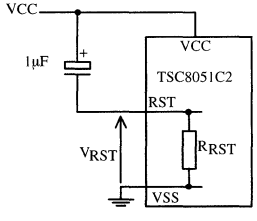


Figure 6. Power–on Reset Circuit

6.6. Oscillator Characteristics

XTAL1 and XTAL2 are respectively the input and output of an inverting amplifier which is configured for use as an on–chip oscillator. As shown in Figure 7. , either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in Figure 8.

There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide–by–two flip–flop. The minimum high and low times specified on the data sheet must be observed however.

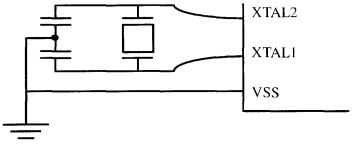


Figure 7. Crystal Oscillator

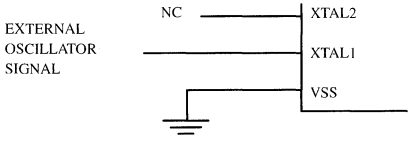


Figure 8. External Drive Configuration

6.7. Memory organization

The memory organisation of the TSC8051C2 is the same as in the 80C51, with the exception that the TSC8051C2 has 4k bytes ROM, 256 bytes RAM, and additional SFRs. Details of the differences are given in the following paragraphs.

In the TSC8051C2, the lowest 4k of the 64k program memory address space is filled by internal ROM. Depending on the package used, external access is available or not. By tying the $\overline{EA}$ pin high, the processor fetches instructions from internal program ROM. Bus expansion for accessing program memory from 4k upward is automatic since external instruction fetches occur automatically when the program counter exceeds 1FFFh. If the $\overline{EA}$ pin is tied low, all program memory fetches are from external memory. The execution speed is the same regardless of whether fetches are from external or internal program memory. If all storage is on–chip, then byte location 0FFFh should be left vacant to prevent an undesired pre–fetch from external program memory address 1000h.

Certain locations in program memory are reserved for specific purposes. Locations 0000h to 0002h are reserved for the initialisation program. Following reset, the CPU always begins execution at location 0000h. Locations 0003h to 002Ah are reserved for the five interrupt request service routines.

The internal data memory space is divided into a 256–bytes internal RAM address space and a 128 bytes special function register address space.

The internal data RAM address space is 0 to FFh. Four 8–bit register banks occupy locations 0 to 1Fh. 128 bit locations of the internal data RAM are accessible through direct addressing. These bits reside in 16 bytes of internal RAM at location 20h to 2Fh. The stack can be located anywhere in the internal data RAM address space by loading the 8–bit stack pointer (SP SFR).

The SFR address space is 100h to 1FFh. All registers except the program counter and the four 8–bit register banks reside in this address space. Memory mapping of the SFRs allows them to be accessed as easily as internal RAM, and as such, they can be operated on by most instructions.The mapping in the SFR address space of the 40 SFRs is shown in Table 2. The SFR names in italic are TSC8051C2 new SFRs and are described in Peripherals Functional Description section. The SFR names in bold are bit addressable.

Table 2. Mapping of Special Function Register

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
F8					*PWM8*	*PWM9*	*PWM10*	*PWM11*
F0	**B**				*PWM4*	*PWM5*	*PWM6*	*PWM7*
E8					*PWM0*	*PWM1*	*PWM2*	*PWM3*
E0	**ACC**				*EICON*	*SOCR*	*HWDR*	*MXCR0*
D8								*PWMCON*
D0	**PSW**							*MXCR1*
C8								
C0								
B8	**IP**							
B0	**P3**							
A8	**IE**							MSCON
A0	**P2**							
98	**SCON**	SBUF						
90	**P1**							
88	**TCON**	TMOD	TL0	TL1	TH0	TH1		
80	**P0**	SP	DPL	DPH				PCON

6.8. Interrupts

The TSC8051C2 has five interrupt sources, each of which can be assigned one of two priority levels. These five interrupt sources are common to the 80C51 and are the external interrupts (INT0 and INT1), the timer 0 and timer 1 interrupts (IT0 and IT1), and the serial I/O interrupt (RI or TI).

6.8.1. Interrupt Enable Register:

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable register (IE SFR). All interrupts sources can also be globally enabled or disabled by setting or clearing the EA bit in IE register.

IE: Interrupt Enable Register

MSB			SFR A8h				LSB
EA	–	–	ES	ET1	EX1	ET0	EX0

Symbol	Position	Name and Function
EX0	IE.0	Enable external interrupt 0.
ET0	IE.1	Enable timer 0 interrupt.
EX1	IE.2	Enable external interrupt 1.
ET1	IE.3	Enable timer 1 interrupt.
ES	IE.4	Enable UART interrupt.
–	IE.5	(Reserved).
–	IE.6	(Reserved).
EA	IE.7	Enable all interrupts.

6.8.2. Interrupt Priority Structure:

Each interrupt source can be assigned one of two priority levels. Interrupt priority levels are defined by the interrupt priority register (IP SFR). Setting a bit in the interrupt priority register selects a high priority interrupt, clearing it selects a low priority interrupt.

IP: Interrupt Priority Register

MSB			SFR B8h				LSB
–	–	–	PS	PT1	PX1	PT0	PX0

Symbol	Position	Name and Function
PX0	IP.0	External interrupt 0 priority level.
PT0	IP.1	Timer 0 interrupt priority level.
PX1	IP.2	External interrupt 1 priority level.
PT1	IP.3	Timer 1 interrupt priority level.
PS	IP.4	UART interrupt priority level.
–	IP.5	(Reserved).
–	IP.6	(Reserved).
–	IP.7	(Unused).

Preview

A low priority interrupt service routine may be interrupted by a high priority interrupt. A high priority interrupt service routine cannot be interrupted by any other interrupt source.

If two requests of different priority levels occur simultaneously, the high priority level request is serviced. If requests of same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus, within each priority level, there is a second priority structure determined by the polling sequence, as follows:

Order	Source	Priority Within Level
1	INT0	(highest)
2	Timer 0	↑
3	INT1	
4	Timer 1	↓
5	UART	(lowest)

6.8.3. Interrupt Handling:

The interrupt flags are sampled at S5P2 of every machine cycle. The samples are polled during the following machine cycle. If one of the flags was in a set condition at S5P2 of the previous machine cycle, the polling cycle will find it and the interrupt system will generate a LCALL to the appropriate service routine, provided this hardware–generated LCALL is not blocked by any of the following conditions:

1. An interrupt of higher or equal priority is already in progress.
2. The current (polling) cycle is not the final cycle in the execution of the instruction in progress.
3. The instruction in progress is RETI or any access to the IE or IP SFR.

Any of these three conditions will block the generation of the LCALL to the interrupt service routine. Note that if an interrupt is active but not being responded to for one of the above conditions, if the flag is not still active when the blocking condition is removed, the denied interrupt will not be serviced. In other words, the facts that the interrupt flag was once active but not serviced is not memorized. Every polling cycle is new.

The processor acknowledges an interrupt request by executing a hardware–generated LCALL to the appropriate service routine. In some cases it also clears the flag that generated the interrupt, and in other case it does not. It clears the timer 0, timer 1, and external interrupt flags. An external interrupt flag (IE0 or IE1) is cleared only if it was transition–activated. All other interrupt flags are not cleared by hardware and must be cleared by the software. The LCALL pushes the contents of the program counter onto the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to, as listed below:

Source	Vector Address
IE0	0003h
TF0	000Bh
IE1	0013h
TF1	001Bh
RI + TI	0023h

Execution proceeds from the vector address until the RETI instruction is encountered. The RETI instruction clears the 'priority level active' flip–flop that was set when this interrupt was acknowledged. It then pops two bytes from the the top of the stack and reloads the program counter with them. Execution of the interrupted program continues from where it was interrupted.

7. Peripherals Functional Description

For detailed functionnal description of standard 80C51 peripherals, please refer to C51 Family, Hardware Description and Programmer's Guides.

7.1. Watchdog Timer

The watchdog timer consists of a 4–bit timer with a 17–bit prescaler as shown in Figure 9. The prescaler is fed with a signal whose frequency is 1/12 the oscillator frequency (1MHz with a 12MHz oscillator).

The 4–bit timer is decremented every 't' seconds, where: t = 12 x 131072 x 1/fosc. (131.072ms at fosc = 12MHz). Thus, the interval may vary from 131.072ms to 2097.152ms in 16 possible steps (see Table 3.).

The watchdog timer has to be reloaded (write to HWDR SFR) within periods that are shorter than the programmed watchdog interval, otherwise the watchdog timer will underflow and a system reset will be generated which will reset the TSC8051C2.

HWDR: Hardware WatchDog Register

MSB			SFR E6h				LSB
WTE	–	–	–	WT3	WT2	WT1	WT0

Symbol	Position	Name and Function
WT0	HWDR.0	Watchdog Timer Interval bit 0.
WT1	HWDR.1	Watchdog Timer Interval bit 1.
WT2	HWDR.2	Watchdog Timer Interval bit 2.
WT3	HWDR.3	Watchdog Timer Interval bit 3.
–	HWDR.4	Reserved for test purpose, must remain to 0 for normal operation.
–	HWDR.5	(Reserved).
–	HWDR.6	(Reserved).
WTE	HWDR.7	Watchdog Timer Enable bit. Setting this bit activates watchdog operation.

Table 3. Watchdog timer interval value format.

WT3	WT2	WT1	WT0	Interval
0	0	0	0	t x 16
0	0	0	1	t x 1
0	0	1	0	t x 2
:	:	:	:	:
:	:	:	:	:
1	1	1	1	t x 15

Once the watchdog timer enabled setting WTE bit, it cannot be disabled anymore, except by a system reset.

The watchdog timer is frozen during idle or power down mode.

HWDR is a write only register. Its value after reset is 00h which disables the watchdog operation.

HWDR is using TSC8051C2 Special Function Register address, E6h.

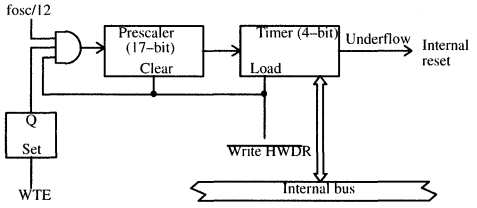


Figure 9. Watchdog timer block diagram

7.2. Power Fail Reset

The TSC8051C2 implements a programmable power fail reset mechanism that avoids the microcontroller running while V_{CC} is under working voltage (see Figure 10.). This system generates an internal reset when V_{CC} falls: during V_{CC} failure or power supply switch off.

When V_{CC} falls below V_{LOW} (see DC Electricals Characteristics), reset is asserted and maintained until power supply is completely off. If V_{CC} rises above V_{LOW}, reset is maintained during at least 2 machine cycles to be well detected by the CPU core. To avoid spurious reset, power glitches of pulses width less than 2 to 3 f_{OSC} periods are filtered out (see Figure 11.).

The PFR must be enabled by setting PFRE bit in PCON register bit location 4 (see Idle and Power Donwn Operation section).

The PFR is disable during Idle and power down modes. Since it is enabled, PFR can no longer be disabled by software. Writing 0 to PFRE bit has no effect, the only way to clear the PFRE bit is to apply an external reset. To avoid period during which PFR is disabled, internal reset sources do not disable PFR.

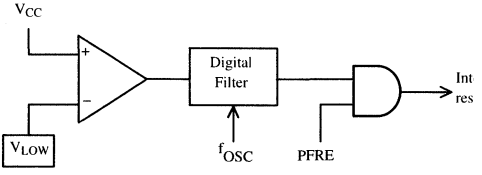


Figure 10. Power–Fail Reset block diagram

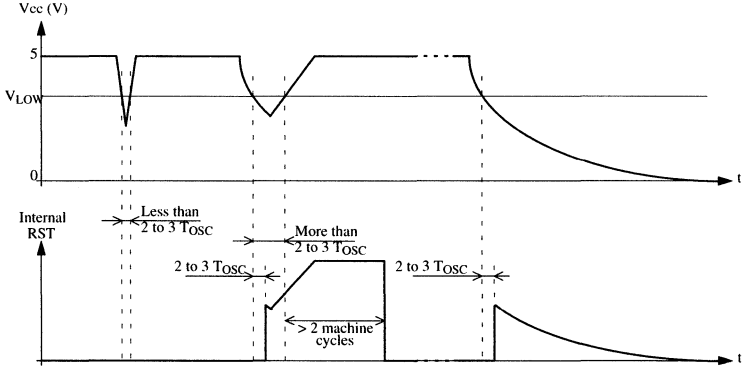


Figure 11. Power Fail Reset timing diagram

7.3. Pulse Width Modulated Outputs

The TSC8051C2 contains twelve pulse width modulated output channels (see Figure 10.). These channels generate pulses of programmable duty cycle with an 8–bit resolution.

The 8–bit counter counts modulo 256 by default i.e., from 0 to 255 inclusive but can count modulo 254 i.e., from 0 to 253 inclusive by programming the bit 0 of the PWMCON register. The counter clock is supplied by the oscillator frequency. Thus, the repetition frequency fpwm is constant and equals to the oscillator frequency divided by 256 or 254 (fpwm=46.875KHz or 47.244KHz with a 12MHz oscillator). The 8–bit counter is common to all PWM channels, its value is compared to the contents of the twelve registers: PWM0 to PWM11. Provided the content of each of these registers is greater than the counter value, the corresponding output is set low. If the contents of these registers are equal to, or less than the counter value the output will be high.

The pulse–width ratio is therefore defined by the contents of these registers, and is in the range of 0 (all '0' written to PWM register) to 255/256 or 1 (all '1' written to PWM register) and may be programmed in increments of 1/256 or 1/254. When the 8–bit counter counts modulo 254, it can never reach the value of the PWM registers when they are loaded with FEh or FFh.

PWMx: Pulse Width Modulator x Register

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

When a compare register (PWM0 to PWM11) is loaded with a new value, the associated output is updated immediately. It does not have to wait until the end of the current counter period. All the PWM outputs are open–drain outputs with standard current drive and standard maximum voltage capability. When they are disabled, eight of them (PWM0 to PWM7) are in high impedance while the other four (PWM8 to PWM11) are standard Port outputs with internal pullups.

PWM0 to PWM11 are write only registers. Their value after reset is 00h.

PWM0 to PWM11 are using TSC8051C2 Special Function Registers addresses as detailed in Table 4.

Table 4. PWM SFR register addresses

Channel	SFR address
PWM0	ECh
PWM1	EDh
PWM2	EEh
PWM3	EFh
PWM4	F4h
PWM5	F5h
PWM6	F6h
PWM7	F7h
PWM8	FCh
PWM9	FDh
PWM10	FEh
PWM11	FFh

Two 8–bit control registers: MXCR0 and MXCR1 are used to enable or disable PWM outputs.

MXCR0 is used for PWM0 to PWM7. MXCR1 is used for PWM8 to PWM11, these PWMs are multiplexed with PORT 1 (see Table 5.)

MXCR0: PWM Multiplexed Control Register 0

MSB			SFR E7h				LSB
PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0

Symbol	Position	Name and Function
PEx	MXCR0.x	PWM_X Enable bit. Setting this bit enables PWMx output. Clearing this bit disables PWMx output.

MXCR1: PWM Multiplexed Control Register 1

MSB			SFR D7h				LSB
–	–	–	–	PE11	PE10	PE9	PE8

Symbol	Position	Name and Function
PEx	MXCR1.x	PWM_{X+8} Enable bit. Setting this bit enables PWMx output. Clearing this bit disables PWMx output and activates the I/O pin (see Table 5).

MXCR0 and MXCR1 are read/write registers. Their value after reset is 00h which corresponds to all PWM disabled.

PWM will not operate in idle and power down modes (frozen counter). When idle or power down mode is entered, the PWM0 to PWM7 output pins are floating and PWM8 to PWM11 pins are set to general purpose P1 port with the value of P1 SFR.

MXCR0 and MXCR1 are using TSC8051C2 Special Function Register addresses, E7h and D7h respectively.

Table 5. PWM alternate pin.

Channel	Pin assignment
PWM8	P1.0
PWM9	P1.1
PWM10	P1.2
PWM11	P1.3

PWMCON is used to control the PWM counter.

PWMCON: PWM Control Register

MSB			SFR DFh				LSB
–	–	–	–	–	–	–	CMOD

Symbol	Position	Name and Function
CMOD	PWMCON.0	Counter modulo. Setting this bit sets the modulo to 254. Clearing this bit sets the modulo to 256.

PWMCON is a write only register. Its value after reset is 00h which sets the PWM counter modulo to 256.

PWMCON is using TSC8051C2 Special Function Register address, DFh.

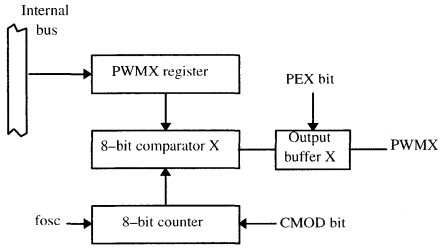


Figure 12. Pulse width modulated outputs block diagram

Figure 13. shows a PWM programming example with PWM register content 55h and counter modulo 256.

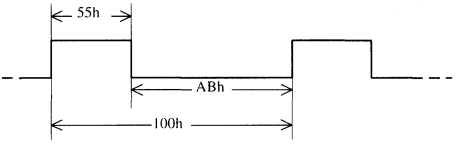


Figure 13. PWM programming example.

Note: when packaging P2.X is selected, PWM0 to PWM7 are not available. Please refer to ordering information.

2

7.4. SYNC Processor

7.4.1. HSYNC and VSYNC Outputs

SOCR is used to configure P3.3 and P3.5 pins as buffered HSYNC and VSYNC outputs or as general purpose I/Os. When either HSYNC or VSYNC is selected, the output level can be respectively programmed as P3.4 or P3.2 input level (inverted or not), or as a low level if not enabled. Figure 14. shows the programmable HSYNC and VSYNC output block diagram.

SOCR: Synchronisation Output Control Register.

MSB		SFR E5h					LSB
–	–	VOS	HOS	VOP	VOE	HOP	HOE

Symbol	Position	Name and Function
HOE	SOCR.0	HSYNC Output Enable bit. Setting this bit enables the HSYNC signal.
HOP	SOCR.1	HSYNC Output Polarity bit. Setting this bit inverts the HSYNC output.
VOE	SOCR.2	VSYNC Output Enable bit. Setting this bit enables the VSYNC signal.
VOP	SOCR.3	VSYNC Output Polarity bit. Setting this bit inverts the VSYNC output.
HOS	SOCR.4	HSYNC Output Selection bit. Setting this bit selects the VSYNC output, clearing it selects P3.5 SFR bit.
VOS	SOCR.5	VSYNC Output Selection bit. Setting this bit selects the VSYNC output, clearing it selects P3.3 SFR bit.
CPE	SOCR.6	Clamp Pulse Enable bit. Setting this bit enables the CPO output.
CPP	SOCR.7	Clamp Pulse Polarity bit. Setting this bit selects positive clamp pulses, clearing it selects negative clamp pulses.

SOCR is a write only register. Its value after reset is 00h which enables P3.3 and P3.5 general purpose I/O pins.

SOCR is using TSC8051C2 Special Function Register address, E5h.

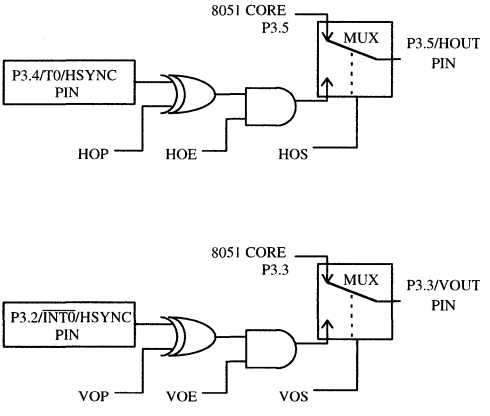


Figure 14. Buffered HSYNC and VSYNC block diagram

7.4.2. HSYNC and VSYNC Inputs

EICON is used to control $\overline{INT0}$VSYNC input. Thus, an interrupt on either falling or rising edge and on either high or low level can be requested. Figure 15. shows the programmable $\overline{INT0}$/VSYNC input block diagram.

EICON is also used to control T0/HSYNC input as short pulses input capture to be able to count them with timer 0. Pulse duration shorter than 1 clock period is rejected; depending on the position of the sampling point in the pulse, pulse duration longer than 1 clock period and shorter than 1.5 clock period may be rejected or accepted; and pulse duration longer than 1.5 clock period is accepted. Moreover selection of negative or positive pulses can be programmed.

Accepted pulse is lengthened up to 1 cycle period to be sampled by the 8051 core (one time per machine cycle: 12 clock periods), this implies that the maximum pulse frequency is unchanged and equal to $f_{OSC}/24$. Figure 16. shows the programmable T0/HSYNC input block diagram. The Digital Timer Delay samples T0/HSYNC pulses and rejects or lengthens them.

EICON: External Input Control Register

MSB			SFR E4h				LSB
-	-	-	-	-	T0L	T0S	I0L

Symbol	Position	Name and Function
I0L	EICON.0	$\overline{INT0}$/VSYNC input Level bit. Setting this bit inverts $\overline{INT0}$/VSYNC input signal. Clearing it allows standard use of $\overline{INT0}$/VSYNC input.
T0S	EICON.1	T0/HSYNC input Selection bit. Setting this bit allows short pulse capture. Clearing it allows standard use of T0/HSYNC input.
T0L	EICON.2	T0/HSYNC input Level bit. Setting this bit allows positive pulse capture. Clearing it allows negative pulse capture.

EICON is a write only register. Its value after reset is 00h which allows standard $\overline{INT0}$ and T0 inputs feature.

EICON is using TSC8051C2 Special Function Register address, E4h.

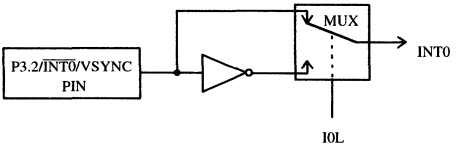


Figure 15. $\overline{INT0}$/VSYNC input block diagram

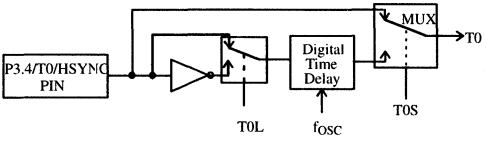


Figure 16. T0/HSYNC input block diagram

7.4.3. Clamp Pulse Output

The TSC8051C2 provides fully programmable clamp pulse output to pre–amplifier IC. User can program a pulse with positive or negative polarity at either the falling or rising edge of the HSYNC signal depending on its polarity.

Figure 17. shows the CPO block diagram. CPE bit in SOCR is used to configure P1.4 pin as general purpose I/O or as open drain clamp pulse output, so enables the CPO. CPP bit in SOCR is used to select the clamp pulse signal polarity. Depending on the HSYNC polarity selected by the T0L bit, Clamp pulse is generated on the falling edge (negative polarity) or on the rising edge (positive polarity) as shown in Figure 18.

The clamp pulse duration depends on the oscillator frequency by the following formula:

$$T_{CPO} = (1/f_{OSC}) \times 7.5 \pm (1/f_{OSC})/2$$

(542ns $\pm$ 42ns at f_{OSC} = 12 MHz)

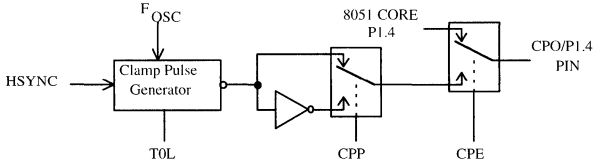


Figure 17. Clamp Pulse Output block diagram

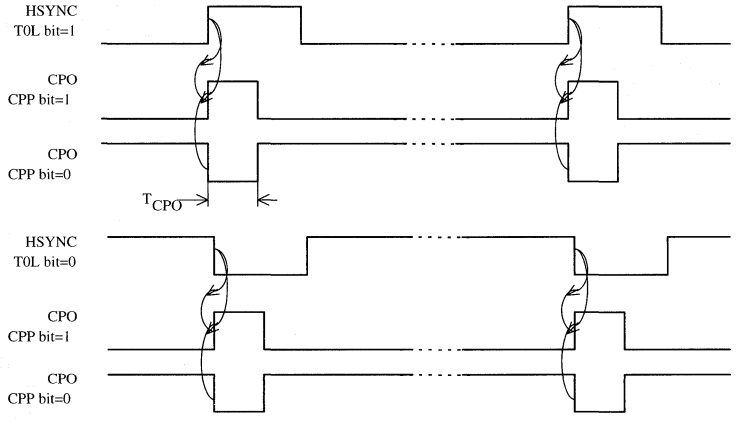


Figure 18. Clamp Pulse Output waveform

8. Electrical Characteristics

Absolute Maximum Ratings(1)

Operating Temperature:
Commercial ..... 0°C to 70°C
Industrial ..... –40°C to +85°C

Storage Temperature ..... –65°C to +150°C

Voltage on VCC to VSS ..... –0.5V to +7V

Voltage on Any Pin to VSS .... –0.5V to VCC + 0.5V

Power Dissipation ..... 1W(2)

Notice:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. This value is based on the maximum allowable die temperate and the thermal resistance of the package.

8.1. DC Characteristics

T_A = 0°C to +70°C; VSS = 0V; VCC = 5V ± 10%; F = 0 to 16MHz.

T_A = –40°C to +85°C; VSS = 0V; VCC = 5V ± 10%; F = 0 to 16MHz.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Inputs						
VIL	Input Low Voltage	–0.5		0.2 Vcc – 0.1	V	
VIH	Input High Voltage except XTAL1, RST	0.2 Vcc + 0.9		Vcc + 0.5	V	
VIH1	Input High Voltage, XTAL1, RST	0.7 Vcc		Vcc + 0.5	V	
IIL	Logical 0 Input Current ports 1, 2 and 3			–50	µA	Vin = 0.45V
ILI	Input Leakage Current			±10	µA	0.45 < Vin < Vcc
ITL	Logical 1 to 0 Transition Current, ports 1, 2, 3			–650	µA	Vin = 2.0V
VLOW	Power Fail Reset Low Voltage	TBD	3.5(5)	TBD	V	
Outputs						
VOL	Output Low Voltage, ports 1, 2, 3, PWM0–7 (6)			0.3 0.45 1.0	V V V	IOL = 100µA(4) IOL = 1.6mA(4) IOL = 3.5mA(4)
VOL1	Output Low Voltage, port 0, ALE, $\overline{PSEN}$ (6)			0.3 0.45 1.0	V V V	IOL = 200µA(4) IOL = 3.2mA(4) IOL = 7.0mA(4)
VOH	Output High Voltage, ports 1, 2, 3	Vcc – 0.3 Vcc – 0.7 Vcc – 1.5			V V V	IOH = –10µA IOH = –30µA IOH = –60µA Vcc = 5V ± 10%
VOH1	Output High Voltage, port 0, ALE, $\overline{PSEN}$	Vcc – 0.3 Vcc – 0.7 Vcc – 1.5			V V V	IOH =–200µA IOH = –3.2mA IOH = –7.0mA Vcc = 5V ± 10%
RRST	RST Pulldown Resistor	50	90 (5)	200	kΩ	
CIO	Capacitance of I/O Buffer			10	pF	fc = 1MHz, T_A = 25°C

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
ICC	Power Supply Current (7) Active Mode 12MHz Idle Mode 12MHz		 TBD TBD	 TBD TBD	 mA mA	 Vcc = 5.5V(1) Vcc = 5.5V(2)
IPD	Power Down Current		5 (5)	30	µA	Vcc = 2.0V to 5.5V(3)

Notes for DC Electrical Characteristics

1. ICC is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5 ns (see Figure 20.), VIL = VSS + 0.5V, VIH = VCC – 0.5V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = VCC. ICC would be slightly higher if a crystal oscillator used (see Figure 19.).
2. Idle ICC is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5ns, VIL = VSS + 0.5V, VIH = VCC–0.5V; XTAL2 N.C; Port 0 = VCC; $\overline{EA}$ = RST = VSS (see Figure 20.).
3. Power Down ICC is measured with all output pins disconnected; $\overline{EA}$ = PORT 0 = VCC; XTAL2 NC.; RST = VSS (see Figure 21.).
4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the VOLs of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi VOL peak 0.6V. A Schmitt Trigger use is not necessary.
5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
6. Under steady state (non–transient) conditions, IOL must be externally limited as follows:
   - Maximum IOL per port pin: 10 mA
   - Maximum IOL per 8–bit port:
     - Port 0: 26 mA
     - Ports 1, 2 and 3: 15 mA
   - Maximum total IOL for all output pins: 71 mA

   If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
7. For other values, please contact your sales office.

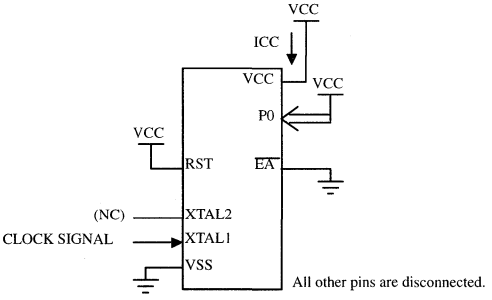


Figure 19. ICC Test Condition, Active Mode.

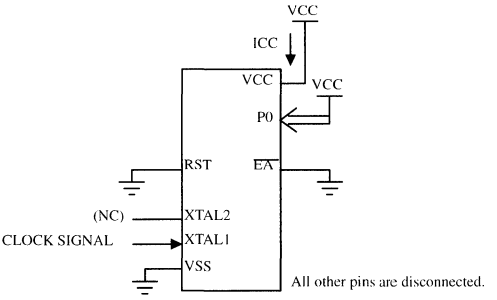


Figure 20. ICC Test Condition, Idle Mode.

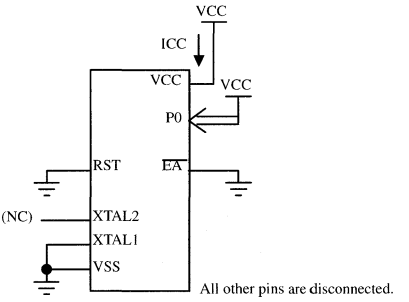


Figure 21. ICC Test Condition, Power Down Mode.

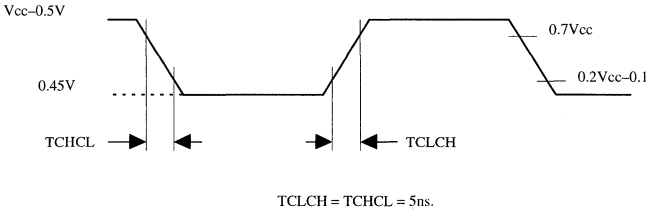


Figure 22. Clock Signal Waveform for ICC Tests in Active and Idle Modes.

8.2. Explanation Of The AC Symbol

Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:

TAVLL = Time for Address Valid to ALE low.

TLLPL = Time for ALE low to PSEN low.

A: Address.	Q: Output data.
C: Clock.	R: READ signal.
D: Input data.	T: Time.
H: Logic level HIGH.	V: Valid.
I: Instruction (Program memory contents).	W: WRITE signal.
L: Logic level LOW, or ALE.	X: No longer a valid logic level.
P: PSEN.	Z: Float.

8.3. AC Parameters

T_A = 0 to +70°C; VSS = 0V VCC = 5V±10%; 0 to 12MHz

T_A = –40°C to +85°C; VSS = 0V; VCC = 5V ± 10%; F = 0 to 12MHz.

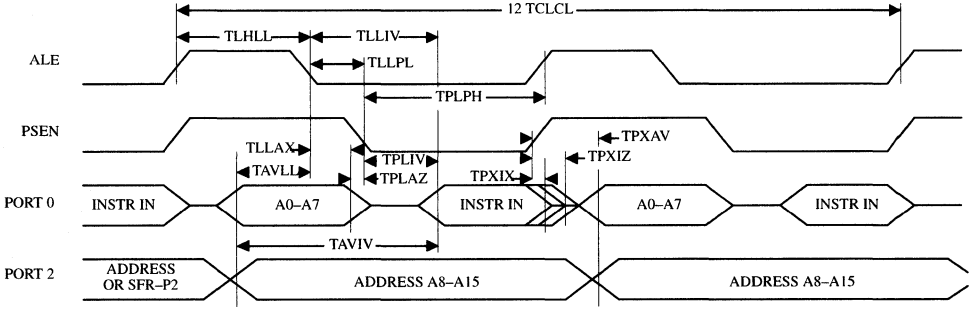
(Load Capacitance for PORT 0, ALE and PSEN = 100pf; Load Capacitance for all other outputs = 80 pF.)

8.4. External Program Memory Characteristics

Symbol	Parameter	0 to 12MHz		Units
		Min	Max	
TLHLL	ALE pulse width	2TCLCL – 40		ns
TAVLL	Address Valid to ALE	TCLCL – 40		ns
TLLAX	Address Hold After ALE	TCLCL – 30		ns
TLLIV	ALE to Valid Instruction In		4TCLCL – 100	ns
TLLPL	ALE to PSEN	TCLCL – 30		ns
TPLPH	PSEN Pulse Width	3TCLCL – 45		ns
TPLIV	PSEN to Valid Instruction In		3TCLCL – 105	ns

Symbol	Parameter	0 to 12MHz		Units
		Min	Max	
TPXIX	Input Instruction Hold After PSEN	0		ns
TPXIZ	Input Instruction Float After PSEN		TCLCL – 25	ns
TPXAV	PSEN to Address Valid	TCLCL – 8		ns
TAVIV	Address to Valid Instruction In		5TCLCL – 105	ns
TPLAZ	PSEN Low to Address Float		10	ns

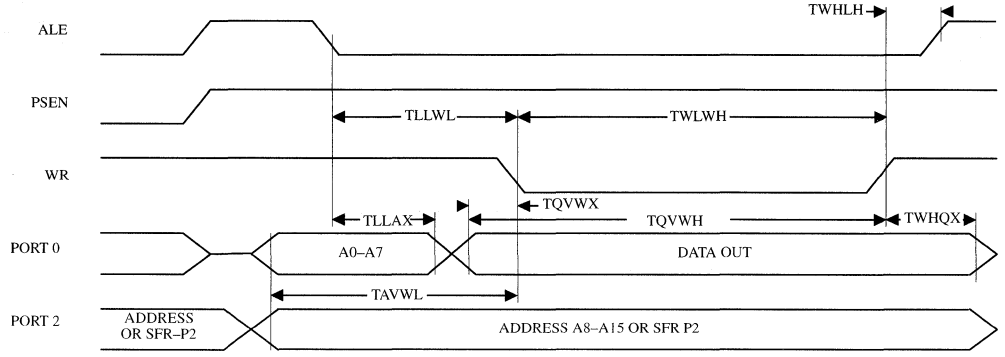
8.5. External Program Memory Read Cycle



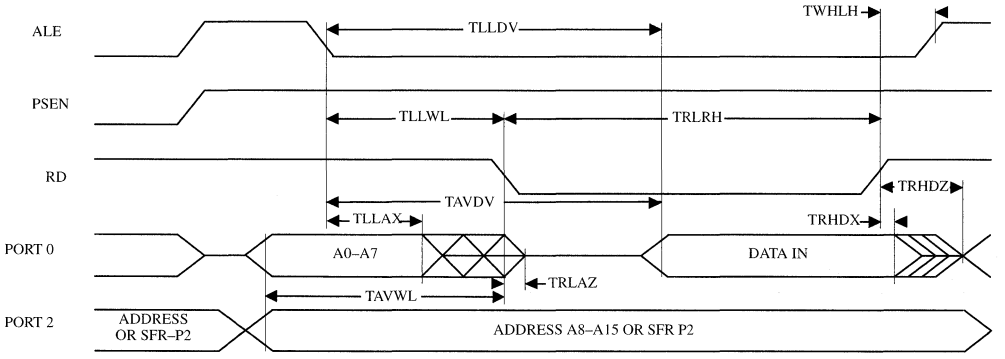
8.6. External Data Memory Characteristics

Symbol	Parameter	0 to 12MHz		Units
		Min	Max	
TRLRH	RD Pulse Width	6TCLCL–100		ns
TWLWH	WR Pulse Width	6TCLCL–100		ns
TRLDV	RD to Valid Data In		5TCLCL–165	ns
TRHDX	Data Hold After RD	0		ns
TRHDZ	Data Float After RD		2TCLCL–60	ns
TLLDV	ALE to Valid Data In		8TCLCL–150	ns
TAVDV	Address to Valid Data In		9TCLCL–165	ns
TLLWL	ALE to WR or RD	3TCLCL–50	3TCLCL+50	ns
TAVWL	Address to WR or RD	4TCLCL–130		ns
TQVWX	Data Valid to WR Transition	TCLCL–50		ns
TQVWH	Data set–up to WR High	7TCLCL–150		ns
TWHQX	Data Hold After WR	TCLCL–50		ns
TRLAZ	RD Low to Address Float		0	ns
TWHLH	RD or WR High to ALE high	TCLCL–40	TCLCL+40	ns

8.7. External Data Memory Write Cycle



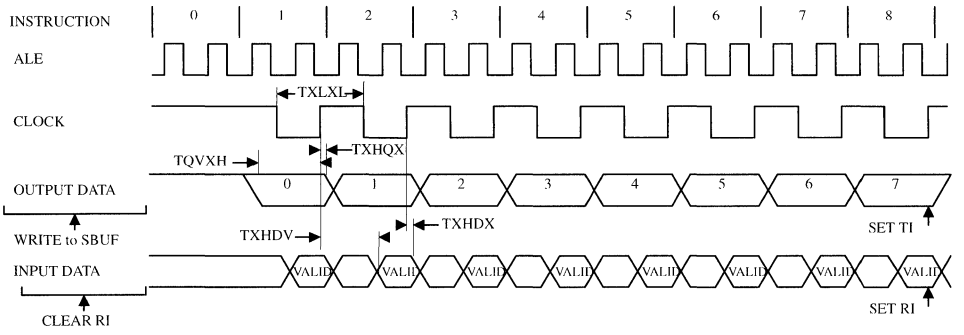
8.8. External Data Memory Read Cycle



8.9. Serial Port Timing–Shift Register Mode

Symbol	Parameter	0 to 12MHz		Units
		Min	Max	
TXLXL	Serial port clock cycle time	12TCLCL		ns
TQVHX	Output data set–up to clock rising edge	10TCLCL–133		ns
TXHQX	Output data hold after clock rising edge	2TCLCL–117		ns
TXHDX	Input data hold after clock rising edge	0		ns
TXHDV	Clock rising edge to input data valid		10TCLCL–133	ns

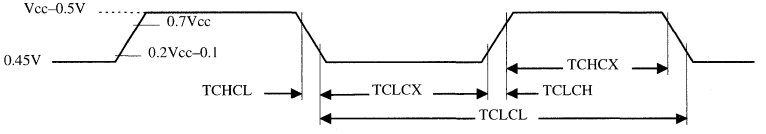
8.10. Shift Register Timing Waveforms



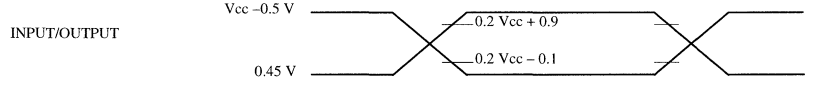
8.11. External Clock Drive Characteristics (XTAL1)

Symbol	Parameter	Min	Max	Units
TCLCL	Oscillator Period	83.3		ns
TCHCX	High Time	5		ns
TCLCX	Low Time	5		ns
TCLCH	Rise Time		5	ns
TCHCL	Fall Time		5	ns

8.12. External Clock Drive Waveforms

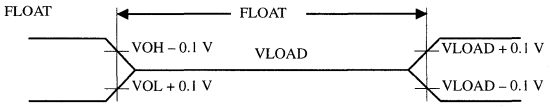


8.13. AC Testing Input/Output Waveforms



AC inputs during testing are driven at Vcc – 0.5 for a logic "1" and 0.45V for a logic "0". Timing measurement are made at VIH min for a logic "1" and VIL max for a logic "0".

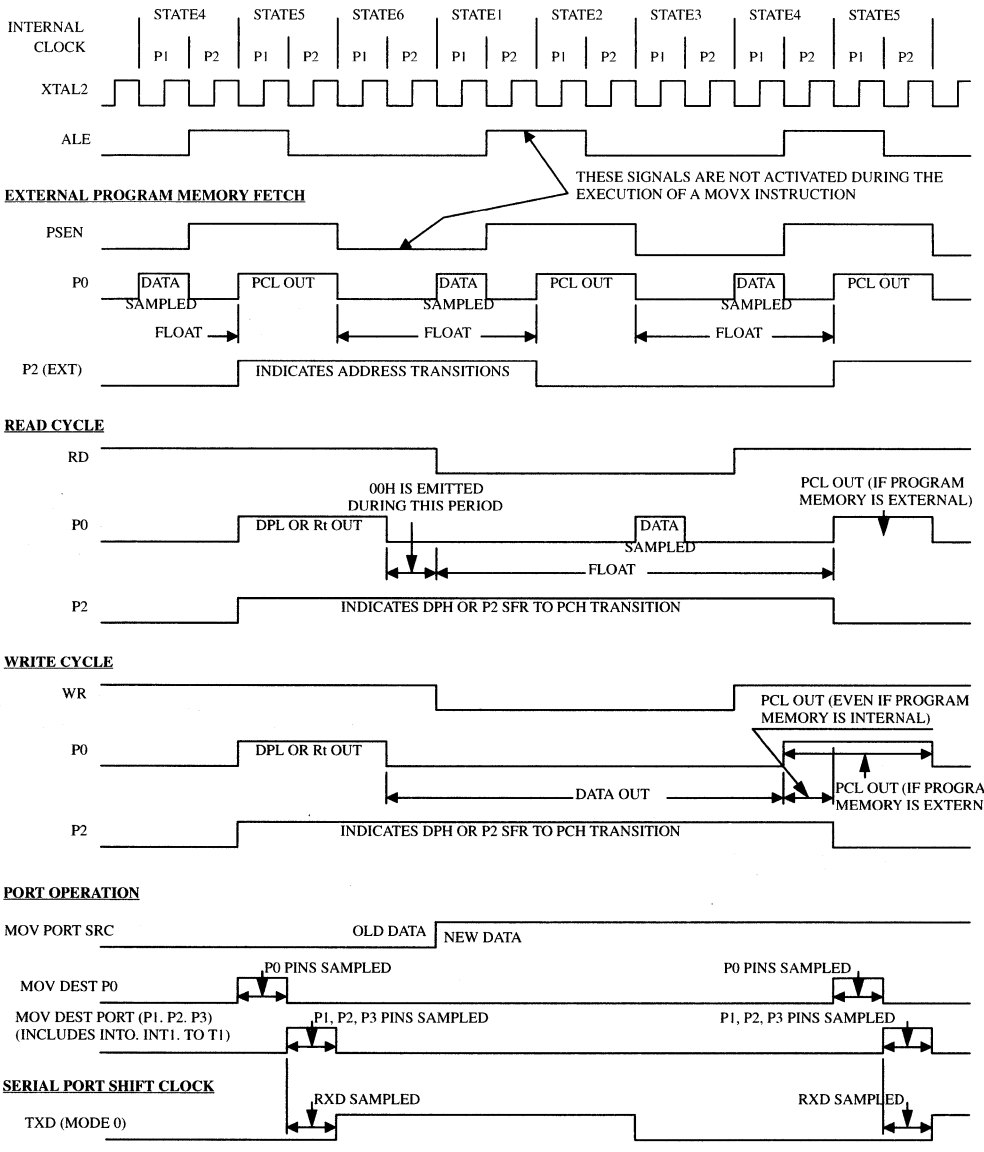
8.14. Float Waveforms



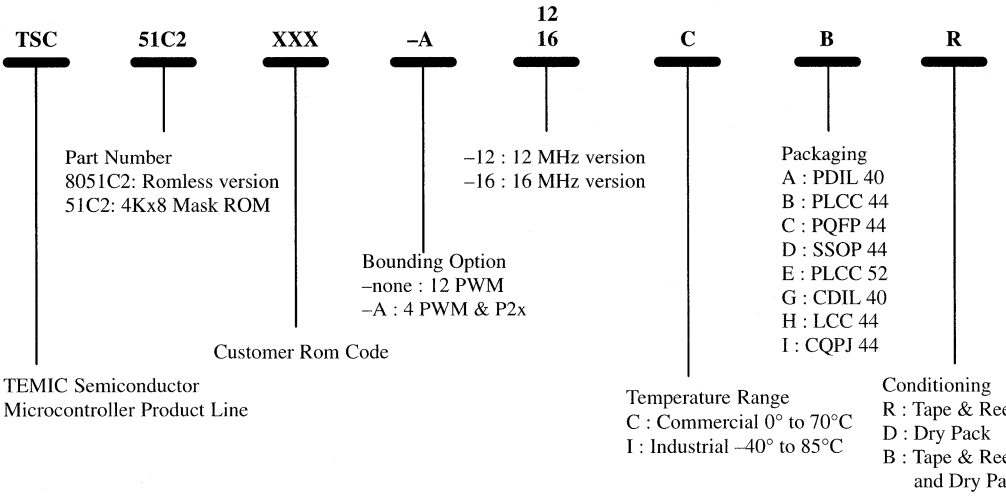
For timing purposes as port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded VOH/VOL level occurs. IOL/IOH ≥ ± 20mA.

8.15. Clock Waveform

This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A=25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50ns. The other signals are typically 85ns. Propagation delays are incorporated in the AC specifications.


INTERNAL CLOCK
STATE4 STATE5 STATE6 STATE1 STATE2 STATE3 STATE4 STATE5
P1 P2
XTAL2
ALE
THESE SIGNALS ARE NOT ACTIVATED DURING THE EXECUTION OF A MOVX INSTRUCTION
EXTERNAL PROGRAM MEMORY FETCH
PSEN
P0
DATA SAMPLED
PCL OUT
FLOAT
P2 (EXT)
INDICATES ADDRESS TRANSITIONS
READ CYCLE
RD
00H IS EMITTED DURING THIS PERIOD
DPL OR Rt OUT
PCL OUT (IF PROGRAM MEMORY IS EXTERNAL)
P2
INDICATES DPH OR P2 SFR TO PCH TRANSITION
WRITE CYCLE
WR
PCL OUT (EVEN IF PROGRAM MEMORY IS INTERNAL)
DATA OUT
PORT OPERATION
MOV PORT SRC
OLD DATA
NEW DATA
MOV DEST P0
P0 PINS SAMPLED
MOV DEST PORT (P1. P2. P3) (INCLUDES INTO. INT1. TO T1)
P1, P2, P3 PINS SAMPLED
SERIAL PORT SHIFT CLOCK
TXD (MODE 0)
RXD SAMPLED

9. Ordering Information



Examples

Part Number	Description
TSC51C2XXX–12CA	Mask ROM XXX, 12 MHz, PDIL 40, 0 to 70°C
TSC8051C2–16CER	ROMless, 16 MHz, PLCC 52, 0 to 70°C, Tape and Reel

Development Tools

Reference	Description
ANM059	Application Note: "How to recognize video mode and generate free running synchronization signals using TSC8051C1/C2 Microcontroller"
IM–80C51–RB–400–40	Emulator Base
PC–TSC8051C1–RB–16	Probe card for TSC8051C1. These products are released by Metalink. Please consult the local tools distributor or your sales office.

Product Marking :

TEMIC
Customer P/N
Temic P/N
© Intel 80, 82
YYWW Lot Number

C51 Automotive Products

TSC8051A1

CMOS Single chip 8–bit Microcontroller with Analog Interface

Description

The TSC8051A1 is a stand-alone, high performance CMOS microcontroller designed for use in automotive and industrial applications.

The TSC80A11 retains all features of the TSC80C51 with extended EPROM capacity (24K bytes), 256 bytes of internal RAM, a 14-source 2-level interrupt, a full duplex serial port, an on-chip oscillator, and two 16 bits timers.
In addition, the TSC8051A1 has an 8-bit 8-channel A/D converter, a serial synchronous port compatible with SPI and mWire protocols, an advanced 8 channels CCU (Capture & Compare Unit), an additional on-chip XRAM of 256 bytes and a high security Watchdog timer with an embedded oscillator.

The fully static design of the TSC8051A1 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.
The design is done with a specific care to reduce EMC emission and susceptibility.

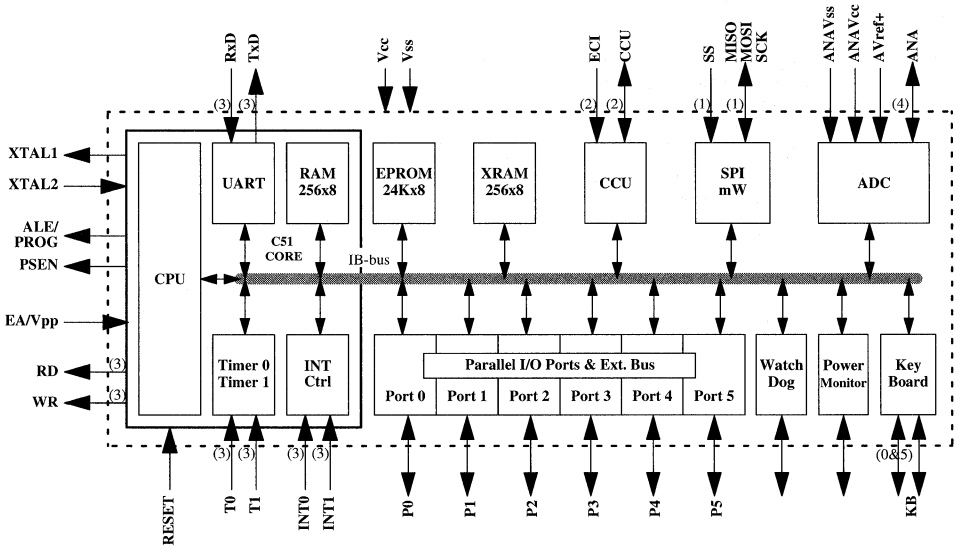
This circuit is manufactured using SCMOS process and is available in commercial, industrial, military and automotive ranges: it runs from 0 up to 20 MHz in the automotive temperature range -40°C to +125°C.

Features

- 80C51 core architecture:
  - 256 bytes of RAM
  - 256 bytes of XRAM
  - 24 Kilobytes of EPROM, OTP or ROM
  - 14-source 2-level interrupt
  - Two 16-bit timer/counter
  - Full duplex UART compatible with standard 80C51 with its own baud rate generator
- 6 8-bit 80C51 I/O Ports bit to bit configurable
- 2 ports with programmable interrupt for keyboard function
- A 8 channels 16-bit CCU with:
  - Rising and/or falling edge capture (pulse measurement capability)
  - Software timer, high speed output and multiple PWM shapes
- A 8-bit resolution analog to digital converter with 8 multiple inputs
- An high security watch-dog timer with an embedded oscillator
- A master/slave synchronous serial peripheral interface (SPI or mWire)
- Several power reduction modes with enhanced wake-up capabilities
- PQFP64 or PLCC68 packages

Preview

Block Diagram



(1): Alternate function of Port 1 (2): Alternate function of Port 2 (3): Alternate function of Port 3 (4): Alternate function of Port 4

Figure 1. TSC8051A1 block diagram

Pin-Out

Pin Functions

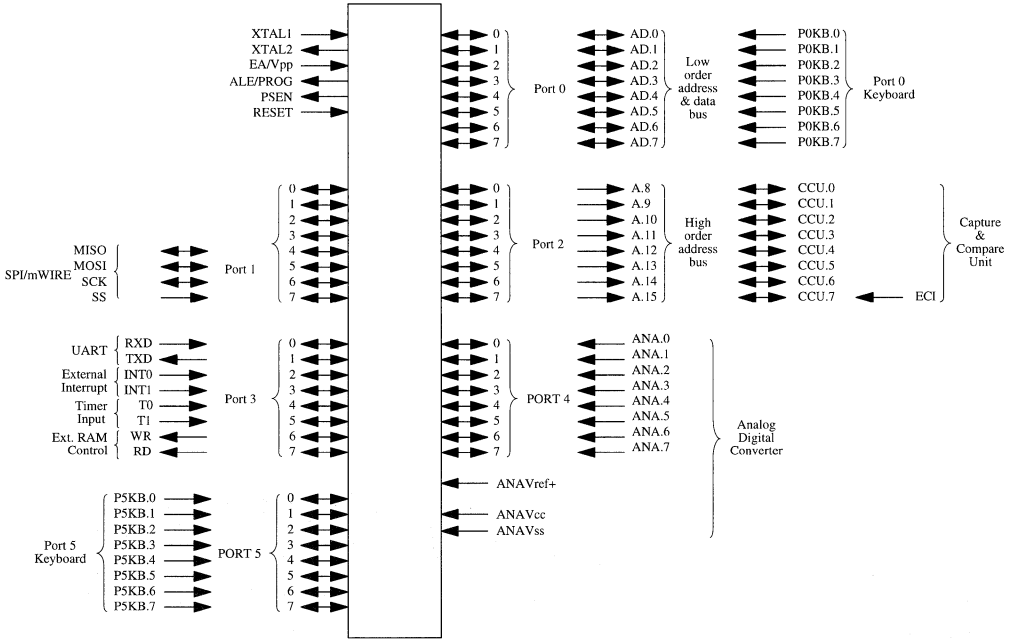


Figure 2. TSC8051A1 pin functions

Pin Configuration

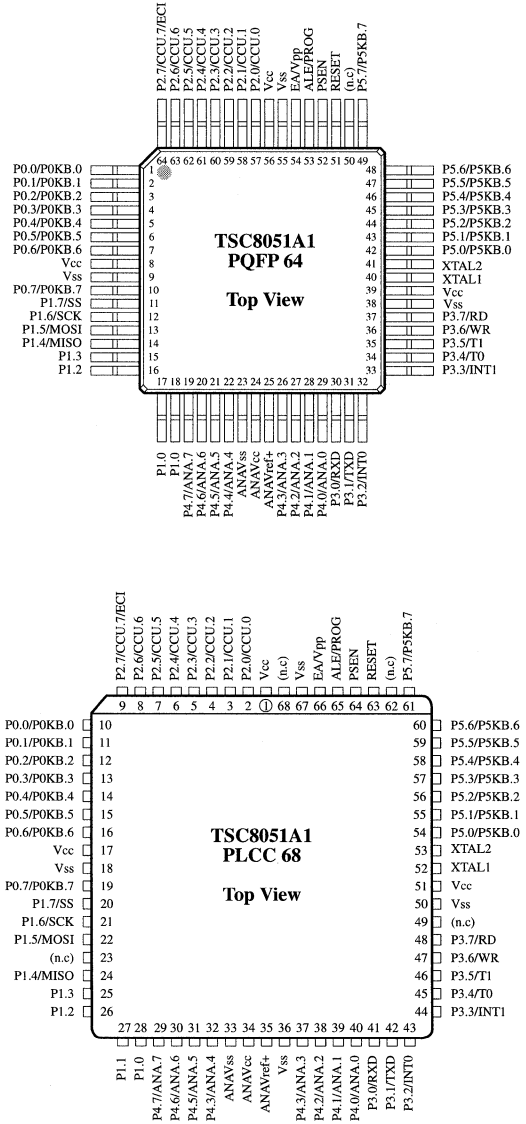


Figure 3. TSC8051A1 Pin Configuration

Pin Assignment

Table 1. Pin Assignment

Pin number		Pin name	Alternate function	Pin number		Pin Name	Alternate function
PQFP 64	PLCC 68			PQFP 64	PLCC 68		
1	10	P0.0	AD.0 / P0KB.0	33	44	P3.3	$\overline{INT1}$
2	11	P0.1	AD.1 / P0KB.1	34	45	P3.4	T0
3	12	P0.2	AD.2 / P0KB.2	35	46	P3.5	T1
4	13	P0.3	AD.3 / P0KB.3	36	47	P3.6	$\overline{WR}$
5	14	P0.4	AD.4 / P0KB.4	37	48	P3.7	RD
6	15	P0.5	AD.5 / P0KB.5		49	(n.c)	-
7	16	P0.6	AD.6 / P0KB.6	38	50	Vss	-
8	17	Vcc	-	39	51	Vcc	-
9	18	Vss	-	40	52	XTAL1	-
10	19	P0.7	AD.7 / P0KB.7	41	53	XTAL2	-
11	20	P1.7	SS	42	54	P5.0	P5KB.0
12	21	P1.6	SCK	43	55	P5.1	P5KB.1
13	22	P1.5	MOSI	44	56	P5.2	P5KB.2
	23	(n.c)		45	57	P5.3	P5KB.3
14	24	P1.4	MISO	46	58	P5.4	P5KB.4
15	25	P1.3	-	47	59	P5.5	P5KB.5
16	26	P1.2	-	48	60	P5.6	P5KB.6
17	27	P1.1	-	49	61	P5.7	P5KB.7
18	28	P1.0	-	50	62	(n.c)	
19	29	P4.7	ANA.7	51	63	RESET	-
20	30	P4.6	ANA.6	52	64	PSEN	-
21	31	P4.5	ANA.5	53	65	ALE/$\overline{PROG}$	-
22	32	P4.4	ANA.4	54	66	$\overline{EA}$ / Vpp	-
23	33	ANAVss	-	55	67	Vss	-
24	34	ANAVcc	-		68	(n.c)	
25	35	ANAref+	-	56	1	Vcc	-
	36	Vss	-	57	2	P2.0	A.8 / CCU.0
26	37	P4.3	ANA.3	58	3	P2.1	A.9 / CCU.1
27	38	P4.2	ANA.2	59	4	P2.2	A.10 / CCU.2
28	39	P4.1	ANA.1	60	5	P2.3	A.11 / CCU.3
29	40	P4.0	ANA.0	61	6	P2.4	A.12 / CCU.4
30	41	P3.0	RXD	62	7	P2.5	A.13 / CCU.5
31	42	P3.1	TXD	63	8	P2.6	A.14 / CCU.6
32	43	P3.2	INT0	64	9	P2.7	A.15 / CCU.7 / ECI

General Signal Description

Vss

Digital ground

Vcc

Digital supply voltage

ANAVss

Analog ground

ANAVcc

Analog supply voltage

$\overline{EA}$ / Vpp

External Access enable must be strapped to Vss in order to enable any device plugged on port 0 / port 2 to fetch code from 0 up to 24K. $\overline{EA}$ must be strapped to Vcc for internal program execution.
This pin also receives the 12V programming supply (Vpp input) to program the internal EPROM.

XTAL2

It is the output from the inverting oscillator amplifier.

$\overline{RESET}$

An active level (low) on this pin, while the oscillator is running, resets the device. An internal pull-up resistor permits power-on reset only using only an capacitor connected to Vss.
The active level of the $\overline{RESET}$ pin is the opposite to the one of C51 standard.

ALE / $\overline{PROG}$

The Address Latch Enable output signal is used to latch the low order byte of the address during accesses to external memory. ALE can sink and source 8 LS TTL loads.
If desired, ALE buffer can be disable. Then, ALE is pulled low.
This pin is also used (program pulse input) to program the internal EPROM.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory, else it remains high. $\overline{PSEN}$ can sink and source 8 LS TTL loads.

PORT 0

Port 0 can act the part of address/data bus or standard I/O port.
Its dedicated alternate function is a 8-bit keyboard interface.
In the default configuration, port 0 operates the same as it does in the 80C51, with open-drain outputs.

PORT 1

Port 1 can act the part of standard I/O port.
This port dedicated alternate functions are P.1[4:7] for synchronous serial link (SPI or mWIRE) interface.
In the default configuration, port 1 operates the same as it does in the 80C51, with internal pullups. Port 1 type C51 is sometimes called "quasi-bidirectional" due to the internal pullups.

PORT 2

Port 2 can act the part of address bus or standard I/O port.
Its dedicated alternate function is the CCU (Capture & Compare Unit) interface.
In the default configuration, port 2 operates the same as it does in the 80C51, with internal pull-ups.

PORT 3

Port 3 can act the part of standard I/O port.
Its dedicated alternate functions are those of the C51 standard (RxD, TxD, INT0, INT1, T0, T1, $\overline{WR}$ & $\overline{RD}$).
In the default configuration, port 3 operates the same as it does in the C51, with internal pull-ups. Port 3 type C51 is sometimes called "quasi-bidirectional" due to the internal pull-ups.

PORT 4

Port 4 can act the part of standard I/O port.
Its dedicated alternate functions are 8 inputs for ADC module.

In the default configuration, port 4 operates as a "quasi-bidirectional" port type C51 with internal pullups.

ANAref+

Positive voltage for the ADC module.

Preview

PORT 5

Port 5 can act the part of standard I/O port.

Its dedicated alternate function is a 8-bit keyboard interface.

In the default configuration, port 5 operates as a "quasi-bidirectional" port type C51 with internal pull-ups.

Electro-Magnetic Compatibility (EMC)

Primary attention is paid to the reduction of electro-magnetic emission of the TSC8051A1. The following features reduce the electro-magnetic emission and additionally improve the electro-magnetic susceptibility:

- The TSC8051A1 provides one analog supply voltage pin and one analog ground pin. Placed on the middle of one side of the package, this pair (ANAVcc/ ANAVss) has short bounding wires, thus reducing the generated noise.
  In order to reduce the radiation loop area, the two pins are adjacent.
- The TSC8051A1 provides three groups of digital supply voltage and digital ground, in pairs of pins (Vss/Vcc). Placed on the middle of the three other sides of the package, these groups have short bounding wires, thus reduces the generated noise.
  In order to reduce the radiation loop area, pins are adjacent inside group.
- External capacitors should be connected across associated pins (ANAVcc/ANAVss or Vcc/Vss). Lead length should be as short as possible. Ceramic CMS capacitors are recommended, 10nF + 100nF.
- Several internal decoupling capacitors improve the EMC radiation behavior and the EMC immunity.
- In order to reduce the spectrum of the TSC8051A1, many signals has been treated, principally the periodic signals. The current provided for external signals, the period of clocks and the raising/falling edges are the major points which has been nursed.
  - For application that never (or temporarily) requires external memory resources, the ALE buffer can be disable.
  - Once the oscillator is started, the gain is reduce by 2 (6 dB).
  - Peripherals receiving XTAL clock have, each one, their own prescaler to produce the operating clock they need.
  - The output buffers are especially designed to control rising and falling edges.

TSC8051A2

CMOS Single Chip 8–bit Microcontroller with Analog Interfaces

Description

The TSC8051A2 is a stand alone, high performance CMOS microcontroller designed for use in automotive and industrial applications.

The TSC8051A2 retains all features of the 80C51 with extended ROM capacity (16K bytes), 256 bytes of RAM, a 10–source 2–level interrupt, a full duplex serial port, an on–chip oscillator and clock and two 16 bits timers.

In addition, the TSC8051A2 has an 8–bit 8–channel A/D converter, a serial peripheral interface compatible with SPI, a high security watchdog and an advanced 8 channel Capture and Compare timer Unit.

The fully static design of the TSC8051A2 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The design is done with a specific care to reduce EMC emission and suceptibility.

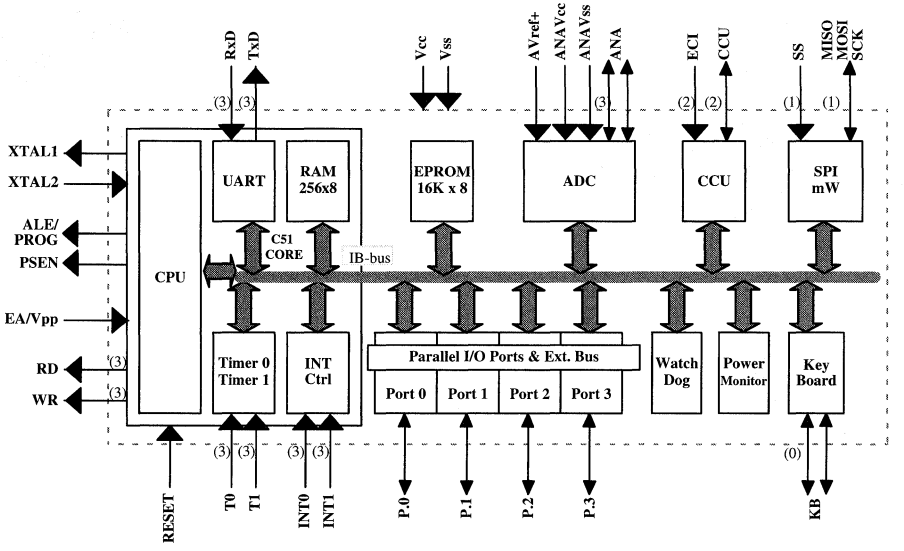
This circuit is manufactured using SCMOS process and is available in commercial, industrial, military and automotive ranges ; it runs from 0 up to 20 MHz in the automotive temperature range –40°C to +125°C.

Features

- 256 bytes of RAM
- 16 K bytes of ROM or OTP
- Four 8–bit I/O ports ; each bit can be:
  - TTL I/O
  - Push–pull output
  - CMOS input trigger with or without pull–down
- Two 16 bit timer/counter
- A programmable window watch–dog with integrated low power RC oscillator; basic period 20 ms typical, maximum period 128 times 20 ms
- A eight channels 16 bits Capture and Compare Unit with:
  - input capture
  - output compare and PWM
- A 8–bit resolution analog to digital converter with eight multiplex inputs ; conversion time 48 machine cycles.
- One port with programmable interrupt for keyboard function
- Several power reduction modes with enhanced wake up capabilities
- Power fail detection, Power on reset bit
- Full duplex UART compatible with standard 80C51
- A serial peripheral interface (SPI+MW)
- PQFP, PLCC or SSOP 44 package ; PQFP 64 for emulation

Preview

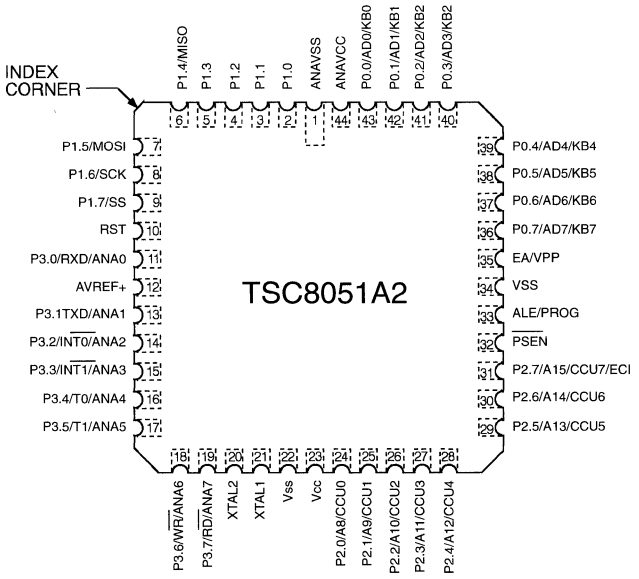
Block Diagram



(1): Alternate function of Port 1 (2): Alternate function of Port 2 (3): Alternate function of Port 3 (0): Alternate function of Port 0

Figure 1. TSC8051A2 Block Diagram

Pin Configuration



Preview

Pin PQFP 44	Pin PLCC 44	Name	Function	Pin PQFP 44	Pin PLCC 44	Name	Function
39	1	ANAVSS	VSS Analog	17	23	VCC	VCC
40	2	P1.0		18	24	P2.0/A08/CCU0	Address bus high order or CCU module 1 external I/O
41	3	P1.1		19	25	P2.1/A09/CCU1	Address bus high order or CCU module 1 external I/O
42	4	P1.2		20	26	P2.2/A10/CCU2	Address bus high order or CCU module 2 external I/O
43	5	P1.3		21	27	P2.3/A11/CCU3	Address bus high order or CCU module 3 external I/O
44	6	P1.4/MISO	SPI master in ,slave out	22	28	P2.4/A12/CCU4	Address bus high order or CCU module 4 external I/O
1	7	P1.5/MOSI	SPI master out, slave in	23	29	P2.5/A13/CCU5	Address bus high order or CCU module 5 external I/O
2	8	P1.6/SCK	SPI serial clock I/O	24	30	P2.6/A14/CCU6	Address bus high order or CCU module 6 external I/O
3	9	P1.7/SS	SPI slave select	25	31	P2.7/A15/CCU7/ ECI	Address bus high order or CCU module 7 external I/O or CCU count input
4	10	RST	Reset	26	32	PSEN	Program store enable
5	11	P3.0/RXD/ANA0	Serial receive port or Keyboard	27	33	ALE/PROG	Address latch enable/Program pulse
6	12	AVREF+	Analog positive reference	28	34	VSS	
7	13	P3.1/TXD/ANA1	Serial transmit port or Analog Input 1	29	35	EA/VPP	External access enable/Programming supply voltage
8	14	P3.2/INT0/ANA2	External interrupt 0 or Analog Input 2	30	36	P0.7/AD7/KB7	Mux. low order address & data bus or Keyboard
9	15	P3.3/INT1/ANA3	External interrupt 1 or Analog Input 3	31	37	P0.6/AD6/KB6	Mux. low order address & data bus or Keyboard
10	16	P3.4/T0/ANA4	Timer/counter 0 input or Analog Input 4	32	38	P0.5/AD5/KB5	Mux. low order address & data bus or Keyboard
11	17	P3.5/T1/ANA5	Timer/counter 1 input or Analog Input 5	33	39	P0.4/AD4/KB4	Mux. low order address & data bus or Keyboard
12	18	P3.6/WR/ANA6	External data memory write strobe or Analog Input 6	34	40	P0.3/AD3/KB3	Mux. low order address & data bus or Keyboard
13	19	P3.7/RD/ANA7	External data memory read strobe or Analog Input 7	35	41	P0.2/AD2/KB2	Mux. low order address & data bus or Keyboard
14	20	XTAL2	Crystal output	36	42	P0.1/AD1/KB1	Mux. low order address & data bus or Keyboard
15	21	XTAL1	Crystal input	37	43	P0.0/AD0/KB0	Mux. low order address & data bus or Keyboard
16	22	VSS	VSS	38	44	ANAVCC	VCC Analog

Pin Functions

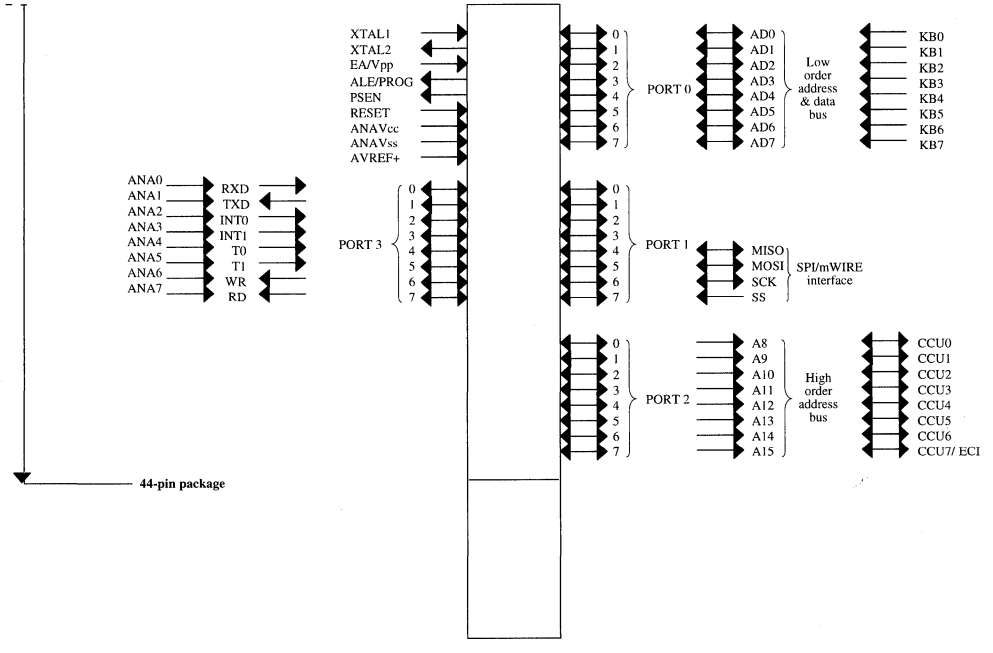


Figure 2. TSC8051A2 Pin Functions

General Signal Description

Vss

Digital ground

Vcc

Digital supply voltage

ANAVss

Analog groundl

ANAVcc

Analog supply voltage

$\overline{EA}$ / Vpp

External Access enable must be strapped to Vss in order to enable any device plugged on port 0 / port 2 to fetch code from 0 up to 16K. $\overline{EA}$ must be strapped to Vcc for internal program execution.
This pin also receives the 12V programming supply (Vpp input) to program the internal EPROM.

XTAL1

It is the input to the inverting oscillator amplifier and the input for external clock generator.

XTAL2

It is the output from the inverting oscillator amplifier.

$\overline{RESET}$

The active level of the RESET pin is low. An active level on this pin, while the oscillator is running, resets the device. An internal resistor permits power-on reset only using an external capacitor. The reset pin is bidirectional; it acts as an output when a reset is issued by the watch–dog function.

ALE / $\overline{PROG}$

The Address Latch Enable output signal is used to latch the low order byte of the address during accesses to external memory. ALE can sink and source 8 LS TTL loads.If desired, ALE buffer can be disable. Then, ALE is pulled low. This pin is also used (program pulse input) to program the internal EPROM.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory, else it remains high. $\overline{PSEN}$ can sink and source 8 LS TTL loads.

PORT 0

Port 0 can act the part of address/data bus or standard I/O port. Its dedicated alternate function are the inputs of the keyboard interrupt. In the default configuration, port 0 operates the same as it does in the 80C51, with open-drain outputs.

PORT 1

Port 1 can act the part of standard I/O port. This port dedicated alternate functions are P.1[4:7] for the synchronous serial link (SPI or mWIRE) interface.

In the default configuration, port 1 operates the same as it does in the 80C51, with internal pullups. Port 1 type C51 is sometimes called "quasi-bidirectional" due to the internal pullups.

PORT 2

Port 2 can act the part of address bus or standard I/O port.Its dedicated alternate function is the CCU (Capture & Compare Unit) interface.In the default configuration, port 2 operates the same as it does in the 80C51, with internal pullups.

PORT 3

Port 3 can act the part of standard I/O port.This port has two types of alternate functions:

- The first ones are the same than in C51 (Rxd, TxD, ..., $\overline{WR}$, $\overline{RD}$),
- The second type of alternate functions are 8 inputs for the 8–bit A/D converter.

In the default configuration, port 3 operates the same as it does in the C51, with internal pullups. Port 3 type C51 is sometimes called "quasi-bidirectional" due to the internal pullups.

AVREF+

- Positive reference voltage for the ADC module.

Electro-Magnetic Compatibility (EMC)

Primary attention is paid to the reduction of electro-magnetic emission of the TSC8051A2. The following features reduce the electro-magnetic emission and additionally improve the electro-magnetic susceptibility:

- The TSC8051A2 provides one analog supply voltage pin and one analog ground pin. Placed on the middle of one side of the package, this pair (ANAVcc/ ANAVss) has short bounding wires, thus reducing the generated noise.
  In order to reduce the radiation loop area, the two pins are adjacent.
- The TSC8051A2 provides one group of digital supply voltage and digital ground, in pairs of pins (Vss/Vcc). Placed on the middle of the sides of the package, this group have short bounding wires, thus reduces the generated noise. In order to reduce the radiation loop area, pins are adjacent inside group.
- External capacitors should be connected across associated pins (ANAVcc/ANAVss or Vcc/Vss). Lead length should be as short as possible. Ceramic CMS capacitors are recommended, 10nF ÷ 100nF.
- Several internal decoupling capacitors improve the EMC radiation behaviour and the EMC immunity.
- In order to reduce the spectrum of the TSC8051A2, many signals has been treated, principally the periodic signals. The current provided for external signals, the period of clocks and the raising/falling edges are the major points which has been nursed.
  - For application that never (or temporarily) requires external memory resources, the ALE buffer can be disable.
  - Once the oscillator is stable, the gain is reduce by 2 (6 dB).
  - Peripherals receiving XTAL clock have, each one, their own prescaler toproduce the operating clock they need.
  - The output buffers are especially designed to control rising and falling edges.

2

TSC8051A11

CMOS Single chip 8–bit Microcontroller with CAN Controller

Description

The TSC8051A11 is a stand-alone, high performance CMOS microcontroller designed for use in automotive and industrial applications.

The TSC80A11 retains all features of the TSC80C51 with extended EPROM capacity (24K bytes), 256 bytes of internal RAM, a 14-source 2-level interrupt, a full duplex serial port, an on-chip oscillator, and two 16 bits timers.
In addition, the TSC8051A11 has an 8-bit 8-channel A/D converter, a serial synchronous port compatible with SPI and mWire protocols, an advanced 8 channels CCU (Capture & Compare Unit), an additional on-chip XRAM of 256 bytes, a high security Watchdog timer with an embedded oscillator and a CAN network line controller.

The CAN controller is fully compliant with the BOSCH CAN standard rev 2.0 part B. It implements all features of a full CAN controller able to handle all frames of the protocol with 14 predefined messages (channels). It includes 14 sets of channel registers. Each channel has its own identifier tag, its own identifier mask and up to 8 bytes (mailbox) to store the received and transmitted message.

The fully static design of the TSC8051A11 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.
The design is done with a specific care to reduce EMC emission and susceptibility.

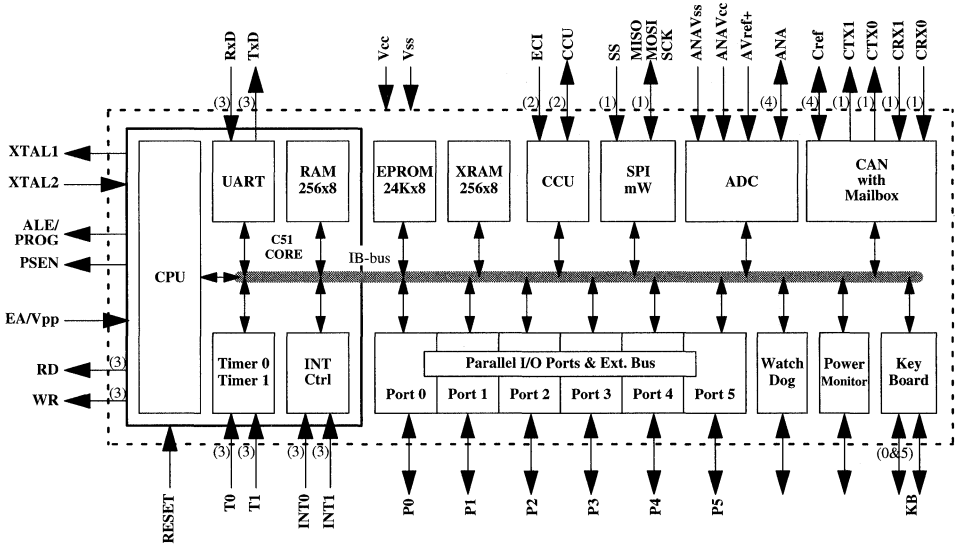
This circuit is manufactured using SCMOS process and is available in commercial, industrial, military and automotive ranges: it runs from 0 up to 20 MHz in the automotive temperature range -40°C to +125°C.

Features

- 80C51 core architecture:
  - 256 bytes of RAM
  - 256 bytes of XRAM
  - 24 Kilobytes of EPROM, OTP or ROM
  - 14-source 2-level interrupt
  - Two 16-bit timer/counter
  - Full duplex UART compatible with standard 80C51 with its own baud rate generator
- 6 8-bit 80C51 I/O Ports bit to bit configurable
- 2 ports with programmable interrupt for keyboard function
- A 8 channels 16-bit CCU with:
  - Rising and/or falling edge capture (pulse measurement capability)
  - Software timer, high speed output and multiple PWM shapes
- A 8-bit resolution analog to digital converter with 8 multiple inputs
- An high security watch-dog timer with an embedded oscillator
- A master/slave synchronous serial peripheral interface (SPI or mWire)
- Full CAN controller:
  - Fully compliant with CAN standard rev 2.0 A and 2.0 B
  - Optimized structure for communication management
  - 14 channels with individual tag and mask filters on 29 identifier-bit
  - Line wake-up capability
  - Automatic reply mode
  - 1 Mbit/s maximum transfer rate
  - Integrated line interface circuitry (output drivers, input comparators, Vcc/2 generator)
- Several power reduction modes with enhanced wake-up capabilities
- PQFP64 or PLCC68 packages

Preview

Block Diagram



(1): Alternate function of Port 1 (2): Alternate function of Port 2 (3): Alternate function of Port 3 (4): Alternate function of Port 4

Figure 1. TSC8051A11 block diagram

Pin-Out

Pin Functions

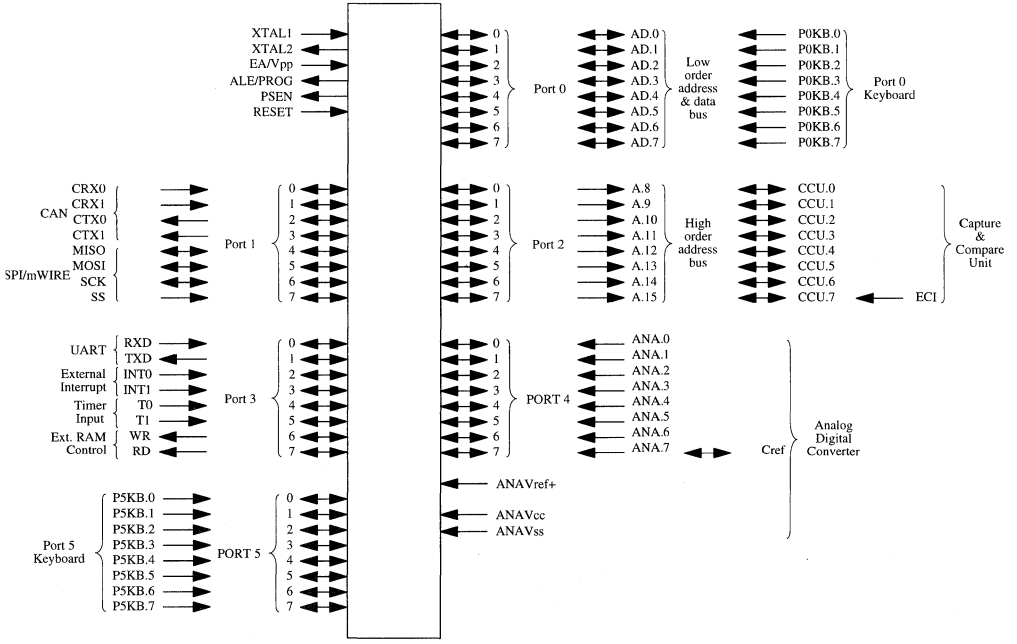


Figure 2. TSC8051A11 pin functions

Pin Configuration

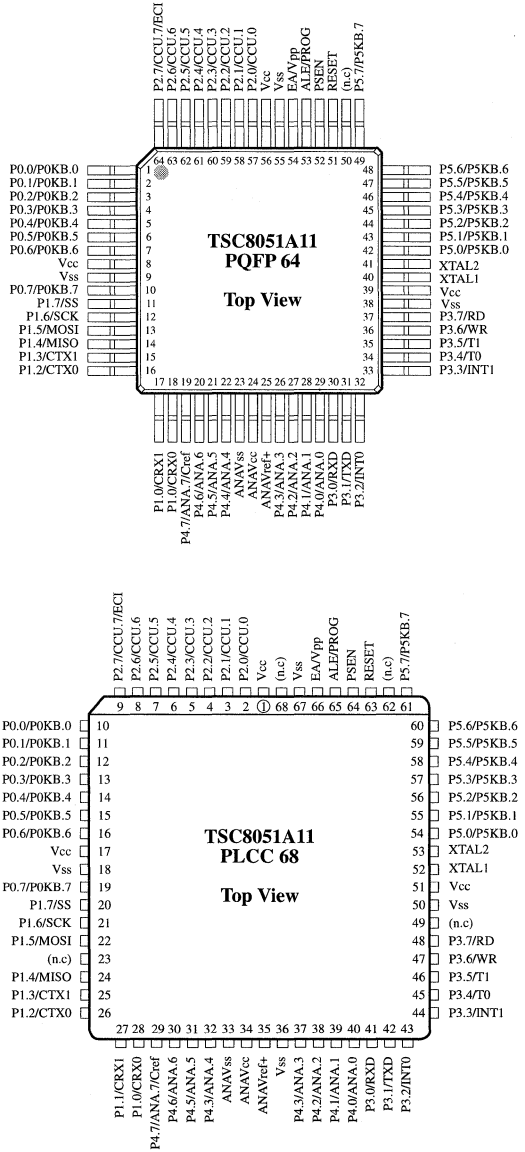


Figure 3. TSC8051A11 pin configuration

Pin Assignment

Table 2. Pin assignment

Pin number		Pin name	Alternate function	Pin number		Pin Name	Alternate function
PQFP 64	PLCC 68			PQFP 64	PLCC 68		
1	10	P0.0	AD.0 / P0KB.0	33	44	P3.3	$\overline{INT1}$
2	11	P0.1	AD.1 / P0KB.1	34	45	P3.4	T0
3	12	P0.2	AD.2 / P0KB.2	35	46	P3.5	T1
4	13	P0.3	AD.3 / P0KB.3	36	47	P3.6	$\overline{WR}$
5	14	P0.4	AD.4 / P0KB.4	37	48	P3.7	RD
6	15	P0.5	AD.5 / P0KB.5		49	(n.c)	-
7	16	P0.6	AD.6 / P0KB.6	38	50	Vss	-
8	17	Vcc	-	39	51	Vcc	-
9	18	Vss	-	40	52	XTAL1	-
10	19	P0.7	AD.7 / P0KB.7	41	53	XTAL2	-
11	20	P1.7	SS	42	54	P5.0	P5KB.0
12	21	P1.6	SCK	43	55	P5.1	P5KB.1
13	22	P1.5	MOSI	44	56	P5.2	P5KB.2
	23	(n.c)		45	57	P5.3	P5KB.3
14	24	P1.2	MISO	46	58	P5.4	P5KB.4
15	25	P1.3	CTX1	47	59	P5.5	P5KB.5
16	26	P1.2	CTX0	48	60	P5.6	P5KB.6
17	27	P1.1	CRX1	49	61	P5.7	P5KB.7
18	28	P1.0	CRX0	50	62	(n.c)	
19	29	P4.7	ANA.7 / Cref	51	63	RESET	-
20	30	P4.6	ANA.6	52	64	PSEN	-
21	31	P4.5	ANA.5	53	65	ALE/$\overline{PROG}$	-
22	32	P4.4	ANA.4	54	66	$\overline{EA}$ / Vpp	-
23	33	ANAVss	-	55	67	Vss	-
24	34	ANAVcc	-		68	(n.c)	
25	35	ANAref+	-	56	1	Vcc	-
	36	Vss	-	57	2	P2.0	A.8 / CCU.0
26	37	P4.3	ANA.3	58	3	P2.1	A.9 / CCU.1
27	38	P4.2	ANA.2	59	4	P2.2	A.10 / CCU.2
28	39	P4.1	ANA.1	60	5	P2.3	A.11 / CCU.3
29	40	P4.0	ANA.0	61	6	P2.4	A.12 / CCU.4
30	41	P3.0	RXD	62	7	P2.5	A.13 / CCU.5
31	42	P3.1	TXD	63	8	P2.6	A.14 / CCU.6
32	43	P3.2	INT0	64	9	P2.7	A.15 / CCU.7 / ECI

General Signal Description

Vss

Digital ground

Vcc

Digital supply voltage

ANAVss

Analog ground

ANAVcc

Analog supply voltage

$\overline{EA}$ / Vpp

External Access enable must be strapped to Vss in order to enable any device plugged on port 0 / port 2 to fetch code from 0 up to 24K. $\overline{EA}$ must be strapped to Vcc for internal program execution.
This pin also receives the 12V programming supply (Vpp input) to program the internal EPROM.

XTAL2

It is the output from the inverting oscillator amplifier.

$\overline{RESET}$

An active level (low) on this pin, while the oscillator is running, resets the device. An internal pull-up resistor permits power-on reset only using only an capacitor connected to Vss.
The active level of the $\overline{RESET}$ pin is the opposite to the one of C51 standard.

ALE / $\overline{PROG}$

The Address Latch Enable output signal is used to latch the low order byte of the address during accesses to external memory. ALE can sink and source 8 LS TTL loads.
If desired, ALE buffer can be disable. Then, ALE is pulled low.
This pin is also used (program pulse input) to program the internal EPROM.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory, else it remains high. $\overline{PSEN}$ can sink and source 8 LS TTL loads.

PORT 0

Port 0 can act the part of address/data bus or standard I/O port.
Its dedicated alternate function is a 8-bit keyboard interface.
In the default configuration, port 0 operates the same as it does in the 80C51, with open-drain outputs.

PORT 1

Port 1 can act the part of standard I/O port.
This port has two dedicated alternate functions:

- P.1[0:3] for CAN (Controller Area Network) interface.
- P.1[4:7] are for synchronous serial link (SPI or mWIRE) interface, In the default configuration, port 1 operates the same as it does in the 80C51, with internal pullups. Port 1 type C51 is sometimes called "quasi-bidirectional" due to the internal pullups.

PORT 2

Port 2 can act the part of address bus or standard I/O port.
Its dedicated alternate function is the CCU (Capture & Compare Unit) interface.

In the default configuration, port 2 operates the same as it does in the 80C51, with internal pull-ups.

PORT 3

Port 3 can act the part of standard I/O port.
Its dedicated alternate functions are those of the C51 standard (RxD, TxD, INT0, INT1, T0, T1, $\overline{WR}$ & $\overline{RD}$).
In the default configuration, port 3 operates the same as it does in the C51, with internal pull-ups. Port 3 type C51 is sometimes called "quasi-bidirectional" due to the internal pull-ups.

PORT 4

Port 4 can act the part of standard I/O port.
This port has two types of alternate functions:

- The first ones are 8 inputs for ADC module,
- The second type of alternate functions is the reference voltage, Cref for CAN module.
  In the default configuration, port 4 operates as a "quasi-bidirectional" port type C51 with internal pullups.

ANAref+

Positive voltage for the ADC module.

PORT 5

Port 5 can act the part of standard I/O port.

Its dedicated alternate function is a 8-bit keyboard interface.

In the default configuration, port 5 operates as a "quasi-bidirectional" port type C51 with internal pull-ups.

Electro-Magnetic Compatibility (EMC)

Primary attention is paid to the reduction of electro-magnetic emission of the TSC8051A11. The following features reduce the electro-magnetic emission and additionally improve the electro-magnetic susceptibility:

- The TSC8051A11 provides one analog supply voltage pin and one analog ground pin. Placed on the middle of one side of the package, this pair (ANAVcc/ ANAVss) has short bounding wires, thus reducing the generated noise.
  In order to reduce the radiation loop area, the two pins are adjacent.
- The TSC8051A11 provides three groups of digital supply voltage and digital ground, in pairs of pins (Vss/Vcc). Placed on the middle of the three other sides of the package, these groups have short bounding wires, thus reduces the generated noise.
  In order to reduce the radiation loop area, pins are adjacent inside group.
- External capacitors should be connected across associated pins (ANAVcc/ANAVss or Vcc/Vss). Lead length should be as short as possible. Ceramic CMS capacitors are recommended, 10nF + 100nF.
- Several internal decoupling capacitors improve the EMC radiation behavior and the EMC immunity.
- In order to reduce the spectrum of the TSC8051A11, many signals has been treated, principally the periodic signals. The current provided for external signals, the period of clocks and the raising/falling edges are the major points which has been nursed.
  - For application that never (or temporarily) requires external memory resources, the ALE buffer can be disable.
  - Once the oscillator is started, the gain is reduce by 2 (6 dB).
  - Peripherals receiving XTAL clock have, each one, their own prescaler to produce the operating clock they need.
  - The output buffers are especially designed to control rising and falling edges.

2

Preview

TSC8051A30

CMOS Single Chip 8–bit Microcontroller with VAN Controller

Description

The TSC8051A30 is a stand alone, high performance CMOS microcontroller designed for use in automotive and industrial applications.

The TSC8051A30 retains all features of the MHS 80C51 with extended ROM capacity (16K bytes), 256 bytes of RAM, a 10–source 2–level interrupt, a full duplex serial port, an on–chip oscillator and clock and two 16 bits timers.

In addition, the TSC8051A30 has an 8–bit 8–channel A/D converter, a serial peripheral interface compatible with SPI, a high security watchdog, an advanced 8 channel Capture and Compare timer Unit, a VAN network line controller with a 128 bytes extra RAM used to store the VAN messages.

The VAN controller is fully compliant with the ISO standard ISO/11519–3. It implements all features of the TSS461C VAN data link controller, including a 128 bytes data dual port RAM to store the received and transmitted messages.

The fully static design of the TSC8051A30 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The design is done with a specific care to reduce EMC emission and suceptibility.

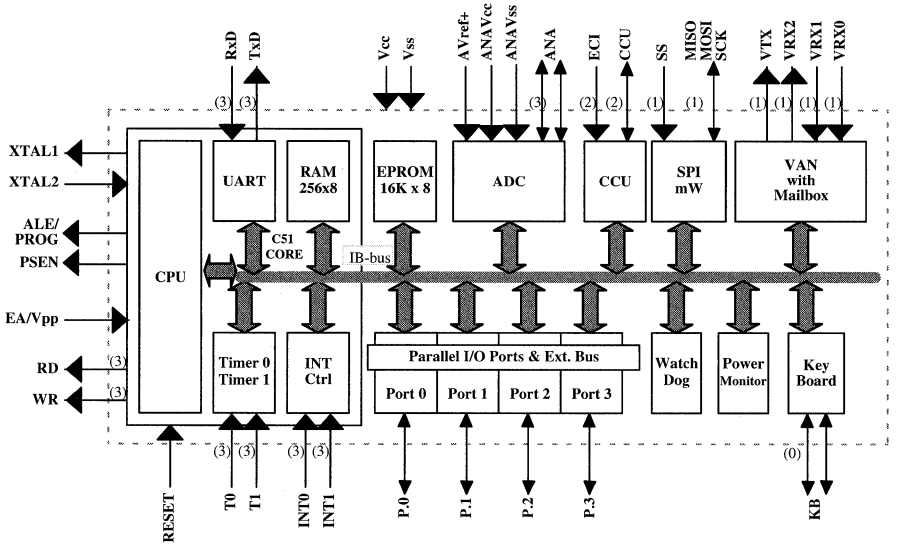
This circuit is manufactured using SCMOS process and is available in commercial, industrial, military and automotive ranges ; it runs from 0 up to 20 MHz in the automotive temperature range –40°C to +125°C.

Features

- 256 bytes of RAM
- 16 K bytes of ROM or OTP
- Four 8–bit I/O ports ; each bit can be:
  - TTL I/O
  - Push–pull output
  - CMOS input trigger with or without pull–down
- Two 16 bit timer/counter
- A programmable window watch–dog with integrated low power RC oscillator; basic period 20 ms typical, maximum period 128 times 20 ms
- A eight channels 16 bits Capture and Compare Unit with:
  - input capture
  - output compare and PWM
- A 8–bit resolution analog to digital converter with eight multiplex inputs ; conversion time 48 machine cycles.
- One port with programmable interrupt for keyboard function
- Several power reduction modes with enhanced wake up capabilities
- Power fail detection, Power on reset bit
- Full duplex UART compatible with standard 80C51
- A serial peripheral interface (SPI+MW)
- VAN controller with 128 bytes data RAM
  - Fully Compliant with VAN standard ISO/11519–3.
  - 14 Identifier Registers with all bits individually maskable
  - 1 Mbits/s Maximum Transfer Rate
  - 3 Separate line inputs with automatic diagnosis and selection
  - Idle and sleep modes
  - Manchester Enhanced or Impulsed Coding
- PQFP, PLCC or SSOP 44 package ; PQFP 64 for emulation

Preview

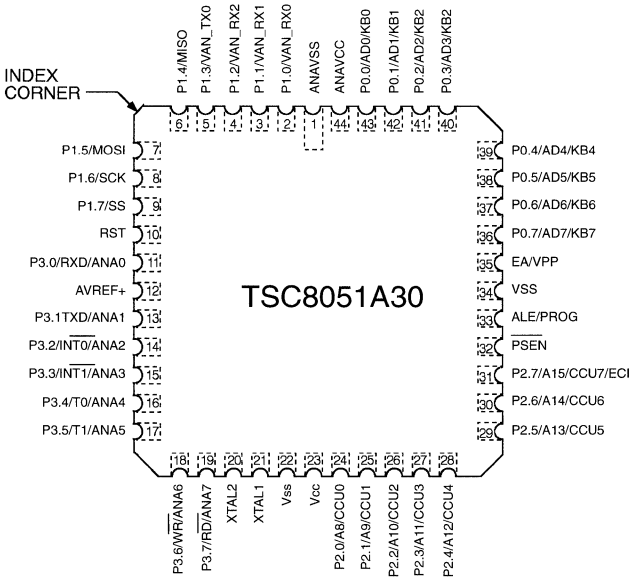
Block Diagram



(1): Alternate function of Port 1 (2): Alternate function of Port 2 (3): Alternate function of Port 3 (0): Alternate function of Port 0

Figure 1. TSC8051A30 Block Diagram

Pin Configuration



Pin PQFP 44	Pin PLCC 44	Name	Function	Pin PQFP 44	Pin PLCC 44	Name	Function
39	1	ANAVSS	VSS Analog	17	23	VCC	VCC
40	2	P1.0/VAN_RX0	VAN RX0	18	24	P2.0/A08/CCU0	Address bus high order or CCU module 1 external I/O
41	3	P1.1/VAN_RX1	VAN RX1	19	25	P2.1/A09/CCU1	Address bus high order or CCU module 1 external I/O
42	4	P1.2/VAN_RX2	VAN RX2	20	26	P2.2/A10/CCU2	Address bus high order or CCU module 2 external I/O
43	5	P1.3/VAN_TX0	VAN TX1	21	27	P2.3/A11/CCU3	Address bus high order or CCU module 3 external I/O
44	6	P1.4/MISO	SPI master in ,slave out	22	28	P2.4/A12/CCU4	Address bus high order or CCU module 4 external I/O
1	7	P1.5/MOSI	SPI master out, slave in	23	29	P2.5/A13/CCU5	Address bus high order or CCU module 5 external I/O
2	8	P1.6/SCK	SPI serial clock I/O	24	30	P2.6/A14/CCU6	Address bus high order or CCU module 6 external I/O
3	9	P1.7/SS	SPI slave select	25	31	P2.7/A15/CCU7/ ECI	Address bus high order or CCU module 7 external I/O or CCU count input
4	10	RST	Reset	26	32	PSEN	Program store enable
5	11	P3.0/RXD/ANA0	Serial receive port or Keyboard	27	33	ALE/PROG	Address latch enable/Program pulse
6	12	AVREF+	Analog positive reference	28	34	VSS	
7	13	P3.1/TXD/ANA1	Serial transmit port or Analog Input 1	29	35	EA/VPP	External access enable/Programming supply voltage
8	14	P3.2/INT0/ANA2	External interrupt 0 or Analog Input 2	30	36	P0.7/AD7/KB7	Mux. low order address & data bus or Keyboard
9	15	P3.3/INT1/ANA3	External interrupt 1 or Analog Input 3	31	37	P0.6/AD6/KB6	Mux. low order address & data bus or Keyboard
10	16	P3.4/T0/ANA4	Timer/counter 0 input or Analog Input 4	32	38	P0.5/AD5/KB5	Mux. low order address & data bus or Keyboard
11	17	P3.5/T1/ANA5	Timer/counter 1 input or Analog Input 5	33	39	P0.4/AD4/KB4	Mux. low order address & data bus or Keyboard
12	18	P3.6/WR/ANA6	External data memory write strobe or Analog Input 6	34	40	P0.3/AD3/KB3	Mux. low order address & data bus or Keyboard
13	19	P3.7/RD/ANA7	External data memory read strobe or Analog Input 7	35	41	P0.2/AD2/KB2	Mux. low order address & data bus or Keyboard
14	20	XTAL2	Crystal output	36	42	P0.1/AD1/KB1	Mux. low order address & data bus or Keyboard
15	21	XTAL1	Crystal input	37	43	P0.0/AD0/KB0	Mux. low order address & data bus or Keyboard
16	22	VSS	VSS	38	44	ANAVCC	VCC Analog

Pin Functions

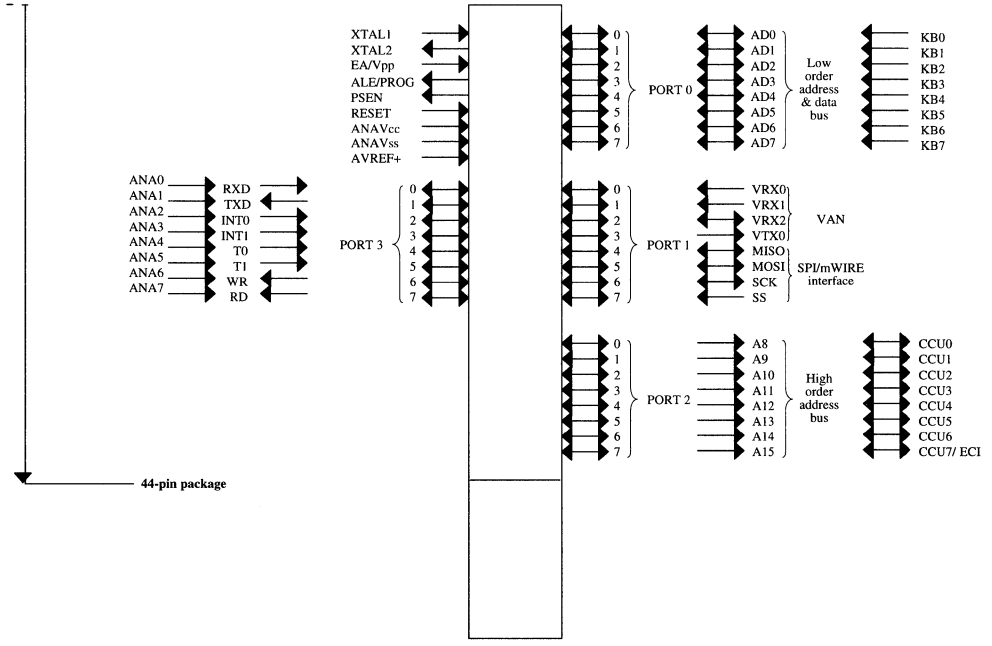


Figure 2. TSC8051A30 pin functions

General Signal Description

Vss

Digital ground

Vcc

Digital supply voltage

ANAVss

Analog groundl

ANAVcc

Analog supply voltage

$\overline{EA}$ / Vpp

External Access enable must be strapped to Vss in order to enable any device plugged on port 0 / port 2 to fetch code from 0 up to 16K. $\overline{EA}$ must be strapped to Vcc for internal program execution.
This pin also receives the 12V programming supply (Vpp input) to program the internal EPROM.

XTAL1

It is the input to the inverting oscillator amplifier and the input for external clock generator.

XTAL2

It is the output from the inverting oscillator amplifier.

$\overline{RESET}$

The active level of the RESET pin is low. An active level on this pin, while the oscillator is running, resets the device. An internal resistor permits power-on reset only using an external capacitor. The reset pin is bidirectional; it acts as an output when a reset is issued by the watch–dog function.

ALE / $\overline{PROG}$

The Address Latch Enable output signal is used to latch the low order byte of the address during accesses to external memory. ALE can sink and source 8 LS TTL loads.If desired, ALE buffer can be disable. Then, ALE is pulled low. This pin is also used (program pulse input) to program the internal EPROM.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory, else it remains high. $\overline{PSEN}$ can sink and source 8 LS TTL loads.

PORT 0

Port 0 can act the part of address/data bus or standard I/O port. Its dedicated alternate function are the inputs of the keyboard interrupt. In the default configuration, port 0 operates the same as it does in the 80C51, with open-drain outputs.

PORT 1

Port 1 can act the part of standard I/O port. This port has two dedicated alternate functions:

•P.1[0:3] for VAN (Vehicle Area Network) interface.

•P.1[4:7] are for synchronous serial link (SPI or mWIRE) interface.

In the default configuration, port 1 operates the same as it does in the 80C51, with internal pullups. Port 1 type C51 is sometimes called "quasi-bidirectional" due to the internal pullups.

PORT 2

Port 2 can act the part of address bus or standard I/O port.Its dedicated alternate function is the CCU (Capture & Compare Unit) interface.In the default configuration, port 2 operates the same as it does in the 80C51, with internal pullups.

PORT 3

Port 3 can act the part of standard I/O port.This port has two types of alternate functions:

- The first ones are the same than in C51 (Rxd, TxD, ..., $\overline{WR}$, $\overline{RD}$),
- The second type of alternate functions are 8 inputs for the 8–bit A/D converter.

In the default configuration, port 3 operates the same as it does in the C51, with internal pullups. Port 3 type C51 is sometimes called "quasi-bidirectional" due to the internal pullups.

AVREF+

- Positive reference voltage for the ADC module.

Electro-Magnetic Compatibility (EMC)

Primary attention is paid to the reduction of electro-magnetic emission of the TSC8051A30. The following features reduce the electro-magnetic emission and additionally improve the electro-magnetic susceptibility:

- The TSC8051A30 provides one analog supply voltage pin and one analog ground pin. Placed on the middle of one side of the package, this pair (ANAVcc/ ANAVss) has short bounding wires, thus reducing the generated noise.
  In order to reduce the radiation loop area, the two pins are adjacent.
- The TSC8051A30 provides one group of digital supply voltage and digital ground, in pairs of pins (Vss/Vcc). Placed on the middle of the sides of the package, this group have short bounding wires, thus reduces the generated noise. In order to reduce the radiation loop area, pins are adjacent inside group.
- External capacitors should be connected across associated pins (ANAVcc/ANAVss or Vcc/Vss). Lead length should be as short as possible. Ceramic CMS capacitors are recommended, 10nF + 100nF.
- Several internal decoupling capacitors improve the EMC radiation behaviour and the EMC immunity.
- In order to reduce the spectrum of the TSC8051A30, many signals has been treated, principally the periodic signals. The current provided for external signals, the period of clocks and the raising/falling edges are the major points which has been nursed.
  - For application that never (or temporarily) requires external memory resources, the ALE buffer can be disable.
  - Once the oscillator is stable, the gain is reduce by 2 (6 dB).
  - Peripherals receiving XTAL clock have, each one, their own prescaler toproduce the operating clock they need.
  - The output buffers are especially designed to control rising and falling edges.

2

Preview

Section III

C51 Application Notes

Secret Tag on 80C51 Family Microcontrollers

Overview

The Secret Tag is a feature which allows serialization of each microcontroller for identification of a specific equipment.

For instance, on a network, each terminal equipment can be identified by comparing the identifier sent via network with the identification number stored in the microcontroller.

One unique number per device is implemented. This serial number is a 64–bit binary value, which is contained and addressable in SFR (Special Function Registers) area.

This value can be used as an identification number, and permits personalization of any electronic equipment using a 80C51 architecture.

The coding of the different registers allows TEMIC to guarantee that each value of the Secret Tag is UNIQUE.

For confidentiality on secret tag value, no special marking is written neither on the die nor on the final package. This value can be read out by classical instruction set routine. This routine is implemented inside the microcontroller ROM memory which can be kept secret (and then the value of the secret tag also) by using a ROM ENCRYPTION.

Description

The secret tag register is composed of two groups of four consecutive bytes in the Special Function Register (SFR) area. One is placed at the FCh to FFh addresses and the other at the ECh to EFh addresses.

These registers are used as follows :

- Lot number (L0–L15) : number from 0 to 65535 referring to TEMIC fab lot number.
- Lot Number Extension (E0–E3) : <space> = 0
  A = 1
  O = 15
- Customized number (C0–C11) : fixed number from 0 to 4095 given by the customer.
- Year (Y0–Y3) : 1994 is 0, 1995 is 1, and so on.
- Month (M0–M3) : number from 1 to 12.
- Wafer Number (W0–W7) : number of Wafer.
- Serial Number (S0–S15) : number from 0 to 65535 incremented step by step.

	ADDRESS	b7	b6	b5	b4	b3	b2	b1	b0
TAG1	ECh	L7	L6	L5	L4	L3	L2	L1	L0
TAG2	EDh	L15	L14	L13	L12	L11	L1O	L9	L8
TAG3	EEh	C3	C2	C1	C0	E3	E2	E1	E0
TAG4	EFh	C11	C10	C9	C8	C7	C6	C5	C4
TAG5	FCh	Y3	Y2	Y1	Y0	M3	M2	M1	M0
TAG6	FDh	W7	W6	W5	W4	W3	W2	W1	W0
TAG7	FEh	S7	S6	S5	S4	S3	S2	S1	S0
TAG8	FFh	S15	S14	S13	S12	S11	S10	S9	S8

Secret Tag Example :

TAG1	TAG2	TAG3	TAG4	TAG5	TAG6	TAG7	TAG8
01	04	02	00	**18**	**0A**	**23**	01

- Lot Number = 1025
- Lot Number Extension = 2
- Customized Number = 0
- Production Year = 1995 (1)
- Production Month = August (8)
- Serial Number = 291

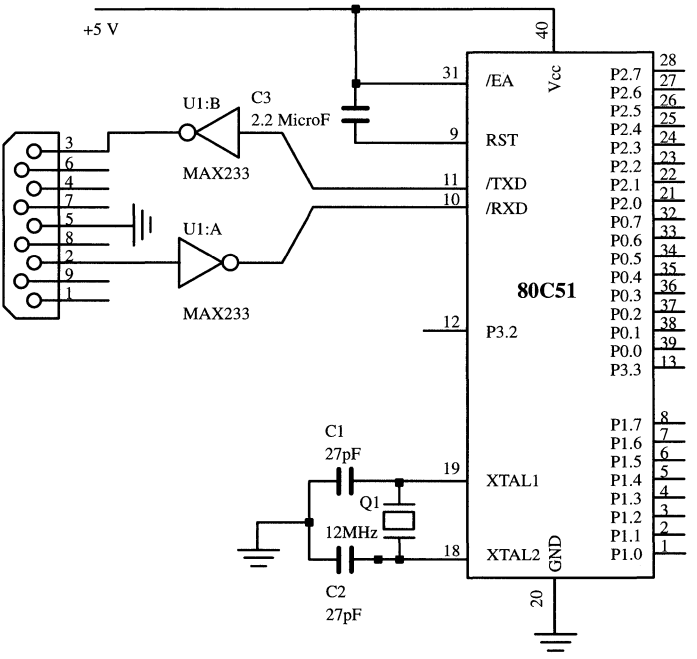
80C51 Routine to Read Out the Secret Tag

The eight secret tag registers are mapped into 80C51 SFR area (Special Function Registers). The routine listed hereafter reads the Secret Tag Registers and sends it on the serial data link .

Main_Program:

```
; ========= UART Initialization ==============
   Mov    SCON,#53H ; 8-bit UART Variable/REN = 1
                    ; TI / RI =1.
   Mov    TMOD,#20H ; 8-bit auto-reload mode for
                    ; baud rate generator.
   Mov    TH1,#0E8H ; 1200bds at 11.059MHZ.
   Setb   TR1
     .
     .
     .
; Somewhere in the program the routine is
; called to transfer the Secret tag registers.
; Call   Secret_Tag_Transfer
     .
     .
; ========= Character Sending Routine =========
Send_Char:
   Jnb    TI,$      ; test if the transmitter is free to
                    ; send a new character.
   Clr    TI
   Mov    SBUF,A    ; send the new character.
   Ret
; ======== Secret Tag Transfer Routine =========
Secret_Tag_Transfer:
   Mov    A,TAG1
   Call   Send_Char
   Mov    A,TAG2
   Call   Send_Char
   Mov    A,TAG3
   Call   Send_Char
```

```
Mov     A,TAG4
Call    Send_Char
Mov     A,TAG5
Call    Send_Char
Mov     A,TAG6
Call    Send_Char
Mov     A,TAG7
Call    Send_Char
Mov     A,TAG8
Call    Send_Char
Ret
```



Additional Information

For additional information on Microcontrollers, and Ordering Information, please refer to the product datasheets available upon request.

How to use a Third Overtone Crystal with a 80C51 Family Microcontroller

Description

For cost reason using an overtone crystal is 5 to 6 times cheaper than a fundamental one. Using this type of crystal is slightly different comparing to a fundamental one . The frequency of an overtone crystal is adjusted on the fundamental one and this one must be trapped by a LC pass–band filter. The typical schematic is shown below.

CP1 and CP2 are the parasitic capacitors due to the packaging and the PCB lay–out. L1 and C1 is the passe–band filter used to trap the fundamental frequency. C2 is a small capacitor to increase a little bit the open–loop gain given by:

$$A \times B = A \times \frac{CP2 + C2}{CP1}$$

where A is the gain a the operating frequency and B is the gain of the feed–back . The frequency of the filter is given below:

$$f_T = \frac{F_Q}{3} = \frac{36.864}{3} = 12.288\ MHz$$

$$L_1 = \frac{1}{(2 \times \pi \times f_T)^2 \times C3}$$

Where C3 = 33 pF

$$L_1 = \frac{1}{(2 \times \pi \times 12.288 \times 10^6) \times (39 \times 10^{-12})} = 4.3\mu H$$

The standard one is 4.7µH and not critical because the bandwidth is large enough . C2 is chosen to be equal to 10pf (a larger value break–down the amplifier and the open loop gain) .

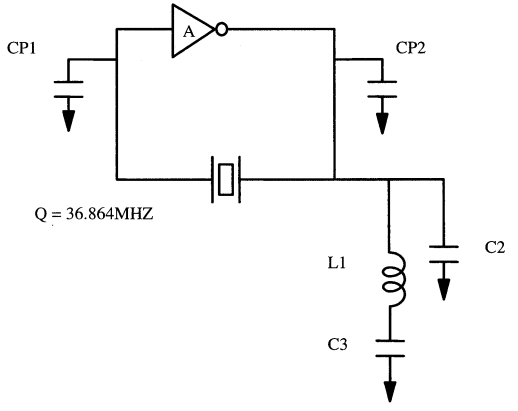


Figure 1. Typical application with a third overtone crystal

How to Read Out the Internal Memory Code of a 80C51 Microcontroller Family

Overview

A single chip microcontroller is a controller with a ROM memory storing the program code of the specific application. The program is masked during the processing of the integrated circuit. The great advantage is that no I/O ressource is consumed to interface the external code memory. I/O line possibilities consequently are increased.

In order to test or to check this internal ROM , some solutions can be implemented.

This application note describes a solution to dump the internal ROM and is based on a specific TEST MODE (TEST MODE VER) used to test the microcontroller in production .

In this note a member of TEMIC's 80C51 family will be named 80Cxxx .

TEST MODE VER to dump the ROM

The TEST MODE VER can be used by setting some 80Cxxx inputs shown in figure 1 . The PORTs P1 and P2 receive respectively the low address lines and the high address lines . The code program in that condition is read from P0 . The lines of PORT0 is open drain and must be tied with 10kohm pull–up resistors .

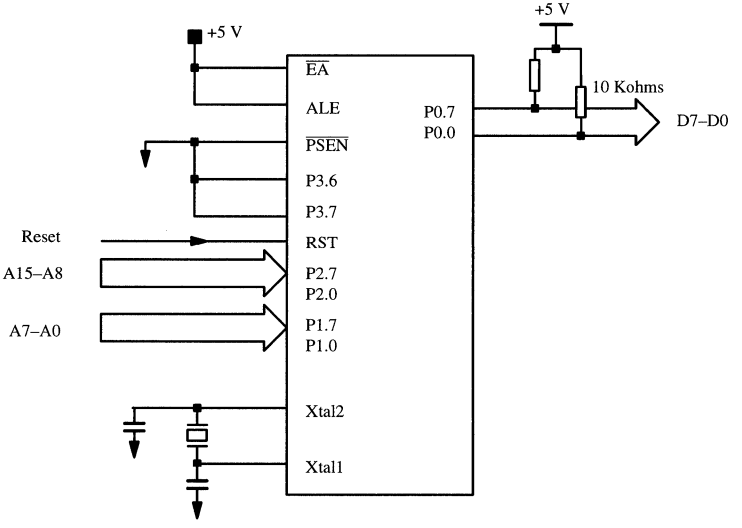


Figure 1. Configuration for the TEST MODE VER

To activate and to dump the ROM a specific timing must be applied, it is shown in figure 2.

Before generating the first Read cycle a delay at least equal to 24 clock periods has to be waited. This time is needed to reset correctly the 80Cxxx. At this time the first address is read by the 80Cxxx from the PORT 1 and 2. To read the first data it is necessary to wait again 12 clock periods. This is due to the internal synchronisation and the internal ROM access time. So the data only appears 36 clock periods after the reset is applied.

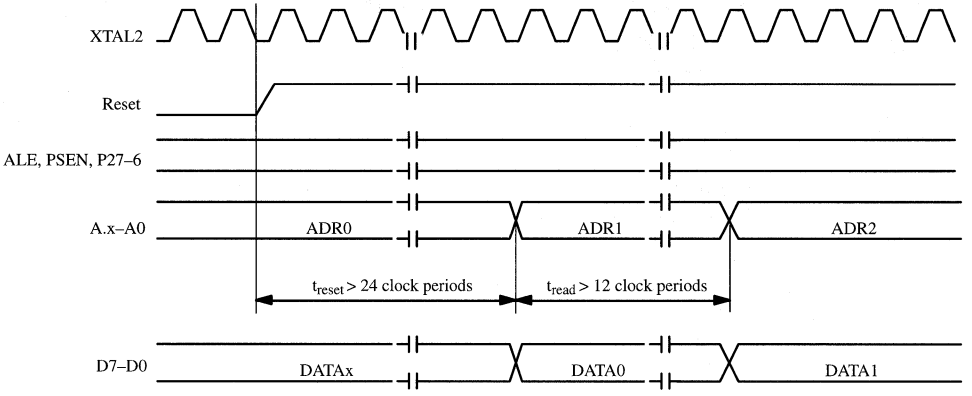


Figure 2. Timings to dump the ROM

Example Dump ROM Application

Figure 3 shows the schematic of this typical application using a 87C51 (OTP version). The main idea is to control the 80Cxxx by another one in order to generate all the signals we need and to output the dumped data on a serial line or to trace the dumped data on PORT0 with a logical analyser.

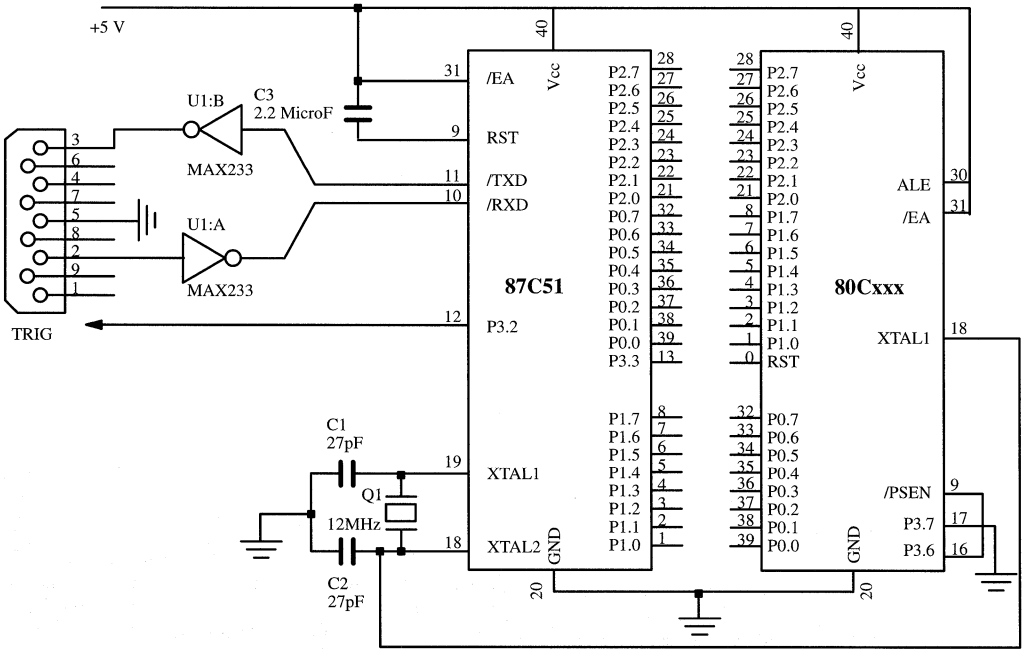


Figure 3. Typical application

Flow chart of the program

Figure 4 shows the flow chart of the program .The program starts with the serial line configuration (2400bds, 8–bit of data) and the set–up of target 80Cxxx for the DUMP operation. Then read operation of the ROM is performed and the read data is transmitted on the serial line. In the same time, the TRIG signal is active low to synchronize an external logical analyser .

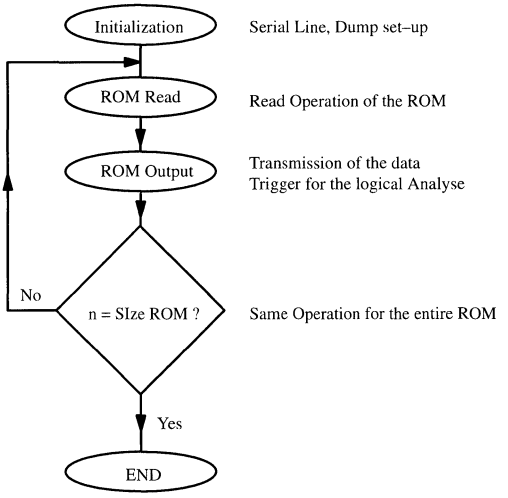


Figure 4. Flow chart for the dump ROM program

Subroutine of the Initialization Sequence

```
;=== initialization ================================
;  Speed = 2400bds , Format = 8 bits
;====================================
;---Set-up the Baud Rate Generator---------------
  SetB   ROM_RST                          ; Target under Reset
  MOV TMOD,#Baud_Rate_Timer               ; TIMER1 = 20H
  MOV TH1,#Speed                          ; Speed = 0F3H
  Setb TR1
;------Set-up the UART-----------------------
  MOV SCON,#FORMAT                        ; FORMAT =42H
;===ROM Dump operation Set-Up==============
;  Size_Rom = 4095 bytes  ,
;---------------------------------
  MOV DPL,#00                             ; starts with first address
```

Subroutine of the dump ROM operation

```
;===ROM Read Operation====================
Dump operation:
  MOV P0,DPL                              ; Address of the Read
  MOV P2,DPH
  CLR  Trig                               ; Analyser TRiggering
  MOV A,P1
  Call Serial_trans                       ; Serial transmission
  SETB Trig
  INC DPTR                                ; Next address
  MOV A,#Size_ROM_Low
  CJNE A,DPL,Dum_operation
  MOV A,#Size_ROM_High
  CJNE A,DPH,Dump_operation
  JMP $
  Serial_trans :
    JNB TI,Serial_trans
    CLR TI
    MOV SBUF,A
    RET
```

Timings analysis

Two parameters are critical in the dump ROM application (figure 2) : **treset** and **tread**.

Treset parameter is the minimum time required from the active Reset to the output of the first data. The minimum value of this parameter is 24 clock periods.

In this application, the first data appears **168 clock periods** after the first address.

To determine when data coming from the ROM can be read, **tread** parameter must be taken into account .

The minimum value of this parameter is 12 clock periods measured when the address is stable and the data can be read.

In this application, **tread** will be read **72 clock periods** after the address is driven. So, both of the parameters are not critical .

Conclusion

This application based on a TEMIC piggy–back is easy to implement and requires only few components.

Furthermore this basic application can be improved by adding a software interface developed on a Personal Computer to compare the dumped ROM and the original one.

Additional Information

For additional information on Microcontrollers, and Ordering Information, please refer to the product datasheets available on request.

Compatibility between 80Cx2 and 8xC154 Microcontrollers

Description

An application based on 80C52/80C32 can be replaced by 83C154/80C154 if some precautions have been taken in order to not activate special features of the 8XC154 contained in one common register. This note gives details about the differences.

Features

The 8XC154 is an enhanced version of the 80C52/80C32. The main differences are mainly due to Internal Program memory, the Power–Down mode, the serial link and the Programmable port impedance.These differences are summarized in Table 1.

Table 1. Main Differences Between Microcontrollers

Features	80C32/80C52	80C154/83C154
ROM (80C52 & 83C154)	8 Kbytes	16 Kbytes
Frame Error Detection	No	Yes
Overrun Error Detection	No	Yes
Recover Mode	No	Yes
Hardware Power–Down Mode	No	Yes
Programmable I/O Port Impedance	No	Yes

Programmable Port Impedance

The impedance of the port 1,2 and 3 can be programmed in one of the three impedance modes through the IOCON register (0F8H) shown in table 2. The impedance can be normal , high or floating .This mode is not supported by the 80C32/80C52 and a program written on 80C32/80C52 never accesses to this register.

Table 2. IOCON register description

I/OCON (0F8h)
I/O Control register

WDT	T32	SERR	IZC	P3HZ	P2HZ	P1HZ	ALF

IZC = 1 — Set by software to select High impedance for Port 1, 2 and 3. When cleared, Port 1, 2 and 3 have a normal impedance.

PxHZ = 1 — When set by software, the Port (1, 2 and 3) become a floating input. When cleared, the impedance is selected by IZC bit.

ALF = 1 — When set by software, all the Ports (1, 2 and 3) become floating when the power–down mode is activated

Power Reduction modes There are basically four power reduction modes in the 8xC154:

- Idle
- Recover
- Software
- Hardware

All these modes are activated with the four bits PD,HPR,RPD and IDL in the PCON register shown in table 3 .

The 80C52/32 has only two power reduction modes : Idle and software power–down modes . All these modes are controlled by the two bits PD and IDL in the PCON register shown in Table 3.

Table 3. PCON register description

PCON (87h) register	SMOD	HPD	RPD	–	GF1	GF0	PD	ID1
	IZC = 1		Set by software to select High impedance for Port 1, 2 and 3. When cleared, Port 1, 2 and 3 have a normal impedance.					

Power–Down Mode

This software mode is used to reduce to the minimum the power consumption (50 µA) . This mode is activated by software by setting to one the bit PD in the PCON register and the way to cancel it depends on the controller used :

- 80C32/80C52 : Only a hardware reset can cancel this mode.
- 8XC154 : A hardware reset or an external interrupt (INT0 or INT1) can cancel this mode.

Idle Mode

This mode is used to reduces the power consumption down to 25% of the nominal consumption and to maintain a minimum of CPU activities (TIMER/COUNTER, UART). This mode is activated by setting to one the bit IDL in the PCON register.The way to cancel it can be done either by an hardware reset or by all the interrupt request sources .

Recover Mode

This mode is used only on the 8XC154 and is enabled by setting to one the bit RPD in the PCON register. This mode controls the way to cancel the power reduction mode (Power–Down and IDLE) and can be either an hardware reset or external interrupt requests (INT0 and INT1). The RECOVER mode allows two ways of cancelling mode :RPD = 0 , the power reduction mode is cancelled by the external interruptions only if they are enabled (EX0=1, EX1=1 in IE register) , RPD = 1 , the power reduction mode is cancelled even if the external interrupts are disabled and if there is an interrupt request.

This mode is not supported by the 80C52/80C32 part and is an enhancement of the 8XC154.

Hardware Power Down Mode

This mode allows to control the Power–Down mode by an external signal through the T1 pin (P3.5). When a falling is applied on this pin and if the HPD bit of the PCON register is set to one, the controller stops the clock and goes in power–down mode. A rising edge on T1 pin awakes the controller, restarts the oscillator and the execution of the program. This mode works independantly of the software mode. **This mode is not supported by the 80C52/80C32 part and is an enhancement of the 8XC154.**

Overrun and Frame Errors

These errors are detected when a problem has been detected on the serial link. If it is the case , the SERR bit in the IOCON register is set to one. The overrun error occured when a new character is received and overwrites the last one which has not been read. The frame error occurs when the length of the data received is not correct (a stop bit is missing). **This mode is supported by the 80C32/80C52 .**

Conclusions

Replacing a 80C32/80C52 by a 8XC154 can be done easily but the programmer must **take care of the RECOVER mode and the HARDWARE power–down mode, which are not to be set in the program**. If no precautions are taken, the application can be disturbed as detailed below:

- Hardware mode : If a rising edge is applied on pin T1, the controller will enter in power–down.
- Recover mode : If the RPD bit is set to one and if the PD bit is set to one as well, the controller will enter in power–down mode and will be cancelled as soon as an interrupt request will be set. If an interrupt is pending, the power–down will be cancelled immediately. In that case it looks like the power–down mode has never been executed.

All other differences will be transparent for the software.

Additional Information

For additional information on Microcontrollers, and Ordering Information, please refer to the following datasheets available on request.

Encryption on 80C51 Family Microcontrollers

Introduction

TEMIC provides a hardware encryption mechanism in order to protect the program memory against piracy.

For this purpose, an encryption array is scrambled within the ROM matrix.

This array is programmed by the factory at the same time as the program memory, its content being different for each application, and is totally secure from outside.

The size of the encryption array depends on the size of the ROM matrix :

- 128 bytes for 80C51
- 256 bytes for 80C52
- 512 bytes for 83C154
- 1024 bytes for 83C154D

When the internal code is read out at a given address, this address selects one byte of the ROM memory map and one byte of the encrypted array following an algorithm.

These two bytes are combined to create an encrypted byte at the output port.

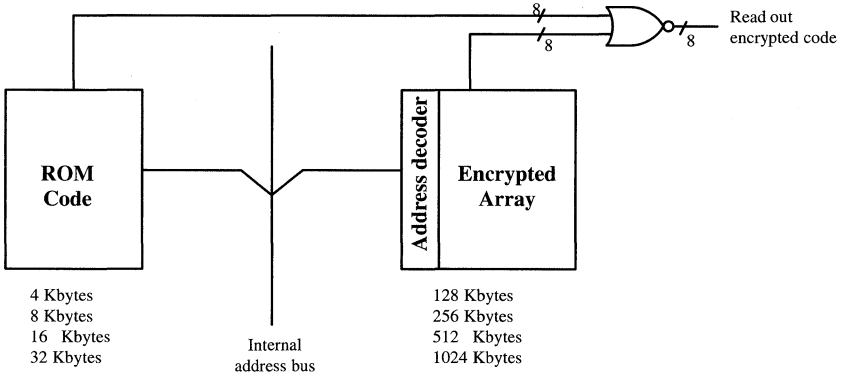
This will be reproduced for each address.

Design Considerations

When the program verification is performed, or when MOVC instructions are executed from external memory for accessing internal memory, each byte of internal ROM is exclusive–nor'ed with an encryption byte, in order to provide on Port 0 an encrypted byte.

The algorithm for selecting one encryption byte uses a combinaison of the internal memory address lines :

- 7 address lines for 80C51
- 8 address lines for 80C52
- 9 address lines for 83C154
- 10 address lines for 83C154D



Adding Features

The External Access pin (EA) is sampled and latched on RESET, and any further switching of this pin is not recognized.

It is always possible to use external memory, but the state of EA during RESET will ascertain what is enabled.

- EA = 0
  - Code memory is exclusively external
  - MOVC instructions access external ROM and return non encrypted data.
- EA = 1
  - Code memory is internal for the lower 4K, and external for the upper bytes for 80C51 (limit is 8K for 80C52, 16K for 83C154 and 32K for 83C154D).
  - MOVC instructions in external ROM code that access internal ROM return encrypted data.

This ensures full protection of ROM content, as detailed in the table below:

Table 1. Use of MOVC intruction to access data in ROM code.

EA	Program counter *	Data pointer *	Program memory	Data	Comments
1	< 4K	< 4K	Internal	Internal	Internal fetches during internal MOVC instruction: data not encrypted
1	< 4K	> 4K	Internal	External	External fetches during internal MOVC instruction: data not encrypted
1	> 4K	< 4K	External	Internal	Internal fetches during external MOVC instruction: data encrypted
1	> 4K	> 4K	External	External	External fetches during external MOVC instruction: data not encrypted
0	X	X	External	External	External fetches during external MOVC instructions: data not encrypted

* : 4K value is for 80C51. Replace by 8K for 80C52, by 16K for 83C154D and by 32K for 83C154D

Additional Information

For additional information on Microcontrollers, and Ordering Information, please refer to the product datasheets available upon request.

How to Get a Second Asynchronous Serial Interface on a 80C51 Microcontroller Family

Description

The 80C51 family has only one asynchronous serial interface.

However some users would like to have a low cost solution to get two in their applications.

This solution exists and is described in this application note.

The goal of this note is to present a very low cost software solution to realise this second asynchronous serial interface.

Features

No external hardware added ;

Full duplex ;

Dissymetrical baud rate in reception and in transmission available ;

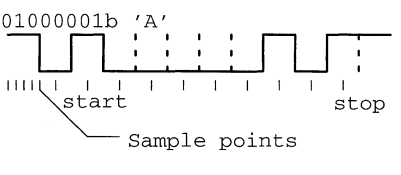
1200 bauds limitation of the internal serial interface (hardware).

Resources used

A time reference with interrupt capability is needed and it can be TIMER 1 even if it is already used as baud rate generator for the internal serial interface. In this case a 32 time speed transmission is obtained on TIMER 1 overflow (TIMER 1 is in mode 2 : 8–bit auto–reload, and serial interface is in mode 1 : 8–bit variable baud rate).

Only two I/O pins are needed : one for RxD and one for TxD (for instance P1.0 and P1.1). Few bytes of memory are used and finally a portion of the CPU time is used to serve TIMER 1 interrupt. Three functions : initialisation, transmission and reception, are allowed to use this serial interface.

Method



Receiver part :

On each TIMER 1 overflow interrupt, RxD input is sampled. Start of transmission is recognised by a transition of 1 to 0 on this pin. So a second sample is made half a bit later to be sure that it is a start bit. Then sampling is made in the middle of the received bits, nine times to get the 8 data bits. The stop bit must have level 1.

Transmitter part :

The operation of the transmitter is nearly the same as for the receiver : start bit is written on TxD output followed by the 8 data bits and the stop bit and so on. Time of bit writing is calculated by counting timer interrupts.

3

Efficiency

Number of machine cycles spent in interrupt sub–routine :

- Minimum : 10 cycles ;
- Maximum : 49 cycles (transmission and reception) ;

The measures hereafter have been done with a 11.059MHz crystal, and same baud rate in emission and in reception, and a hardware serial baud rate of 1200 bauds.

Percentage of CPU usage :

- 41.7% if there is no traffic ;
- 50% with continuous transmission or reception, and 1200 baud rate ;
- 57.4% with continuous transmission and reception, and 1200 baud rate ;
- 68.5% with continuous transmission and reception, and 9600 baud rate.

The hardware serial baud rate is limited to 1200 bauds, increasing it induces an increase of TIMER 1 interrupts frequency, and so an increase of percentage of CPU usage.

Demonstration Program

The demonstration program (listed in the following pages) allows transmission on P1.1 of all characters received on P1.0 without checking receive error.

The function TXD_S starts transmission of the character placed in accumulator when the transmitter is ready.

The function RXD_S waits for reception of a character and return it in accumulator.

Additional Information

For additional information on Microcontrollers, and Ordering Information, please refer to the product datasheets.

Program Listing

```
$TITLE (Software serial interface)      ; Software serial interface
                                        ; with programmable speed
$NOMOD51
$INCLUDE (reg51.inc)      RSEG PROG
NAME UARTSOFT
; Constant definition
       RxD1   EQU         P1.0
       TxD1   EQU         P1.1
; Segment definition
PROG   SEGMENTCODE
VAR1   SEGMENTDATA
BITVAR SEGMENTBIT
STACK  SEGMENTIDATA
       RSEG STACK
       DS 10H                           ; 16 Bytes Stack
; vectors definition
       CSEG AT 0000H                    ; Reset vector
       jmp MAIN
       CSEG AT 001BH                    ; Timer 1 vector
       jmp ITIM1
; bits definition
       RSEG BITVAR
TXRDY: DBIT 1                           ; 1 if transmitter ready
RXRDY: DBIT 1                           ; 1 if receiver ready
RXERR  DBIT 1                           ; 1 if receiver error
INCOM: DBIT 1                           ; 1 if character received
; vars definition
       RSEG VAR1
       ; Receiver
RXSPD: DS 1                             ; speed in reception
RXCH:  DS 1                             ; character in reception
RXCNT: DS 1                             ; internal counter
RXSTAT:DS 1                             ; receiver status
RXCH2: DS 1                             ; last character received
       ; Transmitter
TXSPD: DS 1                             ; speed in transmission
TXCH:  DS 1                             ; character in transmission
TXCNT: DS 1                             ; internal counter
TXSTAT:DS 1                             ; transmitter status
; software serial interface demonstration program
; characters received on P1.0 are transmitted on P1.1
       RSEG PROG
; Main routine
MAIN:  mov    SP,#STACK-1
       lcall  SEINIT                    ; interfaces init.
LOOP:  lcall  RXD_S
       lcall  TXD_S
       sjmp LOOP
```

```
; Initialize serial interfaces
; desired speed is 32 for 1200 bauds, 4 for 9600 bauds
; Oscillator frequency = 11.059 MHz

SEINIT:mov    TCON,#40H              ; Timer 1 enabled
       mov    TMOD,#20H              ; C/T = 0 , mode = 2
       mov    TH1,#0E8H              ; 1200 bauds
       mov    SCON,#52H              ; serial port mode 1
       mov    A,#32                  ; 1200 bauds
       mov    RXSPD,A
       mov    TXSPD,A
       setb   PT1                    ; high priority It.
       setb   TXRDY                  ;transmitter ready
       setb   RXRDY                  ; receiver ready
       clr    RXERR                  ; no error
       mov    IE,#10001000B          ; It. timer 1 enabled
       ret

; Transmission of a character on TxD1
TXD_S: jnb    TXRDY,TXD_S
       mov    C,P
       mov    ACC.7,C                ; set parity
       mov    TXCH,A                 ; character to send
       mov    A,TXSPD                ; 1 bit duration
       rr     A                      ; 1/2 bit duration
       mov    TXCNT,A                ; set counter
       mov    TXSTAT,#0              ; init. status
       clr    TXRDY                  ; start transmission
       ret

; Reading of the received character on RxD1
RXD_S: jnb    INCOM,RXD_S
       mov    A,RXCH2                ; char. received
       clr    INCOM                  ; char. readed
       ret
```

```
; Interrupt routine
ITIM1: jnb     RXRDY,RX1
       ; receiver not busy
       jb      RxD1,TRANS              ; start bit ?
       clr     RXRDY
       push    ACC
       mov     A,RXSPD                 ; 1 bit duration
       rr      A                       ; 1/2 bit duration
       mov     RXCNT,A                 ; load counter
       mov     RXSTAT,#0               ; init. status
       pop     ACC
       sjmp    TRANS
RX1:   djnz    RXCNT,TRANS             ; sample point ?
       push    ACC
       push    PSW
       mov     A,RXSTAT
       jnz     RX3
       jb      RxD1,ERRFRM             ; start bit OK (0) ?
RX2:   inc     RXSTAT
       mov     RXCNT,RXSPD
       sjmp    RX5
ERRFRM:setb    RXRDY
       setb    RXERR                   ; receiver error
       sjmp    RX5
RX3:   cjne    A,#9,$+3                ; 8 bits + stop bit    jnc      RX4
       mov     C,RxD1                  ; bit sampling
       mov     A,RXCH
       rrc     A
       mov     RXCH,A
       sjmp    RX2
RX4:   jnb     RxD1,ERRFRM             ; stop bit OK (1) ?
       mov     RXCH2,RXCH
       setb    RXRDY
       setb    INCOM                   ; 1 char. received
RX5:   pop     PSW
       pop     ACC


TRANS: ; transmission part
       jb      TXRDY,TX5
       djnz    TXCNT,TX5               ; sample point ?
       push    ACC
       push    PSW
       mov     A,TXSTAT
       jnz     TX1                     ; start ?
       clr     TxD1                    ; set start bit
       mov     TXCNT,TXSPD
       inc     TXSTAT
       sjmp    TX4
```

```
TX1:    cjne    A,#9,$+3                ; 8 bits + stop bit
        jnc     TX2
        mov     A,TXCH
        rrc     A                       ; bit to send in carry
        mov     TXCH,A
        mov     TxD1,C                  ; transmission of bit
        mov     TXCNT,TXSPD             ; init. counter
        inc     TXSTAT
        sjmp    TX4
TX2:    cjne    A,#10,TX3               ; end of character ?
        setb    TXRDY
        sjmp    TX4
TX3:    setb    TxD1                    ; set stop bit
        mov     TXCNT,TXSPD
        inc     TXSTAT
TX4:    pop     PSW
        pop     ACC
TX5:    reti

END
```

How to Recognize Video Mode and Generate Free Running Synchronization Signals Using TSC8051C1/C2 Microcontrollers

Description

The TSC8051C1 is an application specific microcontroller for autosync monitor and digital control application. It includes the TEMIC static 8–bit 80C51 CPU core with 8 Kbytes of ROM and 256 bytes of RAM, 12x8–bit PWM channels, buffered HSYNC and VSYNC outputs, a watchdog timer and a multimaster I^2C controller.

This application note describes how to automatically recognize video mode by measuring the period and polarity of horizontal and vertical synchronization signals; it also explains how to generate free running synchronization signal for burn–in purpose.

In the rest of the application note, the use of words Hsync and Vsync means horizontal synchronization signal and vertical synchronization signal respectively.

Typical Autosync Monitor Application

The introduction of the TSC8051C1 in CRT monitors allows manufacturer and final user to get maximum flexibility.

- Automatic parameters adjustment during factory set–up.
- Auto–alignment capabilities.
- Saving of factory default parameters.
- Versatile frequency range up to 100KHz.
- More adjustment parameters are available to the user.
- Automatic video mode recognition that allows automatic monitor adjustment to the values previously saved by user.
- On chip I^2C bus controller allows Access bus implementation and so monitor adjustment by the PC's Keyboard.

Figure 1 shows a block diagram of a typical autosync monitor designed with the TSC8051C1.

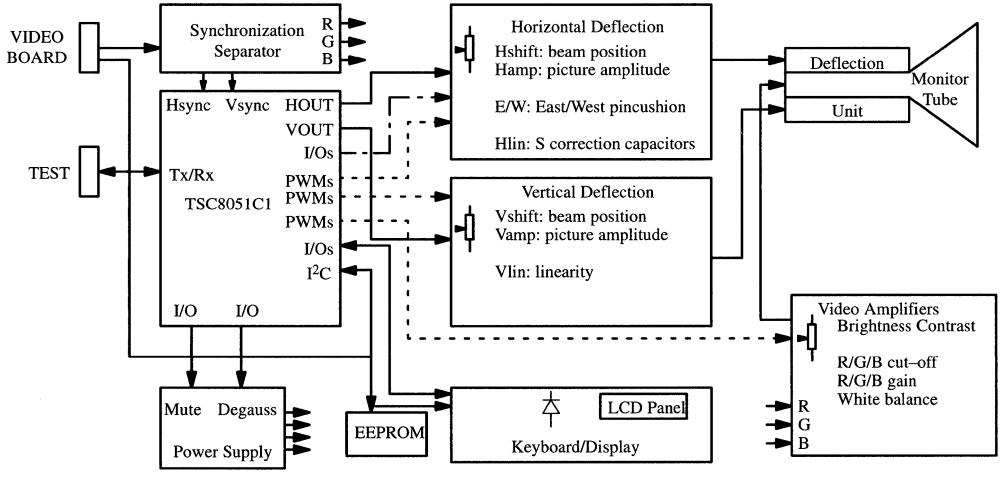


Figure 1. Autosync monitor block diagram with the TSC8051C1

Hardware Description

TSC8051C1 implements some special features to allow video mode recognition without adding any external components.

- Special Hsync and Vsync inputs.
  - Vsync can generate an interrupt on either falling or rising edge. As 8051 core samples inputs one time per machine cycle, pulse duration less than Tosc x 12 (1µs using 12 MHz crystal) are not 100% detected. To allow Hsync pulses counting (duration>150ns), pulses are lengthened up to 1 cycle period to be sampled by the 8051 core. Figure 2 and Figure 3 show the VSYNC and HSYNC input block diagrams.
  - These features are programmable through EICON SFR (address E4h).

MSB **EICON SFR E4h** **LSB**

–	–	–	–	–	T0L	T0S	I0L

Symbol	Position	Name and Function
I0L	EICON.0	INT0/VSYNC input Level bit. Setting this bit inverts INT0/VSYNC input signal. Clearing it allows standard use of INT0/VSYNC input.
T0S	EICON.1	T0/HSYNC input Selection bit. Setting this bit allows short pulse capture. Clearing it allows standard use of T0/HSYNC input.
T0L	EICON.2	T0/HSYNC input Level bit. Setting this bit allows positive pulse capture. Clearing it allows negative pulse capture.

- Special Hsync and Vsync outputs.
- TSC8051C1 implements programmable Hsync and Vsync outputs. User can disable and can invert these outputs to provide good polarity to deflection stages.
- These features are programmable through SOCR SFR (address E5h).

MSB **SOCR SFR E5h** **LSB**

–	–	VOS	HOS	VOP	VOE	HOP	HOE

Symbol	Position	Name and Function
HOE	SOCR.0	HSYNC Output Enable bit. Setting this bit enables the HSYNC signal.
HOP	SOCR.1	HSYNC Output Polarity bit. Setting this bit inverts the HSYNC output.
VOE	SOCR.2	VSYNC Output Enable bit. Setting this bit enables the VSYNC signal.
VOP	SOCR.3	VSYNC Output Polarity bit. Setting this bit inverts the VSYNC output.
HOS	SOCR.4	HSYNC Output Selection bit. Setting this bit selects the VSYNC output, clearing it selects P3.5 SFR bit.
VOS	SOCR.5	VSYNC Output Selection bit. Setting this bit selects the VSYNC output, clearing it selects P3.3 SFR bit.

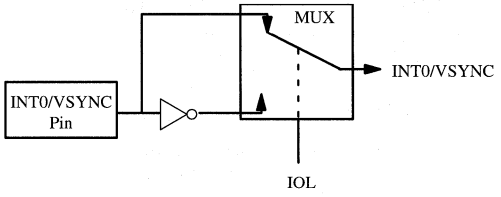


Figure 2. INT0/VSYNC input block diagram

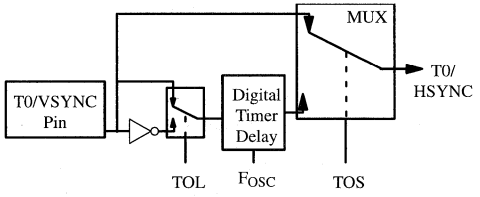


Figure 3. T0/HSYNC input block diagram

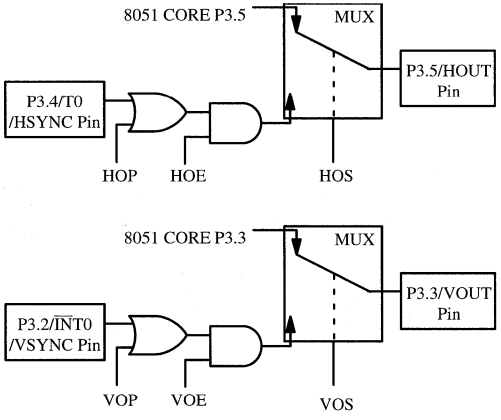


Figure 4. HSYNC and VSYNC outputs block diagram

Video Mode Recognition Description

Vsync input is programmed to generate an interrupt each time a falling edge appears on Vsync.

Vsync period measurement, Vsync polarity detection and Hsync pulse counting are performed using Timer 0. Figure 5 shows the Timer 0 block diagram in mode 1.

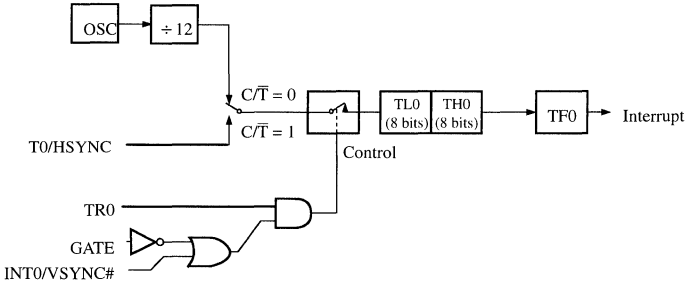


Figure 5. Timer/Counter 0 in mode 1: 16–bit Counter

The measurement cycle is divided in 3 operations (3 Hsync frames):

Timer 0 is reset and Vsync interrupt is enabled.

- Vsync frequency measurement:
- In first interrupt of the cycle, timer 0 is programmed to be used as free running timer with fosc/12 clock. TR0 bit is set to start counting (GATE bit is reset). In the second interrupt, TR0 bit is reset to stop counting. At this time, TH0 and TL0 registers contain a representative value of the Vsync period (in µs if 12MHz crystal is used) (see Figure 6).

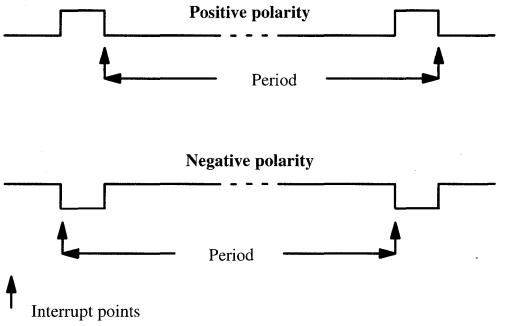


Figure 6. Vsync frequency measurement

- Vsync polarity detection:
- In the second interrupt of the cycle, timer 0 is programmed to be used as gated timer with fosc/12 clock. GATE bit is set and timer counts only during Vsync high level. In the third interrupt, TR0 bit is reset to stop counting. At this time, TH0 and TL0 registers contain a representative value of the Vsync high level duration (in µs if 12MHz crystal is used). If this duration is higher than the Vsync period divided by 2 then, Vsync has a negative polarity else it has a positive polarity (see Figure 7).

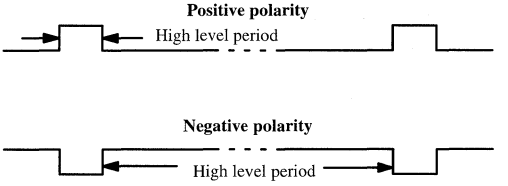


Figure 7. Vsync polarity detection

- Hsync polarity detection:
- In the second interrupt of the cycle, during the Vsync high level duration measurement, the Hsync signal is sampled 16 times, if number of high level samples is greater than 8 then, Hsync has a negative polarity else

it has a positive polarity (see Figure 8). Hsync input filter is then set to accept negative pulses or positive pulses respectively.

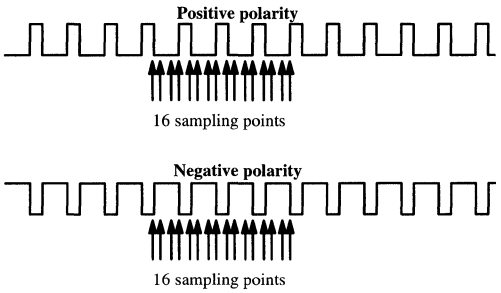


Figure 8. Hsync polarity detection

- Hsync frequency measurement:
- In the third interrupt of the cycle, timer 0 is programmed to be used as external event counter with Hsync clock. TR0 bit is set to start counting. In the fourth interrupt (last of the measurement cycle), TR0 bit is reset to stop counting. At this time, TH0 and TL0 registers contain a representative value of the Hsync period that is the number of Hsync pulses during a Vsync period (see Figure 9). A flag is set to inform main program of the end of cycle.

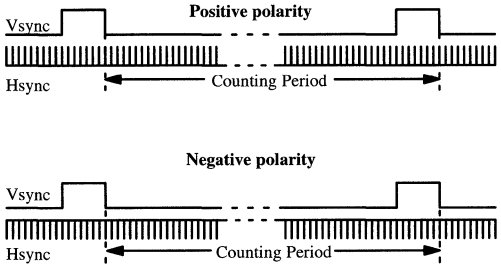


Figure 9. Hsync frequency measurement

When one cycle is completed, the main program checks the values and determines whether if the video mode has changed or not. If yes, the actions to take are listed hereafter:

- Depending on the Hsync frequency, S correction capacitors have to be updated.
- Some PWM values are updated.
- Video mute is activated.
- A research is made in EEPROM to find if the same video mode is already stored.
- If yes recall user set–up (update PWM values) from EEPROM, else default set–up is applied and the video mute is released.

Free Running Generation Description

During manufacturing burn–in, monitors are powered, but no video source is connected to the monitor. To force deflection stages' activity, free running Hsync and Vsync are output.

The software solution for free running generation, offers to the user a maximum of flexibility to program the best frequencies according to the deflection stages.

Two examples are proposed. In the first one, Vsync is a 60.1Hz negative polarity signal with 66µs pulses and Hsync is a 41.7KHz negative polarity signal with 2µs pulses, in the second one Vsync is a 72Hz positive polarity signal with 58µs pulses and Hsync is a 62.5KHz positive polarity signal with 1µs pulses.

Software Description

The software proposed hereafter is divided in two main routines:

- The Vsync Interrupt service routine.
- The Hsync/Vsync free running generation routine.

All the routines are based on a 12MHz oscillator operation; so 1 machine cycle has exactly 1µs duration. In the example, deflection stages are considered having a negative polarity synchronization input. User can program positive Hsync/Vsync outputs, by modifying the software as follows:

```
mov         A,#HOUT_VOUT_ENA
mov         C,Vpol_m
cpl         C     ; set VOP bit for positive
mov         ACC.3,C               ; polarity on Vout
mov         C,Hpol_m
cpl         C     ; set HOP bit for positive
mov         ACC.1,C               ; polarity on Hout
mov         SOCR,A                ; update Vout/Hout polarity
```

Vsync interrupt service routine has the highest priority. Due to the sampling clock, the Vsync period has a basic precision of 1µs. Depending on the instruction executed during the interrupt activation the measured period may be increased up to 4µs. The validation of a new detected video mode is effective only when the difference between the new measured and the previously saved period/counting is significant. This is achieved by the Check_diff subroutine.

The reception of a character on serial port activates one of the two Hsync/Vsync free running generation routine: '1' for the first example, '2' for the second one.

As the generation of the synchronization signals uses 100% of the CPU time, the only ways to disable generation are to clear the activation flag during an interrupt service routine (in the example, the flag is cleared in Vsync interrupt when a video source is input) or to apply a reset.

The listing includes the file reg51c1.inc that is the TSC8051C1 register declarations.

After a new video mode recognition, parameters are stored in the following variables:

```
Vpol_s      Vsync polarity
Hpol_s      Hsync polarity
Vperl_s     Vsync period high order byte
Vperh_s     Vsync period low order byte
Hcntl_s     Hsync count high order byte
Hcnth_s     Hsync count low order byte
```

The table hereafter presents different video modes and their associated parameters.

3

MODE	H. Frequency (KHz)	V. Frequency (Hz)	H. Polarity (Hpol_s)	V. Polarity (Vpol_s)	H. Count (Hcnt_s)	V.period (Vper_s)
EGA 640x350	31.5	70	+ (1)	– (0)	1C2h	37CEh
CGA 640x400	31.5	70	– (0)	+ (1)	1C2h	37CEh
VGA 640x480	31.5	60	– (0)	– (0)	20Dh	411Bh
VGA plus 800x600	35.5	56	+ (1)	– (0)	276h	45C1h
SVGA 800x600	37.8	60	+ (1)	+ (1)	276h	411Bh
VESA 800x600	48	72	+ (1)	+ (1)	29Ch	3641h
8514/a 1024x768	35.5	87	+ (1)	– (0)	198h	2CE6h
1280x1024	63.5	60	+ (1)	+ (1)	422h	411Bh

```
1                ; TEMIC 1996.
2                ; Demonstration program for video mode recognition
3                ; and free running generation with TSC 8051C1
4
5                $RB (0,1)                              ; bank 0 and 1 reserved
                 6   $INCLUDE  (reg51c1.inc)  ; register declarations
                 7   ; TEMIC 1996.
                 8   ; Register declarations for TSC 8051C1 microcontroller
                 9   ; Rev. A
                10
                11   ; BYTE Registers
0080            12   P0               DATA    080H
0090            13   P1               DATA    090H
00A0            14   P2               DATA    0A0H
00B0            15   P3               DATA    0B0H
                16
00D0            17   PSW              DATA    0D0H
00E0            18   ACC              DATA    0E0H
00F0            19   B                DATA    0F0H
0081            20   SP               DATA    081H
0082            21   DPL              DATA    082H
0083            22   DPH              DATA    083H
0087            23   PCON             DATA    087H
0088            24   TCON             DATA    088H
0089            25   TMOD             DATA    089H
008A            26   TL0              DATA    08AH
008B            27   TL1              DATA    08BH
008C            28   TH0              DATA    08CH
008D            29   TH1              DATA    08DH
00A8            30   IE               DATA    0A8H
00B8            31   IP               DATA    0B8H
0098            32   S0CON            DATA    098H
0099            33   S0BUF            DATA    099H
                34
00D8            35   S1CON            DATA    0D8H
00D9            36   S1STA            DATA    0D9H
00DA            37   S1DAT            DATA    0DAH
00DB            38   S1ADR            DATA    0DBH
                39
00AF            40   MSCON            DATA    0AFh
00E4            41   EICON            DATA    0E4h
00E5            42   SOCR             DATA    0E5h
00E6            43   HWDR             DATA    0E6h
00DF            44   PWMCON           DATA    0DFh
00E7            45   MXCRo            DATA    0E7h
00D7            46   MXCR1            DATA    0D7h
00EC            47   PWM0             DATA    0ECh
00ED            48   PWM1             DATA    0EDh
00EE            49   PWM2             DATA    0EEh
00EF            50   PWM3             DATA    0EFh
00F4            51   PWM4             DATA    0F4h
00F5            52   PWM5             DATA    0F5h
00F6            53   PWM6             DATA    0F6h
00F7            54   PWM7             DATA    0F7h
00FC            55   PWM8             DATA    0FCh
00FD            56   PWM9             DATA    0FDh
00FE            57   PWM10            DATA    0FEh
00FF            58   PWM11            DATA    0FFh
                59
                60
                61   ; BIT Registers
                62   ; PSW
00D7            63   CY               BIT     0D7H
```

```
00D6          64    AC              BIT     0D6H
00D5          65    F0              BIT     0D5H
00D4          66    RS1             BIT     0D4H
00D3          67    RS0             BIT     0D3H
00D2          68    OV              BIT     0D2H
00D0          69    P               BIT     0D0H
              70
              71    ; TCON
008F          72    TF1             BIT     08FH
008E          73    TR1             BIT     08EH
008D          74    TF0             BIT     08DH
008C          75    TR0             BIT     08CH
008B          76    IE1             BIT     08BH
008A          77    IT1             BIT     08AH
0089          78    IE0             BIT     089H
0088          79    IT0             BIT     088H
              80
              81    ; IE
00AF          82    EA              BIT     0AFH
00AD          83    ES1             BIT     0ADH
00AC          84    ES0             BIT     0ACH
00AB          85    ET1             BIT     0ABH
00AA          86    EX1             BIT     0AAH
00A9          87    ET0             BIT     0A9H
00A8          88    EX0             BIT     0A8H
              89
              90    ; IP0
00BD          91    PS1             BIT     0BDH
00BC          92    PS0             BIT     0BCH
00BB          93    PT1             BIT     0BBH
00BA          94    PX1             BIT     0BAH
00B9          95    PT0             BIT     0B9H
00B8          96    PX0             BIT     0B8H
              97
              98    ; P3
00B7          99    RD              BIT     0B7H
00B7          100   SDA             BIT     0B7H
00B6          101   WR              BIT     0B6H
00B6          102   SCL             BIT     0B6H
00B5          103   T1              BIT     0B5H
00B5          104   HOUT            BIT     0B5H
00B4          105   T0              BIT     0B4H
00B4          106   HSYNC           BIT     0B4H
00B3          107   INT1            BIT     0B3H
00B3          108   VOUT            BIT     0B3H
00B2          109   INT0            BIT     0B2H
00B2          110   VSYNC           BIT     0B2H
00B1          111   TXD             BIT     0B1H
00B0          112   RXD             BIT     0B0H
              113
              114   ; S0CON
009F          115   SM0             BIT     09FH
009E          116   SM1             BIT     09EH
009D          117   SM2             BIT     09DH
009C          118   REN             BIT     09CH
009B          119   TB8             BIT     09BH
009A          120   RB8             BIT     09AH
0099          121   TI              BIT     099H
0098          122   RI              BIT     098H
              123
              124   ; S1CON
00D85               CR0             BIT     0D8H
00D9          126   CR1             BIT     0D9H
```

```
00DA          127   AA              BIT     0DAH
00DB          128   SI              BIT     0DBH
00DC          129   STO             BIT     0DCH
00DD          130   STA             BIT     0DDH
00DE          131   ENS1            BIT     0DEH
              132
              133
              134
              135
              136   ; CONSTANT DEFINITION
              137   ; --------------------
0080          138   WDT_PER         EQU     80h             ; 2s watchdog period
              139
              140   HOUT_VOUT_SET   EQU     00101000b       ; Hout/Vout=1
00D7          141   HOUT_VOUT_CLR   EQU     11010111b       ; Hout/Vout=0
0035          142   HOUT_VOUT_ENA   EQU     00110101b       ; Hout/Vout enabled
00CF          143   HOUT_VOUT_DIS   EQU     11001111b       ; Hout/Vout disabled
              144
0002          145   EICON_H_NEG     EQU     00000010b       ; negative Hsync selection
0006          146   EICON_H_POS     EQU     00000110b       ; positive Hsync selection
              147
0008          148   VSYNC_DIFF      EQU     8               ; 7us=Vsync diff authorised
0002          149   HSYNC_DIFF      EQU     2               ; 1 pulse=Hsync diff authorised
              150
              151   ; BIT VARIABLE DEFINITION
              152   ; ------------------------
----          153                   BSEG AT 20h
0020          154   Vpol_m:         DBIT    1               ; measured Vsync polarity
0021          155   Hpol_m:         DBIT    1               ; measured Hsync polarity
0022          156   Vpol_s:         DBIT    1               ; saved Vsync polarity
0023          157   Hpol_s:         DBIT    1               ; saved Hsync polarity
0024          158   End_cycle:      DBIT    1               ; measuring end cycle flag (1)
0025          159   Free_run:       DBIT    1               ; Free running generation flag (1)
              160
              161   ; DATA VARIABLE DEFINITION
              162   ; -------------------------
----          163                   DSEG AT 30h
0030          164   Isr_state:      DS      1               ; Interrupt state flag
0031          165   Vperl_m:        DS      1               ; measured period high order byte
0032          166   Vperh_m:        DS      1               ; measured period low order byte
0033          167   Hcntl_m:        DS      1               ; measured count high order byte
0034          168   Hcnth_m:        DS      1               ; measured count low order byte
0035          169   Vperl_s:        DS      1               ; saved period high order byte
0036          170   Vperh_s:        DS      1               ; saved period low order byte
0037          171   Hcntl_s:        DS      1               ; saved count high order byte
0038          172   Hcnth_s:        DS      1               ; saved count low order byte
              173
0039          174   Stack:          DS      10h             ; 16 bytes stack
              175
              176
              177
              178   ;=====================================================================
              179   ;                       BEGIN CODE
              180   ;=====================================================================
              181
              182                   USING   0               ; RB0 used by default
----          183                   CSEG
0000          184                   ORG     0000h           ; reset address
0000 0106     185                   ajmp    Reset
              186
0003          187                   ORG     0003h           ; VSYNC (INT0) interrupt
0003 0200FC   188                   ljmp    Vsync_isr
              189
```

```
                190
                191   ;=======================================================================
                192   ;                           INITIALISATION
                193   ;=======================================================================
                194
0006 758138     195   Reset:          mov     SP,#Stack-1     ; stack pointer initialisation
                196
0009 78FF       197                   mov     R0,#0FFh        ; Internal RAM initialisation
000B 7600       198   Ram_init:       mov     @R0,#00H
000D D8FC       199                   djnz    R0,Ram_init
                200
000F 758DE6     201                   mov     TH1,#0E6h       ; T1 used as baud rate generator
0012 758B00     202                   mov     TL1,#00h        ; at 1200 bauds with 12MHz crystal
0015 758921     203                   mov     TMOD,#21h       ; T0 16b counter, T1 8b autoreload
0018 758841     204                   mov     TCON,#41h       ; T1 run, INT0 falling edge
                205
001B 758700     206                   mov     PCON,#00h       ; SMOD=0
001E 759852     207                   mov     S0CON,#52h      ; 8-bit UART, Rx enabled
                208
0021 75A881     209                   mov     IE,#81h         ; IE0 enabled
0024 75B801     210                   mov     IP,#01h         ; IE0 high priority
                211
0027 75E680     212                   mov     HWDR,#WDT_PER   ; watchdog activation
                213
                214
                215   ;=======================================================================
                216   ;                           MAIN PROGRAM
                217   ;=======================================================================
                218
002A 202410     219   Wait_sync:      jb      End_cycle,Check_mode
002D 75E680     220                   mov     HWDR,#WDT_PER   ; watchdog refresh
                221
                222                   ; here must be inserted the
                223                   ; man-machine interface control
                224
0030 3098F7     225                   jnb     RI,Wait_sync    ; example for free running
0033 C298       226                   clr     RI
0035 E599       227                   mov     A,S0BUF
                228
0037 B43104     229                   cjne    A,#'1',test_car
003A 11B3       230                   acall   H_V_sync_gen_1; Free running generation
003C 012A       231                   ajmp    Wait_sync
                232
003E B432E9     233   test_car:       cjne    A,#'2',Wait_sync
0041 3104       234                   acall   H_V_sync_gen_2
                                                              ; Free running generation
0043 012A       235                   ajmp    Wait_sync
                236
0045 E4         237   Check_mode:     clr     A
0046 A220       238                   mov     C,Vpol_m
0048 92E0       239                   mov     ACC.0,C
004A A222       240                   mov     C,Vpol_s
004C 9400       241                   subb    A,#00
004E 702A       242                   jnz     Mode_changed    ; Vsync polarity changed
                243
0050 A221       244                   mov     C,Hpol_m
0052 92E0       245                   mov     ACC.0,C
0054 A223       246                   mov     C,Hpol_s
0056 9400       247                   subb    A,#00
0058 7020       248                   jnz     Mode_changed    ; Hsync polarity changed
                249
005A A831       250                   mov     R0,Vperl_m
005C A932       251                   mov     R1,Vperh_m
```

```
 005E AA35    252                    mov     R2,Vperl_s
 0060 AB36    253                    mov     R3,Vperh_s
 0062 7C08    254                    mov     R4,#VSYNC_DIFF
 0064 11A0    255                    acall   Check_diff     ; compare new & old period
 0066 7012    256                    jnz     Mode_changed   ; Vsync period changed
              257
 0068 A833    258                    mov     R0,Hcntl_m
 006A A934    259                    mov     R1,Hcnth_m
 006C AA37    260                    mov     R2,Hcntl_s
 006E AB38    261                    mov     R3,Hcnth_s
 0070 7C02    262                    mov     R4,#HSYNC_DIFF
 0072 11A0    263                    acall   Check_diff     ; compare new & old counting
 0074 7004    264                    jnz     Mode_changed   ; Vsync period changed
              265
 0076 C224    266                    clr     End_cycle      ; a new cycle can start
 0078 012A    267                    ajmp    Wait_sync
              268
 007A         269   Mode_changed:
              270
              271   ; user define    setb    Video_mute     ; video mute during mode change
              272   ; user define    acall   Cs_select      ; S correction capacitors update
              273                                           ; depending on Vsync period
              274
 007A 7435    275                    mov     A,#HOUT_VOUT_ENA
 007C A220    276                    mov     C,Vpol_m       ; set VOP bit for negative
 007E 92E3    277                    mov     ACC.3,C        ; polarity on Vout
 0080 A221    278                    mov     C,Hpol_m       ; set HOP bit for negative
 0082 92E1    279                    mov     ACC.1,C        ; polarity on Hout
0084 F5E5     280                    mov     SOCR,A         ; update Vout/Hout polarity
              281
 0086 A220    282                    mov     C,Vpol_m
 0088 9222    283                    mov     Vpol_s,C       ; save new Vsync polarity
 008A 853135  284                    mov     Vperl_s,Vperl_m
 008D 853236  285                    mov     Vperh_s,Vperh_m
                                                            ; save new Vsync period
              286
 0090 A221    287                    mov     C,Hpol_m
 0092 9223    288                    mov     Hpol_s,C       ; save new Hsync polarity
 0094 853337  289                    mov     Hcntl_s,Hcntl_m
 0097 853438  290                    mov     Hcnth_s,Hcnth_m
                                                            ; save new Hsync period
              291
              292   ;    Here must be inserted the research of this video mode in EEPROM
              293   ;    if it is already stored, then recall user's screen parameters
              294   ;    if not, recall factory default screen parameters.
              295   ;    This new mode will be stored in EEPROM after user adjustments
              296
 009A 31F9    297                    acall   Out_results    ; send results to serial port
              298
              299   ; user define    clr     Video_mute     ; end of video mute
 009C C224    300                    clr     End_cycle      ; a new cycle can start
 009E 012A    301                    ajmp    Wait_sync
              302
              303
              304   ;=========================================================================
              305   ;                         SUBROUTINES
              306   ;=========================================================================
              307
              308   ;-------------------------------------------------------------------------
              309   ;
              310   ;      This subroutine checks if the absolute difference of two words
              311   ;      is less than a given byte value
              312   ;
```

```
                313  ;       Inputs:   R0:      word 1 low order byte
                314  ;                 R1:      word 1 high order byte
                315  ;                 R2:      word 2 low order byte
                316  ;                 R3:      word 2 high order byte
                317  ;                 R4:      limit of difference
                318  ;
                319  ;       Outputs:  A:       if A = 0 the difference is less than the limit
                320  ;                          else the difference is greater than or equal to
                                                the limit
                321  ;-------------------------------------------------------------------------
                322
00A0 C3         323  Check_diff:       clr      C
00A1 E9         324                    mov      A,R1
00A2 9B         325                    subb     A,R3          ; A=MSB difference
00A3 700D       326                    jnz      End_check     ; MSB not equal
                327
00A5 E8         328                    mov      A,R0
00A6 9A         329                    subb     A,R2          ; A=LSB difference
00A7 5003       330                    jnc      Check_pos
                331
00A9 C3         332                    clr      C             ; negative difference
00AA EA         333                    mov      A,R2
00AB 98         334                    subb     A,R0          ; A=LSB difference
                335
00AC B50400     336  Check_pos:        cjne     A,AR4,$+3
00AF 5001       337                    jnc      End_check
00B1 E4         338                    clr      A
00B2            339  End_check:       ret
                340
                341
                342
                343  ;-------------------------------------------------------------------------
                344  ;
                345  ;     This subroutine generates free Running synchronization Signals
                346  ;
                347  ;     Hout = 41.7KHz with 2us negative pulses
                348  ;     Vout = 60.1Hz with 66us negative pulses
                349  ;
                350  ;-------------------------------------------------------------------------
                351
00B3 E5E5       352  H_V_sync_gen_1:  mov      A,SOCR
00B5 54CF       353                    anl      A,#HOUT_VOUT_DIS
00B7 F5E5       354                    mov      SOCR,A        ; select P3.3/P3.5 as Vout/Hout
00B9 D225       355                    setb     Free_run      ; set flag (cleared in Vsync isr)
                356
00BB 53B0D7     357  V_pulse_1:       anl      P3,#HOUT_VOUT_CLR
00BE 00         358                    nop
00BF D2B5       359                    setb     HOUT          ; 2us neg pulse on Hout
00C1 790A       360                    mov      R1,#10
00C3 D9FE       361                    djnz     R1,$          ; 20us tempo
                362
00C5 C2B5       363  clr              HOUT
00C7 00         364                    nop
00C8 D2B5       365                    setb     HOUT          ; 2us neg pulse on Hout
00CA 790A       366                    mov      R1,#10
00CC D9FE       367                    djnz     R1,$          ; 20us tempo
                368
00CE C2B5       369                    clr      HOUT
00D0 00         370                    nop
00D1 D2B5       371                    setb     HOUT          ; 2us neg pulse on Hout
00D3 7907       372                    mov      R1,#7
00D5 D9FE       373                    djnz     R1,$          ; 14us tempo
00D7 D2B3       374                    setb     VOUT          ; 66us neg pulse on Vout
```

```
                375
00D9 78E6       376                     mov     R0,#230         ; 230 * 3 Hsync pulses
00DB 00         377   H_pulse_1:        nop
00DC 00         378                     nop
00DD 75E680     379                     mov     HWDR,#WDT_PER ; watchdog refresh
                380
00E0 C2B5       381                     clr     HOUT
00E2 00         382                     nop
00E3 D2B5       383                     setb    HOUT            ; 2us neg pulse on Hout
00E5 790A       384                     mov     R1,#10
00E7 D9FE       385                     djnz    R1,$            ; 20us tempo
                386
00E9 C2B5       387                     clr     HOUT
00EB 00         388                     nop
00EC D2B5       389                     setb    HOUT            ; 2us neg pulse on Hout
00EE 790A       390                     mov     R1,#10
00F0 D9FE       391                     djnz    R1,$            ; 20us tempo
                392
00F2 C2B5       393                     clr     HOUT
00F4 00         394                     nop
00F5 D2B5       395                     setb    HOUT            ; 2us neg pulse on Hout
00F7 7906       396                     mov     R1,#6
00F9 D9FE       397                     djnz    R1,$            ; 12us tempo
                398
00FB 302505     399                     jnb     Free_run,End_gen_1
                                                                ; Free running enabled ?
                400
00FE D8DB       401                     djnz    R0,H_pulse_1
0100 00         402                     nop
0101 01BB       403                     ajmp    V_pulse_1
0103 22         404   End_gen_1:        ret
                405
                406
                407;-------------------------------------------------------------------------------
                408   ;
                409   ;       This subroutine generates free Running synchronization Signals
                410   ;
                411   ;       Hout = 62.5KHz with 1us positive pulses
                412   ;       Vout = 72Hz with 58us positive pulses
                413   ;
                414;-------------------------------------------------------------------------------
                415
0104 E5E5       416   H_V_sync_gen_2: mov     A,SOCR
0106 54CF       417                   anl     A,#HOUT_VOUT_DIS
0108 F5E5       418                   mov     SOCR,A          ; select P3.3/P3.5 as Vout/Hout
010A D225       419                   setb    Free_run        ; set flag (cleared in Vsync isr)
                420
010C 53B0D7     421   V_pulse_2:      orl     P3,#HOUT_VOUT_SET
010F D2B5       422                   clr     HOUT            ; 1us pos pulse on Hout
0111 00         423                   nop
0112 7906       424                   mov     R1,#6
0114 D9FE       425                   djnz    R1,$            ; 12us tempo
                426
0116 C2B5       427                   setb    HOUT
0118 D2B5       428                   clr     HOUT            ; 1us pos pulse on Hout
011A 00         429                   nop
011B 7906       430                   mov     R1,#6
011D D9FE       431                   djnz    R1,$            ; 12us tempo
                432
011F C2B5       433                   setb    HOUT
0121 D2B5       434                   clr     HOUT            ; 1us pos pulse on Hout
0123 00         435                   nop
0124 7906       436                   mov     R1,#6
```

```
0126 D9FE    437                djnz    R1,$            ; 12us tempo
             438
0128 C2B5    439                setb    HOUT
012A D2B5    440                clr     HOUT            ; 1us pos pulse on Hout
012C 00      441                nop
012D 7903    442                mov     R1,#3
012F D9FE    443                djnz    R1,$            ; 6us tempo
0131 D2B3    444                clr     VOUT            ; 58us pos pulse on Vout
             445
0133 78D8    446                mov     R0,#216         ; 216 * 4 Hsync pulses
0135 00      447   H_pulse_2:    nop
0136 00      448                nop
0137 75E680  449                mov     HWDR,#WDT_PER ;watchdog refresh
             450
013A C2B5    451                setb    HOUT
013C D2B5    452                clr     HOUT            ; 1us pos pulse on Hout
013E 00      453                nop
013F 7906    454                mov     R1,#6
0141 D9FE    455                djnz    R1,$            ; 12us tempo
             456
0143 C2B5    457                setb    HOUT
0145 D2B5    458                clr     HOUT            ; 1us pos pulse on Hout
0147 00      459                nop
0148 7906    460                mov     R1,#6
014A D9FE    461                djnz    R1,$            ; 12us tempo
             462
014C C2B5    463                setb    HOUT
014E D2B5    464                clr     HOUT            ; 1us pos pulse on Hout
0150 00      465                nop
0151 7906    466                mov     R1,#6
0153 D9FE    467                djnz    R1,$            ; 12us tempo
             468
0155 C2B5    469                setb    HOUT
0157 D2B5    470                clr     HOUT            ; 1us pos pulse on Hout
0159 00      471                nop
015A 7902    472                mov     R1,#2
015C D9FE    473                djnz    R1,$            ; 4us tempo
             474
015E 302505  475                jnb     Free_run,End_gen_2
                                                        ; Free running enabled ?
             476
0161 D8D2    477                djnz    R0,H_pulse_2
0163 00      478                nop
0164 210C    479                ajmp    V_pulse_2
0166 22      480   End_gen_2:   ret
             481
             482
             483
             484
             485;-------------------------------------------------------------------------
             486   ;
             487   ;       This routine is the VSYNC interrupt service routine
             488   ;
             489;-------------------------------------------------------------------------
             490                USING   1               ; RB1 used in interrupt
             491
0167 C225    492   Vsync_isr:   clr     Free_run        ; stop Free running
0169 302401  493                jnb     End_cycle,Vsync_beg_isr
                                                        ; Cycle not yet treated
016C 32      494                reti
             495
016D C0E0    496   Vsync_beg_isr: push  ACC
016F C0D0    497   push           PSW
```

```
0171 75D008  498                mov     PSW,#08h        ; RB1 selection
0174 E530    499                mov     A,Isr_state     ; load ISR state
             500
0176 B4000F  501   State_0:      cjne    A,#00,state_1
0179 758921  502                mov     TMOD,#21h       ; T0 : free running 16-bit timer
017C 758A00  503                mov     TL0,#00h
017F 758C00  504                mov     TH0,#00h
0182 D28C    505                setb    TR0             ; start measuring Vsync period
0184 0530    506                inc     Isr_state
0186 21F3    507                ajmp    Vsync_end_isr
             508
0188 B40133  509   State_1:      cjne    A,#01,state_2
018B 00      510                nop                     ; nop are inserted for timing
018C 00      511                nop                     ; compensation between start
018D 00      512                nop                     ; and stop counting
018E 00      513                nop
018F C28C    514                clr     TR0             ; stop T0
0191 858A31  515                mov     Vperl_m,TL0
0194 858C32  516                mov     Vperh_m,TH0     ; store Vsync period
0197 758929  517                mov     TMOD,#29h       ; T0 : gated 16-bit timer
019A 758A00  518                mov     TL0,#00h
019D 758C00  519                mov     TH0,#00h
01A0 D28C    520                setb    TR0             ; start measuring Vsync high level
             521
01A2 E4      522                clr     A               ; Hsync polarity detection
01A3 7810    523                mov     R0,#16          ; 16 samples
01A5 A2B4    524   S1_1:        mov     C,HSYNC         ; read pin level
01A7 3400    525                addc    A,#00           ; store state
01A9 D8FA    526                djnz    R0,S1_1
01AB B40800  527                cjne    A,#08,S1_2
01AE 9221    528   S1_2:        mov     Hpol_m,C        ; store Hsync polarity (0 = neg)
01B0 4005    529                jc      S1_3
01B2 75E402  530                mov     EICON,#EICON_H_NEG
                                                        ; negative Hsync pulses selection
01B5 21BA    531                ajmp    S1_4
01B7 75E406  532   S1_3:        mov     EICON,#EICON_H_POS
                                                        ; positive Hsync pulses selection
             533
01BA 0530    534   S1_4:        inc     Isr_state
01BC 21F3    535                ajmp    Vsync_end_isr
             536
01BE B4021B  537   State_2:      cjne    A,#02,state_3
01C1 758925  538                mov     TMOD,#25h       ; T0 : 16-bit counter
01C4 758A00  539                mov     TL0,#00h
01C7 A88C    540                mov     R0,TH0          ; save MSB
01C9 758C00  541                mov     TH0,#00h
01CC D28C    542                setb    TR0             ; start counting Hsync pulses
             543
01CE E532    544                mov     A,Vperh_m       ; Vsync polarity detection
01D0 C3      545                clr     C
01D1 13      546                rrc     A               ; A = Vsync period / 20
01D2 B50800  547                cjne    A,AR0,S2_1      ; test only high order byte
01D5 B3      548   S2_1:        cpl     C
01D6 9220    549                mov     Vpol_m,C        ; store Vsync polarity (0 = neg)
01D8 0530    550                inc     Isr_state
01DA 21F3    551                ajmp    Vsync_end_isr
             552
01DC 00      553   state_3:     nop                     ; nop are inserted for timing
01DD 00      554                nop                     ; compensation between start
01DE 00      555                nop                     ; and stop counting
01DF 00      556                nop
01E0 00      557                nop
01E1 00      558                nop
```

```
01E2 00       559                   nop
01E3 00       560                   nop
01E4 00       561                   nop
01E5 00       562                   nop
01E6 C28C     563                   clr     TR0             ; stop T0
01E8 858A33   564                   mov     Hcntl_m,TL0
01EB 858C34   565                   mov     Hcnth_m,TH0     ; store Hsync pulse count
01EE 753000   566                   mov     Isr_state,#00   ; reset ISR state to start a new
                                                              cycle
01F1 D224     567                   setb    End_cycle       ; set flag for the main program
              568
01F3 D0D0     569   Vsync_end_isr:  pop     PSW
01F5 D0E0     570                   pop     ACC
01F7 32       571                   reti
              572
              573                   USING   0               ; RB0 used by default
              574
              575
              576   ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
              577   ;                                                                       +
              578   ;                   The subroutines hereafter are only used for
                                        demonstration program+
              579   ;                                                                       +
              580   ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
              581
              582   ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
              583   ; Send measured parameters on serial port                               +
              584   ; Vsync period, polarity                                               +
              585   ; Hsync counting, polarity                                             +
              586   ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
01F8 900256   587   Out_results:    mov     DPTR,#Vsync_msge
01FB 512F     588                   acall   Out_msge        ; display Vsync message
01FD E536     589                   mov     A,Vperh_s
01FF 5139     590                   acall   Out_byte
0201 E535     591                   mov     A,Vperl_s
0203 5139     592                   acall   Out_byte        ; display Vsync period
0205 7420     593                   mov     A,#' '
0207 514E     594                   acall   Out_char
0209 742D     595                   mov     A,#'-'
020B A222     596                   mov     c,Vpol_s
020D 5002     597                   jnc     Vpol_neg
020F 742B     598                   mov     A,#'+'
0211 514E     599   Vpol_neg:       acall   Out_char        ; display Vsync polarity
              600
0213 90025F   601                   mov     DPTR,#Hsync_msge
0216 512F     602                   acall   Out_msge        ; display Hsync message
0218 E538     603                   mov     A,Hcnth_s
021A 5139     604                   acall   Out_byte
021C E537     605                   mov     A,Hcntl_s
021E 5139     606                   acall   Out_byte        ; display Hsync count
0220 7420     607                   mov     A,#' '
0222 514E     608                   acall   Out_char
0224 742D     609                   mov     A,#'-'
0226 A223     610                   mov     c,Hpol_s
0228 5002     611                   jnc     Hpol_neg
022A 742B     612                   mov     A,#'+'
022C 514E     613   Hpol_neg:       acall   Out_char        ; display Hsync polarity
022E 22       614                   ret
              615
              616   ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
              617   ; Send a message on serial port                                         +
              618   ; DPTR is the message address                                          +
              619   ; a NUL character is the end of message                                +
```

```
                620  ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
 022F E4        621  Out_msge:        clr     A
 0230 93        622                  movc    A,@A+DPTR
 0231 6005      623                  jz      Out_end        ; last character
 0233 A3        624                  inc     DPTR
 0234 514E      625                  acall   Out_char
 0236 412F      626                  ajmp    Out_msge
 0238 22        627  Out_end:        ret
                628
                629  ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
                630  ; Send a hexadecimal byte on serial port                              +
                631  ; A is the byte to send                                               +
                632  ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
 0239 C0E0      633  Out_byte:        PUSH    ACC
 023B C4        634                  SWAP    A
 023C 5143      635                  ACALL   Out_nib
 023E D0E0      636                  POP     ACC
 0240 5143      637                  ACALL   Out_nib
 0242 22        638                  ret
                639
                640  ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
                641  ; Send a hexadecimal nibble on serial port                            +
                642  ; A is the nibble to send                                             +
                643  ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
 0243 540F      644  Out_nib:         ANL     A,#0FH
 0245 2490      645                  ADD     A,#90H
 0247 D4        646                  DA      A
 0248 3440      647                  ADDC    A,#40H
 024A D4        648                  DA      A
 024B 514E      649                  acall   Out_char
 024D 22        650                  ret
                651
                652  ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
                653  ;Send an ASCII character on serial port                               +
                654  ; A is the character to send                                          +
                655  ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
 024E 3099FD    656  Out_char:        jnb     TI,Out_char
 0251 C299      657                  clr     TI
 0253 F599      658                  mov     S0BUF,A
 0255 22        659                  ret
                660
                661  ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
                662  ; Messages definition                                                 +
                663  ;+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
0256 0A0D5673   664  Vsync_msge:      DB      0Ah,0Dh,'Vsync ',0
 025A 796E6320
 025E 00
025F 0A0D4873   665  Hsync_msge:      DB      0Ah,0Dh,'Hsync ',0
 0263 796E6320
 0267 00
```

Section IV

Introduction to C251 Architecture

C251 Overview/Benefits vs C51

C251 Architecture Overview

Extended 8–bit microcontroller

In the world of 8–bit microcontrollers, the C51 Architecture has become an industry standard for embedded applications. For over 15 years, TEMIC has been a leading provider of this microcontroller family. This unsurpassed experience is the driving force as TEMIC takes this proven family to the next level of performance: the TSC80251 family!

This new C251 Architecture at its lowest performance level (binary mode), is binary code compatible with the 80C51 microcontrollers, hence, attaining an increase in performance has never been easier.

Due to a 3–stage pipeline, the CPU–performance is increased by a factor 5, using existing C51 code without modifications.

Using the new C251 instruction set, the performance will increase up to 15 times at the same clock rate. This performance enhancement is based on the 16–bit instruction bus, allowing for more powerful instructions and additional internal instruction bus, 8–bit and 16–bit data busses.

The 24–bit address bus will allow to access up to 16 Mbytes in a single linear memory space. Please see each individual TSC80251 Product Datasheet for the effective addressable memory range.

Programming flexibility and C–code efficiency are both increased through a Register–based Architecture, the 64–Kbyte extended stack space combining with the new instruction set.
C251 C–compilers are some of the most efficient available (nearly no overhead), coupled with the final codesize which could be a factor of 3 down when compared with the C51 C–compilers.

4

TSC80251 Derivatives

TEMIC is rapidly developing a full family of application specific TSC80251 derivatives. Please see the detailed Datasheet of each product for further information.

These products are designed to help you getting high–performance products to market faster.
Due to the high instruction throughput, the TSC80251 derivatives are focussing on all high–end 8–bit to 16–bit applications.

TSC80251 derivatives are also used in mid–range and lower–end microcontroller applications, where a very low operation frequency is needed, without decreasing the level of CPU–power.
This feature is ideal for today portable applications and EMC sensitive systems.

Typical applications for this family are:

- Automotive:
  - Airbag
  - ABS
  - Gearbox
  - Climate control
  - Car radio
  - Car navigation
- Communication:
  - Cordless phones
  - Cellular phones
  - High speed modems
  - High–end feature phones
  - ISDN phones
  - Line cards
  - Network termination
- Computer:
  - High–end monitors
  - CD–ROM
  - Card–reader
  - Disk drives
  - Computer telephony
- Broadcast media:
  - Set top boxes
  - Audio/video control
  - Signal processing

TEMIC's TSC80251 derivatives are designed around the C251 core, using standard peripherals dedicated to a targetted range of applications.

Here is a selection of peripheral blocks:

- Serial interfaces:
  - UART (Universal Asynchronous Receiver Transmitter)
  - I2C (Inter–Integrated Circuit)
  - SPI (Serial Protocol Interface)
  - µWire (Synchronous Serial Interface)
  - CAN (Control Area Network)
  - J1850
  - USB (Universal Serial Bus)
  - GCI
- Special interfaces:
  - ADC (Analog to Digital Converter)
  - DAC (Digital to Analog Converter)
  - PCA (Programmable Counter Array)
  - PWM (Pulse Width Modulator)
  - Smart Sensor Interfaces
- Control functions:
  - Watchdog Timer
  - Timers/Counters
  - Power monitoring and management
  - Interrupt handler
- Memories:
  - RAM
  - ROM
  - OTPROM
  - EPROM

Most of TEMIC's TSC80251 derivatives are available as ROMless, OTPROM, EPROM and Mask ROM version.

TSC80251 Documentation

The following documentation and Starter tools are available to allow the full evaluation of the TEMIC's TSC80251 derivatives:

- "TSC80251 Design Guides" (for each derivative)
  Contains all information about the products (Block Diagram, Configuration and Memory Mapping, Ports, Peripheral Description, Electrical and Mechanical Information, Ordering Information) and Application Notes.
- "TSC80251 Programmer's Guide"
  Contains all information for the programmer (Architecture, Instruction Set, Programming, Development Tools).
- "TSC80251 Product Starter Kit"
  This kit enables the product to be evaluated by the designer.
  Its contents is:
  - C–Compiler (limited to 2 Kbytes of code)
  - Assembler
  - Linker
  - Product Simulator
  - Optionally TSC80251 Product Evaluation Board with ROM–Monitor
  - Please visit our WWW for updated versions in ZIP format.
- World Wide Web
  Please contact our WWW for possible updated information at http://www.temic.de
- TSC80251 e–mail hotline: C251 @ temic.fr

Microcontroller Architecture

The TSC80251 family of 8–bit microcontrollers is a high–performance upgrade of the widely–used 80C51 microcontrollers. It extends features and performance while maintaining binary–code compatibility, so the impact on existing hardware and software is minimal.

All TSC80251 microcontrollers share a set of common features :

- 24–bit linear addressing and up to 16 Mbytes of memory
- a register–based CPU with registers accessible as bytes, words, and double words
- a page mode for accelerating external instruction fetches
- an instruction pipeline
- an enriched instruction set, including 16–bit arithmetic and logic instructions
- a 64–Kbyte extended stack space
- a minimum instruction–execution time of two clocks (vs. 12 clocks for 80C51 microcontrollers)
- binary–code compatibility with 80C51 microcontrollers

Several benefits are derived from these features :

- preservation of code written for 80C51 microcontrollers
- a significant increase in core execution speed in comparison with 80C51 microcontrollers at the same clock rate
- support for larger programs and more data
- increased efficiency for code written in C

Figure 1. is a functional block diagram of TSC80251 microcontrollers. The core, which is common to all TSC80251 microcontrollers, is described in the next paragraph. Each derivative in the family has its own on–chip peripherals, I/O Ports, external bus, size of on–chip RAM, type and size of on–chip ROM.

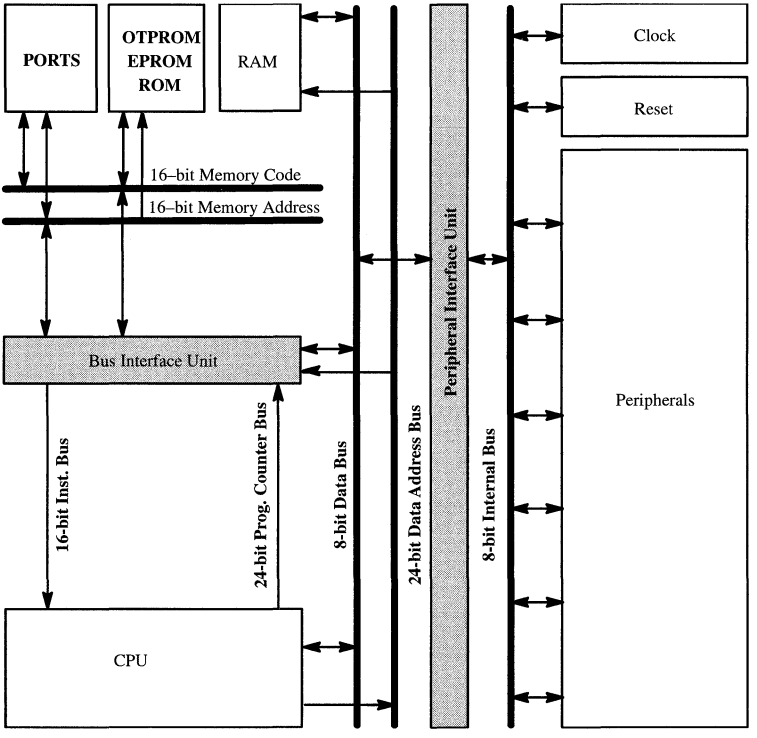


Figure 1. TSC80251 Product Block Diagram

Microcontroller Core

The TSC80251 microcontroller core contains the CPU, the clock and reset unit, the interrupt handler, the bus interface and the peripheral interface (See Figure 1.). The CPU contains the instruction sequencer, ALU, register file and data memory interface (See Figure 2.).

CPU

The TSC80251 fetches instructions from on–chip code memory two bytes at a time or from external memory in single bytes. The instructions are sent over the 16–bit code bus to the execution unit. You can configure the TSC80251 to operate in page mode for accelerated instruction fetches from external memory. In page mode, if an instruction fetch is to the same 256–byte "page" as the previous fetch, the fetch requires one state (two clocks) rather than two states (four clocks). For information regarding the page or non–page mode selection, see Product Datasheet.

The TSC80251 register file has forty registers, which can be accessed as bytes, words and double words. As in the C51 Architecture, registers 0-7 consist of four banks of eight registers each, where the active bank is selected by the program status word (PSW) for fast context switches (See "Programming" chapter).

The TSC80251 is a single–pipeline machine. When the pipeline is full and code is executing from on–chip code memory, an instruction is completed every state time. When the pipeline is full and code is executing from external memory (with no wait states and no extension of the ALE signal) an instruction is completed every two state times.

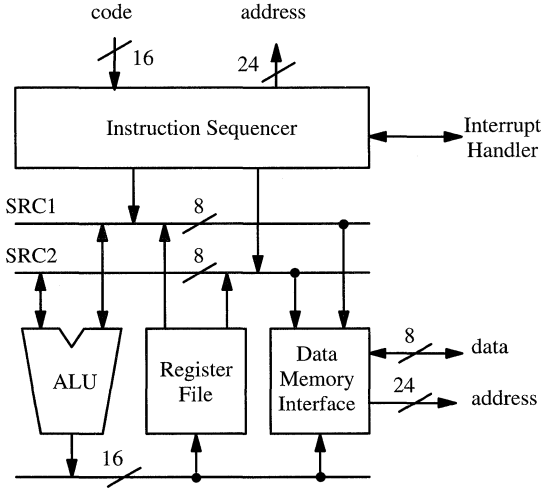


Figure 2. Central Processor Unit Block Diagram

Clock and Reset Unit

The timing source for the TSC80251 microcontroller can be an external oscillator or an internal oscillator with an external crystal/resonator. The basic unit of time in TSC80251 is the state time (or state), which is two oscillator periods. The state time is divided into phase 1 and phase 2 (See Figure 3.).

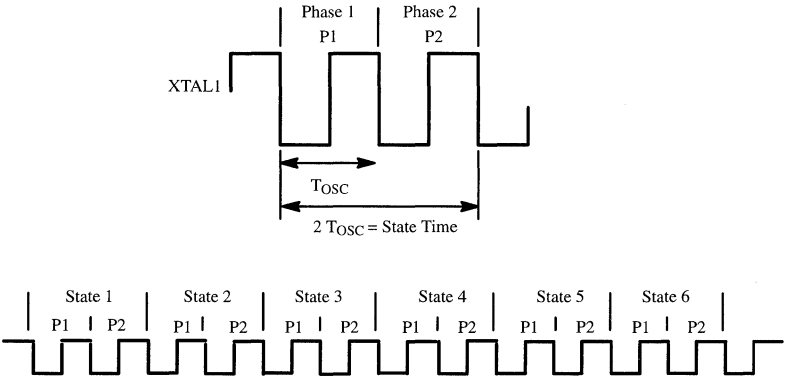


Figure 3. Clocking Definitions

The TSC80251 peripherals operate on a peripheral cycle, which is six state times. (This peripheral cycle is not a characteristic of the C251 Architecture.) A one–clock interval in a peripheral cycle is denoted by its state and phase.

Interrupt Handler

The interrupt handler can receive interrupt requests from many sources: maskable sources and TRAP instruction. When the interrupt handler grants an interrupt request, the CPU discontinues the normal flow of instructions and branches to a routine that services the source that requested the interrupt. You can enable or disable the interrupts individually (except for TRAP which cannot be disabled) and you can assign one of four priority levels to each interrupt.

The reset unit places the TSC80251 into a known state. A chip reset is initiated by asserting the RST pin or allowing the Watchdog Timer to time out when the TSC80251 has one.

AC/DC Characteristics

AC Characteristics

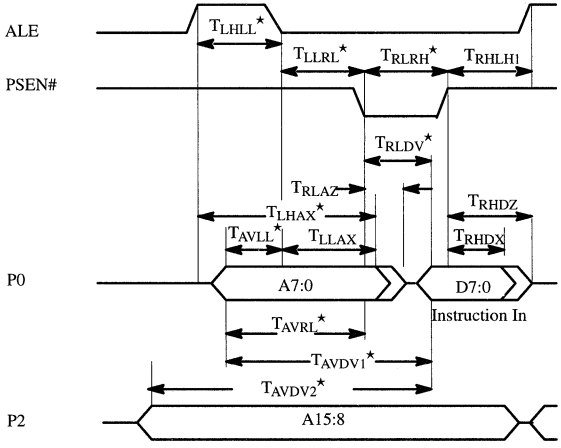
Table 1. AC Characteristics (Capacitive Loading = 50 pF)

Symbol	Parameter	12 MHz		16 MHz		F_{OSC}		Units
		Min	Max	Min	Max	Min	Max	
T_{OSC}	1/F_{OSC}	83		63				ns
T_{LHLL}	ALE Pulse Width	73		53		T_{OSC} -10		ns (2)
T_{AVLL}	Address Valid to ALE Low	63		43		T_{OSC} - 20		ns (2)
T_{LLAX}	Address hold after ALE Low	63		43		T_{OSC} - 20		ns
T_{RLRH} (1)	RD# or PSEN# Pulse Width	65		45		T_{OSC} - 18		ns (3)
T_{WLWH}	WR# Pulse Width	65		45		T_{OSC} - 18		ns (3)
T_{LLRL} (1)	ALE Low to RD# or PSEN# Low	73		53		T_{OSC} - 10		ns
T_{RHRL}	ALE High to RD# or PSEN# High	73		53		T_{OSC} - 10		ns
T_{LHAX}	ALE high to Address hold	147		105		2T_{OSC} - 20		ns (2)
T_{RLDV} (1)	RD# or PSEN# Low to Valid Data/Instruction.		33		13	T_{OSC} - 50		ns (3)
T_{RHDX} (1)	Data/Instruct. hold After RD# or PSEN# high	0		0		0		ns
T_{RLAZ} (1)	RD#/PSEN# Low to Address Float		2		2		2	ns
T_{RHDZ} (1)	Data/Instruct. Float After RD# or PSEN# high		63		43		T_{OSC} - 20	ns
T_{RHLH1} (1)	RD#/PSEN# high to ALE high (Instruction)	68		48		T_{OSC} - 15		ns (1)
T_{RHLH2} (1)	RD#/PSEN# high to ALE high (Data)	235		173		3T_{OSC} - 15		ns (1)
T_{WHLH}	WR# high to ALE high	235		173		3T_{OSC} - 15		ns
T_{AVDV1}	Address (P0) Valid to Valid Data/Instruction In		190		128		3T_{OSC} - 60	ns (2, 3, 4)
T_{AVDV2}	Address (P2) Valid to Valid Data/Instruction In		273		190		4T_{OSC} - 60	ns (2, 3, 4,)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In		128		88		2T_{OSC} - 38	ns
T_{AVRL}	Address Valid to RD#/PSEN# Low	143		101		2T_{OSC} - 24		ns (2)
T_{AVWL1}	Address (P0) Valid to WR# Low	143		101		2T_{OSC} - 24		ns (2)
T_{AVWL2}	Address (P2) Valid to WR# Low	220		158		3T_{OSC} - 30		ns (2)
T_{WHQX}	Data hold after WR# high	63		43		T_{OSC} - 20		ns
T_{QVWH}	Data Valid to WR# high	58		38		T_{OSC} - 25		ns (3)
T_{WHAX}	WR# high to Address hold	147		105		2T_{OSC} - 20		ns
T_{XLXL}	Serial Port Clock Cycle Time	1000		750		12 T_{OSC}		ns

4

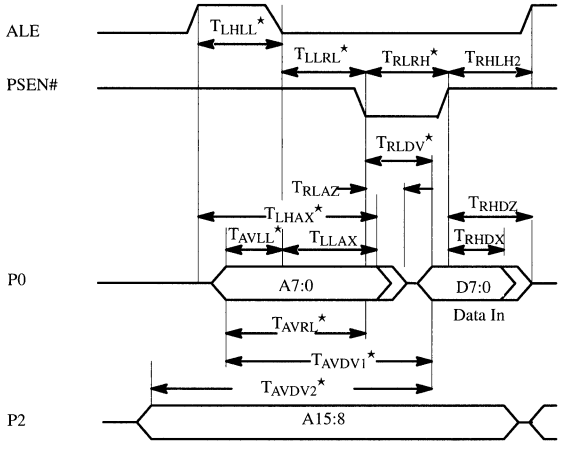
Symbol	Parameter	12 MHz		16 MHz		F_{OSC}		Units
		Min	Max	Min	Max	Min	Max	
T_{QVSH}	Output Data Setup to Clock Rising Edge	870		620		12 T_{OSC} - 133		ns
T_{XHQX}	Output Data hold after Clock Rising Edge	720		510		10 T_{OSC} - 117		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		700		500		10 T_{OSC} - 133	ns

Notes :
1. Specifications for PSEN# are identical to those for RD#.
2. If a wait state is added by extending ALE, add $2T_{OSC}$.
3. If a wait state is added by extending RD#/PSEN#/WR#, add $2T_{OSC}$.
4. If wait states are added as described in both Note 2 and Note 3, add a total of $4T_{OSC}$.



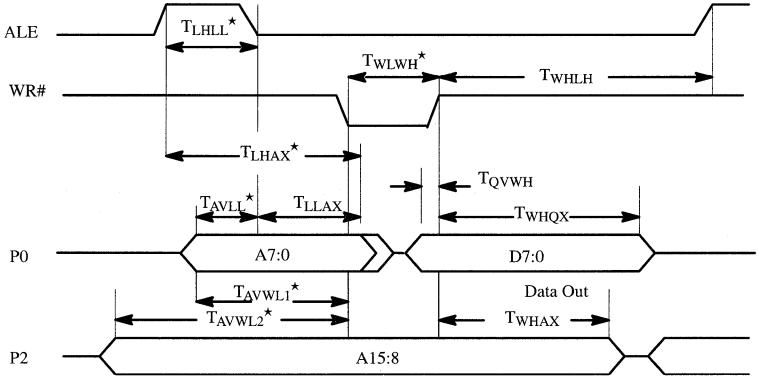
★ The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 1. External Instruction Bus Cycle in Non–Page Mode



★ The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 2. External Data Read Cycle in Non–Page Mode



★ The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 3. External Write Data Bus Cycle in Non–Page Mode

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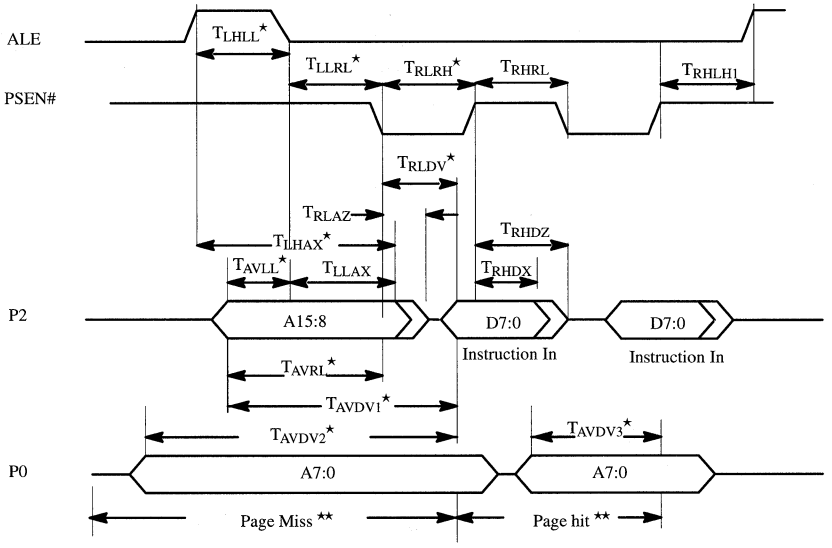
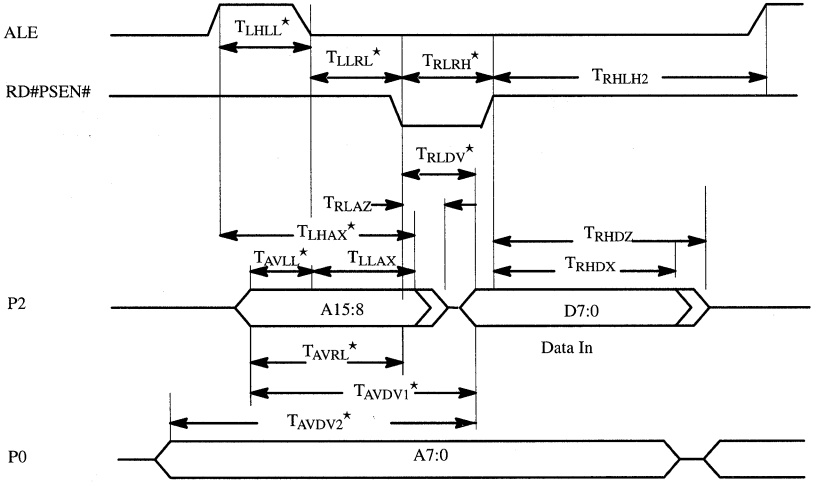


★ The value of this parameter depends on wait states. See the table of AC characteristics.

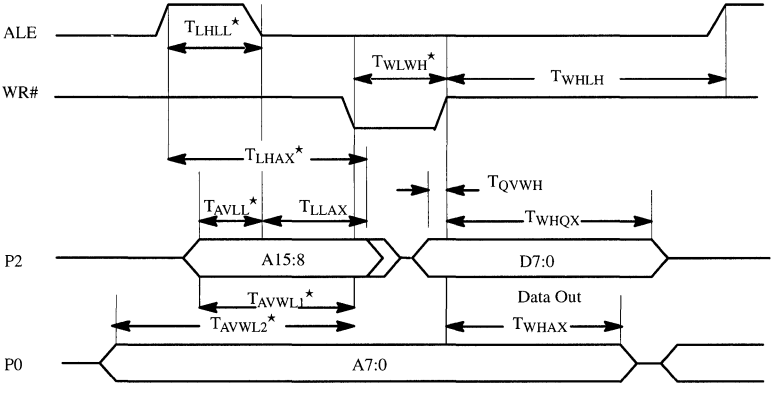
★★ A page hit (i.e., a code fetch to the same 256-byte "page" as the previous code fetch) requires one state ($2T_{OSC}$); a page miss requires two states ($4T_{OSC}$).

Figure 4. External Instruction Bus Cycle in Page Mode



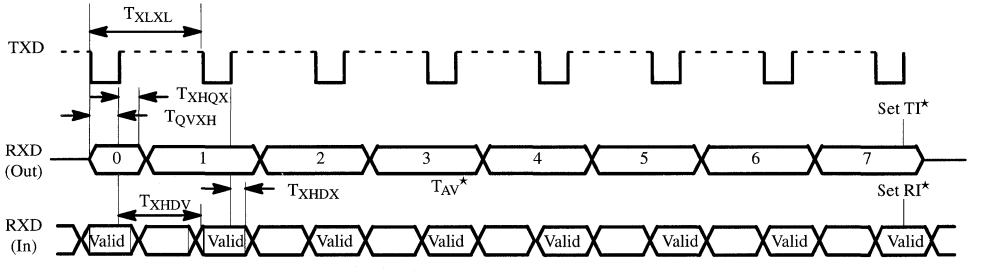
★ The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 5. External Read Data Bus Cycle in Page Mode



★ The value of this parameter depends on wait states. See the table of AC characteristics.

Figure 6. External Write Data Bus Cycle in Page Mode



★ TI and RI are set during S1P1 of the peripheral cycle following the shift of the eight bit.

Figure 7. Serial Port Waveform – Shift Register Mode

Notation for timing parameters name

A = Address	D = Data	E = Enable	G = PROG#	H = high	L = Low
Q = Data out	S = Supply (VPP)	V = Valid	X = No Longer Valid	Z = Floating	

DC Characteristics

Table 2. Absolute Maximum Ratings

• Ambient Temperature Under Bias	
Commercial	0 to +70°C
Industrial	–40 to +85°C
Automotive	0 to +125°C
• Storage Temperature	–65 to +150°C
• Voltage on EA#/VPP Pin to VSS	0 to +13.0 V
• Voltage on any other Pin to VSS	–0.5 to +6.5 V
• I_{OL} per I/O Pin	15 mA
• Power Dissipation	1.5 W

Note:
Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. DC Characteristics

Parameter values applied to all devices unless otherwise indicated.

Commercial
TA = 0 to 70°C
VSS = 0 V
VDD = 5 V ± 10 %

Industrial
TA = –40 to +85°C
VSS = 0 V
VDD = 5 V ± 10 %

Automotive
TA = –40 to +125°C
VSS = 0 V
VDD = 5 V ± 10 %

Symbol	Parameter	Min	Typical (4)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#)	–0.5		0.2VDD - 0.1	V	
V_{IL1}	Input Low Voltage (EA#)	0		0.2VDD - 0.3	V	
V_{IH}	Input high Voltage (except XTAL1, RST)	0.2VDD + 0.9		VDD + 0.5	V	
V_{IH1}	Input high Voltage (XTAL1)	0.7 VDD		VDD + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.3 0.45 1.0	V	I_{OL} = 100 µA I_{OL} = 1.6 mA I_{OL} = 3.5 mA (1, 2)
V_{RST+}	Reset threshold on		3.7		V	
V_{RST-}	Reset threshold off		3.3		V	
V_{RET}	VDD data retention limit		2		V	
V_{OL1}	Output Low Voltage (Ports 0, ALE, PSEN#)			0.3 0.45 1.0	V	I_{OL} = 200 µA I_{OL} = 3.2 mA I_{OL} = 7.0 mA (1, 2)
V_{OH}	Output high Voltage (Ports 1, 2, 3, ALE, PSEN#)	VDD –0.3 VDD –0.7 VDD –1.5			V	I_{OH} = –10 µA I_{OH} = –30 µA I_{OH} = –60 µA (3)

Symbol	Parameter	Min	Typical (4)	Max	Units	Test Conditions
V_{OH1}	Output high Voltage (Port 0 in External Address)	VDD –0.3 VDD –0.7 VDD –1.5			V	I_{OH} = –200 µA I_{OH} = –3.2 mA I_{OH} = –7.0 mA
V_{OH2}	Output high Voltage (Port 2 in External Address during Page Mode)	VDD –0.3 VDD –0.7 VDD –1.5			V	I_{OH} = –200 µA I_{OH} = –3.2 mA I_{OH} = –7.0 mA
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)			- 50 - 75	µA	V_{IN} = 0.45 V Automotive range
I_{LI}	Input Leakage Current (Port 0)			± 10	µA	0.45<V_{IN}<VDD
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)			- 650	µA	VIN = 2.0 V
R_{RST}	RST Pull–Down Resistor	40		225	kΩ	
C_{IO}	Pin Capacitance		10		pF	F_{OSC} = 16 MHz T_A = 25°C
I_{PD}	Powerdown Current		20		µA	
I_{DL}	Idle Mode Current		15		mA	F_{OSC} = 16 MHz
			10		mA	F_{OSC} = 12 MHz
I_{DD}	Operating Current		50		mA	F_{OSC} = 16 MHz
			40		mA	F_{OSC} = 12 MHz

4

Notes:

1. Under steady–state (non–transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: ..... 10 mA
   Maximum I_{OL} per 8–bit port: Port 0 ..... 26 mA
   Ports 1-3 ..... 15 mA
   Maximum Total I_{OL} for all: Output Pins ..... 71 mA
   If I_{OL} exceeds the test conditions, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low–level outputs of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS–level input logic.
3. Capacitive loading on Ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using VDD = 5 V and T_A = 25°C with no guarantee.
They are not tested and there is not guarantee on these values.

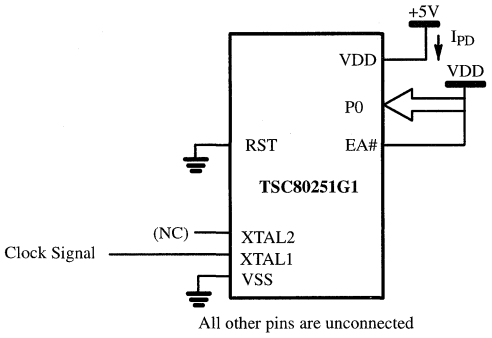


Figure 8. I_{PD} Test Condition, Power–Down Mode

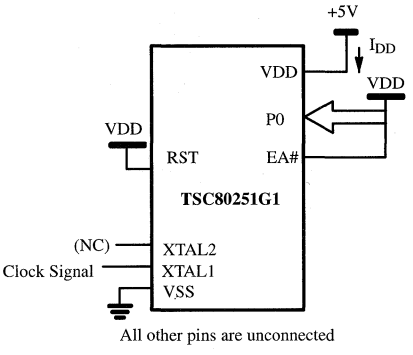


Figure 10. I_{DD} Test Condition, Active Mode

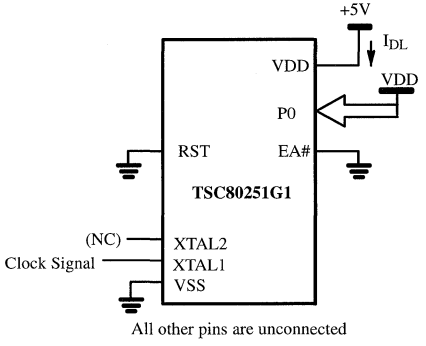


Figure 9. I_{DL} Test Condition, Idle Mode

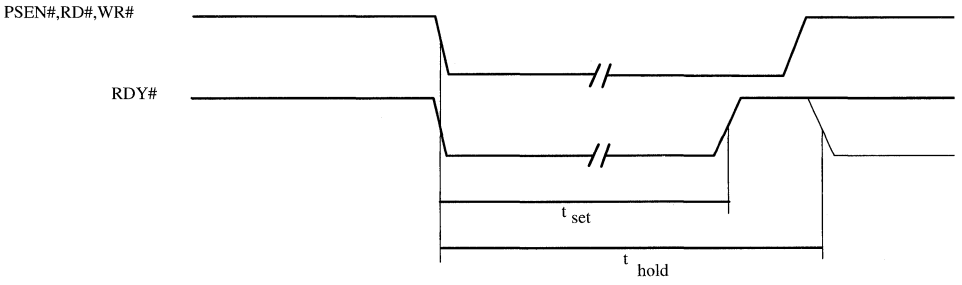


Figure 11. Wait Timings

Table 4. Electrical Parameters

Parameter	Definition	Min	Max	Units
t_{clcl}	Clock period	62,50		ns
t_{set}	Ready valid after strobe (RD#, WR# or PSEN#) low		$(2N+1).t_{clcl} - 15$	ns
t_{hold}	Ready hold after strobe low	$(2N+1).t_{clcl} + 2$		ns

Extended 8–bit TSC80251 Products Overview

Extended 8–bit Microcontroller with Analog Interfaces

General Presentation

The TSC80251A1 products are derivatives of the TEMIC Application Specific Microcontroller family based on the extended 8–bit C251 Architecture described below.

This family of products are tailored to Microcontroller applications requiring analog interface structures.

Three major peripheral blocks have been implemented to provide this facility to the designer:

- Analog to Digital Converter: 4 inputs at 8–bit resolution.
- Pulse Measurement Unit (PMU): 3 modules used to interface to smart analog sensors.
- Event and Waveform Controller (EWC): 5 programmable Counters e.g. for Pulse Width Modulation (PWM) or Compare/Capture functions.

Application focus

Typical applications for these products are CD–ROM, Card or Barcode readers, Monitors, Car Navigation Systems, Airbag and Brake Systems, as well as all kinds of Industrial Control and Measurement Equipment. With the high instruction throughput, the TSC80251A1 products are focussing on all high–end 8–bit to 16–bit applications. They are also well suited to systems where a lower operating frequency is needed to reduce power consumption or Radio Frequency Interference (RFI), while maintaining a high level of CPU–power.

C251 Architecture

The C251 Architecture at its lowest performance level, is Binary Code compatible with the 80C51 Architecture. Due to a 3–stage Instruction Pipeline, the CPU–Performance is increased by up to 5 times, using existing 80C51 code without any modification.

Using the new C251 Instruction Set, the performance will be increased by up to 15 times, at the same clock rate.

This performance enhancement is based on the 16–bit instruction bus and additional internal 8 and 16–bit data busses. The 24–bit address bus will allow an extension of the address space up to 16 Mbytes for future derivatives.

Programming flexibility and C–code efficiency are both increased by the Register–based Architecture, the 64–Kbyte extended stack space, combined with the new Instruction Set.

Combining the above features of the C251 core, the final code size could be reduced by a factor of 3, compared to an 80C51 implementation.

TSC80251A1 Products

The TSC80251A1 is available as a ROMless version (TSC80251A1) or with on–chip Mask Programmable ROM (TSC83251A1). The TSC87251A1 is an EPROM version or OTPROM (One Time Programmable) compatible with the Mask ROM version.

The standard production packages are 44 pins PLCC or TQFP.

The products can be delivered as 12 or 16 MHz versions at 5 Volts and in all major temperature ranges.

Core Features

Based on the extended 8–bit C251 Architecture, the TSC80251A1 includes a complete set of new or improved C51 compatible peripherals as well as a 4 channels 8–bit A/D converter for communication with the analog environment.

The key features of the new C251 Architecture are:

- Register–based Architecture:
  - 40–byte Register File
  - Registers accessible as Bytes, Words, and Double Word.
- 3-stage instruction pipeline
- Enriched Instruction Set
  - 16–bit and 32–bit arithmetic and logic instructions
  - Compare and conditional jump instructions
  - Expanded set of Move instructions
- Reduced Instruction Set
  - 189 generic instructions
  - Free space for additional instructions in the future
  - Additionally all 80C51 instructions are usable in binary mode
- 16–bit internal code fetch
- 64 Kbytes extended stack space
- Maximum addressable memory 16 Mbytes

The benefits of this new architecture are:

- 5 times 80C51 performances in binary mode (80C51 binary code compatibility)
- 15 times 80C51 performances in source mode (full architecture performance)
- Up to a factor 3 of code size reduction (when a C for 80C51 program is recompiled in C251 language)
- Reduction of RFI and power consumption (reduced operating frequency)
- Complete System Development Support
  - Compatible with existing tools
  - New tools available: Compiler, Assembler, Debugger, ICE
- Efficient C language support

Product Features

- 1 Kbyte of internal RAM
- TSC83251A1: 24 Kbytes of on-chip masked ROM
- TSC87251A1: 24 Kbytes of internal programmable ROM (OTP or UV erasable in window package)
- TSC80251A1: ROMless version
- External memory space (Code/Data): 256 Kbytes
- Four 8–bit parallel I/O Ports (Ports 0, 1, 2 and 3 of the standard 80C51)
- Two 16–bit Timers/Counters (Timers 0 and 1 of the standard 80C51)
- Serial I/O Port : full duplex UART (80C51 compatible)
- Three PMU: Pulse Measurement Unit for smart analog interface

For each of the three modules:

- 8–bit prescaler
- 8–bit Timer for period and width measurements (duty cycle)
- The measurement can start either on the rising or on the falling edge
- One interrupt
- Only one port line is used

- EWC: Event and Waveform Controller
  - High-speed output
  - Compare/Capture inputs
  - PWM: Pulse Width Modulator
  - Watchdog Timer capabilities
  - Compatible with PCA: Programmable Counter Array (5 x 16–bit modules)
- 8–bit Analog to Digital Converter
  - 4 channels
  - Conversion time: 600 clock periods (37.5 µs at 16 MHz)
- Power Management
  - Power–On reset (integrated on the chip)
  - Power–Off flag (cold and warm resets)
  - Power-Fail detector
  - Power consumption reduction
    - Software programmable system clock
    - Idle and Power–Down modes
- Power Supply: 5V ± 10%
- Up to 16 MHz operation and three temperature ranges(*):
  - Commercial (0 to 70°C)
  - Industrial (–40 to +85°C)
  - Automotive (–40 to +125°C)
- Packages: PLCC44, CQPJ44 (window) and TQFP44(**)

*Please contact your sales office for availability of speed options
** Please contact your sales office for TQFP availability

Block Diagram

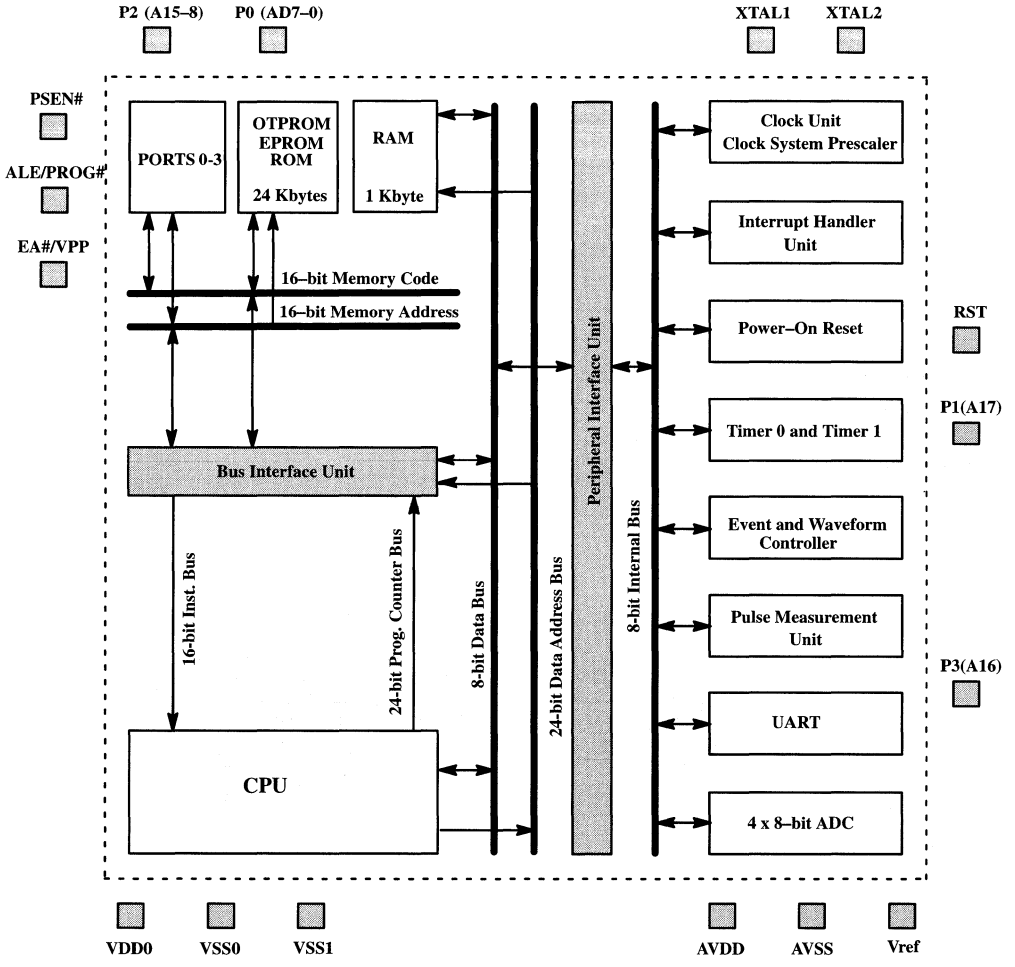


Figure 1. TSC80251A1 Block Diagram

Pin Description

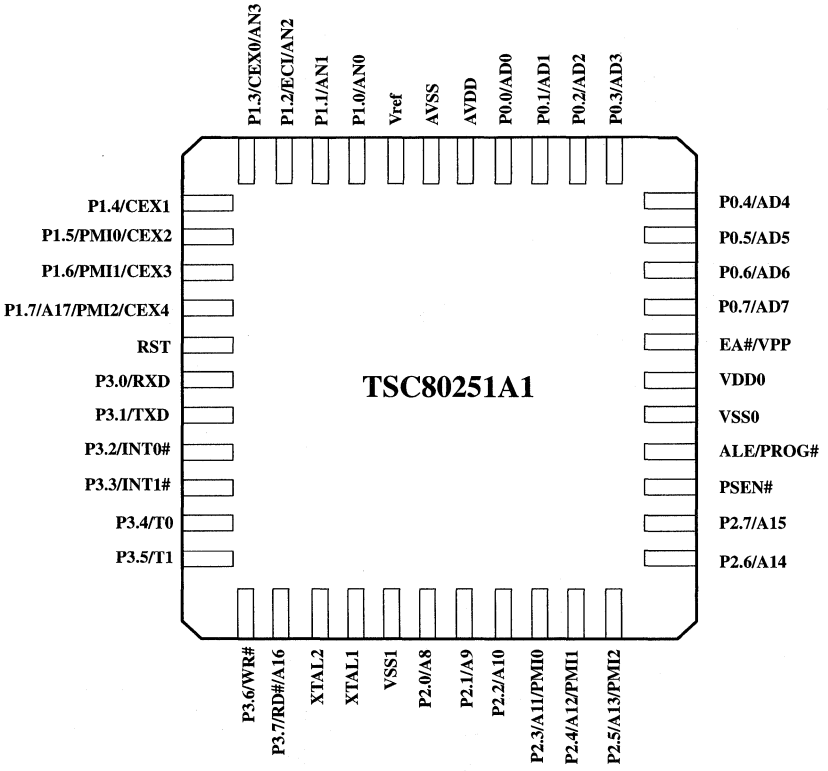


Figure 1. TSC80251A1 Pin Description

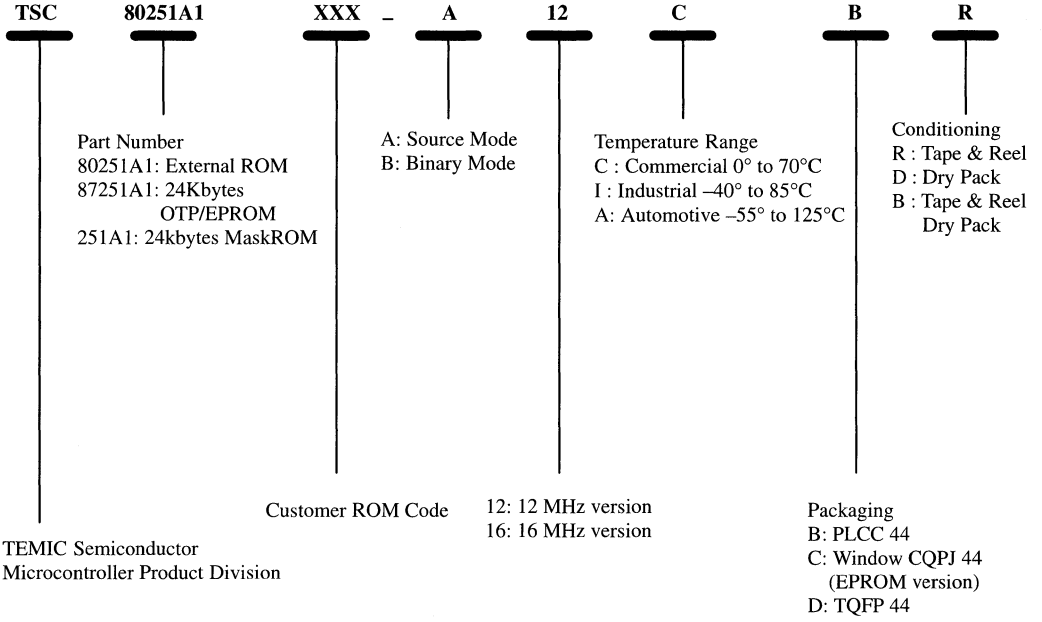
Table 1. TSC80251A1 pin description

Pin	Type	Description
P0.0:7	I/O	**Port 0** This is an 8–bit open–drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high–impedance inputs. It is also Address/Data lines AD0:7, which are multiplexed lower address lines and data lines for external memory. **External pull–ups are required during program verification.**
P1.0:7	I/O	**Port 1** This is an 8–bit bidirectional I/O port. It receives the low–order address byte during EPROM programming and verification. It serves also the functions of various special features: P1.0 AN0 : Analog Input 0, P1.1 AN1 : Analog input 1, P1.2 ECI : EWC External Clock input. AN2 : Analog input 2, P1.3 CEX0 : EWC module 0 Capture input/PWM output. AN3 : Analog input 3, P1.4 CEX1 : EWC module 1 Capture input/PWM output, P1.5 PMI0 : Pulse Measurement input 0, CEX2 : EWC module 2 Capture input/PWM output. P1.6 EAD6 : External Address line 6, PMI1 : Pulse Measurement input 1, CEX3 : EWC module 3 Capture input/PWM output. P1.7 A17 : Address line for the 256–Kbyte memory space depending on the byte CONFIG0 PMI2 : Pulse Measurement input 2, CEX4 : EWC module 4 Capture input/PWM output.
P2.0:7	I/O	**Port 2** This is an 8–bit bidirectional I/O port with internal pull-ups. It is also Address lines A8:15, which are upper address lines for external memory.
P3.0:7	I/O	**Port 3** This is an 8–bit bidirectional I/O port with internal pull-ups. It receives the high–order address bits during EPROM programming and verification. It serves also the functions of various special features: P3.0 RXD : Serial Port Receive Data input. P3.1 TXD : Serial Port Transmit Data output. P3.2 INT0# : External Interrupt 0. P3.3 INT1# : External Interrupt 1. P3.4 T0 : Timer 0 external clock input. P3.5 T1 : Timer 1 external clock input. P3.6 WR# : Write signal for external access. P3.7 A16 : Address line for 128–Kbyte and 256–Kbyte memory space depending on the byte CONFIG0, RD# : Read signal for external access, depending on the byte CONFIG0.
ALE/PROG#	I/O	**Address Latch Enable/Program Pulse** It signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. An external latch can use ALE to demultiplex the address from address/data bus. It is also used as the Program Pulse input PROG#, during EPROM programming.
PSEN#	O	**Program Store Enable/Read signal output** This output is asserted for a memory address range that depends on bits RD0 and RD1 in configuration byte CONFIG0.
EA#/VPP	I	**External Access Enable/Programming Supply Voltage** This input directs program memory accesses to on–chip or off–chip code memory. For EA# = 0, all program memory accesses are off-chip. For EA# = 1, an access is on-chip OTPROM/EPROM/ROM if the address is within the range of the on–chip OTPROM/EPROM/ROM; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without ROM on-chip, EA# must be strapped to ground. It receives also the Programming Supply Voltage VPP during EPROM programming operation.
Vref	I	Voltage reference for the Analog to Digital Converter
VSS0	GND	Digital Ground

4

Pin	Type	Description
VDD0	PWR	Digital Supply Voltage
VSS1	GND	Digital Ground
AVSS	GND	Analog Ground
AVDD	PWR	Analog Supply Voltage
RST	I	**Reset input to the chip** Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and VDD0. Asserting RST when the chip is in Idle mode or Power–Down mode returns the chip to normal operation.
XTAL1	I	**Input to the on–chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing.
XTAL2	O	**Output of the on–chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.

Ordering Information



4

Examples

Part Number	Description
TSC80251A1–A16CBR	ROMless, Source Mode, 16 MHz, PLCC 44, 0 to 70°C, Tape and Reel
TSC87251A1–A12CB	OTP, Source Mode, 12 MHz, PLCC 44, 0 to 70°C
TSC87251A1–A12CBR	EPROM, Source Mode, 12 MHz, PLCC 44, 0 to 70°C, Tape and Reel

Development Tools

Part Number	Description
TSC80251A1–SKA	Software Starter Kit Keil
TSC80251A1–SKB	Software Starter Kit Tasking
TSC80251A1–EKA	Evaluation Kit Keil
TSC80251A1–EKB	Evaluation Kit Tasking

Product Marking :

TEMIC
Customer P/N
Temic P/N
Ⓜ© Intel'95
YYWW Lot Number

Extended 8–bit Microcontroller with Serial Communication Interfaces

General Presentation

The TSC80251G1 products are derivatives of the TEMIC Application Specific Microcontroller family based on the extended 8–bit C251 architecture described below.

This family of products are tailored to microcontroller applications requiring highly increased instruction throughput and addressable memory space combined with an optimized internal power management.

Three major features have been implemented to provide optimized performance to the designer:

- Serial Communication Interfaces: I2C/μWire/SPI and RS232 protocols
- Power Monitoring and Management Unit:
  - Power–Fail reset
  - Internal clock prescaler
  - Power–Down mode (current < 20μA)
- 256 Kbytes of external addressable memory for code and data

Application Focus

Typical applications for these products are ISDN–terminals, digital and analog subscriber linecards, PABX systems, networking applications, high speed modems, computer peripherals or similar systems in other segments. With the high instruction throughput, the TSC80251G1 products are focusing on all high–end 8–bit to 16–bit applications. They are also well suited to systems where a lower operating frequency is needed to reduce power consumption or Radio Frequency Interference (RFI), while maintaining a high level of CPU power.

4

C251 Architecture

The C251 architecture at its lowest performance level, is binary code compatible with the 80C51 architecture. Due to a 3–stage instruction pipeline, the average CPU performance is increased by 5 times, using existing 80C51 code without any modification.
Using the new C251 instruction set, the performance is increased by up to 15 times, at the same clock rate. This performance enhancement is based on a new 16–bit and even partly 32–bit oriented powerful instruction set, and additional internal 8 and 16–bit data busses. A 24–bit address bus will allow an extension of the address space up to 16 Mbytes for future derivatives.
Programming flexibility and C–code efficiency are both increased by the register–based architecture, the 64–Kbyte extended stack space and the new instruction set.
Combining the above features of the C251 core, the final code size could be reduced by a factor of 3, compared to an 80C51 implementation.

TSC80251G1 Products

The TSC80251G1 is available as a ROMless version (TSC80251G1) or with on–chip Mask Programmable ROM (TSC83251G1). The TSC87251G1 is an EPROM version compatible to the Mask ROM version.
The standard production packages are 44 pins PLCC or QFP, 40 pins PDIL.
All products can be delivered as 12 or 16 MHz versions at 5 Volts and in all major temperature ranges. ROMless and Mask ROM versions are also available in 3 Volts.

Core Features

Based on the extended 8–bit C251 architecture, the TSC80251G1 includes a complete set of new or improved C51 compatible peripherals as well as multiple protocol serial interfaces.

The key features of the new C251 architecture are:

- Intel's MCS®251 compliance
- Register–based architecture:
  - 40–byte register file
  - Registers accessible as bytes, words, and double word
- 3-stage instruction pipeline
- Enriched instruction set
  - 16–bit and 32–bit arithmetic and logic instructions
  - Compare and conditional jump instructions
  - Expanded set of move instructions
- Reduced instruction set
  - 189 generic instructions
  - Free space for additional instructions in the future
  - Additionally all 80C51 instructions are usable in binary mode
- 16–bit internal code fetch
- 64 Kbytes extended stack space
- Maximum addressable memory of 16 Mbytes

The benefits of this new architecture are:

- 5 times 80C51 performances in binary mode (80C51 binary code compatibility)
- 15 times 80C51 performances in source mode (full architecture performance)
- Efficient C language support: up to a factor 3 of code size reduction (when a C program for 80C51 is recompiled in C251 language)
- Complete system development support
  - Compatible with existing tools
  - New tools available: C–Compiler, Assembler, Debugger, ICE
- Reduction of RFI and power consumption (reduced operating frequency)

Product Features

- C251 core based (MCS®251Intel compliance)
- Pin–Out compatibility with 80C51 standard products
- 1 Kbyte of internal RAM
- TSC83251G1: 16 Kbytes of on–chip masked ROM
- TSC87251G1: 16 Kbytes of internal programmable ROM (OTP or UV erasable in window package)
- TSC80251G1: ROMless version
- External memory space (Code/Data) programmable from 64 Kbytes to 256 Kbytes
- Four 8–bit parallel I/O Ports (Ports 0, 1, 2 and 3 of the standard 80C51)
- Three 16–bit Timers/Counters (Timers 0, 1 and 2 of the standard 80C51)
- Serial I/O Port: full duplex UART (80C51 compatible) with independent Baud Rate Generator
- EWC: Event and Waveform Controller
  - Compatible with PCA: Programmable Counter Array (5 × 16–bit modules)
  - High–speed output
  - Compare/Capture I/O
  - 8–bit Pulse Width Modulator (PWM)
  - Watchdog Timer capabilities
- SSLC: Synchronous Serial Link Controller
  - I2C protocol
  - µWire and SPI protocols
- Hardware Watchdog Timer
- Power Monitoring and Management
  - Power–Fail reset
  - Power–On reset (integrated on the chip)
  - Power–Off flag (cold and warm resets)
  - Software programmable system clock
  - Idle and Power–Down modes
- Keyboard interrupt on Port 1
- Non Maskable Interrupt input (NMI)
- Real–time Wait states input (WAIT#)
- Power Supply: 5 V +/– 10% and 3 V +/– 10% (*)
- Up to 16 MHz operation and three temperature ranges:
  - Commercial (0 to +70°C)
  - Industrial (–40 to +85°C)
  - Automotive (–40 to +125°C)
- Packages : PLCC44, CQPJ44 (window), QFP44 and PDIL40 (**)

* Please contact your sales office for availability of 3 V option
** Please contact your sales office for QFP and PDIL availability

Block Diagram

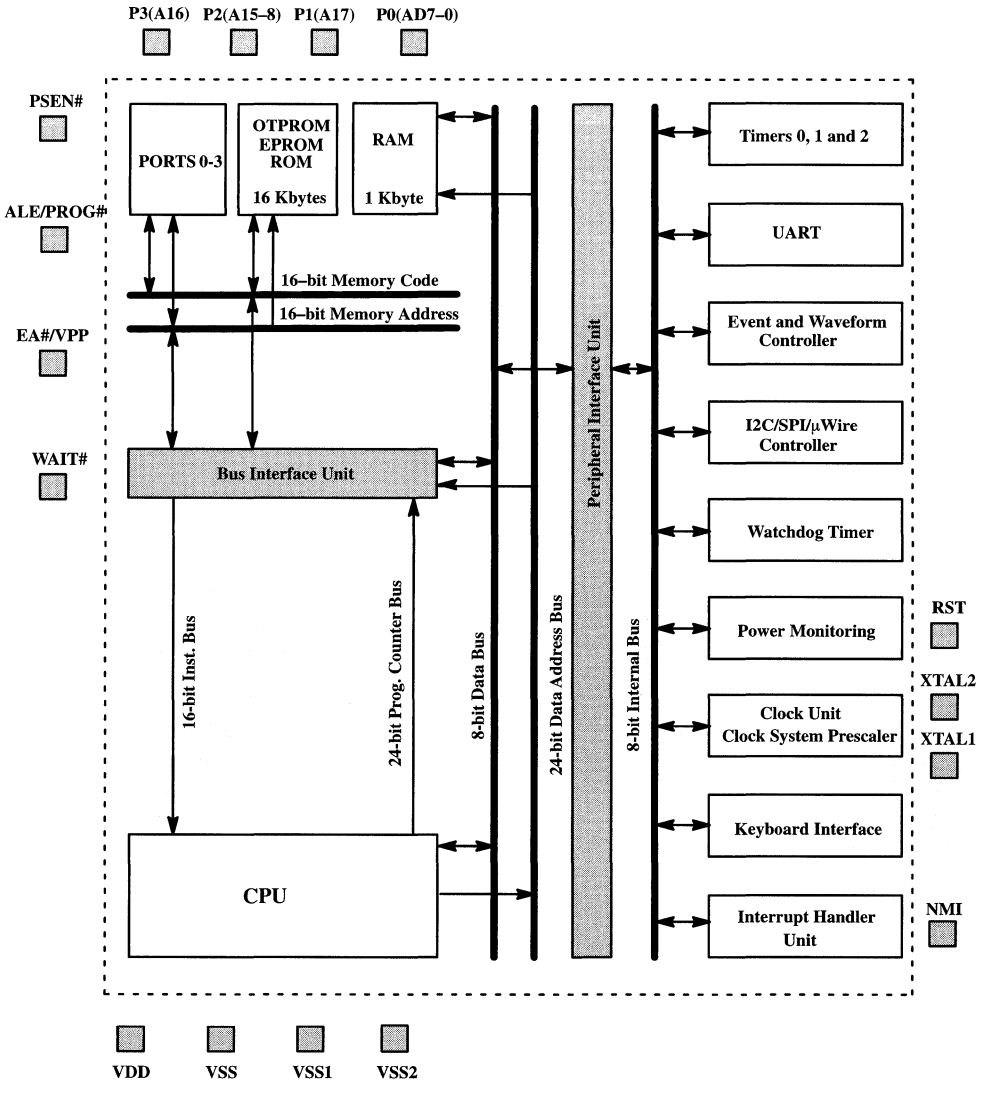


Figure 2. TSC80251G1 Block Diagram

Pin Description

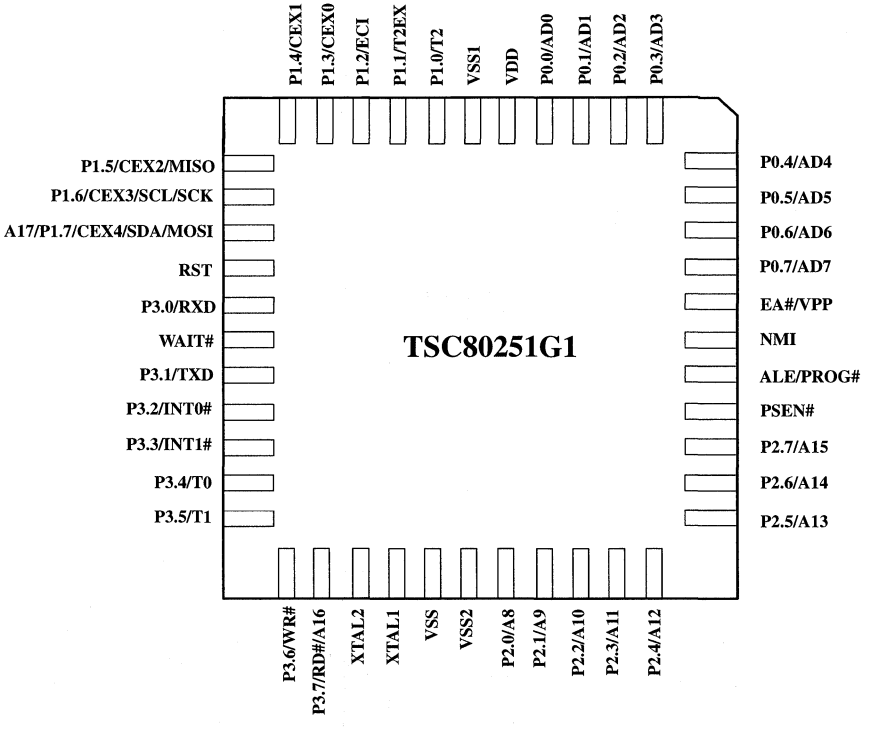


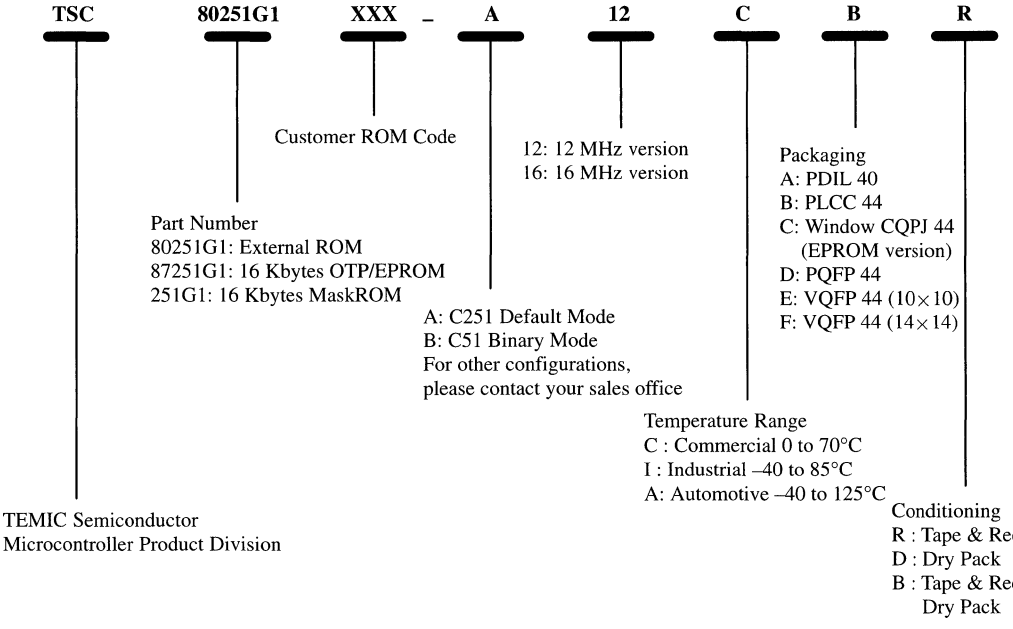
Figure 3. TSC80251G1 Pin Description

Table 1. TSC80251G1 Pin Description

Pin	Type	Description
P0.0:7	I/O	**Port 0** This is an 8–bit open–drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high–impedance inputs. It is also Address/Data lines AD0:7, which are multiplexed lower address lines and data lines for external memory. **External pull–ups are required during program verification.**
P1.0:7	I/O	**Port 1** This is an 8–bit bidirectional I/O port. It receives the low–order address byte during EPROM programming and verification. It serves also the functions of various special features: P1.0 T2 : Timer 2 external clock input/output P1.1 T2EX : Timer 2 external input P1.2 ECI : EWC external clock input P1.3 CEX0 : EWC module 0 Capture input/PWM output P1.4 CEX1 : EWC module 1 Capture input/PWM output P1.5 CEX2 : EWC module 2 Capture input/PWM output MISO : µWire/SPI master input slave output P1.6 CEX3 : EWC module 3 Capture input/PWM output SCL : I2C clock SCK : µWire/SPI serial clock P1.7 A17 : Address line for the 256–Kbyte memory space depending on the byte CONFIG0 CEX4 : EWC module 4 Capture input/PWM output SDA : I2C synchronous serial link data MOSI : µWire/SPI master output slave input Port 1 is also used as a keyboard interface.
P2.0:7	I/O	**Port 2** This is an 8–bit bidirectional I/O port with internal pull-ups. It receives data during EPROM programming and verification. It is also Address lines A8:15, which are upper address lines for external memory.
P3.0:7	I/O	**Port 3** This is an 8–bit bidirectional I/O port with internal pull-ups. It receives the high–order address bits during EPROM programming and verification. It serves also the functions of various special features: P3.0 RXD : Serial Port Receive Data input P3.1 TXD : Serial Port Transmit Data output P3.2 INT0# : External Interrupt 0 P3.3 INT1# : External Interrupt 1 P3.4 T0 : Timer 0 external clock input P3.5 T1 : Timer 1 external clock input P3.6 WR# : Write signal for external access P3.7 A16 : Address line for 128–Kbyte and 256–Kbyte memory space depending on the byte CONFIG0, RD# : Read signal for external access, depending CONFIG0 byte.
ALE/PROG#	I/O	**Address Latch Enable/Program Pulse** It signals the start of an external bus cycle and indicates that valid address information is available on lines A15:8 and AD7:0. An external latch can use ALE to demultiplex the address from address/data bus. It is also used as the Program Pulse input PROG#, during EPROM programming.
PSEN#	O	**Program Store Enable/Read signal output** This output is asserted for a memory address range that depends on bits RD0 and RD1 in CONFIG0 byte.
EA#/VPP	I	**External Access Enable/Programming Supply Voltage** This input directs program memory accesses to on–chip or off–chip code memory. For EA# = 0, all program memory accesses are off-chip. For EA# = 1, an access is on-chip OTPROM/EPROM/ROM if the address is within the range of the on–chip OTPROM/EPROM/ROM; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without ROM on-chip, EA# must be strapped to ground. It receives also the Programming Supply Voltage VPP during EPROM programming operation.
WAIT#	I	Real–time Wait States Input When this pin is active (low level), the memory cycle is stretched until it becomes high.

Pin	Type	Description
NMI	I	Non Maskable Interrupt Holding this pin high for 24 oscillator periods triggers an interrupt.
VDD	PWR	Digital Supply Voltage
VSS	GND	Digital Ground
VSS1	GND	Digital Ground
VSS2	GND	Digital Ground
RST	I	**Reset input to the chip** Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and VDD. Asserting RST when the chip is in Idle mode or Power–Down mode returns the chip to normal operation.
XTAL1	I	**Input to the on–chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing.
XTAL2	O	**Output of the on–chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.

Ordering Information



4

Examples

Part Number	Description
TSC80251G1–A16CBR	ROMless, C251 Default Mode, 16 MHz, PLCC 44, 0 to 70°C, Tape and Reel
TSC80251G1–B16CBR	ROMless, C51 Binary Mode, 16 MHz, PLCC 44, 0 to 70°C, Tape and Reel
TSC87251G1–12CB	OTP, 12 MHz, PLCC 44, 0 to 70°C
TSC87251G1–12CC	EPROM, 12 MHz, CQPJ 44, 0 to 70°C

Development Tools

Part Number	Description
TSC80251G1–SKA	Software Starter Kit Keil
TSC80251G1–SKB	Software Starter Kit Tasking
TSC80251G1–EKA	Evaluation Kit Keil
TSC80251G1–EKB	Evaluation Kit Tasking

Product Marking :

TEMIC
Customer P/N
Temic P/N
Ⓜ© Intel'95
YYWW Lot Number

Section V

Packaging

C51 Microcontroller Family Packaging Selection Guide

Plastic Packages

	PDIL40	PLCC44	PLCC52	PQFP44 13.9 mm foot print	PQFP44 12.3 mm foot print	PQFP64	VQFP44 1.4 mm thickness	TQFP44 1.0 mm thickness
TSC80C31/TSC80C51	•	•		•	•		•	•
TSC80CL31/TSC80CL51	•	•		•	•		•	•
80C31/80C51	•	•		•	•		•	•
80C32/80C52	•	•		•	•		•	•
80C154/83C154	•	•		•	•		•	•
83C154D	•	•		•	•		•	•
TSC8051C1	•	•	•	•				
TSC8051C2*	•	•	•	•				
TSC8051A1*						•		
TSC8051A2*		•		•	•			
TSC8051A11*						•		
TSC8051A30*		•		•	•			

* to be introduced during 1997, check with your TEMIC sales contact for availability

5

Ceramic Packages

	SB40*	CDIL40 (.6)	LCC44*	JLCC44	CQPJ44
TSC80C31/TSC80C51		•	•		•
80C31/80C51		•	•		•
80C32/80C52	•	•	•	•	•
80C154/83C154		•	•		•
83C154D		•	•		•

* only for space grade, drawing not included in this chapter, but available upon request.

Windowed Packages (for EPROM/OTP versions)

Windowed packages	CDIL40**	CQPJ44	CQPJ64**
TSC87C51*	•	•	
87C52*	•	•	
TSC8751C1*	•	•	
TSC8751C2*	•	•	
TSC8751A1*			•
TSC8751A2*		•	
TSC8751A11*			•
TSC8751A30*		•	

* to be introduced during 1997, check with your TEMIC sales contact for availability
** package drawings to be defined

Package Drawings

1. PDIL 40
2. PLCC 44
3. PLCC 52
4. PQFP 44 (13.9 mm Foot Print)
5. PQFP 44 (12.3 mm Foot Print)
6. VQFP 44 (1.4 mm Thickness)
7. TQFP 44 (1.0 mm Thickness)
8. PQFP 64
9. CDIL 40 (.6)
10. LCC44
11. CQPJ 44
12. CQPJ 44 with Window

1. PDIL 40

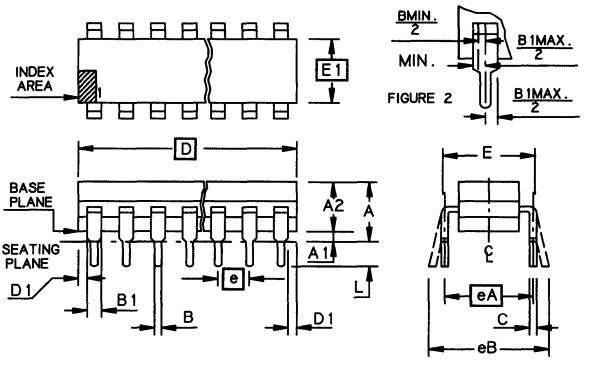


Figure 1. PDIL Package Size

	MM		INCH	
	Min	**Max**	**Min**	**Max**
A	–	5.08	–	.200
A1	0.38	–	.015	–
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	50.29	53.21	1.980	2.095
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
eB	–	17.78	–	.700
L	2.93	3.81	.115	.150
D1	0.13	–	.005	–

5

2. PLCC 44

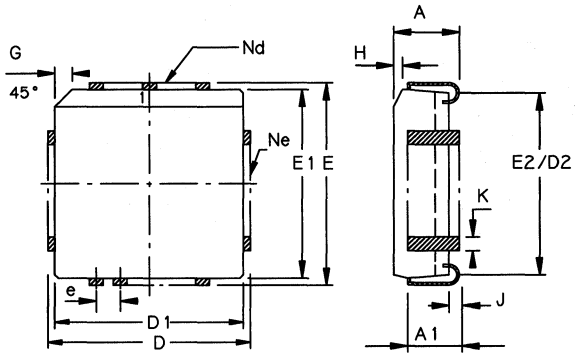


Figure 2. PLCC Package Size

	MM		INCH	
	Min	**Max**	**Min**	**Max**
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	.120
D	17.40	17.65	.685	.695
D1	16.44	16.66	.647	.656
D2	14.99	16.00	.590	.630
E	17.40	17.65	.685	.695
E1	16.44	16.66	.647	.656
E2	14.99	16.00	.590	.630
e	1.27 BSC		.050 BSC	
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	–	.020	–
K	0.33	0.53	.013	.021
Nd	11		11	
Ne	11		11	

3. PLCC 52

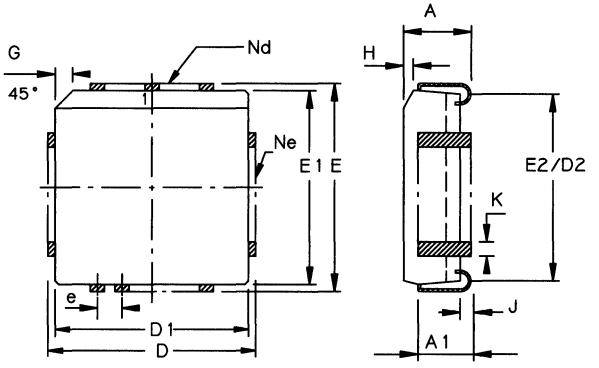


Figure 3. PLCC Package Size

	MM		INCH	
	Min	**Max**	**Min**	**Max**
A	4.20	5.08	.165	.200
A1	2.29	3.30	.090	.130
D	19.94	20.19	.785	.795
D1	19.05	19.25	.750	.758
D2	17.53	18.54	.690	.730
E	19.94	20.19	.785	.795
E1	19.05	19.25	.750	.758
E2	17.53	18.54	.690	.730
e	1.27 BSC		.050 BSC	
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	–	.020	–
K	0.33	0.53	.013	.021
Nd	13		13	
Ne	13		13	

4. PQFP 44 (F1 Code)

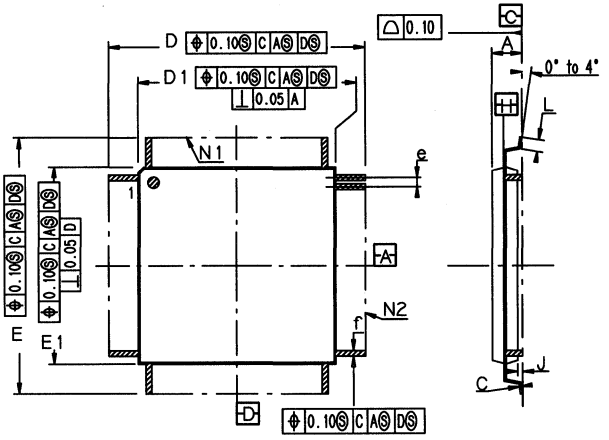


Figure 4. PQFP Package Size

	MM		INCH	
	Min	Max	Min	Max
A	2.00	2.40	.079	.094
C	0.10	0.20	.004	.008
D	13.65	14.15	.537	.557
D1	9.90	10.10	.390	.398
E	13.65	14.15	.537	.557
E1	9.90	10.10	.390	.398
e	0.80 B.S.C.		.0315 B.S.C.	
f	0.20	0.40	.008	.016
J	0.00	0.30	.000	.012
L	0.65	0.95	.025	.037
N1	11		11	
N2	11		11	

5. PQFP 44 (F2 Code)

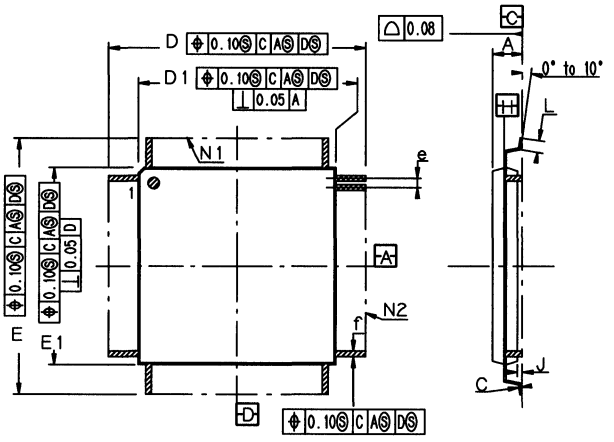


Figure 5. PQFP Package Size

	MM		INCH	
	Min	Max	Min	Max
A	1.90	2.40	.075	.095
C	0.10	0.20	.004	.008
D	12.10	12.50	.476	.492
D1	9.90	10.10	.390	.398
E	12.10	12.50	.476	.492
E1	9.90	10.10	.390	.398
e	0.80 B.S.C.		.0315 B.S.C.	
f	0.25	0.45	.010	.018
J	0.00	0.20	.000	.008
L	0.35	0.65	.014	.026
N1	11		11	
N2	11		11	

5

6. VQFP 44

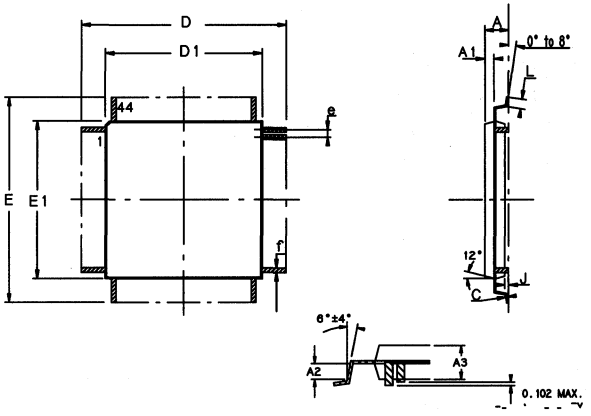


Figure 6. VQFP Package Size

	MM		INCH	
	Min	Max	Min	Max
A	–	1.60	–	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025REF	
A3	1.35	1.45	.053	.057
D	11.90	12.10	.468	.476
D1	9.90	10.10	.390	.398
E	11.90	12.10	.468	.476
E1	9.90	10.10	.390	.398
J	0.05	–	.002	6
L	0.45	0.75	.018	.030
e	0.80 BSC		.0315 BSC	
f	0.35 BSC		.014 BSC	

7. TQFP 44

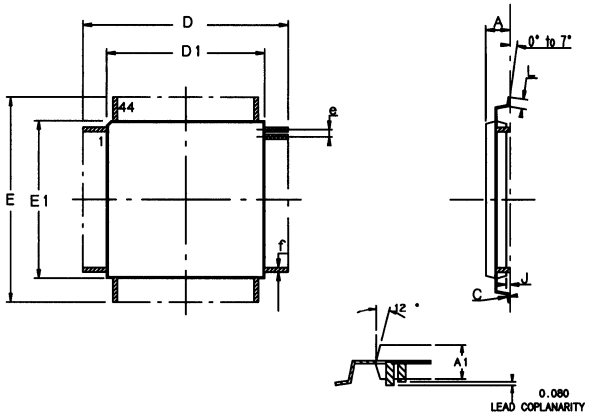


Figure 7. TQFP Package Size

	MM		INCH	
	Min	Max	Min	Max
A	–	1.20	–	.047
A1	0.95	1.05	.037	.041
C	0.09	0.20	.004	.008
D	12.00 BSC		.472 BSC	
D1	10.00 BSC		.394 BSC	
E	12.00 BSC		.472 BSC	
E1	10.00 BSC		.394 BSC	
J	0.05	0.15	.002	.006
L	0.45	0.75	.018	.030
e	0.80 BSC		.0315 BSC	
f	0.30	0.45	.012	.018

5

8. PQFP 64

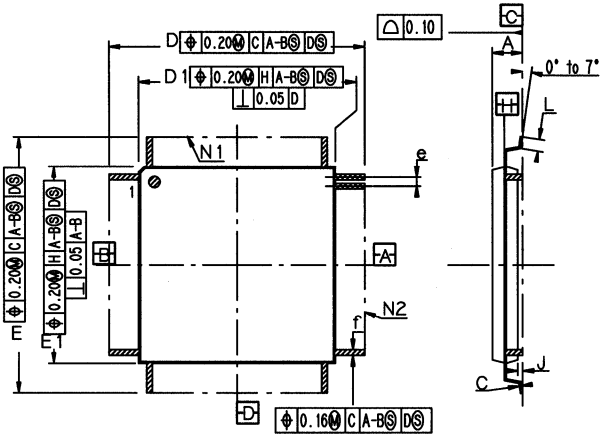


Figure 8. PQFP Package Size

	MM		INCH	
	Min	**Max**	**Min**	**Max**
A	2.65	3.00	.104	.118
C	0.13	0.23	.005	.009
D	16.95	17.45	.667	.687
D1	13.95	14.05	.549	.553
E	16.95	17.45	.667	.687
E1	13.95	14.05	.549	.553
e	0.80 BSC		.0315 BSC	
f	0.30	0.45	.012	.018
J	0.10	0.25	.004	.010
L	0.65	0.95	.026	.037
N1	16		16	
N2	16		16	

9. CDIL 40 (.6)

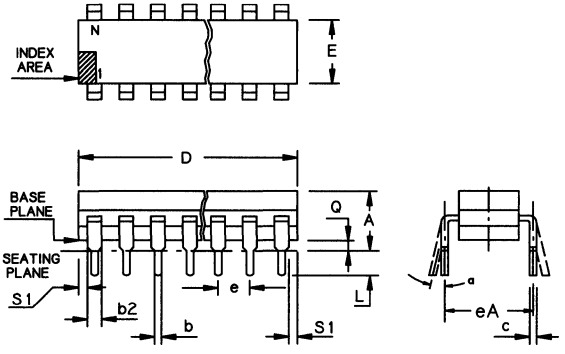


Figure 9. CDIL Package Size

	MM		INCH	
	Min	**Max**	**Min**	**Max**
A	–	5.71	–	.200
b	0.36	0.58	.014	–
b2	1.14	1.65	.045	.195
c	0.20	0.38	.008	.022
D	–	53.47	–	.070
E	13.06	15.37	.514	.015
eA	15.24 BSC		.600 BSC	
e	2.54 BSC		.100 BSC	
L	3.18	5.08	.125	.200
Q	0.38	1.40	.015	.055
S1	0.13	–	.005	–
a	0° – 15°		0° – 15°	
N	40			

5

10. LCC 44

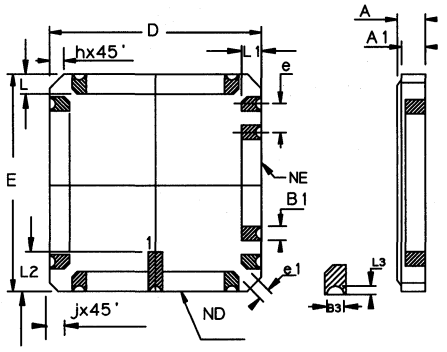


Figure 10. LCC Package Size

	MM		INCH	
	Min	**Max**	**Min**	**Max**
A	1.75	3.05	.069	.180
A1	1.37	2.23	.054	.120
B1	0.56	0.71	.022	.028
B3	0.15	0.56	.006	.022
D/E	16.25	16.82	.640	.662
e	1.27 BSC		.050 BSC	
e1	0.38	–	.015	–
h	1.02 REF		.040 REF	
j	0.51 REF		.020 REF	
L/L1	1.14	1.40	.045	.055
L2	1.90	2.41	.075	.095
L3	0.08	0.38	.003	.015
Nd	11		11	
Ne	11		11	

11. CQPJ 44

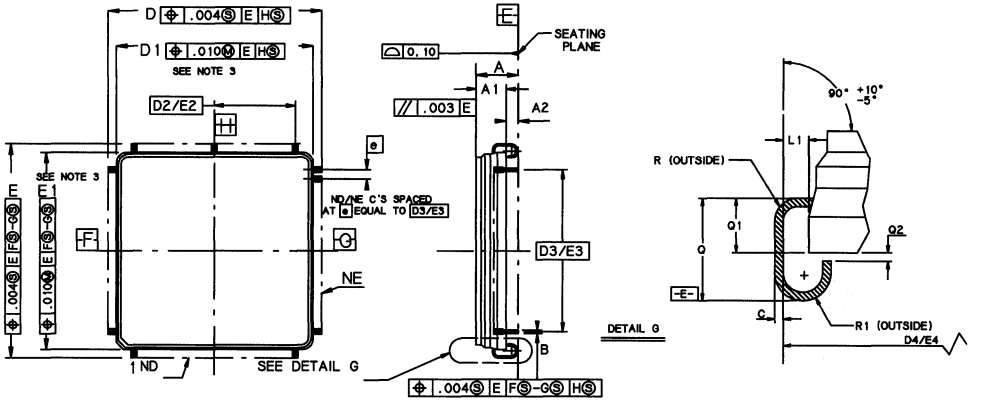


Figure 11. PDIL Package Size

	MM		INCH	
	Min	Max	Min	Max
A	2.16	4.83	.085	.190
A1	1.91	3.81	.075	.150
A2	0.76	1.27	.030	.050
B	0.46	0.56	.018	.022
C	0.14	0.28	.0054	.011
D/E	17.40	17.65	.685	.695
D1/E1	16.31	16.71	.642	.658
D2/E2	6.35 BSC		.250 BSC	
D3/E3	12.70 BSC		.500 BSC	
D4/E4	16.84	17.30	.663	.681
e	1.27 BSC		.050 BSC	
L1	0.25	–	.010	–
Q	2.41	2.92	.095	.115
Q1	1.52	1.78	.060	.070
Q2	0.08	–	.003	–
R	0.38	–	.015	–
R1	0.76	1.02	.030	.040
ND/NE	11		11	

12. CQPJ 44 with Window

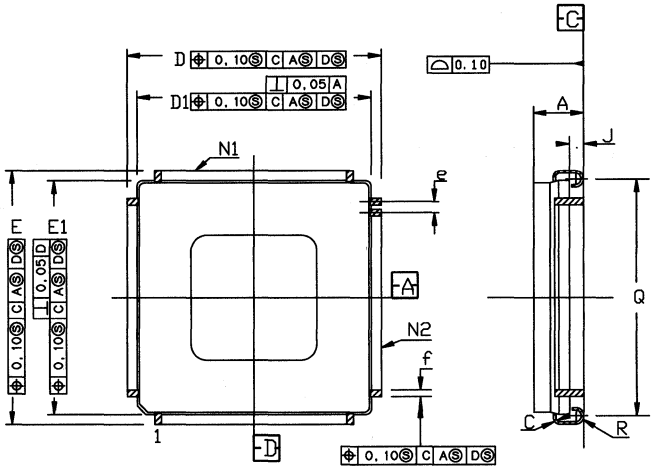


Figure 12. CQPJ Package Size

	MM		INCH	
	Min	Max	Min	Max
A	–	4.90	–	.193
C	0.15	0.25	.006	.010
D – E	17.40	17.55	.685	.691
D1 – E1	16.36	16.66	.644	.656
e	1.27 TYP		.050 TYP	
f	0.43	0.53	.017	.021
J	0.86	1.12	.034	.044
Q	15.49	16.00	.610	.630
R	0.86 TYP		.034 TYP	
N1	11		11	
N2	11		11	

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