The Business System 300 Architecture

Hardware Concepts Session
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ABSTRACT

The use of specialized LSI circuitry has made possible a high performance, compact, cost effective multiuser system for business applications. The features of the Business System 300 architecture, their functions, and their benefits to the user will be covered.

The Business System 300 unit combines a processsor, up to 512K bytes of memory, disk controller, printer interface, video display terminal, and optional communications interfaces into a single integral unit. This unit provides more processing power, requires less electrical power, fits in a smaller space, can be easily placed in any office environment, uses Winchester based mass storage devices, and is a more reliable system than previous systems of the same functionality. The ability to create the Business System 300 Series, a multiuser desktop computer with integral video display, was made possible by specialized LSI technology. The majority of this paper will be devoted to discussing this LSI technology with short discussions of Winchester technology, communications interfaces, and software.

LSI CHIPS

The functions implemented using specialized LSI technology include the microprocessor (TMS 99000), memory chips (TMS 4164), communications register unit chip (CRU), memory mapping chip (MAP), error correction and control chip (CCC), and mass storage interface chip (MSIC). Each of these LSI chips will be discussed in detail and are shown in Figure 1 of the System 300 processor board.

The processor of the Business System 300 is based on memory-to-memory architecture in which all general purpose registers reside in memory. A high speed bidirectional 16-bit data bus transfers data between the CPU (central processing unit), memory, and other devices such as disk files. The System 300 processor is built around the Texas Instruments TMS 99000 microprocessor.

The TMS 99000 microprocessor retains the memory-to-memory architecture introduced in 1975 with the 990/10 minicomputer and TMS 9900 microprocessor. This architecture was a deviation from conventional architecture. Processors originally had but a single accumulator to handle the logic and arithmetic functions. As time passed and implementation costs fell, processors were designed with multiple accumulators to simplify coding. Finally, with the advances of Medium Scale Integration (MSI) and Large Scale Integration (LSI), machines could be cost effectively designed with general purpose registers. These machines could do the logical and arithmetic operations as had the previous accumulator implementations, and in addition, could be used for operand address generation and index addressing.

Since the function of registers and memory were basically the same, and because the speed of memory devices was rapidly approaching that of on board registers, the designers of the TMS 9900 microprocessor and TI 990 computer family chose to take a different approach to their new design. They implemented a memory oriented architecture instead of a register oriented architecture. This implementation was made by creating a pseudo "register file" in main memory, pointed to by a single hardware register in the processor. The primary benefit of this approach was to drasticaly reduce the work required to perform a context switch. This meant that only three registers (Work Space Pointer, Status, and Program Counter) in the 990/9900 processor had to be saved and loaded to give the user a clean set of 16 registers. With the register architecture, each of the 16 registers would have had to have been saved and loaded separately. Thus the memory architecture provides a significant time savings during context switching, which is extremely important for interrupt processing and subroutine calls.

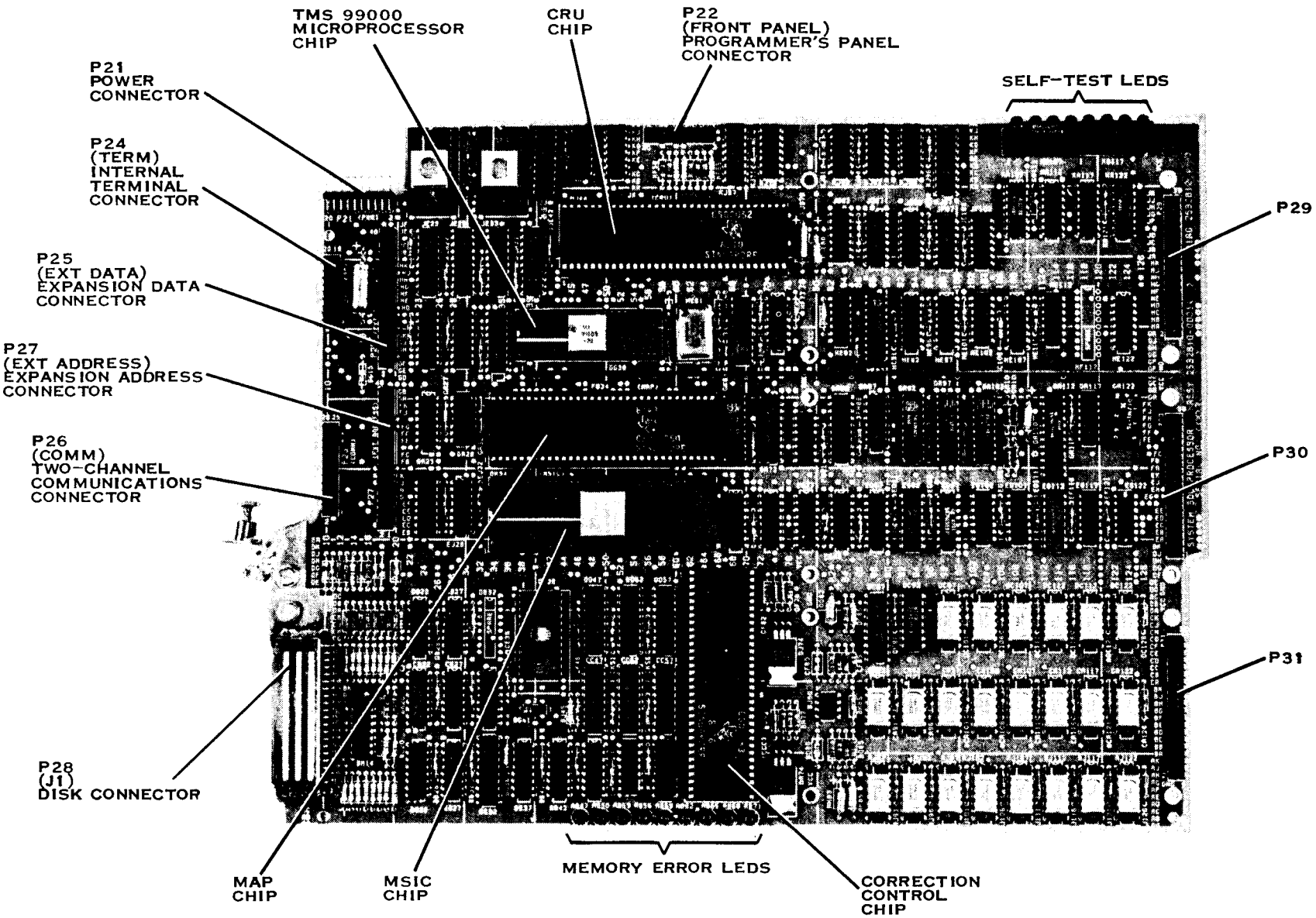

FIGURE 1 - SYSTEM 300 PROCESSOR

Faster execution of a function is also an advantage of the 990/9900. Though individual instructions may be slower because of the memory architecture, fewer instructions are usually needed than with a register oriented architecture, and therefore function execution time is faster. For instance, with the 990/9900 to move a word in memory only requires the execution of the MOVE instruction. With the register architecture, the word would have to LOADed into a register, and then SAVEed into the new memory location. This also provides a machine much easier to program, giving a 3:1 typical instruction reduction.

As just discussed, the TMS 99000 memory-to-memory architecture provides for reduction in overhead in transferring data, reduction in the number of bytes of memory required for an operation, a reduction in the number of instructions required for a function with the final result being that execution time for a program is greatly reduced. These advantages of memory-to-memory archectiture translate into more efficient programs for the user.

The third-generation TMS 99000 microprocessor is software compatible with the second generation TMS 9900 microprocessor. Since the memory for the System 300 is all on the processor board, the System 300 does not require the use of the TILINE bus to access memory or the disk and therefore is not slowed down by the TILINE.

The 64 K dynamic random access memory (DRAM) chips used in the System 300 memory are the highest capacity chips commerically avaialable in the market today. Not only do these memory chips provide four times the amount of memory in the same space as the 16 K DRAM chips but also require less power and are more reliable. The cost of one 64 K DRAM is less than the cost of four 16 K DRAMs. Another benefit of the System 300 is the ability to easily increase the memory size from 128K bytes to 512 K bytes in 128 K byte increments allowing the user to purchase the amount of memory needed for his application. Unlike many systems on the market that do not have easily expandable memory.

The Communications Register Unit (CRU) chip decodes CRU addresses from the microprocessor to generate enable signals and strobes that perform specific control and I/O functions on a bit oriented basis. The CRU chip replaces 61 chips that were required to implement this function on the 990/10 board. The Correction Control Chip (CCC) provides circuitry that corrects single-bit data errors from the memory arrays and can detect double-bit data errors. By using a custom LSI chip for this function the chip count was reduced from 50 to 1. The MAP chip converts the 15 bit logical address into a 20 bit memory mapped physical address on each memory cycle. The custom MAP chip reduced the chip count from 56 to 1.

The System 300 processor mass storage controller is a memory mapped interface designed to enable DX10 software to communicate with PBUS compatible mass storage subsystems such as WD500s and WD800s. The function of the controller is to pass commands from the processor to the formatter, to handle direct memory accesses necessary for memory storage and to perform self test. The S300 controller consists of an interface to the processor, a PBUS interface and the mass storage interface chip (MSIC). The MSIC is a memory mapped I/O device that uses control words written by the processor to direct data to and from the mass storage device. The functions of the MSIC include direct memory accesses to and from System 300 memory, PBUS parity generation and checking, command decode, and self test. The MSIC and its 19 support chips replace 108 devices that are used by similar controllers. The System 300 controller contains two Peripheral Control Spaces. Each of these spaces can control up to four devices. The System 300 can control up to four disk and up to four tapes or up to eight disks if no tape devices are used.

Extensive use of programmable array logic (PALs) in the System 300 provides for the implementation of such functions as the memory controller, row decode logic, write inhibit controller, CRU, memory address decode, and bus status code decode. This allowed for up to 10:1 reduction in the number of devices required for these functions since one PAL replaces the need for ROM chip(s) and a register.

The number of devices and the number of connections have been greatly reduced in the System 300 unit due to LSI chips which were incorporated as shown in Table 1. The four custom LSI chips and their supports chips have decreased the chip count for the CRU, CCC, MAP and disk controller functions from 275 to 23 and the pin count from 4560 to 988.

TABLE 1 CHIP TECHNOLOGY

	CHIP COUNT	PIN COUNT
CRU CHIP	FROM 61 TO 1	FROM 854 TO 64
CCC CHIP	FROM 50 TO 1	FROM 828 TO 64
MAP CHIP	FROM 56 TO 1	FROM 934 TO 64
MSIC CHIP AND SUPPORT CHIPS	FROM 108 TO 20	FROM 1944 TO 396

P-BUS

The PBUS interface is an 8 bit data bus with seven control lines. Data is transferred on a byte by byte basis with the most significant byte of each word transferred first. The PBUS operates via differentially driven cable which are RS422 compatible. Factors affecting the transfer rate are system clock speed, relative system usage, size of the data blocks being transferred, and speed of the formatter. The System 300 controller can operate at burst rates of approximately 700 K bytes/second under optimum conditions.

SELF-TEST ON THE PROCESSOR

Extensive self-test firmware on the System 300 processor provides internal loopback and diagnostic capability for a number of functions. These tests are provided for the MAP chip, the CCC chip, interrupts, integral terminal, two-channel communications board, MSIC chip, and mass storage bus interface. Eight Light Emitting Diodes (LED's) which are visible through the top of the System 300 unit provide visual indication of the self-test results. At initial power-up, one green LED is unlit and seven red LEDs are lit. As the various self-tests are passed the red LEDs are turned off and on and upon completion of the system load the green LED is lit. Any group of red LEDs left on indicates an error has been detected. The lighted red LEDs indicate an error code that tells what failed during self-test.

VIDEO DISPLAY UNIT

The video display unit of the System 300 is microprocessor controlled. It features a full 128 ASCII character set with lower descenders, 24 lines of 80 characters per line, normal and high inensity, user adjustable intensity, non-destructive block cursor, self-test on power-up, and optional line graphics. Optional tilt base and anti glare screens are available for operator comfort. The detachable keyboard features 94 stepped keys with typamatic capability, a 14 key numeric pad, 12 positioning and editing keys, and eight operator programmable function keys. An integral RS-232-C port provides for a printer to be attached to the System 300.

COMMUNICATIONS

Having covered the System 300 processor and terminal capabilities it is now time to look at communications with devices outside the unit. Two communications boards are available for the Business System 300. One provides two ports and the other provides four ports. The two channel communications board provides one asynchronous port and one programmable asynchronous or synchronous port for additional terminals. The synchronous port can have a local asynchronous terminal attached or an interface to an external modem either synchronous or asynchronous. The synchronous port can also be used with either 3780/2780 or

3270 communications software packages under DX10. The asynchronous port interfaces to a local asynchronous terminal. A four channel communications interface provides four asynchronous ports and can interface four local asynchronous terminals. These communications interfaces are independent of each other. A System 300 can have either communications interface or both interfaces or none.

Another benefit is the simplicity of adding Business System terminals. The four channel interface provides four asynchronous ports for the addition of four terminals. A two channel communications interface which can also be added provides an asynchronous port for a Business System terminal and a programmable asynchronous or synchronous port for either an additional terminal or a communications line.

WINCHESTERS

The mass storage devices for the Business System 300 are based on Winchester technology using either 5 1/4" or 8" drives. Mass storage capacity for the System 300 ranges from a 5 MB unit using a 5 1/4" Winchester drive to 172 MB using four 8" Winchester drives. Winchester drives have lowered the cost per byte of storage significantly.

Reliability of Winchester based disk units is greater than other technologies because Winchester technology seals the hard disk, actuator, and read/write heads in an enclosure. Since a Winchester drive operates in a totally sealed environment, surface and head contamination has been eliminated and therefore a major cause of disk failure has been eliminated. Misalignment problems have also been eliminated because the media is not removable. In systems with removable media, the media can be damaged when removing or installing the disk pack. The removable media surface can also be scratched or damaged while being stored. Data stored on Winchester based systems are not subject to these types of damage. Winchesters also eliminate interchangeability problems experienced with all removable media disk drives.

A major problem with small disk drives that use flexible disks is the constant shift of the disk surface with changes in temperature and humidity. Most flexible media use Mylar as the base substrate that deforms with temperature, humidity, and stress relaxation effects. The changes can be enough to cause a data track to be missed when it's read after the disk media shift. The shifting problem of flexible disk media has been eliminated in Winchester technology based disk subsystem.

The flying height of the heads for a 5 1/4-inch Winchester is 19 microinches which allows for higher densities of data and higher rotational speed (3600 rpm). The majority of flexible disk drives have heads that are in contact with the disk media. The rotational speed of flexible disk drives is lower (360 rpm) because of the head contact with the flexible media.

Data integrity is the most important characteristic of a mass storage device. TI small Winchester units use an error correction code (ECC). During write and format operations, the data stream is passed through the error logic to generate an ECC check. The ECC check is appended to either the end of the block of data or the ID field. When the data is read from the disk, the data is again passed through the ECC logic and the value from the ECC logic is compared to the ECC check read from the disk. If the two checks do not match then the data is re-read from the disk. The number of re-reads on this type of disk is usually around three. If there are two re-reads with the same check but not in agreement with the ECC read from the disk, then a microprocessor on the formatter/data separator board will determine if the error is correctable. For example, the ECC polynomial that is used in the TI WD500 disk subsystem can correct single burst errors of less than 8 bits. Single burst errors of 8 to 32 bits and double burst errors of less than two bits (which are less than 32 bits apart) can be detected but can not be corrected.

The soft read error rates for flexible disk drives are around one error in 10^8 reads and soft read error rates for Winchester drives around one error in 10^{10} reads. The lower soft read error rates combined with error detection and

correction algorithms available on 5 1/4-inch Winchesters can greatly increase data integrity for small systems.

The 8" Winchester drives can provide formatted storage up to 43 MB which equals the storage capacity of disk units much larger. Many large disk units require special power and cooling that 8" Winchester units do not. Therefore System 300 units with 8" Winchester drives can be placed in office environments without special power or cooling.

The 5 1/4-inch Winchester disk uses the rotary-band swing arm design because of its small size. This allows the design of a 5 1/4-inch Winchester disk drive that can fit in the small physical space. Data separator and formatter functions that are implemented to interface the drive to a computer can easily be placed in drive box. Therefore, the 5 1/4-inch Winchester based mass storage subsystems to be used with mini and microcomputers are the same size, or smaller, than many current 8-inch flexible disk drive subsystems.

The higher recording density has helped bring the cost and size of Winchester drives down. The smaller disk size of the Winchester based mass storage subsystems makes them transportable and ideal candidates for depot maintenance repair. Depot repair offers the user a lower maintenance rate for his system and therefore lowers his overall multiple year operating cost.

The lower maintenance costs for Winchester disks over removable disks has lowered the five year cost of ownership significantly. Another advantgae of Winchester based masss storage systems is that the units are much quieter and will not disturb people in an office. Large removable disk units because of the greater cooling and the requirement to move air over the disk surface are very noisy.

SYSTEM CONSIDERATIONS

Business System 300 units can be placed in an ordinary office environment. The System 300 components (system unit, mass storage units, printers, add-on terminals, etc.) use grounded three wire 115 volt power which is available in most offices. Thus eliminating the need for 240 volt power required by many other computer systems for disk units. Since power consumption has been greatly reduced from units with the same functionality, the need for special air conditioning has been eliminated because the amount of heat generated is relatively small. The expense of needing a special computer room has been eliminated because of the reduction is size of the System 300, the reduction in heat generated by the Business System 300 components and the quieter disk provided by Winchester technology.

The functionality of the System 300 processor and four channel communications board took up to nine chassis slots in a TI 990/10 system (2 slots for /10, 3 slots for 512 KB memory, 1/2 slot for printer, 3 slots for 5 CRTs, and 1 slot for the Disk conrtoller). The power required for this functionality has been reduced from 1707 watts (Model 4 with DS10 and 810 printer) to 510 watts (System 351 with 810 printer).

SOFTWARE COMPATIBILITY

No discussion of system architecture would be complete without some mention of software. The operating system for the Business System 300 Series is DX10 release 3.5.1. DX10 is a highly rated field proven operating system that is compatible with all 990 systems and the new Business System 600 and 800 series. Languages provided under DX10 for the System 300 include COBOL, Basic, Pascal, and Fortran 78. Applications written in COBOL, Basic, Pascal or Fortran 78 for use on TI 990 systems using DX10 can be easily moved to the System 300 without source modification. Allowing users to preserve their application software investment made over the years.

CONCLUSION

The high degree of Large Scale Integration used in the Business System 300 provides for a compact, high performance, easy to expand, and cost effective desk top computer system. The mass storage devices are all based on Winchester technology providing more reliable and lower cost mass storage. In addition, user application software investment made on TI 990 computers has been preserved giving current users an easy upgrade path.

About the Author

Ivan Erickson is a product manager for Business System computers with the Data Systems Group of Texas Instruments in Austin, Texas. He holds a Bachelor of Science degree in electrical engineering from the University of Maine (1970) and a Masters of Business Administration from Penn State University (1975). Also, he has done post graduate work in financial management at the University of Texas. He is a member of the Institute of Electrical and Electronic Engineers (IEEE), Tau Beta Phi, and Eta Kappa Nu. He has authored and coauthored with John Purvis a number of papers covering computer systems, data communications, and computer cost analysis. These have been presented at TI-MIX symposiums, ISA conferences, and the 1980 MIMI conference in Mexico City. Several papers have appeared in the proceedings of ISA, ISMM, and in other publications including **InTech** and **Business Computer Systems.**

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