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UNIMUX

COMMUNICATION LINE ADAPTOR

REFERENCE MANUAL
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UNICOMP, INC.
18219 Parthenia Street
Northridge, California 91324
(213) 886-7722

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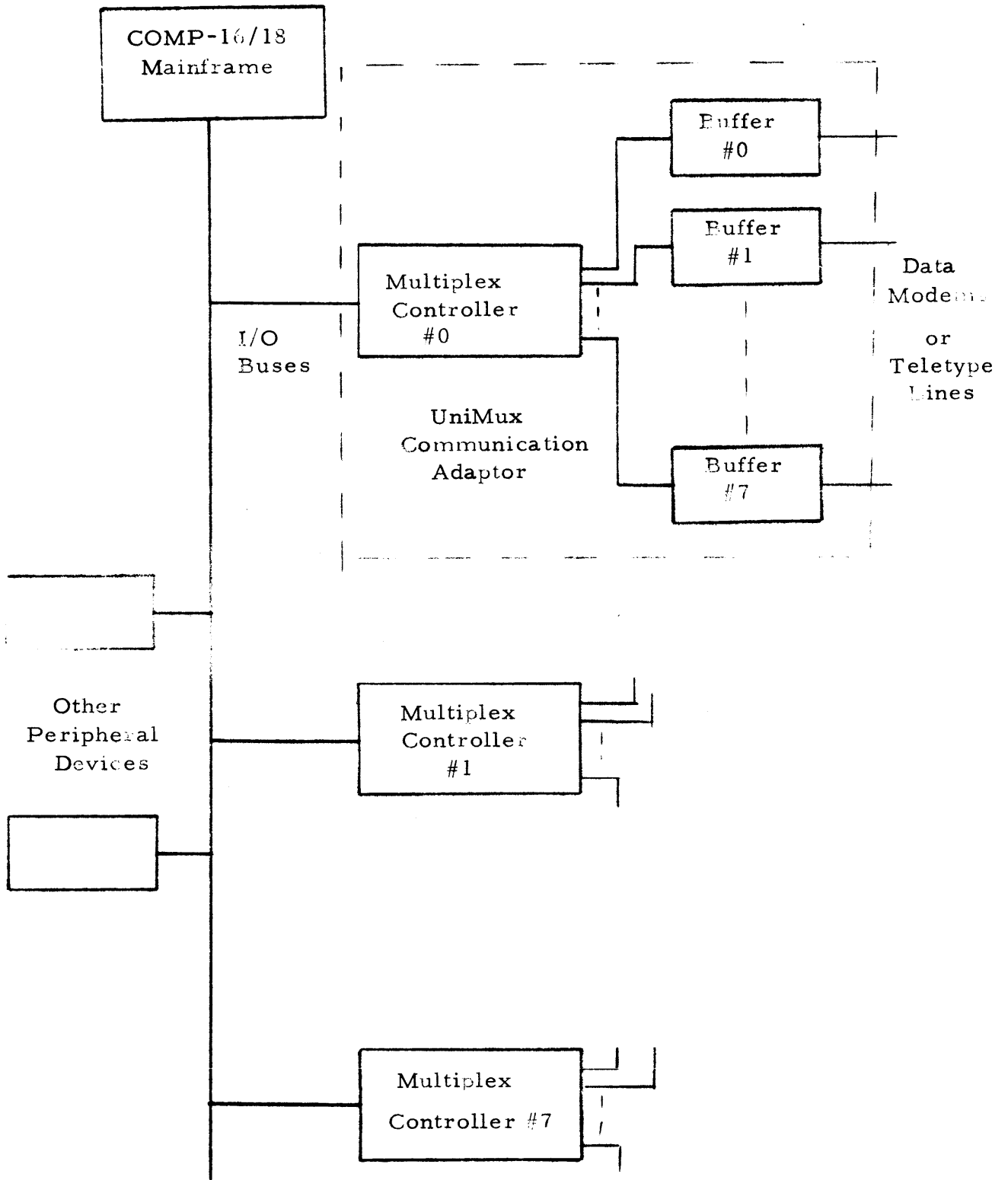
The UNIMUX COMMUNICATION LINE ADAPTOR is an optional accessory to the UniComp COMP-16 and COMP-18 computers. This adaptor allows the COMP-16/18 to communicate with remote devices over either telephone or teletype lines. These remote devices may be remote data terminals, other computers, or computer peripherals.

Telephone line communication is performed over data modems which connect to the UniMux Adaptor by means of the RS-232C interface in a synchronous mode. Any modem employing this interface can be used, such as the IBM Model 4872, the Lenkurt Model 26C, the Milgo Model 4400, the Rixon Models FM18, PM24, SEB1T48, 48C, or 96, or the Bell System Data Phones. Teletype Communication is performed directly over a two-wire teletype line.

As shown in Figure 1, three devices constitute the UniMux Adaptor option for the COMP-16/18. They are:

- 1) The Data Modem Buffer, Model 16-412 or 18-412.
- 2) The Teletype Line Buffer, Model 411.
- 3) The UniMux Multiplex Controller, Model 410.

The two types of buffers perform the direct communication between the adaptor and the Modem or Teletype Line, respectively. Their purpose is to provide a temporary store of up to 18 bits of the data being transmitted, and either supply a bit at a time, or accept a bit at a time as transmission proceeds.



Block Diagram
 COMP-16/18 with UniMux Communication Line Adaptor

The Multiplex Controller acts as the device which controls the transfer of data between the individual buffers and the COMP-16/18 memory. Up to eight Buffers may be utilized with each Multiplex Controller, and up to eight Controllers may be used with one COMP-16/18.

The following three sections describe the three elements of the UniMux Adaptor in detail.

DATA MODEM BUFFER

The Data Modem Buffer provides an interface to any data modem which utilizes the EIA RS-232C interface specification. Each Buffer can operate in either a Transmit or Receive mode (half duplex). However, two buffers may be combined to operate in full duplex.

In the Transmit Mode, as controlled by COMP-16/18 command, the Data Modem Buffer accepts up to an 18 bit word (16 bits for COMP-16) from a specifically designed section of the COMP-16/18 memory via the Multiplex Controller. It then transmits these bits to the modem at a rate controlled by the transmit clock supplied by the modem. When all bits have been transmitted, a signal is supplied to the Multiplex Controller, which then secures another word from memory for continuing the transmission. Transmission ceases when the Multiplex Controller determines from data stored in memory that all data designated for that buffer has been transmitted.

The Buffer can transmit fewer than 16 or 18 bits of each word under program control. The computer supplies a numeric value to each buffer specifying the number of bits to be transmitted from each 16 or 18 bit word.

The receive mode commences whenever the modem supplies a Received Signal Present (Signal CF of Table 1) to the Buffer. If the Buffer has been previously placed in an "Input Mode" by the computer program, the input data are accepted as received. If the Input Mode has not been called, an interrupt is supplied to the computer so that the computer can call for an Input Mode or not as the case may require. If no Input Mode is called, the input data is ignored.

In the receive mode, the Buffer accepts data bits from the modem, storing them in a 16 or 18 bit register as received. When the proper number of bits has been received (as determined by program output), a signal is supplied to the Multiplex Controller which then stores the word in a block of memory comprising any number of words specifically designated to go with the specific buffer. When the designated block of memory has been filled, the computer is notified through an interrupt, and either a new block of memory is designated by program, or no further information is accepted. Data receipt usually ceases when the modem supplies a signal indicating that the transmission being received by the modem is no longer present. In such an instance, the computer is also supplied an interrupt signal.

Table 1 is a list of signals passing between each Data Modem Buffer and a Data Modem. These signals correspond directly to the RS-232C interface and use a ± 4 volt signal from Buffer to Modem. An ON signal is +4 volts, and OFF signal is -4 volts. Signals received by the Buffer from the Modem may vary between ± 3 volts to ± 25 volts.

Data Modem Buffers may be operated in pairs to allow full duplex operation over one modem. One buffer is operated as a receive buffer, and one as a transmit buffer. In such a case, certain signals to or from the modem go to the transmit buffer, others to the receive buffers, and some signals go

Circuit	Description	Gnd	Data		Control		Timing		Connection for Full Duplex Buffer	
			From Modem	To Modem	From Modem	To Modem	From Modem	To Modem	XMT Buffer	Recv. Buffer
AA	Protective Ground	X							X	X
AB	Signal Ground	X							X	X
BA	Transmitted Data			X					X	
BB	Received Data		X							X
CA	Request to Send					X			X	
CB	Clear to Send				X				X	
CC	Data Set Ready				X				X	X
CD	Data Terminal Ready					X			X	X
CE	Ring Indicator				X					X
CF	Received Signal Present				X					X
CG	Signal Quality Detector				X					X
CH	Not Used									
CI	Not Used									
DA	Not Used									
DB	Transmitter Timing Clock						X		X	
DD	Receiver Timing Clock						X			X

Table 1
Data Modem/Buffer Interface Signals
per RS-232C

to both, as indicated in Table I.

TELETYPE LINE BUFFER

The Teletype Line Buffer works in a similar manner to the Data Modem Buffer, the primary differences being:

- 1) It interfaces a teletype line directly (no modem required).
- 2) It receives or transmits data in 8 bit characters.
- 3) The end of an input message is determined by the receipt of a pre-designated 8 bit character detected by the buffer.
- 4) Transmission and Receipt of data are both performed over a single pair of wires in a half-duplex mode.

The transmit mode is originated under computer command control, as with the Modem Buffer. A 16 or 18 bit word is secured from memory by the Multiplex Controller, and supplied to the Buffer. The Buffer then transmits the 16 or 18 bits as two characters, comprising 8 information bits, plus 3 control bits. The 3 control bits are a start bit of zero (or space), and two stop bits of one (or mark). The transmission rate of these bits is 110 baud, giving a character rate of 10 per second.

After the two 8-bit characters have been transmitted, a signal is supplied by the Buffer to the Multiplex Controller, which accesses the memory to obtain another 16 or 18 bit word. When all data in memory designated for the particular buffer have been transmitted, the transmission ceases, and an interrupt signal is supplied to the computer.

Data Receipt commences whenever a data signal occurs on the communication lines, but only if the buffer has previously been set up in the Input

Mode. If the Input Mode has not been called, an interrupt is sent to the computer, so that an Input Mode may be set up or not, as required.

Each Teletype Line Buffer may be supplied an arbitrary 8-bit character under program control which is designated the "End of Message" character. When that character is received, the buffer supplies an "End of Message" signal to the Multiplex Controller, which in turn supplies an interrupt signal to the computer.

A group of status signals supplied by each Teletype Line Buffer may be interrogated under computer command. These status signals include:

- 1) Input Mode ON
- 2) Output Mode ON
- 3) Character Being Received
- 4) Character Being Transmitted
- 5) Input attempted during output

Because transmission and receiving is performed over the same pair of wires, it is possible for both to be attempted at the same time. If this happens, the information will be garbled, but status signal number 5 above will go on and an interrupt will be supplied by the Multiplex Controller.

UNIMUX MULTIPLEX CONTROLLER

The Multiplex Controller performs the task of providing communication between each Buffer and the COMP-16/18 memory. It can perform this communication for up to eight such Buffers, including eight Modem Buffers, eight Teletype Line Buffers, or four of each. It is used in a time-shared mode for this communication.

There are six specific tasks which the Multiplex Controller performs in carrying out its duties:

- 1) It obtains from a memory location specifically designated for each buffer, the address of the location in memory into which a word is to be stored as received by a Buffer, or from which a word is to be obtained for transmission by the Buffer.
- 2) It increments the above address as each word is received or transmitted.
- 3) It obtains the ending address of the block of memory assigned to a Buffer for transmission or receiving operations, and compares this address with the present address of each word defined in 1) above as it is incremented as described in 2) above.
- 4) It either stores the word obtained from the buffer, or obtains a word for transmission from the location determined in 1) above.
- 5) It provides interrupts to the computer upon occurrence of any one of the following conditions:
 - a) When the incremented address of the words being transferred becomes equal to the ending address defined in 3) above.
 - b) When an input signal is received by any Buffer without that Buffer being put in an Input Mode.

- c) When a Modem indicates a loss of received signal, indicating an end of transmission.
 - d) When a Teletype Line Buffer receives an end of message character.
- 6) It supplies status bits to the computer upon program interrogation.

The Multiplex Controller performs its operations by continuously scanning the status of the various Buffers to determine which buffer needs servicing, i. e. data transfer to or from memory, or creation of an interrupt.

If a Buffer is found which needs data transfer to or from memory, the Controller uses the Direct Memory Access (DMA) feature of the COMP-16/18 to obtain an address (called the word address) from memory designating a location to or from which a word is to be transferred. The address is obtained from a specific location designated to go with the particular buffer as follows:

Buffer #0	7500
#1	7501
#2	7502
.	.
.	.
#7	7507

Thus, for Buffer #1, the word address is obtained from location 7501. The Multiplex Controller then increments the word address and stores it back in the same word from which it came.

The Controller then obtains a second address (called the final address) from another location designated for each buffer as follows:

Buffer #0	7600
Buffer #1	7601
Buffer #2	7602
.	.
.	.
Buffer #7	7607

The final address designates the last word of the block of memory from which or to which data are to be transferred between the memory and the buffer. A comparison is made between this address and the word address obtained previously to determine if the operation should be terminated. If it should be terminated, the buffer is put in a non-operation mode, and an interrupt is supplied to the computer. If the operation should continue, the controller will use the word address to access the memory for storing or obtaining a data word received or to be transmitted by the particular buffer involved.

(Up to 8 Multiplex Controllers and associated buffers may be used with one COMP-16/18, giving a total possible of 64 buffers. Words 7510 to 7577 and 7610 to 7677 are used for word addresses and final addresses for these added buffers).

The various possible interrupt conditions associated with all the buffers are assembled by the Multiplex Controller into one single 16-bit word which can be interrogated at any time by computer command. This 16-bit word comprises two 8-bit halves. Each half comprises one bit for each of the 8 buffers. In one half, a bit is on if an I/O operation is terminated for the particular buffer because the last word of the designated block of memory has been transferred. In the other half, the bit is on for a particular buffer if a received signal indicates a termination of an input operation,

or if a received signal indicates that a new message is commencing without the buffer being put in an input mode.

If any of the 16 interrupt bits occur, a single interrupt signal is sent to the computer. The computer program determines the cause of the interrupt by interrogating the interrupt status register of the Multiplex Controller.

PROGRAMMING CONSIDERATIONS

Operation of the Multiplex Controller and Buffers are under computer program control. There are four aspects of programming for control and processing of associated data:

- 1) Setup of blocks of Memory for data transfer over the communication lines.
- 2) Direct Control of the buffers.
- 3) Processing required because of interrupts.
- 4) Interrogation of Buffer and Multiplex Controller Status.

Memory Setup:

Prior to a transmit or receive operation by a particular buffer, a block of memory must be designated for storage of the data being transferred. If a transmission is to be made, the data to be transmitted must be stored in the designated block of memory prior to transmission, starting with the first word in the lowest number address. Data meant for modem transmission are stored in successive words such that bit 16 or 18 is

transmitted first and bit 1 last. Bit 16 or 18 of one word follows bit 1 of the preceding word.

A block of memory comprising N words is designated by beginning and ending addresses of the block of memory in two predetermined words in memory. The beginning address is stored in location $7500 + B$, where B is the buffer number with a value $0 \leq B \leq 77$ (octal notation). The ending address is stored in $7600 + B$. As an example, assume that a block of 140 words (octal) are to be designated for Buffer number 3, and that the beginning address is to be 4400. The program must store 4400 in 7503, and 4537 in 7603.

Control of Buffers:

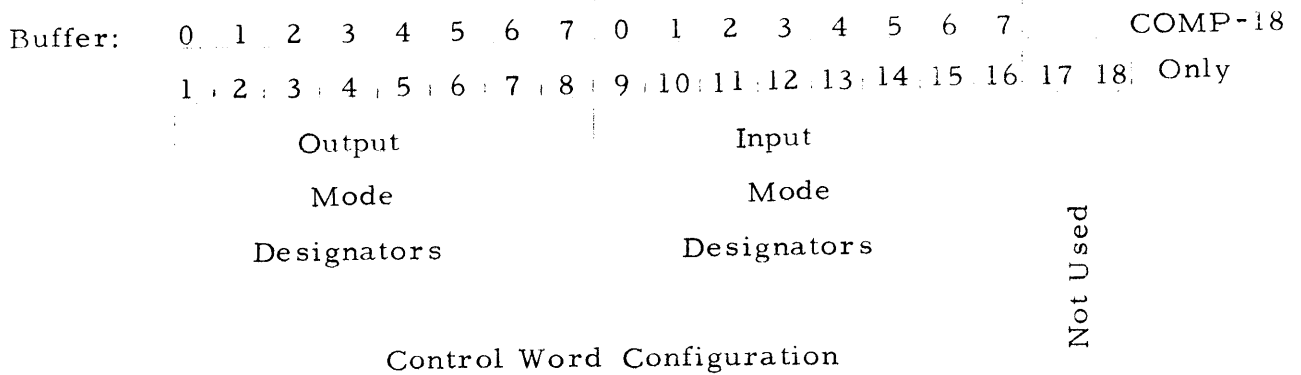
Control of the Buffers are performed through OUT function commands executed by the COMP-16/18. (See the COMP-16 or COMP-18 reference or programming manual for description of COMP-16/18 commands.)

All buffers associated with a particular Multiplex-Controller are controlled by means of a single 16-bit Control word transferred to the Multiplex Controller with one OUT function command. Each two bits of this word are associated with one of the eight buffers. One of these bits, if it has the value of one, is for designating an output function, and one for an input. If both bits are zero, neither an input nor output function is designated.

The Control word is transferred to one of the eight Multiplex Controllers by means of an OUT command with an address of $40 + M$, where M is the number of the Multiplex - Controller, $0 \leq M \leq 7$.

When a word is transferred, it must contain the correct operating conditions of all buffers. Thus, if a particular buffer is in an input state, and a second

buffer must change state, the bit designating an input state for the first buffer must be kept as a one even though the control bits of the second buffer change.



Operating Data comprising two words may be supplied to each buffer by means of an OUT command with an address of 300 + B where B is the buffer number, 00 < B < 77. Operating data is for one of two purposes depending upon the type of buffer:

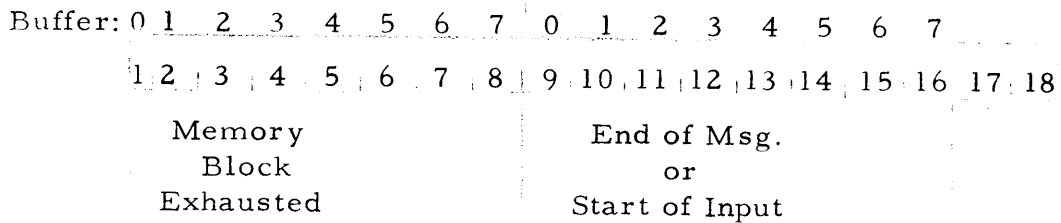
- 1) For a Data Modem Buffer, the Operating Data comprise a binary number of up to 5 bits identifying the number of bits comprising each word of the transmitted message format. The binary number can be any value up to 18 (16 for the COMP-16). The number is taken from bits 12 to 16 of the Accumulator when the OUT command is obeyed.
- 2) For the Teletype Buffer, the Operating Data comprise the End of Message Character Code which identifies the end of a received transmission. The Code is secured from bits 9-16 of the Accumulator.

The operating data remain stored in the buffer indefinitely and need be renewed only when there is a change, or when the system is first started after power-up.

Interrupt Processing:

When an interrupt is caused by a condition involving a Buffer, an interrupt signal is supplied by the Multiplex Controller to the COMP-16/18 Interrupt Section. Each Multiplex Controller supplies a separate interrupt signal so that the program can determine from interrogating the interrupt register by means of a RIN command with address of 010 which Controller caused the interrupt. (The assignment of interrupt lines varies with the application; hence, the identity of the bit in relation to the controller will vary.)

When the Controller identity is known, an Interrupt Status register for that Controller may be interrogated under program control using a RIN command with an address of 040 + M, where M is the number of the particular Multiplex Controller, 0 ≤ M ≤ 7.



Multiplex-Controller Interrupt Status Word

If the interrupt indicates that a memory block has been exhausted, the program must immediately supply new addresses defining a block in words 7500 + B and 7600 + B, then re-initiate the Input or Output operation for the particular buffer. (An interrupt indicating an end of block stops any input or output process in operation by the particular buffer.)

If the interrupt indicates that the received signal indicates an end of message (a bit 9 to 16 is on in the input mode), the processor may take whatever action is deemed necessary, such as putting the buffer in an idle

state, leaving it in an input state with new block addresses, or initiating an output state.

If the interrupt indicates that an input signal is received without an input mode being active (a bit 9 to 16 is on not in the input state), the processor must set up a block of memory and call for an input state, or else the input data will be ignored.

In general, the computer has about 1.6 milliseconds to respond to an interrupt caused by a buffer operating with a modem at 9600 baud, and proportionately more time with lower speed modems.

Status Interrogation:

Upon the occurrence of an interrupt, or anytime during computer processing, the computer can interrogate the status of any buffer. This interrogation takes place by means of a RIN command with an address of 300 + B (octal notation) where B is the number of the Buffer, 00-B-77, (octal notation). When this command is obeyed, a set of status bits are put into the accumulator. The meaning of these bits are according to the following two tables (a binary 1 in the bit is a true state, a zero is false):

Data Modem Buffer

Bit 16	Data Set Ready)	
Bit 15	Clear to Send (if used))	From
Bit 14	Ring Indicator (if used))	Modem
Bit 13	Line Signal Being Received)	
Bit 12	Signal Quality Detector (if used))	
Bit 11	Input Mode On)	
Bit 10	Output Mode On)	
Bit 9	Service Request (of Controller))	
Bits 3-8	Value of Word Size Indicator)	
Bits 1-2	Not Used)	

Teletype Buffer

Bit 16	End of Message Character Received
Bit 15	Not Used
Bit 14	Not Used
Bit 13	Input Signal Received
Bit 12	Not Used
Bit 11	Input Mode On
Bit 10	Output Mode On
Bit 9	Service Request (of Controller)
Bits 1-8	End of Message Character Code (for which the Buffer is looking).