AN/UYK-7(V)

The Next Generation

UNIVAC

THE NEXT GENERATION

The U.S. Navy's newest "next generation" computer is now ready for service. Built by Univac Federal Systems Division, under the sponsorship of the Naval Ship Engineering Center, the AN/UYK-7(V) computer represents a major advancement in real-time data processing.

Designed to cope with the increasing complexity of modern shipboard operations, AN/UYK-7(V) is a reliable, general purpose, high performance computer — adaptable to a wide variety of real-time data processing applications. These applications include signal processing, command and decision, control and information systems.

The AN/UYK-7(V) combines the advantages of modular "building block" construction and microelectronic integrated circuits to provide higher reliability . . . faster processing speeds . . . and greater data processing capabilities than any militarized computer presently in service. Yet the AN/UYK-7(V) is smaller in physical size, weighs less, and has a lower power consumption than the normal large scale digital computer. Through the use of this unique, modular "building block" design concept, the AN/UYK-7(V) provides for ease of system expansion and adaptation to changing mission requirements.

Whether your requirements emphasize large, high speed input/output capability, multi-processing capability or large memory capacity, the AN/UYK-7(V) can be adapted to your needs. Updating the system for meeting future changing environmental and operational requirements is possible without extensive computer re-design. Expansion is achieved by adding only those modules necessary for providing the required functions.

The AN/UYK-7(V) multi-processing capabilities, combined with memory sharing by both the processors and the input/output controllers, plus memory overlap and interleaving features, allows an economic selection of modules to process more data in much shorter time and with much less hardware.

In the past, shipboard operational conditions may have required three or more separate or different unit computers to perform the various data processing tasks, thus compounding problems in equipment standardization, maintenance and logistics. The compact AN/UYK-7(V) modularized computer offers the opportunity to standardize all shipboard digital computers for increased system reliability — thus reducing the costs normally incurred in maintaining extensive multi-computer parts inventories, training and repair facilities.

The AN/UYK-7(V) computer represents a refinement of the unit computers presently operating aboard ships of the fleet. It is designed to meet the Navy's expanded electronic data processing plans, and enables a new concept of tactical planning through its large scale, real-time data processing capabilities.

HISTORY

Development of the AN/UYK-7(V) Digital Data Computer System began in December 1967 when the Naval Ship Systems Command awarded its initial contract to Univac.

As a major supplier of data processing systems and sub-systems to the Department of Defense and other government agencies, Univac Federal Systems Division has maintained close contact with the various U.S. Navy Commands which are involved in the development of digital systems.

Over the years, Univac has provided maximum interchange of technical and management information with the Navy through regular briefings on Univac activities and participation by Univac personnel at symposiums and technical sessions sponsored by Navy organizations.

Through this active interchange of information, Univac has become knowledgeable of the many requirements and problems existing in the development of tactical data systems. This knowledge, in addition to Univac's long record of experience in building computers for the Navy, assures the successful completion of the AN/UYK-7(V) program and the future systems it will serve.

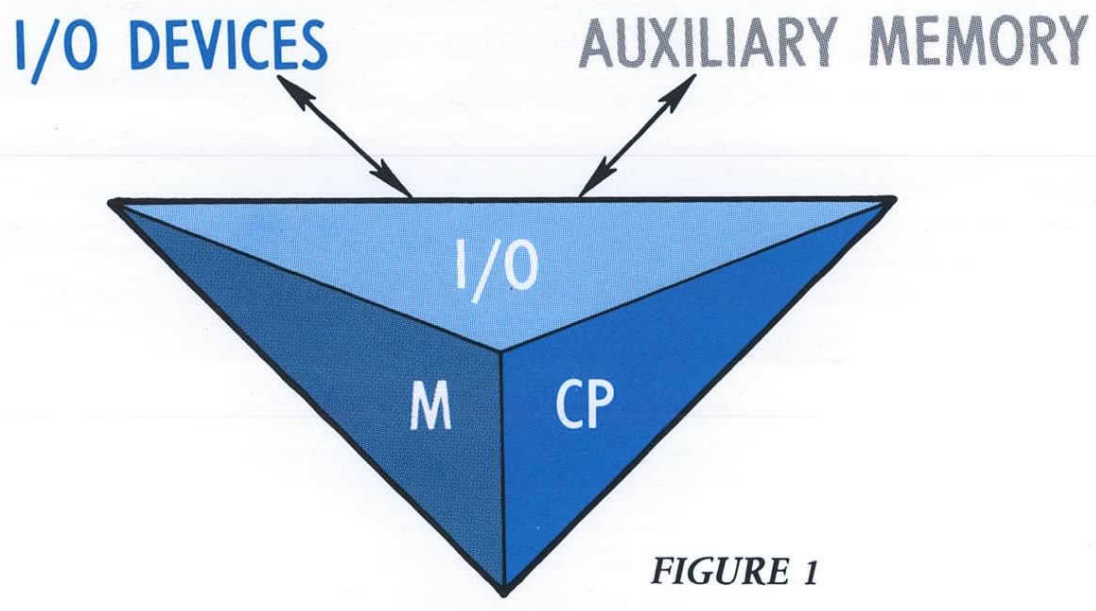


FIGURE 1

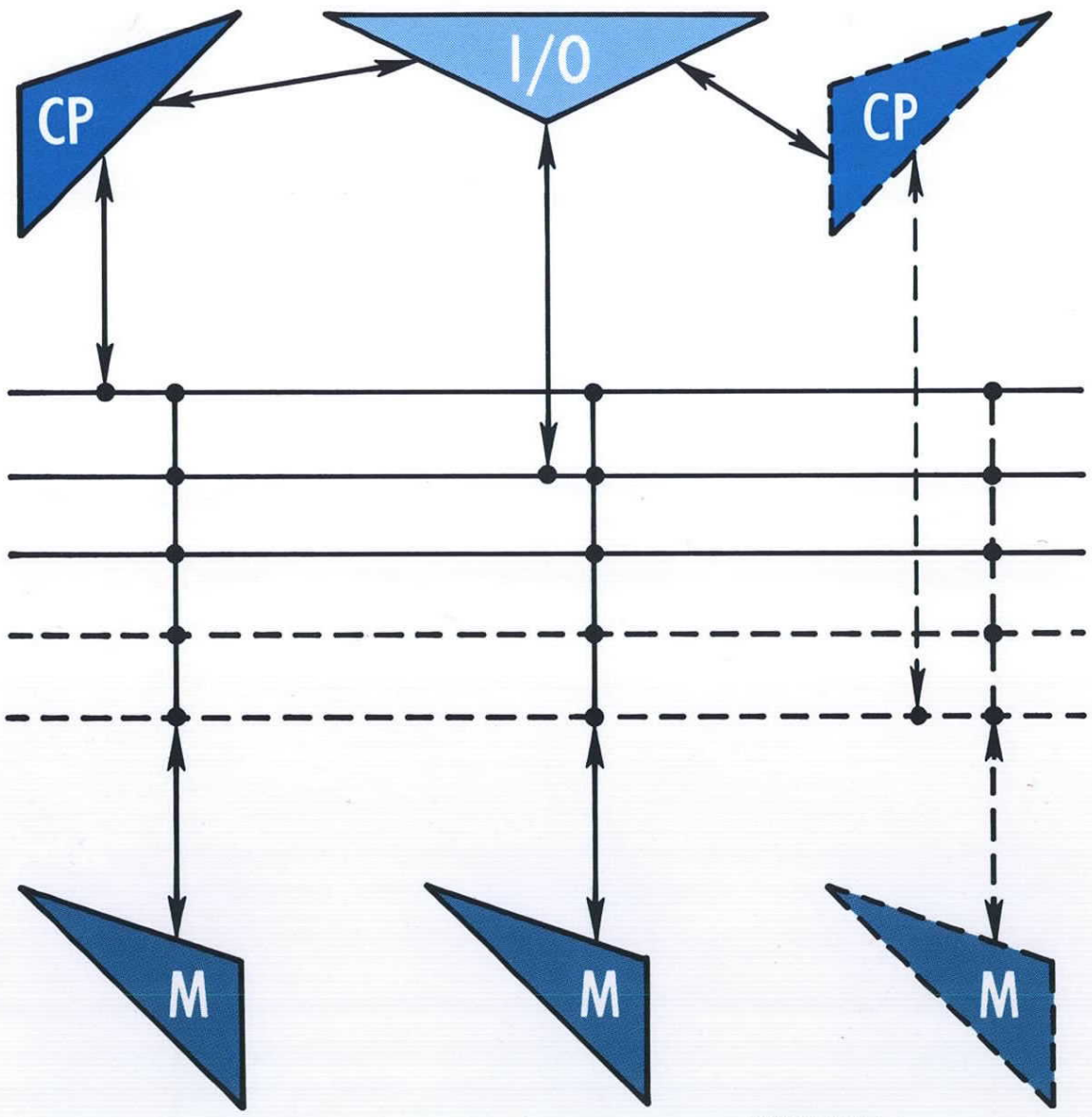


FIGURE 2

MODULAR "BUILDING-BLOCK" CONCEPT

Figure 1 shows a typical configuration of a "unit computer." The central processor module controls the timing of the entire unit. When one portion — processor, memory or input-output controller — is operating, the others must wait for completion to continue their operation. This concept causes many problems in various applications. The "unit computer," because it was designed specifically for a particular application, is not general purpose enough to be used most efficiently for other applications such as weapons control and signal processing.

To solve these applications problems, the Navy considered several solutions. The first, a "compromise computer," would include only the features needed for satisfying each application. The disadvantage of this approach is that none of the applications systems would operate in its most efficient mode. Another approach, the "super-computer," would consist of a large scale computer capable of solving all applications problems. However, by its very size, its cost would be excessive for initial installation.

The final solution, and the solution used in the design of the AN/UYK-7(V), is the "building-block" concept. This modular concept places complete functional sections within independent modules. To provide maximum versatility, the processor, memory and input-output controller modules communicate with each other on a request and acknowledge basis.

As shown in figure 2, each module operates independently under its own control. A prime advantage of this design is that it provides for easy adaptation to changing operational and mission requirements. Thus, an initial AN/UYK-7(V) installation can be economically expanded in the field to meet newer and larger requirements through easy "add on" of needed modules. By the nature of the modular "building-block" design, special purpose equipment can be attached to standard interfaces.

GENERAL CHARACTERISTICS

The AN/UYK-7(V), because of its design, provides for multi-processing and shared-memory operation. All the features required for an efficient multi-processing system are designed into the AN/UYK-7(V).

The instruction repertoire of the AN/UYK-7(V) is extensive, providing separate hardware functions for double-precision fixed-point and floating-point arithmetic, as well as the many special functions required for multi-processing.

The central processor cycle time is 750 nanoseconds, and the memory module cycle time is 1.5 microseconds. In addition to the basic hardware speeds, several program operational advantages can be gained through the unique design features, such as multiple state operation, which provides the user with a sophisticated system of interrupt levels; processor overlapping and interleaving of memory banks, which avoids conflicts in time memory shared systems; and command

chaining of I/O controller instructions, which provides system advantages in repetitive I/O operations through parallel operation with the central processor.

Optional electrical interface capabilities (NTDS FAST, SLOW, A-NEW, and SERIAL) combined with the ability to handle parallel slow, fast and/or serial data transmissions permit the AN/UYK-7(V) to operate with most presently used external data sources.

The AN/UYK-7(V) has been designed to provide maximum reliability. The mean-time-between-failure is 2000 hours, for the basic system. The mean-time-to-repair is 15 minutes. Components, and packaging techniques, are military approved.

EXPANSION CHARACTERISTICS

The AN/UYK-7(V) computer is configured from the following modules, as required:

Central Processor
Input/Output (I/O) Controller
Input/Output (I/O) Adapter, 4, 8, 12 or 16 I/O Channels)
16K Word Memory (16,384 32-bit words)
Power Supply

The AN/UYK-7(V) modular design concept eliminates many of the system limiting factors imposed by present-day unit computers.

Expansion limits are determined only by the amount of inter-module communication required and the addressing capability of each module. Each central processor uses two memory accesses and each I/O controller uses one access.

The central processor module can communicate with four input-output controllers, and up to 16 memory modules. The memory modules each have eight accesses. The input-output controller communicates through an input-output adapter to 16 channels. It also can communicate with three central processor modules and up to 16 memory modules.

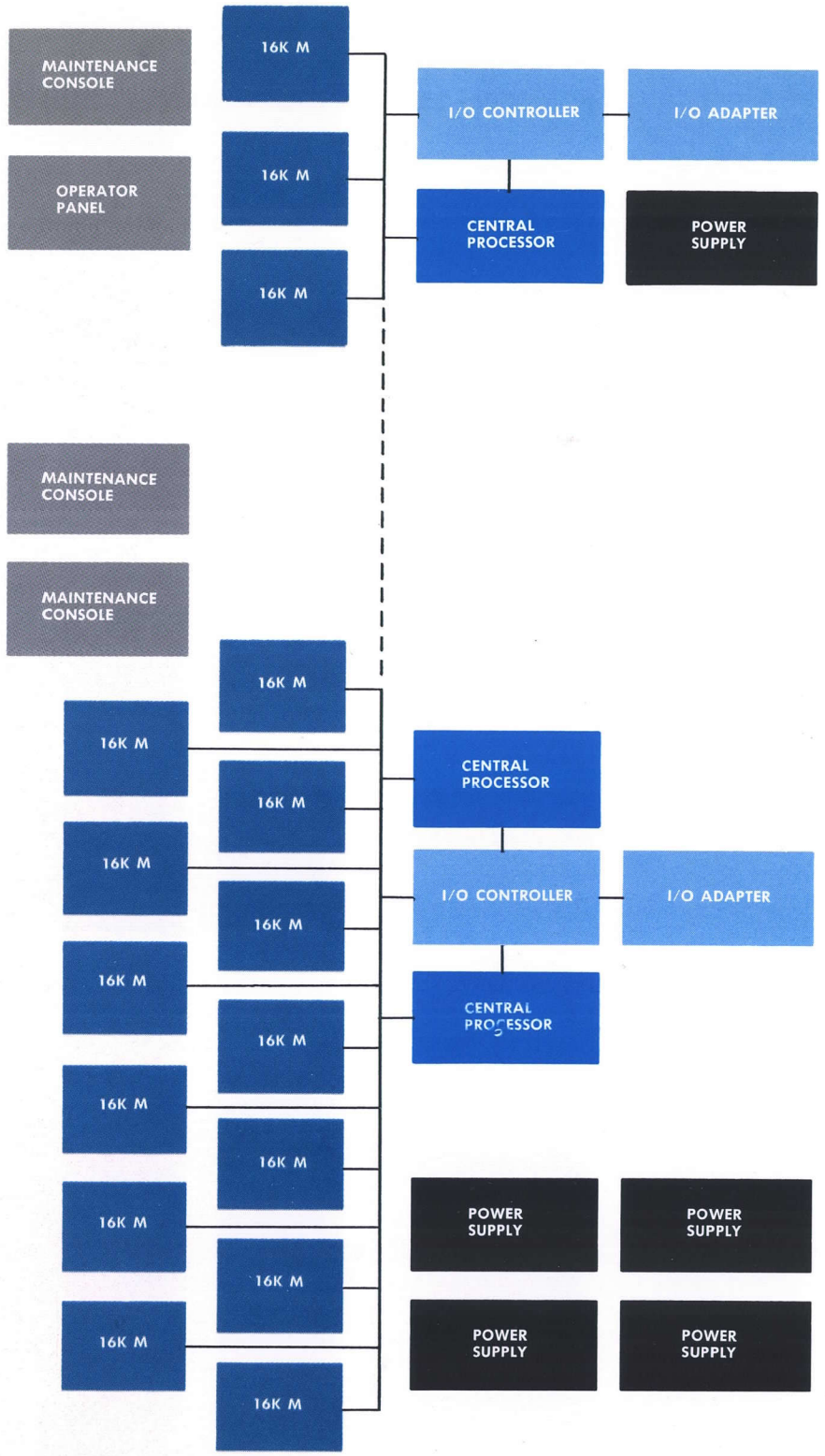
EXPANSION CAPABILITIES

Modular multi-point connections, combined with asynchronous operation of the central processor, memory and I/O controller components permit a wide variety of computer configurations. Typical large-scale AN/UYK-7(V) configurations having multiple central processors, I/O controllers and shared memory units can include:

TWO CENTRAL PROCESSOR MODULES
Four I/O controller modules
Four I/O adapter modules
(64 I/O channels)
Sixteen memory modules (262,144 32-bit words)
Five power supply modules
Two maintenance consoles

(or)

THREE CENTRAL PROCESSOR MODULES
Two I/O controller modules
Two I/O adapter modules
(32 I/O channels)
Sixteen memory modules (262,144 32-bit words)
Five power supply modules
Three maintenance consoles



APPLICATIONS

The AN/UYK-7(V) has been designed to operate flexibly in many distinct applications. In the total environment, such as a ship, there are many diverse operations. These include sensor processing, weapons control, logistics and over-all command and decision. Following is a brief description of these applications, as they are handled by the AN/UYK-7(V) computer.

Radar Signal Processing

A major shipboard application is that of signal processing. In this application, radar, beacon, sonar, and those signals used in electronic warfare, must be processed and acted upon in a minimum of time. Radar applications provide a continual input of data in a real-time environment. This requires a great deal of processing in order to determine targets, direction, and other information. The combination of this large amount of data, and the complex processing required, places an enormously large load on the computer. In the AN/UYK-7(V), the real-time data processing task is handled easily due to the fast, independent operation of the modular functional sections, the high speed memory and fast central processing cycle time, as well as the very large and comprehensive instruction repertoire which allows computations to be performed in a high speed real-time mode. The handling of input data in a real-time response is accomplished by the very fast input-output section, which can be expanded by additional input-output controllers and input-output adapter modules if they are required.

Weapons Control Systems

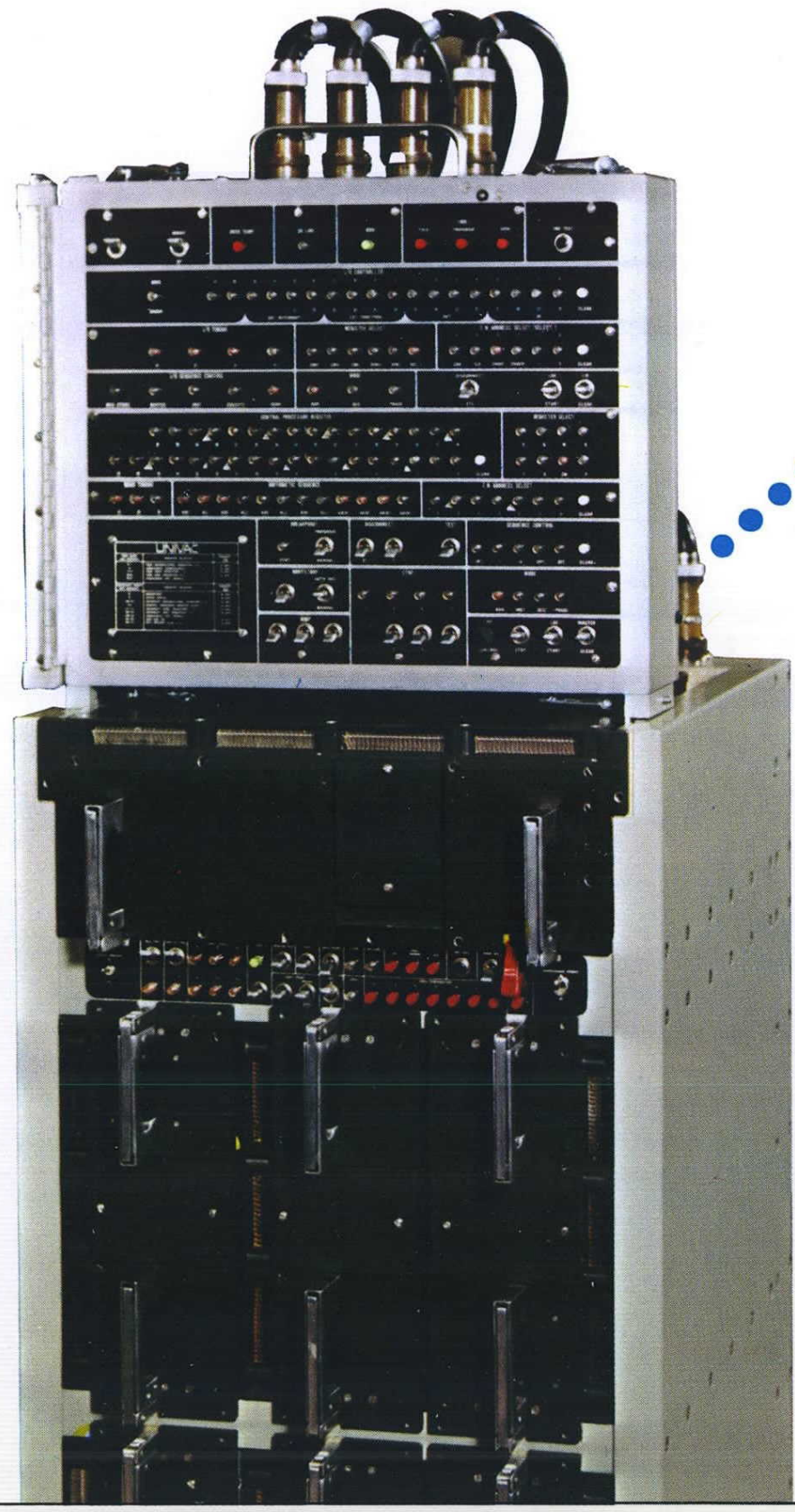
In addition to weapons control systems, other control systems normally found on board ship include air traffic, radar, electronic countermeasures, and navigational control systems. Complex weapons control systems, as with signal processing applications, require high computational capabilities in the central processor. While the quantity of input data is lower, input is received from more than one source. Once again, the AN/UYK-7(V) is uniquely qualified for this application since the number of input-output channels can be expanded to the number necessary for the multiple input data. In addition, the complex computation required for swiftly determining directional commands for the weapons is easily accomplished with the floating-point arithmetic feature, double-precision hardware, multiple accumulators, and by the 750 nanosecond speed of the central processor.

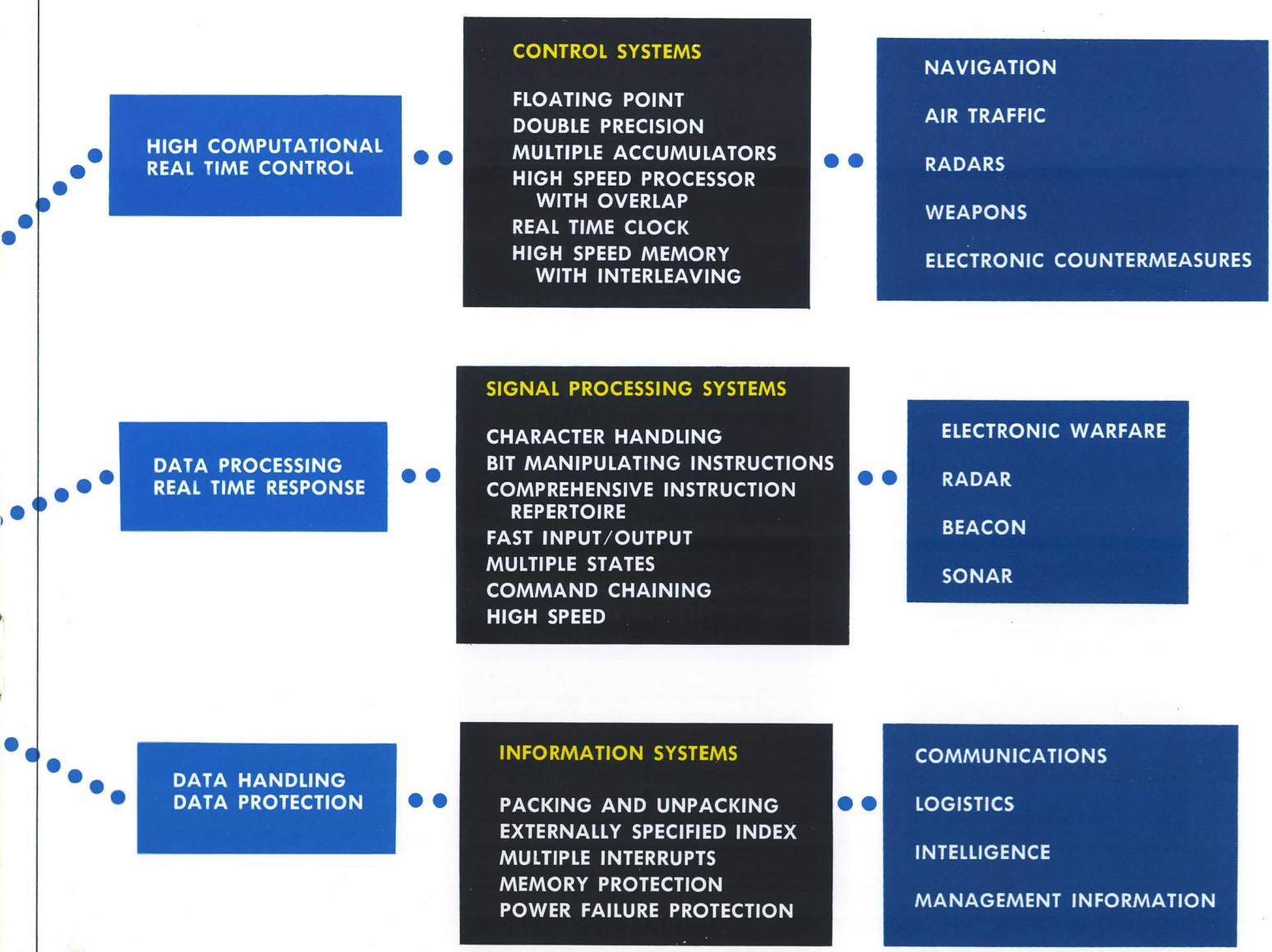
Information Systems

Logistics, intelligence control, communications and other management information is an additional problem to be solved. In this area, the operational requirements are for accepting and storing a very large amount of data, providing minimum computation on this data, and then directing selected amounts of it to various command sources. The modular memory feature suits this application quite well in that additional memory components can be added to accept a large store of data. The reduction and selective communication of this data can be handled by the AN/UYK-7(V) through use of its flexible input-output structure. The memory protect feature allows isolation of data and insures against access to data by unauthorized personnel.

Command and Decision Systems

All of these different applications are combined within a total command and decision network. Here again, rather than using a different computer, the AN/UYK-7(V) can be structured to provide those features unique to the command and decision requirements. Because of the modular capabilities, the user does not require different computers because the AN/UYK-7(V) functions in itself as a whole family of computers, meeting each specific requirement.




HIGH COMPUTATIONAL
REAL TIME CONTROL
CONTROL SYSTEMS
FLOATING POINT
DOUBLE PRECISION
MULTIPLE ACCUMULATORS
HIGH SPEED PROCESSOR
WITH OVERLAP
REAL TIME CLOCK
HIGH SPEED MEMORY
WITH INTERLEAVING
NAVIGATION
AIR TRAFFIC
RADARS
WEAPONS
ELECTRONIC COUNTERMEASURES
DATA PROCESSING
REAL TIME RESPONSE
SIGNAL PROCESSING SYSTEMS
CHARACTER HANDLING
BIT MANIPULATING INSTRUCTIONS
COMPREHENSIVE INSTRUCTION
REPERTOIRE
FAST INPUT/OUTPUT
MULTIPLE STATES
COMMAND CHAINING
HIGH SPEED
ELECTRONIC WARFARE
RADAR
BEACON
SONAR
DATA HANDLING
DATA PROTECTION
INFORMATION SYSTEMS
PACKING AND UNPACKING
EXTERNALLY SPECIFIED INDEX
MULTIPLE INTERRUPTS
MEMORY PROTECTION
POWER FAILURE PROTECTION
COMMUNICATIONS
LOGISTICS
INTELLIGENCE
MANAGEMENT INFORMATION

AN/UYK-7(V)
CENTRAL PROCESSOR INSTRUCTION REPERTOIRE

Octal Code	Mnemonic Code	Name	Overlapped Execution Time (μ sec)
01 0	OR	Inclusive OR	1.5
01 1	SC	Selective Clear	1.5
01 2	MS	Masked Selective Substitute	1.5
01 3	XOR	Exclusive OR	1.5
01 4	ALP	Add Logical Product	1.5
01 5	LLP	Load Logical Product	1.5
01 6	NLP	Add Negative Logical Product	1.5
01 7	LLPN	Load Logical Product Next	1.5
02 0	CNT	Count Ones	7.5
02 2	XR	Execute Remote	1.5
02 3	XRL	Execute Remote Lower	1.5
02 4	SLP	Store Logical Product	1.5
02 5	SSUM	Store Sum	2.5
02 6	SDIF	Store Difference	2.5
02 7	DS	Double Store A	3.0
03 0	ROR	Replace Inclusive OR	2.5
03 1	RSC	Replace Selective Clear	2.5
03 2	RMS	Replace Masked Selective Substitute	2.5
03 3	RXOR	Replace Exclusive OR	2.5
03 4	RALP	Replace Add Logical	2.5
03 5	RLP	Replace Logical Product	2.5
03 6	RNLP	Replace Add Negative Logical Product	2.5
03 7	TSF	Test and Set Flag	2.5
05 0	DL	Double Load A	3.0
05 1	DA	Double Add A	3.0
05 2	DAN	Double Add Negative A	3.0
05 3	DC	Double Compare A	3.0
06 0	FA	Floating Point Add	6.0
06 1	FAN	Floating Point Add Negative	6.0
06 2	FM	Floating Point Multiply	10.0
06 3	FD	Floating Point Divide	16.0
06 4	FAR	Floating Point Add with Round	6.0
06 5	FANR	Floating Point Add Negative with Round	6.0
06 6	FMR	Floating Point Multiply with Round	10.0
06 7	FDR	Floating Point Divide with Round	16.0
07 0	XS	Enter Executive State	3.0
07 1	AEI	Allow Interrupt	3.0
07 2	PEI	Prevent Interrupt	3.0
07 3	LIM	Load, Enable IOC Monitor Clock	3.0
07 4	IO	Initiate I/O	3.0
07 5	IR	Interrupt Return	3.0
07 6	RP	Repeat	3.0
10	LA	Load A	1.5
11	LXB	Load A and Index B	1.5
12	LDIF	Load Y-A	1.5
13	ANA	Add Negative A	1.5
14	AA	Add A	1.5
15	LSUM	Load Y A	1.5
16	LNA	Load Negative A	1.5
17	LM	Load Magnitude A	1.5
20	LB	Load B	1.8
21	AB	Add B	1.8
22	ANB	Add Negative B	1.8
23	SB	Store B	1.5
24	SA	Store A	1.5
25	SXB	Store A and Index B	1.5
26	SNA	Store Negative A	1.5
27	SM	Store Magnitude A	1.5
32	BZ	Clear Bit	2.5
33	BS	Set Bit	2.5
34	RA	Replace Add	2.5
35	RI	Replace Increment	2.5
36	RAN	Replace Add Negative	2.5
37	RD	Replace Decrement	2.5
40	M	Multiply	7.5
41	D	Divide	14
42	BC	Compare Bit to Zero	1.5
43	CXI	Compare Index Increment	1.8
44	C	Compare A	1.5
45	CL	Limit Compare A	1.5
46	CM	Masked Compare A	1.5
47	CG	Gated Compare A	1.5
50 0	JEP	Jump on Even Parity	2.25
50 1	JOP	Jump on Odd Parity	2.25
50 2	DJZ	Jump on Double Precision Zero	2.25
50 3	DJNZ	Jump on Double Precision Not Zero	2.25
51 0	JP	Jump A Positive	1.5
51 1	JN	Jump A Negative	1.5
51 2	JZ	Jump A Zero	1.5
51 3	JNZ	Jump A Not Zero	1.5
52 0	LBJ	Load B and Jump	1.8
52 1	JBNZ	Jump B Not Zero	1.8
52 2	JS	Jump SY b	1.5
52 3	JL	Unconditional Jump Lower	1.5
53 00	JNF	Jump on No Overflow	1.5
53 01	JNE	Jump on Not Equal	1.5
53 10	JOF	Jump on Overflow	1.5
53 11	JE	Jump on Equal	1.5
53 21	JG	Jump on Greater Than	1.5
53 31	JGE	Jump on Greater Than or Equal	1.5
53 41	JLT	Jump on Less Than	1.5
53 51	JLE	Jump on Less Than or Equal	1.5
53 61	JNW	Jump Not Within Limits	1.5
53 71	JW	Jump Within Limits	1.5
53 2	RJ	Return Jump	3.0
53 2	RJC	Return Jump on Conditional Setting	3.0
53 2	RJSC	Return Jump, Stop on Conditional Setting	3.0
53 3	J	Jump	1.5
53 3	JC	Jump on Conditional Setting	1.5
53 3	JSC	Jump Stop on Conditional Setting	1.5
54	LCT	Load Task CMR with Y	1.5
55	LCI	Load Interrupt CMR with Y	1.5
56	SCT	Store Task CMR	1.5
57	SCI	Store Interrupt CMR	1.5
60	HSCT	Store Task CMR in A	1.5
60	HSCI	Store Interrupt CMR in A	1.5
61	HLCT	Load Task CMR	1.5
61	HLCI	Load Interrupt CMR	1.5
62	HLC	Shift Left Circularly	1.8
63	HDLC	Shift Double Left Circularly	1.5
64	HRZ	Shift Right Fill Zeros	1.5
65	HDRZ	Shift Double Right Fill Zeros	1.5
66	HRS	Shift Right Fill Sign	1.5
67	HDRS	Shift Double Right Fill Sign	1.5
70 0	HSF	Scale Factor A	2.0
70 1	HDSF	Double Scale Factor	2.0
70 2	HCP	Complement A	*1.5/0.75
70 3	HDCP	Double Complement	*1.5/0.75
71 0	HOR	Inclusive OR A	*1.5/0.75
71 1	HA	Sum	*1.5/0.75
71 2	HAN	Difference	*1.5/0.75
71 3	HXOR	Exclusive OR A	*1.5/0.75
71 5	HAND	And A	*1.5/0.75
74 0	HM	Multiply	7.75/7.75
74 1	HD	Divide	14/14
74 2	HRT	Square Root	15/15
74 3	HLB	Load Ba with Bb	1.5
74 4	HC	Compare Aa with Ab	*1.5/1.0
74 5	HCL	Limit Compare Register	*1.5/1.0
74 6	HCM	Mask Compare Register	*1.5/1.0
74 7	HCB	Compare Ba with Bb	1.5
77 0	HSIM	Store I/O Monitor Clock	3.0
77 1	HSTC	Store RTC	3.5
77 4	HPI	Prevent Class III Interrupts	2.25
77 5	HAI	Allow Class III Interrupts	2.25
77 6	HALT	Stop	1.5

*High value when instruction is in upper half of word; low value when instruction is in lower half of word.

I/O CONTROLLER COMMANDS

10	IB	Initiate Input Buffer on Cj	3.25
11	OB	Initiate Output Buffer on Cj	3.25
12	FB	Initiate EF Buffer on CJ	3.25
13	XB	Initiate EI Buffer on Cj	3.25
14k0	TIB	Terminate Input Buffer on Cj	3.0
14k1	TOB	Terminate Output Buffer on Cj	3.0
14k2	TFB	Terminate EF Buffer on Cj	3.0
14k3	TXB	Terminate EI Buffer on Cj	3.0
15k0	IMIR	Set Input Monitor Interrupt Request on Cj	2.5
15k1	OMIR	Set Output Monitor Interrupt Request on Cj	2.5
15k2	FMIR	Set EF Monitor Interrupt Request on Cj	2.5
15k3	XMIR	Set EI Monitor Interrupt Request on Cj	2.5
16k0	AIC	Set Input Chain Active on Cj	2.5
16k1	AOC	Set Output Chain Active on Cj	2.5
16k2	AFC	Set EF Chain Active on Cj	2.5
16k3	AXC	Set EI Chain Active on Cj	2.5
17m0	TBZ	Test for Bit Not Set	4.0
17m1	TBS	Test for Bit Set	4.0
20	JIO	Jump Command to Y	2.5
22	LICM	Load Control Memory	3.25
23	ILTC	Load RTC	4.0
24	SICM	Store Control Memory	2.75
25	IBS	Set Bit	3.25
26	IBZ	Clear Bit	3.25
27	ITSF	Test and Set Flag	3.25

AN/UYK-7(V) DIGITAL COMPUTER SPECIFICATIONS

RANGE OF CAPABILITY

- *MINIMUM*

ONE PROCESSOR MODULE
ONE INPUT/OUTPUT CONTROLLER MODULE
ONE INPUT/OUTPUT ADAPTER MODULE (4 CHANNELS)
ONE MEMORY MODULE (16,284 WORDS)
ONE POWER SUPPLY MODULE

- *TYPICAL LARGE*

THREE PROCESSOR MODULES
TWO INPUT/OUTPUT CONTROLLER MODULES
TWO INPUT/OUTPUT ADAPTER MODULES (32 CHANNELS)
SIXTEEN MEMORY MODULES (262,144 WORDS)
FIVE POWER SUPPLY MODULES

FUNCTIONAL

- *CENTRAL PROCESSOR*

GENERAL PURPOSE, PARALLEL, BINARY
FLEXIBLE BASE AND INDEX ADDRESSING
CASCADED INDIRECT ADDRESSING
REPERTOIRE OF 131 INSTRUCTIONS
FIXED AND FLOATING POINT ARITHMETIC
SINGLE AND DOUBLE PRECISION ARITHMETIC
INSTRUCTION WORD LENGTH — 16 AND 32 BITS
DATA WORD LENGTH — 8/16/32 BITS
VARIABLE LENGTH CHARACTER ADDRESSING
MULTIPLE ACCUMULATORS
MONITOR CLOCK
MEMORY OVERLAP

- *MEMORY*

TEMPERATURE STABLE COINCIDENT CURRENT CORE
MODULAR IN UNITS OF 16,384 — 32 BIT WORDS
EXPANDABLE TO 262,144 WORDS
ASYNCHRONOUS OPERATION
EIGHT ACCESSES PER MODULE
1.5 MICROSECONDS CYCLE TIME
BYTE SIZE 8/16/32 BITS
INTERLEAVE

- *INPUT/OUTPUT*

INDEPENDENT ASYNCHRONOUS PROGRAMMABLE I/O CONTROLLER

EACH I/O CONTROLLER MAY COMMUNICATE WITH THREE CENTRAL PROCESSORS

SIXTEEN CHANNELS PER I/O CONTROLLER

OPTIONAL ELECTRICAL INTERFACES IN FOUR CHANNEL GROUPS
NTDS SLOW (—15 VOLT)
NTDS FAST (—3 VOLT)
A-NEW (+3.5 VOLT)
SERIAL

INTEGRATED CIRCUIT BUFFER CONTROL MEMORY (64 WORDS)

MAXIMUM INPUT/OUTPUT WORD RATE PER I/O CONTROLLER — 167 KHZ (SINGLE-CHANNEL) NTDS FAST AND A-NEW, 41 KHZ (SINGLE CHANNEL) NTDS SLOW, 175 KHZ (SINGLE-CHANNEL) SERIAL, 1 MHZ (TOTAL INTERFACE)

REAL TIME CLOCK

GENERAL CHARACTERISTICS

WHOLE-WORD, HALF-WORD OR QUARTER-WORD CAN BE SELECTED FOR USE IN THE ARITHMETIC OPERAND

FULL DOUBLE-PRECISION FIXED POINT ARITHMETIC, INCLUDES ADD, SUBTRACT, ENTER, STORE, TEST, AND BRANCH OPERATIONS

FLOATING POINT ARITHMETIC WITH MANTISSA LENGTH OF 32 BITS AND A CHARACTERISTIC LENGTH OF 16 BITS

A SHIFT MATRIX ACCOMPLISHES MULTIPOSITION SHIFTS IN ONE PLACE SHIFT TIME. SHIFTING CAN BE EITHER LOGICAL (ZERO-FILLED), ARITHMETIC (SIGN-FILLED) OR CIRCULAR

EIGHT ARITHMETIC ACCUMULATORS ALLOWS PARALLEL AND CUMULATIVE COMPUTATION, DUPLICATE SETS OF ACCUMULATORS FOR USE IN THE INTERRUPT AND TASK STATES

REGISTER-TO-REGISTER ARITHMETIC AND LOGICAL OPERATIONS THROUGH THE USE OF HALF-WORD INSTRUCTIONS

A COMPLETE SET OF LOGICAL OPERATIONS AND COMPARE INSTRUCTIONS

PHYSICAL

- *CONSTRUCTION*

MODULAR, EXPANDABLE, CONDUCTION COOLING

- *BASIC CONFIGURATION*

ONE CENTRAL PROCESSOR MODULE
ONE INPUT/OUTPUT CONTROLLER MODULE
ONE INPUT/OUTPUT ADAPTER MODULE (16 CHANNELS)
THREE MEMORY MODULES (49,152 WORDS)
ONE POWER SUPPLY MODULE
ONE MAINTENANCE CONSOLE

- *VOLUME* (BASIC)

10.4 CUBIC FEET

- *WEIGHT* (BASIC)

500 POUNDS

- *POWER CONSUMPTION*

2300 WATTS (BASIC SYSTEM)

- *SIZE*

41 IN. HEIGHT, 20 IN. WIDTH, 22 IN. DEPTH

- *MAINTENANCE*

THROW AWAY PRINTED CIRCUIT CARDS

- *RELIABILITY*

2000 HOURS MTBF (EST.)

- *ENVIRONMENTAL*

MIL-E-16400 CLASS 1

- *OPERATING TEMPERATURE*

—54°C TO +65°C

- *NON-OPERATING TEMPERATURE*

—62°C TO +75°C

- *VIBRATION*

MIL-STD-167, TYPE 1

- *SHOCK*

MIL-S-901, CLASS 1, GRADE A

FAST . . . COMPACT . . . RELIABLE

AN/UYK-7(V) is designed to perform data processing tasks in a more reliable, real-time manner, and with greater speed and efficiency, than ever before.

Using creative hardware design, Univac has developed the AN/UYK-7(V) into a highly flexible computing system. The system can perform all data processing tasks now handled by a series of unit computers. The use of modular design permits a new level of equipment standardization. Standard modules simplify logistic and support requirements, and greatly reduce over-all user costs. Support software and a powerful instruction repertoire provide the facility for developing and debugging computer programs.

Fast, compact and reliable, the AN/UYK-7(V) is ready to carry out a diversity of shipboard data processing tasks — now and in the future.

FEDERAL SYSTEMS DIVISION

Univac Federal Systems Division has for many years devoted a major portion of its resources to the solution of real-time military problems encountered in weapons control, command and decision, and instrumentation systems. This experience has encompassed all types of military environments including airborne, spaceborne, shipboard, ground mobile and fixed sites. Because of its concentration in these areas, Univac has developed the unique scientific research, engineering design and development, and the organizational structures necessary for designing, developing and manufacturing "state-of-the-art" digital computing systems. In addition, as a Division of the Sperry Rand Corporation, Univac has available, through the diversified resources of other corporate divisions, the synergistic scope of capabilities and disciplines required by today's complex systems problems.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Additional information for the AN/UYK-7(V) system application may be obtained from the regional offices or:

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Director, Navy Marketing
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Thank you for your interest in UNIVAC-Division of Sperry Rand Corporation and, in particular, our newly announced AN/UYK-7 Military Computer System. In response to your recent request, we have enclosed a brief descriptive brochure covering this equipment.

If, after reviewing this data, you should wish additional information for your application, please call our representative in your area as listed below or contact me directly in St. Paul.

Thank you for this opportunity to be of service.

Sincerely,

UNIVAC-Division of Sperry Rand
Federal Systems Division

L. J. Franklin/cw

L. J. Franklin
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LJF/amw
Enclosure