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NOTE: Please forward along with other documentation additional routing

Branch Office:
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P.C. #1146
Cust. Doc. #6242
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Engineer (2)

SYSTEM MEMO

RG-82-887-s.c. (V)
*REV A

Customer	McDonnell Douglas
Sales Order:	432183
S.O.E. Number:	744-0104-00
Charge Number:	432183
Date:	March 25, 1982
From:	R. Gardner

*Please reference System Arrangement Drawing (SAD) No. 6650650 Rev X2

THIS MEMO CONFORMS TO MDEC SPEC B54J0011-14 REV P

REVISION HISTORY

Original issue: January 18, 1982

Revision "A": March 25, 1982

874-B20
/ac

I N D E X

(See Section 1.0 for included options)

Section

1.0 EQUIPMENT SUMMARY

1 each - F2960-01	V76 CPU w/14" Chassis and V77-600 Processor
1 each - F3065-05	Option Board w/PMA V77-600
1 each - F2960-12	CPU Power Supply 37A
1 each - F2961-00	I/O Power Supply 17A
1 each - F2961-06	I/O Chassis
1 each - F2961-05	I/O Expander
2 each - F3024-01	PIM
3 each - F3024-02	BIC
1 each - F2960-13	Map Power Supply
2 each - F3020-02	Memory 64KB
2 each - F3004-00	UASC
1 each - Q6029-XX	Interim Map
1 each - 0102152-007	Filler Panel
1 each - T6315-02	MAINTAIN III - Paper Tape

2.0 SYSTEM I/O BUS LOAD DISTRIBUTION

Primary I/O Buss

Console
Processor
Megamap
Option Board
Non-ECC Memory 128K BYTES (not a load)
I/O Expander #1

I/O Expander #1 I/O Buss

UASC #1
UASC #2
**Floppy Disc
BIC #2
PIM #2
PIM #1
BIC #1
**PMAC
**DIOC
BIC #3
**Matrix Multiplier

**Customer Supplied

3.0 SYSTEM POWER REQUIREMENTS

This system operates from 115VAC, 60HZ, 1 Phase.

3.1 System Power

The following require a standard 15 Amp, 115VAC "U" ground wall connector Hubbell 5230 or equivalent.

2 each - 15 Amp circuit for Power Supply.

All additional equipment mounts in cabinet and uses cabinet AC power.

4.0 SYSTEM ASSIGNMENTS

4.1 Controller Board Slot Assignments V77-6XX/V7X

a. 14" Mainframe Chassis A2

Slot

15	Processor V77-600
9	Memory Map
8	Option Board V77-600
3	Memory #2 64K BYTES
1	Memory #1 64K BYTES

V7X I/O Chassis

RH Slot		LH Slot	
13	I/O Cable	13	PIM #2
12	I/O Expander #1	12	PIM #1
11	Term Shoe	11	BIC #1
9	I/O Cable	**10	PMAC
6	UASC #1	** 9	PMAC
5	UASC #2	** 8	PMAC
** 3	Floppy Disc	** 7	DIOC
2	BIC #2	** 6	DIOC
		5	BIC #3
		4	Term Shoe
		** 3	Matrix Multiplier
		** 2	Matrix Multiplier

**Customer Supplied

4.2 PIM/BIC Assignments

4.2.1 PIM Priority Assignments

PIM #1

Device Address 40
Interrupt Address 100-117
Priority Levels:

0. _____
1. _____
2. _____
3. _____
4. TTY Read Ready
5. TTY Write Ready
6. _____
7. _____

PIM #2

Device Address 41
Interrupt Address 120-137
Priority Levels:

(CUSTOMER USAGE)

0. _____
1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____

4.2.2 BIC Assignments

BIC #1

Device Address 20, 21
Controller Assignments:

1. PMAC **
2. DIOC **
3. _____
4. _____
5. _____

BIC #2

Device Address 22, 23
Controller Assignments:

1. Floppy Disc **
2. UASC #1
3. UASC #2
4. _____
5. _____

BIC #3

Device Address 24, 25
Controller Assignments:

1. Matrix Multiplier **
2. _____
3. _____
4. _____
5. _____

**Customer Supplied

4.3 Device Address Assignments

DA	DEVICE
01	Operator Console
02	UASC #2
03	UASC #1
04	
05	
06	
07	
010	
011	
012	
013	
014	
015	
016	
017	
020	BIC #1
021	BIC #1
022	BIC #2
023	BIC #2
024	BIC #3
025	BIC #3
026	
027	
030	
031	
032	
033	
034	
035	
036	
037	

DA	DEVICE
040	PIM #1 IA = 100-117
041	PIM #2 IA = 120-137
042	
043	
044	All PIMs, ECC Memory
045	MP
046	MAP
047	RTC
050	
051	
052	
053	
054	
055	
056	
057	
060	
061	
062	
063	
064	
065	
066	
067	
070	
071	
072	
073	
074	
075	
076	
077	

4.4 System Priority Assignments - V77-6XX/V7X

1.	MEMORY PROTECT	6.	RTC
2.	PF/R	7.	MAP
3.	BIC #2	8.	PIM #1
4.	BIC #1	9.	PIM #2
5.	BIC #3	10.	CONSOLE

For Priority Drawing refer to System Arrangement Drawing 6650650.

Priority Look Ahead Required [ ] Yes [X] No

The priority look ahead is installed on the I/O Expander.

The Look Ahead components are on the I/O Exp. 44P0670, as indicated per 91C0435.

5.0 MAINFRAME AND MEMORY JUMPER ASSIGNMENTS (V77-6XX)

5.1 Processor Assignments - Refer to 01A1331

1. Install "Processor to Memory Map A" Jumpers.
2. Clock source is CPU clock, jumper J1 to J2.
3. Memory wraparound is more than 32K, E2 to 22B Installed.
4. Memory map is installed, jumper L2 to L3.

5.2 Option Assignments - Refer to 01A1332

1. PFR — Option to be enabled, remove jumpers between E7 and E8, E9 and E10

2. RTC

   FRC = 100 us, add jumper E13 to E18.
   IIC = 10 KHZ, add jumper E13 to E14.

5.2 Option Assignments - Refer to 01A1332 (continued)

3. Memory Parity Switch Location T9

Position A (non error correct memory)
Disable Parity. Add jumper E61 to E62.

4. Memory Protect

Disable Memory Protect. Remove jumper E98 to E99 and E100 to E101.

Memory Bus Selection Add jumpers for A bus selection.

5. Interrupt Clock

Set up for interrupt rate of 990 n.s.
Add jumpers between E2 and E3, E4 and E5

6. TTY/CRT

Enable CRT. Delete jumper E96 to E97.
Set up CRT for 1200 BPS and 1 Stop Bit.
Install jumpers as follows:

Add:	E20 to E21	E30 to E31	E36 to E37
	E24 to E25	E28 to E29	E38 to E39
	E26 to E27	E46-E47	E107 to E108
	E48-E49	E113-E115	E44 to E45
	E119-E120		

7. Memory Time-Out Logic

Install jumpers A24-B51, C25 -B49
(Subject to removal due to inconsistencies)

8. PMA

ADD: Jumpers E73-E74, E75-E76,
E77-E78, E79-E80.

Hog Mode: not used
Hog Mode: Delete jumper B27-C27, A27-B27
PMA Memory Request - Jumper B25-C25
B Port is not shared between PMA and CPU.
Add E89-E90

PMA Address
Bits 9-15

Add jumpers: Bn-Cn (n=11, 13, 15, 17, 19, 21, 23

5.3 Console - Refer to 01A1335

1. Control Disable

   To disable all switches, install jumpers between C-E.

2. ABL

   Selectable, no jumpers between A-A, B-B.

3. I-Register Display

   a. Delete Jumper clips:

From	To
E5	E6
E7	E8
E9	E10

   b. Add Jumper clips:

From	To
E4	E8
E5	E11
E7	E10

5.4 Memory Map - Refer to 01A1892

1.	Device Address = 46	Jumper E2-E3
2.	Normal DMA Priority	E8-E18
3.	High Speed DMA Priority	No jumpers to HS DMA, inputs are floating.
4.	Interrupt Enable	Disable interrupt for VORTEX II. Jumper E22-E21.
5.	Key Bit Select	Install jumper clips between E23-E25, E26-E28, E29-E31, E32-E34.
6.	Privileged Instruction Enable	Install clip E35-E36

5.4 Memory Map - Refer to 01A1892 (continued)

7.	Executive Mode Enable	Install clip E39-E40
8.	Memory Request Delay #1	Select jumper for 80 n.s. delay E61-E72.
9.	Memory Request Delay #2	Select jumper for 120 n.s. delay E67-E73.
10.	Memory Lock Out	No Jumper E42-E41, E44-E45, E48-E49, E51-E52, E54-E55, E57-E58.
11.	Memory Lock Bus B	Add jumpers B31-A31
12.	Memory Port Connection	Install jumper for "A" Port. Bn-Cn n = 1-51
13.	Memory Read Back Enable	Install E76-E74.
14.	Key MUX Control	Install E77-E78, E81-E80.
15.	Memory Protect	Install E85-E83.
16.	Memory Expansion Connection	Memory #0 - P1 Backplane Memory #1 - J8-38/37

5.8 Memory Assignments - Refer to 01A1862

a. Memory Address Assignments

Memory Bank #1	0-64KB	(16 Bit)	A2 Slot 1
Memory Bank #2	128-192K	(16 Bit)	A2 Slot 3

b. Memory Bus Assignments - SW Location A1

Memory Bank #1

SW #1 ON:	Selects Memory Done (YDNMX-) from Memory
SW #2 ON: SW #3 OFF:	Selects Port A Memory Request (MRQYA-) P1 Backplane
SW #4 ON: SW #5 OFF	Selects Internal Refresh Memory Request
SW #6 OFF: SW #7 ON	Selects Port B Memory Request (MRQYB-) J1-2

5.8 Memory Assignments - Refer to 01A1862

b. Memory Bus Assignments - SW Location A1 (continued)

Memory Bank #2

SW #1 ON: Selects Memory Done (YDNMX-) from memory

SW #2 OFF: Selects Port A Memory Request (MRQYA-)
SW #3 ON from J1-14 (Map)

SW #4 ON: Selects Internal Refresh Memory Request
SW #5 OFF

SW #6 ON: Selects Port B Memory Request (MRQYB-)
SW #7 OFF: P1 Backplane

c. Modify all memories for "A" Port Priority. See section 9.0, Appendix. (N/A for non-Eagle Systems)

6.0 CONTROLLER JUMPER/SWITCH CONFIGURATIONS

6.2 UASC - 98A0767

Baud Rate	Div. By	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12
1200	120	X	X	X		X	X	X					

X = Add Jumpers

Add Jumpers

*E14 One Stop Bit

Delete Jumpers

*E13 Parity Bit Disabled
*E15 & E16 Eight Data Bits Per Character

* Standard

6.3.2 I/O Expander - 44P0670-000

Add twisted pair jumpers as follows:

From	To	
E230	E63	
E229	E64	
E232	E60	- (used for BIC on non-V77
E233	E59	connector planes)
E234	E65	
E235	E66	
E236	E67	
E237	E68	
E240	E69	
E241	E70	
E242	E71	
E243	E72	

7.0 SPECIALS/SYSTEM INFORMATION

7.1 Specials - N/A

7.2 System Information

a. Customer to supply Op-Com Input Device and Cable.
b. PFR will not function without Data Save.
c. Configure per Spec. B-54J0011-14.
d. Memory will be non-contiguous.

7.3 EN 87755-1 and EN 84694 N/A as these systems use "A" Port.

7.4 Memory terminators must be Rev. "B".
REV. "C" will not work (cache fix).

7.5 MAINTAIN III PMA-DMA test will not work under present configuration.

7.6 Add wiring per Wire List No. 95W0319A to Cnassis A3.

8.0 SYSTEM WIRING

8.1 Wiring by Chassis

a. Chassis A2

Standard wiring already installed.

b. Chassis A3 I/O

Delete

All I/O voltage wiring, pins 117-122, from Slot 13 RH;
& all BIC wiring, pins 49, 50, 52, 54, 56, 58 and 60,
between Slots 2 RH and 13 LH and between Slots 5 LH and 6 LH.
All I/O wiring, pins 1-60, between Slots 10 RH and 9 RH.

Add

System Priority

From	To
13 RH-37	2 RH-37
13 RH-34	2 RH-38
2 RH-42	11 LH-37
2 RH-40	11 LH-38
11 LH-42	5 LH-37
11 LH-40	5 LH-38
5 LH-42	13 RH-39
5 LH-40	13 RH-36
13 RH-41	12 LH-37
13 RH-38	12 LH-38
12 LH-42	13 LH-37
13 LH-42	13 RH-42
13 LH-40	13 RH-40

Device Address Wiring

Device	Location	Wiring
PIM #1 DA = 40 IA = 100-117	Slot 12 LH	64-66, 67-69 70-72, 63-74
PIM #2 DA = 41 IA = 120-137	Slot 13 LH	64-65, 67-69 70-72

Device Address Wiring (continued)

Device	Location	Wiring
BIC #1 DA = 20, 21	Slot 11 LH	65-69, 70-72 115-118,
BIC #2 DA = 22, 23	Slot 2 RH	65-68, 70-72 115-118
BIC #3 DA = 24, 25	Slot 5 LH	65-69, 70-71 115-118
UASC #1 DA = 03	Slot 6 RH	64-66, 67-69 71-72, 76-83 77-85, 78-87
UASC #2 DA = 02	Slot 5 RH	65-66, 67-69 71-72, 76-83 77-85, 78-87

PIM Interrupts

PIM #1 DA = 40 IA = 100-117

Signal	From	To	Function
IL04	13 RH-75	12 LH-102	TTY Read
R	13 RH-76	12 LH-101	Complete Ready
IL05	13 RH-77	12 LH- 88	TTY Write
R	13 RH-78	12 LH- 87	Complete Ready

Key Bit Wiring

Signal	From	To	To	To	To
IOK1-I	13 RH-109	2 RH-109	11 LH-109	5 LH-109	4 LH-109
R	13 RH-100	2 RH-100	11 LH-100	5 LH-100	4 LH-100
IOK2-I	13 RH-110	2 RH-110	11 LH-110	5 LH-110	4 LH-110
R	13 RH-111	2 RH-111	11 LH-111	5 LH-111	4 LH-111
IOK3-I	13 RH-112	2 RH-112	11 LH-112	5 LH-112	4 LH-112
R	13 RH-114	2 RH-114	11 LH-114	5 LH-114	4 LH-114
IOK4-I	13 RH-113	2 RH-113	11 LH-113	5 LH-113	4 LH-113
R	13 RH-122	2 RH-122	11 LH-122	5 LH-122	4 LH-122
BIMES	13 RH- 93	2 RH- 93	11 LH- 93	5 LH- 93	4 LH- 93
R	13 RH- 57	3 RH- 57	12 LH- 57	4 LH- 57	3 LH- 57
BTMES	13 RH- 94				4 LH- 94
R	13 RH- 95				4 LH- 95

9.0 APPENDIX

1. PIM External Interrupt Sheet
2. Alternate Ground Pin Chart

PIM External Interrupts

The PIM (1 to 8 AC External Interrupts) are brought into PIM Board via Front Pins or via J1 or J2 "EDGE" connectors on the later model PIM Board.

FUNCTION	FRONT PINS (Both Models)	J1 or J2
IL00-	108	3
R	107	4
IL01-	114	13
R	113	14
IL02-	104	9
R	103	10
IL03-	110	15
R	109	16
IL04-	102	11
R	101	12
IL05-	88	5
R	87	6
IL06-	112	1
R	111	2
IL07-	86	7
R	85	8

NOTE: IL00- is highest priority; IL07- is lowest priority.

Input Levels =	+5V	= OFF	=	No Int.
=	0V	= ON	=	Int.
=	+5V to OV transition	= ON	=	Int.

I/O jumpers for PIM Interrupt Addresses:

100-117 = 74-63, 80 & 106 = Open
120-137 = 74, 80 & 106 = Open
140-157 = 106-74, 74-63, 80 = Open
160-177 = 106-63, 74 & 80 = Open

ALTERNATE GROUND PIN CHART

The following lists gives the pin numbers of all standard ground pins. When wrapping a wire to a ground pin, if the pin already has three wires wrapped to it, use the closest available alternate ground pin. If none available in the same slot, use the closest available adjacent slot (staying in the same connector plane on V77 Chassis).

"U" Connector Plane		"S" Connector Plane		"DCM" Connector Plane		
Slot	J1,2,3,4	Slot	J1, 2	Slot MUX #1	Conn. J1,2	Slot MUX #2
22	1	1	1	1	1	1
24	23	3	2	49	2	41
26	25	5	23	59	23	42
28	27	7	25	60	25	53
30	29	9	27	63	27	59
34	31	22	29	64	29	63
39	33	24	31	65	31	87
41	35	26	33	69	33	101
43	37	28	35	72	35	105
45	39	30	37	76	37	122
53	41	32	39	77	39	
76	43	34	41	78	41	
78	45	36	43	122	43	
80	47	38	45		45	
82	49	40	47		47	
84	51	48	49		49	
88	53	51	53		53	
93	56	53	56		56	
95	58	55	58		58	
97	60	57	60		60	
99		59				
101		122				
103						

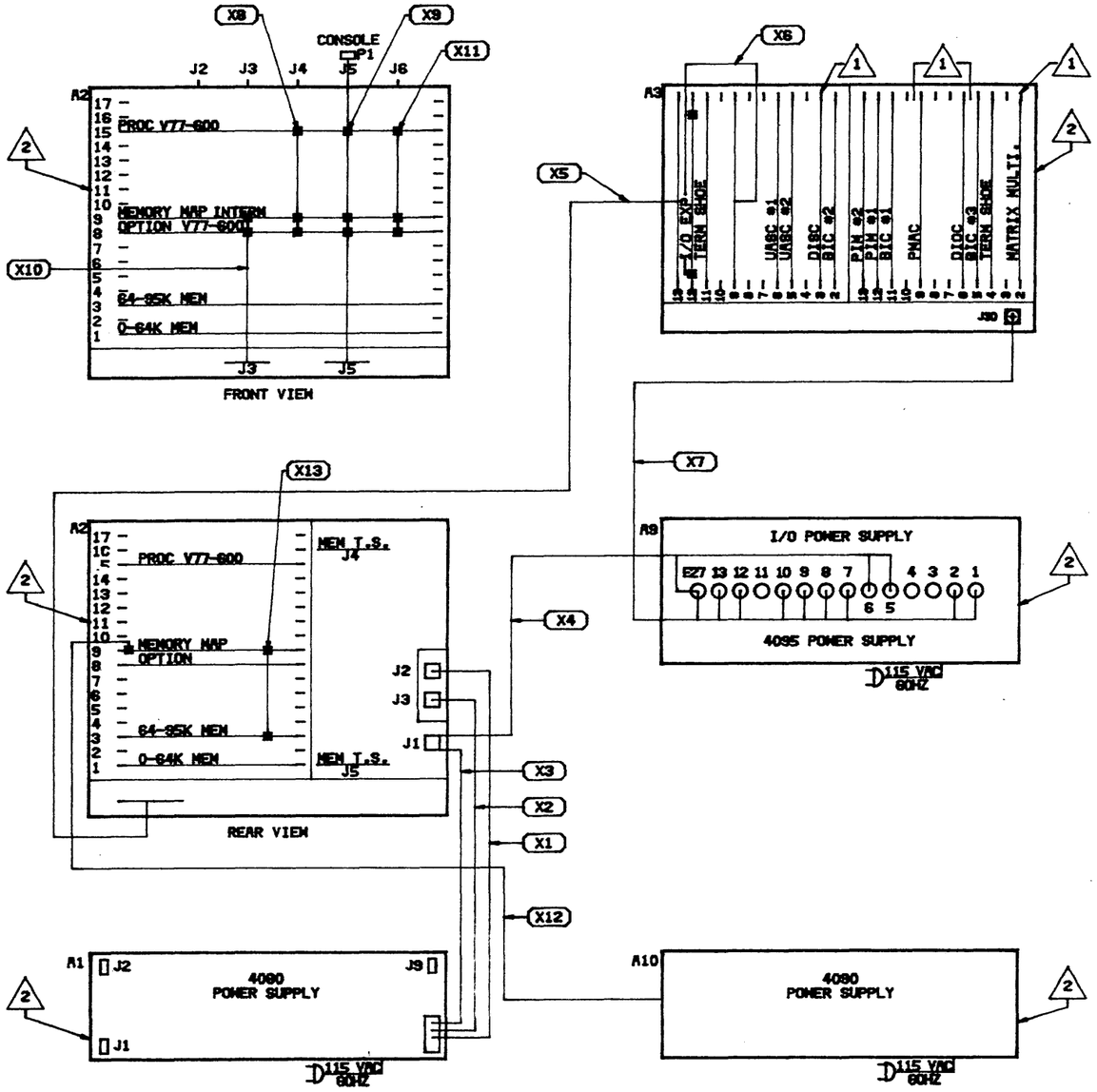
10.0 CABLE IDENTIFICATION

CABLE DESIGN	FROM	TO	PART NUMBER	CABLE LENGTH	FUNCTION
X1	A1 PS	A2 J2	53P0917	48"	DC Power
X2	A1 PS	A2 J3	53P0797	48"	Control
X3	A1 PS	A2 J1	53P0796	48"	Fan Power
X4	A2 J1	A9 +5B1-5,6 & E27	53P0685	Std.	Turn-On
X5	A2J2	A3 RH Slot 13	53P0715	24"	I/O
X6	A3 RH Slot12	A3 RH Slot 9	6600709-00		I/O Expander
X7	A9 PS	A3 J30	53P0686	Std.	I/O Power
X8	A2 CPU J4	A2 Map J4 A2 Option J4	53P0674-025		Opt.
X9	Console	A2 CPU J5 A2 Map J5 A2 Opt J5 A2 J5	53P0807-011		I/O
X10	A2 Map J3	A2 Opt J3 A2 J3	53P0674-031		Aux I/O
X11	A2 CPu J6	A2 Map J6 A2 Opt. J6	53P0674-025		Map
X12	A10 PS	A2 Map J7	53P0872	72"	Map Power
X13**	A2 Mem#1 J1-14	A2 Map J8-38 37	53P0909	18"	Mem. Request
++X14			W5300720-72		PMA Cable

Sheet 1 of 1

**Attention PC: Issue Standard Cable Rework to Modify
++ To ship unconfigured

REVISIONS (CONTROLLING PIC REV LEVEL APPEARS ON THE FIRST SHEET)						
ZONE	LTR	EIR	DESCRIPTION — FOR DETAILS SEE EIR	CHK	DATE	APPROVED



2 V76 EQUIPMENT

1 CUSTOMER SUPPLIED

UNLESS OTHERWISE SPECIFIED			LAYOUT	DATE	CLASS	SPERRY UNIVAC
DIMENSIONS IN INCHES TOL ON						
2 PLACE DECIMALS	3 PLACE DECIMALS	ANGLES	DRAFTSMAN BRENDA RODMAN			TITLE: MCDONNEL DOUGLAS MDEC SPEC B-54J0011-14
± .03	± .010	± 0.5°	CHECKER			
HOLE DIA TOL			ENGINEER R. GARDNER			
0 THRU .250 +.003 −.002	.251 THRU .500 +.005 −.003	.501 AND LARGER +.010 −.005	APPROVAL			SIZE B; CODE IDENT NO. 21101; DWG NO. 6650650
THREADS: EXT CL 2A, INT CL 2B						SCALE NONE; WEIGHT; SHEET 1 OF 2
COMMODITY CODE						

S.O. 432183

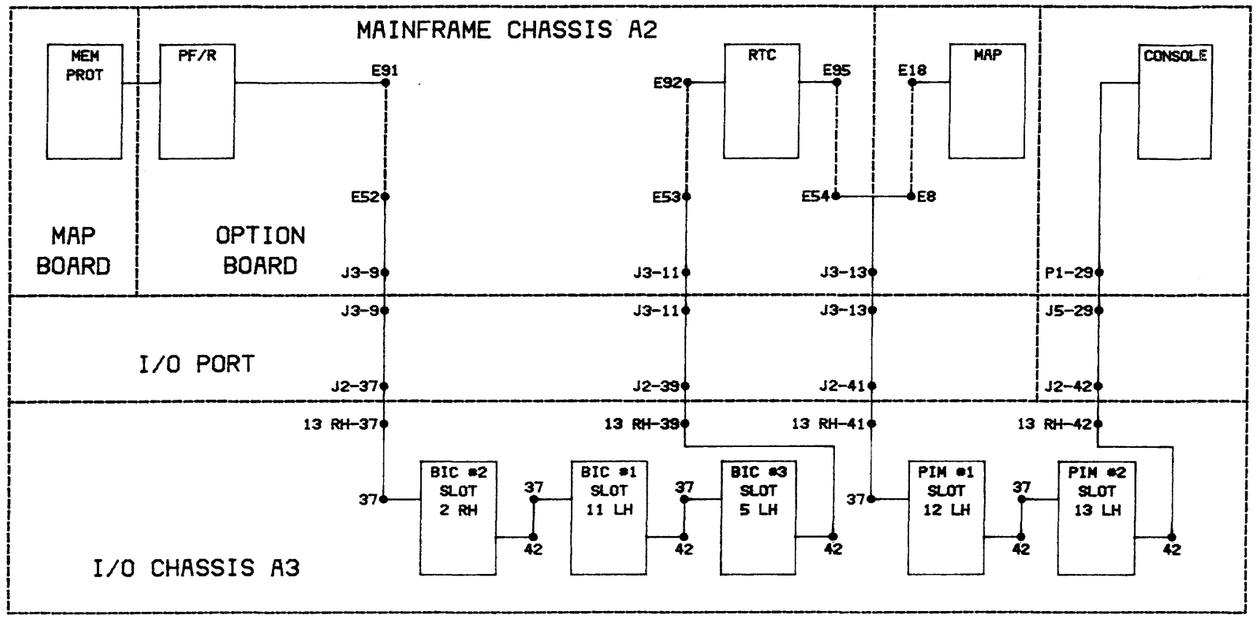
SYSTEM ARRANGEMENT DRAWING

PART NO.
IDENT NO.

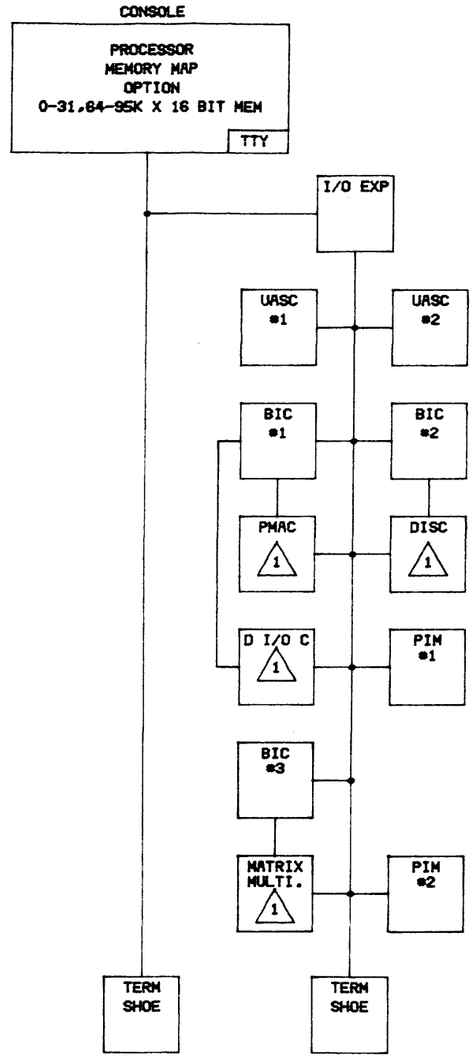
FOR MATL REQUIREMENTS SEE PL.
PL REV LETTER CONTROLS DOCUMENT.

REVISIONS						
ZONE	LTR	EIR	DESCRIPTION — FOR DETAILS SEE EIR	CHK	DATE	APPROVED

4.5 SYSTEM PRIORITY DRAWING



2.0 SYSTEM BLOCK DIAGRAM



S.O. 432183

CLASS	SPERRY UNIVAC		
SIZE B	CODE IDENT NO. 21101	DWG NO. 6650650	
SCALE NONE	WEIGHT	SHEET 2 OF 2	

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